

Proceedings

International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces

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March 14-17, 1999

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MONDAY, MARCH 15

CONTINENTAL BREAKFAST
7 AM - 8 AM

REGISTRATION
7 AM - 6:30 PM

SESSION 1:

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- 011 Development of Solderless Joining Technologies using Conductive Adhesives
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- 016 Characterization of Silver Flakes Utilized for Isotropic Conductive Adhesives
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- 021 Curing Kinetics Study for Designing of Novel Electronic Adhesives
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- 073 **Pre-applied Underfills for Low Cost Flip Chip Processing**
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EXHIBIT OPEN

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ShellCase Ultrathin Chip Size Package

ShellCase, POB 48328, Jerusalem 96251, Israel.

Tel: +972 2 6798890, Fax: +972 2 6798850.

Key Words: CSP, Wafer level CSP, Manufacturing, SMT, Optical Package, Reliability.

INTRODUCTION: The Thinnest Wafer-Level Chip Size Package

As the demand for ever-smaller electronic and optical devices grows, manufacturers are seeking ways to reduce the size and weight of IC. Now a fully packaged integrated circuit can be as small and thin as the chip itself. The Chip Size Package (CSP) is fundamentally changing the way electronic products are being designed. The ShellCase CSP, for peripheral, area array and BGA applications and for optical applications, is distinguished by its ultra-thin profile, its reliability, and its cost-effective wafer-level process.

The Integrated Package:

You can never be too rich or too thin. The same goes for Chip Size Packages. The ShellCase wafer-level packaging process yields completely packaged wafer-level processed devices employing thin film technology that complies fully with JEDEC and SMT standards and can be accomplished with commercial Semiconductor wafer processing equipment.

The Wafer Level technology, produces CSP's that measure 300 to 700 microns in thickness, yielding the thinnest packages on the market for use in Various electronic products where package size is a crucial factor.

Wafer-level manufacturing, achieves economies of scale, flexibility. It also proves to be reliable, the ICs are encased securely in a solid die-size shell.

The package prevents silicon from being exposed and ensures excellent mechanical and environmental protection Compliant bumps provide on board reliability.

Semiconductor Foundries, can incorporate wafer level Integrated Circuits packaging into existing (not longer used) manufacturing lines, basically with the addition of a few processing machines.

The flexibility of the wafer level processing is immense, enabling slight changes in the package configuration that yield a variety of CSP's fit to meet specific needs:

- An area array CSP (Figure 1) -- ShellBGA a CSP ball grid array, with thickness down to 0.5 mm.
- A peripheral leads CSP - ShellPACK for peripheral lead layouts with thickness down to 0.3 mm.
- A transparent package for Electro-Optical applications -- ShellOP (Figure 4)

The wafer level packaging characterizes by the following attributes:

- Miniature footprint equal to the die-size, with standard lead layout

- Fast turnaround for processing new dies
- Flexible manufacturing process reduces redesign and retooling times
- Ease of assembly using conventional SMT soldering techniques
- Low parasitics -- short leads minimize parasitic capacitance and inductance
- Excellent thermal dissipation
- Low cost



Figure 1: ShellCase Chip Size Packages, Shell-BGA Area array lead configuration at 0.5 mm pitch And Shell-PACK Peripheral lead configuration at 0.3 mm pitch.

The ShellCase Manufacturing Process

The packaging is implemented at the wafer level. The integrated circuit device is CSP packaged using semiconductor type manufacturing processes. This manufacturing paradigm offers a standards-based extension of existing IC Semiconductor processes to Chip Scale Packaging.

At the time of the packaging process, the dies are packaged and encapsulated into separate enclosures while still in wafer form. Metallic leads are attached to the individual contact pads by a non bonding method, and the wafer singulation yields finished packaged devices.

The basic steps in this wafer-level manufacturing process are as follows (Figure 2):

1. A thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive.
2. The silicon material between the dies (streets) is etched away (back side), yielding individual IC's attached to the supporting glass layer.
3. The grooves between the dies are filled with an inert material, and a second thin glass cover is bonded onto the silicon dies back side to achieve a complete protective enclosure for each die.
4. An organic layer is applied and patterned to act as a compliant layer underneath the solder joints.
5. Deep notches are drawn between the dies, revealing the cross-sections of the bond pads.
6. A metal layer, patterned by lithography to individual leads, is deposited to contact the bond pads at their cross-sections. Soldering leads are formed on the upper surface of the package. Contacts are plated by nickel.
7. A solder mask layer is applied.
8. For BGA type devices, the bumps are screened and then reflowed at wafer level
9. Wafer dicing yields individual packaged dies.

Wafer level Packaging Cost-Effectiveness

The IC Semiconductor production contends with a technology chasm, laying right in the middle of the IC production line. The Integrated Circuit manufacturing process begins at the wafer level using Thin Film technology. Later, down the production line, mechanical processing of individual die substitutes to the semiconductor technology, to yield the package die.

The procedure of manufacturing and packaging the IC at the Semiconductor plant grants economic and logistic advantages. It allows to skip costly processes such as the wafer probing and sorting, eliminates

overseas shipping of the wafers for packaging. This gives to the IC manufacturer a better control of the whole IC production cycle.

More over, Wafer Level CSP manufacturing brings an economical fabrication process regardless from die size and lead-count.

It enables to package all the dies of the entire wafer at the same time rather than to one die at a time, thus significantly reduces the labor and equipment involved.

In addition, several process steps, can be reduced, such as backgrinding, probing and sorting.

Beyond achieving these economies of scale, the wafer-level technology permits infrastructure and piece parts reductions. There is no longer need for lead frames, molding, trim and form, dice attach, or wire-bonding. Except for a single tool, all equipment is commercial wafer processing equipment (sputter, etcher, dicing saw, etc).

Flexibility

Semiconductor packaging process allows easy and flexible transition from one product to another, by the mere change of a mask set. The three -- five masks processes of the ShellCase manufacturing permit to transfer easily from one package design to another package design, this allows a flexible plant operation, and an easy processing of small volumes.

First years' CSP applications involve multiple small orders of Chip Size Packages. Production line flexibility is essential, in order to deal with small orders, to process simultaneously several different dies, and to handle different pad layout associated to the JEDEC and EIA standards.

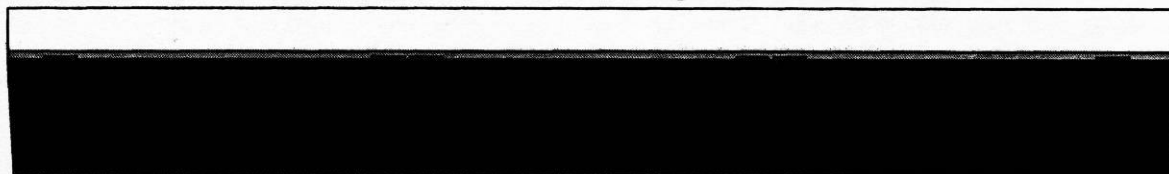
Materials

ShellCase technology accommodates regular production wafers, and uses regular commercial and most often multiple sourced raw materials for the package. These materials are available off the shelf, and the process is not dependent on the supply of special parts or chemicals.

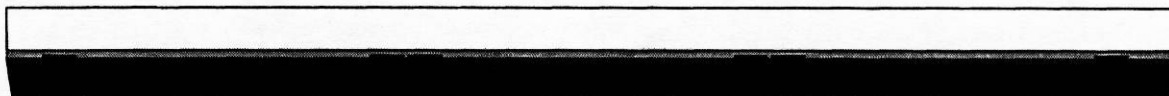
Cost

Wafer Scale manufacturing was widely discussed, advocating for the cost competitiveness of wafer wise processing. Based on current production line data, ShellCase evaluates the processing direct cost to be below \$90 for 6" wafers, at volumes above 250 wafers processed per day.

Figure 2: the Wafer Level manufacturing - Schematical Process Flow



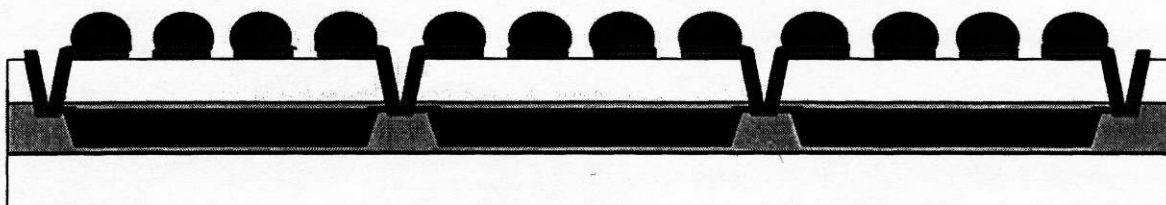
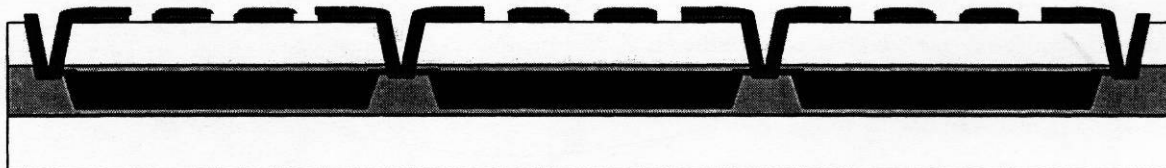
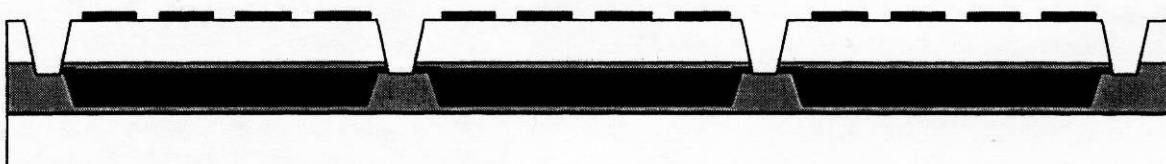
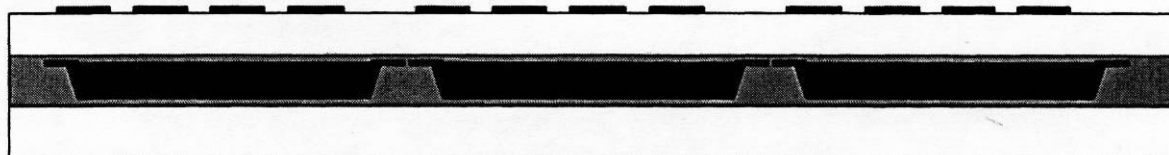
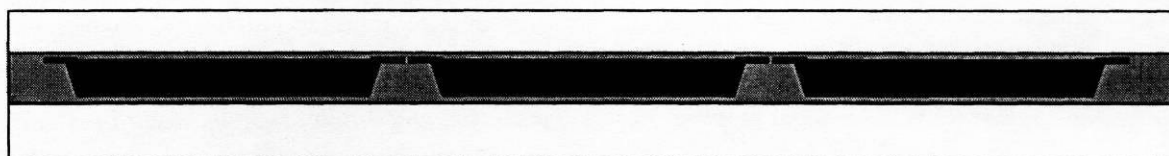
- A. A protective glass layer is attached to the active side of a silicon wafer



- B. The silicon wafer is Back - Grinded to 100 microns



- C. The silicon material between the dies (streets) is etched away



Electrical Features

The ShellCase package has very short leads, resulting in very low parasitic inductance and capacitance.

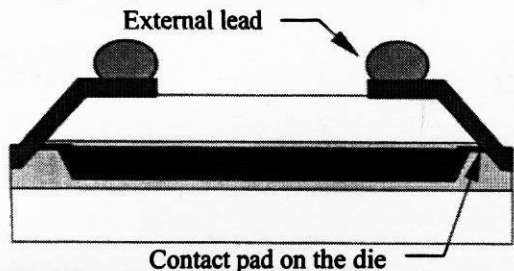


Figure 3: The CSP schematical cross section

Measurements of lead-to-lead capacitance yield an upper limit of 0.07 pF and lead-to-lead inductance of 0.3 nH for ShellPACK. This low lead inductance reduces high frequency delays, improves speed, and attenuates ground-bounce.

Thermal Dissipation

The CSPs thermal dissipation has been measured using a dedicated test die comprising both a resistive heater and miniature thermometers monitoring the internal die temperature. Thermal dissipation measurements yielded a θ_{JA} as low as to 40°C/W without heat sink, in still air. The efficiency results from the short thermal path for heat transfer through the thin glass layer.

ShellCase Specialty Applications

ShellCase offers CSP packaging solutions for several specialized applications:

- ShellPACK -- CSP for peripheral lead layouts
- ShellBGA -- CSP for area array leads layout
- Smart card applications with ultra-thin, breakage-resistant, and enhanced security feature;
- Integrated passives where size is a key factor.
- Radio applications that can benefit from low parasitics of the ShellCase CSP and the unique ability to integrate metal structures on the package.
- ShellOP, for optical solid state detectors and Imagers, including Silicon light detectors, CMOS image sensors, and CCD devices.

The Optronic CSP

The glass transparent package encases the Imager Die in a solid protecting optically clear enclosure (Figure 4).

The package has special features both in relation to conventional Opto-Electronic packaging and Chip Size Packaging.

- Transparent Chip Size Package.
- Ability to integrate absorption or interference (dichroic) optical filters into the package, to control the light spectral response of the packaged die.

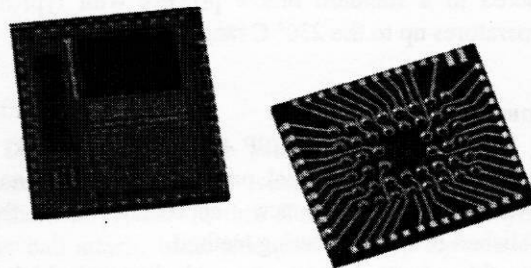


Figure 4: Photobit PB0159 CMOS Active Pixel Image Sensor packaged in the Shell-OP Optronic CSP

Reliability

ShellCase packages are subject to a rigorous battery of reliability tests for Thermal Cycling, Humidity (THB, PCT, Popcorn), endurance, as illustrated in the table below.

ShellCase Reliability Results -- September '98				
Test	Conditions	Chip size Criteria	Fail	Comments
Temp Cycling	-25 +125°C 30 cycles/day	7 x 7 mm 1000 Cycles	0/22	BGA on PCB
Temp Cycling	-25 +125 °C 72 cycles/day	2 X 4 mm 1000 Cycles	0/77	BGA On PCB 0/77 Unmounted
TH	85°C/ 85% RH No bias	2 X 4 mm 1000 hours	0/77	BGA Unmounted
THB	85°C; 85%RH; 5V Bias	2 X 4 mm 1000 hours	0/77	BGA on PCB
Storage Bake	150°C	2 X 4 mm 1000 Hours	0/77	BGA Unmounted
HTOL -DLT (Dynamic Life Test)	125°C	2 x 4 mm 1000 Hours	0/77	BGA (8 Leads) On PCB
Moisture Level 2	85°C, 60% 3 reflow 220°C	2 x 4mm 168 Hours	0/77	BGA
Pressure Pot	2 atm, 121°C	96 hrs	0/84	BGA
HAST	110°C 85% RH	2 x 6 mm 500 Hours	0/77	BGA

Solderability

ShellPACK (with a minimum 0.3 mm peripheral lead pitch) and ShellBGA (0.5 mm) are soldered to a printed circuit board by a regular SMT process. The leads are nickel gold-plated. Shell BGA is available at standard JEDEC pitches down to 0.5 mm, with bump material of SnPbAg. Both configurations can be soldered in a standard reflow process with typical temperatures up to the 230° C range.

Summary:

The spreading wave of CSP technologies, break a breach in the conventional packaging wisdom, and provides challenging new approaches to the established IC manufacturing method.

Faster throughput, lower costs, and ultimately higher yields will be the long range driving factors for the adoption of wafer level CSP, based on Semiconductor processes.

Wafer Scale thin film technology demonstrates the next step in Chip Scale Packaging, specific CSP's tailored for exact fit to the IC market segmentation. The ShellCase technology provides specialized products and configurations both the Smart Cards, the Opto-Electronic and the RF/ Microwave applications.

REFERENCES:

1. ShellPACK a Thin Chip Size, Integrated Circuit Package, Semicon West, CSP session, June 1996.
2. ShellBGA a Thin Chip Size Integrated Circuit Package, ISHM Workshop on CSP, August 1996.