Backside illuminated (BSI) complementary metal-oxide-semiconductor (CMOS) image sensors

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4.1 Introduction

The first backside illuminated (BSI) sensors were introduced by the scientific community in the mid-1970s. The main driving force was their superior quantum efficiency (QE), especially in the UV and the blue spectrums. These sensors were produced in low quantities and with poor yields. Today the innovation in image sensor technology is driven by mass market applications. BSI technology was proven useful for coupling light into pixels smaller than 2 μm commonly used in every smart phone. This chapter is devoted to a review of BSI technology and focuses on its application for the high-end market.

In this section we describe briefly the challenges for scaled down pixels in a modern complementary metal-oxide-semiconductor (CMOS) image sensor chip. We review various technologies used to overcome these challenges and show why BSI is the most natural solution for such sensors.

CMOS image sensors (CSIs) consist of an array of light-sensitive pixels. Each pixel consists of a photodiode (PD), which is the light-sensitive element, and several control transistors. The PD collects and stores the photo-carriers while the control transistors are used for setting the exposure time, transforming charge to voltage, and for readout control sequence. The pixel array is connected to the control circuit by several metallization layers. Each metallization layer is separated by inter-dielectric material. The interface between the chip and the outside world is the passivation layer which is placed above all the metallization layers and isolates the chip from environmental hazards.

In a frontside illuminated (FSI) sensor (see Fig. 4.1A), the light reaches the PD active region through the passivation, metallization, and inter-dielectric layers. Several are the loss mechanisms associated with the coupling of light from the frontside of the sensor. First, the reflection of light from the passivation layer, second, the reflection of light from the metal control lines which surround the PD, and third, the shift

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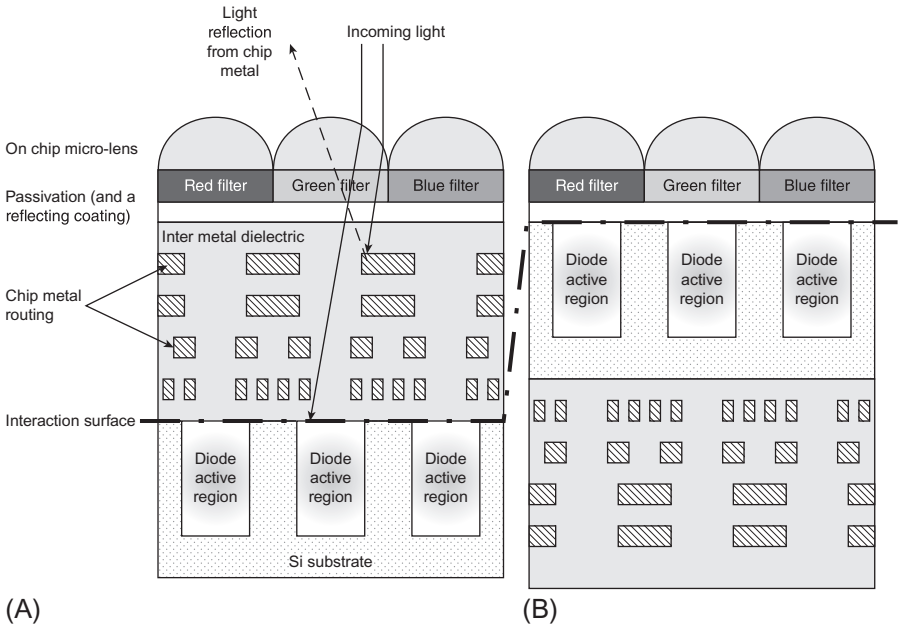


Fig. 4.1 Illustration of (A) frontside vs (B) backside illuminated sensor.

and reflectance of light coming from large angles to the sensor, especially at the edges of the sensor. This angled light travels through the thick inter-dielectric layer and it may be collected by a neighboring pixel. These three mechanisms cause reduction in the maximum available photons or in other words, QE reduction, and contribute to large cross talk, and as a result, reduction of the sensor's signal-to-noise ratio (SNR). Moreover, the stratification of the different layers above the PD can cause a chip nonuniformity which leads to a difference in the light collection from the edges to the center of the image sensor.

A BSI sensor contains the same components as a FSI sensor but the sensor's metals are located behind the PD (see Fig. 4.1B). During manufacturing the wafer is flipped upside down so the metallization and passivation layers are now located beyond the PD with respect to light. The manufacturing of such a sensor is highly complicated since it requires processing steps from both sides of the wafer. The main technological challenges associated with BSI are bonding of the wafer to a holding wafer and then thinning of the original wafer to a thickness of a few microns. In addition, there are also some issues related to the optimization of the sensor's optical and electrical performance, such as inherent large color cross talk, which degrades the image quality, and excess dark current coming from the additional interface. In the past, these problems prevented the mass market manufacturing of BSI sensors. Consequently, until recent years, BSI was in use just in niche high-end markets where low-light performance could not be compromised.

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4.2 Challenges facing a scaled-down FSI sensor

The typical back-end scheme of a CMOS image sensor is shown in Fig. 4.2A. It is very common to design a sensor that uses three layers of metal in the pixel array area, and four in the periphery (digital and analog circuitry). The passivation layer is typically composed of oxide and nitride layers and is located above the last inter-dielectric layer (dielectric four, in the case of a four level metals scheme). The red, green, and blue polymeric filters, which are responsible for the color reproduction of the images are located above the passivation layer (a single pixel without a color filter can only provide monochrome information). The micro-lens that is supposed to direct the light into

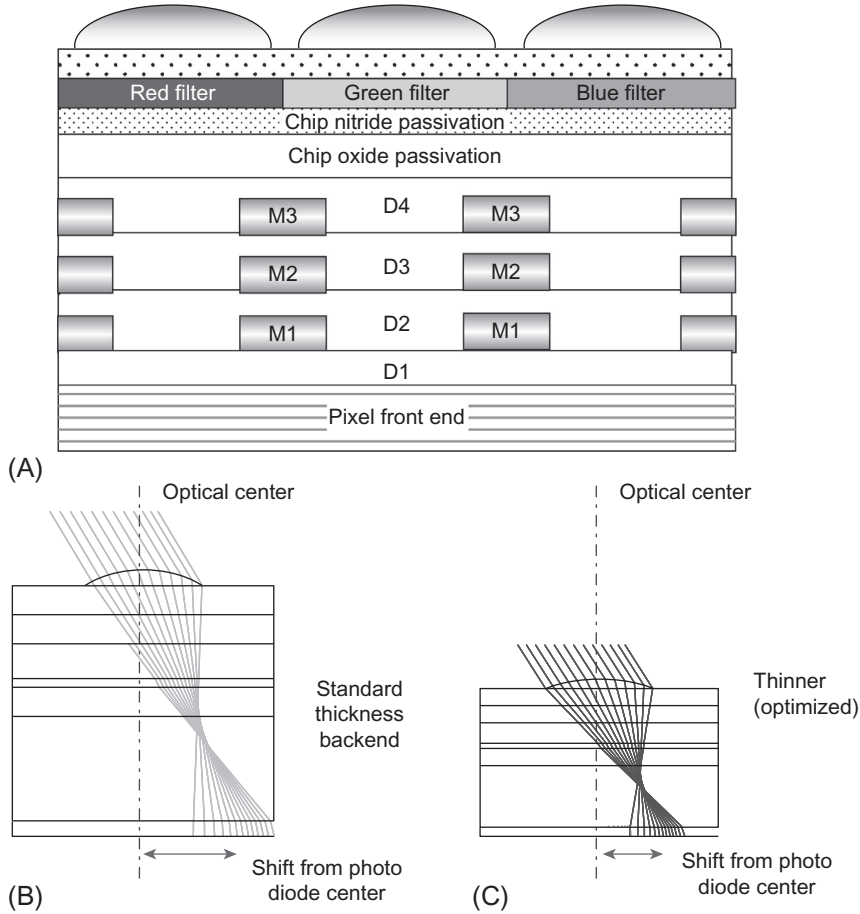


Fig. 4.2 (A) Simplified schematics of a pixel metallization backend, (B) illustration of the optical power shift for angled light rays for a standard CMOS backend, and (C) illustration of the optical power shift for angled light rays for an optimized CIS backend.

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the PD is located above the color filter. There are two fundamental problems that prevent light that hits the micro-lens from reaching the PD active region:

1. The physical size of the aperture on the first metallization that the light encounters (the last metal). For a small pixel, this aperture is rather small unless an advanced metal routing technology is used. If the aperture is not large enough or if the micro-lens is not strong enough, the light will reflect back and will effectively be lost.
2. The light reaches the micro-lens with a wide angle due to the aperture of the system lens. If the optical path from the bottom of the micro-lens to the diode is long, the light can easily reach a different pixel and cause a severe cross-talk problem.

The main optimization techniques traditionally used to solve these problems were improving the micro-lens performance (power) and reducing the total height of the metallization backend. The ability of the micro-lens to increase the number of photons available for detection becomes much more efficient when the micro-lens is placed closer to the active region of the PD. The difference between a pixel with thinner metallization and inter-dielectric compared with a pixel that uses standard metallization is shown in Fig. 4.2B and C. The simple ray tracing illustration shows that a micro-lens that is placed over a thinner stack can focus light closer to the center of the diode than the same micro-lens placed over a thicker metallization backend.

A larger optical opening above the PD is key for achieving higher QE and better angular response. It can be achieved by using narrow control lines for the pixel. A pixel designer would use (in most cases) the narrowest line width that could be manufactured in a given set of fabrication tools. Therefore, moving from one pixel generation to the next (smaller pixel) will by definition require also moving to a smaller technology node. This approach was dominant for many pixel generations and thus, the technology node used for CIS moved from 0.5 μm down to 0.18 μm (Agranov et al., 2005).

For the 0.13-μm CMOS process node, the metallization is replaced by copper. The main reason is that copper allows higher current density and therefore narrower and thinner lines compared to aluminum. The image sensor industry does not use high current densities for the pixel control lines but could use the narrow and thin copper line for widening the optical opening above the PD. The copper inter-dielectric layers are also thinner and the total height of the backend can be reduced compared to an older generation of the fabrication process.

On the other hand, unlike the natural adoption of advanced aluminum process nodes for image sensor fabrication, moving to a copper backend created a major challenge for CIS. The main challenge is that during the fabrication of copper lines, there are alternate nitride and oxide layers for the inter-dielectric layers (Edelstein et al., 1997). The alternating dielectrics with different permittivity cause light in a certain wavelength to be reflected just like light hitting an interference filter. Thus, in order to use a copper back end for image sensors, the nitride layers in the optical path to the silicon surface have to be removed (Cohen et al., 2006). The immediate result is that shrinking pixel dimensions could not be done just by moving to a more advanced fabrication node, and the gap between the modern image sensor process and standard logic fabrication becomes wider.

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For fabricating CIS with pixel sizes below 3 μm, creative solutions and nonstandard backend modules were developed. One example is recess of the metallization stack above the pixels array (Adkisson et al., 2010). This starts by designing a pixel using only two metal lines for operation, with an opening as large as possible above the diode. This task requires either a very advanced fabrication process (90 nm and below) or development of an additional module of a local interconnect metallization below the first metallization layer (Rhodes, 2008). In this solution the array periphery is still being designed by using four levels of metallization. The inter-dielectric layer between the last metal and the second metal is then selectively etched over the pixel array area. The result is that color filters and micro-lenses are placed very close to the top metal of the pixel (second metal) instead of the top metal of the sensor (fourth metal) and this significantly increases the pixel performance, especially for angled light.

Another example is the "light pipe" solution (Gambino et al., 2006; Agranov et al., 2009) which is illustrated in Fig. 4.3. A "light pipe" (or "light guide") is fabricated by

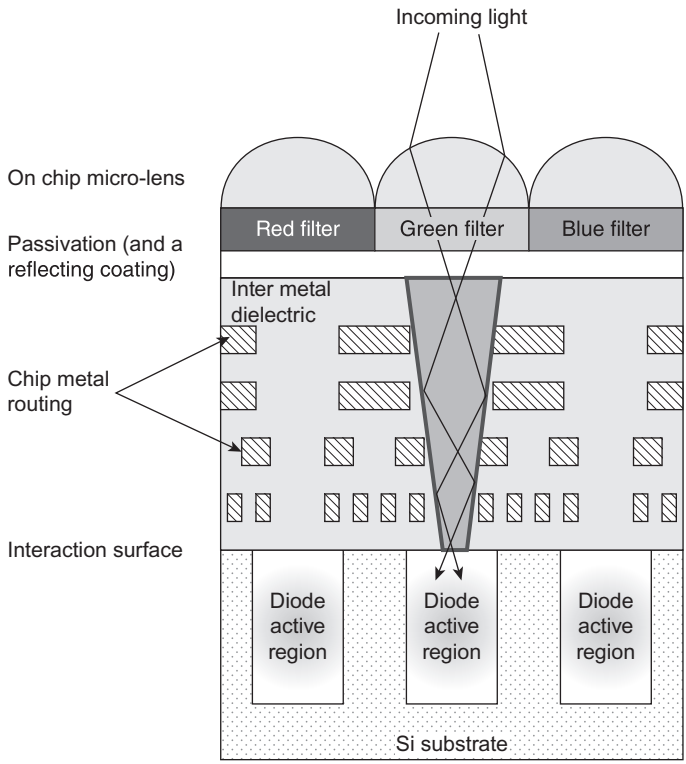


Fig. 4.3 Illustration of the light pipe concept. Deep vias etched through the inter-metal dielectric layer above each diode. The vias are filled with a slightly higher refractive index than their surroundings. The μ-lenses are modified to ensure good coupling of the photons into the light pipe. Due to the higher refractive index in the pipe, photons are guided from the chip top surface to the diodes.

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etching a deep via from the passivation layer down to the diode surface. After the etch process, the via is filled with spin on glass (SOG) (Reznik et al., 2008) or with a special polymer having a high refractive index (Gambino et al., 2007). These three-dimensional structures, if designed properly, can trap the light beams inside the light pipe thus reducing or even eliminating completely the color cross talk. There are many obstacles for successfully integrating light pipes into a reliable sensor; the most significant ones are the relatively high aspect ratio etch with uniform depth over many millions of pixels passivation of the pipe walls, and filling the pipe with high refractive index material. This process is not scalable, namely, each pixel pitch will require a different etch recipe and sometimes a different fill recipe as well. Thus, for each pixel generation, this process will require re-optimization.

In Fig. 4.4, there is a good example of optical path optimization made by Aptina. The chip was taken out of a Lenovo phone and was analyzed by Chipworks (Chipworks, 2012). The chip was fabricated using 65 nm copper metallization. The tight metallization enables pixel routing using only two levels of metals. In addition to the recessed backend, Aptina also used light pipe technology to reduce the optical cross talk even further. The light pipe etch serves also for removal of the nitride-oxide-nitride layers which comes as a standard at this process node.

In the previous paragraphs we showed the enormous efforts invested by different companies in coupling the light into the pixel; thinner and nonstandard metallization backend processes to decrease the optical path, light guides, and a recessed backend.

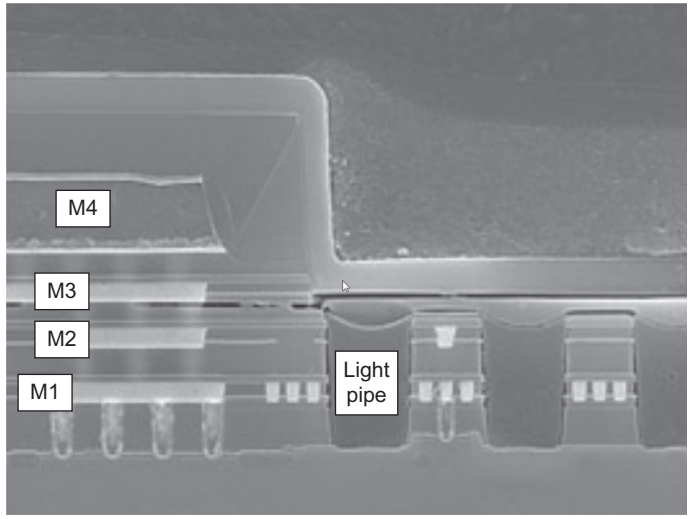


Fig. 4.4 An Aptina sensor taken from a LENOVO phone (courtesy of Chipworks, 2012). The sensor is fabricated using a Cu backend. There are two levels of metals in the pixel array and four levels of metals in the array periphery. In addition to the recessed backend, Aptina is using a light pipe to improve the pixel optics. The light pipe also solved the potential reflectance issue coming from the nitride-oxide-nitride interference by etching them away during the light pipe etch.

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These solutions needed re-optimization over and over again for each new pixel dimension.

The alternative approach is to try to couple the light from the back side of the sensor. This approach could in principle save the effort of customizing the backend process and allow using advanced CMOS fabrication technology. The other benefit from BSI is an increased QE due to optimization of an antireflecting coating (ARC) layer. This led many market leaders to seek a wafer-scale BSI process that is compatible with modern fabrication tools (unlike the BSI process which was used for scientific applications and other niche markets). In 2007, OmniVision (OVT) was the first to introduce a BSI 5 mega-pixel sensor for the cellular phone market.

4.3 Basics of BSI sensor process integration

Typical integration scheme of a modern, wafer level BSI sensor was presented by Wuu from TSMC and Rhodes from OVT at IISW 2009 (Wuu, 2009; Rhodes, 2009). Their flow is illustrated in Fig. 4.5. The flow used by others is similar in principle but each sensor manufacturer takes somewhat of a different approach to solve the same physical problem. Most of these flows were developed with small pixel dimensions in mind. But other sensors with relatively large pixels, such as the ones used for cinematography, or UV-sensitive sensors for machine vision or medical applications, could also benefit from wafer level backside illumination process. These special sensors are less cost sensitive but still can benefit from modern, high yield, processes. In this section we review the most common technique to integrate the full sensor and the common difficulties that can arise at each process step. The impact on the pixel performance is discussed as well.

4.3.1 Starting material selection

The sensor fabrication process begins by starting material selection. This is a very important technological choice which will have many integration consequences in later fabrication steps. OVT and TSMC chose to start with a P on P+-doped wafer. The P on P+-doped wafer is available with a proven supply chain, relatively cheap and widely used in the CIS industry for FSI devices. The other choice is to use silicon on insulator (SOI) wafers (Pain, 2009) which were used, for example, by Sony in an early BSI process generation (Iwabuchi and Maruyama, 2006) and by TowerJazz for devices targeted at high-end markets (Edelstein et al., 2011). The main advantage of SOI substrates over bulk material is that the buried oxide (BOX) of the SOI acts as a built-in etch stop layer as well as a protection to the active silicon layer during the backside thinning process as it is discussed in detail later. The main disadvantages are the cost and availability of such wafers, compared to bulk wafers which make it less (Getman et al., 2007) attractive for high volume production for the mobile phone market.

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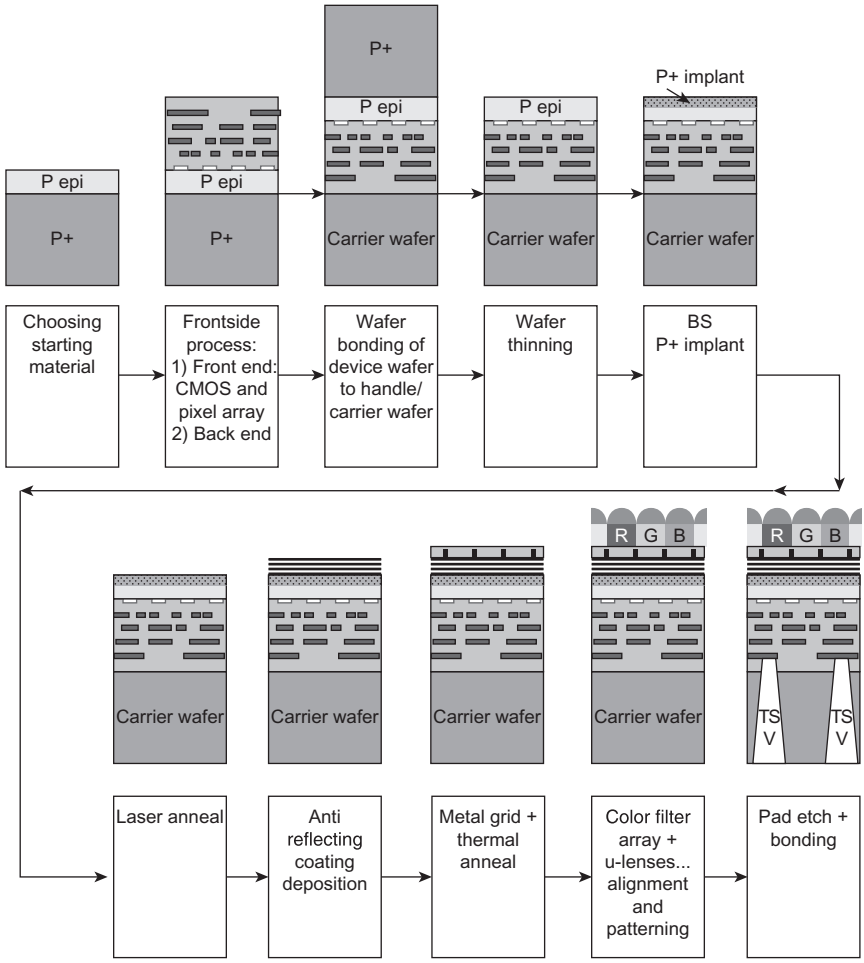


Fig. 4.5 Typical BSI complete process flow (inspired by TSMC and OmniVision from IISW 2009 (Wuu, 2009; Rhodes, 2009)).

4.3.2 Frontside processing

Next is the frontside processing of the image sensor. This stage is very different from one sensor manufacturer to another. Each company has chosen a different technology node to fabricate the frontend and uses a different set of manufacturing tools. Nevertheless, there are many similarities which come from identical optimization targets of the BSI pixel design. One of the main physical limitations, which are inherent to a BSI sensor, is that light is absorbed far from the PD and the resulting photoelectron may diffuse and be collected by an adjacent pixel. This is illustrated in Fig. 4.6. The increased electrical cross talk reduces the modulation transfer function (MTF) for monochrome sensors and degrades the post color interpolation SNR (Yadid-Pecht

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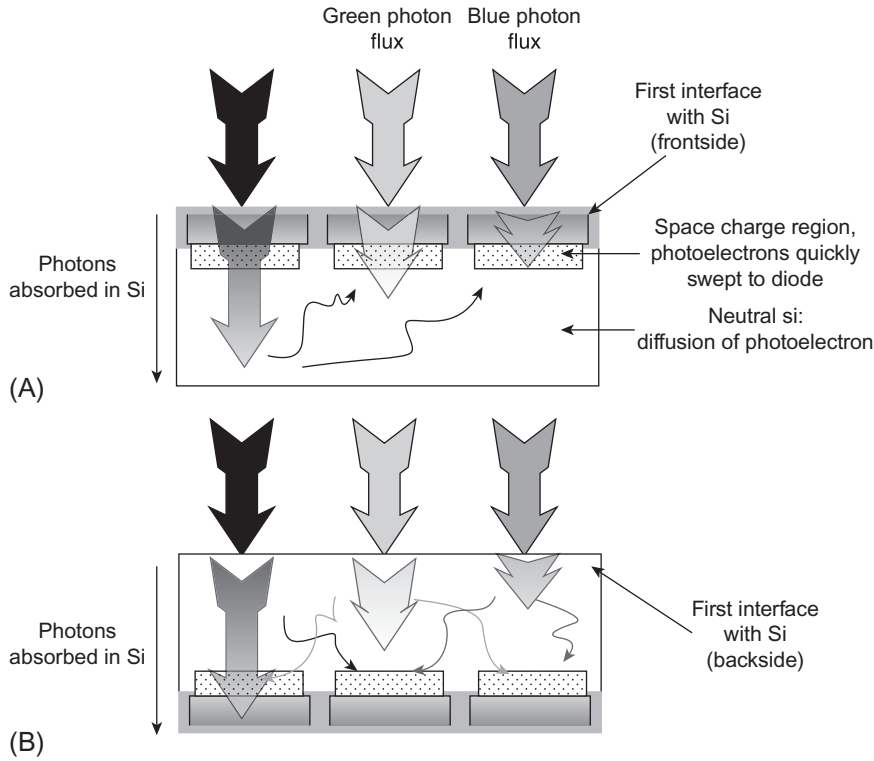


Fig. 4.6 Illustration of photon absorption in FSI pixel compared to BSI.

and Etienne-Cummings, 2004). This is also a known problem on FSI devices but in the latter case, it is limited to red photons which are absorbed deep below the PD (Shah et al., 2003; Tournier et al., 2011). In BSI pixels, the problem becomes severe since a significant amount of green photons ($\lambda = 550$ nm, ~30% absorption in the first 0.5 μm) and the blue photons ($\lambda = 470$ nm, ~70% absorption in the first 0.5 μm) are strongly absorbed (Nakamura, 2005; pveducation, 2014).

The optimization path taken by OVT in solving this problem was to create the diode implants much deeper than the ones used for the FSI device. This same route was also reported by ST Microelectronics (Michelot et al., 2011) who reported implants energies of at least 800 keV and for some cases, even more than 1 MeV, to create the deep diodes which are suitable for green photoelectron absorption. The main problem in using this method is the difficulty to achieve fast transfer of electrons from the deep diode to the sampling node which causes increased noise, image lag and nonlinear response at low illumination levels. An alternative similar solution is to use a deep P+ implant to try to isolate the diodes (Prima et al., 2007). Two further alternatives which rely on deep implants raise additional problems such as the difficulty to anneal the silicon defects which are caused by the high-energy implants. These defects, without a proper anneal, may cause high dark current (DC) and

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blemish. As is very well known, proper anneals require a long, high-temperature process that is not compatible with modern CMOS technology nodes.

For companies that choose SOI as their starting material there is an additional problem to solve during frontend fabrication. One of the most fundamental problems that were solved in the early days of silicon imagers was gettering of the metal elements during fabrication (Prima et al., 2007; Reiner and Coppen, 1978). A P/P+-doped wafer usually contains oxygen precipitates in the P+ layer and even heavily doped polysilicon on the backside of the wafer. These well-known methods are used to getter or "capture" the metal atoms far away from the diode collection area. Sensors manufactured without this gettering technique (or others) will produce images that exhibit very poor performance in the dark due to dark current generation, centered around the metal atom. However, when producing the image sensor on an SOI substrate, these known methods cannot be used because heavy metals cannot pass through the buried oxide film. Therefore, the oxygen precipitates or polysilicon layer on the backside of the wafer cannot prevent heavy metal contamination near the active region of the PD and are basically useless. A different and new gettering method for heavy metals, suitable for pixels in SOI is required.

There are many published techniques for achieving good gettering in SOI substrates. We usually classify the techniques into three groups:

1. The "local gettering" technique that relies on local gettering centers in close proximity to the pixel active region (Teranishi, 2012; Chepis et al., 1997). Implementation of this technique is achieved through modifications to the front-end flow.
2. The "vertical gettering" technique which relies on gettering centers created in the epi active region or in some cases in the silicon substrate (Capedelli, Di Turi, and Faralli, 2006a).
3. The "post process" technique which relies on (i) creating gettering centers after bottom oxide removal, (ii) special thermal treatment which moves metallic atoms into the gettering centers, and finally (iii) removal of the damaged layer (Uya et al., 2010).

We briefly point out two examples of these techniques which emphasize the severity of the problem and the efforts needed to successfully solve it. The first example of "vertical gettering" is from Sony in a 2010 patent (Takizawa, 2009). Sony suggests using gettering centers on the SOI substrate part. A path for the metal contamination in the active epitaxial layer to the silicon is created by damaging the SOI oxide layer which separates the epitaxial from the Si substrate. Implementation of such a technique requires very strong cooperation of many parties including SOI and epitaxial layers vendors. Another profound change to a standard front-end process can be found in a "lateral gettering" example which was patented by ST Microelectronics in 2006 (Capedelli et al., 2006b). Here, ST Microelectronics suggests gettering the metallic atoms in polysilicon filled deep trenches. The patent application does not specify where this gettering center should be placed, but a similar module was already reported (Tournier et al., 2011) by ST Microelectronics in their 1.4 μm FSI pixel technology. The extra process modules are added immediately after the shallow trench isolation is completed and use 45 nm photolithography and etch tools. The aspect ratio for the etched trench is higher than 1 to 25. ST Microelectronics reports that special passivation was used on the deep trench isolation (DTI) walls before gap filling, in order to reduce DC to the level of the DC achieved without the DTI. To conclude this

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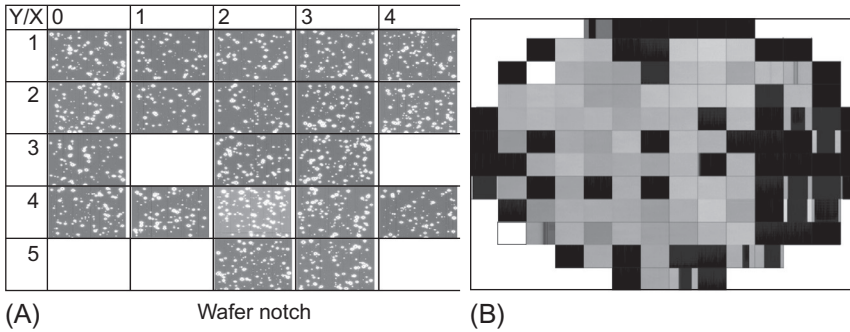


Fig. 4.7 Dark image taken from a full wafer with BSI sensor manufactured by TowerJazz (A) gray image wafer map for early process version with no proper gettering technique and (B) gray image wafer map for process which includes gettering technique.

subject, in Fig. 4.7, gray level images (50% saturation at 30 fps) taken at wafer level for two different BSI products which ran at TowerJazz on SOI starting material are illustrated. In Fig. 4.7A the process does not include a special gettering process and exhibits many bright points. Clean images can be seen in Fig. 4.7B for an optimized gettering process.

4.3.3 Bonding

The next process step, taken after finishing the frontend flow including all of the metallization layers, is the bonding of the device wafer to an additional handling wafer. Bonding is a crucial step which is required in order to supply mechanical support for the next steps of fabrication. Direct bonding of two wafers requires stringent control of surface properties like micro-roughness, wafer flatness, and surface chemistry. The main parameters which are affected by poor control of wafer uniformity and flatness are voids in the boundary interface, mechanical stress imposed on the device wafer which can easily cause alignment errors in the subsequent fabrication steps, and bonding strength and reliability (Gaudin and Riou, 2010; Lagahe-Blanchard and Aspar, 2009; Blanchard and Radu, 2011). Fig. 4.8 illustrates a modern wafer to wafer bonding technique known as direct bonding^{TM} from Ziptronix (Blanchard and Radu, 2011; Enquist, 2012). In this method, the device wafer and the handling wafer surfaces are cleaned using special chemical mechanical polish (CMP) and then plasma activated. The actual bonding occurs when the two surfaces are placed one on top of the other.

4.3.4 Wafer thinning

After bonding, the wafer is flipped and ready for the next process flow on the wafer backside. The first process on the backside is wafer thinning. The quality of the thinning has a direct impact on the overall performance of the BSI sensor and is considered one of the most important challenges of BSI integration. In the case of an SOI wafer

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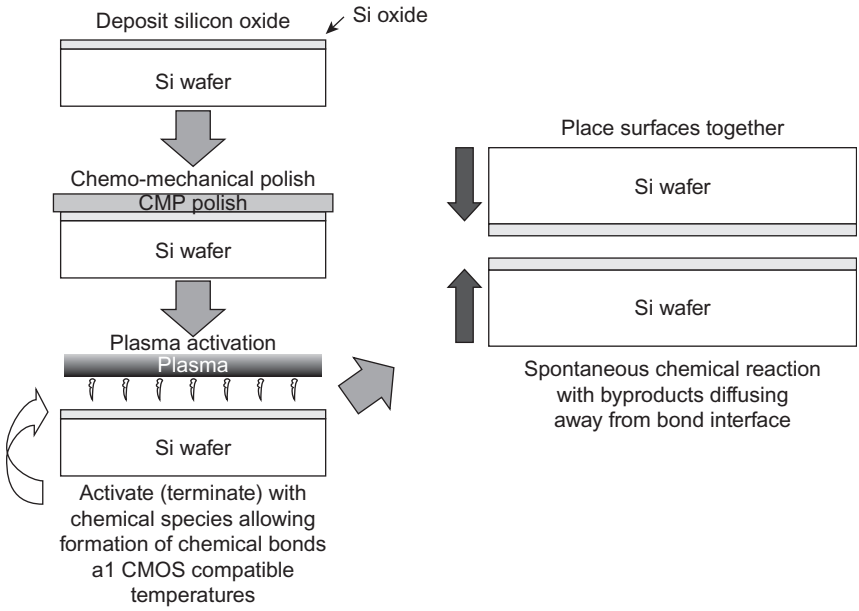


Fig. 4.8 Modern wafer-to-wafer bonding (ZiBona process flow). Taken from Ziptronix presentation (Direct Bonding TM).

being chosen, the wafer thinning is quite simple and involves removing the silicon and stopping on the BOX. Immediately after, the BOX itself is removed (now the active silicon is used as an etch stop) and the wafer is ready for the next steps of fabrication. These steps are well described in Fig. 4.9.

The simplicity of the wafer-thinning step in the case of SOI is the main reason for choosing this starting material over the P/P+ standard wafer since thinning of a P/P+ wafer is very challenging. In such case, there is no etch stop layer and thus, one of the most common thinning methods is to use the concentration difference between the P and P+ layer as an etch stop interface. The final silicon thickness after thinning target is between 2 and 3 μm, for pixel sizes under 2 μm, so the thinning of a P/P+ wafer usually starts with mechanical grinding from initial thickness of about 700 μm down to 20 μm, and only then comes the special etch, that removes the silicon to the final thickness target. In Fig. 4.10, the etch rates of an hydrofluoric-nitric-acetic (HNA)-based solution is plotted versus the doping level of a bare silicon wafer. It can be seen that the etch rate is negligible until a doping level of 10^{18} cm^{-3} atoms. The doping concentration of the P active layer of a P/P+ wafer is in the order of 10^{15} while the P+ concentration level is in the order of 10^{19}. This, in principle, should supply enough margins for thinning process control.

In practice, there are many practical problems with utilizing a good wet etch thinning. The first problem is the out diffusion of the boron from the P+ layer to the P active layer. At the start of the frontend fabrication process, the boundary of the P+ and the P layer is well defined and controlled by the wafer manufacturer. But this clear boundary becomes somewhat fuzzy since, during the frontend processing, there

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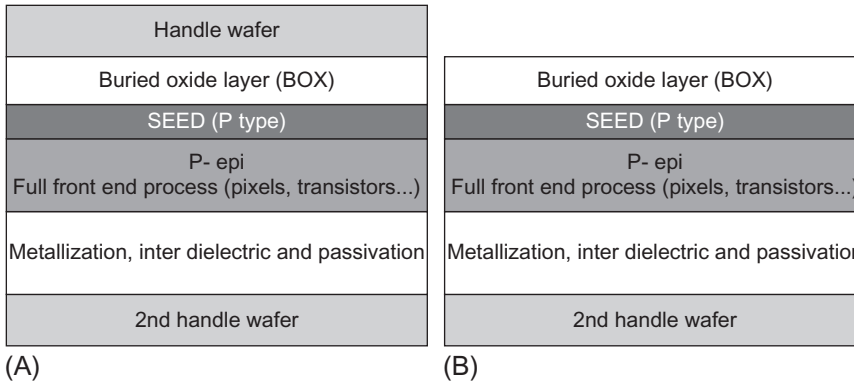


Fig. 4.9 (A) SOI wafer after wafer bonding and flipping and (B) SOI wafer after removing the first handling wafer and stopping on the SOI bottom oxide.

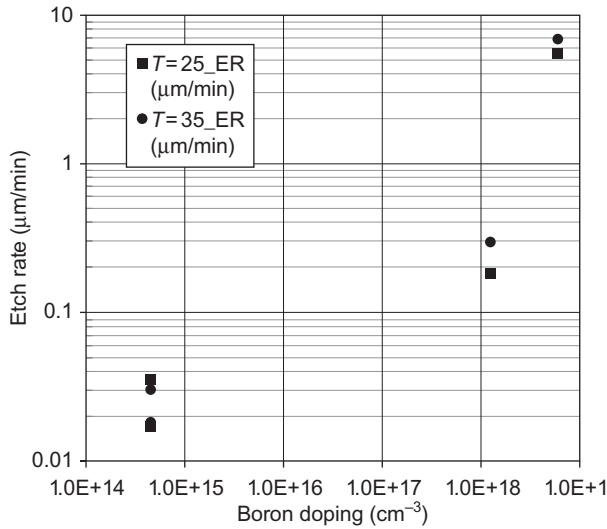


Fig. 4.10 Etch rates differences with respect to the doping level of a bare silicon wafer.

are many long high-temperature anneals that drive the boron from the P+ layer into the P layer. As a result, when the thinning step arrives, there is no longer a clear boundary that can serve as an etch stop mechanism. The second problem is that the edges of the wafer are exposed to the etchant from both the top of the wafer and from its side. This causes an increased etch rate in the wafer periphery compared to its center. In Fig. 4.11, a picture of a 200 mm wafer that was etched without any edge protection is shown. It can be easily seen that the active silicon is fully etched at the periphery. Protecting the edges during etch is more complicated than one may think, since standard photo resists which are regularly used in modern silicon fabrication for such purposes, are also etched by the HNA-based solution. Moreover, protecting the wafer

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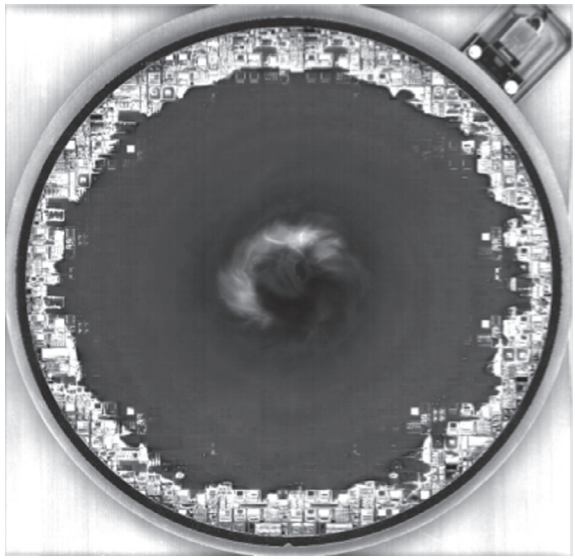


Fig. 4.11 A 200 mm P/P+ wafer after HNA etch without edge protection. The P active layer thickness is 5 µm and the HNA process started after grinding of the silicon down to 20 µm. At the edge of the wafer there is no active silicon left and the first inter-dielectric layer of the metallization is fully exposed.

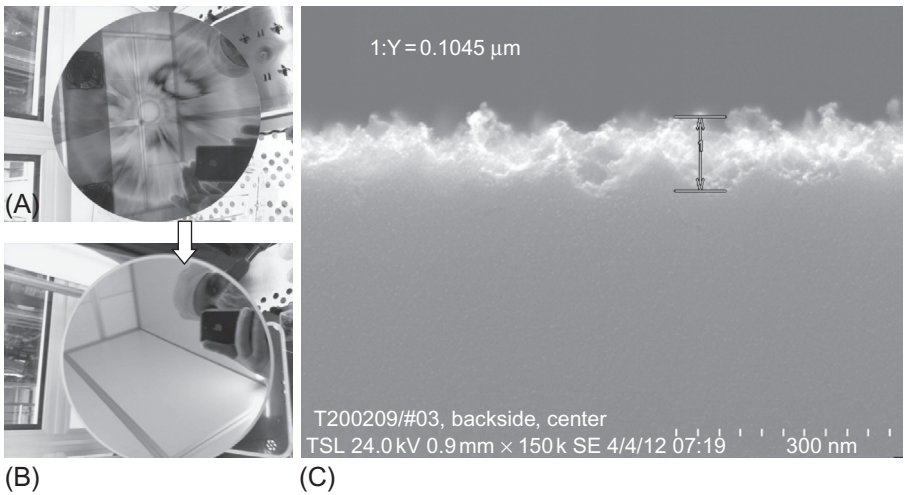


Fig. 4.12 (A) 200 mm wafer surface after HNA thinning, (B) 200 mm wafer surface after HNA thinning and CMP, and (C) X-section of the device wafer after HNA thinning showing the surface roughness.

edge requires nonstandard exposure since the photoresist material has to be completely removed from all the wafer area apart from its edges, a task that cannot be performed by using standard photolithography mask and a photo scanner tool. Finally, the last problem is that the surface roughness after etch is not sufficient and a special CMP process is required in order to get the required surface roughness for the next processing step and for a proper device, as shown in Fig. 4.12.

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The difficulties in achieving good thickness control on a P/P+ wafer is the main reason why today SOI starting material is used for most BSI high-end sensors. The optical area of such sensors is usually relatively large and even a moderate change in the active silicon layer thickness will show up as optical response variation along the sensor. In cinematography, it is customary to have two or more cameras on the shooting set. This dictates very strict demands on the allowed variations between sensors which is very hard to achieve without precise control of the thickness of the active silicon layer. Nevertheless, TSMC reports impressive thickness control of less than ± 0.1 μm achieved on 200 mm bulk wafers.

4.3.5 Surface passivation

The next process step is backside surface passivation. The FSI method for surface passivation is based on surface pinning using high-dose implant, activated, and annealed in relatively high temperatures. However, this method cannot be applied to the BSI wafer at the final stages of manufacturing since metallization layers already exist on the wafer and therefore, the wafer cannot withstand these high thermal cycles. There are at least three widely accepted methods which are used to passivate the back surface of the BSI wafer. A good review of the different methods being used can be found in a paper by Bedabrata Pain from IISW 2009 (Pain, 2009). We discuss briefly these three common methods.

4.3.5.1 Laser annealing

This method involves the following steps:

- The backside of the wafer is implanted by shallow p-type implant (for n-type PD which is manufactured on a p-type substrate).
- The implant is annealed and activated by a powerful laser beam pulse. The pulse length is in the order of several hundred nanosecond (<200 ns). The heat generated by the pulse is enough for local annealing of implant damages and activating of the traps (Huet et al., 2011).
- Since the pulse is very short, the temperature is the metallization area of the wafer does not change.

This method is widely used for commercial manufacturing of BSI CSI. Apart from using relatively high cost dedicated equipment which is not standard for regular CMOS foundries, the main problems associated with this method are:

- Difficulties in annealing large sensors—multiple shots of laser on one die are required in order to cover the sensor area. This can cause later artifacts in the image.
- Need to optimize the implant+anneal to have good QE in short wavelengths

4.3.5.2 Passivation using low-temperature growth of highly doped epitaxial-silicon layers

This method was invented by the California Institute of Technology (CALTECH) and Jet Propulsion Labs (JPL) (Huet et al., 2011; Hoenk et al., 1992) and was widely used for scientific applications (Pain et al., 2005) of BSI close-coupled device (CCD) and

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CMOS sensors. The main advantage of this method is the high QE which can be achieved for short wavelengths. The main disadvantage is the requirement of low-temperature epitaxial growth that can be carried out only by using a molecular beam epitaxial (MBE) growth machine which is not standard in the silicon industry, is very costly and has low throughput.

4.3.5.3 Passivation using dielectric with negative fixed charge

Recently (Meynants, 2010), Guy Meynants of CMOSIS, suggested using Al_2O_3 as a passivation layer. The Al_2O_3 is deposited over SiO_2 and has some inherent fixed negative charge. This negative charge creates a mobile hole accumulation layer close to the interface between the Si and the oxide and can, in some conditions, pin the interface and deactivate the charge. The main advantage of this method is the relative simplicity compared to the previously described methods and the compatibility with standard silicon foundry equipment. The main disadvantage is the difficulty to get a controlled high amount of fixed charge in the Al_2O_3 layer. Here, the thin oxide layer just above the active silicon needs to be of good quality and have a low level of defects.

4.3.6 Light coupling

The next process steps are dedicated to the light coupling into the sensor. It is customary at this step to create:

- an antireflecting coating
- a metal grid
- a color filters array (CFA) and μ-lenses

4.3.6.1 Antireflecting coating

One of the big advantages of a BSI sensor is the freedom to use a dedicated optimized ARC to increase QE for a given application. This is the main driving force for high-end sensor designers to move into BSI. High volume sensor manufacturers tend to use HfO, SiON, and SiO_2, but more exotic material systems like MgF_2 and Ta_2O_5 are commonly used as well. A nice example of ARC deposited on a Sony 1.55 BSI sensor can be seen in Fig. 4.13.

4.3.6.2 Metal grid

Deposition and patterning of a thin metal grid at the physical boundaries of each pixel is a common practice for most high volume manufacturers. For a small pixel, there is a significant amount of light arriving at the pixel periphery. These photons tend to increase the cross talk between pixels and can also hit the color filter array in places where the color filters are not defined which causes increased photon response nonuniformity (PRNU).

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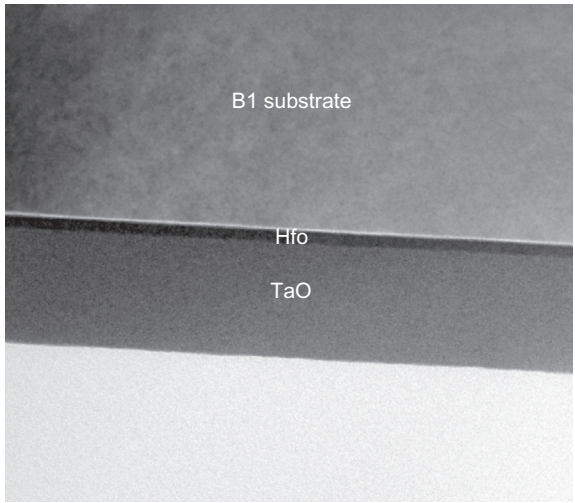


Fig. 4.13 Antireflecting coating example of 1.55 μm generation from Sony BSI. Courtesy of Chipworks (Sony, 2012. ISX014, CMOS Image Sensor (SOC) With Built-in High-Performance Image-Processing Engine and Camera System Functions. http://www.sony.net/Products/SC-HP/cx_news/vol70/pdf/isx014.pdf).

4.3.6.3 Color filters array (CFA) and μ-lenses

Color filter array and μ-lenses patterning is very similar to the front-end case. The main difficulty here is to align the optical stack and the metal grid to the pixel active diode area. Typically, the Si thickness after thinning may be over 2 μm for a high volume small pixel sensor and over 5 μm for a high-end sensor. Hence, alignment of backside structures to the pixel active area needs to upgrade to an IR alignment tool or devolving, a solution which can work with the standard fabrication tool. At TowerJazz, for example (see Fig. 4.14), deep trench marks formed at the frontside of the wafer, and subsequently exposed at the bonded backside after thinning, are used for backside alignment.

4.4 Interface solutions to BSI sensors

Finally, a few words on the interface of the BSI sensor to the outside world are discussed here. For a conventional wire-bonded frontside sensor, the passivation layer above the last metallization is removed above the pads. This is a similar/identical process to a regular CMOS chip. The pads are then bonded and wired using standard wire bond (usually gold) techniques. For BSI sensors, the pads are "hidden" by the thick supporting wafer and the standard pad opening is not applicable and therefore, some alternative solutions are used. A solution known as through silicon Via (TSV) where a deep via is etched through the support wafer to the "hidden" pads is known to be used by some mass market players (Fontaine, 2011), and also for FSI wafer-level packaged (WLP) devices. A more straightforward solution is to open the pads from the backside by etching first the antireflective dielectric coating, through the epitaxial active layer and the first frontside inter-dielectric, stopping at the M1 pads as shown in Fig. 4.15.

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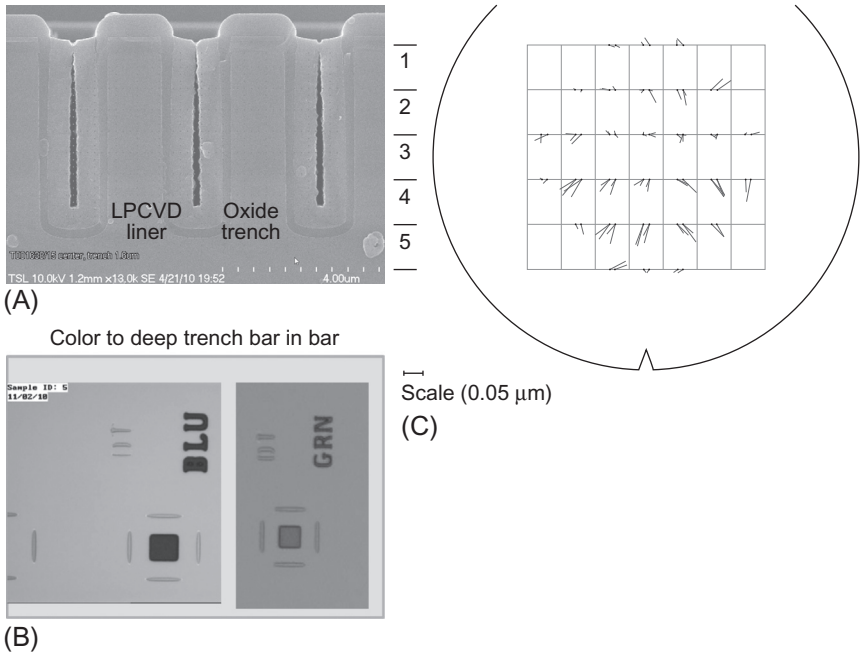


Fig. 4.14 Alignment of the color filter array to the frontend using deep trenches (A) SEM pictures of the deep trenches alignment mark, (B) *blue* and *green* color filter alignment to the deep trench mark, and (C) typical wafer map which measure the misalignment between the deep trench mark and the color filter.

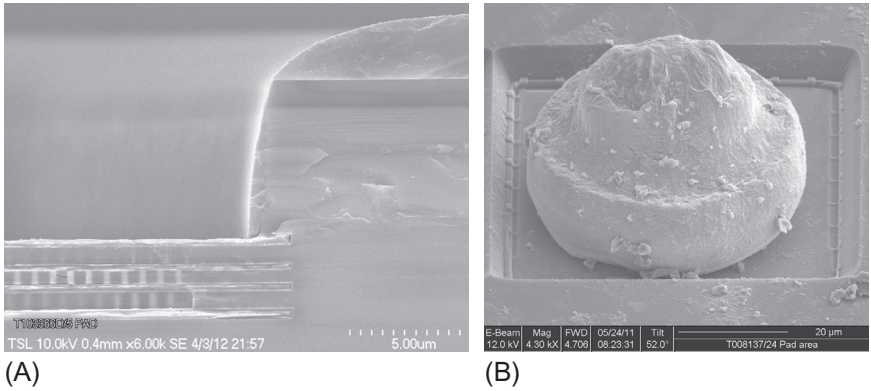


Fig. 4.15 Pad opening scheme (A) cross section showing deep etch from the sensor backside which stops at M1 of the pad structure and (B) arbitrary unit bonding in the center of the backside pad.

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A discussion on the most advanced method for interfacing a BSI sensor to the outside world concludes the chapter. In this method, the carrying wafer which was previously discussed as a dummy wafer, becomes an electrically active circuit. Some circuits which used to be printed on the image sensor are now fabricated on the carrier wafer. The image sensor wafer is fabricated as before. The last metal in each wafer is designed to connect the electrical circuit from the image sensor wafer to the readout integrated circuit (ROIC) wafer. The wafers are aligned frontside to frontside, bonded, and annealed to create the full active device and the backside flow continues as described before. Contacts can be either TSV on the ROIC wafers or on the imager wafer or regular wire bond as described above. The process of electrically bonding the two wafers is schematically described in Fig. 4.16. Sony has already announced (Sony, 2012) an image sensor chip which is using some readout circuits in the carrier

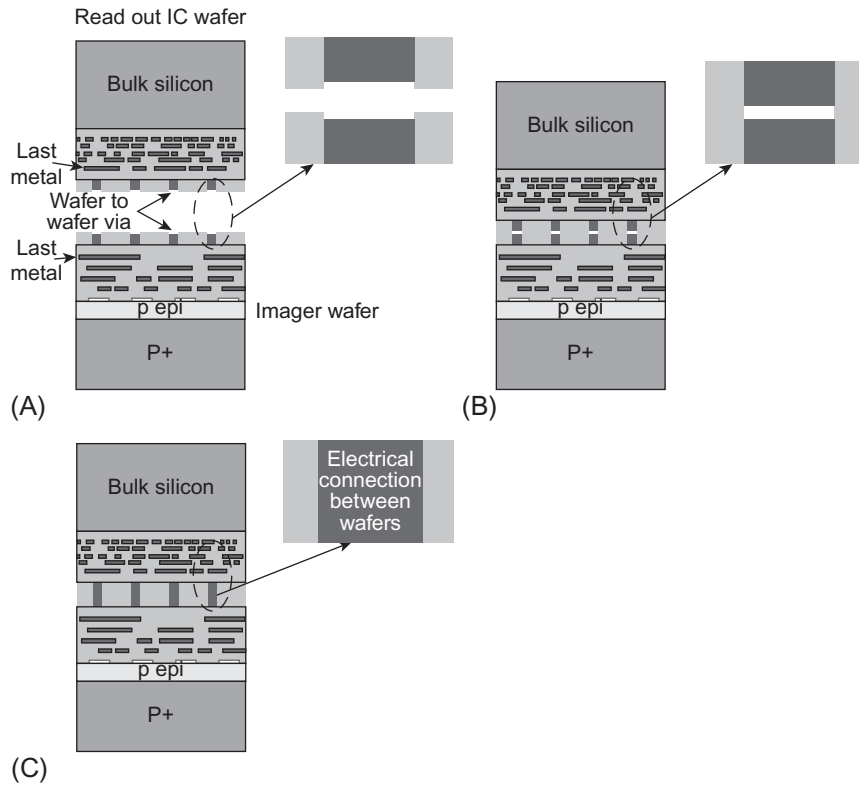


Fig. 4.16 Illustration of a typical 3D bonding between imager wafer and an ROIC wafer (A) alignment of imager wafer and ROIC wafer (each wafer surface has been prepared carefully before alignment), (B) wafers are now carefully placed one on top of the other. The surfaces of the waters are cleaned and sometimes activated by plasma. As a result strong oxide-to-oxide bonding between the two wafers is achieved, (C) thermal treatment causes the metal to expand and create electrical connection between metals.

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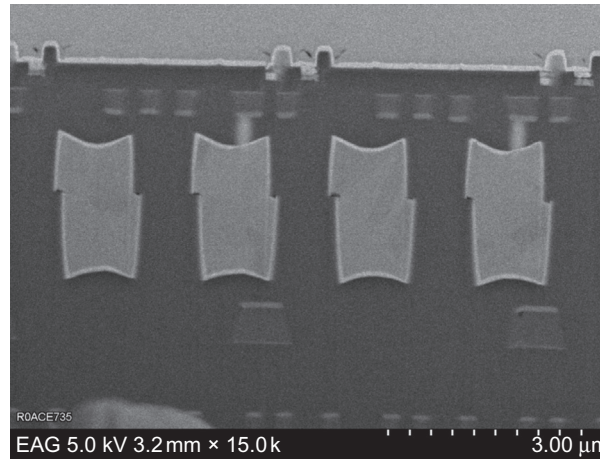


Fig. 4.17 Cross section of a wafer-to-wafer electrical test structure with 2 µm separation between the vias. Courtesy of Ziptronix (Huet, F. R. K., Boniface, C., Venturini, J., Ait Fqir Ali-Guerry, Z., Beneyton, R., Marty, M., Dutartre, D., 2011. High performance and high yield junction formation with full device exposure laser thermal annealing. In International Image Sensor Workshop).

wafer. The next evolutionary step in this technology, considered to be the "holy grail" for pixel and camera designers all over the world, is to use the same technology with one or two connections per pixel between the image sensor wafer to the ROIC wafer. A cross section of a wafer-to-wafer bonding with 2 µm separation is shown in Fig. 4.17. Some prototypes of a 3-Meg imager were reported by Ziptronix (Ziptronix, 2013). If this technology finally reaches the market, the possibilities are endless, especially for high-end sensors. For example, one can design the image sensor wafer with a dedicated process with long thermal anneal which will result in a very clean image due to low dark current and low 1/*f* noise. This cannot be achieved in a traditional image sensor due to many compromises imposed by the fast logic process (Lahav and Fenigstein, 2008). Application of this technology includes a better global shutter pixel with very low parasitic light sensitivity, low noise application, and sophisticated high dynamic range sensors like time to saturation sensors or well-cycling sensors (Yang and El Gamal, 1999).

4.5 Conclusion

In this chapter we reviewed some of the major challenges and trends in the fabrication of BSI sensors. We started by describing the advantages of a BSI sensor over an FSI sensor. We showed that the possibility to use advanced materials to create a highly optimized antireflecting coating is the main driving force for BSI technology for scientific and high-end applications. On the other hand, for pixels sizes <2 µm intended for the mass market, BSI is a natural choice and a necessity. It might even turn out to be a cheaper solution than the other complicated front-end methods which are used to couple light into these pixels.

Our discussion continued with a detailed look at the fabrication of a wafer level backside illumination sensor. We reviewed the pros and cons of SOI starting material

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which is widely used for scientific applications and showed that the gettering issue needs to be addressed properly in order to achieve an acceptable working sensor.

Finally, we discussed the different options of connecting the sensor to the outside world. The exciting concept of an image wafer bonded to an ROIC wafer was brought forward. We predicted that BSI sensors with a pixel-to-pixel contact to an ROIC wafer could enhance high-end image sensor performance such as high-quality global shuttering and sophisticated high dynamic range sensors.

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