

MOS Area Sensor: Part II—Low-Noise MOS Area Sensor with Antiblooming Photodiodes

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Abstract—The development of a high-sensitivity 320×244 element MOS area sensor and a novel fixed pattern noise (FPN) suppressing circuit are reported in this paper. The new device incorporates p^+-n^+ high- C photodiodes and double-diffused sense lines.

The p^+-n^+ high- C photodiodes provide a large dynamic range and a large saturation signal of $1.4 \mu A$ with 6-lx W-lamp illumination. The double-diffused sense lines are introduced to vastly improve blooming characteristics, making use of a built-in potential barrier.

FPN is proved to stem mainly from inversion charge variations through horizontal switching MOS gate capacitances. A simple high-performance FPN suppressing circuit is proposed which realizes high signal-to-noise (S/N) ratios of more than 68 dB at saturation. The new sensor is tested in a high-sensitivity black-and-white VTR hand-held camera and will find broad applications.

I. INTRODUCTION

RAPID and consecutive developments in Si VLSI technologies have generated interest in utilizing Si area image sensors in the VTR and ITV camera fields. To date, various types of sensors [1]–[3], [7], [8], [12], [13] have been reported.

Some CCD black and white (B/W) sensors [4], [5] have been placed on the market. These devices, however, are not practical because they are very expensive. In addition, they have poor blooming characteristics. Furthermore, dark currents reduce picture quality and increase fixed pattern noise (FPN), especially during high-temperature operation. On the other hand, MOS sensors [6], [11], [14], [15] have suffered from poor signal-to-noise ratios (S/N), although they offer high sensitivity, small chip size, and potentially low costs.

Consequently, more advanced area sensors with high sensitivity, high S/N , and good blooming characteristics have been eagerly sought. This paper presents a new MOS area sensor with an antiblooming photodiode structure and a novel FPN suppressing circuit. In Section II, design considerations on the new B/W image sensor are presented. After the description on device fabrication in Section III, the measured performance and FPN suppressing circuitry are reported in Section IV. A single-chip color imager was described in Part I of this series.

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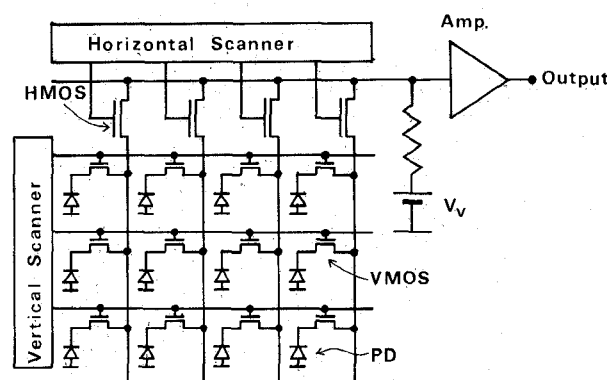


Fig. 1. Circuit configuration of MOS area sensor.

II. DESIGN CONSIDERATIONS

A. High-Density Array Configuration

A conventional MOS area sensor contains p - n junction photodiodes, vertical switching transistors (VMOS), horizontal switching transistors (HMOS), and a vertical and horizontal scanner as shown in Fig. 1. Based on this configuration, a new MOS sensor was designed which realizes a high-sensitivity, $\frac{2}{3}$ -in lens format B/W VTR camera. 320×244 photodiodes were arranged in a scan area of $8.8 \text{ mm} \times 6.6 \text{ mm}$ with the unit cell size in the array being $27 \mu\text{m} \times 27 \mu\text{m}$. This new sensor was designed to operate with two-phase clock pulses and a single dc power supply. All of the scanning shift registers on the chip are two-phase dynamic circuits.

B. Sensitivity

One feature of the new sensor is its unique photodiode structure with a p^+-n^+ high- C photodiode and a double-diffused sense line, as shown in Fig. 2. The p^+-n^+ high- C photodiodes were introduced to achieve a large storage capacitance, a large dynamic range, and a large saturation signal.

With these photodiodes, sensitivity S ($\mu A/\mu W$) can be calculated as

$$S(\lambda) = \frac{q \cdot \beta \cdot (1 - R_{ox}) \cdot (1 - R_{Si}) \lambda}{h \cdot c} \cdot \{ \eta(\lambda) - (\eta(\lambda) - \eta_p(\lambda)) \cdot \alpha_p \}. \quad (1)$$

Here, q is electron charge, h is Planck's constant, c is the velocity of light, λ is wavelength, and β is the aperture efficiency.

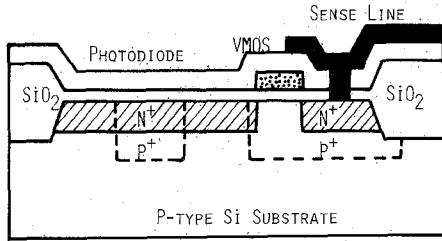
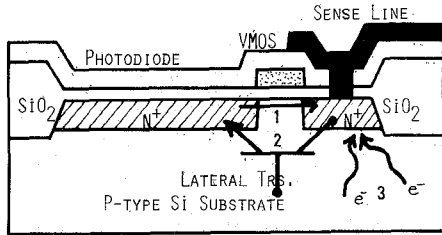
Fig. 2. Cross section of antiblooming photodiode with p⁺ layer.

Fig. 3. Blooming mechanism in MOS sensor.

α_p is the ratio of high-C photodiode area to the photo element area, and R_{ox} and R_{Si} are the reflection coefficients at the air-SiO₂ and SiO₂-Si interfaces, respectively. $\eta(\lambda)$ and $\eta_p(\lambda)$ are quantum efficiencies in the p-n⁺ normal and p⁺-n⁺ high-C regions. These quantum efficiencies can be approximately expressed with the following equations, using absorption coefficient $\alpha(\lambda)$, diffusion length L_d , and diffusion depth x_j :

$$\eta(\lambda) = 1 - \exp(-\alpha(\lambda) \cdot L_d) \quad (2)$$

$$\eta_p(\lambda) = 1 - \exp(-\alpha(\lambda) \cdot x_j) \quad (3)$$

In (3), a depletion layer is neglected.

Since there is no poly-Si photogate in the new sensor, high sensitivity can be expected.

Saturation signal charge Q_s is obtained as follows:

$$Q_s = A_{pd} \cdot (1 - \alpha_p) \sqrt{2 \cdot q \cdot \epsilon_{Si} N_a} \cdot \left(1 + \frac{\alpha_p}{1 - \alpha_p} \sqrt{\frac{N_p}{N_a}}\right) \cdot \sqrt{V_v + V_{bi}} \quad (4)$$

Here, A_{pd} is photodiode area, ϵ_{Si} is Si dielectric constant, V_v is output video bias voltage, V_{bi} is built-in potential, and N_a and N_p are impurity concentrations of the p-type substrate and of the p⁺ layer, respectively. In this equation, the saturation potential of a photodiode is assumed to be 0 V.

Saturation signal charge Q_s was originally designed to be 0.25 pC for 7-lx faceplate illumination with a W lamp. Sensitivity can then be estimated to be 0.22 $\mu A/\mu W$ at 550 nm, using (1) when $\beta = 0.67$, $R_{ox} = 0.02$, $R_{Si} = 0.23$, and $\alpha_p = 0.25$ [16].

C. Antiblooming Photodiodes

Another important characteristic in a sensor is blooming. The blooming phenomena in sensors are very similar to α -particle problems in VLSI digital memories. The blooming mechanism in an MOS area sensor without any countermeasures is illustrated in Fig. 3, in which three dominant components for blooming currents are shown schematically.

1) Tailing current from a photodiode to a vertical sense line through a VMOS is very severe.

2) Another component is lateral bipolar transistor current under VMOS gate and isolation regions.

3) The other current is due to excess charges diffusing directly from the bulk in the substrate to the output drain.

The new photodiodes, as shown in Fig. 2, have p⁺ layers under the gate and around the output n⁺ drain. The p⁺ layer under the gate raises the threshold voltage V_{th} of the VMOS.

The blooming charge Q_{b1} from one photodiode to the output drain for a horizontal period t_h (63.5 μs) must satisfy the following equation. Here, it is assumed that I_t is the tailing current from one pixel, Q_s is the saturation charge given in (4), and S_n is the allowable S/N for blooming.

$$Q_{b1} \leq \frac{Q_s}{q \cdot S_n \cdot I_t \cdot t_h} \quad (5)$$

Tailing current I_t in (5) is given in the following form:

$$I_t = I_{th} \cdot 10^{(V_{GL} + V_{PD} + K \sqrt{V_{PD}} - V_{th}/\alpha_T)} \quad (6)$$

Here, I_{th} is the threshold current in the VMOS, α_T is the tailing coefficient, V_{GL} is the gate low level, and V_{PD} is the photodiode forward bias when blooming occurs.

Equations (5) and (6) indicate that the VMOS threshold voltage V_{th} must satisfy the next equation, in order to suppress the tailing current through the VMOS

$$V_{th} \geq V_{GL} + V_{PD} + K \sqrt{V_{PD}} - \alpha_T \cdot \log \left(\frac{Q_s}{S_n \cdot Q_{b1}} \cdot \frac{q}{I_{th} \cdot t_h} \right) \quad (7)$$

The p⁺ layer under the VMOS gate is also effective for reducing charge injection from the photodiode to the p-type substrate through n-p-n lateral bipolar transistors. In addition, the p⁺ layer around the output drain makes a potential barrier $\Delta\phi$ which is approximately expressed as

$$\Delta\phi = \frac{kT}{q} \cdot \ln \left(\frac{N_p}{N_a} \right) \quad (8)$$

where k is Boltzmann's constant and T is temperature.

A part of excess charges generated in the bulk of the substrate are blocked by this potential barrier. In order to get excellent blooming characteristics, the impurity concentration in the p⁺ layer was made as high as possible for acceptable resolution to be obtained, although stray capacitance of the output line increases as impurity density increases.

D. FPN in MOS Area Sensor

In an MOS area sensor, there are many kinds of noises such as FPN random noise, and spike noise. Among these, FPN has proved to be the most severe problem and limits sensor S/N.

There are three primary sources of FPN in an array like the one in Fig. 1. During array scanning, each horizontal switching transistor (HMOS) goes on and off. When the HMOS goes on, it induces inversion charges under the gate through a nonlinear gate capacitance C_g and a gate-to-drain capacitance C_p . The

HMOS pushes the charges to the output line, when going off. As a result, FPN stems mainly from the induced charge fluctuations.

The FPN charge Q_{ng} through gate capacitance C_g can be represented as

$$Q_{ng} = \Delta C_g \cdot (V_G - V_{tH} - V_v) + C_g \cdot \Delta (V_G - V_{tH} - V_v). \quad (9)$$

Here, V_G is the output pulse amplitude of the horizontal shift register, V_{tH} is the threshold voltage in the HMOS, V_v is output video bias, and Δ denotes variation. The FPN charge Q_{np} through the gate-to-drain capacitance C_p is expressed in the same form as follows:

$$Q_{np} = \Delta C_p \cdot V_G + C_p \cdot \Delta V_G. \quad (10)$$

Another major source of FPN is due to variations in thermal leakage current, which strongly depends on the process technology. Other sources of FPN may be:

- Waveform variations in output pulses from the horizontal shift register, that is, variations in rise and fall times, and phase and width of pulses;
- displacement current fluctuations in the shift register, leading to spike noise fluctuations through the substrate;
- charge pumping current;
- diffusion of charges from the chip periphery due to undershoots of external pulses;
- vertical switching noise related to (9) and (10) which is like the horizontal stripe or dot noise in a monitor.

Among these sources, the variations in displacement charges during HMOS switching operations, expressed in (9) and (10), seem to be most significant for FPN. This leads to several device design guidelines to suppress FPN. They include:

- low noise shift register free of pulse amplitude variation and operation at low voltages;
- small gate capacitance C_g and small gate-to-drain capacitance C_p ;
- small dimension fluctuations of ΔC_g and ΔC_p , and small threshold voltage variations ΔV_{tH} .

In addition, the sources of noise in (9) and (10) may be also greatly suppressed by appropriate signal processing, as discussed in Section IV.

E. High-Density Horizontal Shift Register

In the new sensor, a new low-noise shift register was designed to make FPN low. This register has eight transistors and two bootstrap capacitances per stage. The shift register provides the HMOS gates with uniform pulses by using bootstrap circuitry. This means that the original charge variations Q_{FPN} can be made small, since $\Delta V_G \rightarrow 0$ in (9) and (10).

Another key point in this register is the fact that there is no overlapping of adjacent two output pulses from the register. Thus spike noises from adjacent HMOS's are separated to permit signal processing in the idling time and to get the desired signals without FPN.

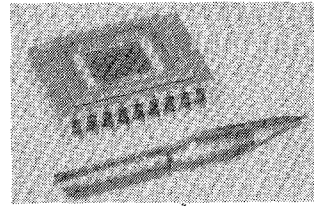


Fig. 4. Photograph of sensor mounted in 20-pin DILC package.

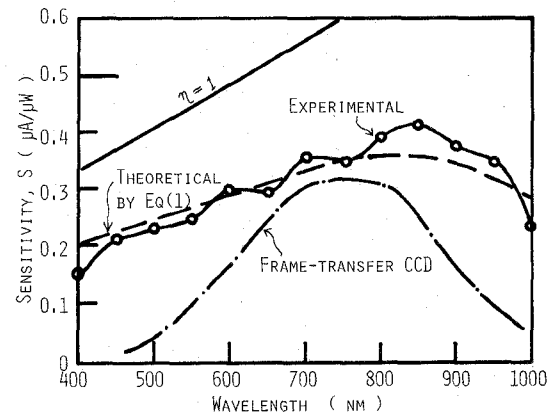


Fig. 5. Spectral response. Solid line shows measured response and the broken line shows the calculated value for (1).

Actual power dissipation was about 30 mW, when the device operates with a 6-MHz two-phase clock pulse. This is in close agreement with the original design considerations.

III. FABRICATION

The new sensor was fabricated using n-channel Si-gate technology with repeated annealing processes to decrease thermal leakage current. As a result, a dark current of less than 0.3 nA/cm² was obtained at room temperature with this configuration. The photo cell measures 27 μm × 27 μm and the chip size is 9.8 mm × 8.4 mm. The new sensor was mounted in a 20-pin DILC package as demonstrated in Fig. 4.

IV. EXPERIMENTAL RESULTS

A. Light-Transfer Characteristics

The new sensor operates successfully, with only a single 9-V power supply, to provide excellent quality pictures. The spectral response of this sensor is represented by the solid line in Fig. 5. This device shows high sensitivity when compared with a frame-transfer CCD sensor [17]. This is because the MOS sensor does not have any poly-Si photogates. The broken line shows the calculated characteristics using (1) with $R_{ox} = 0.02$, $R_{Si} = 0.23$, $\beta = 0.67$, and $\alpha_p = 0.25$. Good agreement between (1) and the experimental results is indicated in the figure.

A 1.4-μA saturation current was obtained with a 6-1x face-plate illumination.

B. Blooming Characteristics

The threshold voltage V_{th} of a VMOS was set to be around 3 V from (7). This adjustment reduced tailing current along the VMOS by more than 3 orders of magnitude.

The p⁺ layer under the VMOS gate and around the output

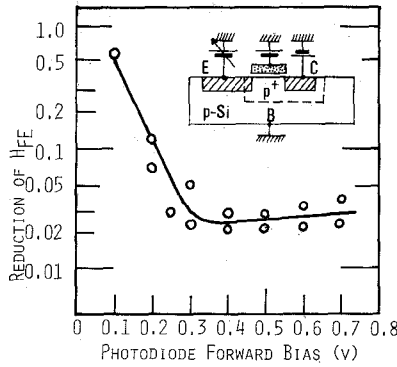


Fig. 6. Current gain h_{FE} in lateral bipolar transistor with p^+ layer. h_{FE} is normalized by h_{FE} in transistor without p^+ layer.

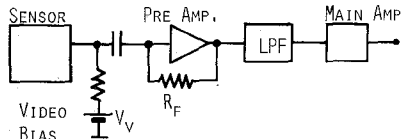


Fig. 7. Experimental apparatus for FPN.

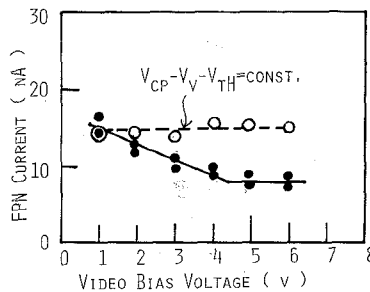


Fig. 8. FPN with parameter of output video bias.

n^+ drain reduced the current gain of lateral n-p-n bipolar transistors to $\frac{1}{10}$ to $\frac{1}{30}$ of the gain without the p^+ layer. This gain with the p^+ layer is shown in Fig. 6. The potential barrier for excess charges in the bulk by the p^+ layer was measured to be 0.1 V. The fact that only a 0.1-V potential barrier around the drain can greatly suppress blooming current suggests that the antiblooming photodiode structure with the p^+ layer will be very effective for realizing a high-sensitivity sensor. This is because the sensor will not need an overflow drain. This structure may work well to suppress soft errors by α -particles in VLSI's.

C. Fixed-Pattern Noise

FPN was measured using a signal-processing circuit as shown in Fig. 7. The preamplifier is a low-noise feedback amplifier and has a closed-loop bandwidth (-3 dB) of more than 10 MHz. The device was operated with 6-MHz clock pulses and the bandwidth of the low-pass filter was 3 MHz.

The FPN currents I_{FPN} are plotted in Fig. 8 with output video bias V_v as a parameter. In this figure, the solid line represents the FPN characteristics when the video bias was changed. Here, FPN decreases as video bias V_v increases. An S/N of 46 dB was obtained with a 5-V video bias and with a 1.4- μ A signal current.

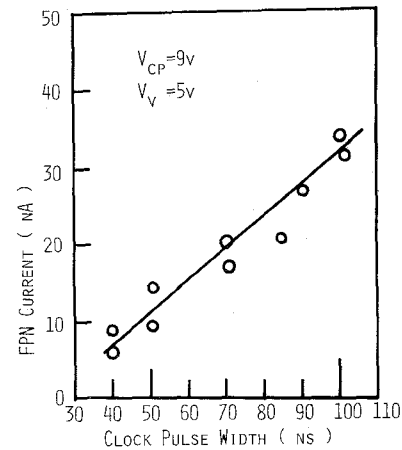


Fig. 9. Relationship between FPN and clock pulsewidth.

On the other hand, the broken line shows the FPN when $V_G - V_v - V_{th}$ remained constant. In this case, no change in FPN was observed. From this figure, it can be concluded that the FPN charge Q_{FPN} in this new sensor can be described analytically as

$$Q_{FPN} = \Delta C_g \cdot (V_G - V_v - V_{th}) + C_g \cdot \Delta V_{th}. \quad (11)$$

Since FPN is caused by variations in the displacement spike noises of HMOS's, FPN was found to change as the clock pulsewidth was varied, as illustrated in Fig. 9. The pulsewidth is equal to the time between a positive spike and the associated negative spike in this sensor as mentioned earlier. When a clock pulsewidth becomes small, in other words, a pair of spikes are closer, the integration effect in the low-pass filter works to reduce FPN.

Using (11), it was calculated that $\Delta V_{th} = 60 \sim 100$ mV, $\Delta C_g/C_g = 2-3$ percent, and $\Delta C_p = 0$ in this sensor. The threshold voltage variations are the same sources to sense amplifier errors in VLSI memories. The MOS sensors will be powerful tools to monitor process technology level and to analyze process defect modes.

D. FPN Suppressing Circuit

The experimental results discussed above suggest that it is possible to make the optical signal immune to FPN if the signal is read out with an appropriate processing circuit. Consequently, one of the features of the new sensor is a novel FPN suppressing circuit. This new circuitry and the timing necessary to effect switching noise cancellation are shown in Fig. 10.

This simple circuit contains an emitter-follower amplifier, an integration capacitance, a reset switch, and a load resistor. The emitter voltage $V_E(t)$ follows the base bias $V_B(t)$, that is, the spike noise $V_S(t)$, from the sensor. This results in the following emitter current $I_E(t)$ using the built-in potential V_{bi} :

$$I_E(t) = \frac{V_E(t)}{R_E} = \frac{V_B(t) - V_{bi}}{R_E} = \frac{V_S(t) - V_{bi}}{R_E}. \quad (12)$$

After the reset switch goes off, emitter current $I_E(t)$ flows as described in (12) and capacitance C is discharged. The collector bias goes down until the next reset pulse ϕ_R is applied.

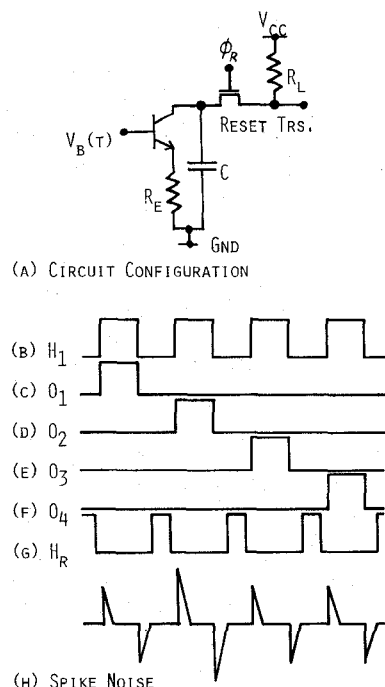


Fig. 10. Proposed FPN suppressing circuit and related timing chart.

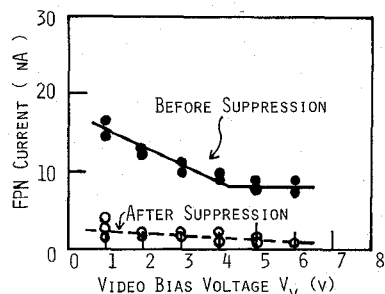


Fig. 11. FPN level reduced by new FPN suppressing circuitry. • before suppression and ○ after suppression.

The total discharging charges Q_{dc} for an integration period t_i can be expressed as

$$Q_{dc} = \int_0^{t_i} \frac{V_S(t) - V_{bi}}{R_E} dt. \quad (13)$$

As a result, a pair of spikes are integrated or canceled, leaving only the output signal generated by incident light.

Here, the noise charges are capacitively coupled and, hence, can have no steady-state dc value other than 0. Therefore, the total charges coupled to integration capacitance C may be almost zero. This simple circuit works very effectively with good frequency characteristics to suppress FPN, as shown in Fig. 11. The • marks show the experimental values before FPN suppression and the ○ marks are for after suppression. FPN is suppressed to about 0.5 nA with a 5-V video bias and is eliminated by a factor of 7 to 10, i.e., 17 to 20 dB. The novel circuitry made the FPN lower than the random-noise level as demonstrated in Fig. 12. In line with this, a high signal-to-noise ratio of more than 68 dB was obtained. Performance of the new sensor is limited by random noise of about 0.6 nA now that FPN has been fundamentally elimi-

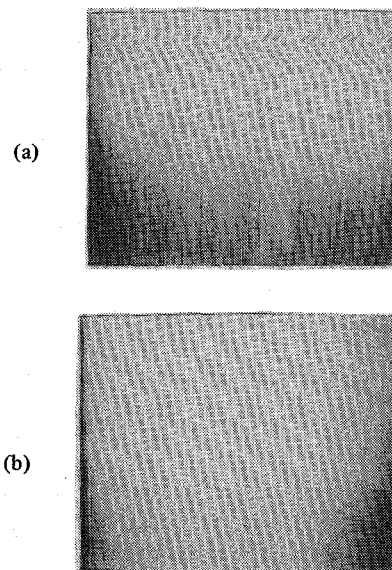


Fig. 12. Improvement in picture quality. (a) Before improvement and (b) after.

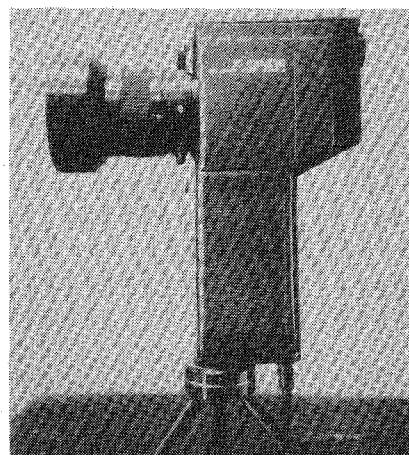


Fig. 13. B/W VTR hand-held camera.

nated. This means that the new sensor should provide better performance than image tubes such as the Vidicon.

Various alternative techniques [6], [9], [10] have been reported for FPN reduction. They, however, involve more complicated circuits. It was found that the simple FPN suppressing circuit described here achieves equal or better performance than those other techniques.

E. Hand-Held Camera for VTR

The new sensor was used in a B/W VTR camera, that can be hand-held, as shown in Fig. 13. This camera makes good-quality pictures. The camera includes a sensor and all the circuits necessary to successfully generate acceptable NTSC TV signals. The entire unit weighs only 680 g including a 1:4 zoom-lens and dissipates only 1.6 W.

A 240 TV-line horizontal resolution and a 190 TV-line vertical resolution were obtained. The characteristics of this new sensor are summarized in Table I. Many features, such as anti-blooming photodiodes, low-noise shift registers, small dark-

TABLE I
CHARACTERISTICS OF THE SENSOR

Number of Elements	320 (H) X 244 (V)
Pitch	27 μm X 27 μm
Scan Area	8.8 mm X 6.6 mm
Chip Size	9.8 mm X 8.4 mm
Package	20 pin DILC
Power Supply	9 v $\pm$ 10 %
Power Dissipation	30 mW
Horizontal Clock Rate	6 MHz
Saturation Current	1.4 μA
Faceplate Illumination	6.2 lx (W-lamp)
Sensitivity	0.22 $\mu\text{A/lx}$ (W-lamp)
Signal-to-noise ratio For FPN	46 dB (without suppression) 68 dB (with suppression)
For Random Noise	66 dB (p-p/rms)
Dark Current	0.1 nA/cm ²
Blooming Suppression	3 to 5 times of Saturation
Horizontal Resolution	240 TV lines
Vertical Resolution	190 TV lines

current process technology, and novel FPN suppressing circuitry are integrated on the same chip to realize this high-sensitivity, low-cost, and small B/W VTR hand-held camera. The good low-light level performance suggests a big potential market in the video camera field, for example, VTR and ITV cameras, astronomic telescopes, and security-watch cameras.

V. CONCLUSIONS

A new high sensitivity 320 X 244 element MOS area sensor with p⁺-n⁺ high-C photodiodes and double-diffused sense lines has been developed. The p⁺-n⁺ high-C photodiodes were introduced to provide a large storage capacitance, a large dynamic range, and a large saturation current of 1.4 μA with 6-lx W-lamp illumination. The double-diffused sense lines successfully reduce tailing current and provide a potential barrier which blocks excess charges. Blooming characteristics were improved vastly.

FPN was proved to be caused mainly by gate capacitance and threshold-voltage variations in horizontal-switching MOS transistors. A novel integration circuit was proposed and it successfully reduces FPN by 20 dB.

Excellent results were obtained using this sensor and related circuitry to realize a new movie camera. This sensor is expected to find broad applications especially in the VTR and ITV camera fields.

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REFERENCES

- [1] P. K. Weimer, W. S. Pike, M. G. Kovac, and F. V. Shallcross, "The design and operation of charge coupled image sensor," in *ISSCC Dig. Tech. Papers*, p. 132, 1973.
- [2] H. K. Burke and G. J. Michon, "Charge injection imaging," *IEEE Trans. Electron Devices*, vol. ED-23, pp. 189-196, Feb. 1976.
- [3] J. D. Plummer and J. D. Meindl, "A low-light level self scanned MOS image sensor," in *ISSCC Dig. Tech. Papers*, p. 30, 1972.
- [4] Fairchild CCD 201 data sheet, 1975.
- [5] Fairchild CCD 202 data sheet, 1976.
- [6] J. D. Plummer and J. D. Meindl, "MOS electronics for a portable reading aid for the blind," *IEEE J. Solid-State Circuits*, vol. SC-7, pp. 111-119, Apr. 1972.
- [7] H. Heyns and J. G. V. Santen, "The resistive gate CTD area-image sensor," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 135-139, Feb. 1978.
- [8] S. Ochi, S. Yamanaka, Y. Kanoh, and T. Nishimura, "A device structure and spatial spectrum for checker-pattern CCD color camera," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 261-266, Feb. 1978.
- [9] P. L. P. Dillon, D. M. Lewis, and F. G. Kaspar, "Color imaging system using a single CCD area array," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 102-107, Feb. 1978.
- [10] C. Anagnostopoulos, "Signal readout in CID image sensor," *IEEE Trans. Electron Devices*, vol. ED-25, pp. 85-89, Feb. 1978.
- [11] N. Koike, I. Takemoto, K. Sato, H. Matsumaru, M. Ashikawa, and M. Kubo, "An NPN structure 484 X 384 MOS imager for a single-chip color camera," in *ISSCC Dig. Tech. Papers*, p. 192, 1979.
- [12] K. Horii, "512 X 486 cell CCD image sensor," *J. Inst. Eng. Japan*, vol. 33, no. 7, p. 523, 1979.
- [13] N. Harada, Y. Endo, M. Iwasawa, and M. Matsushima, "512 X 340 element CCD image sensor," *J. Inst. Telev. Eng. Japan*, vol. 23, no. 7, p. 536, 1979.
- [14] T. Takamura and H. Tanaka, "Single-chip MOS color image sensor," *J. Inst. Telev. Eng. Japan*, vol. 23, no. 7, p. 560, 1979.
- [15] T. Ando, S. Akaboshi, and H. Ishihara, "Solid state Si image sensor and its design considerations," *J. Inst. Telev. Eng. Japan*, vol. 26, no. 1, p. 33, 1972.
- [16] H. F. Wolf, *Silicon Semiconductor Data*. New York: Pergamon.
- [17] C. H. Sequin, F. J. Morris, T. A. Shankoff, M. F. Tompsett, and E. J. Zimany, "Charge-coupled area image sensor using three levels of polysilicon," *IEEE Trans. Electron Devices*, vol. ED-21, pp. 712-720, Nov. 1974.