

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY LIMITED,
Petitioner,

v.

ALIDDOUBLE, INC.,
Patent Owner.

IPR2023-00372
Patent 6,169,319 B1

Before KRISTINA M. KALAN, CHRISTOPHER M. KAISER, and
JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

KALAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Taiwan Semiconductor Manufacturing Company Limited (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–6 of U.S. Patent No. 6,169,319 B1 (Ex. 1001, “the ’319 patent”). Alidouble, Inc. (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).

To institute *inter partes* review, we must determine that the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). For the reasons discussed below, after considering the parties’ submissions and the evidence of record, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one claim of the ’319 patent, and we institute *inter partes* review on all challenges raised in the Petition. 37 C.F.R. § 42.108 (2022).

A. *Related Proceedings*

The parties identify the following district court litigation as related matters: *Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Ltd.*, No. 2:22-cv-00298-JRG (E.D. Tex.) (pending) (“parallel District Court litigation”); *Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Ltd.*, No. 2:21-cv-00452-JRG (E.D. Tex.) (dismissed). Pet. 87; Paper 3, 2 (Patent Owner’s Mandatory Notices).

B. *Real Parties-in-Interest*

Petitioner identifies Taiwan Semiconductor Manufacturing Company Limited as the real party-in-interest. Pet. 87. Patent Owner identifies Alidouble, Inc. as the real party-in-interest. Paper 3, 2.

C. The '319 Patent

The '319 patent is titled “Backside Illuminated Image Sensor” and relates to solid state image sensors used in, e.g., video cameras. Ex. 1001, code (54), 1:12–15. The '319 patent discloses a back-illuminated Complementary Metal-Oxide-Semiconductor (CMOS) image sensor including a matrix of pixels, e.g., CMOS active-pixel sensor (APS) cells utilizing photodiode light sensitive regions, that are fabricated on a semiconductor substrate. *Id.* at code (57), 5:65–67.

Figure 5 of the '319 patent is reproduced below.

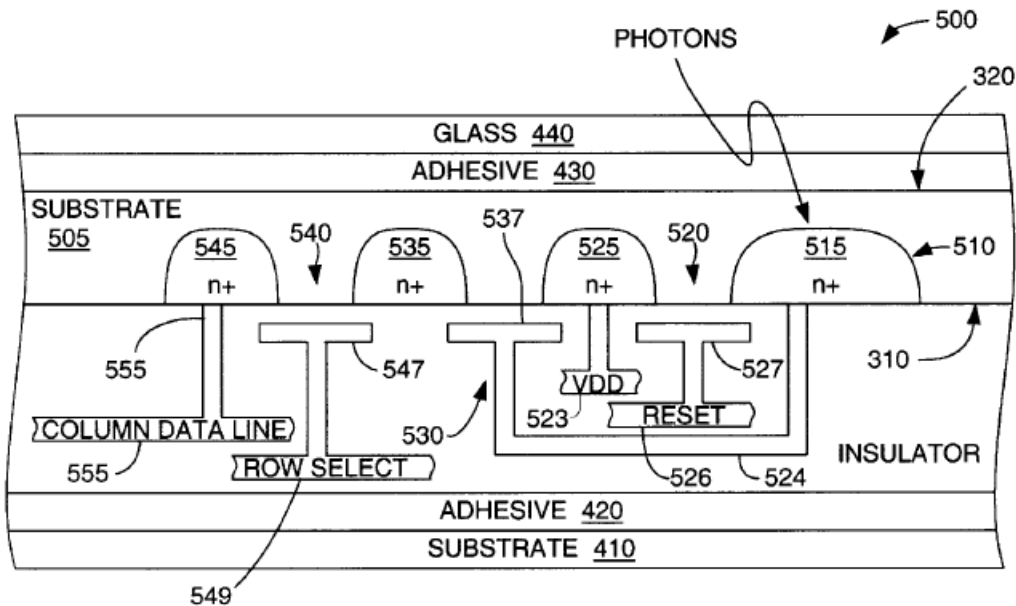


FIG. 5

Figure 5 is a simplified cross-sectional view of a portion of a back-illuminated CMOS image sensor. *Id.* at 8:64–65. As shown in Figure 5, light-sensitive pixel region or CMOS APS cell 500 is formed on first surface 310 of semiconductor substrate 505 and includes photodiode 510 formed by diffusion region 515 extending into semiconductor substrate 505

from first surface 310. *Id.* at 9:6–9. Metal line 524 is formed in an insulator material that is located adjacent first surface 310 of semiconductor substrate 505. *Id.* at 9:9–13. Protective substrate 410 is secured to semiconductor substrate 505 such that metal line 524 is located between protective substrate 410 and semiconductor substrate 505. *Id.* at 9:13–17. Transparent substrate 440 is secured to second surface 320 of semiconductor substrate 505 such that semiconductor substrate 505 is sandwiched between transparent substrate 440 and protective substrate 410. *Id.* at 9:17–20. First adhesive layer 420 is located between protective substrate 410 and semiconductor substrate 505, and second adhesive layer 430 is located between transparent substrate 440 and semiconductor substrate 505. *Id.* at 9:29–35. The '319 patent discloses that semiconductor substrate 505 “is processed by grinding, chemical etching and an optional chemical/mechanical polishing process to have a thickness defined such that light-sensitive pixel region 500 is effectively exposed through second surface 320.” *Id.* at 9:21–25.

D. Illustrative Claim

Claim 1 is reproduced below.

1. [1pre] A backside illuminated image sensor comprising:
 - [1a] a semiconductor substrate having a first surface and a second surface;
 - [1b] a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate and including a photodiode diffusion region extending into the semiconductor substrate from the first surface;
 - [1c] a metal line formed adjacent the first surface of the semiconductor substrate;
 - [1d] a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate; and

- [1e] a transparent substrate secured to the second surface of the semiconductor substrate such that the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate;
- [1f] wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface.

Ex. 1001, 11:21–42 (bracketed designations added by Petitioner).

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability.

Ground	Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1	1, 2, 5, 6	103	Nixon ²
2	3	103	Nixon, Merrill ³
3	4	103	Nixon, Watanabe ⁴
4	1, 2, 5, 6	103	Badihi ⁵
5	4	103	Badihi, Watanabe
6	1, 2, 3, 5, 6	103	Merrill, Badihi
7	4	103	Merrill, Badihi, Watanabe

In support of its unpatentability arguments, Petitioner relies on the declaration of Dr. Konstantinos P. Giapis. Ex. 1003.

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. § 103. Because the ’319 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA version of § 103.

² US 6,429,036 B1, issued August 6, 2002 (Ex. 1004).

³ US 5,789,774, issued August 4, 1998 (Ex. 1049).

⁴ JP H6-268183, published September 22, 1994 (certified translation) (Ex. 1007).

⁵ A. Badihi, *ShellCase Ultrathin Chip Size Package*, 1999 International Symposium on Advanced Packaging Materials, IEEE Cat. No. 99TH8405, pp. 236–40, March 1999 (Ex. 1101).

II. ANALYSIS

A. Claim Construction

We apply the claim construction standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). 37 C.F.R. § 42.100(b). Under *Phillips*, claim terms are afforded “their ordinary and customary meaning.” *Phillips*, 415 F.3d at 1312. The “ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Petitioner “does not believe the claim terms need to be construed to resolve the prior art issues presented in [the] Petition.” Pet. 9 (citing Ex. 1003 ¶ 56).

Patent Owner proposes a construction for the claim term “effectively exposed,” arguing that this term “should be construed as it is defined in the specification of the ’319 patent.” Prelim. Resp. 10–11. According to Patent Owner, the ’319 patent specification defines “effectively exposed” to mean “the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through second surface.” *Id.* at 10 (citing Ex. 1001, 6:48–51).

To define specific terms used to describe an invention, an inventor must do so “with reasonable clarity, deliberateness, and precision” and must

“‘set out his uncommon definition in some manner within the patent disclosure’ so as to give one of ordinary skill in the art notice of the change” in meaning. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (quoting *Intellicall, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1387–1388 (Fed. Cir. 1992)). As Patent Owner notes, the ’319 patent states that the “term ‘effectively exposed’ is used herein to indicate that the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through [the] second surface.” Ex. 1001, 6:52–55; Prelim. Resp. 10–11. This language suggests that some electron flow in response to light is necessary for a region to be “effectively exposed.” But, as Petitioner notes (Pet. 32 n.3), the ’319 patent also says that

[t]he exposed backside surface of the semiconductor substrate is then subjected to the material erosion process . . . to thin the semiconductor substrate until the semiconductor substrate is transparent to visible light, thereby effectively exposing the light-sensitive pixel diffusion regions of the image sensor circuit through the backside surface.

Ex. 1001, 4:63–5:4. This suggests that merely the transparency of the overlying structure to visible light is sufficient for the underlying structure to be “effectively exposed.”

Given the ambiguity in the present record, we do not agree with Patent Owner that the ’319 patent defines “effectively exposed” sufficiently clearly and precisely that we can conclude that it means “the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through [the] second surface.” Instead, on the present record, we synthesize the different uses of the term within the specification to arrive at a preliminary conclusion that the term means “having a semiconductor substrate that is thin enough to be transparent to visible light,

thereby rendering the pixels of the light sensitive pixel regions capable of generating electron flow in response to light (photons) passing through the substrate.” For purposes of this decision, we adopt this construction of the term “effectively exposed,” but we encourage both parties to address the construction of this term during trial.

We determine we need not expressly construe any other claim term at this stage of the proceeding. *See Realtime Data*, 912 F.3d at 1375.

B. Level of Ordinary Skill in the Art

Petitioner asserts that one of ordinary skill in the art “would have been a person having a Master’s degree in electrical engineering, computer engineering, or physics with at least two years of industry experience in integrated circuit design, layout, packaging or fabrication” and that a “greater level of experience may compensate for less education, and vice versa.” Pet. 9 (citing Ex. 1003 ¶¶ 52–55). Patent Owner “reserves the right to dispute Petitioner’s definition of a POSA [person of ordinary skill in the art] if an IPR is instituted.” Prelim. Resp. 10.

For the purposes of this Decision, we adopt Petitioner’s proposal regarding the level of one of ordinary skill in the art. The level of ordinary skill in the art is also reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Discretion under 35 U.S.C. § 314(a)

Institution of *inter partes* review is discretionary. *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he [U.S. Patent and Trademark Office] is permitted, but never compelled, to institute an IPR proceeding.”). In assessing whether to exercise such discretion, the Board weighs six non-exclusive factors, known as the *Fintiv* factors. *Apple*

Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”). Recognizing that “there is some overlap among these factors” and that “[s]ome facts may be relevant to more than one factor,” the Board “takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.* On June 21, 2022, the Director of the USPTO issued several clarifications concerning the application of the *Fintiv* factors. *See Interim Procedure For Discretionary Denials In AIA Post-Grant Proceedings With Parallel District Court Litigation*, issued June 21, 2022 (“Interim Procedure”).⁶ The Interim Procedure clarifies “the PTAB’s current application of *Fintiv* to discretionary institution where there is parallel litigation” and explains that “[c]onsistent with *Sotera Wireless, Inc.*, the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Interim Procedure 2–3 (internal footnote omitted) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A)). The Interim Procedure explains that such a *Sotera* stipulation “mitigates concerns of potentially conflicting decisions and duplicative efforts between the district court and the PTAB . . . [and] allows the PTAB to review grounds that the parallel district court litigation will not resolve.” *Id.* at 7–8.

In this proceeding, Petitioner

⁶ Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

stipulates that if the PTAB institutes *inter partes* review in relation to any petition filed by [Petitioner] with respect to the '319 patent, Petitioner will not pursue in the district court litigation any ground raised or that could have been reasonably raised in the instituted IPR with respect to the patent claim subject to the instituted IPR

and argues that “[t]his stipulation precludes discretionary denial under § 314(a).” Pet. 88–89.

Patent Owner urges us to exercise discretion to deny institution of *inter partes* review under § 314(a) in light of the parallel District Court litigation involving the '319 patent. Prelim. Resp. 11–14 (citing *Fintiv*). Patent Owner argues that “Petitioner has not filed a stipulation in district court.” *Id.* at 13. Patent Owner also argues that Petitioner’s stipulation is narrower than that in *Sotera* and is not the type of stipulation that should preclude discretionary denial. *Id.* at 13–14.

We consider the parties’ arguments in light of the *Fintiv* factors, as explained below.

1. Factor 1: Whether a Stay Exists or Is Likely to Be Granted if a Proceeding Is Instituted

Neither party has directed us to any evidence that the district court has stayed or is likely to stay the parallel proceeding, so the first factor is neutral.

2. Factor 2: Proximity of the Court’s Trial Date to the Board’s Projected Statutory Deadline

Trial in the parallel District Court litigation is scheduled to begin on May 6, 2024, approximately two and a half months before our final written decision would be due, so the second factor weighs somewhat in favor of exercising discretion to deny institution. Ex. 2004, 1.

3. *Factor 3: Investment in the Parallel Proceeding by the Court and Parties*

As of the date when our institution decision is due, there will be significant work left to do in the parallel District Court litigation, including claim construction, fact and expert discovery, and dispositive motions, so the third factor weighs against discretionary denial. *Id.* at 1–4.

4. *Factor 4: Overlap Between Issues Raised in the Petition and in the Parallel Proceeding*

According to the Interim Procedure, we should not exercise discretion to deny institution where a petitioner “stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” Interim Procedure at 7. Here, Petitioner’s stipulation uses this language but is further limited “to the patent claim subject to the instituted IPR.” Pet. 87. We agree with Patent Owner that this stipulation is “narrower” than the stipulation “that was considered by the Board in *Sotera*,” because it adds further limiting language to the model *Sotera* stipulation. Prelim. Resp. 13. Accordingly, we do not find that this stipulation implicates the Interim Procedure’s prohibition against discretionary denial where a *Sotera*-type stipulation is presented.

We do not agree with Patent Owner that the stipulation must be filed in district court. All the Interim Procedure requires is that Petitioner “stipulate[]” or “present[] a stipulation,” not that the stipulation be filed in district court. Interim Procedure at 3, 7. Accordingly, we do not discount Petitioner’s stipulation because Petitioner failed to file it in district court.

Thus, although Petitioner’s stipulation does not track the language of the model *Sotera* stipulation, it does minimize the possibility of overlapping

issues between the parallel proceeding and this proceeding, in which all claims of the '319 patent are challenged in the Petition. Accordingly, the fourth factor weighs against discretionary denial.

5. *Factor 5: Whether the Petitioner and the Defendant in the Parallel Proceeding Are the Same Party*

Petitioner here is the defendant in the District Court proceeding, so the fifth factor weighs in favor of discretionary denial.

6. *Factor 6: Other Circumstances that Impact the Board's Exercise of Discretion, Including the Merits*

Neither party raises additional circumstances impacting our exercise of discretion, so the sixth factor is neutral.

7. *Balancing the Fintiv Factors*

We have considered the circumstances and facts before us in view of the *Fintiv* factors, taking “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv* at 6. Having evaluated all of the factors, and taking into account Petitioner’s stipulation, we determine that the circumstances presented here do not warrant exercising our discretion under § 314(a) to deny institution.

D. *Reasonable Likelihood under 35 U.S.C. § 314(a)*

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)); see also 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element

of the claim is found in the prior art patents or printed publications relied upon).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) differences between the prior art and the claims at issue; (3) the level of ordinary skill in the pertinent art; and (4) when presented, objective evidence of nonobviousness, i.e., secondary considerations.⁷ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). Petitioner cannot satisfy its burden of proving obviousness by employing “mere conclusory statements,” but “must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). A reason to combine or modify the prior art may be found explicitly or implicitly in market forces; design incentives; the “interrelated teachings of multiple patents”; “any need or problem known in the field of endeavor at the time of invention and addressed by the patent”; and the background knowledge, creativity, and common sense of the person of ordinary skill. *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1329 (Fed. Cir. 2009) (quoting *KSR*, 550 U.S. at 418–421).

⁷ At this stage, Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations).

E. Ground 1

Petitioner argues that Nixon renders obvious claims 1, 2, 5, and 6. Pet. 23–35. Patent Owner disagrees. Prelim. Resp. 16–23.

1. Nixon

Nixon is a U.S. patent titled “Backside Illumination of CMOS Image Sensor.” Ex. 1004, code (54). Figure 2 of Nixon is reproduced below.

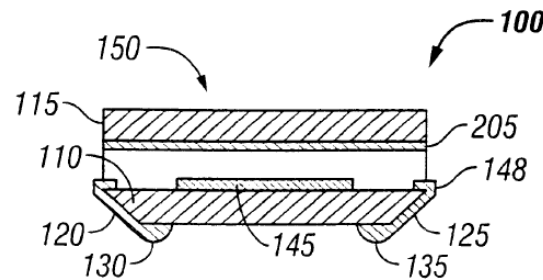


FIG. 2

Figure 2 illustrates CMOS image sensor 100 including silicon substrate 105 (*see id.* at Fig. 1 for label of silicon substrate 105) sandwiched between protective plates 110, 115. *Id.* at 2:1–3, 2:15–16. Pixels 145 are positioned on top surface 148 of silicon substrate 105. *Id.* at 2:8–9. Electrical leads 120, 125 connect to pads 130, 135 of the sensor die. *Id.* at 2:6–8. Color filter array (CFA) 205 is deposited on bottom protective plate 115. *Id.* at 2:17–19. Image sensor 100 is light sensitive along back side 150. *Id.* at 2:8–9.

2. Petitioner’s Arguments

Petitioner argues that Nixon renders obvious claim 1, as follows.

[1pre] A backside illuminated image sensor comprising: (Pet. 23–24 (citing Ex. 1003 ¶¶ 82–83; Ex. 1004, 1:8–10, Abstract, Figs. 1, 2, 4A–4G; Ex. 1005 (Nixon Provisional), 4–5, Figs. 1–2, 7–9, Fig. 4));

[1a] a semiconductor substrate having a first surface and a second surface; (Pet. 24 (citing Ex. 1003 ¶¶ 84–85; Ex. 1004, 1:65–2:10, Fig. 2; Ex. 1005, 4–5, Fig. 2, 8–9, Figs. 3–4));

[1b] a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate and including a photodiode diffusion region extending into the semiconductor substrate from the first surface; (Pet. 25–28 (citing Ex. 1003 ¶¶ 86–89; Ex. 1004, 2:8–9, Fig. 2; Ex. 1005, 4, Fig. 2, 8, Figs. 3–4; “using any one of the three well-known and available CMOS pixel implementations would have been a simple design choice that a POSITA ‘ha[d] good reason to pursue’”));

[1c] a metal line formed adjacent the first surface of the semiconductor substrate; (Pet. 28–29 (citing Ex. 1003 ¶¶ 90–92; Ex. 1004, 2:6–8, 2:20–22, 2:58–61; Ex. 1005, 4–5, Fig. 2, 8, Fig. 4; “a POSITA would readily understand that Nixon’s CMOS image sensor 100 includes the claimed ‘metal line’”));

[1d] a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate; and (Pet. 29–30 (citing Ex. 1003 ¶¶ 93–94; Ex. 1004, 2:1–6, Fig. 2; Ex. 1005, 4–5, Fig. 2, 8, Fig. 4));

[1e] a transparent substrate secured to the second surface of the semiconductor substrate such that the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate; (Pet. 30–31 (citing Ex. 1003 ¶¶ 95–97; Ex. 1004, 1:65–2:10, Abstract, 1:37–47, 2:49–57, Fig. 2; Ex. 1005, 4–5, Fig. 2, 7–8, Fig. 4));

[1f] wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second

surface. Pet. 32 (citing Ex. 1003 ¶¶ 98–99; Ex. 1004, 2:36–41, 3:7–17, 1:37–39, 1:65–2:10, Fig. 4B; Ex. 1005, 4–5, Fig. 2, 8, Fig. 4).

Petitioner presents additional arguments based on Nixon for claims 2, 5, and 6. Pet. 33–35 (citing Ex. 1003 ¶¶ 100–110).

3. Patent Owner's Arguments

First, Patent Owner argues that Nixon does not disclose or render obvious the “photodiode diffusion region” limitation of claim [1b]. Prelim. Resp. 16. More particularly, Patent Owner argues, “Nixon does not describe the photodiode diffusion region as ‘extending into the semiconductor substrate.’ Rather, it sits on top of it.” *Id.* at 17. Patent Owner disagrees that Nixon renders this claim obvious, because Petitioner’s declarant’s testimony is “conclusory.” *Id.*

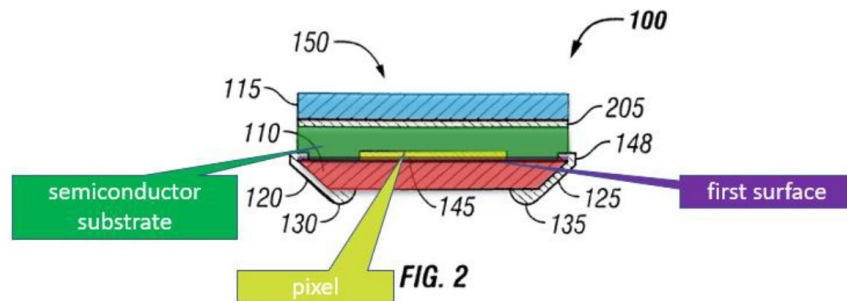
Second, Patent Owner argues that Nixon “does not disclose or render obvious the ‘protective substrate’ limitation” or the “transparent substrate” limitation. *Id.* at 18. According to Patent Owner, the alleged glass layer in Nixon corresponding to the “protective substrate” of claim 1 does not provide any structural support and, therefore, cannot provide the structural support required by the ’319 patent of its protective substrate. *Id.* at 18–19. Moreover, Patent Owner argues, the alleged glass layer in Nixon corresponding to the “‘protective substrate’ of claim 1 is a transparent substrate, not the required non-transparent protective substrate.” *Id.* at 20–21. According to Patent Owner, a “POSA would readily know that a thin glass layer disclosed by Nixon is not a non-transparent protective substrate providing structural support as claimed by the ’319 patent.” *Id.* at 21.

Finally, Patent Owner argues that Nixon does not disclose or render obvious the “effectively exposed” limitation in claim [1f]. *Id.* at 21–23.

Patent Owner faults Petitioner for presenting “no evidence that Nixon discloses that electron flow is generated with the light sensitive pixel regions (*i.e.*, the image sensor) being exposed to light (photons) after the grinding/thinning process.” *Id.* at 22. Patent Owner does not otherwise challenge Petitioner’s arguments or evidence regarding the remaining limitations.

4. Analysis

First, regarding Patent Owner’s argument that Nixon does not disclose or render obvious the photodiode diffusion region of claim [1b] (Prelim. Resp. 16), we note that claim [1b] requires a “photodiode diffusion region extending into the semiconductor substrate from the first surface.” Ex. 1001, 11:27–28. Petitioner argues that Nixon’s silicon substrate 105 and top surface 148 correspond to the claimed “semiconductor substrate” and “first surface,” respectively, and that Nixon’s pixels 145 extend into silicon substrate 105 from top surface 148, as shown in Petitioner’s annotated Figure 2, reproduced below.



Pet. 25–26. Nixon’s annotated Figure 2 depicts first surface 148 in purple, semiconductor substrate 105 in green, and pixels 145 in chartreuse. Petitioner argues that “it would have been a matter of routine, design choice to implement Nixon’s pixels 145 as *active pixels with photodiodes*, which include *photodiode diffusion regions*.” *Id.* at 27 (citing Ex. 1003 ¶ 89).

Although Patent Owner highlights Nixon's statement that pixels 145 "are positioned at the top surface 148 of the silicon substrate 105," (Ex. 1004, 2:8–9), the language of this statement does not appear to preclude the orientation depicted in Nixon's Figure 2, in which the pixels 145 appear to extend into semiconductor substrate 105. On this record, we are persuaded that Petitioner's reasoning and depictions demonstrating the orientation of Nixon's pixels 145 could support a finding that Nixon teaches a photodiode diffusion region extending into the semiconductor substrate from the first surface. *Id.* Thus, on the present record, Petitioner shows sufficiently that Nixon teaches or suggests this limitation.

Second, regarding the "protective substrate" and "transparent substrate" limitations, Nixon's "thin silicon substrate . . . is sandwiched between two thin protective plates" attached by "[a]n epoxy adhesive layer." Ex. 1004, 2:1–6. The "first glass plate," described also as "a thin protective layer," "is bonded while the active surface of the silicon wafer is facing up into the encapsulate." *Id.* at 2:22–31. Patent Owner argues that the '319 patent uses the word "protective" to mean that a protective substrate provides structural support. Prelim. Resp. 18–19 (citing Ex. 1001, code (57), 4:48–50). There is language to this effect in the '319 patent. Ex. 1001, code (57) ("With the protective substrate providing structural support"), 4:50–52 ("because the method utilizes a protective substrate to support the semiconductor substrate"). When the '319 patent makes these statements, it is discussing the invention as a whole rather than any individual embodiment. *Id.* On the present record, we are not persuaded that the '319 patent defines "protective" so clearly and precisely as to constitute a redefinition of the term under *Paulsen*. We invite both parties, within the

limits imposed by our rules, to supplement the record as to the proper interpretation of the term “protective” during trial. On the present record, we consider Nixon’s description of the first glass plate as “protective” sufficient to show, at least for purposes of institution, that this plate is “protective.” Ex. 1004, 2:1–6, 2:22–31.

Patent Owner also argues that, to constitute a protective substrate within the meaning of claim 1, a substrate must be non-transparent. Prelim. Resp. 28–29. Specifically, Patent Owner argues that the claim’s recitation of both “protective substrate” and “transparent substrate,” together with the rule that “[d]ifferent terms in the same claim usually have different meanings,” means that the protective substrate must be non-transparent. *Id.* at 28. We disagree. It is true that different terms in the same claim generally mean different things. *See Neville v. Aldridge Constr., Inc.*, 825 F. App’x 808 (Fed. Cir. 2020); *Firstface Co., Ltd. v. Apple Inc.*, 859 F. App’x 579 (Fed. Cir. 2021). This does not mean that the structures referred to by the terms in question cannot share any characteristics in common. Here, there must be a protective substrate and a transparent substrate, so there could not be a single structure that fulfills both roles. In addition, the protective substrate would need to be protective, and the transparent substrate would need to be transparent, but we are not presented with any reason that the protective substrate could not also be transparent or that the transparent substrate could not also be protective. On the present record, Petitioner shows sufficiently that Nixon discloses this limitation.

Finally, regarding the “effectively exposed” limitation, as discussed above with respect to claim construction, on the present record, we do not adopt Patent Owner’s proposed construction of the term “effectively

exposed.” Instead, we interpret the term as “having a semiconductor substrate that is thin enough to be transparent to visible light, thereby rendering the pixels of the light sensitive pixel regions capable of generating electron flow in response to light (photons) passing through the second surface.” Nixon teaches that “the silicon wafer . . . is ground to a predetermined thickness” that “allows for the light sensitive area of the die . . . to be illuminated from . . . the back side.” Ex. 1004, 2:36–41, 3:7–17, Fig. 4B. Thus, on the present record, Petitioner shows sufficiently that Nixon discloses this limitation.

We have reviewed the parties’ arguments and the cited evidence, and, on the present record, Petitioner shows sufficiently that Nixon discloses the limitations of claims 1, 2, 5, and 6. For the limitations undisputed by Patent Owner, we agree with Petitioner, based on the evidence and arguments presented in the Petition, that Nixon teaches or suggests those limitations. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claims 1, 2, 5, and 6 would have been obvious in view of Nixon.

F. Ground 2

Petitioner argues that Nixon and Merrill render obvious claim 3. Pet. 35–47. Patent Owner disagrees. Prelim. Resp. 24.

1. Merrill

Merrill is a U.S. patent titled “Active Pixel Sensor Cell That Minimizes Leakage Current.” Ex. 1049, code (54). Merrill discloses a CMOS APS cell including a photodiode combined with active transistors “which, in addition to forming an electrical signal, provide amplification, readout control, and reset control.” *Id.* at 1:34–37.

Figure 9B of Merrill is reproduced below.

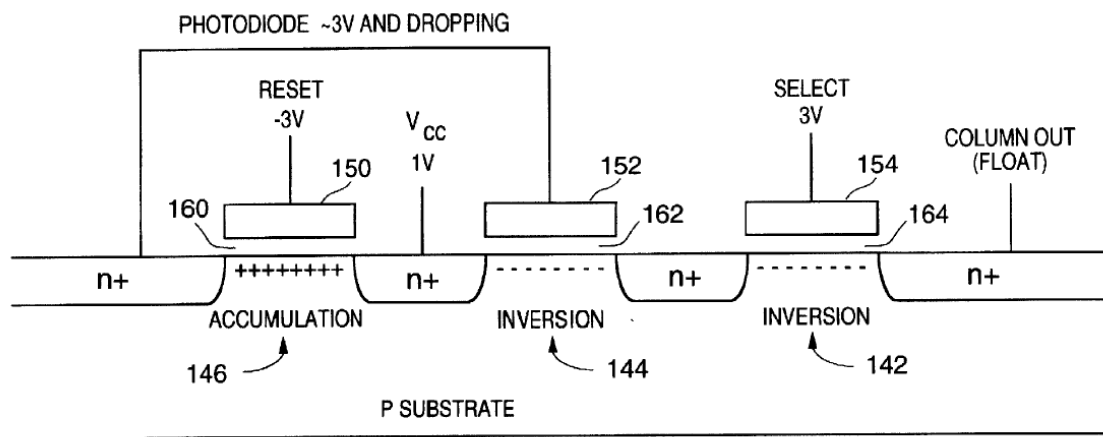


FIG. 9B

Figure 9B is a cross-sectional view of APS cell 100. *Id.* at 6:9–12 (*see id.* at Fig. 8 for label of APS cell 100). As shown in Figure 9B, APS cell 100 includes doped n regions in a p substrate to form an n⁺ photodiode and n⁺ source and drain regions for the transistors of APS cell 100. *Id.* at 5:13–17; 7:31–36. APS cell 100 further includes reset line 150 functioning as the gate of a reset transistor, local interconnect line 152 functioning as the gate of a sense transistor, and select line 154 functioning as the gate for a select transistor. *Id.* at 6:6–8, 6:41–46, 7:23–28; *see id.* at 1:38–44.

2. Analysis

Claim 3 depends from claim 1 and adds limitations reciting the orientations of diffusion regions and gate structures. Ex. 1001, 12:6–31. Petitioner argues that Nixon and Merrill teach or suggest these limitations. Pet. 35–47 (relying on Ex. 1003 ¶¶ 111–134). Petitioner also argues that one of ordinary skill in the art “would have naturally looked to Merrill’s CMOS APS with ‘a conventional photodiode . . . typically combined with a number

of active transistors’ to modify Nixon’s manufacturing process for a BSI CMOS image sensor” with a reasonable expectation of success. *Id.* at 37. On the present record, Patent Owner does not substantively dispute Petitioner’s arguments. Prelim. Resp. 24. We have reviewed Petitioner’s argument and the cited evidence, and, on the present record, Petitioner shows sufficiently that Nixon and Merrill disclose the limitations of claim 3 and one of ordinary skill in the art would have been motivated to combine them with a reasonable expectation of success. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claim 3 would have been obvious in view of Nixon and Merrill.

G. Ground 3

Petitioner argues Nixon and Watanabe render obvious claim 4. Pet. 47–51. Patent Owner disagrees. Prelim. Resp. 24.

1. Watanabe

Watanabe is a Japanese patent application publication titled “Manufacture of Semiconductor Device.” Ex. 1007, code (54). Watanabe discloses a back-thinned infrared detector including a thinned substrate bonded to an insulating supporting substrate. *Id.* at code (57).

2. Analysis

Claim 4 depends from claim 1 and adds “wherein the thickness of the semiconductor substrate is in the range of 10 to 15 microns.” Ex. 1001, 12:32–34. Petitioner argues that Nixon and Watanabe teach or suggest these limitations. Pet. 47–51 (relying on Ex. 1003 ¶¶ 135–143). Petitioner also argues that “Watanabe’s substrate thinning to a thickness of 5 to 15 microns is readily applicable to Nixon’s manufacturing process, and a POSITA could have modified Nixon’s manufacturing process to include Watanabe’s

substrate thinning to a thickness of 5 to 15 microns with a reasonable expectation of success.” *Id.* at 49. On the present record, Patent Owner does not substantively dispute Petitioner’s arguments. Prelim. Resp. 24. We have reviewed Petitioner’s argument and the cited evidence, and, on the present record, Petitioner shows sufficiently that Nixon and Watanabe disclose the limitations of claim 4 and one of ordinary skill in the art would have been motivated to combine them with a reasonable expectation of success. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claim 4 would have been obvious in view of Nixon and Watanabe.

H. Ground 4

Petitioner argues Badihi renders obvious claims 1, 2, 5, and 6. Pet. 51–64. Patent Owner disagrees. Prelim. Resp. 24–32.

1. Badihi

Badihi is an IEEE paper titled “ShellCase Ultrathin Chip Size Package.” Ex. 1101, 236. Badihi discloses a chip size package (CSP) manufacturing process applicable to CMOS image sensors. *Id.* at 236, 239.

Figure 2 of Badihi is reproduced below.

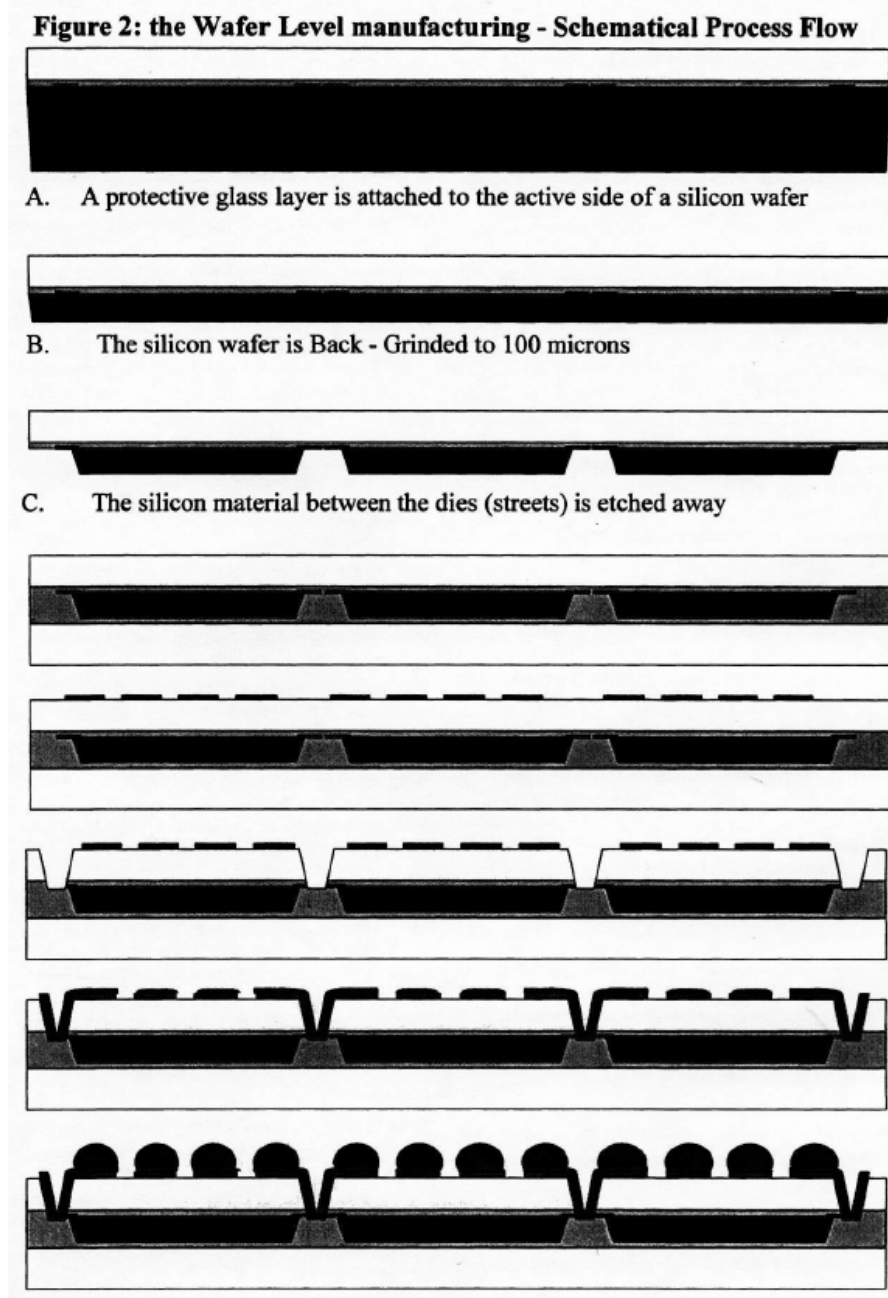


Figure 2 shows the wafer-level manufacturing process of the CSP. *Id.* at 238. As disclosed by Badihi and shown in Figure 2, the CSP manufacturing process includes the following steps: 1) A thin protective glass layer is bonded to the active side of a silicon wafer; 2) The silicon

material between dies (streets) is etched away (back side), yielding individual ICs attached to the supporting glass layer; 3) The grooves between the dies are filled with an inert material, and a second thin glass cover is bonded onto the back side of the silicon dies; 4) An organic layer is applied and patterned to act as a compliant layer underneath solder joints; 5) Deep notches are drawn between the dies, revealing cross-sections of bond pads; 6) A metal layer, patterned by lithography to individual leads, is deposited to contact the bond pads at their cross-sections and soldering leads are formed on the upper surface of the package. *Id.* at 237.

Figure 3 of Badihi is reproduced below.

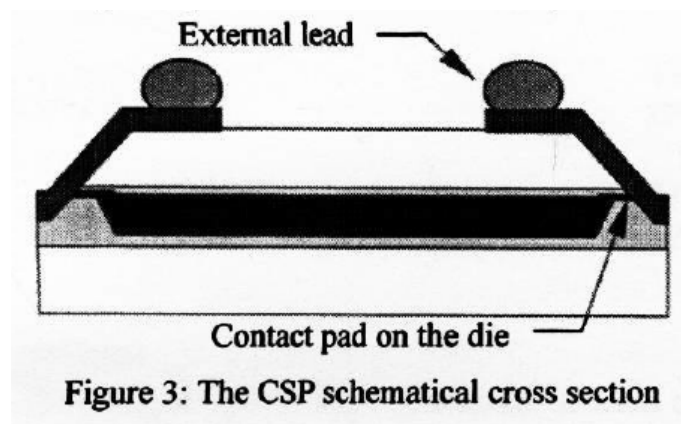


Figure 3 is a cross-sectional view of the CSP after wafer dicing yields individual packaged dies. *Id.* at 237, 239.

2. *Petitioner's Arguments*

Petitioner argues that Badihi renders obvious claim 1, as follows.

[1pre] A backside illuminated image sensor comprising: (Pet. 52–54 (citing Ex. 1003 ¶¶ 145–149; Ex. 1101, 237, 239, Figs. 2, 3; Ex. 1055, Ex. A, Fig. 4, 239; Ex. 1051, 1));

[1a] a semiconductor substrate having a first surface and a second surface; (Pet. 55 (citing Ex. 1003 ¶¶ 150–151; Ex. 1101, 237, Fig. 3));

[1b] a plurality of light-sensitive pixel regions formed on the first surface of the semiconductor substrate and including a photodiode diffusion region extending into the semiconductor substrate from the first surface; (Pet. 55–57 (citing Ex. 1003 ¶¶ 152–155; Ex. 1101, Figs. 3, 4; “it would have been a matter of routine, design choice to incorporate active pixels with photodiodes, which include photodiode diffusion regions, into Badihi’s wafer-level semiconductor processing”));

[1c] a metal line formed adjacent the first surface of the semiconductor substrate; (Pet. 57–58 (citing Ex. 1003 ¶¶ 156–157; Ex. 1101, 237, Fig. 3));

[1d] a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate; and (Pet. 58–59 (citing Ex. 1003 ¶¶ 158–159; Ex. 1101, 237, Fig. 3));

[1e] a transparent substrate secured to the second surface of the semiconductor substrate such that the semiconductor substrate is sandwiched between the transparent substrate and the protective substrate; (Pet. 59–60 (citing Ex. 1003 ¶¶ 160–161; Ex. 1101, 237, Fig. 3));

[1f] wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface. Pet. 60–61 (citing Ex. 1003 ¶¶ 162–164; Ex. 1101, Fig. 2; a “POSITA would readily understand that the purpose of grinding the silicon wafer from its backside before enclosing it in a glass transparent package is so that the photons absorbed by the remaining semiconductor substrate are closer to the photodiode for a better response”).

Petitioner presents additional arguments based on Badihi for claims 2, 5, and 6. Pet. 61–64 (citing Ex. 1003 ¶¶ 165–175).

3. Patent Owner's Arguments

First, Patent Owner argues that Badihi does not disclose or render obvious the “backside illuminated image sensor” limitation. Prelim. Resp. 24. Patent Owner also asserts that “Badihi does not disclose or suggest that its packaging process could be applied to BSI image sensors,” or that one of ordinary skill “would be motivated to apply the packaging method disclosed in Badihi for BSI image sensors.” *Id.* at 26–27.

Second, Patent Owner argues that Badihi “does not disclose or render obvious the ‘protective substrate’ limitation” or the “transparent substrate” limitation. *Id.* at 27. According to Patent Owner, the alleged glass layer in Badihi corresponding to the “protective substrate” of claim 1 does not provide any structural support and, therefore, cannot provide the structural support required by the ’319 patent of its protective substrate. *Id.* at 27–28. Moreover, Patent Owner argues, the alleged glass layer in Badihi corresponding to the “‘protective substrate’ of claim 1 is a transparent substrate, not the required non-transparent protective substrate.” *Id.* at 28–29. According to Patent Owner, a “POSA would readily know that a thin glass layer disclosed by Badihi is not a non-transparent protective substrate providing structural support as claimed by the ’319 patent.” *Id.* at 29.

Finally, Patent Owner argues that “Badihi does not disclose or render obvious the ‘effectively exposed’” limitation in claim [1f]. *Id.* at 29. Patent Owner further argues that Badihi “is directed to general back-side grinding and packaging of wafer” and Badihi “mentioned nothing whatsoever about CMOS photodiodes and/or BSI sensors,” so “no POSA reading Badihi

would understand the general back-side grinding disclosed in Badihi is to ‘effectively expose’ the BSI image sensors such that electron flow is generated with the light sensitive pixel regions (*i.e.*, the image sensor) being exposed to light (photons).” *Id.* at 30–31.

4. *Analysis*

First, regarding Patent Owner’s argument that Badihi does not disclose or render obvious a BSI sensor (Prelim. Resp. 24), Badihi teaches that its process is applicable to CMOS image sensors and CCD devices. Ex. 1101, 239. In addition, Badihi teaches an image sensor whose metal leads and solder bumps cover the front side of the sensor. *Id.* at 237, Fig. 2. This evidence could support a finding that Badihi suggests an image sensor illuminated from the back side. *Id.* Thus, on the present record, Petitioner shows sufficiently that Badihi teaches or suggests this limitation.

Second, regarding the “protective substrate” and “transparent substrate” limitations, Badihi’s “thin protective glass layer is bonded to the active side of a silicon wafer.” Ex. 1101, 237; *see* Ex. 1101, Fig. 2 (“A protective glass layer is attached to the active side of a silicon wafer.”). Patent Owner argues that the ’319 patent uses the word “protective” to mean that a protective substrate provides structural support. Prelim. Resp. 27–28 (citing Ex. 1001, code (57), 4:48–50). As discussed above, we are not persuaded that the ’319 patent defines “protective” so clearly and precisely as to constitute a redefinition of the term under *Paulsen*, and we invite both parties, within the limits imposed by our rules, to supplement the record as to the proper interpretation of the term “protective” during trial. On the present record, we consider Badihi’s description of the thin protective glass

layer as “protective” sufficient to show, at least for purposes of institution, that this layer is “protective.”

Patent Owner also argues that, to constitute a protective substrate within the meaning of claim 1, a substrate must be non-transparent. Prelim. Resp. 28–29. Specifically, Patent Owner argues that the claim’s recitation of both “protective substrate” and “transparent substrate,” together with the rule that “[d]ifferent terms in the same claim usually have different meanings,” means that the protective substrate must be non-transparent. *Id.* We disagree. It is true that different terms in the same claim generally mean different things. *See Neville*, 825 F. App’x 808; *Firstface*, 859 F. App’x 579. But this does not mean that the structures referred to by the terms in question cannot share any characteristics in common. Here, there must be a protective substrate and a transparent substrate, so there could not be a single structure that fulfills both roles. In addition, the protective substrate would need to be protective, and the transparent substrate would need to be transparent, but we are not presented with any reason that the protective substrate could not also be transparent or that the transparent substrate could not also be protective. On the present record, Petitioner shows sufficiently that Badihi discloses this limitation.

Finally, regarding the “effectively exposed” limitation, as discussed above with respect to claim construction, on the present record, we do not adopt Patent Owner’s proposed construction of the term “effectively exposed.” Instead, we interpret the term as “having a semiconductor substrate that is thin enough to be transparent to visible light, thereby rendering the pixels of the light sensitive pixel regions capable of generating electron flow in response to light (photons) passing through the second

surface.” Badihi teaches that the back surface of the wafer is ground until the wafer is 100 microns thick. Ex. 1101, Fig. 2. Petitioner directs us to evidence suggesting that the purpose of this grinding would have been to expose the back side of the light-sensitive pixel regions to light. Pet. 5 (citing Ex. 1003 ¶ 50 (citing Ex. 1020, 2:10–22, 6:10–42; Ex. 1022, 14; Ex. 1010, 144)). Thus, on the present record, Petitioner shows sufficiently that Badihi teaches or suggests this limitation.

We have reviewed the parties’ arguments and the cited evidence, and, on the present record, Petitioner shows sufficiently that Badihi discloses the limitations of claims 1, 2, 5, and 6. For the limitations undisputed by Patent Owner, we agree with Petitioner, based on the evidence and arguments presented in the Petition, that Badihi teaches or suggests those limitations. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claims 1, 2, 5, and 6 would have been obvious in view of Badihi.

I. Ground 5

Petitioner argues Badihi and Watanabe render obvious claim 4. Pet. 64–67. More particularly, Petitioner argues that “Watanabe’s substrate thinning to a thickness of 5 to 15 microns is readily applicable to Badihi’s manufacturing process, and a POSITA could have modified Badihi’s manufacturing process to include Watanabe’s substrate thinning to a thickness of 5 to 15 microns with a reasonable expectation of success.” *Id.* at 66 (citing Ex. 1003 ¶ 179). On the present record, Patent Owner does not substantively dispute Petitioner’s arguments. Prelim. Resp. 32. We have reviewed Petitioner’s argument and the cited evidence, and, on the present record, Petitioner shows sufficiently that Badihi and Watanabe disclose the

limitations of claim 4 and one of ordinary skill in the art would have been motivated to combine them with a reasonable expectation of success. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claim 4 would have been obvious in view of Badihi and Watanabe.

J. Ground 6

Petitioner argues Merrill and Badihi render obvious claims 1, 2, 3, 5, and 6. Pet. 67–83. Petitioner reasons that one of ordinary skill in the art would have been motivated to modify Merrill’s CMOS APS cells to include the wafer-level semiconductor packaging process as taught by Badihi, because “a POSITA could have used Badihi’s wafer-level semiconductor packaging process to package the CMOS APS cell as taught in Merrill with a reasonable expectation of success since it is a conventional process readily understood by a POSITA at the time of invention.” *Id.* at 67–68 (citing Ex. 1003 ¶¶ 185–186). Petitioner presents its arguments as to where it believes each element of the challenged claims is found in the combination of Merrill and Badihi. *Id.* at 69–83.

Patent Owner disagrees. Prelim. Resp. 33–34. More particularly, Patent Owner argues “neither Badihi nor Merrill even mentions a BSI sensor,” so “Petitioner’s argument that a combination of those references teaches a BSI sensor” is “through hindsight” and should be rejected. *Id.* at 33. Patent Owner also relies on its previous arguments that Badihi does not disclose the “protective substrate.” *Id.* at 34.

Regarding whether Badihi discloses the “protective substrate,” we have addressed this issue *supra* and refer to that analysis as applicable to Patent Owner’s arguments here. Regarding whether Petitioner’s

combination is based on hindsight, we disagree, on this record, that Petitioner's proposed combination impermissibly reconstructs the claimed invention. *See, e.g., In re McLaughlin*, 443 F.2d 1392, 1395 (CCPA 1971) ("Any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning, but so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made and does not include knowledge gleaned only from applicant's disclosure, such a reconstruction is proper."). Rather, Petitioner provides adequate reasoning, on this record, that Merrill's and Badihi's disclosures are relevant and applicable to BSI sensors (Pet. 69–72; Ex. 1049, Fig. 9B; Ex. 1101, 237, 239, Fig. 3), supporting its assertions with declarant testimony that provides adequate reasoning for making the combination (Ex. 1003 ¶¶ 185–191). Accordingly, on this record, Petitioner shows a reasonable likelihood of prevailing on its argument that claims 1, 2, 3, 5, and 6 would have been obvious in view of Merrill and Badihi.

K. Ground 7

Petitioner argues Merrill, Badihi, and Watanabe render obvious claim 4. Pet. 83–86. More particularly, Petitioner argues that "Watanabe's substrate thinning to a thickness of 5 to 15 microns is readily applicable to Merrill's CMOS APS with photodiodes and Badihi's manufacturing process," and "a POSITA could have modified Merrill's CMOS APS with photodiodes and Badihi's manufacturing process to include Watanabe's substrate thinning to a thickness of 5 to 15 microns with a reasonable expectation of success." Pet. 85 (citing Ex. 1003 ¶ 228). On the present record, Patent Owner does not substantively dispute Petitioner's arguments. Prelim. Resp. 34. We have reviewed Petitioner's argument and the cited

evidence, and, on the present record, Petitioner shows sufficiently that Merrill, Badihi, and Watanabe disclose the limitations of claim 4, and one of ordinary skill in the art would have been motivated to combine them with a reasonable expectation of success. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claim 4 would have been obvious in view of Merrill, Badihi and Watanabe.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one challenged claim of the '319 patent, and we institute *inter partes* review on all challenges raised in the Petition.

At this preliminary stage of the proceeding, we have not made a final determination as to the patentability of any challenged claim or any factual or legal issue underlying the patentability inquiry. Any final determination will be based on the record developed during trial. We place Patent Owner on express notice that any argument not asserted in a timely-filed Response to the Petition, or in another manner permitted during trial, shall be deemed waived, even if that argument was presented in the Preliminary Response.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that *inter partes* review is instituted on each of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this decision.

IPR2023-00372
Patent 6,169,319 B1

FOR PETITIONER:

James M. Glass
John T. McKee
Jonathan S. Tse
Andrew M. Holmes
QUINN EMANUEL URQUHART & SULLIVAN, LLP
jimglass@quinnemanuel.com
johnmckee@quinnemanuel.com
jonathantse@quinnemanuel.com
drewholmes@quinnemanuel.com

FOR PATENT OWNER:

Eric Cohen
RIMON PC
eric.cohen@rimonlaw.com