

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.,

Patent Owner.

IPR2023-00372

U.S. Patent No. 6,169,319

PATENT OWNER'S RESPONSE

UNDER 37 C.F.R. § 42.107

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Exhibit No.	Exhibit Name
2014	Declaration of Ron Maltiel
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I. INTRODUCTION

Alidouble, Inc. (“Alidouble” or “Patent Owner”) submits this Patent Owner’s Response to Taiwan Semiconductor Manufacturing Company Ltd.’s (“Petitioner” or “TSMC”) Petition challenging Claims 1-6 of U.S. Patent No. 6,169,319. For the reasons discussed below, the Petitioner has not shown that the references or combinations of references upon which Petitioner relies satisfies Petitioner’s burden to establish by a preponderance of the evidence that claims 1- 6 of the ‘319 Patent are unpatentable. *See* 35 U.S.C. § 316(e).

II. THE ‘319 PATENT

The ‘319 Patent is entitled *Backside Illuminated Image Sensor*, was filed on November 17, 1999, and issued to Yacov Malinovich and Ephie Tivon as inventors on January 2, 2001. Ex. 0001 (‘319 Patent, Coversheet) (hereinafter, “319 Patent”).

A. The Invention of the ‘319 Patent

The ‘319 Patent discloses and claims a method for producing a back-illuminated CMOS image sensor that includes a matrix of pixels that are fabricated on a semiconductor substrate that utilizes conventional CMOS fabrication processes and that minimizes the fabrication and production costs associated with conventional CMOS fabrication processes.

The ‘319 Patent discloses the semiconductor substrate is secured to a protective substrate by an adhesive so that the frontside surface of the semiconductor

substrate – the surface that is processed to fabricate the CMOS image sensor, including the matrix of pixels – so that the frontside surface faces the protective substrate.

The protective substrate provides structural support to the semiconductor substrate and exposes the backside surface of the semiconductor substrate. The ‘319 Patent discloses grinding, chemical etching, or both the exposed backside of the semiconductor substrate to thin the semiconductor substrate advantageously to a range of 10 to 15 microns.

The ‘319 Patent then discloses securing a transparent substrate to the backside surface of the semiconductor substrate so that light may transmit through the transparent substrate. Thus, the ‘319 Patent discloses sandwiching the semiconductor substrate between the transparent substrate and the protective substrate.

B. The Technology Of Backside Illuminated Image Sensors

Solid state image sensors are used in video cameras and are in integrated circuits using a complementary metal oxide semiconductor (“CMOS”) technology. These image sensors are based on a two-dimensional array of pixels where each pixel includes a sensing element – a photo diode - that is capable of converting a portion of an optical image into an electronic signal and includes circuitry to measure the intensity of light detected by the sensing element and then to generate electronic

signals are then used by other circuitry to regenerate the optical image on a display. Ex. 2014 (Declaration of Ron Maltiel, ¶¶ 39-46 (hereinafter “Maltiel Decl.”)). CMOS image sensors were first developed in 1967 and utilize the photovoltaic response. *Id.* at ¶¶ 39-46. The photo-voltaic response occurs when silicon is exposed to light. When photons in the visible and near-IR regions of the spectrum impinge on a silicon surface and have sufficient energy to create an electron-hole pair. *Id.* at ¶¶ 39-46. The number of electrons generated is proportional to the light intensity. *Id.* at ¶¶ 39-46.

CMOS image sensors (“CIS”) have benefited from advances in CMOS technology for microprocessors and application specific integrated circuits. *Id.* at ¶¶ 39-46. Shrinking lithography, coupled with advanced signal-processing algorithms provide for sensor arrays, sensor array control, and image processing on one integrated circuit manufactured using well-established CMOS techniques. *Id.* at ¶¶ 39-46.

In frontside illuminated image sensors (“FSI”), the frontside surface of the semiconductor substrate includes the image sensor, the CMOS circuitry, and metal lines, manufactured of metals or polysilicon, that connect the image sensors to the CMOS circuitry and that connect both to peripheral circuitry that controls the image sensor in general, that transmits signals off the image sensor, that receive, interpret,

and implement control signals from off the image sensor, and that provide power and power control to all the circuits and sensors. Maltiel Decl., ¶¶ 39-46

CMOS Image Sensors (CIS) may be either FSI or BSI; the difference between a BSI image sensor and an FSI image sensor is the arrangement of imaging elements in the sensor with respect to incident light to the pixel. In FSI, the photons pass through the metal wiring layers before they reach the image sensors (e.g., photo diodes):

[i]n a frontside illuminated (FSI) sensor (see Fig. 4. 1A), the light reaches the PD active region through the passivation, metallization, and inter-dielectric layers. Several are the loss mechanisms associated with the coupling of light from the frontside of the sensor the reflection of light from the metal control lines which surround the PD [photodiode]

Ex. 2001 at 95; Maltiel Decl., ¶¶ 39-46. In contrast, in a BSI image sensor, the photons reach image sensors directly from the backside without passing through the metal wiring layer on the front side:

[a] BSI sensor contains the same components as a FSI sensor but the sensor's metals are located behind the PD [photodiode]

Id. at 96; Maltiel Decl., ¶¶ 39-46.

In BSI image sensors, the photons reach photodiodes directly without passing through metal wiring layers. Maltiel Decl., ¶¶ 39-46.

Although BSI image sensors contain the same components as FSI, the BSI's metal wiring layers are located behind the photodiode with respect to the direction of photons. Maltiel Decl., ¶¶ 39-46. The main technological challenge associated

with producing BSI is the bonding of the original wafer to a protective substrate to provide structural support while the semiconductor substrate is being grinded down to a thickness of a few microns. Maltiel Decl., ¶¶ 39-46.

C. Semiconductor Manufacturing Processes

Semiconductor imaging devices, such as described in the '319 patent, can be formed on silicon wafers. In its pure, crystalline form, silicon is a poor conductor. However, by introducing specific ions or impurities into the silicon (a process known as “doping”), silicon can be made to conduct electricity in a controlled fashion. Silicon is doped to form either an “n-type region” (a region that can donate electrons) or a “p-type region” (a region that can accept electrons, which is also referred to as donating “holes”) depending on the specific ions or impurities used, with each region having unique electrical properties. To indicate relative doping concentrations, it is common to use a “+” or “-” following the doping type. Thus, a “p-type” region would have a lower doping concentration compared to a “p+ region,” which in turn would have a lower doping concentration compared to a “p++ region.” Maltiel Decl., ¶¶ 27-34, 39-46.

The n-type and p-type regions in a semiconductor are formed by shooting ions into the silicon substrate. A p-type region can be formed, for example, by implanting boron into the substrate and activating the boron by a heat treatment at a high temperature. An n-type region can be formed, for example, by implanting

phosphorus into the substrate and activating the phosphorus by a heat treatment at a high temperature. The ion implantation energy will determine how deep the ions will be embedded in the substrate, and the dose will determine the doping concentration. An additional heat treatment will diffuse the implanted ions deeper and, in every direction, away from the original implant location. Maltiel Decl., ¶¶ 27-34, 39-46.

A backside-illuminated image sensor (BSI) is an image sensor where light is sensed from the back of the silicon substrate, while the circuit that monitors the sensing and digitally processes the image signal is located on the front side. Backside sensing has the advantage of being able to sense light from the entire back of the substrate, without being blocked by circuitry that covers part of the front side. Maltiel Decl., ¶¶ 27-34, 39-46.

Backside illumination has several benefits such as increasing the quantum efficiency of the sensor. As mentioned above, backside illumination can improve quantum efficiency by allowing more light to reach the sensor. This is a major advantage over front-illuminated image sensors, which can have quantum efficiencies as low as 50%. Maltiel Decl., ¶¶ 27-34, 39-46.

Backside sensor will also reduce noise in images. This is because the light that reaches the sensor is not scattered by the circuitry on the front side. Maltiel Decl., ¶¶ 27-34, 39-46.

Backside illumination can also improve the dynamic range of images. This is the range of brightness levels that an image sensor can capture. Front-illuminated image sensors often have limited dynamic range, which can lead to washed-out or dark images. Maltiel Decl., ¶¶ 27-34, 39-46.

In the typical fabrication of semiconductor products, transistors are first created on the surface of a silicon substrate. Then, several layers of metal wires are fabricated above the transistors to connect them, with each layer separated from the next layer by an insulating layer. Maltiel Decl., ¶¶ 27-34, 39-46.

The fabrication of semiconductor products is a complex process that typically begins with the creation of a silicon wafer. The wafer is then subjected to a series of steps, including deposition, lithography, etching, and metallization. These steps are used to create the transistors, capacitors, resistors, and other components of the semiconductor product. Maltiel Decl., ¶¶ 27-34, 39-46.

A semiconductor is typically a solid chemical element or compound that conducts electricity under some specific conditions. This makes it an ideal medium to control electrical current for use in electronic products. The most commonly used semiconductor material is silicon. Semiconductor devices, typically referred to as computer chips, image sensors, die or integrated circuits, are made by depositing thin layers of metals and/or dielectrics. Maltiel Decl., ¶¶ 27-34, 39-46.

The structure of semiconductor devices requires numerous processing steps

that start with a single crystal silicon wafer, called a substrate. A processed wafer has hundreds of semiconductor products called dies. Each of these dies may have millions of transistors acting as switches. Transistors are fabricated in the substrate by modifying the structure of the substrate and by building up layers of other materials that are deposited and patterned on the substrate. The fabrication processes create active regions, which readily conduct electricity, and passive regions which are non-conducting or insulating. Maltiel Decl., ¶¶ 27-34, 39-46.

Key wafer processing technologies include the deposition of thin films of materials and also etching patterns in those materials. Deposited dielectric films are used for isolation, passivation, barrier, masking and antireflective-coating applications in ultra-large-scale integrated (ULSI) semiconductor circuits. Maltiel Decl., ¶¶ 27-34, 39-46.

Thin films of conductors and insulators can be formed into patterns by using the processes of photolithography in combination with etching. Photolithography is used to transfer a mask pattern etched into a photo mask onto a photosensitive film that has been applied on the silicon wafer's surface. The photosensitive film is called photoresist. During wafer exposure with visible or ultraviolet light, the photo mask with a desired opaque pattern prevents penetration of the light through the opaque pattern, while allowing radiation to pass through the mask's clear glass. The chemical structure of photoresist is such that the light changes its solubility in a

developing solution. The photoresist can then be locally removed from the surface of the wafer during a subsequent developing process. Maltiel Decl., ¶¶ 27-34, 39-46.

The process that immediately follows the photolithography process is the removal of material from areas of the wafer unprotected by photoresist. Various etching techniques are used for this purpose. Etching processes are characterized by their selectivity to a specific material and their degree of anisotropy (vertical etching). For example, the etching agent should attack silicon dioxide, but not photoresist or silicon. Upon completion of the etching, the etching mask is removed. Maltiel Decl., ¶¶ 27-34, 39-46.

The details of the etching process depends on the etching speed and the thickness (and variation in the thickness) of the layer being etched. The etch process is typically chosen to have a fast etch rate of the layer being etched and a slow etch of the underlining layer. This ensures that we do not penetrate the underlining layer even if a portion of the layer is etched with a minimal thickness. Maltiel Decl., ¶¶ 27-34, 39-46.

D. Image Sensor Technology

Generally, an image sensor is an electrical device which captures light and converts the light into electric signals to form an electronic representation of an image. Typically, the light receiving portions are analog circuits which, when

exposed to light, create a stored charge relative to the intensity and duration of the light striking the circuit. This charge is then read out by peripheral circuitry and often converted to digital signals usable by modern computing systems to display or store the information. Solid state image sensors are used in video cameras and are in integrated circuits using a complementary metal oxide semiconductor (“CMOS”) technology. These image sensors are based on a two-dimensional array of pixels where each pixel includes a sensing element – a photo diode - that is capable of converting a portion of an optical image into an electronic signal and includes circuitry to measure the intensity of light detected by the sensing element and then to generate electronic signals are then used by other circuitry to regenerate the optical image on a display. CMOS image sensors were first developed in 1967 and utilize the photovoltaic response. The photo voltaic response occurs when silicon is exposed to light. When photons in the visible and near-IR regions of the spectrum impinge on a silicon surface and have sufficient energy to break covalent bonds an electron, the photo voltaic effect results in the breaking covalent bonds creating an electron-hole pair. The number of electrons generated is proportional to the light intensity. Maltiel Decl., ¶¶ 34-38, 47-63.

CMOS image sensors have benefited from advances in CMOS technology for microprocessors and application specific integrated circuits. Shrinking lithography, coupled with advanced signal-processing algorithms provide for sensor arrays,

sensor array control, and image processing on one integrated circuit manufactured using well-established CMOS techniques. Pixels, however, cannot shrink indefinitely or they will have an insufficient light-sensitive area. In addition, shrinking lithography provides reduced metal-line widths that connect CMOS transistors and buses in the pixel array and allows for greater density of pixels. Image sensors are optimized by increasing density with photo-diodes adequate to capture sufficient density of light. Optimization may be measured in a number called the “fill factor.” Maltiel Decl., ¶¶ 34-38, 47-63.

In frontside illuminated image sensors, the frontside surface of the semiconductor substrate includes the image sensor, the CMOS circuitry, and metal lines, manufactured of metals or polysilicon, that connect the image sensors to the CMOS circuitry and that connect both to peripheral circuitry that controls the image sensor in general, that transmits signals off the image sensor, that receive, interpret, and implement control signals from off the image sensor, and that provide power and power control to all the circuits and sensors. Maltiel Decl., ¶¶ 34-38, 47-63.

The presence of the metal and polysilicon lines associated reduces the amount of light that reaches the photodiode region resulting in a non-optimal fill factor. The reduction of metal-line width associated with more recent CMOS fabrication processes exposes more silicon to light but, even very thin metal lines the density of the metal lines and the circuitry still block significant amounts of light, thereby

preventing frontside illuminated image sensors from achieving optimal fill factor. Maltiel Decl., ¶¶ 34-38, 47-63.

Backside illuminated image sensors are an alternative that address the fill factor problems associated with front illumination. Backside illuminated image sensors receive light through the backside surface of the semiconductor substrate. As the photo-diode is fabricated on the front-side surface, to detect light from the backside, the semiconductor substrate must be extremely thin (i.e., in the range of 15 to 20 microns). While backside illuminated image sensors improve on the fill factor problems associated with frontside illuminated sensors, conventional methods for fabricating backside illuminated image sensors are expensive. Most notably, many conventional methods require non-standard fabrication process steps, such as boron doping and diffusion of special metal films that vary from standard CMOS processes. In addition, packaging of backside illuminated image sensors was typically performed after image sensor fabrication is completed - such as after the pixel array was fabricated on a semiconductor substrate, backside treatment of the semiconductor substrate, segmenting the image sensors, mounting the image sensor onto a permanent Substrate, and thinning the semiconductor substrate. The post-production packaging of backside illuminated image sensors is logistically complex and increases production costs. Maltiel Decl., ¶¶ 34-38, , 47-63.

The '319 patent teaches how to fabricate backside illuminated image sensor

composed of a pixel matrix array. The control circuitry (120) and the pixel array matrix (110) are initially fabricated on the front side of the wafer. The pixel matrix (110, green) is an array of photodiodes that are fabricated on the front side of the silicon wafer and extend into the wafer, as shown in Figure 3(B) below. Maltiel Decl., ¶¶ 34-38, 47-63.

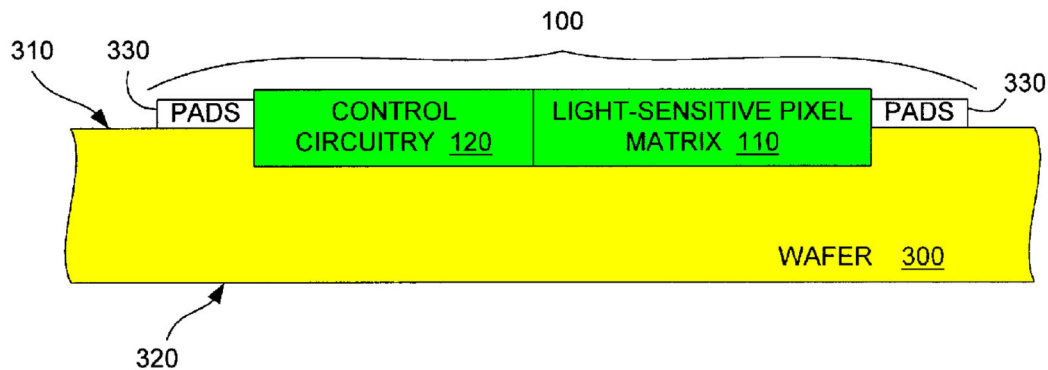


FIG. 3(B)

Following the fabrication of the control circuit and the pixel matrix on the first side of the wafer (310), “A first adhesive layer 420 is deposited onto protective substrate 410, and then wafer 300 is placed onto protective substrate 410 such that first surface 310 contacts the deposited adhesive layer 410.” ‘319 patent, CC 6:36-40. It is easier to minimize the number of particles surrounding a protective substrate when the adhesive is applied to it. This helps to ensure that the surface remains clean and free of particles, which reduces the exposure of the wafer to an environment with potential particles. Maltiel Decl., ¶¶ 34-38, 47-63.

Figure 4(C) shows the back side of the wafer (320) facing up, and the front facing down. The back side of the wafer is grounded and etched to a thickness range of 10 to 15 microns (T2).

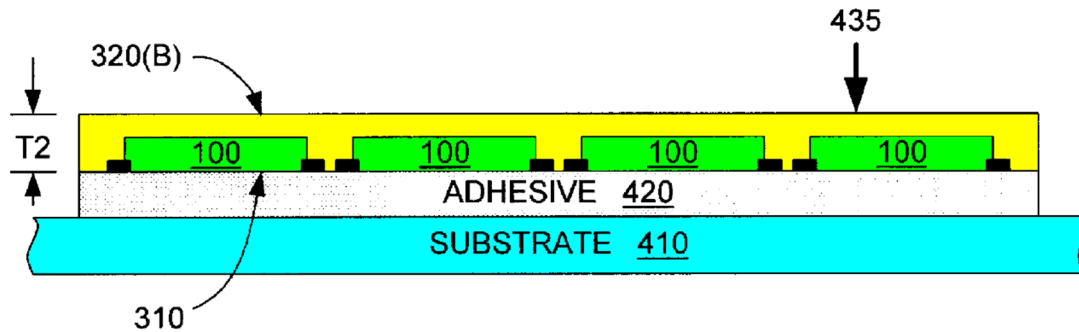


FIG. 4(C)

The Thickness of the remaining silicon layer T2 is a critical parameter. It must be thick enough to generate enough electrons from photons shining on the back side, but thin enough to allow those electrons to be collected by the photodiode on the front of the wafer. Maltiel Decl., ¶¶ 34-38, 47-63.

Individual image sensor circuits (100, green) are separated by creating grooves (437) between patterned photoresist (436, purple), as shown in fig4(D) below. Maltiel Decl., ¶¶ 34-38, 47-63.

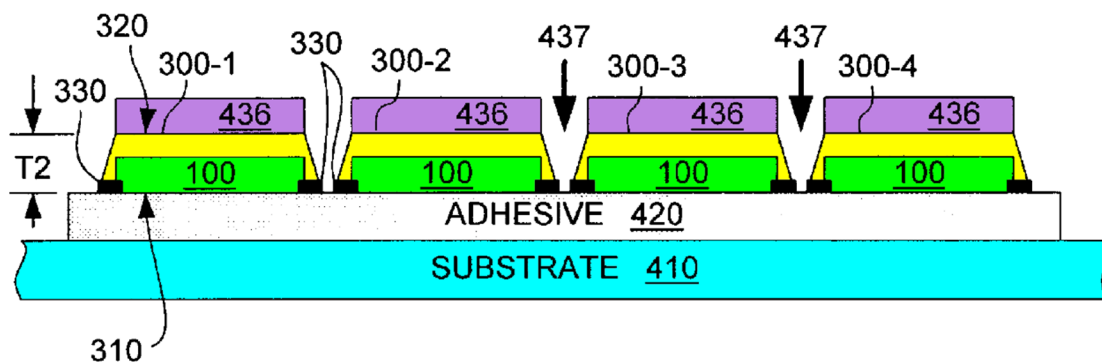


FIG. 4(D)

In the next step adhesive 430 is applied the back side of the silicon wafer (300, yellow) followed by an attachment of transparent glass (440, pink) to the adhesive 430, as shown in fig 4(E). Maltiel Decl., ¶¶ 34-38, 47-63.

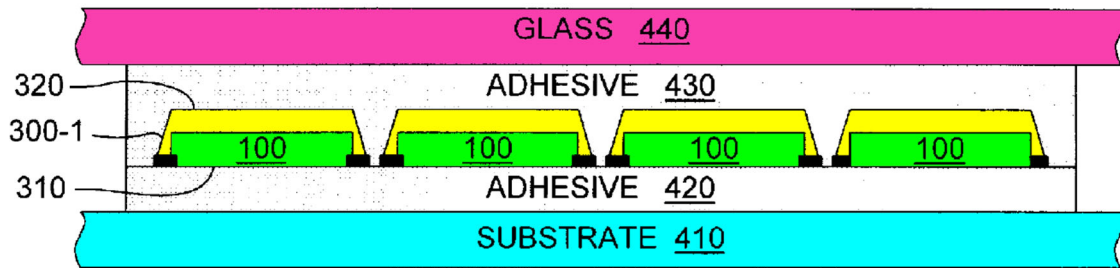


FIG. 4(E)

The next few figures (4(D), 4(E)) are flipped relative to Figure 4(C), with the front side of the wafer facing up and the back side facing down. The front side of the wafer is facing up because it is the side that was exposed to the next few fabrication steps. Maltiel Decl., ¶¶ 34-38, 47-63.

To separate the dies, grooves (455) are created between them as shown in figure 4(F). Maltiel Decl., ¶¶ 34-38, 47-63.

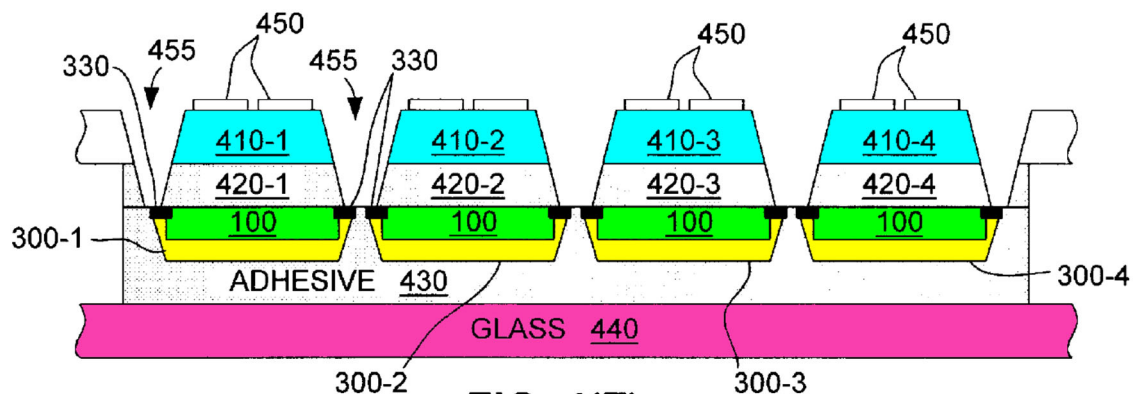
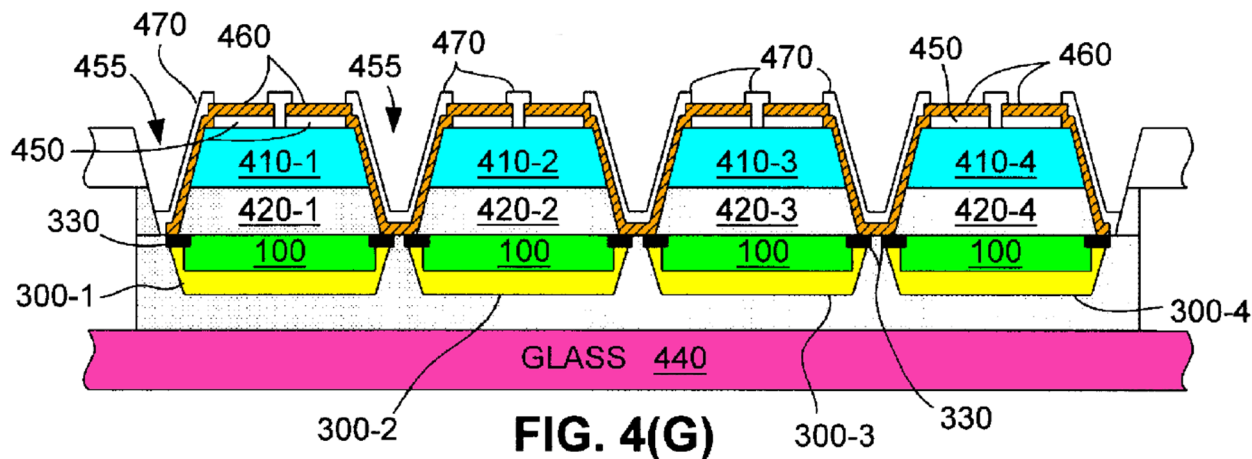


FIG. 4(F)

In the next steps metal lines (460, red) will be deposited to connect the pads

(330, black), which are adjacent to the pixels (100, green) as shown below in figure 4(G). Maltiel Decl., ¶¶ 34-38, 47-63.



Slicing “waferwise sandwich” producing plurality of backside illuminated image sensor. Maltiel Decl., ¶¶ 34-38, 47-63.

III. PERSON OF ORDINARY SKILL

The ‘319 Patent describes and claims an invention relating to “[a] method for producing a back-illuminated CMOS image sensor” ‘319 Patent, Abstract. After reviewing the ‘319 Patent’s specification, claims and prosecution history, a POSITA would have at least a bachelor’s degree in electrical engineering, chemical engineering, or material science. In addition, a POSITA would have 3-5 years’ experience that includes some experience in image sensors. Maltiel Decl., ¶¶ 25-26.

IV. CLAIM CONSTRUCTION

A. Claim Construction Standard

In *inter partes* review, patent claims are construed under the *Phillips* standard,

37 C.F.R. § 42.100, according to their “ordinary and customary.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005) (*en banc*); 37 C.F.R. § 42.100(b). Under *Phillips*, “the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

B. Terms for Construction

1. “Effectively Exposed” – Claim 1

Claim 1 is the only independent claim and includes the limitation “effectively exposed.” ‘319 Patent, 11:40-42. “Effectively exposed” is properly interpreted as the specification defines it:

the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through second surface.

Ex. 1001, 6:48-51 (“The term ‘effectively exposed’ herein is used to indicate ...”).

An inventor may define specific terms used to describe invention. *See In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994); *Commscope Tech. LLC v. Dali Wireless, Inc.*, 20223 WL 5053347 (Patent Tr. & App. Bd. July 21, 2023) (citing *In re Paulsen*, 30 F.3d at 1480). In addition, the Manual for Patent Examining Practice states:

an applicant is entitled to be his own lexicographer; where an explicit definition is provided by the applicant for a term, that definition will control interpretation of the term as it is used in the claim

Manual for Patent Examining Practice 2111.01.IV.A.

2. “Protective Substrate” – Claim 1

Claim 1 includes a limitation, “a protective substrate” that should be construed to require that the protective substrate provide structural support to the semiconductor substrate.

The abstract of the ‘319 patent discloses that “the *protective substrate provid[es] structural support*” . . . ‘319 Patent, Abstract (emphasis added). The specification further explains that “because the method utilizes *a protective substrate to support the semiconductor substrate*, the thinning process is less expensive to perform.” *Id.* at 4:48-50 (emphasis added). The intrinsic disclosure is consistent with the plain and ordinary meaning as understood by a POSITA that the protective substrate is configured to provide structural support to the semiconductor substrate. Maltiel Decl., ¶¶ 83-84; Ex. 2001 at 2 (disclosing that the main technological challenge associated with producing BSI is the bonding of the original wafer containing photodiodes to a protective substrate to provide structural support while the original wafer is being grinded down to a thickness of a few microns); Ex. 2002 at 476 (discussing the challenges that backside grinding increases chip failures because of die cracks by stating “[h]owever, die cracks still originate from flaws on

the back side due to backgrinding operations used to manufacture thin packages."); Ex. 2003 at 1 (discussing backside grinding induces damage in the wafer that leads to crack propagation by stating "[g]rind processes will induce damage in the wafer backsurface that can lead to crack propagation, growth, and fracture).

V. SUMMARY OF PETITIONER'S CITED REFERENCES

Petitioner cites references, Nixon, Badihi, and Merrill as primary references.

A. Nixon

Nixon is a U.S. patent claiming priority to the Nixon Provisional Application. The Nixon Provisional Application includes two documents: (1) an Invention Disclosure Technical Description ("IDTD"); and (2) an article entitled "A CSP Optoelectronic Package for Imaging and Light Detection Applications" by Shweky et al. ("Shweky"). The IDTD has very limited information with an only one and half page written description and two hand-sketched figures. *See* Ex. 1005, 4-6. Also, there is nothing in the IDTD indicating that Shweky is incorporated as a prior art reference, and the IDTD discloses the exact same method as discussed in Shweky. *Id.*

B. Badihi

Badihi is a printed publication published in the Proceedings International Symposium of Advanced Packaging Materials, Processes, Properties and Interfaces. Ex. 1101. The paper is entitled: *Shell Case Ultrathin Chip Size Package*, and is not

related to backside image sensor processing. *Id.*; Maltiel Decl., ¶ 73. Thus, as discussed in detail below, it is not obvious for a POSA to apply the method disclosed in Badihi for manufacturing BSI image sensors.

C. Merrill

Merrill is a U.S. patent titled “Active pixel sensor cell that minimizes leakage current,” which does not describe BSI image sensors. Merrill discloses a CMOS APS cell including a “conventional photodiode ... typically combined with a number of active transistors”. Ex. 1049, 1:31-45, 6:13-18.

VI. APPLICABLE LEGAL STANDARD

Petition only asserts grounds based on obviousness, 35 U.S.C. Section 103. The Supreme Court has determined that when analyzing a claim for validity under Section 103:

a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 418-19 (2007). For this reason:

it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does

Id. at 418. “One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art.” *In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir.

1988).

[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.

KSR Int'l Co., 550 U.S. at 418. “This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.” *Id.* at 418-419. For this reason, “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.” *Id.* at 418. “One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art.” *In re Fine*, 837 at 1075.

“[M]ere conclusory statements” are not sufficient. *Wowza Media Sys., LLC v. Adobe Sys. Inc.*, IPR2013-00054, 2013 WL 5653113, at *8 (Patent Tr. & App. Bd. April 8, 2013). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). The burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

To carry its burden, a petitioner must both:

clearly point out the differences between the claimed invention and [the prior art] and

explain why a person of ordinary skill in the art would have found the claimed subject matter obvious in spite of those differences.

Synopsys, Inc. v. Mentor Graphics Corp., IPR2012-00041, 2013 WL 3355865 at *8 (Patent Tr. & App. Bd. Feb. 22, 2013). A petitioner must specifically recite where the challenged limitation is found in the secondary reference(s) and must explain why a POSITA would have modified the primary reference with the recited limitation from the secondary reference(s). *See Microsoft Corp. v. Secure Web Conf Corp.*, IPR2014-00745, 2014 WL 4925718, at *6-7 (P.T.A.B. Sept. 29, 2014).

VII. THE CITED REFERENCES DO NOT INVALIDATE THE CHALLENGED CLAIMS

A. Ground 1: Nixon Does Not Render Claims 1, 2, 5, 6 Obvious

1. Claim 1

Petitioner has failed to carry its burden of establishing that Nixon renders Claim 1 obvious. *Harmonic Inc.*, 815 F.3d at 1363; *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d at 1378.

a. “Effectively Exposed”

The material limitation "effectively exposed" is recited in Claim 1:

wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface.

‘319 Patent, 11:39-42. As explained above in Section IV.B.1, the inventors define the "effectively exposed" limitation to require "the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through second

surface.”

Petitioner asserts that this limitation is disclosed because Nixon discloses:

removing material from the second surface of the wafer to "a predetermined thickness that allows for the light sensitive area of the die 430 to be illuminated from ... the back side."

Pet. at 32. Petitioner, however, has presented no evidence that Nixon discloses that electron flow is generated with the light sensitive pixel regions (*i.e.*, the image sensor) is exposed to light (photons) after the grinding/thinning process. A POSITA would have known that the grinding/thinning process is not exclusively for exposing light-sensitive pixel regions to generate electron flow. *See e.g.*, Ex. 2002 at 20, 66, 71, 74 (discussing flip-chip, *i.e.*, back-side processed chips, have general advantages in decreasing electromagnetic effects, increasing interconnection capability, and their applications in high performing I/O packaging, all of which have nothing to do with effectively exposing CMOS photodiodes whatsoever); Ex. 2005 (in its Abstract: "[t]his paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in packaging, *i.e.*, a technology for processing silicon dies with a thickness of 100 um or less and a technology for handling thinning ultrasmall dies."); Ex. 2006. 2007, 2008 (where the grinding/thinning process is performed in general semiconductor packaging rather than image sensors). Ex. 2003 at 1 (discussing dies with back-grinding are routinely

used for its advantage of better heat dissipation, which is important for high-power RF chips. Thus back-grinding process is routinely used in packaging technology that has nothing to do with effectively exposing CMOS photodiodes.) Thus, the grinding/thinning process is not just/inclusively for image sensors, i.e., for exposing light-sensitive pixel regions to generate electron flow. Maltiel Decl., ¶¶ 78-79.

Indeed, electron flow would not necessarily be generated when the light-sensitive pixel regions of each image sensor circuit are illuminated because, for example, there may be an illumination threshold that has to be reached before electron flow is generated. *See e.g.*, Ex. 2009 (discussing how the threshold of silicon photodiodes should be designed to reduce noise interference and yet preserve high sensitivity); Ex. 2010 (discussing how to improve threshold uniformity among photodiodes in an array to increase the quality of imaging); Ex. 2011 (discussing how to tune thresholds of photodiodes to reduce current contamination to neighboring photodiodes, e.g., antiblooming photodiodes); Ex. 2012 (indicating the threshold of the photodiodes used in the research is lower than 5V). Maltiel Decl., ¶¶ 78-79.

Accordingly, this material limitation "effectively exposed" would not be rendered obvious by Nixon.

b. “Protective Substrate”

Claim 1 includes a limitation “protective substrate,” ‘319 Patent, 11:20-

41specifically, “securing the wafer onto a protective substrate such that the first surface faces the protective substrate.” Nixon does not disclose, teach, or suggest the “protective substrate,” so does not render Claim 1 obvious.

The alleged glass layer in Nixon does not provide any structural support. Maltiel Decl., ¶¶ 83-85.

Contrary to Petitioner's arguments, Nixon does not disclose a “protective substrate.” In Nixon, the supposed "protective substrate" asserted by Petitioner is just a thin layer of glass permitting light to go through. *See* Pet. at 29. Petitioner has presented no evidence that the identified thin layer of glass in Nixon provides any structural support. In contrast, the protective substrate in the '319 patent would have been designed to be thick enough to fulfill the purpose of providing structural support.

Nixon does not disclose, teach, or suggest a protective substrate that provides structural support according to Claim 1. Maltiel Decl., ¶¶ 83-85. A POSITA would readily know that a thin glass layer disclosed by Nixon is not a protective substrate providing structural support. Accordingly, Nixon does not render Claim 1 obvious.

c. “photodiode diffusion region”

Claim [1b] recites “a photodiode diffusion region extending into the semiconductor substrate from the first surface.” Although Petitioner argues with reference to Nixon’s Fig. 2 that “pixels 145 extend[] into silicon substrate 105 from

top surface 148”, Pet. at 25, that is not how the Nixon reference describes Fig. 2. Describing Fig. 1, Nixon states that “[p]ixels 145 are positioned at the top surface 148 of the silicon substrate 105.” Ex. 1004, 2:8-9. With respect to Fig. 2, Nixon states that “[f]ig. 2 illustrates the image sensor 100 of Fig. 1 modified to include a color filter array (CFA) 205.” *Id.*, 2:15-16. Thus, Nixon does not describe the photodiode diffusion region as “extending into the semiconductor substrate.” Rather, it sits on top of it. Maltiel Decl., ¶¶ 80-81.

Nor does Nixon render this limitation obvious. The conclusory statement of Petitioner’s expert does not establish otherwise. In this case, Petitioner’s expert merely parrots the petition. This is not evidence. *See, e.g., Xerox Corp. et al. v. Bytemark, Inc.*, IPR2022-00624, Paper 12 at 4-5 (P.T.A.B. Feb. 10, 2023) (expert declaration that offered conclusory assertions without underlying factual support and repeated, *verbatim*, Petitioner’s conclusory arguments given little weight); *Unirac, Inc. v. Ecofasten Solar, LLC*, IPR2021-00532, 2021 WL 3116853, at *7 (P.T.A.B. July 22, 2021) (denying institution where “Petitioner’s witness merely parrots the conclusory statements of Petitioner”); *Unified Patents Inc. v. GE Video Compression, LLC*, IPR2019-00726, 2019 WL 3714386, at *11 (P.T.A.B. Aug. 6, 2019) (giving little weight to expert testimony that “simply parrots the Petition without providing any basis for his opinion” and denying institution); *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) (“conclusory expert

testimony is inadequate to support an obviousness determination”); *Elbit Sys. of Am., LLC v. Thales Visionix, Inc.*, 881 F.3d 1354, 1359 (Fed. Cir. 2018) (“Attorney argument is not evidence.”) (quoting *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017)); *Free-Flow Packaging Int’l, Inc. v. Automated Packaging Sys., Inc.*, IPR2016-00447, Paper 7, at 10 (P.T.A.B. June 22, 2016) (denying institution where the petitioner’s expert did “nothing more than parrot the language of the Petition word for word”).

2. Claim 2

Because Nixon fails to render claim 1 obvious, it follows that Claim 2 that depends on Claim 1 is not obvious. *See Rembrandt Wireless Techs., LP v. Samsung Elecs. Co.*, 853 F.3d 1370, 1380 (Fed. Cir. 2017) (citing, *In re Fine*, 837 F.2d at 1076 (“Dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.”)).

3. Claim 5

Because Nixon fails to render Claim 1 obvious, it follows that Claim 5 that depends on Claim 1 is not obvious. *See Rembrandt Wireless Techs.*, 853 F.3d at 1380.

4. Claim 6

Because Nixon fails to render Claim 6 obvious, it follows that Claim 6 that depends on Claim 1 is not obvious. *See Rembrandt Wireless Techs.*, 853 F.3d at

1380.

B. Ground 2: Nixon In View Of Merrill Does not Render Claim 3 Obvious

Petitioner has failed to carry its burden of establishing that Nixon in view of Merrill renders Claim 3 obvious. *Harmonic Inc.*, 815 F.3d at 1363; *Dynamic Drinkware*, 800 F.3d at 1378.

Claim 3 depends from Claim 1. Nixon fails to render claim 1 obvious. Petitioner did not cite Merrill against Claim 1. Thus, Petitioner has not carried its burden of establishing that Nixon in view of Merrill renders Claim 3 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

C. Ground 3: Nixon In View Of Watanabe Does not Render Claim 4 Obvious

Claim 4 depends from Claim 1. Nixon fails to render claim 1 obvious. Petitioner did not cite Watanabe against Claim 1. Thus, Petitioner has not carried its burden of establishing that Nixon in view of Merrill renders Claim 3 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

D. Ground 4: Badihi Does Not Render Claims 1, 2, 5, and 6 Obvious

1. Claim 1

a. “Backside Illuminated Sensors”

Claim 1 includes the limitation “backside illuminated sensors.” ‘319 Patent, 11:22. Badihi does not disclose or render obvious the “backside illuminated image sensors” limitation. Maltiel Decl., ¶¶ 96-97.

Petitioner admits that Badihi's disclosures are not specific to image sensors. Pet. at 52, 70. Badihi is directed to general back-side grinding and packaging of wafer that may not have any implication to BSI image sensors. *See e.g.*, Ex. 2002 at 20, 66, 71, 74 (discussing flip-chip, i.e., back-side processed chips, have general advantages in decreasing electromagnetic effects, increasing interconnection capability, and their applications in high performing I/O packaging, all of which have nothing to do with BSI image sensors)); Ex. 2005 (in its Abstract: "[t]his paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in packaging, i.e., A technology for processing silicon dies with a thickness of 100 um or less and a technology for handling thinning ultrasmall dies."); Ex. 2006, 2007, 2008 (where the grinding/thinning process is performed in general semiconductor packaging rather than image sensors); Ex. 2003 at 1 (discussing dies with back-grinding are routinely used for its advantage of better heat dissipation, which is important for high-power RF chips. Thus back-grinding process is routinely used in packaging technology that has nothing to do with BSI image sensors).

Petitioner asserts that POSITA would understand "Badihi could be used for BSI CMOS image sensors," citing Petitioner's parroting conclusory statement as support. Pet. at 70. The conclusory statement of Petitioner's expert cannot establish that a POSITA would understand that the general packaging process taught by

Badihi could be used for BSI image sensors. Maltiel Decl., ¶¶ 96-97. *Compare, e.g.,* Pet. at 52-54 *with* Ex. 1003 ¶¶ 145-149 (parroting same argument with the use of same annotated Figures). *See, e.g., Xerox Corp. et al.*, IPR2022-00624, Paper 12 at 4-5 (expert declaration that offered conclusory assertions without underlying factual support and repeated, *verbatim*, Petitioner’s conclusory arguments given little weight); *Unirac, Inc.*, IPR2021-00532, 2021 WL 3116853, at *7 (denying institution where “Petitioner’s witness merely parrots the conclusory statements of Petitioner”); *Unified Patents Inc.*, IPR2019-00726, 2019 WL 3714386, at *11 (giving little weight to expert testimony that “simply parrots the Petition without providing any basis for his opinion” and denying institution); *TQ Delta, LLC*, 942 F.3d at 1359 (“conclusory expert testimony is inadequate to support an obviousness determination”); *Elbit Sys. of Am., LLC*, 881 F.3d at 1359 (“Attorney argument is not evidence.”) (quoting *Icon Health & Fitness, Inc.*, 849 F.3d at 1043); *Free-Flow Packaging Int’l, Inc.*, IPR2016-00447, Paper 7 at 10 (denying institution where the petitioner’s expert did “nothing more than parrot the language of the Petition word for word”).

Moreover, Badihi does not disclose or suggest that its packaging process could be applied to BSI image sensors. Maltiel Decl., ¶¶ 96-97. Although Badihi discloses that its packaging process can be readily applied to silicon light detectors, CMOS image sensors, and CCD devices. Pet. at 52, 70; Ex. 1101 at 239, “a claimed

species or subgenus is encompassed by a prior art genus is not sufficient by itself to establish a prima facie case of obviousness.” *In re Baird*, 16 F.3d 380, 382, 29 USPQ2d 1550, 1552 (Fed. Cir. 1994); MPEP 2144.08 – Obviousness of Species When Prior Art Teaches Genus. Because a claimed species (*e.g.*, BSI image sensors) may be encompassed by a disclosed genus (*e.g.*, CMOS image sensors) does not render that species obvious, Petitioner has presented no evidence that a POSA would be motivated to apply the packaging method disclosed in Badihi for BSI image sensors.

In this regard, Badihi does not disclose how its packaging process should be applied to BSI image sensors, and there is nothing in the prior art that even suggests how to do it. Maltiel Decl., ¶¶ 96-97. Thus, Petitioner has presented no evidence that a POSA would be motivated to apply the packaging method disclosed in Badihi for BSI image sensors.

b. “Protective Substrate”

Claim 1 recites “a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate.” Ex. 1001, 11:20-41. Badihi does not disclose, teach, or suggest the “protective substrate,” so does not render Claim 1 obvious.

The alleged glass layer in Badihi does not provide any structural support. Maltiel Decl., ¶¶ 99-100.

Contrary to Petitioner's arguments, Badihi does not disclose a “protective substrate.” In Badihi, the supposed "protective substrate" asserted by Petitioner is just a thin layer of glass permitting light to go through. *See* Pet. at 58, 75. Petitioner has presented no evidence that the identified thin layer of glass in Badihi provides any structural support. In contrast, the protective substrate in the '319 patent would have been designed to be thick enough to fulfill the purpose of providing structural support. Maltiel Decl., ¶¶ 99-100.

Badihi does not disclose, teach, or suggest a protective substrate that provides structural support according to Claim 1. Maltiel Decl., ¶¶ 99-100. A POSITA would readily know that a thin glass layer disclosed by Badihi is not a protective substrate providing structural support. Accordingly, Badihi does not render Claim 1 obvious.

c. “Effectively Exposed”

Badihi does not disclose or render obvious the “effectively exposed” limitation of Claim 1.

Claim 1 recites:

wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface.

‘319 Patent, 11:39-42. As explained above in Section IV.B.1, the inventors define the "effectively exposed" limitation in the ‘319 patent to require “the pixel of each light-sensitive pixel region generates electron flow in response to light (photons)

passing through second surface.”

Petitioner asserts that Badihi discloses that:

the process step where the silicon wafer is grinded from its backside until 100 microns is left . . . A POSIT A would readily understand that the purpose of grinding the silicon wafer from its backside before enclosing it in a glass transparent package is so that the light-sensitive pixel regions are exposed from the backside of the silicon wafer.

Pet. at. 60-61. Petitioner’s argument is a conclusory statement that should be ignored because it is without any support.

First, as previously discussed, Badihi is directed to general backside grinding and packaging of wafer. *See* Section V.B. Backside grinding was routinely known in the semiconductor packaging industry for advantages not related to image sensing. Maltiel Decl., ¶¶ 92-95; *see e.g.*, Ex. 2002 at 20, 66, 71, 74 (discussing flip-chip, *i.e.*, back-side processed chips, have general advantages in decreasing electromagnetic effects, increasing interconnection capability, and their applications in high performing I/O packaging, all of which have nothing to do with effectively exposing CMOS photodiodes whatsoever); *see also* Ex. 2005 (in its Abstract: “[t]his paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in packaging, *i.e.*, A technology for processing silicon dies with a thickness of 100 um or less and a technology for handling thinning ultrasmall dies.”); *see also* Ex. 2006, 2007, 2008 (where the grinding/thinning process is performed in general

semiconductor packaging rather than image sensors); *see also* Ex. 2003 at 1 (discussing dies with back-grinding are routinely used for its advantage of better heat dissipation, which is important for high-power RF chips. Thus, back-grinding process is routinely used in packaging technology that has nothing to do with effectively exposing CMOS photodiodes); Maltiel Decl., ¶¶ 92-95. Second, Badihi does not, teach, or suggest CMOS photodiodes or BSI sensors, or both. No POSITA reading Badihi would understand the general back-side grinding disclosed in Badihi is to “effectively expose” the BSI image sensors such that electron flow is generated with the light sensitive pixel regions (i.e., the image sensor) being exposed to light (photons). Maltiel Decl., ¶¶ 92-95.

Indeed, electron flow would not necessarily be generated when the light-sensitive pixel regions of each image sensor circuit are illuminated because, for example, there may be an illumination threshold that has to be reached before electron flow is generated. *See e.g.*, Ex. 2009 (discussing how the threshold of silicon photodiodes should be designed to reduce noise interference and yet preserve high sensitivity); *see also* Ex. 2010 (discussing how to improve threshold uniformity among photodiodes in an array to increase the quality of imaging); *see also* Ex. 2011 (discussing how to tune thresholds of photodiodes to reduce current contamination to neighboring photodiodes, e.g., antiblooming photodiodes); *see also* Ex. 2012 (indicating the threshold of the photodiodes used in the research is lower than 5V);

Maltiel Decl., ¶¶ 92-95.

Further for Badihi, the disclosed step of thinning/grinding is just for reducing the thickness of the silicon substrate for achieving a chip size packaging instead of illuminating the image sensor, which further eliminate the possibility of generating electron flow. Ex. 1101, 237. In summary, the thinning/ grinding process in the cited references is totally different from that of the '965 patent. Maltiel Decl., ¶¶ 92-95.

Thus, Badihi does not disclose, teach, or suggest the invention of claim 1 of the '319 patent. As stated above, Petitioner's expert report, which simply parrots the Petition, is insufficient to establish that the limitations not disclosed in Badihi would be obvious to a POSITA. *Xerox Corp*, IPR2022-00624 at Paper 12 at 4-5; *Unirac*, IPR2021-00532, 2021 WL 3116853 at *7; *Unified Patents Inc.*, IPR2019-00726, 2019 WL 3714386, at *11; *TQ Delta*, 942 F.3d at 1359; *Elbit Sys. of Am.*, 881 F.3d at 1359; *Free-Flow Packaging Int'l*, IPR2016-00447, Paper 7, at 10.

2. Claims 2, 5, 6

Because Badihi fails to render claim 1 obvious, it follows that claims 2, 5, and 6, which depend on claim 1, are not obvious. *See Rembrandt Wireless Techs.* 853 F.3d at 1380.

E. Ground 5: Badihi In View Of Watanabe Does Not Render Claim 4 Obvious

Claim 4 depends from claim 1. Badihi fails to render claim 1 obvious. Petitioner did not cite Watanabe against claim 1. Thus, Petitioner has not carried its

burden of establishing that Nixon in view of Merrill renders Claim 3 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

F. Ground 6: Merrill In View Of Badihi Does Not Render Claims 1, 2, 3, 5, and 6 Obvious

Merrill is a U.S. patent titled “Active pixel sensor cell that minimizes leakage current,” which does not describe BSI image sensors. Maltiel Decl., ¶¶ 106-107. Merrill discloses a CMOS APS cell including a “conventional photodiode ... typically combined with a number of active transistors”. Ex. 1049, 1:31-45, 6:13-18.

Petitioner’s expert, who parrots the arguments in the Petition, provides no evidence in support for Petitioner’s assertion that a POSITA would have been motivated to modify Merrill’s CMOS APS cells to include the semiconductor packaging taught by Badihi. Pet. at 67. But even if a POSITA were to do that, neither prior art reference, either alone or in combination, suggests the claimed invention. Maltiel Decl., ¶¶ 106-107.

Because neither Badihi nor Merrill even mentions a BSI sensor, Petitioner’s argument that a combination of those references teaches a BSI sensor does not hold water. Maltiel Decl., ¶¶ 106-107. In fact, the only way one could conceivably envision a combination of Badihi and Merrill to even remotely suggest BSI sensors is through hindsight, using the ’319 patent and its claims as a guide. Maltiel Decl., ¶¶ 106-107. This, however, is not a proper way to combine references. “Obviousness

cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.” *Univ. of Strathclyde v. Clear-Vu Lighting LLC*, 17 F.4th 155, 162 (Fed. Cir. 2021).

Further, as mentioned above, Badihi does not disclose the “protective substrate.” Thus, claim limitations [1d] and [1e] are entirely missing from the combination of references, because Petitioner does not argue that Merrill discloses those limitations. Maltiel Decl., ¶¶ 106-107. Further, Badihi does not disclose claim limitation [1f] for the reasons set forth above, and Petitioner does not argue that Merrill discloses it. Maltiel Decl., ¶¶ 106-107.

Because the combination of Merrill and Badihi does not disclose or render obvious independent claim 1, those references do not disclose or render obvious dependent claims 2, 3, 5, and 6. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

G. Ground 7: Merrill In View of Badihi and Watanabe Does Not Render Claim 4 Obvious

As is demonstrated above, the combination of Merrill and Badihi fail to render claim 1 obvious. Petitioner did not cite Watanabe against claim 1. Thus, claim 1 is patentable over Merrill in view of Badihi and Watanabe. Because claim 1 is patentable, claim 4 is also patentable. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

VIII. CONCLUSION

For these reasons, Patent Owner submits that Petitioner has failed to meet its

burden of proving that any challenged claim of the '319 patent is unpatentable.

DATE: October 11, 2023

Respectfully Submitted,

/s/ Eric Cohen

Eric Cohen

Registration No. 27,429

Counsel for Patent Owner Alidouble Inc.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24, I hereby certify that the foregoing Patent Owner Response contains 8061 words as measured by the word processing software used to prepare the document, excluding the cover page, signature block, and portions exempted under 37 C.F.R. § 42.24.

DATE: October 11, 2023

Respectfully Submitted,

/s/ Eric Cohen
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Counsel for Patent Owner Alidouble Inc.

CERTIFICATE OF SERVICE

Pursuant to 37 CFR § 42.6(e), the undersigned hereby certifies that a copy of the Patent Owner's Response Under 37 C.F.R. §42.107 by P-TACS electronic notification and electronic mail to each of the following individuals on the date indicated below:

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