

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.,

Patent Owner.

IPR2023-00372

U.S. Patent No. 6,169,319

DECLARATION OF RON MALTIEL

I, Ron Maltiel, declare the following to be true:

I. INTRODUCTION

1. I have been retained by Alidouble Inc. through its counsel, to provide my opinions regarding U.S. Patent No. 6,169,319 (the ‘319 Patent). A copy of the ‘319 Patent is Exhibit 1001.

2. I make this declaration in support of Alidouble’s Patent Owner’s Response to the Petition in IPR2023-00372.

3. This declaration contains statements of my opinions formed to date regarding the ‘319 Patent and the bases and reasons for those opinions. I may offer additional or different opinions based on further review of materials in this IPR, including review of opinions or testimony of other expert witnesses or future positions taken by Petitioner or its witnesses.

II. PROFESSIONAL EXPERIENCE AND QUALIFICATIONS

4. My educational and professional background, patents, and professional association memberships are listed in my *curriculum vitae*, which is Exhibit 2015.

5. I am a senior member of the Institute of Electrical and Electronics Engineers (IEEE) with more than 30 years’ experience in all phases of design and implementation of semiconductor manufacturing. I have worked in the development and production of new integrated circuit technologies and semiconductor devices such as CMOS devices, used for products such as Dynamic Ram (DRAM), Flash

(NAND, NOR), EEPROM, ROM, and Static RAM (SRAM) memories which are used in microprocessors, logic, digital, analog, and image sensor products.

6. I graduated in 1977 from Ben Gurion University in Israel with a Bachelor of Science degree in Materials Science & Engineering. In 1978, I earned a Master's Degree in Materials Science & Engineering from Stanford University in Palo Alto, California.

7. In 1980, I was awarded an Engineer Degree from Stanford University in Materials Science & Engineering. At Stanford University, an Engineer Degree is an additional graduate degree that can be earned after a Master's Degree. The degree differs from a Ph.D. in that an Engineer Degree's focus is primarily on professional engineering work as opposed to a Ph.D.'s primary focus on theoretical research or university teaching.¹ An Engineer Degree requires two years of additional study beyond a Master's Degree and the completion of a thesis.² My thesis related to defects in silicon and electrical measurements of their properties and was entitled *Electrical Properties Of Gold And Titanium In Silicon*. My thesis led to my first patent.³

8. Following my studies at Stanford, I worked in four semiconductor

¹ See <http://gap.stanford.edu/4-3.html>

² See *id.*

³ [Gold-doped IC resistor region - #4,432,008, https://www.maltiel.com/ron-maltiels-patents.html](https://www.maltiel.com/ron-maltiels-patents.html)

companies, focusing on the development and manufacturing of new semiconductor devices. Through the years I was responsible for integrating the work product of all the various disciplines into final manufacturing processes.

9. In 1980, my first position was at Intel. I worked to develop the first commercial non-volatile EEPROM devices. NAND memory such as Flash memory was subsequently developed using EEPROM as its basic building block. Among other responsibilities, I analyzed the manufacturing reliability and designed the production and testing of operation flow.

10. In 1982, I left Intel and joined American Micro Systems, where I was in charge of developing the manufacturing process for a new non-volatile memory product line.

11. In 1983, I joined Advanced Micro Devices (AMD) working on a project combining non-volatile with DRAM memories. I developed memory circuitry and its manufacturing process. This work led to three patents where I am named as an inventor. Following this project, I worked on several other technologies at AMD. While at AMD, I was in charge of consolidating the designs of all the test chips made by all of AMD's various divisions into one library. The test chips were used during new technology development and production to monitor the electrical properties of semiconductor products following their fabrication.

12. In 1989, I joined Maxim Integrated Products, Inc. where I was in charge of developing all the CMOS process developments for analog products and introducing them to production. When Maxim bought its first fabrication line, I developed the production process for the diffusion and etch areas.

13. I currently work as an independent consultant providing consulting services in various aspects of semiconductor technology and manufacturing.

14. In 2008, I was recognized as a Senior Member of the IEEE, the leading professional association for electrical engineers.⁴ Senior Member is the highest grade and recognizes a member with at least 10 years of industry experience including 5 years of which the member has shown “significant performance.”⁵

15. For more than 20 years, I have been managing a semiconductor industry website (www.maltiel-consulting.com) and providing to the semiconductor industry a resource full of pertinent information about new semiconductor patents as well as semiconductor products and their introduction to manufacturing. This resource addresses the informational needs of technology companies, attorneys, and investors and is used regularly by the United States Patent and Trademark Office, the Justice Department, major semiconductor companies, and universities from more than 99 countries.

⁴ See <http://www.ieee.org/about/index.html>

⁵ See <http://www.ieee.org/membership/senior/senior-requirements.html>

16. I am the named inventor of six patents. The patents are in the areas of process and circuit development. Three of my patents are related to creating new semiconductor devices and to monitoring the properties of semiconductor lines during fabrication. Two of my patents are related to measurements of wafers during fabrication. One of my patents is related to integrating resistors into doped regions in the semiconductor substrate. My patents have been referenced in other United States patents more than 150 times.

III. COMPENSATION

17. I am compensated at a rate of \$720 per hour for my work. I am also being separately reimbursed for any out-of-pocket expenses. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of any proceeding.

IV. MATERIALS CONSIDERED

18. Among the materials I considered are as follow. If there are materials I referenced but are not listed below, those should be part of the materials considered.

No.	Document
1.	U.S. Patent No. 6,168,319
2.	Prosecution File History for the '319 Patent
3.	Declaration of Dr. Konstantinos P. Giapis
4.	U.S. Patent No. 6,429,036 ("Nixon")
5.	U.S. Provisional Patent Application No. 60/116144 ("Nixon Prov.")

6.	Certified translation of JP H06-268183 (“Watanabe”)
7.	Certified translation of JP H10-116977 (“Muramatsu”)
8.	Certified translation of Sakai, H., <i>CSP Development of ShellCase Type</i> , in THE J. OF JAPAN INST. OF INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS, vol. 12, no. 3, pp. 144-147 (1997) (“Sakai”)
9.	Fossum, E., <i>Ultra-low power imaging systems using CMOS image sensor technology</i> , in ADV. MICRODEVICES AND SPACE SCIENCE SENSORS, SPIE, vol. 2267, pp. 107-111 (Sept. 23, 1994) (“Fossum I”)
10.	Barbe, F., <i>A Tradeoff Analysis for CCD Area Imagers: Frontside Illuminated Interline Transfer vs. Backside Illuminated Frame Transfer</i> , in PROCS., CCD APPLICATIONS CONF., pp. 13-20 (1973) (“Barbe”)
11.	Fossum, E., <i>Active Pixel Sensors: Are CCDs Dinosaurs?</i> , in CHARGE-COUPLED DEVICES AND SOLID STATE OPTICAL SENSORS III, SPIE, vol. 1900, pp. 2-14 (1993) (“Fossum II”)
12.	Brissot, L., et al., <i>High-definition CCDs for enhanced definition television</i> , in HIGH-RESOLUTION SENSORS AND HYBRID SYSTEMS, SPIE, vol. 1656, pp. 427-436 (Aug. 12, 1992) (“Brissot”)
13.	<i>Introduction to Quantum Efficiency</i> , TELEDYNE, available at https://www.photometrics.com/learn/imaging-topics/quantum-efficiency (“Quantum Efficiency”)
14.	U.S. Patent No. 5,244,817 (“Hawkins”)
15.	U.S. Patent No. 5,270,221 (“Garcia”)
16.	U.S. Patent No. 5,494,833 (“Martin”)
17.	U.S. Pat. No. 5,455,455 (“Badehi I”)
18.	<i>CMOS Fundamentals</i> , SILICON IMAGING, available at http://www.siliconimaging.com/cmos_fundamentals.htm#:~:text=Passive%2Dpixel%20sensors%20(PPS),the%20photosites%20and%20their%20connections (“CMOS Fundamentals”)
19.	U.S. Patent No. 8,063,963 (“Dierickx”)

20.	U.S. Patent No. 6,960,795 (“Rhodes”)
21.	“Digital camera,” <i>Encyclopedia Britannica</i> (https://www.britannica.com/technology/webcamming) (“Digital camera”)
22.	Sorrell, C., <i>Inside the Nobel Prize: How a CCD Works</i> , WIRED (Oct. 7, 2009), available at https://www.wired.com/2009/10/ccd-inventors-awarded-nobel-prize-40-years-on/ (“How a CCD Works”)
23.	<i>CCD vs. CMOS</i> , TELEDYNE DALSA, available at https://www.teledynedalsa.com/en/learn/knowledge-center/ccd-vs-cmos/ (“CCD vs. CMOS”)
24.	<i>Introduction to Charge-Coupled Devices (CCDs)</i> , NIKON, available at https://www.microscopyu.com/digital-imaging/introduction-to-charge-coupled-devices-ccds (“Intro to CCDs”)
25.	<i>What Is a CMOS Image Sensor?</i> , NANOTEC MUSEUM, available at https://www.tel.com/museum/exhibition/principle/cmos.html (“What is a CMOS Image Sensor”)
26.	Fowler, B., et al., <i>CMOS image sensors – past, present and future</i> ”, Proceedings ICIS 2006 – International Congress of Imaging Science (2006) (“Fowler”)
27.	L. J. Kozlowski, et al, <i>Comparison of passive and active pixel schemes for CMOS visible imagers</i> , Proc. SPIE 3360, Infrared Readout Electronics IV (September, 1998) (“Kozlowski”)
28.	U.S. Patent No. 9,257,479 (“Koizumi”)
29.	Fossum and Hondongwa, <i>A Review of the Pinned Photodiode for CCD and CMOS Image Sensors</i> , IEEE Journal of the Electron Devices Society (May, 2014) (“Fossum III”)
30.	<i>Back-illuminated sensor</i> , WIKIPEDIA, available at https://en.wikipedia.org/wiki/Back-illuminated_sensor
31.	Fossum, Eric R., <i>CMOS Image Sensors: Electronic Camera-On-A-Chip</i> , 44 IEEE TRANSACTIONS ON ELECTRON DEVICES, no. 10, pp. 1689-98 (Oct. 1997) (“Fossum IV”)
32.	U.S. Pat. No. 6,084,259 (“Kwon”)

33.	Fossum, Eric R., <i>Image capture circuits in CMOS</i> , IEEE INT’L SYMPOSIUM ON VLSI TECH. SYS. AND APPLICATIONS, 52-57 (June 3, 1997) (“Fossum V”)
34.	<i>Introduction to CMOS Image Sensors</i> , OLYMPUS LS, available at https://www.olympus-lifescience.com/en/microscope-resource/primer/digitalimaging/cmosimagesensors/ (“Olympus article”)
35.	U.S. Pat. No. 5,789,774 (“Merrill”)
36.	Photodiodes, LEARN ABOUT Electronics, available at https://learnabout-electronics.org/Semiconductors/diodes_27.php (“LEB article”)
37.	“PB-159: Digital Camera On A Chip,” PHOTOBIT (“PB-159 datasheet”)
38.	U.S. Pat. No. 3,676,715 (“Brojdo”)
39.	Curriculum Vitae of Dr. Konstantinos P. Giapis
40.	Declaration of Dr. Sylvia Hall-Ellis
41.	Affidavit of Nathaniel E Frank-White
42.	Badihi, A., <i>ShellCase Ultrathin Chip Size Package</i> , in PROCS. INT’L SYMPOSIUM ON ADV. PACKING MATERIALS, PROCESSES, PROPERTIES AND INTERFACES (IEEE CAT. NO. 99TH8405), IEEE, pp. 236-40 (Mar. 1999) (“Badihi”), attached as Exhibit 1101 to Declaration of Dr. Sylvia Hall-Ellis
43.	Sakai, attached as an Exhibit to Declaration of Dr. Sylvia Hall-Ellis
44.	Petition For <i>Inter Partes</i> Review of U.S. Patent No. 6,169,319
45.	Patent Owner’s Preliminary Response to Petition For <i>Inter Partes</i> Review of U.S. Patent No. 6,169,319 and associated Exhibits
46.	Institution Decision For <i>Inter Partes</i> Review of U.S. Patent No. 6,169,319
47.	Backside illuminated (BSI) complementary metal-oxidesemiconductor (CMOS) image sensors (2020)
48.	Microelectronics Packaging Handbook, 2nd edition (1997)

49.	WARPAGE AND MECHANICAL STRENGTH STUDIES OF ULTRA THIN 150MM WAFERS (1996)
50.	<i>Alidouble Inc., v. Taiwan Semiconductor Manufacturing Company Limited.</i> , Case No. 2:22-cv 00298-JRG (E.D. Tex), Docket Control Order.
51.	Die level thinning after bonding on the substrate in 3D packaging (2023)
52.	U.S. Patent No. 6,153,495
53.	U.S. Patent No. 6,239,033
54.	U.S. Patent No. 6,300,148
55.	Ultrahigh sensitivity single-photon detector using a Si avalanche photodiode for the measurement of ultraweak bioluminescence (April 1, 1995)
56.	A New MOS Imager Using Photodiode as Current Source (August 1991).
57.	MOS Area Sensor: Part n-Low-Noise MOS Area Sensor with Antiblooming Photodiodes (1980)
58.	A Dielectrically Isolated Photodiode Array by Silicon-Wafer Direct Bonding (1987)
59.	Ceramic and Glass-Ceramic Packaging in the 1990s (1991)
60.	Curriculum Vitae, Ron Maltiel

V. LEGAL PRINCIPLES

19. I am not a lawyer and I do not have formal training in patent law. I do, however, have practical experience with patents and the patenting process from my involvement in the prosecution of my U.S. patents. Any representations I make in this declaration regarding the law, however, are as I understand the law to be as

explained to me by the lawyers from Rimon, P.C. I have used my understanding of these legal principles when forming my opinions.

A. Legal Principles Of Claim Construction

20. I understand that in an IPR petition filed after November 13, 2018, terms of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent. Regarding a POSITA, I understand that a POSITA has ordinary creativity, and is not an automaton.

21. I understand that all limitations of a claim are to be interpreted with an eye to giving all limitations effect.

B. Legal Principles Of Obviousness

22. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

23. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the

modification or combination of elements claimed in the patent; and

- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

24. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

VI. LEVEL OF ORDINARY SKILL IN THE ART

25. The ‘319 Patent describes and claims an invention relating to “[a] method for producing a back-illuminated CMOS image sensor” ‘319 Patent, Abstract.

26. After reviewing the ‘319 Patent’s specification, claims and prosecution history, in my opinion, a POSITA would have at least a bachelor’s degree in electrical engineering, chemical engineering, or material science. A bachelor’s degree in one of these subjects is necessary to have a foundation in solid state physics and integrated circuit processing technology. A degree in computer science would not include sufficient chemistry and physics to enable a person to learn the integrated circuit process technology sufficiently to be a POSITA for the ‘319 Patent. In addition, a POSITA would have 3-5 years’ experience that includes some experience in image sensors. Three to five years’ experience is necessary for a POSITA to understand the variability of processing and device interactions.

VII. TECHNOLOGY OVERVIEW

A. Semiconductor Manufacturing Processes

27. In the typical fabrication of semiconductor products, transistors are first created on the surface of a silicon substrate. Then, several layers of metal wires are fabricated above the transistors to connect them, with each layer separated from the next layer by an insulating layer.

28. The fabrication of semiconductor products is a complex process that typically begins with the creation of a silicon wafer. The wafer is then subjected to a series of steps, including deposition, lithography, etching, and metallization. These steps are used to create the transistors, capacitors, resistors, and other components of the semiconductor product.

29. A semiconductor is typically a solid chemical element or compound that conducts electricity under some specific conditions. This makes it an ideal medium to control electrical current for use in electronic products. The most commonly used semiconductor material is silicon. Semiconductor devices, typically referred to as computer chips, image sensors, die or integrated circuits, are made by depositing thin layers of metals and/or dielectrics.

30. The structure of semiconductor devices requires numerous processing steps that start with a single crystal silicon wafer, called a substrate. A processed wafer has hundreds of semiconductor products called dies. Each of these dies may

have millions of transistors acting as switches. Transistors are fabricated in the substrate by modifying the structure of the substrate and by building up layers of other materials that are deposited and patterned on the substrate. The fabrication processes create active regions, which readily conduct electricity, and passive regions which are non-conducting or insulating.

31. Key wafer processing technologies include the deposition of thin films of materials and also etching patterns in those materials. Deposited dielectric films are used for isolation, passivation, barrier, masking and antireflective-coating applications in ultra-large-scale integrated (ULSI) semiconductor circuits.

32. Thin films of conductors and insulators can be formed into patterns by using the processes of photolithography in combination with etching. Photolithography is used to transfer a mask pattern etched into a photo mask onto a photosensitive film that has been applied on the silicon wafer's surface. The photosensitive film is called photoresist. During wafer exposure with visible or ultraviolet light, the photo mask with a desired opaque pattern prevents penetration of the light through the opaque pattern, while allowing radiation to pass through the mask's clear glass. The chemical structure of photoresist is such that the light changes its solubility in a developing solution. The photoresist can then be locally removed from the surface of the wafer during a subsequent developing process.

33. The process that immediately follows the photolithography process is the removal of material from areas of the wafer unprotected by photoresist. Various etching techniques are used for this purpose. Etching processes are characterized by their selectivity to a specific material and their degree of anisotropy (vertical etching). For example, the etching agent should attack silicon dioxide, but not photoresist or silicon. Upon completion of the etching, the etching mask is removed.

34. The details of the etching process depends on the etching speed and the thickness (and variation in the thickness) of the layer being etched. The etch process is typically chosen to have a fast etch rate of the layer being etched and a slow etch of the underlining layer. This ensures that we do not penetrate the underlining layer even if a portion of the layer is etched with a minimal thickness.

B. Image Sensor Technology

35. Generally, an image sensor is an electrical device which captures light and converts the light into electric signals to form an electronic representation of an image. Typically, the light receiving portions are analog circuits which, when exposed to light, create a stored charge relative to the intensity and duration of the light striking the circuit. This charge is then read out by peripheral circuitry and often converted to digital signals usable by modern computing systems to display or store the information.

36. Semiconductor imaging devices, such as described in the '319 patent, can be formed on silicon wafers. In its pure, crystalline form, silicon is a poor conductor. However, by introducing specific ions or impurities into the silicon (a process known as “doping”), silicon can be made to conduct electricity in a controlled fashion. Silicon is doped to form either an “n-type region” (a region that can donate electrons) or a “p-type region” (a region that can accept electrons, which is also referred to as donating “holes”) depending on the specific ions or impurities used, with each region having unique electrical properties. To indicate relative doping concentrations, it is common to use a “+” or “-” following the doping type. Thus, a “p-type” region would have a lower doping concentration compared to a “p+ region,” which in turn would have a lower doping concentration compared to a “p++ region.”

37. The n-type and p-type regions in a semiconductor are formed by shooting ions into the silicon substrate. A p-type region can be formed, for example, by implanting boron into the substrate and activating the boron by a heat treatment at a high temperature. An n-type region can be formed, for example, by implanting phosphorus into the substrate and activating the phosphorus by a heat treatment at a high temperature. The ion implantation energy will determine how deep the ions will be embedded in the substrate, and the dose will determine the doping

concentration. An additional heat treatment will diffuse the implanted ions deeper and, in every direction, away from the original implant location.

38. A backside-illuminated image sensor (BSI) is an image sensor where light is sensed from the back of the silicon substrate, while the circuit that monitors the sensing and digitally processes the image signal is located on the front side. Backside sensing has the advantage of being able to sense light from the entire back of the substrate, without being blocked by circuitry that covers part of the front side.

C. The Technology Of Backside Illuminated Image Sensors

39. Backside illumination has several benefits such as increasing the quantum efficiency of the sensor. As mentioned above, backside illumination can improve quantum efficiency by allowing more light to reach the sensor. This is a major advantage over front-illuminated image sensors, which can have quantum efficiencies as low as 50%.

40. Backside sensors also reduce noise in images. This is because the light that reaches the sensor is not scattered by the circuitry on the front side.

41. Backside illumination also improves the dynamic range of images. This is the range of brightness levels that an image sensor can capture. Front-illuminated image sensors often have limited dynamic range, which can lead to washed-out or dark images.

42. Solid state image sensors are used in video cameras and are in integrated circuits using a complementary metal oxide semiconductor (“CMOS”) technology. These image sensors are based on a two-dimensional array of pixels where each pixel includes a sensing element – a photo diode - that is capable of converting a portion of an optical image into an electronic signal and includes circuitry to measure the intensity of light detected by the sensing element and then to generate electronic signals are then used by other circuitry to regenerate the optical image on a display. CMOS image sensors were first developed in 1967 and utilize the photovoltaic response. The photo voltaic response occurs when silicon is exposed to light. When photons in the visible and near-IR regions of the spectrum impinge on a silicon surface and create an electron-hole pair. The number of electrons generated is proportional to the light intensity.

43. CMOS image sensors have benefited from advances in CMOS technology for microprocessors and application specific integrated circuits. Shrinking lithography, coupled with advanced signal-processing algorithms provide for sensor arrays, sensor array control, and image processing used in integrated circuit manufactured with well-established CMOS techniques.

44. Frontside illuminated image sensors (“FSI”), the frontside surface of the semiconductor substrate includes the image sensor, the CMOS circuitry, and metal lines that connect the image sensors to the CMOS circuitry and that connect

both to peripheral circuitry that controls the image sensor in general, that transmits signals to or from the image sensor, that receive, interpret, and implement control signals from off the image sensor, and that provide power and power control to all the circuits and sensors.

45. CMOS Image Sensors (CIS) may be either FSI or BSI; the difference between a BSI image sensor and an FSI image sensor is the arrangement of imaging elements in the sensor with respect to incident light to the pixel. In FSI, the photons entering the silicon from the frontside pass through the metal wiring layer before they reach the image sensors:

[i]n a frontside illuminated (FSI) sensor (see Fig. 4. 1A), the light reaches the PD active region through the passivation, metallization, and inter-dielectric layers. Several are the loss mechanisms associated with the coupling of light from the frontside of the sensor the reflection of light from the metal control lines which surround the PD [photodiode]

Ex. 2001 at 95.

46. In contrast, in a BSI image sensor, the photons reach image sensors directly from the backside without passing through the metal wiring layers on the front side:

[a] BSI sensor contains the same components as a FSI sensor but the sensor's metals are located behind the PD [photodiode]

Id. at 96.

D. The Invention Of The '319 Patent

47. The '319 patent is directed generally to methods of manufacturing BSI image sensors. The '319 patent discloses that the traditional BSI image sensors are expensive because:

(1) they are made using nonstandard complementary metal-oxide-semiconductor (CMOS) processes and

(2) packaging the BSI image sensors is complex.

Id. at 4: 13-29. To address these problems, the '319 patent discloses an innovative method for making and packaging BSI image sensors using standard wafer processing techniques and equipment. *Id.* at 8:47-50.

48. The '319 Patent discloses and claims a method for producing a back-illuminated CMOS image sensor that includes a matrix of pixels that are fabricated on a semiconductor substrate that utilizes conventional CMOS fabrication processes and that minimizes the fabrication and production costs associated with conventional CMOS fabrication processes.

49. The '319 Patent discloses the semiconductor substrate is secured to a protective substrate by an adhesive so that the frontside surface of the semiconductor substrate – the surface that is processed to fabricate the CMOS image sensor, including the matrix of pixels – so that the frontside surface faces the protective substrate. '319 Patent, 4:56-63.

50. The protective substrate provides structural support to the semiconductor substrate and exposes the backside surface of the semiconductor

substrate. The '319 Patent discloses grinding, chemical etching, or both the exposed backside of the semiconductor substrate to thin the semiconductor substrate advantageously to a range of 10 to 15 microns. '319 Patent, Abstract, 5: 4-10, 7:37-41, 9:20-27, and 12:33 - 35.

51. The '319 Patent then discloses securing a transparent substrate to the backside surface of the semiconductor substrate so that light may transmit through the transparent substrate. Thus, the '319 Patent discloses sandwiching the semiconductor substrate between the transparent substrate and the protective substrate. '319 Patent, Abstract, 5:4-9, 8:2-8, 8:45-51, 9:12-18, 10:60-63, and 10:65 – 11:2..

52. The '319 patent teaches how to fabricate backside illuminated image sensor composed of a pixel matrix array. The control circuitry (120) and the pixel array matrix (110) are initially fabricated on the front side of the wafer. The pixel matrix (110, green) is an array of photodiodes that are fabricated on the front side of the silicon wafer and extend into the wafer, as shown in Figure 3(B) below.

53. In Figure 3, the '319 Patent discloses a backside illuminated image sensor.

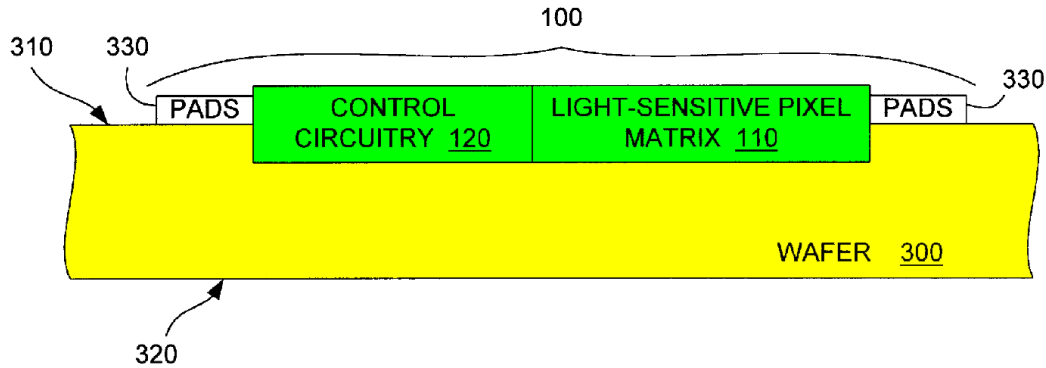


FIG. 3(B)

‘319 Patent, Fig 3(B).

54. Following the fabrication of the control circuit and the pixel matrix on the first side of the wafer (310), “A first adhesive layer 420 is deposited onto protective substrate 410, and then wafer 300 is placed onto protective substrate 410 such that first surface 310 contacts the deposited adhesive layer 420.” ‘319 patent, 6:36-40.

55. Figure 4(C) shows the back side of the wafer (320) facing up, and the front facing down. The back side of the wafer is grounded and etched to a thickness range of 10 to 15 microns (T2).

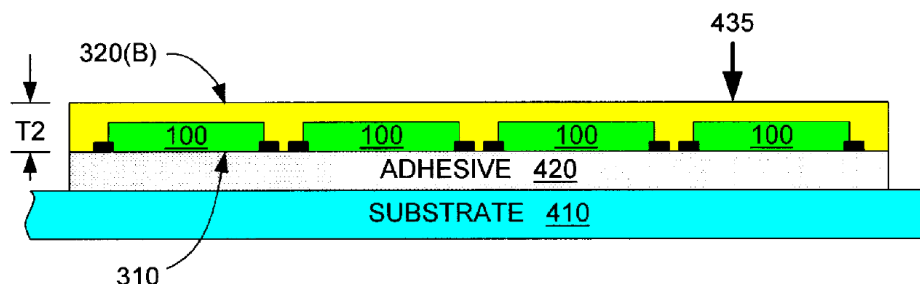


FIG. 4(C)

‘319 Patent, Fig 4(C).

56. The thickness of the remaining silicon layer T2 is a critical parameter. It must be thick enough to generate enough electrons from photons shining on the back side, but thin enough to allow those electrons to be collected by the photodiode on the front of the wafer.

57. Individual image sensor circuits (100, green) are separated by creating grooves (437) between patterned photoresist (436, purple), as shown in Fig. 4(D) below.

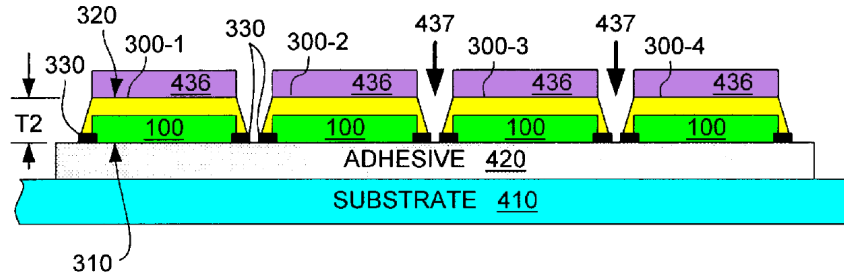


FIG. 4(D)

‘319 Patent, Fig 4(D).

58. In the next step adhesive 430 is applied the back side of the silicon wafer (300, yellow) followed by an attachment of transparent glass (440, pink) to the adhesive 430, as shown in Fig. 4(E).

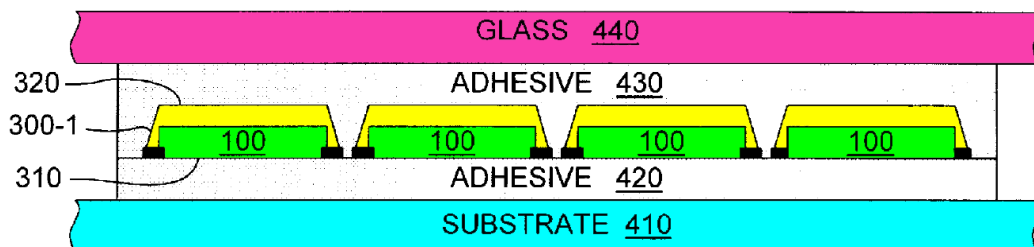
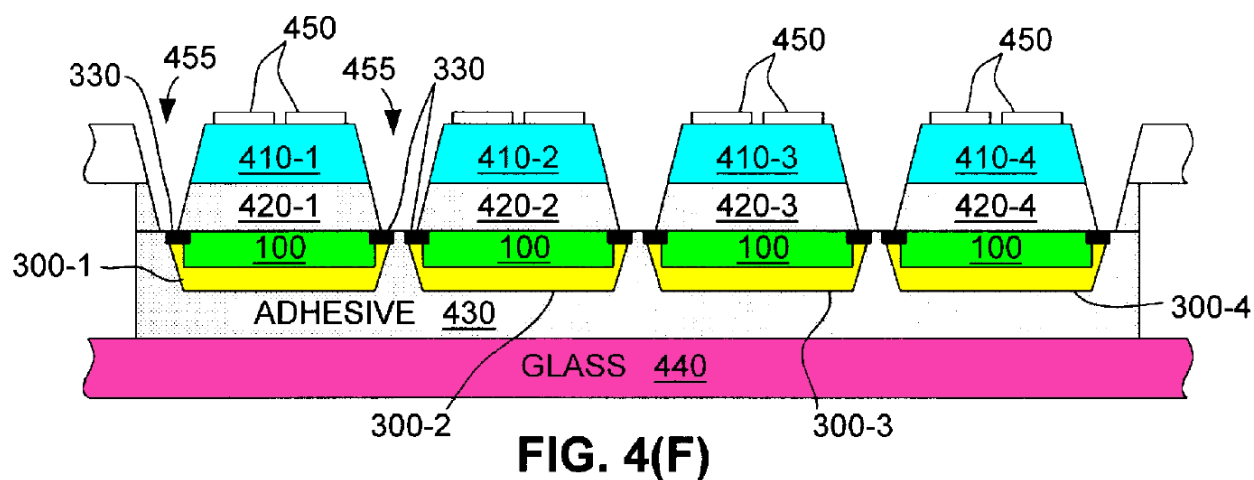


FIG. 4(E)

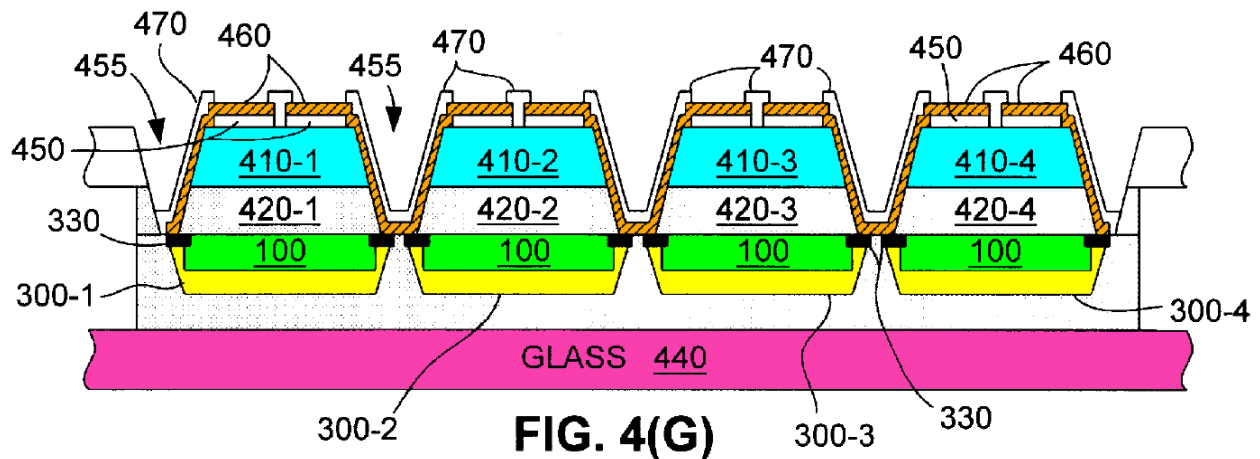
‘319 Patent, Fig 4(D). The next few figures (4(D), 4(E)) are flipped relative to Figure 4(C), with the front side of the wafer facing up and the back side facing down. The front side of the wafer is facing up because it is the side that is exposed to the next few fabrication steps.

59. To separate the dies, grooves (455) are created between them as shown in figure 4(F).



‘319 Patent, Fig 4(F).

60. In the next steps metal lines (460, orange) will be deposited to connect the pads (330, black), which are adjacent to the pixels (100, green) as shown below in figure 4(G).



‘319 Patent, Fig 4(G).

61. Slicing “waferwise sandwich” producing pluralities of backside illuminated image sensor.

62. This sequence is also in the specifications “A first adhesive layer 420 is deposited onto protective substrate 410, and then wafer 300 is placed onto protective substrate 410 such that first surface 310 contacts the deposited adhesive layer 410.” ‘319 Patent, 6:36-40

63. In the ‘319, metal leads are connected to the pads on the front side of the wafer, as described in “Referring to FIG. 4(G), after grooves 455 are formed, metal leads 460 are formed over die-sized sections 410-1 through 410-4. Each metal lead 460 extends from an associated compliant layer portion 450 to an associated metal contact pad 330.” ‘319 Patent, 8:26-31.

VIII. SUMMARY OF PETITIONER’S CITED REFERENCES

64. Petitioner cites three references, Nixon, Assadi, and Badihi as primary references.

A. Nixon

65. I understand that Nixon is a U.S. patent, Ex. 1004 (hereinafter, “Nixon”), claiming priority to the Nixon Provisional Application. Ex. 1005 (hereinafter, “Nixon Prov.”). The Nixon Provisional Application includes two documents: (1) an Invention Disclosure Technical Description (“IDTD”); and (2) an article entitled “A CSP Optoelectronic Package for Imaging and Light Detection Applications” by Shweky *et al.* (“Shweky”).

66. Nixon includes no disclosure of order of applying adhesive to a protective substrate or to a semiconductor substrate.

67. While in Nixon, metal leads are connected to pads on the back side as described in Fig. 3 steps 335 “Apply lead deposition to backside” and described in the specification:

Proceeding to state 335, a metal layer is deposited to contact each pad at its cross section as seen in FIG. 4F. The metal layer is patterned by a lithography process into individual leads 455 that contact the pads

Nixon, 2:62-67.

68. Nixon does not disclose how the metal leads are connecting to the pads on the die. In figures 4C we are shown how the dies (430, green) are separated along

435, in 4D a second glass (440, yellow) is attached. In Figure 4E opening for metal leads along 450 are created, and in Figure 4F, metal leads are deposited.

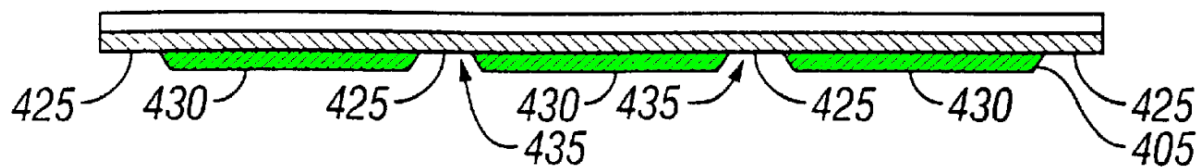


FIG. 4C

Nixon, Fig. 4C.

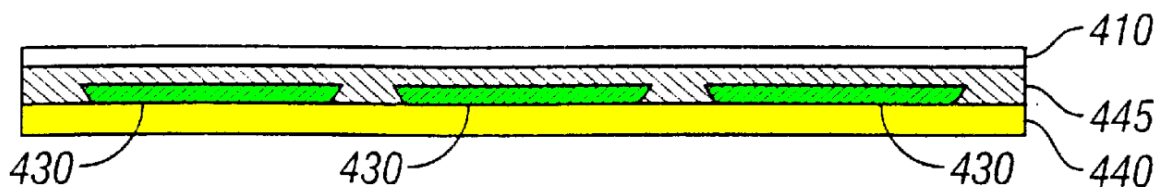


FIG. 4D

Nixon, Fig. 4D.

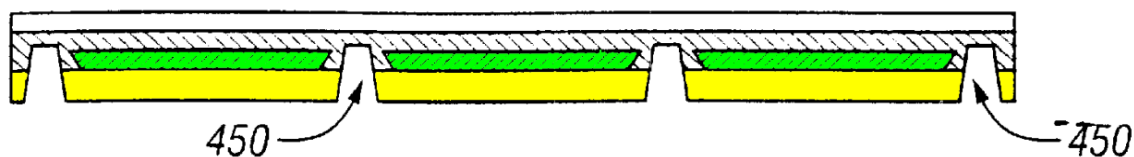


FIG. 4E

Nixon, Fig. 4E.

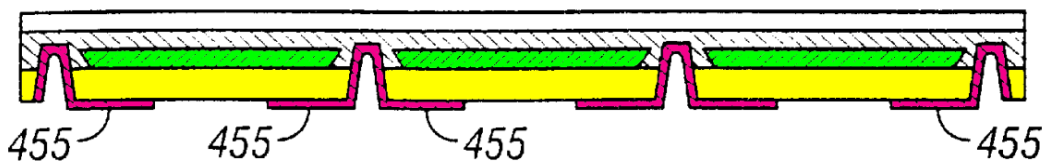


FIG. 4F

Nixon, Fig. 4F.

69. However, none of the metal leads (455, pink) are connected to any of the dies (430, green).

70. Also figure one and two below, do not show how metal leads 120 (pink) and 125 (pink) connecting pads 130 and 135 to the pixel dies 145 (green)

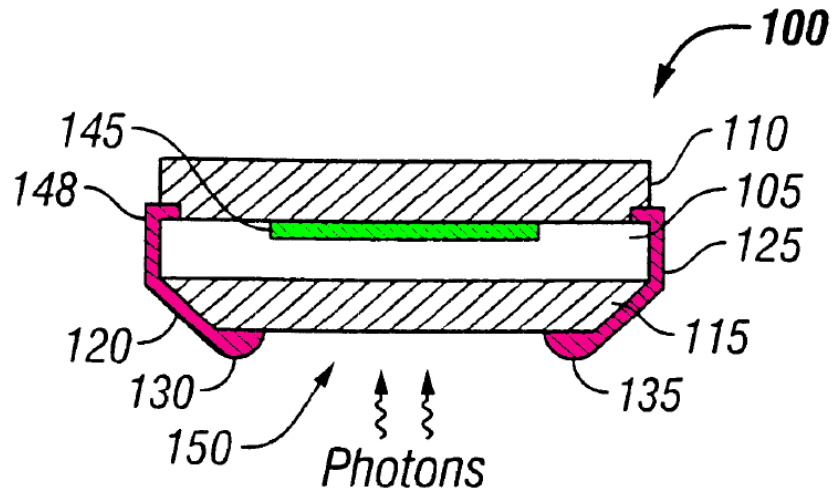


FIG. 1

Nixon, Fig. 1.

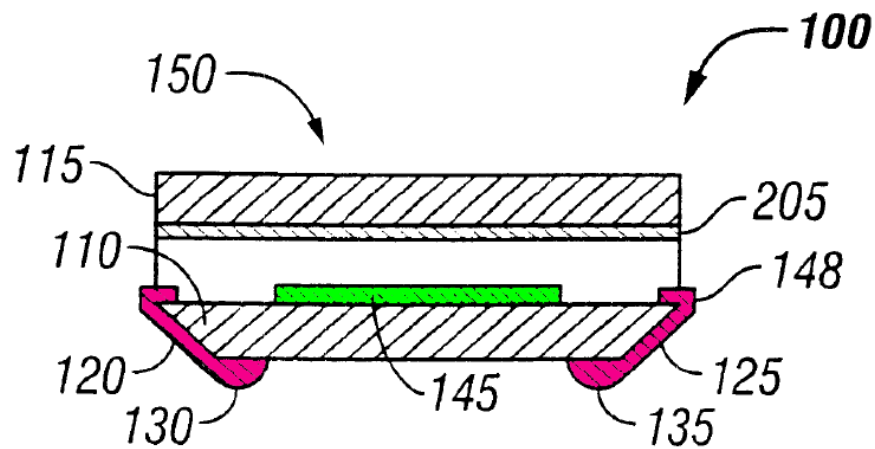


FIG. 2

Nixon, Fig. 2

B. Assadi

71. I understand that Assadi is a U.S. Patent that may disclose a passivation layer 230 that “[o]verlie[ies] the top surface of image sensor 175” and is made, for example, of silicon nitride based on its “particular resistance to environmental contaminants, particularly moisture.” Ex 1044, 4:35-45, Fig. 3b; Ex. 1003 ¶78. (hereinafter, “Assadi”). From reviewing Assadi, I understand that Assadi discloses bond pads 225 which may be on the “top surface of sensor 176” and in bond pad area 240 and that the passivation layer 230 “overlies the entirety of sensor 175, including . . . bond pad area 240.” Assadi, ¶¶ 151-53.

72. I understand that Assadi includes no disclosure of order of applying adhesive to a protective substrate or to a semiconductor substrate.

C. Badihi

73. I understand that Badihi is a printed publication published in the Proceedings International Symposium of Advanced Packaging Materials, Processes, Properties and Interfaces. Ex. 1101 (hereinafter, “Badihi”). The paper is entitled: *Shell Case Ultrathin Chip Size Package*, and is not related to backside image sensor processing. *Id.* A POSITA understand or be motivated to not apply the method disclosed in Badihi to manufacturing BSI image sensors.

D. Merrill

74. I understand Petitioner contends that Merrill teaches conventional CMOS transistors. Pet., 19 - 21

E. Watanabe

75. I understand Petitioner contends that Watanabe teaches “thinning a CMOS infared transistor.” Pet., 21.

76. Badihi includes no disclosure of order of applying adhesive to a protective substrate or to a semiconductor substrate.

IX. THE CITED REFERENCES DO NOT INVALIDATE THE CHALLENGED CLAIMS

A. Ground 1: Nixon Does Not Render Claims 1, 2, 5, Or 6 Obvious

a. Claim 1

i. “Effectively Exposed”

77. I understand that Claim 1 includes the limitation "effectively exposed":

removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface.

‘319 Patent, 11:40-42. I was informed, and a POSITA would understand, that the inventors define the "effectively exposed" limitation to require "the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through second surface.”

78. A POSITA would have known that the grinding/thinning process is not exclusively for exposing light-sensitive pixel regions to generate electron flow. *See e.g.*, Ex. 2002 at 20, 66, 71, 74 (discussing flip-chip, i.e., back-side processed chips, have general advantages in decreasing electromagnetic effects, increasing

interconnection capability, and their applications in high performing I/O packaging, all of which have nothing to do with effectively exposing CMOS photodiodes whatsoever); *see also* Ex. 2005 (in its Abstract: "[t]his paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in packaging, *i.e.*, a technology for processing silicon dies with a thickness of 100 um or less and a technology for handling thinning ultrasmall dies."); Ex. 2006. 2007, 2008 (where the grinding/thinning process is performed in general semiconductor packaging rather than image sensors); *see also* Ex. 2003 at 1 (discussing dies with back-grinding are routinely used for its advantage of better heat dissipation, which is important for high-power RF chips. Thus back-grinding process is routinely used in packaging technology that has nothing to do with effectively exposing CMOS photodiodes.) Thus, the grinding/thinning process is not just/inclusively for image sensors, *i.e.*, for exposing light-sensitive pixel regions to generate electron flow.

79. A POSITA would understand that electron flow would not necessarily be generated when the light-sensitive pixel regions of each image sensor circuit are illuminated because, for example, there may be an illumination threshold that has to be reached before electron flow is generated. *See e.g.*, Ex. 2009 (discussing how the threshold of silicon photodiodes should be designed to reduce noise interference and yet preserve high sensitivity); *see also* Ex. 2010 (discussing how to improve

threshold uniformity among photodiodes in an array to increase the quality of imaging); *see also* Ex. 2011 (discussing how to tune thresholds of photodiodes to reduce current contamination to neighboring photodiodes, *e.g.*, antiblooming photodiodes); *see also* Ex. 2012 (indicating the threshold of the photodiodes used in the research is lower than 5V).

ii. “photodiode diffusion region”

80. I understand that Claim 1 recites:

a photodiode diffusion region extending into the semiconductor substrate from the first surface

‘319 Patent, 11:27-28. Describing Fig. 1, I understand Nixon to state that “[p]ixels 145 are positioned at the top surface 148 of the silicon substrate 105.” Ex. 1004, 2:8-9. With respect to Fig. 2, Nixon states further that “[f]ig. 2 illustrates the image sensor 100 of Fig. 1 modified to include a color filter array (CFA) 205.” *Id.*, 2:15-16.

81. A POSITA would understand that Nixon does not describe the photodiode diffusion region as “extending into the semiconductor substrate.” Rather, a POSITA would understand Nixon to describe the photodiode diffusion region as sitting on top of it.

iii. “protective substrate”

82. I understand that Claim 1 recites:

a protective substrate secured to the semiconductor substrate such that

the metal line is located between the protective substrate and the semiconductor substrate

‘319 Patent, 11:20-41.

83. I understand that the Abstract of the ‘319 patent discloses that “the protective substrate provid[es] **structural support**....” ‘319 Patent, at Abstract (emphasis added). I understand that the specification further explains that “because the method utilizes **a protective substrate to support the semiconductor substrate**, the thinning process is less expensive to perform.” *See id.*, 4:48-50 (emphasis added).

84. A POSITA would understand that the protective substrate in the ‘319 patent is configured to provide structural support to the BSI image sensor. *See. e.g.*, Ex. 2001 at 2 (disclosing that the main technological challenge associated with producing BSI is the bonding of the original wafer containing photodiodes to a protective substrate to provide structural support while the original wafer is being grinded down to a thickness of a few microns); *see also* Ex. 2002 at 476 (discussing the challenges that backside grinding increases chip failures because of die cracks by stating “[h]owever, die cracks still originate from flaws on the back side due to backgrinding operations used to manufacture thin packages.”); *see also* Ex. 2003 at 1 (discussing backside grinding induces damage in the wafer that leads to crack propagation by stating “[g]rind processes will induce damage in the wafer backsurface that can lead to crack propagation, growth, and fracture.

85. A POSITA would understand that Nixon does not disclose a “protective substrate.” In Nixon, the supposed “protective substrate” asserted by Petitioner is a thin layer of glass permitting light to go through. *See* Pet. at 29. A POSITA would not understand that the identified thin layer of glass in Nixon provides any structural support to the semiconductor substrate

b. Claim 2

86. Claim 2 depends from Claim 1. I understand that Nixon does not render Claim 2 obvious because Nixon does not render Claim 1 obvious.

c. Claim 5

87. Claim 5 depends from Claim 1. I understand that Nixon does not render Claim 5 obvious because Nixon does not render Claim 1 obvious.

d. Claim 6

88. Claim 6 depends from Claim 1. I understand that Nixon does not render Claim 6 obvious because Nixon does not render Claim 1 obvious.

B. Ground 2: Claim 3 Is Not Obvious Over Nixon In View Of Merrill

89. I understand that Claim 3 depends from Claim 1 and that because Claim 1 is not obvious, Claim 3 is also not obvious.

C. Ground 3 Because Claim 4 Is Not Obvious Over Nixon In View Of Watanabe

90. I understand Claim 1 depends from claim 1 and that because Claim 1 is not obvious, Claim 4 is also not obvious.

D. Ground 4 Because Claims 1, 2, 5, or 6 Are Not Obvious Over Badihi

a. Claim 1

i. “effectively exposed”

91. I understand that Claim 1 recites:

wherein the semiconductor substrate has a thickness defined such that the light-sensitive pixel region is effectively exposed through the second surface.”

’319 Patent, 11:39-42. I was informed, and a POSITA would understand, that the inventors define the “effectively exposed” limitation in the ’319 patent to require “the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through second surface.

92. Badihi is directed to general back-side grinding and packaging of wafer. Section VII.C. Back-side grinding was routinely done in the semiconductor packaging industry for advantages that have nothing to do with image sensing. *See e.g.*, Ex. 2002 at 20, 66, 71, 74 (discussing flip-chip, i.e., back-side processed chips, have general advantages in decreasing electromagnetic effects, increasing interconnection capability, and their applications in high performing I/O packaging, all of which have nothing to do with effectively exposing CMOS photodiodes whatsoever); *see also* Ex. 2005 (in its Abstract: “[t]his paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in

packaging, *i.e.*, a technology for processing silicon dies with a thickness of 100 um or less and a technology for handling thinning ultrasmall dies.”); *see also* Ex. 2006. 2007, 2008 (where the grinding/thinning process is performed in general semiconductor packaging rather than image sensors); *see also* Ex. 2003 at 1 (discussing dies with back-grinding are routinely used for its advantage of better heat dissipation, which is important for high-power RF chips. Thus, back-grinding process is routinely used in packaging technology that has nothing to do with effectively exposing CMOS photodiodes). Second, Badihi mentioned nothing whatsoever about CMOS photodiodes and/or BSI sensors.

93. No POSITA reading Badihi would understand the general back-side grinding disclosed in Badihi is to “effectively expose” the BSI image sensors such that electron flow is generated with the light sensitive pixel regions (*i.e.*, the image sensor) being exposed to light (photons).

94. A POSITA would understand that electron flow would not be necessarily generated when the light-sensitive pixel regions of each image sensor circuit are illuminated because, for example, there may be an illumination threshold that has to be reached before electron flow is generated. *See e.g.*, Ex. 2009 (discussing how the threshold of silicon photodiodes should be designed to reduce noise interference and yet preserve high sensitivity); *see also* Ex. 2010 (discussing how to improve threshold uniformity among photodiodes in an array to increase the

quality of imaging); *see also* Ex. 2011 (discussing how to tune thresholds of photodiodes to reduce current contamination to neighboring photodiodes, e.g., antiblooming photodiodes); *see also* Ex. 2012 (indicating the threshold of the photodiodes used in the research is lower than 5V).

95. Further for Badihi, the disclosed step of thinning/grinding is for reducing the thickness of the silicon substrate for achieving a chip size packaging instead of illuminating the image sensor, which further eliminate the possibility of generating electron flow. Ex. 1101, 237.

ii. “backside illuminated image sensor”

96. Badihi is directed to general back-side grinding and packaging of wafer that may not have any implication to BSI image sensors. *See e.g.*, Ex. 2002 at 20, 66, 71, 74 (discussing flip-chip, i.e., back-side processed chips, have general advantages in decreasing electromagnetic effects, increasing interconnection capability, and their applications in high performing I/O packaging, all of which have nothing to do with BSI image sensors)); *see also* Ex. 2005 (in its Abstract: “[t]his paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in packaging, *i.e.*, a technology for processing silicon dies with a thickness of 100 um or less and a technology for handling thinning ultrasmall dies.”); *see also* Ex. 2006, 2007, 2008 (where the grinding/thinning process is performed in

general semiconductor packaging rather than image sensors); *see also* Ex. 2003 at 1 (discussing dies with back-grinding are routinely used for its advantage of better heat dissipation, which is important for high-power RF chips. Thus back-grinding process is routinely used in packaging technology that has nothing to do with BSI image sensors).

97. Petitioner asserts that POSITA would understand “Badihi could be used for BSI CMOS image sensors,” citing Petitioner’s parroting conclusory statement as support. Pet. at 70. Badihi does not disclose or suggest that its packaging process could be applied to BSI image sensors. A POSITA would not be motivated to apply the packaging method disclosed in Badihi for BSI image sensors given the different nature between packaging process versus BSI image sensor manufacturing process.

iii. “protective substrate”

98. I understand that Claim 1 recites “a protective substrate secured to the semiconductor substrate such that the metal line is located between the protective substrate and the semiconductor substrate.” ‘319 Patent, 11:20-41.

99. The abstract of the ‘319 patent discloses that “the protective substrate provid[es] **structural support**....” ‘319 Patent, Abstract (emphasis added). The specification further explains that “because the method utilizes **a protective substrate to support the semiconductor substrate**, the thinning process is less expensive to perform.” *Id.* at 4:48-50 (emphasis added). The ‘319 Patent’s

disclosure is consistent with the plain and ordinary meaning as understood by a POSITA that the protective substrate in the '319 patent is configured to provide structural support to the BSI image sensor.

100. A POSITA would not understand Badihi to disclose a “protective substrate.” In Badihi, the supposed “protective substrate” asserted by Petitioner is just a thin layer of glass permitting light to go through. *See* Pet. at 58, 75. A POSITA would not understand from Badihi that the alleged “protective substrate” provides any structural support.

b. Claim 2

101. I understand that Claim 2 depends from Claim 1. Badihi fails to render Claim 1 obvious. I understand that because Claim 1 is not obvious, Claim 2 is also not obvious..

c. Claim 5

102. I understand that Claim 5 depends from Claim 1. Badihi fails to render Claim 1 obvious. I understand that because Claim 1 is not obvious, claim 5 is also not obvious.

d. Claim 6

103. I understand that Claim 6 depends from Claim 1. I understand that because Claim 1 is not obvious, Claim 6 is also not obvious.

E. Ground 5: Badihi In View Of Watanabe Does Not Render Claim 4 Obvious

104. Petitioner has failed to carry its burden of establishing that Badihi in view of Watanabe renders Claim 4 obvious.

105. I understand that Claim 4 depends from Claim 1 and that because Claim 1 is not obvious, Claim 4 is also not obvious.

F. Ground 6 Merrill In View Of Badihi Does Not Render Claims 1, 2, 3, 5, Or 6 Obvious

a. Claim 1

106. A POSITA would understand that Merrill is a U.S. patent titled “Active pixel sensor cell that minimizes leakage current,” which does not describe BSI image sensors. A POSITA would understand that Merrill discloses a CMOS APS cell including a “conventional photodiode ... typically combined with a number of active transistors.” Merrill, 1:31-45, 6:13-18.

107. A POSITA would not have been motivated to modify Merrill’s CMOS APS cells to include the semiconductor packaging taught by Badihi. Because neither Badihi nor Merrill mentions a BSI sensor.

b. Claim 2

108. I understand that Claim 2 depends from Claim 1. I understand that because Claim 1 is not obvious, Claim 2 is also not obvious.

c. **Claim 3**

109. I understand that Claim 3 depends from Claim 1 and that because Claim 1 is not obvious, Claim 2 is also not obvious.

d. **Claim 5**

110. I understand that Claim 5 depends from Claim 1 and that because Claim 1 is not obvious, Claim 2 is also not obvious.

e. **Claim 6**

111. I understand that Claim 6 depends from Claim 1 and that because Claim 1 is not obvious, Claim 2 is also not obvious.

G. Ground 7: Merrill In View of Badihi and Watanabe Does Not Render Claim 4 Obvious

112. I understand that Claim 4 depends from Claim 1 and that because claim 1 is not obvious, claim 4 is also not obvious.

113. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of the '319 patent.

Dated: Oct 11, 2023



RONMALTIEL