

(19) Japan Patent Office (JP)

(12) Japanese Unexamined Patent
Application Publication (A)

(11) Japanese Unexamined Patent
Application Publication Number

H11-284067

(43) Publication date **October 15, 1999**

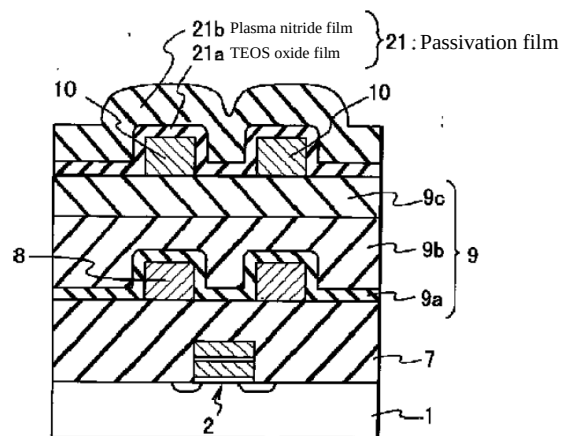
(51) Int. Cl. ⁶	Identification codes	FI			
H01L 21/768		H01L	21/90	M	
21/316			21/316	M	
21/318			21/318	M	
27/115			27/10	434	
21/8247			29/78	371	
Request for examination Not yet requested Number of claims 14 OL (Total of 13 pages) Continued on last page					
(21) Application number	Japanese Patent Application H10-81066	(71) Applicant	000003078 Toshiba Corporation No. 72 Horikawa-cho, Saiwai-ku, Kawasaki- shi, Kanagawa-ken		
(22) Date of application	March 27, 1998	(72) Inventor	YOICHI OSHIMA % Toshiba Yokohama Works, 8 Shinsugita-ku, Isogo-ku, Yokohama-shi, Kanagawa-ken ADDRESS		
		(72) Inventor	SEIICHI MORI % Toshiba Yokohama Works, 8 Shinsugita-ku, Isogo-ku, Yokohama-shi, Kanagawa-ken		
		(74) Agent	Patent attorney HIDEAKI TOGAWA		

(54) (TITLE OF THE INVENTION) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD FOR THE SAME

(57) (ABSTRACT)

(PROBLEM) Improve the reliability of a semiconductor device by ameliorating the interlayer insulation film structure so as to prevent diffusion of hydrogen into circuit elements such as non-volatile memory cells, etc. from the passivation film.

(MEANS FOR SOLVING) A non-volatile memory cell 2 is formed on a silicon substrate, and is covered by a first interlayer insulation film 7 made of BPSG or the like. After a layer 1 metal trace 8 has been formed on the first interlayer insulation film 7, a second interlayer insulation film 9 having a three-layer structure is formed. Plasma oxide film 9a is deposited in such a way that the surface thereof reflects the contours of the trace; TEOS oxide film 9b is deposited thereupon and levelled; and plasma oxide film 9c is further deposited thereupon. A layer 2 metal trace 10 is then formed on the second interlayer insulation film 9, after which a passivation film 21 comprising TEOS oxide film 21a and plasma nitride film 21b is formed thereupon.



(SCOPE OF PATENT CLAIMS)

(CLAIM 1) Semiconductor device comprising a semiconductor substrate, circuit elements integrated on this semiconductor substrate, a multilayered trace formed on these circuit elements across interlayer insulation film, and passivation film that includes silicon nitride film deposited by plasma CVD in such a way as to cover the topmost layer of this multilayered trace, characterized in that:

Interlayer insulation film serving as the base for at least one of trace layer number n of the aforesaid multilayered trace has a stacked structure comprising:

Levelled insulation film deposited in such a way as to achieve an essentially level surface so as to eliminate the step of trace layer number (n-1); and

Compact insulation film deposited on this levelled insulation film that is more compact than the levelled insulation film.

(CLAIM 2) Semiconductor device set forth in claim 1, characterized in that the aforesaid levelled insulation film is silicon oxide film deposited by CVD or spin-on glass with organic oxysilane as the primary source gas, and the aforesaid compact insulation film is silicon oxide film deposited by plasma CVD with silane as the primary source gas.

(CLAIM 3) Semiconductor device set forth in claim 1 or 2, characterized in that the aforesaid compact insulation film has a film thickness of 200-600 nm.

(CLAIM 4) Semiconductor device set forth in claim 1 or 2, characterized in that the aforesaid levelled insulation film has a film thickness of 200-500 nm.

(CLAIM 5) Semiconductor device comprising a semiconductor substrate, circuit elements integrated on this semiconductor substrate, a multilayered trace formed on these circuit elements across interlayer insulation film, and passivation film that includes silicon nitride film deposited by plasma CVD in such a way as to cover the topmost layer of this multilayered trace, characterized in that:

Interlayer insulation film serving as the base for at least one of trace layer number n of the aforesaid multilayered trace has a stacked structure comprising:

First insulation film deposited so as to have a surface step mirroring the step of trace layer number (n-1);

Second insulation film deposited level on this first insulation film in such a way as to have an essentially level surface that eliminates the surface step thereof; and

A third insulation film deposited on this second insulation film that is more compact than the second insulation film.

(CLAIM 6) Semiconductor device set forth in claim 5, characterized in that the aforesaid first and third insulation film is silicon oxide film deposited by plasma CVD with silane as the primary source gas, and

The aforesaid second insulation film is silicon oxide film deposited by plasma CVD or spin-on glass with organic oxysilane as the primary source gas, and then levelled.

(CLAIM 7) Semiconductor device set forth in claim 6, characterized in that the aforesaid second insulation film is

silicon oxide film with a film thickness of 200-500 nm.

(CLAIM 8) Semiconductor device set forth in claim 6, characterized in that the aforesaid third insulation film is silicon oxide film with a film thickness of 200-600 nm.

(CLAIM 9) Semiconductor device set forth in any one of claims 1 through 8, characterized in that the aforesaid circuit elements include non-volatile memory cells with a charge accumulation layer.

(CLAIM 10) Manufacturing method for semiconductor device having a process in which circuit elements are integrated on a semiconductor substrate; a process in which a multilayered trace is formed on the aforesaid circuit elements across interlayer insulation film; and a process in which silicon nitride film is formed by plasma CVD as a passivation layer covering the topmost layer of the aforesaid multilayered trace, characterized in that:

A process for forming interlayer insulation film serving as the base for at least one of trace layer number n of the aforesaid multilayered trace includes:

A process in which a first silicon oxide film is deposited by plasma CVD with silane as the primary source;

A process in which a second silicon oxide film is deposited on the aforesaid first silicon oxide film by CVD or spin-on glass with organic oxysilane as the primary source; and

A process in which a third silicon oxide film is deposited on the aforesaid second silicon oxide film by plasma CVD with silane as the primary source.

(CLAIM 11) Manufacturing method for semiconductor device having a process in which circuit elements, including non-volatile memory cells with a charge accumulation layer, are integrated on a semiconductor substrate; a process in which multilayered trace is formed on the aforesaid circuit elements across interlayer insulation film; and a process in which passivation film containing silicon nitride film is deposited by plasma CVD covering the topmost layer of the aforesaid multilayered trace, characterized in that:

A process for forming interlayer insulation film serving as the base for at least one of trace layer number n of the aforesaid multilayered trace includes:

A process in which a first silicon oxide film having a surface step that reflects the step of trace number (n-1) is deposited;

A process in which a second silicon oxide film is deposited on the aforesaid first silicon oxide film by CVD or spin-on glass with organic oxysilane as the primary source;

A process in which the surface of the aforesaid second silicon oxide film is levelled; and

A process in which a third silicon oxide film is deposited on the aforesaid second silicon oxide film by plasma CVD with silane as the primary source.

(CLAIM 12) Manufacturing method for semiconductor device set forth in claim 11, characterized in that heat treatment is performed at 300-450 °C after levelling the surface of the aforesaid second silicon oxide film.

(CLAIM 13) Manufacturing method for semiconductor device set forth in claim 10 or 11, characterized in that the aforesaid second and third silicon oxide film is formed more thickly than the aforesaid first silicon oxide film.

(CLAIM 14) Manufacturing method for semiconductor device set forth in claim 10 or 11, characterized in that the aforesaid third silicon oxide film is deposited to a thickness of 200-600 nm.

(DETAILED DESCRIPTION OF THE INVENTION)

(0001)

(TECHNICAL FIELD OF THE INVENTION) This invention relates to a semiconductor device having a multilayered trace structure that could prove of value when applied to non-volatile semiconductor memory in particular, and to a manufacturing method for the same.

(0002)

(PRIOR ART) In non-volatile semiconductor memory devices used to non-volatilely store data by accumulating an electrical charge in a floating gate, one known method of preventing deterioration of the ability of a memory cell to retain charge was to adopt a two-layer film structure in which silicon nitride film was deposited by plasma CVD on the topmost layer thereof as passivation film (hereinafter referred to as plasma nitride film), and silicon oxide film was deposited as the base thereof by plasma CVD using silane (SiH₄) gas (hereinafter referred to as plasma oxide film). The objective for doing this was to block diffusion of hydrogen with the oxide film so as to prevent the diffusion of hydrogen from the nitride film from impacting the write/erase properties of the non-volatile memory cell.

(0003) In contrast, in semiconductor devices with a multilayered trace structure, advances in miniaturization have led to the use of silicon oxide film deposited by CVD using organic oxysilane gas as the source gas, of which TEOS (tetraethyloxysilane: Si(OC₂H₅)₄) gas is exemplary, as the interlayer insulation film for the trace layers thereof (hereinafter referred to as TEOS oxide film). However, because TEOS oxide film tends to absorb moisture, if it is used in non-volatile semiconductor memory, moisture from the TEOS oxide film is known to adversely impact the charge retention ability of memory cells. For this reason, one approach with non-volatile semiconductor memory devices is to deposit on the order of 100-200 nm of plasma oxide film under the TEOS oxide film.

(0004) FIG. 26 shows a prior-art example thereof. A plurality of memory cells 102 are formed on a silicon substrate 101. A typical configuration for the memory cells 102 is stacked gate, in which the floating gate and the control gate are stacked across gate insulation film. A first metal trace 104 is formed on an interlayer insulation film 103 formed over the memory cell 102. A plasma oxide film 105a is formed to on the order of 100-200 nm on the layer 1 trace 104, and TEOS oxide film 105b is further deposited thereupon. A layer 2 metal trace 106 is then formed on this two-layer interlayer insulation film 105. A film stack of plasma oxide film 107a and plasma nitride film 107b is then formed as a passivation film 107 on this layer 2 trace 106.

(0005)

(PROBLEM TO BE SOLVED BY THE INVENTION) One conceivable method of ensuring the reliability of memory cells is an interlayer insulation film structure of the kind shown in FIG. 26. However, with advances in element and trace miniaturization, it has become challenging for such structures to prove efficacious. In short, in order to prevent diffusion of hydrogen from the plasma nitride film 107b, it is desirable for the plasma oxide film 107a to have a thickness

beyond a certain level. However, due to advances in trace miniaturization and narrowing of the pitch of the layer 2 trace 106, the plasma oxide film 107, which has poor step coverage, becomes thin near the side of the trace 106, as shown in FIG. 27, which hinders the intended effect of preventing hydrogen diffusion. It has become evident that, when used in an actual non-volatile memory cell, performance is impaired by trace amounts of hydrogen and moisture, which might otherwise not be an issue in a standard MOS transistor.

(0006) Similarly, the trend toward reduced pitch between traces of the layer 1 metal trace 104 facilitates the occurrence of voids between traces, for which reason fluorine is sometimes added into the insulation film to improve step coverage. In such cases, in the event that a multilayered trace comprising three or more layers of metal trace is formed to achieve greater integration of elements, the risk is that a single thin plasma oxide film 105a may no longer be adequate to fully prevent diffusion of fluorine or moisture contained in the interlayer insulation film of the multilayered trace into the memory cells.

(0007) This invention was devised in view of these circumstances, having as its objective to provide a semiconductor device that seeks to improve reliability by ameliorating the interlayer insulation film structure of a multilayered trace so as to prevent the diffusion of moisture, fluorine, etc. from the upper layer passivation film or the interlayer insulation film into circuit elements such as non-volatile memory cells, and to a manufacturing method for the same.

(0008)

(MEANS FOR SOLVING THE PROBLEM) This invention is a semiconductor device comprising a semiconductor substrate, circuit elements integrated on this semiconductor substrate, a multilayered trace formed on these circuit elements across interlayer insulation film, and passivation film that includes silicon nitride film deposited by plasma CVD in such a way as to cover the topmost layer of this multilayered trace, characterized in that: interlayer insulation film serving as the base for at least one of trace layer number n of the aforesaid multilayered trace has a stacked structure comprising: levelled insulation film deposited in such a way as to achieve an essentially level surface so as to eliminate the step of trace layer number (n-1); and compact insulation film deposited on this levelled insulation film that is more compact than the levelled insulation film.

(0009) For example, in concrete terms, silicon oxide film deposited by CVD or spin-on glass with organic oxysilane as the primary source gas can be used as levelled insulation film, and silicon oxide film deposited by plasma CVD with silane as the primary source gas can be used as compact insulation film. Preferably, the compact insulation film has a film thickness of 200-600 nm, and the levelled insulation film has a film thickness of 200-500 nm.

(0010) This invention is also a semiconductor device comprising a semiconductor substrate, circuit elements integrated on this semiconductor substrate, a multilayered trace formed on these circuit elements across interlayer insulation film, and passivation film that includes silicon nitride film deposited by plasma CVD in such a way as to cover the topmost layer of this multilayered trace, characterized in that: interlayer insulation film serving as the

base for at least one of trace layer number n of the aforesaid multilayered trace has a stacked structure comprising: first insulation film deposited so as to have a surface step mirroring the step of trace layer number (n-1); second insulation film deposited level on this first insulation film in such a way as to have an essentially level surface that eliminates the surface step thereof; and third insulation film deposited on this second insulation film that is more compact than the second insulation film.

(0011) The first and third insulation film is, for example, silicon oxide film deposited by plasma CVD with silane as the primary source, and the second insulation film is silicon oxide film deposited by plasma CVD or spin-on glass with organic oxysilane as the primary source, and then levelled. The third insulation film is preferably silicon oxide film with a film thickness of 200-600 nm, and the second insulation film is preferably silicon oxide film with a film thickness of 200-500 nm.

(0012) In this invention, it is preferable that the aforesaid circuit elements include non-volatile memory cells with a charge accumulation layer. This invention is also a manufacturing method for semiconductor device having a process in which circuit elements are integrated on a semiconductor substrate; a process in which multilayered trace is formed on the aforesaid circuit elements across interlayer insulation film; and a process in which silicon nitride film is formed by plasma CVD as a passivation layer covering the topmost layer of the aforesaid multilayered trace, characterized in that: a process for forming interlayer insulation film serving as the base for at least one of trace layer number n of the aforesaid multilayered trace includes: a process in which a first silicon oxide film is deposited by plasma CVD with silane as the primary source; a process in which a second silicon oxide film is deposited on the aforesaid first silicon oxide film by CVD or spin-on glass with organic oxysilane as the primary source; and a process in which a third silicon oxide film is deposited on the aforesaid second silicon oxide film by plasma CVD with silane as the primary source.

(0013) Furthermore, this invention is a manufacturing method for semiconductor device having a process in which circuit elements, including non-volatile memory cells with a charge accumulation layer, are integrated on a semiconductor substrate; a process in which multilayered trace is formed on the aforesaid circuit elements across interlayer insulation film; and a process in which passivation film containing silicon nitride film is deposited by plasma CVD covering the topmost layer of the aforesaid multilayered trace, characterized in that: a process for forming interlayer insulation film serving as the base for at least one of trace layer number n of the aforesaid multilayered trace includes: a process in which a first silicon oxide film having a surface step that reflects the step of trace number (n-1) is deposited; a process in which a second silicon oxide film is deposited on the aforesaid first silicon oxide film by CVD or spin-on glass with organic oxysilane as the primary source; a process in which the surface of the aforesaid second silicon oxide film is levelled; and a process in which a third silicon oxide film is deposited on the aforesaid second silicon oxide film by plasma CVD with silane as the primary source.

(0014) In the method of this invention, it is preferred that heat treatment is performed at 300-450 °C after levelling the surface of the aforesaid second silicon oxide film. According to this invention, the interlayer insulation film serving as the base for an arbitrary trace layer number n among the multilayered trace is given at minimum a two-layer structure comprising levelled insulation film such as TEOS oxide film or the like to eliminate the step in the trace layer number (n-1) and compact insulation film comprising compact plasma oxide film or the like that is more compact than the TEOS oxide film deposited thereupon.

(0015) By adopting an interlayer insulation film structure of this kind, it becomes possible to deposit the compact insulation film on the levelled insulation film to the thickness of 200 nm or greater that is required in order to reduce hydrogen diffusion to a level that will not impact circuit elements such as non-volatile conductor memory cells and the like, and does so without introducing defects even if plasma oxide film with poor step coverage is used. Consequently, it is possible to reliably suppress hydrogen diffusion from the plasma oxide film into circuit elements even if plasma oxide film is used for the passivation film.

(0016) In this invention, the effect of preventing hydrogen diffusion increases with increase in compact insulation film thickness. However, increasing thickness to an unnecessary extent can make it challenging to machine contact holes and embed via plugs, and hence for practical purposes the thickness should desirably be limited to no greater than 600 nm. In contrast, the levelling insulation film should desirably be given a thickness of 200 nm or greater in order to ensure that the step in the basal trace layer is adequately eliminated so as to obtain a materially level surface. However, to ensure that contact holes can be machined and via plugs can be embedded, an upper limit on the thickness thereof is generally on the order of 500 nm.

(0017) In this invention, it is even more preferred that the aforesaid interlayer insulation film has a 3-layer structure comprising compact insulation film such as plasma oxide film or the like whose surface reflects the step in the trace layer number (n-1) (first insulation film); a levelled insulation film such as TEOS oxide film or the like whose surface has been levelled (second insulation film); and a compact insulation film such as plasma oxide film or the like further deposited levelly thereupon (third insulation film).

(0018) According to a 3-layer interlayer insulation film structure of this kind, because numerous compact insulation films are formed in the interlayer insulation film, it is possible to simultaneously prevent diffusion of hydrogen from the passivation film into the circuit elements, as described above, as well as to adequately prevent diffusion of moisture and the like contained in the levelled film such as TEOS film or the like into circuit elements.

(0019) This invention is particularly effective in improving reliability in cases when it is applied to semiconductor devices with non-volatile memory cell arrays, which are greatly affected by diffusion of hydrogen, moisture, fluorine, etc. from the passivation film or interlayer insulation film.

(0020)

(EMBODIMENTS OF THE INVENTION) Embodiment examples of this invention will be described below with reference to the drawings. FIG. 1 through FIG. 6 show the manufacturing process for embodiment example no. 1, in which this

invention is applied to a stacked gate-type non-volatile semiconductor memory with a 2-layer metal trace.

(0021) As shown in FIG. 1, a standard stacked gate non-volatile memory cell 2 is formed on a silicon substrate 1 by the known method. The non-volatile memory cell 2 is created by stacking a floating gate 3 and a control gate 4 across gate insulation film, and forming source and drain diffusion layers 5, 6. The memory cell 2 typically has an array structure, and several different such array structures are known. However, for convenience, only one cell is shown, as the anticipated effect of this invention does not depend on the array structure.

(0022) A first interlayer insulation film 7 in the form of, for example, BPSG film, is deposited over the entire surface above the non-volatile memory cell 2, and then levelled. A contact hole is then formed in this first interlayer insulation film 7 to provide an electrode (not shown in the drawings), after which 400 nm of trace material film such as Al or the like is deposited, and a layer 1 trace 8 is formed by patterning. Concretely, the structure used for the Al trace material film is one in which Al-Cu film is deposited across a barrier metal film of Ti/TiN, and then TiN film is further deposited thereupon. The same manner of trace material film is used for the upper trace layer.

(0023) Next, as shown in FIG. 2, plasma oxide film 9a is deposited over the entire surface to a thickness of no greater than on the order of 100 nm to 200 nm, whereupon TEOS oxide film 9b is further deposited thereupon. Here, the reason why the thickness of the plasma oxide film 9a is set to 100 nm to 200 nm is that the effect of preventing diffusion of moisture and the like will be inadequate below 100 nm, and coverage will be impaired above 200 nm, facilitating the formation of voids and the like. Furthermore, it is preferred that this plasma oxide film 9a is deposited on the layer 1 trace 8 serving as support in such a way that it attains a thickness of on the order of 20 nm or greater on the sides thereof, and hence is deposited to a film thickness that will yield such a thickness on the sides as well. In concrete terms, roughly 150 nm of plasma oxide film 9a is deposited by plasma CVD using mixed gas containing at least SiH₄ and N₂O gas as the source gas, such that the step of the layer 1 trace 8 is reflected on the surface. In concrete terms, roughly 150 nm of TEOS oxide film 9b is deposited by CVD using Si(OC₂H₅)₄+F₂ as the source gas. By this means, the TEOS oxide film 9b will become a film that, during deposition thereof, incorporates fluorine in a concentration of at least 5×10^{20} atoms/cm³.

(0024) Next, the uneven surface of the TEOS oxide film 9b is removed by a method such as, for example, CMP (Chemical Mechanical Polishing) until, as shown in FIG. 3, a leveled surface with a thickness of 450 nm is achieved. The reason why this is done is because, in devices with a multilayered trace structure with two or more layers, it is necessary to flatten the interlayer insulation film in consideration of the impact on trace layers formed in the upper layers. Aside from CMP, this can be accomplished by applying resist and then etching back. However, any method can be used to achieve leveling in this way in this invention, as long as it achieves the intended effect.

(0025) As miniaturization of traces advances, and the pitch of the layer 1 trace 8 becomes increasingly narrow, the shape of the interlayer insulation film deposited thereupon

becomes increasingly degraded, facilitating the formation of voids. In this embodiment example, TEOS oxide film 9b is deposited under conditions where it will contain a high concentration of fluorine in the hope that, by imparting the resultant film with superior step coverage in comparison with TEOS oxide film with a fluorine concentration of no greater than 1×10^{20} atoms/cm³, this will have a mitigating effect on shape deformation arising from miniaturization. An even more preferable concentration of fluorine in the TEOS oxide film during film deposition is on the order of 1×10^{21} atoms/cm³.

(0026) The plasma oxide film 9a is a compact film with low gas permeability in comparison with TEOS oxide film 9b. However, because its step coverage is not very good, it cannot be deposited too thickly. This is why the thickness is increased by depositing the TEOS oxide film 9b on the plasma oxide film 9a, followed by leveling. To add to this, using only plasma oxide film 9a is disadvantageous towards achieving high speed due to the fact that its high permittivity would result in a large capacitance between layers if used on its own. Hence, it is efficacious to use low-permittivity TEOS oxide film 9b as interlayer insulation film, which will have electrode traces at the top and bottom thereof.

(0027) After the TEOS oxide film 9b has been leveled, annealing is performed, for example at 450 °C. Next, as shown in FIG. 4, plasma oxide film 9c is deposited over the entire surface of the TEOS oxide film 9b under the same conditions as the previous plasma oxide film 9a, for example to a thickness of on the order of 500 nm. As stated above, plasma oxide film has poor step coverage; however, because the base has been levelled by the TEOS oxide film 9b, it is possible to accumulate the thickness required to prevent hydrogen diffusion without accruing defects.

(0028) By this means, it is possible to form a second interlayer insulation film 9 with a three-layer structure comprising a stack of plasma oxide film 9a as first insulation film, TEOS oxide film 9b as second insulation film, and plasma oxide film 9c as third insulation film.

(0029) Subsequently, although not shown in the drawings, via-holes are formed and via plugs are embedded into the interlayer insulation film 9 in order to establish an electrical connection between the layer 1 trace 8 and the traces to be formed above the same.

(0030) After formation of via plugs, as shown in FIG. 5, a layer 2 metal trace 10 is formed by depositing 600 nm of metal trace material such as Al or the like and patterning according to the standard method.

(0031) Next, as shown in FIG. 6, a passivation film 21 is formed by depositing TEOS oxide film 21a over the entire surface to on the order of 300 nm, and then depositing plasma nitride film 21b to on the order of 600 nm. Subsequently, although not shown in the drawings, a pad portion is formed by selectively etching back the passivation film 21 according to the standard method, after which terminals are extracted, thereby completing the non-volatile semiconductor memory.

(0032) The reason why annealing is performed in this embodiment example after performing CMP on the TEOS oxide film 9b in the process in FIG. 3 is to anneal out the moisture absorbed thereby, as TEOS oxide film 9b readily absorbs moisture. Another reason for performing annealing

is to anneal out readily released fluorine contained in the TEOS oxide film 9b. Excess fluorine can have the undesirable effect of causing increased absorption of moisture in the TEOS oxide film 9b. Additionally, applying the plasma oxide film 9c onto the TEOS oxide film 9b without first performing annealing will prevent venting of excess fluorine gas during the subsequent heating process, which can lead to anomalies such as peeling depending on the fluorine concentration.

(0033) Toward the above-stated objective, it is preferred to perform annealing of the TEOS oxide 9b within a temperature range of 300-450 °C. In situations where it is possible to enact controls preventing problematic levels of moisture absorption during the manufacturing process, or where there is no risk of peeling due to fluorine, it is not strictly necessary to implement the above-described annealing process. Furthermore, although annealing was performed in the embodiment example after levelling the TEOS oxide film 9b, it is also acceptable to perform annealing immediately after deposition. However, the most preferred approach is to anneal out after levelling and then to immediately coat the plasma oxide film 9c, as gas is more easily removed if annealing is performed after the overall thickness has been reduced by levelling, and moisture may become re-absorbed in the interim if levelling is performed after annealing.

(0034) According to this embodiment example, a plasma oxide film 9a is formed directly under a TEOS oxide film 9b, thereby making it possible to prevent diffusion of moisture into the non-volatile memory cells 2 in the layers below. For the thickness of the plasma oxide film 9a, a thickness of on the order of 100-200 nm is required. The reason why, in this embodiment example, a plasma oxide film 9c is deposited over the entire surface of a levelled TEOS oxide film 9b is to prevent diffusion of hydrogen in the plasma nitride film 21b that is a component of the passivation film 21. To obtain this effect, the plasma oxide film 9c in the interlayer insulation film 9 of the topmost layer preferably has a thickness of 200 nm or greater. In consideration of subsequent processes, the thickness thereof is desirably set to a practicable level of no more than 600 nm. Note that, prior to now, it was believed that the way to control diffusion of hydrogen from nitride film was a structure in which plasma oxide film is provided immediately beneath plasma nitride film, as shown in FIG. 26. However, as miniaturization progresses and the pitch of the topmost layer of trace consequently becomes narrower, it will become impossible to cover the trace in the topmost layer with plasma oxide film, which provides a poor coverage shape. According to the structure of this embodiment example, the topmost layer of the interlayer insulation film 9 below the topmost trace layer 10 is a plasma oxide film 9c deposited on a levelled TEOS oxide film 9b, which makes it easy to form the plasma oxide film 9c to the thickness required to prevent diffusion of hydrogen.

(0035) Note that, in this embodiment example, the TEOS oxide film 9b is levelled by CMP or the like immediately after deposition, and the preferred thickness after levelling is 200-500 nm. The reason for this is to make it possible to deposit the plasma oxide film 9c formed thereupon in a relative uniform manner, as well as to accommodate the requirements for forming vias in the interlayer insulation film 9, and the requirements for performing

photolithography for the purpose of patterning the trace 10 formed on the interlayer insulation film 9. Consequently, as long as a practicable degree of levelness can be maintained, it is not strictly necessary to intentionally implement a levelling process.

(0036) Moisture diffusing into the interlayer insulation film has the detrimental effect of lowering the threshold of non-volatile memory cells in write mode. Furthermore, hydrogen diffusing from plasma nitride film upon repeated writing/erasing of non-volatile memory cells causes degradation of the write/erase performance thereof, lowering the operating margin of the device. According to this embodiment example, adopting a 3-layer structure comprising a plasma oxide film 9a, a TEOS oxide film 9b, and a plasma oxide film 9c makes it possible to prevent diffusion of moisture and hydrogen into the non-volatile memory cell area, thereby making it possible to obtain highly reliable non-volatile memory.

(0037) FIG. 7 through FIG. 12 show the manufacturing process for embodiment example no. 2, in which this invention is applied to non-volatile semiconductor memory with a 3-layer metal trace. FIG. 7 corresponds to the state in FIG. 3 for embodiment example no. 1, which is the state in which annealing has been performed after stacking a plasma oxide film 9a and TEOS oxide film 9b on a layer 1 trace 8 and levelling the TEOS oxide film 9b. The embodiment examples are identical up until this point.

(0038) Subsequently, unlike in embodiment example no. 1, as shown in FIG. 8, via plugs not shown in the drawings are embedded and the layer 2 metal trace 10 is patterned without first depositing a plasma oxide film. Next, under the same conditions as those for the process in embodiment example no. 1 in which a second interlayer insulation film 9 was formed, a plasma oxide film 11a and TEOS oxide film 11b are deposited (FIG. 9); the surface of the TEOS oxide film 11b is levelled (FIG. 10); and plasma oxide film 11c is deposited thereupon, thereby forming a third interlayer insulation film 11 with a 3-layer structure (FIG. 11).

(0039) After then embedding via plugs into this third interlayer insulation film 11 and forming a pattern in the layer 3 trace 12, a passivation film 21 is formed (FIG. 12). The passivation film 21 consists of a film stack of TEOS oxide film 21a and plasma nitride film 21b formed under the same conditions as embodiment example no. 1.

(0040) In this embodiment example, the second interlayer insulation film 9 between the layer 1 trace 8 and the layer 2 trace 10 has a two-layer structure comprising a plasma oxide film 9a and TEOS oxide film 9b, while the third interlayer insulation film 11 between the layer 2 trace 10 and the layer 3 trace 12 has a three-layer structure comprising plasma oxide film 11a, TEOS oxide film 11b, and plasma oxide film 11c. The reason why the third interlayer insulation film 11 is given a three-layer structure is the same as the reason why the second interlayer insulation film 9 in embodiment example no. 1 is given a three-layer structure. Namely, because the lowermost plasma oxide film 11a serves the function of preventing diffusion of moisture from the levels above the same into the non-volatile memory cells 2. Additionally, the plasma oxide film 11c that is the topmost layer of the three-layer structure serves the function of preventing diffusion of hydrogen from the levels above the same into the non-volatile memory cells 2.

(0041) Since diffusion of hydrogen from the passivation film 21 is prevented by the plasma oxide film 11c, the second interlayer insulation film 9 is given a two-layer film structure without forming a plasma oxide film immediately above the TEOS oxide film 9b. As described above, the plasma oxide film 9a immediately below the TEOS oxide film 9b serves the same purpose of preventing diffusion of moisture from the TEOS oxide film 9b.

(0042) Because this embodiment example is also able to adequately prevent diffusion of moisture and hydrogen into non-volatile memory cells, it is possible for a non-volatile memory device to maintain highly reliable performance.

(0043) Note that although this embodiment example was described using as an example non-volatile memory with a 3-layer trace structure, the same effect can be obtained using the same interlayer insulation film structure in a device with a multilayered trace structure of four or more layers. In short, generally speaking, if the focus is on the function of preventing diffusion of hydrogen from the passivation film, the reliability of non-volatile memory can be improved by adopting a two-layer stacked structure comprising plasma oxide film and TEOS oxide film for the interlayer insulation film interposed between an arbitrary trace layer number (n-1) and trace layer number n of a multilayered trace, or, if also taking into consideration the function of preventing diffusion of moisture from the TEOS film, by adopting a three-layer stacked structure comprising plasma oxide film, TEOS oxide film, and plasma oxide film.

(0044) FIG. 13 through FIG. 17 show the manufacturing process for embodiment example no. 3, in which this invention is applied to non-volatile semiconductor memory with a 3-layer metal trace. FIG. 13 corresponds to FIG. 5 of embodiment example no. 1, showing the state in which a layer 2 trace 10 is formed on a second interlayer insulation film 9 with a 3-layer structure.

(0045) Subsequently, a plasma oxide film 11a is deposited and a TEOS oxide film 11b is deposited (FIG. 14); the TEOS oxide film 11b is levelled and annealed (FIG. 15); and a plasma oxide film 11c is deposited on the levelled TEOS oxide film 11b under the same conditions as the second interlayer insulation film 9 (FIG. 16). This yields a third interlayer insulation film 11 with a 3-layer structure identical to that of the second interlayer insulation film 9.

(0046) Next, after embedding the required via plugs into the interlayer insulation film 11, the layer 3 trace 12 is patterned in the same way as embodiment example no. 2, and a passivation film 21 is formed thereupon (FIG. 17).

(0047) In this embodiment example, the interlayer insulation film 9 and 11 interposed between the three trace layers 8, 10, and 12 each have a three-layer structure comprising plasma oxide film/TEOS oxide film/plasma oxide film. In short, the plasma oxide film 9a and 11a serving as the base for the TEOS oxide film 9b and 11b is uneven in a way that reflects the unevenness of the traces, and serves the function of preventing diffusion of moisture from the TEOS oxide film 9b and 11b situated above the same. The plasma oxide film 9c and 11c formed levelly on each respective levelly formed TEOS oxide film 9b and 11b is given an adequate thickness to serve the function of preventing diffusion of hydrogen from the passivation film.

(0048) This embodiment differs from embodiment example no. 2 in particular in the fact that the interlayer insulation

film 9 above the layer 1 trace 8 is also given a 3-layer structure, which yields the following effect. By levelling the TEOS oxide film 9b and then annealing out before capping by depositing a plasma oxide film 9c over the entire surface thereof, it becomes possible to suppress re-absorption of moisture into the TEOS oxide film 9b after the moisture has been annealed out. This also makes it possible for the plasma oxide film 9c to prevent diffusion of moisture and fluorine from the interlayer insulation film 11 of the layer above. (0049) According to this embodiment example, it is possible to even more reliably prevent diffusion of moisture, hydrogen, etc. into the non-volatile memory cell in comparison with embodiment example no. 2, thereby making it possible to maintain highly reliable performance of the non-volatile memory cell.

(0050) Moreover, in each of the above-described embodiment examples, the standard procedure is to first form the passivation layer and then finally perform sintering at a temperature of on the order of 450 °C. However, in the event that heat treatment is performed with each trace layer covered with plasma oxide film in the manner described for each embodiment example, in some instances it may prove impossible to release N contained in the TiN film of the trace layer to the exterior due to the fact that the plasma oxide film is a compact film, which may result in film peeling.

(0051) To overcome this challenge, it is preferred that heat treatment is performed after each trace layer has been formed, but prior to depositing plasma oxide film thereupon, at a temperature of on the order of no greater than 400 °C. This makes it possible to release N contained in the trace material film to the exterior, thereby preventing the occurrence of film peeling during the subsequent heat treatment process. This heat treatment performed immediately after trace formation needs to be performed at a relatively low temperature in order to prevent the occurrence of Al hillocks. In short, assuming that the trace material has a Ti/TiN/Al-Cu/TiN stack structure, as described above, this means that the Al-Cu film is enclosed on the top and bottom by TiN film, so performing heat treatment at on the order of 450 °C or greater will cause hillocks to form on the sides of the trace, potentially causing trace shorts if the pitch is fine enough. In order to prevent the growth of such hillocks and simultaneously allow N to disperse, it is preferred that heat treatment is performed immediately after trace formation within the temperature range of 380-400 °C. Performing low-temperature heat treatment for an excessively long time will cause hillock growth, so heat treatment time should be short, preferably on the order of 15 minutes or less.

(0052) By thus including a heat treatment process for removal of N immediately after trace formation, it becomes possible to prevent the trace from peeling when subsequently heat treatment is performed after levelling the TEOS film or when sintering is performed after forming the passivation film.

(0053) Additionally, although in each of the above-described embodiment examples TEOS oxide film was deposited thickly for the purpose of levelling the trace layer, voids 31 may occur between traces in the manner indicated in FIG. 18 in the event that the coat of TEOS oxide film is poorly shaped. If CMP is performed under these conditions, when the ground surface attains the void 31, contaminants such as

grinding compound will infiltrate into the void 31, adversely impacting the reliability of the memory cells, which are particularly sensitive to contamination.

(0054) Consequently, in the event that voids 31 of the kind shown in FIG. 18 should occur, it is preferred that the levelling process be controlled in such a way that performing CMP does not cause the surface level of the TEOS oxide film 9b to attain the voids 31, as shown in FIG. 19. The same applies in the case of the upper TEOS oxide film 11b.

(0055) Furthermore, although a detailed description was not provided for the contact components between the memory cell, etc. and the diffusion layer, the standard procedure is to form the contact holes, then perform ion implantation in such a way as to overlap with the diffusion layer already formed through the contact hole, and then perform RTA (Rapid Thermal Annealing) for the purpose of activating the implanted impurities. However, if RTA is performed for only a short length of time, in some instances it may not be possible to eliminate process damage occurring on the surface of the trace layer during formation of contact holes by RIE.

(0056) An example of the preferred contact hole formation process for solving this problem will be described with reference to FIG. 20 through FIG. 24. FIG. 20 shows the state in which a first interlayer insulation film 7 made of BPSG or the like has been deposited after formation of memory cells 2. Subsequently, as shown in FIG. 21, contact holes 32 are formed in the diffusion layer 5 by RIE. Next, in this state, furnace annealing is performed in an N₂ atmosphere at a lower temperature than the temperature at which RTA was performed to activate the impurities. Preferred conditions for this furnace annealing are: 700-900 °C for on the order of 30 minutes.

(0057) Subsequently, as shown in FIG. 22, self-aligned ion implantation is carried out in the contact holes 32. RTA is then performed in an N₂ atmosphere at 900 °C for on the order of 30 seconds to activate the implanted impurities, forming a high-concentration n⁺⁺ diffusion layer 5a overlapping with the diffusion layer 5, as shown in FIG. 23. Finally, as shown in FIG. 24, a metal trace 33 is formed.

(0058) Using a manufacturing process of this kind, performing furnace annealing after contact hole formation makes it possible to restore process damage caused during contact hole formation, as well as to simultaneously anneal out moisture absorbed by the interlayer insulation film 7 of BPSG film or the like. Because moisture contained in the interlayer insulation film 7 is a major cause of deterioration of reliability in non-volatile memory cells, this furnace annealing makes it possible to improve reliability. In particular, furnace annealing after contact hole formation is effective because doing so anneals out moisture from the contact holes formed in the vicinity of the memory cells.

(0059) Furthermore, by performing the above-described furnace annealing prior to the ion implantation process, which is self-aligning relative to the contact holes, it is possible to prevent unnecessary extension of the diffusion layer. Additionally, activation of implanted impurities by high-temperature/short-duration RTA yields low contact resistance in the traces. This manner of furnace annealing and RTA can be applied even in cases where a high-concentration p⁺⁺-type layer is formed by self-aligning ion

implantation of BF₂ or the like into the p⁺⁺-type diffusion layer from the contact holes.

(0060) Although the preceding embodiment examples all focused exclusively on the interlayer insulation film of the metal trace layers, it is also possible to form a plasma oxide film 7b on the surface of the first interlayer insulation film 7 of BPSG or the like that covers the element formation surface, as shown in FIG. 24. This makes it possible to more effectively prevent diffusion of hydrogen from the passivation film to the memory cells, etc.

(0061) Furthermore, although in the embodiment examples TEOS film was used for the levelled insulation film, this invention is efficacious even if insulation film or SOG (Spin-On-Glass) film or the like made using different organic oxyasilane gas is used as the levelled insulation film.

(0062)

(EFFECT OF THE INVENTION) As described above, according to this invention, by adopting a stacked structure for the interlayer insulation film comprising levelled insulation film made of TEOS film or the like and compact insulation film made of plasma oxide film or the like, or even more preferably, adopting a three-layer stacked structure of compact insulation film/levelled insulation film/compact insulation film, it is possible to prevent diffusion of hydrogen from the passivation film, which includes plasma nitride film, to the circuit element area, or diffusion of moisture or fluorine from the levelled insulation film to the circuit element area, thereby improving the reliability of the semiconductor device, which in particular provides a significant effect when applied to non-volatile semiconductor memory.

(FIG. 1) Cross-section showing the process up until formation of the layer 1 trace in embodiment example no. 1 of this invention.

(FIG. 2) Cross-section showing the process of depositing TEOS oxide film of the second interlayer insulation film in the same embodiment example.

(FIG. 3) Cross-section showing the process of levelling the TEOS oxide film in the same embodiment example.

(FIG. 4) Cross-section showing the process of depositing plasma oxide film on the TEOS oxide film in the same embodiment example.

(FIG. 5) Cross-section showing the process of forming the layer 2 trace in the same embodiment example.

(FIG. 6) Cross-section showing the process of forming the passivation film in the same embodiment example.

(FIG. 7) Cross-section showing the process of forming the second interlayer insulation film according to embodiment example no. 2.

(FIG. 8) Cross-section showing the process of forming the layer 2 trace in the same embodiment example.

(FIG. 9) Cross-section showing the process of depositing the TEOS oxide film of the third interlayer insulation film in the same embodiment example.

(FIG. 10) Cross-section showing the process of levelling the TEOS oxide film in the same embodiment example.

(FIG. 11) Cross-section showing the process of depositing plasma oxide film on the TEOS oxide film in the same embodiment example.

(FIG. 12) Cross-section showing the process of forming the layer 3 trace and passivation film in the same embodiment example.

(FIG. 13) Cross-section showing the process up until formation of the layer 2 trace in embodiment example no. 3.
 (FIG. 14) Cross-section showing the process of depositing the TEOS oxide film of the third interlayer insulation film in the same embodiment example.
 (FIG. 15) Cross-section showing the process of levelling the TEOS oxide film in the same embodiment example.
 (FIG. 16) Cross-section showing the process of depositing plasma oxide film on the TEOS oxide film in the same embodiment example.
 (FIG. 17) Cross-section showing the process of forming the layer 3 trace and passivation film in the same embodiment example.
 (FIG. 18) Cross-section showing the manner in which voids are produced in the TEOS oxide film.
 (FIG. 19) Cross-section showing the process of levelling the TEOS oxide film without eliminating voids.
 (FIG. 20) Cross-section showing the process up until formation of the first interlayer insulation film, serving to illustrate the preferred contact hole formation process.
 (FIG. 21) Cross-section showing the process of forming contact holes in the first interlayer insulation film.
 (FIG. 22) Cross-section showing the process of performing ion implantation through the contact holes.
 (FIG. 23) Cross-section showing the RTA process after ion

implantation.

(FIG. 24) Cross-section showing the process of forming traces after performing RTA.

(FIG. 25) Cross-section showing an example of the deposition of plasma oxide film on the first interlayer insulation film.

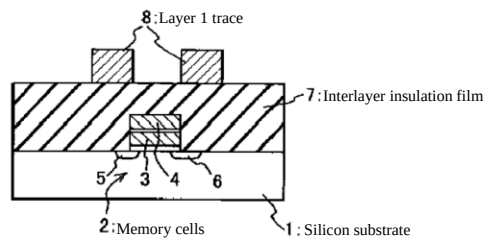
(FIG. 26) Cross-section showing the two-layer trace structure of prior-art non-volatile memory.

(FIG. 27) Cross-section illustrating the issues with prior-art non-volatile memory with a two-layer trace structure.

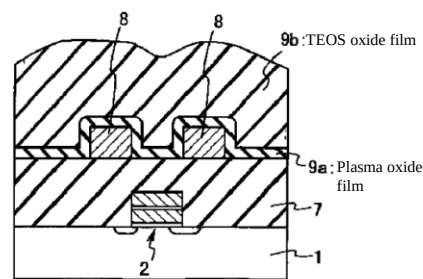
(EXPLANATION OF REFERENCES)

1: Silicon substrate, 2: non-volatile memory cell, 7: first interlayer insulation film, 8: layer 1 metal trace, 9: second interlayer insulation film, 9a: plasma oxide film, 9b: TEOS oxide film, 9c: plasma oxide film, 10: layer 2 metal trace, 11: third interlayer insulation film, 11a: plasma oxide film, 11b: TEOS oxide film, 11c: plasma oxide film, 12: layer 3 metal trace, 21: passivation film, 21a: TEOS oxide film, 21b: plasma nitride film.

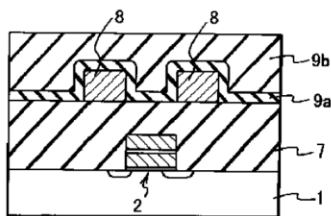
(FIG. 1)



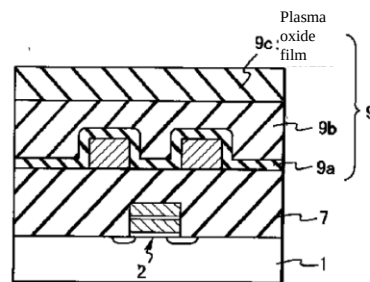
(FIG. 2)



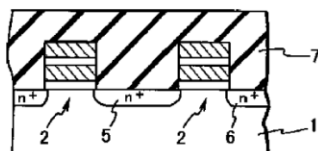
(FIG. 3)



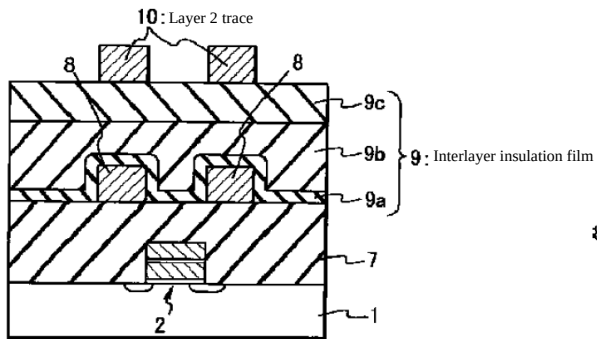
(FIG. 4)



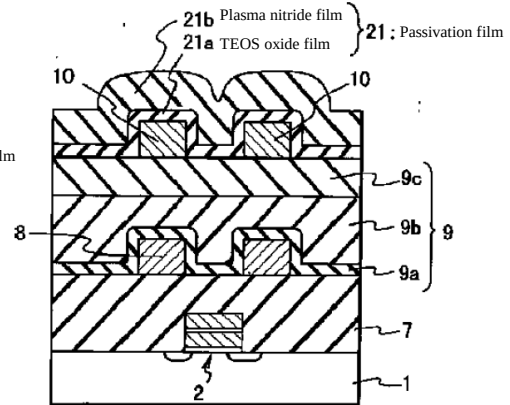
(FIG. 20)



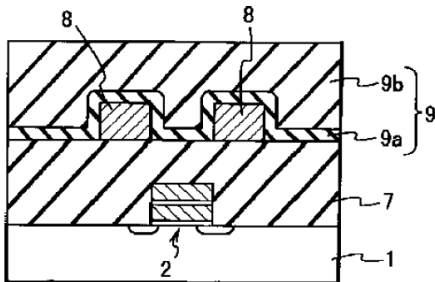
(FIG. 5)



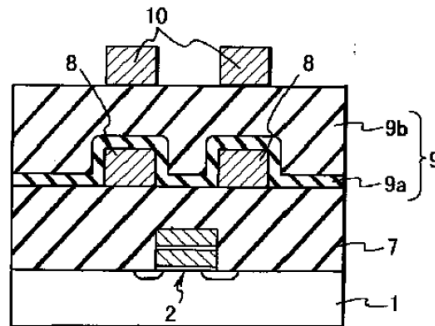
(FIG. 6)



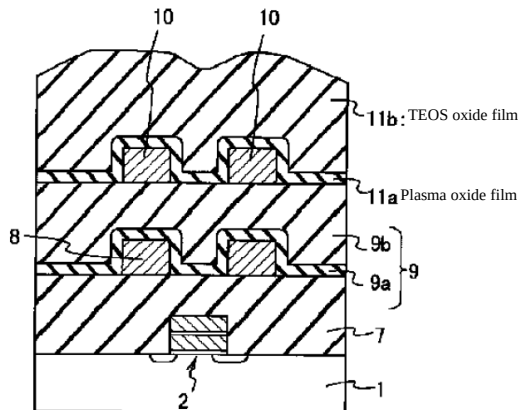
(FIG. 7)



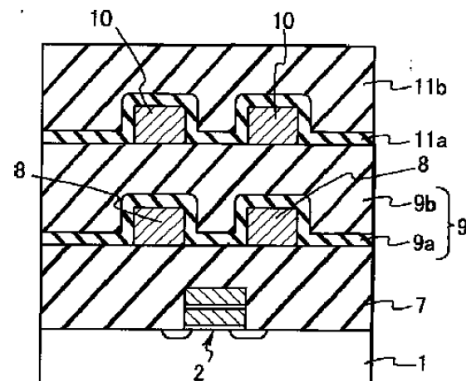
(FIG. 8)



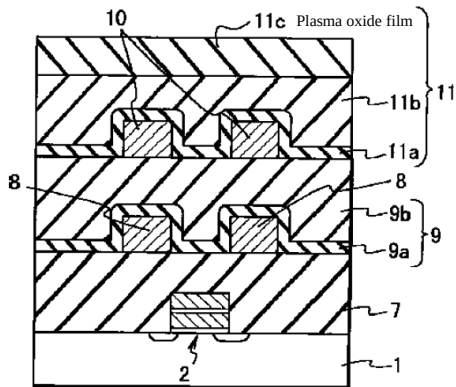
(FIG. 9)



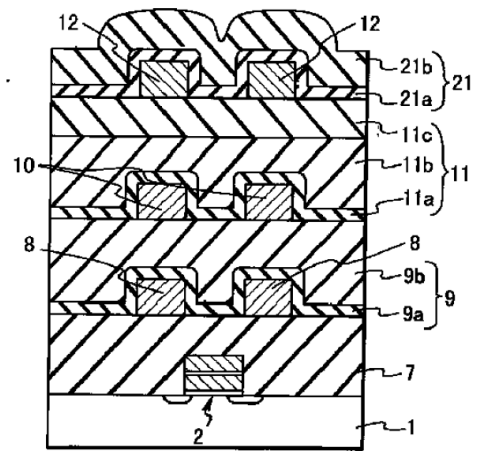
(FIG. 10)



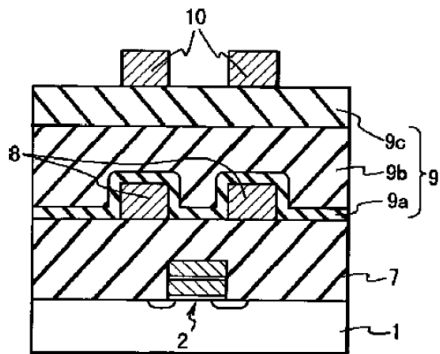
(FIG. 11)



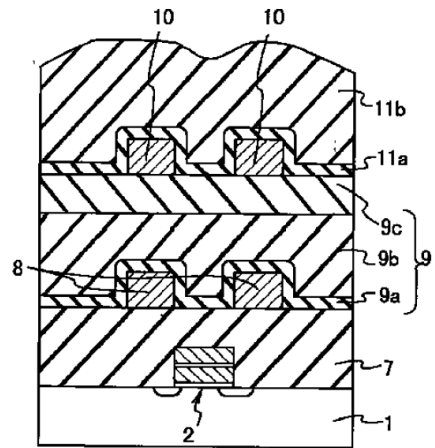
(FIG. 12)



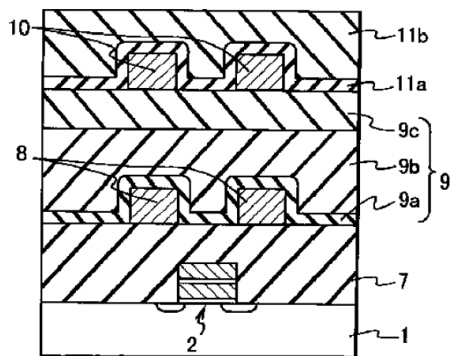
(FIG. 13)



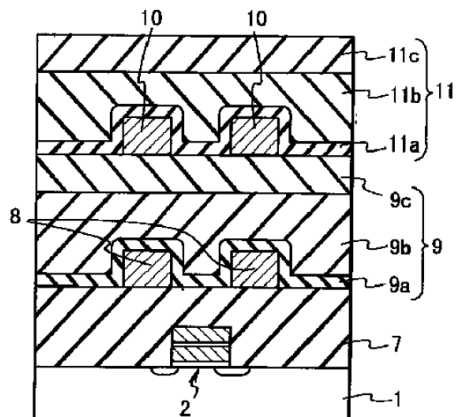
(FIG. 14)



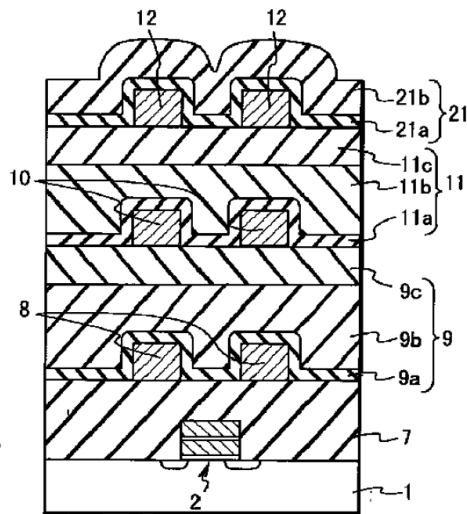
(FIG. 15)



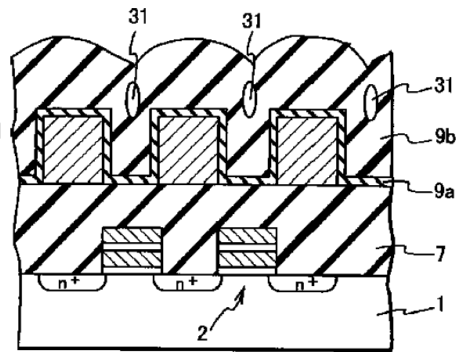
(FIG. 16)



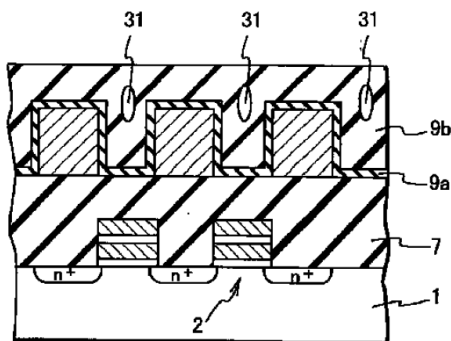
(FIG. 17)



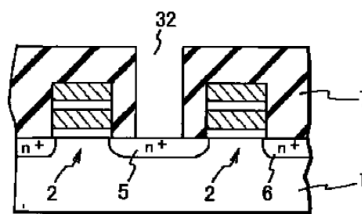
(FIG. 18)



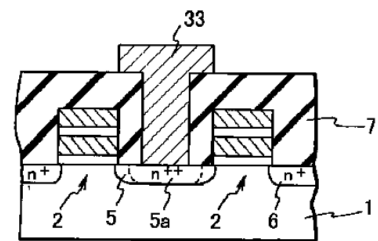
(FIG. 19)



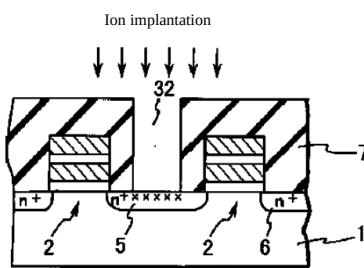
(FIG. 21)



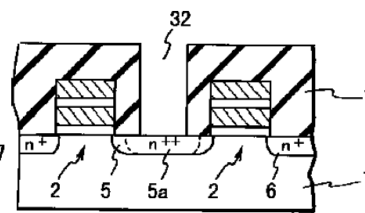
(FIG. 24)



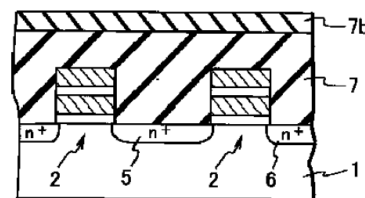
(FIG. 22)



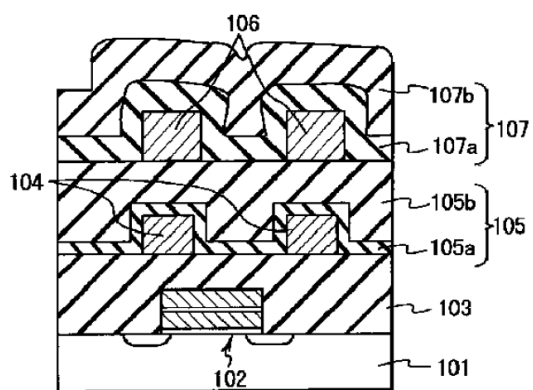
(FIG. 23)



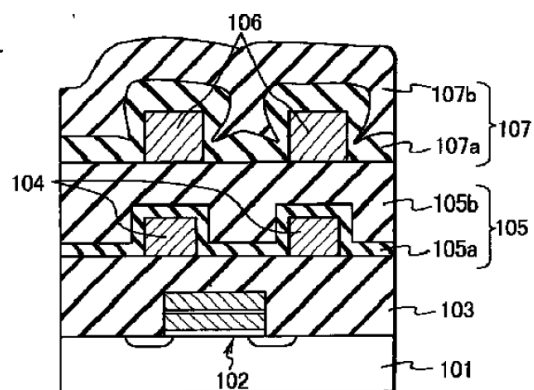
(FIG. 25)



(FIG. 26)



(FIG. 27)



Continued from front page

(51) Int. Cl.⁶

H01L 29/788
29/792

Identification codes

FI