

Silicon Processing

for the VLSI Era

Volume 2 - Process Integration

**SILICON PROCESSING
FOR
THE VLSI ERA**

**VOLUME 2:
PROCESS INTEGRATION**

STANLEY WOLF Ph.D.
Professor, Department of Electrical Engineering
California State University, Long Beach
Long Beach, California

LATTICE PRESS

Sunset Beach, California

DISCLAIMER

This publication is based on sources and information believed to be reliable, but the authors and Lattice Press disclaim any warranty or liability based on or relating to the contents of this publication.

Published by:

Lattice Press,
Post Office Box 340
Sunset Beach, California 90742, U.S.A.

Cover design by Roy Montibon, Visionary Art Resources, Inc., Santa Ana, CA.

Copyright © 1990 by Lattice Press.

All rights reserved. No part of this book may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying, recording or by any information storage and retrieval system without written permission from the publisher, except for the inclusion of brief quotations in a review.

Library of Congress Cataloging in Publication Data
Wolf, Stanley

Silicon Processing for the VLSI Era
Volume 2 : Process Integration

Includes Index

1. Integrated circuits-Very large scale integration. 2. Silicon. I. Title

ISBN 0-961672-4-5

9 8 7 6 5 4 3 2 1

PRINTED IN THE UNITED STATES OF AMERICA

- PECVD TEOS film, deposited at 330°C. (Figure 4-54c shows that the resulting hillock size and density are both small.)¹⁷²
- ECR deposition (see section 4.4.10).
- Photo-CVD SiO₂.¹⁸³
- Afterglow-CVD of SiO₂.²⁴
- Anodized Al deposition.¹⁸⁴

Once such dielectric films are in place, they suppress hillock growth during later thermal cycling.

- *Use of refractory metal films such as W or Mo (which exhibit much less propensity to form hillocks at 400°-500°C) in place of Al.*
- *Use of an ionized cluster beam deposition process to deposit smooth Al/CaF₂/Si films. According to the report on this process, the films remained hillock free up to temperatures of 500°C.*¹⁸⁵

4.7.4.2 Dielectric Void Reliability Problems. If the voids are opened following an etchback step, they can trap moisture or photoresist residues that can cause long term reliability problems. In addition, metal may be deposited into the voids that can be very difficult to remove by etching, thus producing shorting between neighboring metal lines.

4.8 PASSIVATION LAYERS

Following patterning of the final metal layer, a passivation layer is deposited over the entire top surface of the wafers. This is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging. The desired properties of the passivation materials are given in Table 4-5. In general, the thicker the passivation layer the better, since a thicker layer will provide better protection and improve the electromigration resistance of underlying Al lines. On the other hand, because thicker CVD films (especially silicon nitride films) have a higher tendency to crack, there is normally an upper limit to the thickness.

The final mask, called the pad mask or bonding contact mask, is used to define patterns corresponding to the regions in which electrical contact to the finished circuit will be made. These patterns in a resist layer allow openings in the passivation layer to be etched down to Al areas on the circuit called bonding pads (see chap. 5, Fig. 5-16). Either wet or dry etching can be used to etch the passivation layer. Since the dimensions of the pads are so large (i.e., normally 100 x 100 μm), wet etching is still frequently used to etch PSG films, while silicon nitride films are more easily etched by means of a dry etching process.

Phosphorus-doped, low-temperature CVD SiO₂ films were the first passivation layers to be used. The phosphorus is added to the SiO₂ to reduce the stresses in the film (and to thereby decrease the tendency of the film to crack), as well as to improve the gettering

properties of the film (with respect to sodium ions and other fast-diffusing metallic contaminants). The higher the phosphorus concentration, the better these characteristics will be.

On the other hand, if more than 6 wt% phosphorus is added to the film, corrosion can become a serious problem, especially in the case of chips mounted in plastic, nonhermetic packages. Water vapor can rapidly penetrate the plastic packaging material, transporting with it contaminants from the surface of the package. If the PSG contains excess phosphorus, the moisture can react with it to form phosphoric acid (HPO_3), which will eventually penetrate the film. As noted earlier, electrochemical corrosion of the Al lines can lead to metallization failure. While the transport of contaminated moisture through the PSG is a relatively slow process, if cracks or defects (e.g., pinholes) exist in the film, the water vapor will be able to penetrate it much more rapidly.

Silicon nitride has also been used as a passivation-layer material because it provides an impermeable barrier to moisture and mobile impurities (e.g., sodium) and also forms a tough coat that protects the chips against scratching. Its high dielectric constant is not a disadvantage for this application, since the passivation layer is deposited on top of the last metal layer.

However, because the passivation layer must be deposited over Al films, only PECVD silicon nitride can be used for this application (since it is deposited at $\sim 300^\circ\text{C}$). Unfortunately, PECVD nitride films normally exhibit a high mechanical stress ($\sim 6\text{--}8 \times 10^8 \text{ Pa}$), which can cause cracks in the film during heating after deposition (especially at steps). The high compressive stresses in the films have also been shown to enhance void formation in Al interconnects (see section 4.7).

In addition, PECVD silicon nitride tends to be nonstoichiometric and contains substantial quantities of atomic hydrogen (10-30 at%). Large quantities of hydrogen have been found to accelerate hot-electron aging effects in MOS devices (see section 5.6.6). It has also been reported that the hydrogen from PECVD nitride is responsible for the formation of bubbles or cavities at the metal-plasma nitride interface when Al:Si alloys are used as the metallization. These appear after the 450°C anneal that is carried out following nitride deposition. It is supposed that the hydrogen reacts with the Si precipitates in the Al film to form gaseous compounds that produce the bubbles.^{186,187} It has been recommended that a low-hydrogen-content passivation film be used, if nitride passivation is selected for MOS technologies with gate lengths of less than $1.5 \mu\text{m}$ (in which hot-electron degradation is significant).

Work has been done to develop processes for growing nitride films with low hydrogen concentration and stress, and more is now understood about the relationship of the film properties to such deposition conditions as rf frequency, power, and bias.¹⁸⁸ Lower H_2 concentrations in the nitride have been obtained when the film is formed with $\text{SiH}_4\text{-N}_2$ mixtures rather than with conventional $\text{SiH}_4\text{-NH}_3$ mixtures.¹⁸⁹ Fluorinated nitride (F-SiN) films have been developed that exhibit only 0.6% of hydrogen (in the form of Si-H).^{190,191}

The use of PECVD silicon-oxynitride films (deposited with SiH_4 , NH_3 , N_2 , and N_2O mixtures) as alternative passivation materials has also been investigated, since they exhibit nearly the same the moisture and sodium barrier characteristics of nitrides.

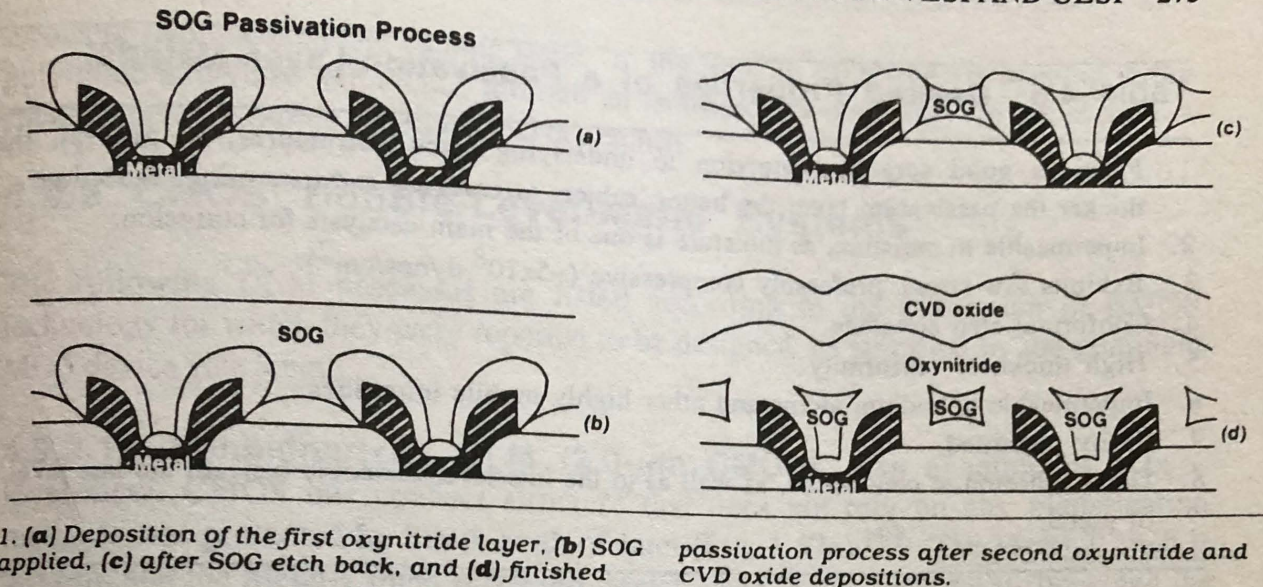


Fig. 4-56 Using SOG film as a part of the passivation overcoat improves EPROM reliability.²⁵⁶ Reprinted with permission of Semiconductor International.

While not quite as good as those of nitrides, the characteristics are better than those of oxides.¹⁹² However, their stress is between that of APCVD oxide (tensile) and plasma nitride and oxide (compressive).¹⁹³ In addition, because the stress is a function of applied rf power, pressure, and bias, it is possible to optimize the stress by using bias. Ideally, a very low-stress dielectric oxynitride film can be formed that will still maintain good diffusion-barrier properties. (It is important to characterize the stress over the entire temperature range of operation to which the dielectric film will be subjected, since the stress can exhibit hysteresis effects. These may be due to structural changes in the film due to loss of material during heating.) Finally, it is reported that PECVD oxynitride films can be formed that contain considerably less H_2 (~one-half, in one report) than do PECVD nitrides.¹⁹⁴

Another, more recently adopted approach to the formation of passivation layers involves multilayer passivation coating. An initial coating of PECVD oxide is deposited, followed by a PECVD nitride. The oxide layer reduces the mechanical stress (~40%) and the hydrogen content of the passivation layer, while the nitride protects the device against handling, humidity, and mobile ions. This inorganic bilayer may be followed by a polyimide layer that is several microns thick (especially useful in automated bump-bonding processes) and a thick layer of silicone gel, or similar material, for cushioning and for void elimination during die bonding.

In a second variation of this technique applied to EPROMs, a sandwich oxynitride- (etchedback) SOG-oxynitride layer is first formed. This film is then covered with a low phosphorus- content CVD-oxide layer to complete the composite passivation film (Fig. 4-56). Sandwiching the SOG film between the two oxynitride layers reduces the occurrence of voids and seams in the passivation layer. These voids and seams caused degraded passivation film coverage, which in turn correlated with increased EPROM array failures after steam stressing.²⁵⁶

5.3.2 Silicon-Gate MOS Technology

One of the key process innovations for MOS ICs was the use of heavily doped polysilicon as the gate electrode in place of Al (see Vol. 1, chap. 6 for more information on polysilicon thin films). The development of this *silicon gate technology* improved the fabrication of MOS ICs in the following ways:

- Since aluminum must be deposited following completion of all high-temperature process steps (including drive-in of the source and drain regions), the gate electrode must be separately aligned to the source and drain. This alignment procedure adversely affects both packing density and parasitic overlap capacitances between the gate and source/drain regions. Since polysilicon has the same high melting point as the silicon substrate, it can be deposited prior to source and drain formation. Furthermore, the gate itself can serve as a mask during formation of the source and drain regions (by either diffusion or ion implantation). The gate thereby becomes nearly perfectly aligned over the channel, with the only overlap of the source and drain being that due to lateral diffusion of the dopant atoms. This *self-alignment* feature simplifies the fabrication sequence, increases packing density, and reduces the gate-source and gate-drain parasitic overlap capacitances.
- The threshold voltage of PMOS devices is reduced by the use of a polysilicon gate, since the ϕ_{ms} is less negative (see Eqs. 5-2). For PMOS devices on <111>-Si, the threshold voltage is reduced from roughly -4 V to -2 V. This smaller threshold voltage value enabled PMOS ICs to become compatible with TTL (bipolar) ICs, allowing MOS to be designed into many digital systems that operated at TTL-defined power supply voltage levels (i.e., 0 V to 5 V).
- The ability of polysilicon to withstand high temperatures also permits it to be completely encapsulated by an SiO_2 layer. This allows the polysilicon film to function as an interconnect path, in addition to serving as the gate electrode. By taking advantage of this new interconnection structure (without having to use a second layer of metal, as was necessary with bipolar ICs), it was possible to give MOS ICs an additional level of interconnection that could be crossed by the usual metal layer, or even by another polysilicon layer. This eased the problem of routing the electrical paths among the devices of an IC, thereby facilitating the layout of compact digital integrated circuits. (Techniques for establishing contact between the polysilicon layer and substrate are described in chap. 3, section 3.11.1). The ability of polysilicon to withstand high temperatures was also exploited to allow the dielectric (e.g. phosphorus-doped SiO_2) that covers it to be flowed, thereby making a significantly smoother surface topography for metallization layers.

The greatest disadvantage of polysilicon as a gate material compared to Al is its significantly higher resistivity. Even when doped at the highest practical levels, it is still much less conductive than aluminum.

concentrations, a 0.5- μm -thick polysilicon film has a sheet resistance of about 20 Ω/sq (compared to ~ 0.05 Ω/sq for a 0.5- μm -thick Al film). The resulting high values of interconnect line resistance can lead to relatively long RC time constants (i.e., long propagation delays) and severe dc voltage variations within a VLSI circuit. Consequently, the formation of refractory metal silicide layers on top of polysilicon layers (which results in so-called *polycide* films) was developed to reduce the severity of this drawback. Such polycide films can provide sheet resistances of 1 Ω/sq , at the expense of more complex processing (see Vol. 1, chap. 11 for more information on polycides). Despite of the above limitation, the development of silicon-gate technology proved to be the most important contribution to MOS technology during the reign of PMOS.

5.3.3 Reduction of Oxide-Charge Densities

Another set of important advances allowed the magnitude of the positive oxide-charge densities to be reduced. These oxide charge reduction techniques can be summarized as those involving *cleanliness*, *gettering*, *annealing*, and *replacing <111> wafers with <100> wafers*.

Cleanliness and gettering techniques reduced the densities of *mobile ionic charge*, which are due to the incorporation of ionized alkali metal atoms (Na^+ , K^+) in the gate oxide. Na contamination can be controlled through clean gate oxidation processing. Gettering is used to prevent any Na^+ that enters the gate oxide from significantly degrading the V_T (see Vol. 1, chap. 7). Although tests for Na contamination of MOS devices must be routinely performed to ensure that accidental contamination does not occur, it is possible to establish fabrication procedures in which the instability of V_T due to mobile ionic charge is less than 0.1 V.

Another source of positive oxide charge is the *interface trap charge*. Again, as described in Volume 1, chapter 7, two annealing techniques were discovered that reduced this charge to acceptably low levels (i.e., to the low $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ range). At these levels the contribution to the threshold voltage of the device is acceptably small for modern MOS devices.

The final source of positive oxide charge is the so-called *fixed oxide charge* which is located in the transition region between the silicon and the SiO_2 (see Vol. 1, chap. 7). It was learned that this charge can be reduced by the use of proper annealing techniques and that the lowest fixed oxide charge densities ($\sim 10^{10} \text{ cm}^{-2}$) are obtained on <100> wafers. As a result, the production of MOS ICs was shifted from <111> to <100> starting material.

In summary, the threshold voltage is negatively shifted by an amount proportional to the sum of these three oxide charge densities, Q_{tot} . When Q_{tot} was quite high this had an extremely important influence on MOS production. Through an enormous effort by the semiconductor community (industry and universities), each of the positive oxide charge density values was reduced. As a result, Q_{tot} can now be kept to 10^{10} cm^{-2} or less. For MOS devices, the oxide charge contribution to