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Reactive ion etch of 150 nm Al lines for interconnections in dynamic random access memory

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Three different aluminum reactive ion etch (RIE) processes have been developed for manufacturing 175 and 150 nm line/space wiring patterns in multilevel interconnection. The three approaches vary in complexity: (1) Conventional organic antireflective coating (ARC) with a photoresist etch mask, (2) inorganic silicon oxynitride dielectric ARC with a photoresist etch mask, and (3) a physical vapor deposition tungsten cap layer used as a hardmask. The reliability performance for the 150 nm Al RIE lines scales with previous technologies at larger groundrules. The process windows for each key parameters are evaluated. It is also shown that the metal etch processes can be extended to even smaller ground rules with a line or space width to height aspect ratio as high as 5 without requiring a new tool set. © 2000 American Vacuum Society. [S0734-2101(00)12704-6]

I. INTRODUCTION

The reduction of operating voltage for each new generation of very large scale integrated devices and commensurate scaling of circuit design ground rules requires geometrically narrower multilevel wiring dimensions. Furthermore, low power consumption calls for the low sheet resistance of the metal wiring, which is usually met by increasing the metal wire stack height or by introduction of lower resistance materials. Aluminum metal reactive ion etch (RIE) wires combined with chemical vapor deposition tungsten plugs has been the standard back-end-of-line (BEOL) multilevel interconnect technology for many years. As Cu technology matures, the question of how much further Al technology could be extended becomes a topic of interest in the semiconductor manufacturing industry. The extension of Al technology is particularly important for dynamic random access memory producers where low cost is essential.¹⁻³ Moreover, it is the common interest of many manufacturers to extend the existing equipment tool sets, designed for Al technology, to the smaller ground rules.

Compared to previous generations, the reduction of wire pitch and the increase in metal stack thickness result in substantially larger aspect ratios of the wire. This presents a substantial challenge to the BEOL aluminum RIE process to etch the thicker metal stack, maintaining the dimensional fidelity of the design ground rule with high manufacturing yield. The higher aspect ratio wiring geometry gives rise to a higher intralevel capacitance and, hence, will affect the device load impedance. This work, however, is concerned only with the process improvements, which make Al RIE extendable to smaller feature sizes. In this article, we report on three aluminum RIE processes that can be applied to a 150 nm or smaller ground-rule technology. The three approaches vary in complexity: (1) Conventional organic antireflective coating (ARC) with a photoresist etch mask, (2) inorganic

silicon oxynitride dielectric ARC (DARC) with a photoresist etch mask, and (3) a physical vapor deposition (PVD) tungsten cap layer used as a hardmask. Various parameters that affect the RIE process will be presented.

II. EXPERIMENT

The work reported here was done in a state-of-the-art class 1 clean room environment equipped with a 200 mm manufacturing tool set. Metal deposition was done in an Endura 5500 clustered PVD tool.⁴ Lithography was done on a 248 nm wavelength 0.68 numerical aperture stepper with integrated track. An attenuated phase shift mask was used in this work.

The designed aspect ratio of the wire for a 175 nm technology is 2.5, with a worst case of approximately 3.2. For 150 nm lines, the aspect ratio required to meet resistance design requirements is substantially higher. For the two processes that use photoresist as the etch mask, the main task of the RIE process is to minimize the consumption of the resist during etch.²

Metal deposition of Ti/TiN/Al (0.5 wt % Cu) Ti/TiN stack was carried out in an Applied Materials Endura 5500 system. The PVD conditions are fairly conventional. The total metal stack thickness for this work is 435 nm. After metal deposition, the wafers are coated with 60 nm deep ultraviolet (UV) antireflection coating, followed by photoresist spin coating at a given thickness. The lithographic process consists of 140 °C bake and exposure on a deep UV (DUV) stepper using attenuated phase shift mask. The patterned wafers are then brought into the metal etch chamber.

Of the three processes evaluated, the first two etch processes utilizing a photoresist etch mask restrict the metal stack height to that determined by the etch selectivity of metal to resist, with the maximum resist thickness being determined by the lithography process tolerance for a 150 nm target resolution. The total remaining resist and ARC thickness is to be greater than 150 nm after metal etch to avoid an irregular side wall profile. The metal etch utilized a LAM

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TABLE I. Few process conditions for 60 nm ARC open.

Pressure (mT)	200 ^a	30	30	30	30
radio frequency (rf) TC power (W)	200	200	400	400	200
rf bias power (W)		175	175	175	175
Ar flow rate (sccm)	300	100			95
N ₂ flow rate (sccm)			50	50	
O ₂ flow rate (sccm)	50	6	3		6.5
Cl ₂ flow rate (sccm)					5
Etch time (s)	18	20	40	65	45
Etch selectivity to resist	1	0.8	0.65	0.52	0.33

^aThis column shows data taken from *ex situ* chamber.

TCP 9600SE low pressure, high density plasma RIE tool using Cl₂, BCl₃, and N₂ based chemistry. The chamber pressure was kept at 30 and 10 mTorr for ARC open and metal etch, respectively. The etch sequence starts with an ARC, DARC, or W hard mask open etch step, followed by a Cl₂/BCl₃ based Al stack etch. An overetch is performed after a triggered end point to remove the metal stringers at the bottom of the space. Subsequent processing includes a downstream H₂O oxygen plasma ash, followed by a water rinse. The wafers are then wet cleaned to further remove residual polymers formed during the metal etch step.

We have found that the etch selectivity is becoming more sensitive to the pattern factor (percentage of metal that is masked) as the ground rule shrinks and the aspect ratio of the structures increases. The etch selectivity can change by a factor of 3 as the pattern factor varies from 20% to 50%.² In this work all the data presented are taken from wafers that have approximately 50% pattern factor.

Electrical tests were carried out on designed structures. The line-to-line short test was made on a pair of parallel lines with line/space at 175/175 and 150/150 nm, respectively. The total length of each line is greater than 10 m. The output of the measurement is the current value between the two lines under a certain applied voltage. The sheet resistance is measured on a single line with given linewidth. The output value is the electric current that passes through the line at the applied voltage, and the resistance value is then calculated using Ohm's law and normalized to a given linewidth.

III. RESULTS AND DISCUSSION

A. Pre-Al metal stack etch

1. Organic ARC open

Since printing the smaller features requires thinner resist in order to have better resolution and reduce the chances of resist pattern collapsing, the metal etch should be optimized to have highest selectivity to resist possible, i.e., to consume the least amount of photoresist. We have found that the Ar/O₂ based ARC open process on this plasma RIE system has the lowest etch selectivity (etch rate of film/etch rate of resist mask) among all etching steps, i.e., this step consumes more resist per unit stack thickness. The optimized ARC open selectivity with respect to resist is approximately 0.8, which compares to metal etch selectivity of about 1.

The ARC open etch selectivity to resist can be distinctly improved if the ARC open is carried out "*ex situ*" with an alternative process. For example, by using an alternate oxide etch chamber with the same chemistry but in higher flow and pressure regime, or by employing a different chemistry, such as a CO/O₂/CF₄/Ar/CHF₃/N₂ mixture. In terms of process cost, complexity and process yield, it is desirable to perform the ARC open and the metal etch in the same chamber. With the RIE etch chamber, the ARC open selectivity varies from 0.3 to 0.8, depending on the process gas selection. Table I lists a few processes that can be used for the ARC open. The ARC open etch selectivity to resist varies noticeably as process conditions change.

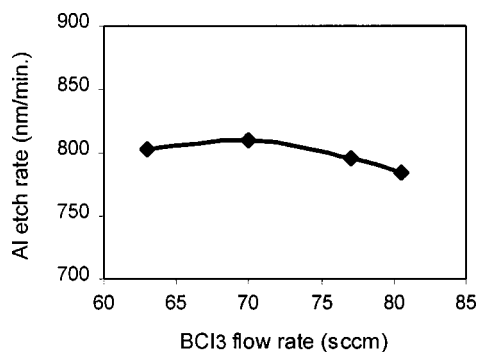
The electrical test results show that there is no line-to-line yield impact from the ARC open step, as long as the ARC open time exceeds 3 s after the ARC end point signal is triggered.

2. Dielectric ARC open

A 20 nm silicon oxynitride (SiO_xN_y) DARC film was deposited on the top TiN surface of the metal stack. After the lithographic patterning, the DARC was etched in a separate RIE chamber using CF₄ based chemistry, since the metal etch chamber used for this work has no CF₄ supply. The DARC etch selectivity to resist is approximately 0.4. One difference of using DARC (as opposed to ARC) is that the antireflective film is thinner and, hence, consumes less resist during the ARC open etch. An advantage of using DARC is the improved lithographic imaging, particularly on surfaces with topography. After DARC open, the wafers are etched in the metal etcher. The etch mask in this scheme is still the DUV photoresist, and the 20 nm DARC film has no noticeable effect on metal etch. The DARC film is left on top of the metal stack after resist strip and wet clean.

3. Tungsten hard mask open

A 50 nm PVD tungsten cap layer was deposited on the surface of the metal stack. Owing to the high etch selectivity of aluminum and TiN with respect to tungsten, this layer is designed to function as a hard mask.⁵ The W layer is opened after photolithography in an *ex situ* RIE chamber using SF₆ based chemistry. Other chemistries, such as Cl₂ and BCl₃, may be used to etch the thin W layer, although the etch selectivity to resist is lower. Since the W etch selectivity

FIG. 1. Patterned Al etch rate as a function of BCl₃ flow rate.

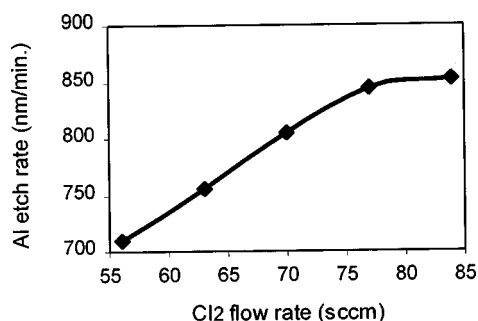
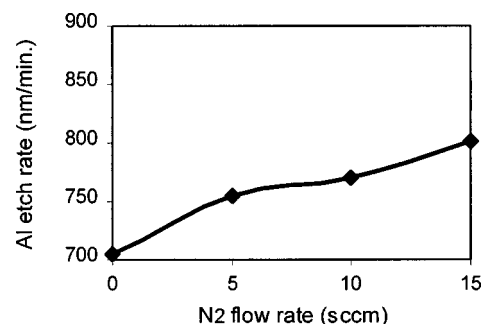
with respect to resist is high, the 50 nm W hard-mask open consumes only a small amount (<150 nm) of resist. After hard-mask open the remaining resist is stripped and the wafer is etched in absence of any organic materials on the wafer.

The advantage of this scheme is that the photoresist thickness can be significantly reduced, thereby increasing the lithography process window. Another advantage is that the metal etch is carried out without the presence of organic materials. Thus, sidewall polymers, which are often a corrosion problem because of the trapped chlorides, are of less concern in this case. In addition, the requirement on the post-metal etch wet clean is not as stringent since much less sidewall polymers are formed as compared to the resist mask situation and they are also easier to remove.

B. Al metal stack etch

1. Metal etch on small ground rules

Aluminum based metal RIE has been well developed for many years. However, there has been no literature found that indicates the application of Al RIE to 175 and 150 nm ground rules with relatively thick metal stack. In this work it is demonstrated that <100 nm space structures can be etched on 300 nm pitch hardware with the aspect ratio of the space being approximately 5. Due to current limitations in DUV lithography, pitches smaller than 300 nm have yet to be printed. However, we believe that the metal etch process can be extended to even smaller structures without any major tool set change.

FIG. 2. Patterned Al etch rate as a function of Cl₂ flow rate.FIG. 3. Patterned Al etch rate as a function of N₂ flow rate.

2. Al stack etching chemistry

The two active constituents used in the aluminum stack etch are Cl₂ and BCl₃. The metal etch and overetch can be done with the same gas flow ratio, or a higher Cl₂/BCl₃ ratio can be used for the overetch. The metal etch selectivity with respect to resist varies quite noticeably with the Cl₂/BCl₃ ratio. For arrays with equal line/space width at 350 and 300 nm pitch, the overall metal etch selectivity with respect to resist is approximately 1, whereby the Ti/TiN etch rate is around three times lower than that of the aluminum.

Although the higher flow ratio of Cl₂/BCl₃ (with upper limit of 5:1) gives better etch selectivity, this also results in a higher concentration of chlorine contained in the sidewall polymer. This effect is undesirable because of the catalytic effect of chlorine on aluminum corrosion in the presence of moisture. Even though the wafer is processed by the downstream plasma resist strip and water rinse without breaking of vacuum following the metal etch, the small amount of residual polymers is still capable of gathering the moisture in the air, which in turn attacks Al lines. Therefore, the wet clean is required to remove all the residual polymeric materials soon after the wafer is out of the metal etcher.

Aluminum etch rate as a function of gases flow has been studied. The referred etch rate here is the thickness of aluminum removed per minute in a patterned wafer. We have found that the etch rate has little dependence on BCl₃ flow as shown in Fig. 1. This is in agreement with the reported result that the rate-limiting factor is the gas phase dissociation of BCl₃.⁶ The Cl₂ flow, however, has a much larger effect on the aluminum etch rate, primarily due to the fact that the Cl₂ etches aluminum spontaneously and does not require plasma for the generation of the etching species. As the Cl₂ flow gets higher, the chlorine adsorption on aluminum is limited which results in the saturation of the etch rate (Fig. 2). Figure 3 shows the influence of N₂ flow rate on the aluminum etch rate. The enhanced aluminum etch rate with increasing N₂ flow is probably due to the increasingly more anisotropic nature of the RIE in presence of N₂.

A typical postetch cross-sectional scanning electron microscopy (SEM) of 150 nm Al lines using photoresist as etch mask is shown in Fig. 4. The thickness of remaining resist and ARC after metal etch is about 170 nm [Fig. 4(a)]. After resist strip and wet clean, the metal line cross sections are in rectangular shape with no apparent upper corner erosion, as

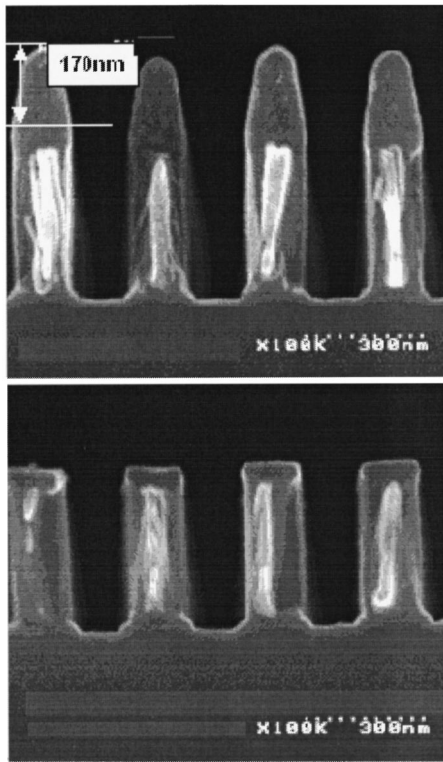


FIG. 4. Cross-section SEM micrographs of 300 nm pitched aluminum lines etched using resist/ARC as mask. (a) After RIE without resist strip and (b) after resist strip and wet clean.

can be seen in Fig. 4(b). The width of the Ti/TiN barrier and cap layer is larger than that of the Al, due to the etch rate difference between Al and Ti/TiN. Figure 5 shows a SEM micrograph of an etched feature of 85 nm width, with a metal stack height of 435 nm, and pitch of 300 nm, indicating the potential to extend the RIE process to smaller feature sizes.

Cross-section SEM of 150 nm lines using photoresist and DARC as etch mask is shown in Fig. 6. The thickness of remaining resist is slightly larger than that of the ARC [see Figs. 4(a) and 6(a)], due to the reduced resist consumption in the DARC open process. The metal profile is not much different from that processed using organic ARC. The remain-

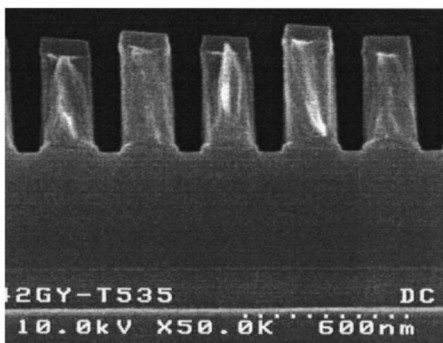


FIG. 5. Cross-section SEM of a structure with printed narrow space at 300 nm pitch. The space is approximately 80 nm.

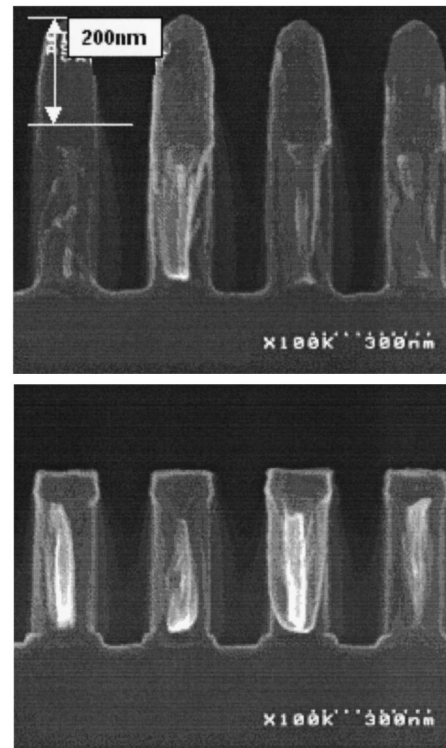


FIG. 6. Cross-section SEM micrographs of 300 nm pitched aluminum lines etched using resist/DARC as mask. (a) After RIE without resist strip and (b) after resist strip and wet clean.

ing 20 nm DARC on top of metal stack has no noticeable effect on the reliability performance of the Al wires.

The etch profile after 50 nm PVD W hard-mask open can be seen in Fig. 7. It is apparent from Fig. 7(a) that much more resist remains after W hard-mask open as compared to Fig. 4(a). The thickness of remaining resist including ARC exceeds 450 nm. The resist is subsequently stripped and the aluminum stack is etched. A cross section of 175 nm Al line/space profile produced with the W hard-mask process is shown in Fig. 7(b). Even after exposing the wafer without postetch wet clean for 2 weeks to the ambient atmosphere, no indication for Al corrosion could be detected, indicating the substantial reduction of sidewall polymer with the hard-mask process. This is particularly important, since the postetch wet clean can be critical to the reliability performance of the wire.

3. Influence of electrostatic chuck temperature

It has been reported that the aluminum etch rate increases as temperature inner diameter raised.⁶ In the system that is used in this work, the electrostatic chuck (e-chuck) temperature (controlled by a water chiller) may drift up to 4° around the set point. The effect of e-chuck temperature on sidewall profile and electrical shorts yield was studied and the results show that the metal line profile is extremely sensitive to the e-chuck temperature, which in turn has a major effect on line-to-line electrical shorts yield. This effect is especially

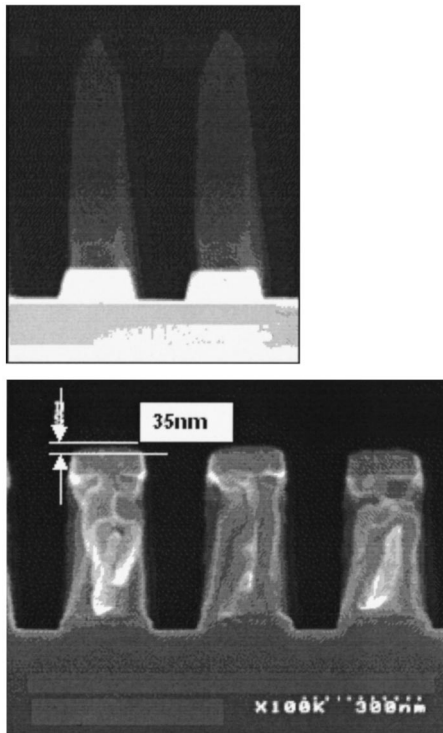


FIG. 7. Cross-section SEM micrographs of 350 nm pitched aluminum lines etched using 50 nm PVD W as mask. (a) After W mask open without resist strip and (b) after metal etch with no wet clean performed.

significant at smaller line/paces and high aspect ratio structures. On the other hand, metal etch selectivity to resist is not a strong function of e-chuck temperature.

For 175 nm line/175 nm space structures etched at varying chuck temperatures in the range of 20–40 °C, the metal wire sidewall profile angle gradually changed from 85° to 95°, i.e., from a slightly tapered to a slightly retrograde. The change in line profile is clearly shown in the cross-section micrographs of Fig. 8. A quantified plot of line width versus e-chuck temperature is shown in Fig. 9. We have found that the trend of line shape change versus e-chuck temperature is the same for samples taken from the wafer center and from the wafer edge. The metal lines in the sample have a total metal height of 435 nm and a pitch of 350 nm. These line shape results are consistent with the line to line electrical short data. The line-to-line electrical shorts yield varied from ~20% to >90% as the e-chuck temperature increased. This is in good agreement with the cross-section SEM results, since the main cause of the line-to-line short is the presence of residual barrier metals at the bottom. A larger space at the bottom would reduce the chances for shorting. The sheet resistance of 175 nm line also increased linearly as the e-chuck temperature increased due to the decrease of the cross-section area of the metal lines.

The increase of space width at the bottom portion of the aluminum lines with raising temperature is presumably due to less polymeric protection during the etch. It has been reported that the line width is strongly dependent on the sticking coefficient of reincident photoresist reaction byproducts

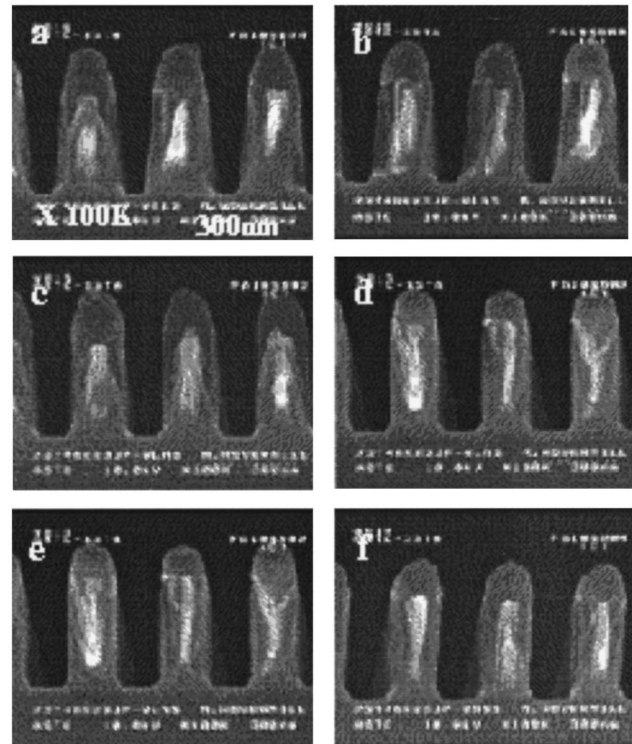


FIG. 8. Cross-section SEM micrographs of 350 nm pitched aluminum lines etched at different e-chuck temperatures. (a) 20; (b) 24; (c) 28.5; (d) 34; (e) 38.5; and (f) 40 °C.

which protect the sidewall of lines from attack.^{7,8} The value of this coefficient is strongly dependent on temperature. In addition, the higher temperature accelerates the spontaneous reaction of Cl_2 aluminum. However, the temperature variation has little impact on the ion-assisted chemistry (BCl_3). Hence, the line profiles can be adjusted by affecting polymer deposition/etching balance as temperature changes.

C. Post end-point aluminum overetch

Post end-point aluminum overetch is performed in the same chamber used for the metal etch, directly after the end point of the bulk aluminum stack. The metal etch and overetch can be done with the same gas flow ratio, or a higher Cl_2/BCl_3 ratio can be used for the overetch. The ideal overetch time should be kept as short as possible in order to

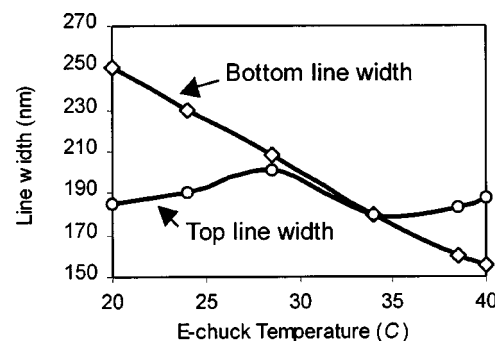


FIG. 9. Etched Al line width as a function of electrostatic chuck temperature of the chamber.

reduce photoresist consumption, while still maintaining good electrical shorts yield. Due to the etch rate differential, at normal etch conditions the largest width of Al line cross section always at the bottom Ti/TiN. The electrical shorts between lines predominantly takes place at this narrow space between the bottom Ti/TiN. The overetch process should remove between 10 and 15 nm of underlying oxide to ensure a good line-to-line shorts yield.

Tests result do not indicate any degradation of electromigration resistance as metal line width shrinks from a few micrometers to 175 nm.⁹ Separate test results confirmed that the electromigration performance for 150 nm lines scales with those at larger ground rules.

IV. CONCLUSIONS

Three different manufacturable aluminum etch processes have been developed for 175/175 and 150/150 nm line/space structures. It has been shown that the RIE process can clear a sub-100 nm space for metal stacks having a height of 435 nm. This indicates that aluminum RIE can be extended for even smaller structures without require a new generation of the tool set. In the schemes that use photoresist as etch mask, the thickness of the total metal stack is limited by the thickness of the photoresist. In the scheme that uses a PVD W hard mask, the total metal thickness is not a limiting factor for metal etch. The electrostatic chuck temperature plays a major role influencing metal profile and shorts yield. Reliability results of line/space type Al RIE lines with smaller ground rules scale with data from previous technologies at larger ground rules. Electrical test results also show that with

proper process optimizations the yield of the smaller Al lines can be manufactured at the same level as previously device generations with larger ground rules. An optimized RIE process for a particular technology depends on various factors, such as cost, manufacturing strategy, process commonality, final yield, and reliability performance.

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¹J. G. Ryan *et al.*, IBM J. Res. Dev. **39**, 371 (1995).

²X. J. Ning *et al.*, Proceedings of 16th VLSI Multilevel Interconnection Conference, Santa Clara, 1999, p. 47.

³R. Ravikumar *et al.*, International Interconnect Technology Conference, IEEE Electron Device Society, San Francisco, 1999, p. 203.

⁴S. Weber *et al.*, in Proceedings of ULSI Adv. Metallization Conference, 1998.

⁵S. Athavale, G. Stojakovic, M. Gutsche, and X. J. Ning, Proceedings of the 196th Meeting of the Electrochemical Society, Honolulu, Hawaii, 1999, p. 705.

⁶D. A. Danner and D. W. Hess, J. Electrochem. Soc. **133**, 151 (1986).

⁷J. Jacobs, K. Saito, and J. Yamamoto, Jpn. J. Appl. Phys., Part 1 **37**, 2359 (1998).

⁸M. Izawa, S. Tachi, R. Hamasaki, and M. Kojima, Proc. of Dry Process Symp., Tokyo, 1997, p. 45.

⁹R. G. Filippi *et al.*, J. Appl. Phys. (submitted).