

A Low Voltage SONOS Nonvolatile Semiconductor Memory Technology

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Abstract—The triple-dielectric polysilicon-blocking oxide-silicon nitride-tunnel oxide-silicon (SONOS) structure is an attractive candidate for high density E²PROM's suitable for semiconductor disks and as a replacement for high-density dynamic random access memories (DRAM's). Low programming voltages (5 V) and high endurance (greater than 10⁷ cycles) are possible in this multielectric technology as the intermediate Si₃N₄ layer is scaled to thicknesses of 50 Å. The thin gate insulator and low programming voltage enable the scaling of the basic memory cell and associated complementary metal-oxide-semiconductor (CMOS) peripheral circuitry on the memory chip. A SONOS 1TC memory cell is proposed in a NOR architecture with a cell area of 6F², where F is the technology feature size. A 0.20 μm feature size permits a 1TC area of 0.24 μm² for advanced 1-Gb nonvolatile semiconductor memory chips. A physical model is presented to characterize the erase/write, retention and endurance properties of the nonvolatile semiconductor memory (NVSM) SONOS device.

Index Terms—EEPROM, nonvolatile semiconductor memory, SONOS.

I. INTRODUCTION

IN THE electrically erasable programmable read only memory (EEPROM) semiconductor device area there have been essentially two technologies which compete for an ever-expanding world market:

- 1) floating gate EEPROM's;
- 2) polysilicon-blocking oxide-silicon nitride-tunnel oxide-silicon (SONOS) [historically metal-nitride-oxide-semiconductor (MNOS)] or floating-trap EEPROM's.

More recently, there has been renewed interest in ferroelectric EEPROM's [1]; however, there are material technology problems which must be addressed to bring this promising technology to a competitive level with the other two technologies. In this paper we will concentrate on the SONOS technology as it is compatible with mainstream complementary metal-oxide-semiconductor (CMOS) technology and offers advantages in low voltage programming for scaled, high-density nonvolatile semiconductor memory (NVSM) memories. The applications

for low voltage EEPROM's are television tuners, postage meters, automobiles, neural networks, solid-state disks, electronic video and sound storage, and so-called *smart* cards. More recently [2], [3] dynamic random access memories (DRAM) replacement has been discussed as SONOS cell areas of 6F² are possible with a simplified process technology, which reduces step-coverage problems and relaxes lithography requirements. In this instance, long-term retention is not as important as in EEPROM and NVRAM applications.

In the early period of EEPROM development, the MNOS and SONOS technologies were not viewed as "mainstream" and criticism was levied by the technical community at the need to control the ultra-thin oxides employed in these technologies. However, with the use and familiarity of nitride films in localized oxidation of silicon (LOCOS), interpolydielectrics in polysilicon FLASH EEPROM's, and SiN cap passivation combined with thin CMOS gate oxides of 3–4 nm for 100–200 nm channel lengths, the SONOS low-voltage technology becomes an attractive alternative to "floating gate" EEPROM's. In addition, the scaling of peripheral CMOS circuitry necessitates strong consideration for reducing the "on-chip" programming and erase voltages, which are currently generated by *charge pump* [4] circuit techniques. The desirable features for EEPROM's are low cost (small cell size and simple fabrication process), low programming voltage, fast erase/write times, good retention, high endurance and, in some instances, a wide operating temperature range with radiation hardness.

II. PHYSICAL ELECTRONICS OF SONOS DEVICES

MNOS memories were invented nearly 30 years ago [5] and were the first electrically-alterable nonvolatile semiconductor memory (EAROM) device. In the early 70's, *p*-channel MNOS EAROM's were fabricated with densities of 8 Kb in a tri-gate implementation. These arrays employed a so-called *drain-source protected* (DSP) transistor cell [6] in an early form of the *flash* EEPROM architecture. Early EAROM memories used an aluminum gate technology (see Fig. 1) and required a TTL 5 V and several high voltage (25–30 V) power supplies. The speed limitation of an all *p*-channel approach combined with the lack of polysilicon gates and LOCOS isolation technologies restricted the penetration of EEPROM's into the commercial marketplace.

The limitations in scaling the programming voltages of the standard dual dielectric MNOS device were attributed to the finite charge distribution of several 10's of nanometers

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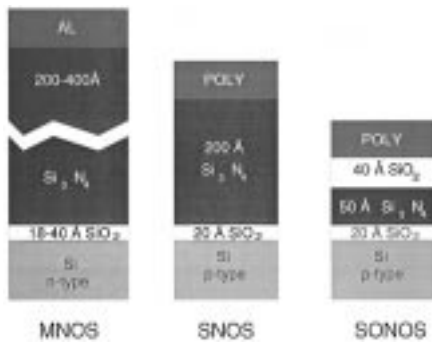


Fig. 1. Evolution of MNOS technology.

within the nitride layer such that the latter could not be reduced indefinitely. The triple-dielectric MONOS structure was introduced in 1968 [7]. The advantages of the triple-dielectric SONOS structure [8], [9] were used to reduce instabilities associated with the polysilicon gate-nitride interface where the blocking oxide minimized charge injection from the gate electrode. In the ensuing years, a polysilicon gate technology [10] combined with the use of low pressure chemical vapor deposition (LPCVD) silicon nitride technology for uniform control of the nitride thickness provided 16-Kb SNOS EEPROM's.

The reliability of the polysilicon gate combined with a pre-metallization, high-temperature hydrogen anneal have been important factors in the development of this multielectric nonvolatile technology. The control of the nitride thickness was long realized to be a major limitation in the performance of MNOS memory arrays [11] as electric field strengths in the silicon nitride were required to be below 5.5 MV/cm. to extend the endurance to erase/write cycling beyond 10^7 cycles. In addition, the control over the ultra-thin tunnel oxide (UTO) (thicknesses of 1.5–2.5 nm) has been a major factor in attracting commercial silicon device manufacturers [12] to adopt the multielectric NVSM technology. Fig. 2 illustrates the early MNOS device cross section and the more recent scaled SONOS device cross section.

The advantages of the triple dielectric structure are:

- 1) lower programming voltages since the blocking action of the top oxide removes any limitation on the reduction of the nitride thickness;
- 2) charge injection from and to the gate electrode is minimized for both gate polarities, particularly for hole injection;
- 3) improved memory retention since there is minimal loss of charge to the gate electrode;
- 4) increased endurance to extended erase/write cycling.

III. CHARGE TRANSPORT AND STORAGE IN SONOS MEMORY DEVICES

The analysis of the *erase/write* charge transport and storage in SONOS devices is presented in this section for a *n*-channel SONOS transistor with a negative gate potential (*erase*) and a positive gate potential (*write*). The latter is the program mode since this operation requires a channel to be formed for tunneling of carriers through the ultra-thin, tunnel oxide. The

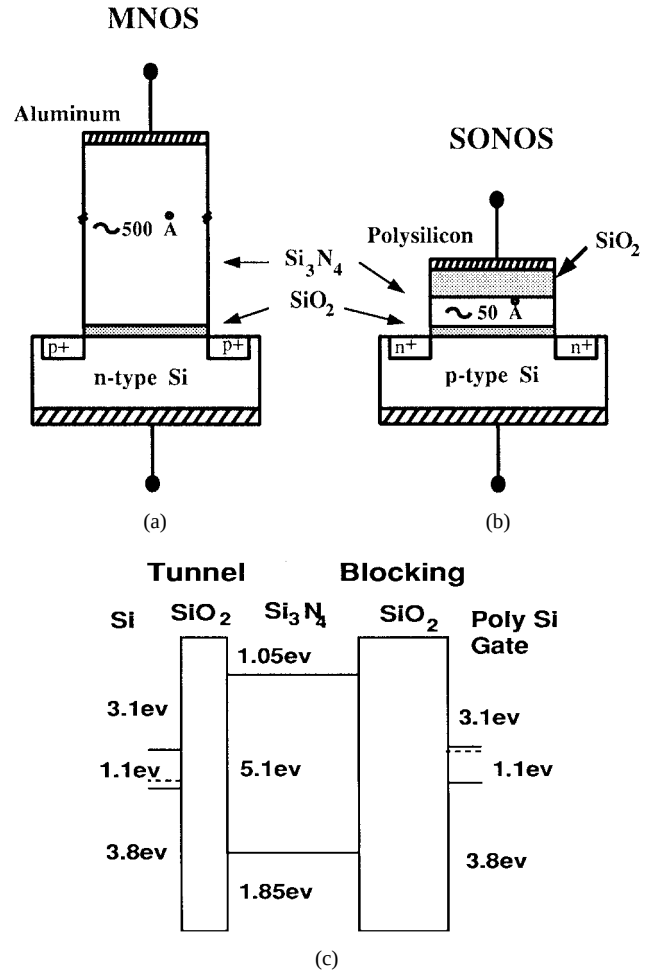


Fig. 2. (a) The conventional MNOS, (b) the scaled down SONOS, and (c) SONOS ideal energy band diagram.

programming of a cell may be “inhibited” or “unselected” by raising the source terminal to the programming voltage. The *n*-channel SONOS can be integrated into a *p*-well, single voltage supply, CMOS process [13]. A *p*-channel SONOS device has been integrated into an *n*-well, single power supply (+10 V), CMOS process for advanced electronic memory systems [14] and application specific integrated circuits (ASIC's). A *n*-channel SONOS device has been integrated into a *p*-well, dual voltage supply (−4 V, +5 V), CMOS process for 1-Mb EEPROM's with application for semiconductor disks [15]. In this paper, we present a scaled *n*-channel SONOS device in the form of a one transistor cell (1TC) as shown in Fig. 3. The cell may be used in a dual string NOR (DuSNOR) architecture [16] which has a smaller reported cell area than the NAND flash design.

Fig. 4 illustrates an operational table for the SONOS 1TC configured in a *p*-well with appropriate use of a single programming voltage, V_P , a read voltage, V_R , and ground. If *n*-channel operation is required with a *p*-type starting substrate, then negative charge pumps are needed to supply the *erase* voltage. These voltages are applied to the device terminals for the various operational modes of READ, WRITE, and ERASE. In the ERASE mode, it is important to remember the SONOS device must be *erased* over the entire length of

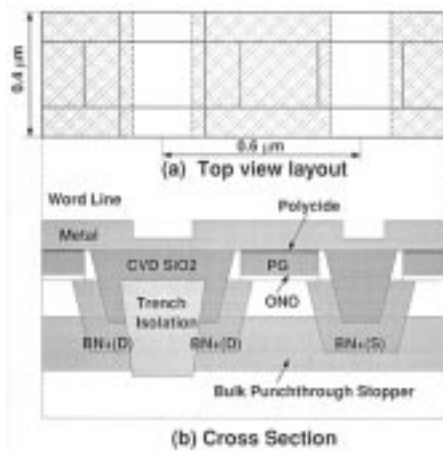


Fig. 3. Scaled SONOS 1TC with $0.20\ \mu\text{m}$ feature size and cell area of $0.24\ \mu\text{m}^2$ for advanced 1-Gb nonvolatile semiconductor memory.

the channel. Thus, the gate is grounded and the remaining terminals have V_P applied. In the WRITE mode, the gate is connected to the programming voltage V_P , the selected Bit Line is grounded and the drain is floated. If current drain from the V_P supply can be tolerated, the drain terminal can be raised to V_P during writing. The WRITE operation is inhibited by floating or supplying V_P to the drain and raising the source of the unselected Bit Line to V_P . In the READ mode, V_R is applied to the gate, V_P is applied to the drain, and the source is grounded. The READ voltage V_R tends to write the erased device and the duration of V_R needs to be carefully chosen to minimize this disturbance.

A. Programming Mechanisms

There have been conflicting methods of describing the *erase* and *write* states for a SONOS device. For a number of years, the *erase* state referred to the state of highest conduction, while the *write* state denoted the state of lowest conduction for a specified read voltage. However, more recently, this method has been replaced by the concept of *reset* and *program*, where *erase* and *write* designations are used in an interchangeable manner. In general, for *flash* the reset operation is performed for all the memory cells on the chip over a long period of time, historically referred to as *block erase* in *block oriented random access memories* or BORAM. The *program* operation is generally of shorter duration. These shorter programming pulses, in the case of *n*-channel SONOS devices, are the positive applied voltages on the gate relative to the substrate, while the longer pulses perform the *erase* or *clear* function. Fig. 5 illustrates the *erase* tunneling current components for a *n*-channel SONOS device. For a large negative gate *erase* voltage, band to band *direct* tunneling (J_{OTp}) will occur where holes leave the silicon valence band and tunnel in a “direct” manner to the valence band of the silicon nitride. If the voltage levels are reduced, then the holes will not tunnel “directly” into the valence band of the silicon nitride, but rather through a second “trapezoidal” barrier into the nitride valence band. This process is referred to as *modified Fowler Nordheim* tunneling [17] and the holes thereby enter the nitride valence band at a distance further from the tunnel oxide-nitride interface.

Operational modes	Drain	Gate	Source	Bulk
Erase	V_P	0	V_P	V_P
Write	float*	V_P	0	0
Inhibit	float*	V_P	V_P	0
Read	V_P	V_R	0	0

Fig. 4. The terminal voltages applied to the scaled *n*-channel SONOS memory device during the various programming modes. The gate is treated as a word line and the source as the bit line. The WRITE operation is inhibited by floating the drain and raising the source of the unselected Bit Line to V_P . If current drain from the V_P supply can be tolerated, the shared drain terminal can be raised to V_P during writing*.

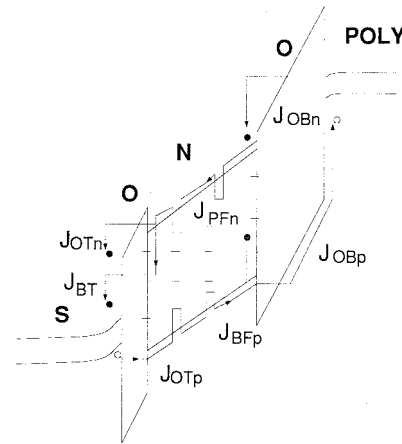


Fig. 5. Erase operation for a scaled *n*-channel SONOS device.

In addition, some electrons may back-tunnel (J_{BT}) from the traps in the nitride to the semiconductor conduction band. At even lower voltage levels, charge transport occurs through a trap-assisted tunneling mechanism [2].

Injected holes may be captured by traps and/or enter the nitride valence band where they will either 1) be captured by deep-level, local traps, or 2) drift to the nitride-blocking oxide interface due to the scaled-down nitride dimensions ($\leq 200\ \text{\AA}$) and the nitride field (3–6 MV/cm). The combination of the scaled nitride thickness and the 1.85 eV energy barrier height will cause some holes to accumulate at the nitride-blocking oxide interface. As the hole charge begins to accumulate in the silicon nitride, the electric field across the tunnel oxide will decrease with a concomitant decrease in the hole tunnel current, J_{OTp} . Concurrently, the blocking oxide field will increase with the possibility of hole tunneling current, J_{OBp} , to the gate electrode and a band-to-band electron tunneling current, J_{OBn} , from the N^+ polysilicon gate electrode to the conduction band of the silicon nitride. This process will start out as a small contribution to the stored charge in the silicon nitride. But as time increases, this component becomes a limitation to the maximum shift in the device threshold voltage. The gate injection may be minimized with a P^+ polysilicon gate process to reduce the supply of electrons.

At high injection levels, the electron back-tunneling current, J_{OTn} , will be small compared to the hole forward-tunnel current, J_{OTp} , and trap-assisted tunneling [18] is less favorable at the high electric fields in Fig 5. In a practical *write* or *erase* operation, the tunnel oxide fields decrease from an initial value

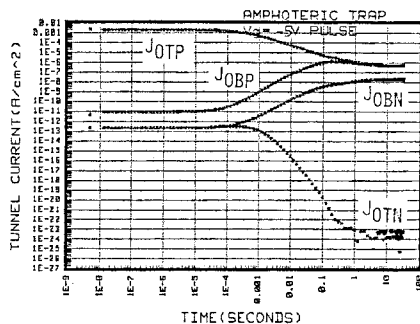


Fig. 6. Simulated currents in the erase operation for a n -channel SONOS device with $X_{OT} = 20$ Å, $X_N = 50$ Å, $X_{OB} = 35$ Å and an applied gate voltage, $V_G = -5$ V.

of ≈ 10 MV/cm to a final sustaining value of ≈ 6 MV/cm. In ultra-thin tunnel oxides (i.e., less than 20 Å), hole transport by *modified Fowler-Nordheim* tunneling to the nitride will be the dominant injection mechanism under negative gate bias. In general, the nitride traps can be *saturated* with holes for long erase times, in excess of 100 ms, in ultra-thin nitride (≤ 50 Å) which leads to a saturation in the threshold voltage of the device, whereas in thicker nitride, the threshold voltage is likely to saturate due to the balance of electron and hole currents ($J_{OTp} = J_{OBn}$). In ultra-thin nitride, trap saturation occurs before the electric field increases to a point in the blocking oxide so as to permit substantial gate current to be injected into the nitride.

B. Scaled SONOS Devices

Fig. 6 shows the simulation of the current density components associated with the *erase* operation for a scaled n -channel SONOS device. This simulation does not consider trap-assisted tunneling which can provide a significant contribution to the threshold voltage shift when the tunnel oxide electric field falls below ≈ 6 MV/cm [2]. In the *erase* mode, there will be very few electrons in the nitride conduction band since they will either be captured by the deep-level nitride traps or exit through the tunnel oxide as shown in Fig. 5.

A reduction in the ultra-thin tunnel oxide thickness has a major effect on the erase speed of a n -channel SONOS device and the write speed of a p -channel SONOS device. Under these conditions, a net positive charge will accumulate in the nitride which shifts the n -channel SONOS threshold voltage in a negative direction. Fig. 7 illustrates the effect of tunnel oxide thickness reduction on the *erase-write* characteristics of a scaled n -channel SONOS device. In this instance the tunnel oxide was scaled from 20 Å to 18 Å with little improvement in the 100 μ s write speed of the device. However, the erase speed of the device has been improved by an order of magnitude from 10 ms to 1 ms to achieve the same memory window of approximately 2.5 V. A positive gate bias will cause electron transport to occur by *modified Fowler-Nordheim* tunneling from the silicon conduction band to the nitride conduction band. A reduction in the ultra-thin tunnel oxide thickness has a relatively minor effect on the write speed of a n -channel device and the erase speed of its p -channel counterpart. The reason for this aspect of device operation is a consequence of the

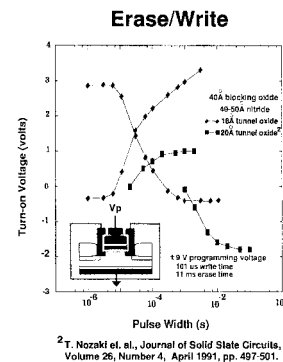


Fig. 7. Experimental erase-write characteristics for a scaled n -channel SONOS device to illustrate the effect of tunnel oxide variation [21]. The SONOS device has a $X_{OT} = 20$ Å, $X_N = 50$ Å, $X_{OB} = 35$ Å and an applied gate voltage, $V_G = \pm 9$ V. The initial conditions were set with $V_G = \pm 9$ V for 10 s to reach saturation.

ERASE/WRITE Measurement

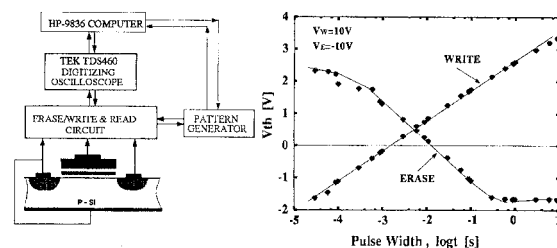


Fig. 8. Erase-write measurements on the SONOS device of Fig. 7. The SONOS device has dielectric thicknesses of $X_{OT} = 20$ Å, $X_N = 50$ Å, $X_{OB} = 35$ Å with programming voltages of $V_G = \pm 10$ V.

initial electric fields electron and hole injection. Consequently, in the case of electron injection, where reduced electric fields are electric fields involved, carrier transport is by *modified Fowler-Nordheim* tunneling which is relatively insensitive to variations in tunnel oxide thickness because electrons must travel through a portion of the silicon nitride in addition to the tunnel oxide. In the case of hole injection, we have *direct* tunneling, which is very sensitive to tunnel oxide thickness variations.

Fig. 8 illustrates erase/write measurements on the scaled SONOS device of Fig. 7 while the retention characteristics of a similar device is shown in Fig. 9 [20]. The *erase-write* characteristics of a scaled version of a n -channel SONOS device, suitable for high-density NVSM arrays, are shown in Fig. 10. The *erase* and *program* voltages are -5 , 1 ms and $+5$, 1 ms, respectively. The initial state is set with a sequence of 10 alternating *erase/write* pulses to represent successive cycle times. The read operations begin with a 1 μ s pulse, which slightly alters the initial state of the device. The SONOS 1TC requires enhancement mode threshold voltages for both the erase and write states of the device to ensure that nonselected devices do not contribute sense current to the bit line upon addressing the selected word line. Fig. 10 illustrates the possibility of obtaining threshold voltages of $V_{T1}(\text{Write}) = 0.65$ V and $V_{T0}(\text{Erase}) = 0.05$ V for a 1 ms *erase/write* programming sequence. The triple ONO dielectric

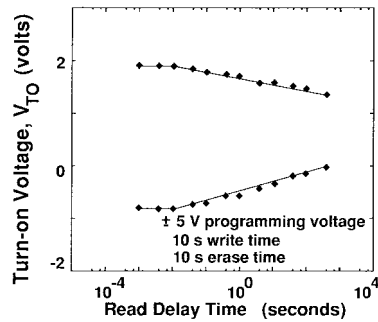


Fig. 9. Retention measurement [20] of SONOS device with dielectric thickness of $X_{OT} = 18$ Å, $X_N = 50$ Å, $X_{OB} = 40$ Å given a programming voltage of $V_G = \pm 5$ V and a 10-s erase and write time.

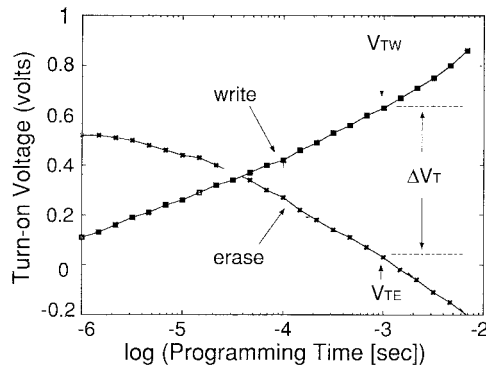


Fig. 10. Erase-write measurements of scaled SONOS device with 5 V erase/program. The initial conditions were set with ± 5 V, 1 ms erase/write pulses. The ONO dielectric for the scaled devices have thicknesses of $X_{OT} = 8$ Å, $X_N = 70$ Å, $X_{OB} = 45$ Å.

for these scaled devices has thicknesses of $X_{OT} = 8$ Å, $X_N = 70$ Å, and $X_{OB} = 45$ Å. This is not an optimum combination at this point in the research, however the results clearly indicate the potential for the scaled SONOS device to operate at ± 5 V at 1 ms program/erase times for high-density NVSM arrays. The data retention measurement of the scaled device at 85 °C is shown in Fig. 11. At the present time these devices can be employed in applications where the long term data retention is not required.

C. Fabrication Considerations

The scaled SONOS devices reported in this paper are fabricated with a modified RCA clean to terminate the surface in protons and prevent the initial growth of oxides prior to the formation of the tunnel oxide in-situ within the LPCVD nitride chamber. The tunnel oxide thickness on these scaled devices is estimated to be in the range of 0.8–1.0 nm. The silicon nitride is 7.0 nm and is formed with a $\text{NH}_3:\text{SiCl}_2\text{H}_2$ ratio of 10:30 sccm at 680 °C, which has been found by AFM measurements to provide the lowest surface roughness. The blocking oxide is 4.5 nm and formed with a N_2O deposited oxide at 650 °C followed by a steam densification at 900 °C for 30 min. Future process variations will consider high-temperature hydrogen anneals [19] to reduce the interface trap density and the near-interface oxide traps (NIOT's) which influence the short term retention or memory properties of the SONOS device.

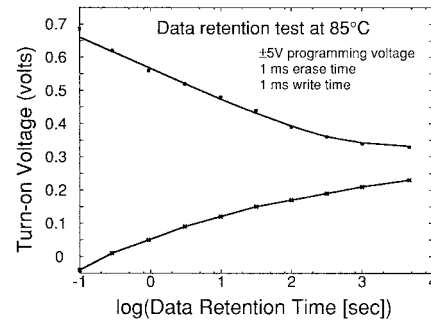


Fig. 11. Data retention measurement at 85 °C with ± 5 V, 1 ms erase/write pulses. The ONO dielectric for the scaled device has thicknesses of $X_{OT} = 8$ Å, $X_N = 70$ Å, $X_{OB} = 45$ Å.

IV. CONCLUSION

The results of these studies on scaled SONOS nonvolatile semiconductor memory devices clearly indicate their potential for a low-voltage, single transistor cell (1TC) in high-density NVSM arrays. The data demonstrate that ± 5 V, 1 ms programming is possible with further improvements expected with continued studies of the processes used to form the ONO sandwich. A 1TC is possible with $6F^2$ (F = feature size) in contrast with present-day $8F^2$ DRAM cells. Thus, with 0.2 μm feature sizes, we expect that a cell area of 0.24 μm^2 should be possible, leading eventually to 1-Gb NVSM arrays and possibly as a substitute for DRAM's. The use of these 1TC SONOS cells in a DuSNOR architecture provides a maximum packing density for SONOS arrays. The design of buried-channel SONOS devices is an option for improved mobility, and thus, higher sense current drive during a READ operation.

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