

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.

Patent Owner.

U.S. Patent No. 9,431,455

DECLARATION OF KONSTANTINOS P. GIAPIS, PH.D

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I. INTRODUCTION

1. I have been retained as an expert witness on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) for the above captioned Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 9,431,455 (the “455 patent”). Ex. 1001.

2. I am being compensated for my time in connection with this IPR at my standard consulting rate of \$700 per hour. My compensation is not affected by the outcome of this matter.

3. I have been asked to provide my opinions regarding whether claims 1–3, 5–12, and 15–19 (the “Challenged Claims”) are invalid as being anticipated by or obvious over the prior art.

4. I am not currently, and have not at any time in the past been, an employee of TSMC. I have no financial interest in TSMC.

II. BACKGROUND AND QUALIFICATIONS

5. I am a professor of chemical engineering at the California Institute of Technology (“Caltech”). I have held that position since 1992.

6. My research relates to processing of semiconductors, dielectrics, and metals, as performed in the fabrication of semiconductor devices, including microprocessors and digital memories. In particular, my work has focused upon patterning layers of electronic materials to fabricate sub-micron features such as

transistor gates, vias, and metal interconnects found in VLSI circuits. I have also conducted modeling and simulations of the evolution of poly-silicon and metal gate profiles subjected to plasma etching and studied their charging interactions with plasmas. Since the start of my graduate career in 1985, I have accumulated over 35 years of experience on semiconductor materials, devices, and their processing.

7. In my professorial duties at Caltech, I have developed and taught new undergraduate and graduate level courses on semiconductor device physics and their processing. These innovative courses combined solid state physics and electronic materials processing technologies with the more traditional chemical engineering subjects of transport phenomena and chemical thermodynamics. The courses have prepared several generations of students for successful careers in the semiconductor industry.

8. During my research career, I have authored or co-authored 98 peer-reviewed papers, 12 refereed conferences proceedings, two book chapters. Most of my publications relate to semiconductor device processing. My papers on charging damage during plasma-processing of high-density integrated devices such as microprocessors, and digital memories are highly cited. This work includes studies of charging effects during the plasma deposition of interlevel dielectrics on patterned metal interconnects. My laboratory has also extensively used and studied plasma-

deposited silicon oxide layers from silane and TEOS precursors. I have also been granted 13 patents.

9. My curriculum vitae is provided as Exhibit 1021 to the petition.

III. MATERIALS REVIEWED AND CONSIDERED

10. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the alleged invention.

11. In forming my opinions, I have reviewed and considered the following documents:

No.	Short Name	Exhibit
1001	'455 patent	U.S. Patent No. 9,431,455
1002	'455 Prosecution History	Prosecution history for U.S. Patent No. 9,431,455
1003	Oshima Japanese	Japanese Patent Publication No. JPH11-284067
1004	Oshima Certificate	Translation Certificate for JPH11-284067
1005	Oshima	Certified English Translation of JPH11-284067
1006	Nagai	U.S. Patent No. 7,598,557
1007	Lee	U.S. Patent Publication No. 2009/0072282
1008	Crook	U.S. Patent No. 9,165,762
1009	Miyazaki	European Patent Publication No. 1,065,714

1010	Wang	U.S. Patent No. 7,803,647
1011	Omi	U.S. Patent No. 7,816,749
1012	Foggiato	J. Foggiato, Chemical Vapor Deposition of Silicon Dioxide Films, Handbook of Thin Film Deposition Processes and Techniques, <i>Principles, Methods, Equipment and Applications</i> , 2nd Ed. at 111-150 (2001)
1013	Wolf I	S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 1: Process Technology</i> , 2 nd Ed. (2000)
1014	Wolf II	S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 2: the Submicron MOSFET</i> (1990)
1015	Stojakovic	G. Stojakovic and X.J. Ning, <i>Reactive Ion Etch of 150 nm Al Lines for Interconnections in Dynamic Random Access Memory</i> , Journal of Vacuum Science & Tech. A 18, 1425 (2000)
1016	White	M. H. White et al., A Low Voltage Sonos Nonvolatile Semiconductor Memory Technology, IEEE Part A, Vol. 20, No. 2, at 191 (1997)
1017	Frank	W. E. Frank, <i>Approaches For Patterning of Aluminum</i> , Microelectronic Engineering 33 (1997)
1018	Riley	<i>Plasma Etching of Aluminum Metallizations For Ultralarge Scale Integrated Circuits</i> , J. Electrochem. Soc. 140 1518 (1993)
1019	Hwang	<i>Modeling of Charging Damage During Interlevel Oxide Deposition In High-Density Plasma</i> , J. of Applied Physics, Vol. 84, No. 1 (1998)

IV. LEGAL STANDARDS

12. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

13. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the Phillips standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

B. Anticipation

14. I understand that a claim is invalid if it is anticipated. Anticipation of a claim requires that every element of a claim be disclosed expressly or inherently in a single prior-art reference, arranged in the prior-art reference the same way it is arranged in the claim, so that the disclosure effectively puts the public in possession of the invention. For the claim to be anticipated implicitly, I understand that the reference must make clear that the missing descriptive matter in the claim of the patent is necessarily or implicitly present in the allegedly anticipating reference, and that it would be so recognized by one of ordinary skill in the art.

C. Obviousness

15. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed.

16. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

17. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

18. I understand that a POSITA has ordinary creativity, and is not an automaton.

19. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

20. I understand that prior art to the '455 patent includes patents and printed publications in the relevant art that predate the Priority Date of the '455 patent.

21. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

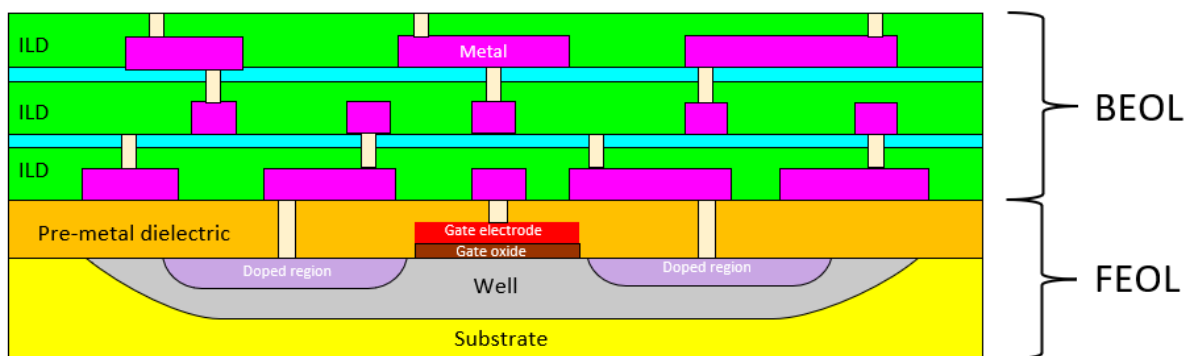
V. OVERVIEW OF THE TECHNOLOGY

A. Back-End And Front-End Semiconductor Processing

22. A semiconductor device is fabricated on a wafer, which is a substrate typically made of silicon. During the fabrication process, the wafer undergoes a number of steps including implantation, etching, and deposition such that layers of materials having different electrical and mechanical properties can be formed and

patterned within and over the wafer. The end product is a circuit chip that can receive and route electrical signals into individual device components such as transistors, resistors, and capacitors, formed on the substrate.

23. Semiconductor fabrication processes are largely divided into front-end-of-the-line (FEOL) processes and back-end-of-the-line processes (BEOL). A simplistic cross-sectional view of a conventional semiconductor device is illustrated below:



24. Front-end processing involves ion-implanting and diffusing dopants (*i.e.*, an impurity element introduced into a material to alter its electrical properties) in the **silicon substrate** (yellow) to form wells (gray), *i.e.*, surface regions that will contain devices such as transistors. A thin oxide film is typically formed next on the well surface, followed by the deposition of a polycrystalline silicon (polysilicon) layer. After patterning of the polysilicon and oxide, a gate structure consisting of **gate oxide** (brown) and **gate electrode** (red) is formed. The gate electrode is

conventionally made of polysilicon because its high melting point allows it to withstand subsequent high temperature process steps during IC fabrication. Ex. 1014 at 318–319. Doping of the areas adjacent to the gate results in the formation of the **source and drain regions** (purple), thereby completing the formation of a planar transistor. Next, a **pre-metal dielectric layer** (orange) is formed over the polysilicon gate, source, and drain to protect and electrically isolate the transistor terminals. Vias, also sometimes referred to as contacts, are then opened in the pre-metal dielectric and subsequently filled with metal to create electrical contacts to the source, drain and gate of each transistor.

25. Back-end processing encompasses the formation of interconnects over the premetal dielectric layer. Interconnects are patterned metal wires, which connect electrically transistors and other electrical elements to the world outside the semiconductor device. A semiconductor device typically has multiple layers of **interconnects** (magenta), called metallization levels, which are stacked at different levels above the transistors. Connections between metal wires of different metallization levels are facilitated by means of metal-filled vias (white). Because the metal wires carry different signals, it is important to maintain electrical isolation between the wires within each metallization level and across different metallization levels. Ex. 1012 at 111. In the 1990s, one well-known way of accomplishing isolation was to deposit a dielectric material over the patterned metal lines in each

level. Such layers, referred to as **interlevel dielectric (ILD) layers** (green), must fill the spaces in-between the metal lines entirely. After filling, the surface of the ILD layer is planarized to remove shape irregularities and create a smooth flat surface for the next metallization level.

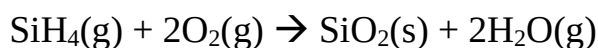
B. Formation Of ILD Layers And Hydrogen Control

26. In semiconductor devices fabrication at the time of the claimed invention, the metal interconnect lines/traces were commonly formed of aluminum, which in the 1990s was often deposited as a continuous layer and then patterned by plasma etching. The **ILD layers** (green) are deposited subsequently on the patterned metal lines with the goal to fill the space in-between the lines to provide electrical isolation. Conformal step coverage around the metal lines is of paramount importance for the performance of semiconductor devices.

27. The chemical composition, structure, and physical properties of ILD layers have been widely studied. Early on, the ILD material was silicon dioxide, which was deposited at high pressure (~1 atm) from silane (SiH_4) and oxygen precursors in heated reactors (furnaces), Ex. 1012 at 112. The process became known as “Atmospheric Pressure CVD (APCVD).” *Id.* The resultant films had suitable electrical characteristics, but due to gas phase reactions, the step coverage was poor. *Id.* at 113.

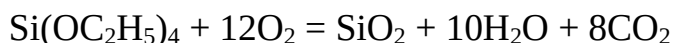
28. Step coverage improved significantly by using plasma-enhanced chemical-vapor deposition (PECVD) reactors with a source of silicon called TEOS (vide infra) at low pressure. Ex. 1014, at 198. Plasmas permit controlled dissociation of precursors in the gas-phase to generate reactive species that can be deposited at lower temperature. Plasma ions also assist in directional deposition for void-free filling of high aspect ratio spaces. Id. at 198. Also, the plasma process ensures better control of deposition rate and film properties. Ex. 1012, at 126. Both atmospheric pressure and plasma-enhanced chemical vapor deposition techniques were extensively in use by 2001.

29. As the '455 patent admits, a “principal component” commonly used to form an ILD is silicon dioxide (SiO₂), and the “[t]wo prevalent reactive gases” used for forming silicon dioxide are silane (SiH₄) and tetra-ethyl-ortho-silicate (TEOS, Si(OC₂H₅)₄). Ex. 1001 at 1:57–60, 2:4–8; Ex. 1012 at 113–114. For example, as stated above, a silicon dioxide dielectric film can be formed by reacting silane with oxygen gases as follows:



Ex. 1001 at 9:46; see also Ex. 1012 at 116, 132. A silane-based dielectric film, however, suffers from poor gap-filling characteristic because of its higher reactivity. Ex. 1012 at 112; Ex. 1001 at 9:47–50.

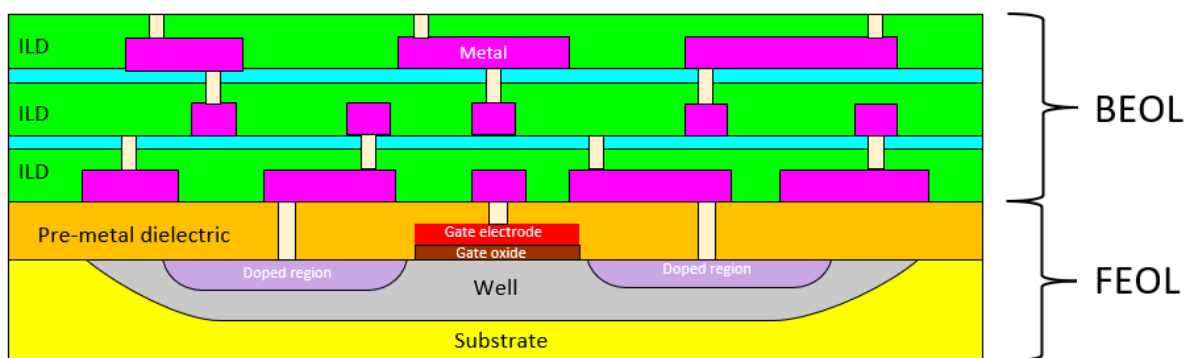
30. It was known since at least the 1980s, that use of TEOS plus oxygen or ozone could help overcome this limitation. Ex. 1012 at 114. For example, a dielectric film can be formed by reacting TEOS with oxygen as follows:



The use of TEOS as the silicon-supplying reactant provides a more conformal film than obtainable with silane chemistry. Ex. 1012 at 132; Ex. 1001 at 5:53–57 (using TEOS-based oxide as an ILD material was “well known due to their superior gap-filling characteristics.”). But these reactions produced a large amount of moisture (10H₂O) per deposited SiO₂ molecule, which was problematic because the residual moisture reacts with aluminum in subsequent fabrication processes to generate hydrogen. While some hydrogen may help passivate surface states at the gate oxide interface with silicon, too much hydrogen can lead to problems in the front end and a deterioration in the semiconductor device performance. Ex. 1001 at 2:53–60; Ex. 1012 at 117.

31. In light of the strengths and weaknesses associated with silane-based and TEOS-based dielectric films, it was also known to use a combination of films as separate **dielectric layers** (cyan) in semiconductor devices. By using a TEOS-based ILD layer with another denser dielectric layer (*e.g.*, silane-grown), one could leverage the gap-filling characteristic of the TEOS-based film to securely maintain separation between metal layers while mitigating generation and diffusion of

hydrogen. See, e.g., Oshima (Ex. 1005), Nagai (Ex. 1006), and Lee (Ex. 1007). The dielectric layers used for hydrogen control are depicted in cyan in the illustrative cross-sectional view of a conventional semiconductor device, schematically depicted below.



VI. OVERVIEW OF THE '455 PATENT

32. The '455 patent is titled *Back-end Processing Using Low-Moisture content Oxide Cap Layer*. Ex. 1001. The patent was filed on November 9, 2014 and issued on August 30, 2016. *Id.*

A. Specification of the '455 Patent

33. The '455 patent is directed to semiconductor fabrications processes and more particularly to back-end-of-the-line processing. Ex. 1001 at 1:7–9. It describes that “[t]he importance of hydrogen for the performance of CMOS devices is well known in semiconductor industry.” *Id.* at 2:18–19. While a certain amount of hydrogen is needed, “excess amounts of hydrogen are responsible for device instabilities” such as by causing “floating gate memory retention loss.” *Id.* at 2:24–

25. The '455 patent discusses various known approaches to controlling the generation and migration of hydrogen. *E.g.*, *id.* at 3:27–41 (use of a gettering/barrier layer on a pre-metal dielectric); 3:42-63 (extra high-temperature annealing); 4:14–17 (“‘reflow’ bake to achieve ‘silane Oxide’ protection quality using a modified ‘TEOS-based oxide’ in BPSG formation”).

34. The structure of a semiconductor IC of the '455 patent is illustrated in Fig. 2. *First*, in front-end processing, doped **diffusion regions 103-1, 103-2, 103-3, and 103-4** (purple) are formed in a **semiconductor substrate 101** (yellow), and then **polycrystalline silicon structures 110-1, 110-2, and 110-3** (red) are formed on respective gate oxide structures on an upper surface 102. *Id.* at 11:62–67. A **pre-metal dielectric layer 122** (orange) is then deposited over the polycrystalline silicon structures.

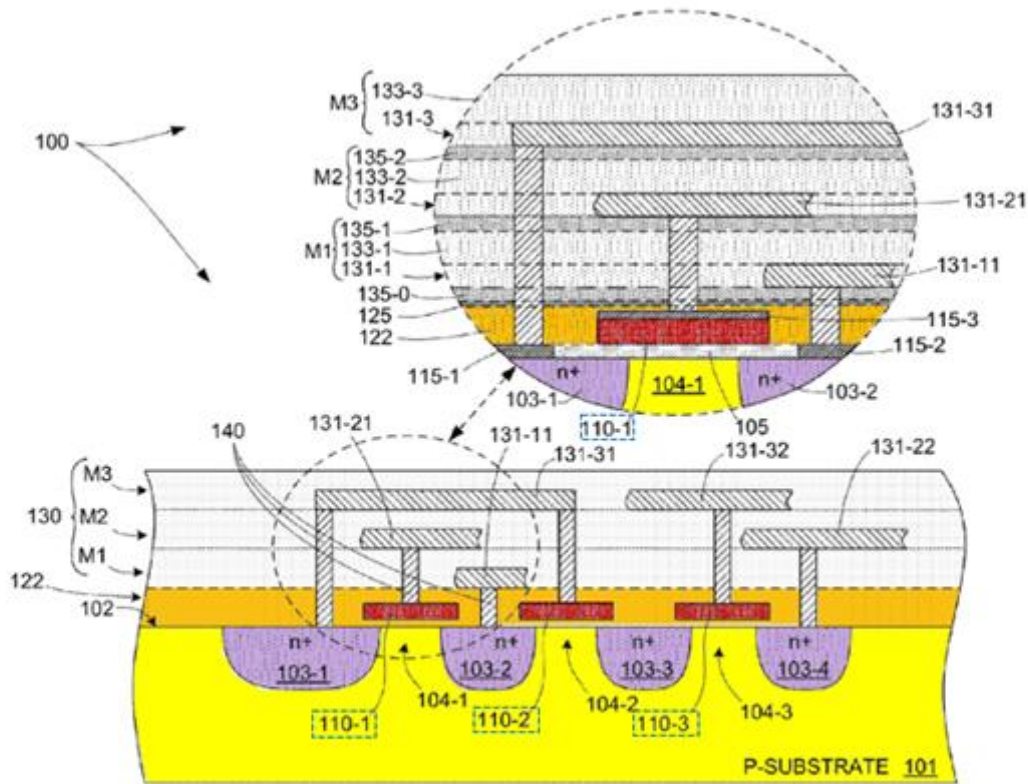


FIG. 2

35. In back-end processing, **metallization layers M1, M2, and M3** (magenta) are sequentially formed in a stack arrangement over the pre-metal dielectric layer 122. *Id.* at 10:47–53. As in “conventional back-end processing,” each metallization layer M1 to M3 includes a patterned metal structure covered by an **ILD layer** (green). *Id.* at 10:53–62. A silane oxide is then deposited to form **cap layers 135-1 and 135-2** (cyan) on **ILD layers 133-1 and 133-2**. *Id.* at 11:6–10.

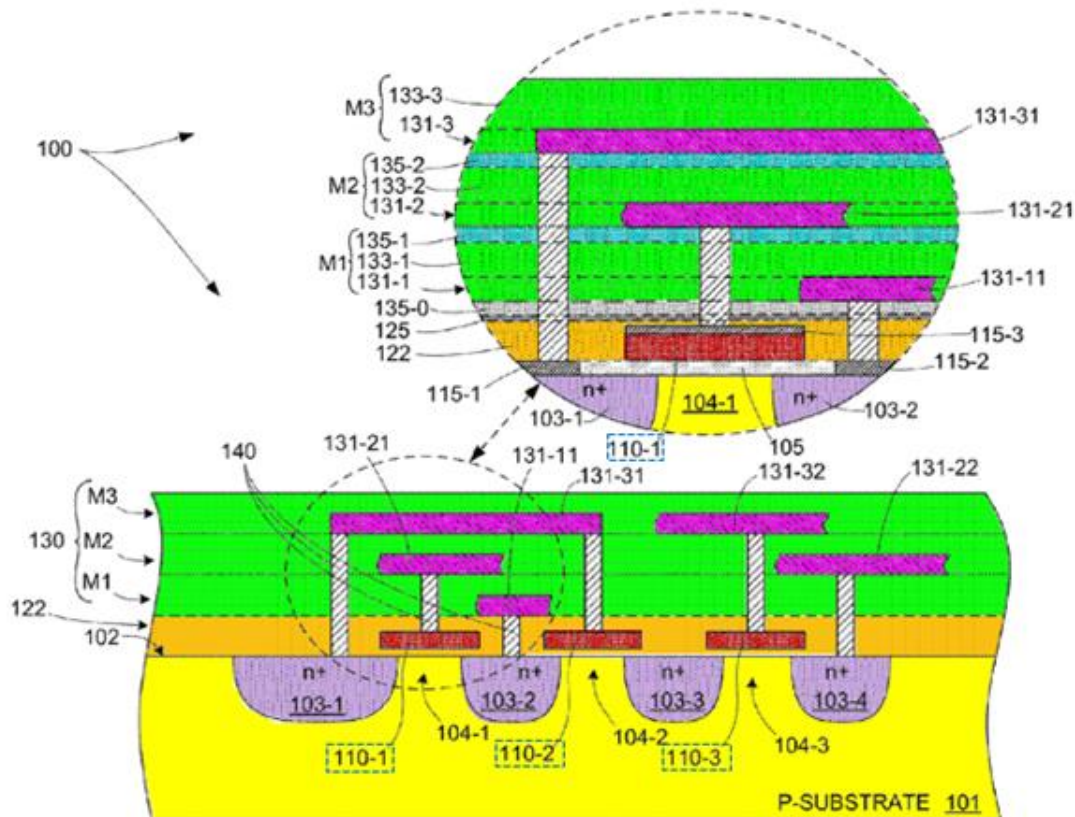


FIG. 2

36. According to the '455 patent, [t]he combined use of TEOS-based oxide and silane oxide produces a superior ILD structure in that the use of TEOS-based oxide facilitates excellent gap filling over patterned metal structures 131-11 and 131-21, and the use of silane oxide cap layers 135-1 and 135-2 having the optimized thickness was found to significantly reduce the generation and migration of hydrogen atoms/ions into front-end structures.” *Id.* at 11:10–17.

37. The '455 patent acknowledges that capping layers were known in the prior art and that their main purpose was to “improve the properties of the first dielectric stack which includes BPSG (the layer that is used for gettering).” *Id.* at

11:29–33; *see also id.* at 3:27–41 (describing that a silicon nitride or silicon oxy-nitride was typically formed under a gettering/barrier layer, which is formed on the pre-metal dielectric layer to protect the front-end structures before beginning back-end processing). According to the '455 patent, the high-density low-moisture cap layer of the '455 patent is different because its “main purpose” is “to isolate the TEOS-based oxide of the ILD layer from the plasma environment during aluminum over-etch. *Id.* at 11:34–38. In particular, the '455 patent describes that “it was critically important to adjust the [] cap layer thickness to comply with the aluminum over etch penetration depth” namely “100 Å or greater.” *Id.* at 11:38–51.

38. With respect to the phrase “high-density low-moisture content oxide,” the '455 patent states that it is not limited to silane oxide and may include other suitable oxide materials “such as high-density, low moisture silicon oxy-nitride (i.e., oxy-nitride formed using a plasma process, e.g., by adding N₂ or NO to silane oxide).” *Id.* at 10:4–10.

B. Prosecution History of the '455 Patent

39. On January 21, 2016, the Examiner issued a Non-final Rejection, rejecting original claims 1–11, 14–20 for indefiniteness due to the lack of sufficient antecedent basis for “the patterned aluminum structure” term of claim 1. Ex. 1002, January 21, 2016 Office Action at 5. The Examiner rejected all independent claims as obvious based on U.S. Pub. Nos. 2007/0170546, 2012/0175736, and

2013/0092929. The Examiner identified claims 4–5, 7–8, and 16–17 as allowable if rewritten in independent form. *Id.* at 15.

40. On April 21, 2016, the Applicant amended independent claims to recite the limitations of claim 4. Original claim 4 recited “[t]he method of Claim 2, wherein forming the cap layer over said ILD layer comprises generating silane oxide over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer.” Claim 1, in relevant part, was amended to incorporate claim 4 as follows:

forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

- forming a patterned metal structure;
- forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned ~~aluminum~~ metal structure; and
- forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer,

Id., April 21, 2016 Amendment at 6. The Applicant stated that the amendment was “to include the gist of Claim 4” and that, in view of the amendment, claim 1 is “patentable over all cited prior art.” *Id.* at 14–15.

C. Priority Date

41. The ’455 patent was filed on November 9, 2014 and issued on August 30, 2016. Ex. 1001. It does not claim priority to an earlier priority date. *Id.*

VII. LEVEL OF ORDINARY SKILL IN THE ART

42. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

43. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '455 patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '455 patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

44. In my opinion, a person of ordinary skill in the art at the time of the alleged invention ("POSITA") would have been a person having a Master's degree in Electrical Engineering, Chemical Engineering, Materials Science, or Physics and three to five years of industry experience in integrated circuit design, layout, packaging or fabrication; or a Ph.D. specializing in the field. This level of skill is

approximate, and a greater level of experience in the relevant field may compensate for less education, and vice versa.

45. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VIII. CLAIM CONSTRUCTION

A. Claim 19 Preamble

46. The preamble of claim 19 recites “[a]n image sensor comprising.” Ex. 1001 at claim 1. The preamble of claim 19 merely recites an intended use for the invention, namely “an image sensor,” and the structural elements of a semiconductor device are only recited in the claim body. As such, I understand that the preamble of claim 19 should be construed as non-limiting.

B. “silane oxide” and “TEOS-based oxide”

47. The Challenged Claims recite a “silane oxide” and a “TEOS-based oxide.” The ’455 patent specification describes the terms as “SiO₂ formed using silane” and “SiO₂ formed using TEOS,” respectively. See Ex. 1001 at 2:8–12 (“Because the step coverage (gap filling) ability of SiO₂ formed using TEOS (referred to herein as “TEOS-based oxide”) is better than SiO₂ formed using silane (referred to herein as “silane oxide”), TEOS-based oxide is preferred in semiconductor manufacture.”). For purposes of this Petition, these claim terms have been interpreted with the plain and ordinary meaning as would be understood by

POSITA at the time of the invention and is consistent with the disclosures in the '455 patent.

48. For the remaining terms, I have applied the ordinary and customary meaning as it would have been understood by a person of ordinary skill in the art at the time of the alleged invention, in the context of the '455 patent and its prosecution history, as well the consistent with Patent Owner's reading and contentions advanced in the related matters.

49. I reserve the right to respond to any constructions that Patent Owner may submit.

IX. OVERVIEW OF THE PRIOR ART

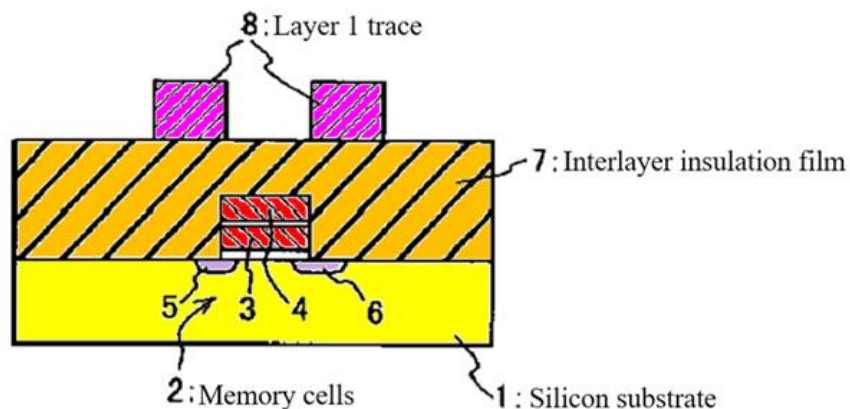
A. Oshima (JPH11-284067)

50. Oshima is a Japanese patent publication titled, *Semiconductor Device And Manufacture Thereof*. Ex. 1005. The original publication is provided as Exhibit 1003. An affidavit of translation and certified translation are provided as Exhibits 1004 and 1005. Oshima was filed on March 27, 1998 and published on October 15, 1999. I understand that Oshima thus qualifies as prior art under 35 U.S.C. § 102(a)(1).

51. Oshima is directed to a semiconductor device having a multilayer wiring structure and a method of manufacturing the same. Ex. 1005 at [0001]. Oshima starts with the initial structure of Fig. 1, reproduced below. *Id.* at [0021].

This device includes a standard stacked gate memory cell 2 formed on a **silicon substrate** (yellow) according to a known method. *Id.* The non-volatile memory cell 2 is formed by stacking **a floating gate 3 and a control gate 4** (red) and **source and drain diffusion regions 5 and 6** (purple). An **interlayer insulating film 7** (orange) in the form of borophosphosilicate glass (BPSG) is deposited over the entire surface above the non-volatile memory cell 2. *Id.* at [0022]. Over the interlayer insulating film 7, a trace material film such as aluminum (Al) is deposited and patterned to form a **metal trace 8** (magenta). *Id.*

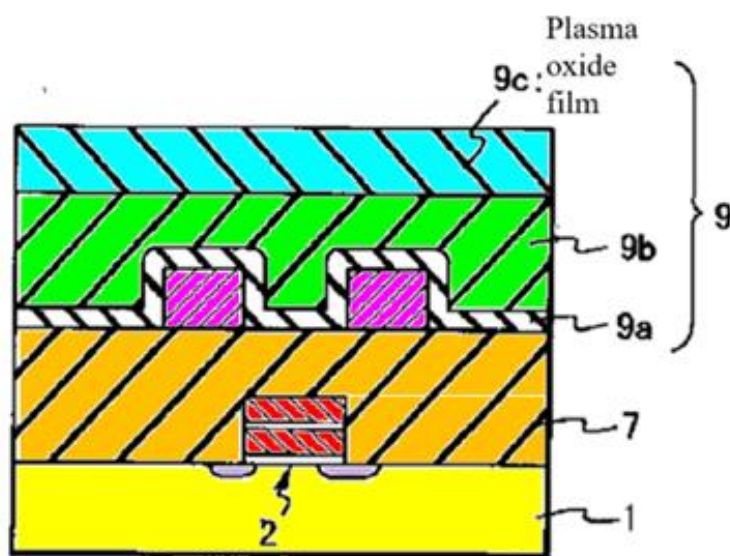
(FIG. 1)



52. With the structure of Fig. 1 as a starting point, Oshima teaches forming, in order, a plasma oxide film 9a, a **TEOS oxide film 9b** (green), and a **plasma oxide film 9c** (cyan). *Id.* at [0023]–[0027]; Fig. 4. The plasma oxide film 9a is a silicon oxide film deposited by plasma CVD using mixed gas containing silane (SiH_4) and N_2O gas. *Id.* at [0023], [0002]. The TEOS oxide film 9b is deposited by CVD using a source gas of TEOS and F_2 . *Id.* at [0023]. Subsequently, a plasma oxide film 9c

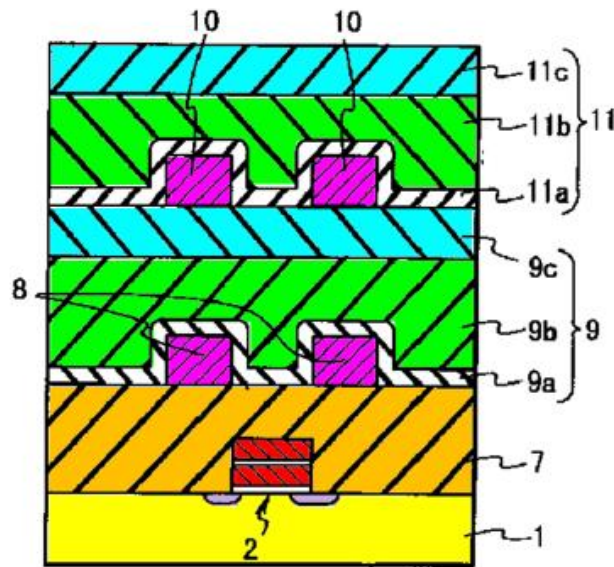
is formed over the TEOS oxide film using the same conditions as the previous plasma oxidation film 9a to a thickness of about 500 nm. *Id.* at [0027]. Oshima teaches that the “poor step coverage” of the plasma oxide film 9c is supplemented by the use of TEOS oxide film 9b, thus providing “the thickness required to prevent hydrogen diffusion without accruing defects.” *Id.*

(FIG. 4)



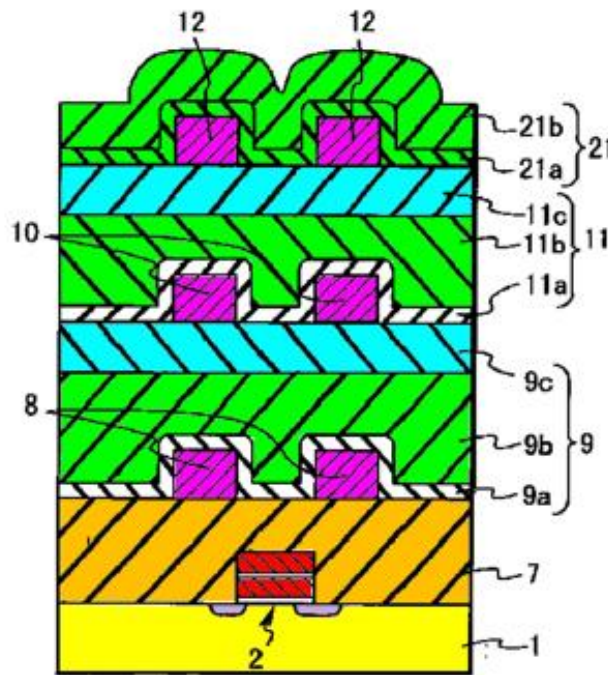
53. The next step of Oshima’s method is to stack the structure with more metallization layers. A second metal trace 10 is formed on the plasma oxide film 9c in the same manner as the first wiring layer 8. *Id.* at [0044]. Thereafter, the same three-layer structure—consisting of a plasma oxide film 11a, TEOS oxide film 11b, and plasma oxide film 11c—is deposited over the metal trace 10 in the same manner as the films 9a, 9b, and 9c, as shown in Fig. 16. *Id.* at [0045]; Fig. 16.

(FIG. 16)



54. Finally, a third metal trace 12 is patterned, over which a passivation film 21 consisting of a TEOS oxide film 21a and plasma nitride film 21b is formed.
Id. at [0046], [0039].

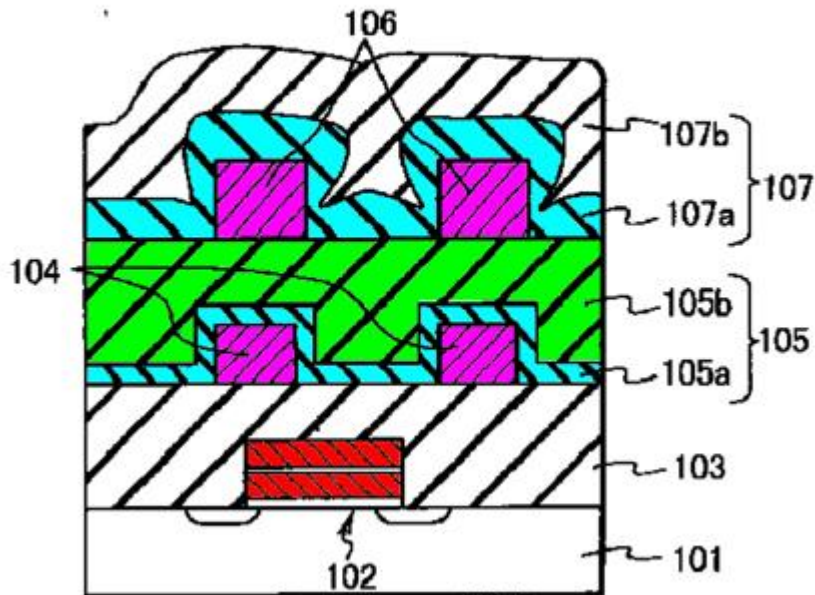
(FIG. 17)



55. Oshima discloses that, in prior art, TEOS oxide film was deposited as an interlayer insulating film 105b between metal trace layers, as depicted in Fig. 27; though, TEOS was known to easily absorb moisture, which deteriorates the charge retention characteristics of a memory cell. *Id.* at [0003]; Figs. 26–27. Thus, prior art solutions taught depositing a plasma oxide layer 105a (cyan) between the **TEOS oxide film 105b** (green) and the **metal trace 104** (magenta), to prevent absorption of moisture by TEOS. But Oshima notes that, because a **plasma oxide layer 107a** (cyan), particularly in the passivation layer 107, would become thin at the edges of the metal trace, there was insufficient prevention of hydrogen diffusion from the

plasma nitride 107b of the passivation layer 107 into the front-end structure. *Id.* at [0003]–[0005].

(FIG. 27)

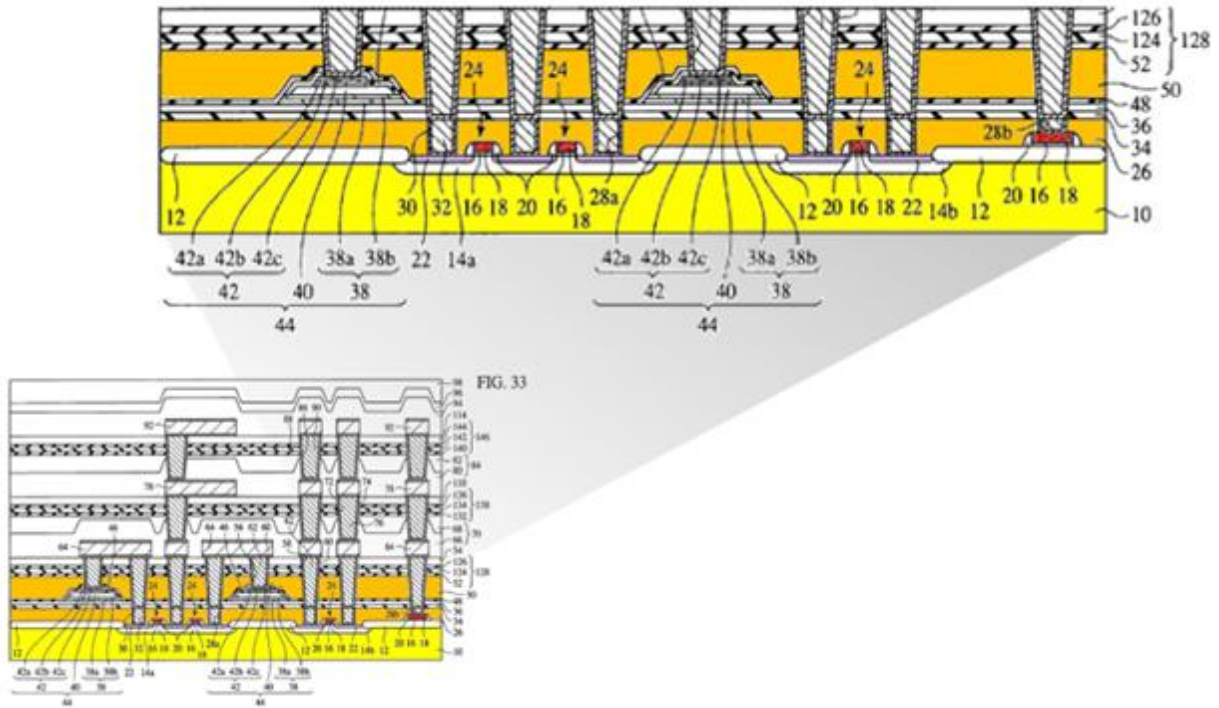


56. Oshima's three-film structure (plasma oxide / TEOS oxide / plasma oxide) overcomes this problem by enabling the overlying plasma oxide film to maintain sufficient thickness for preventing hydrogen diffusion. *Id.* at [0034], [0047]. Taking the first stack as an example, the upper plasma oxide film 9c covers the entire surface of the TEOS film 9b, thereby preventing moisture from being absorbed again in the TEOS oxide film 9b after it is annealed out and preventing diffusion of moisture from the insulating film 11 of the upper layer. *Id.* at [0048].

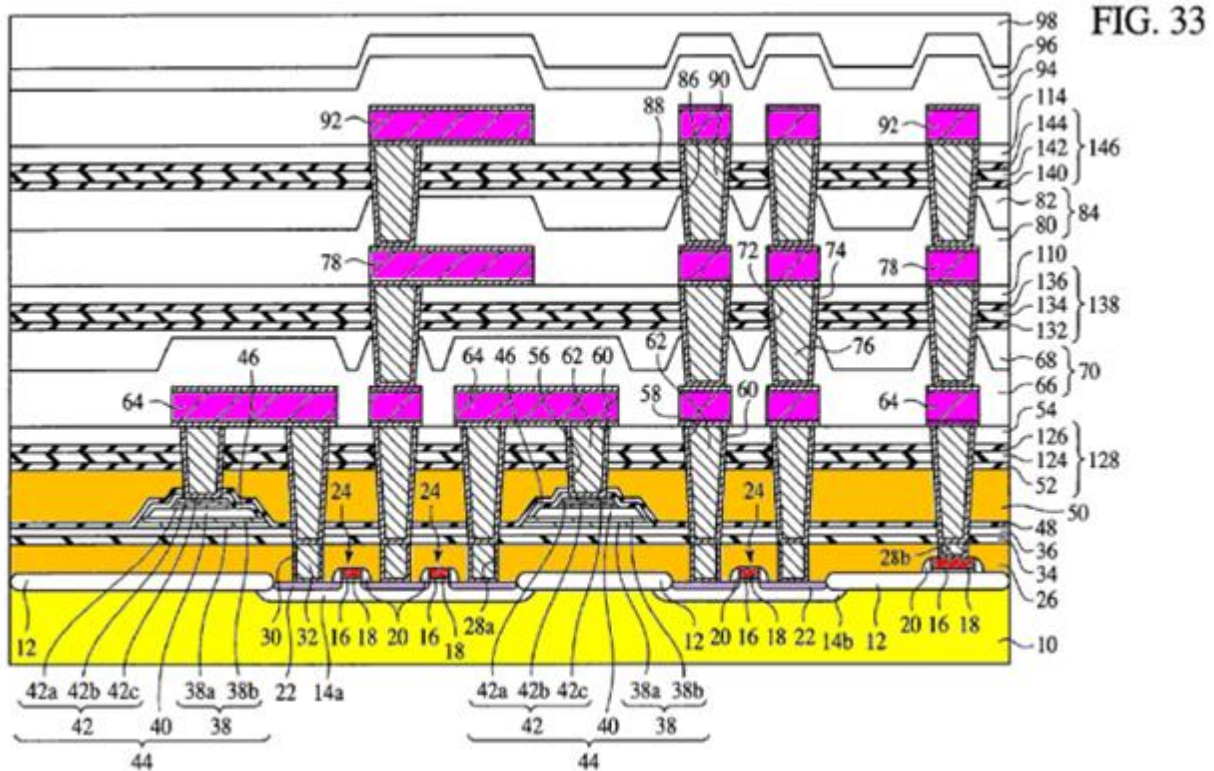
B. Nagai (US7598557)

57. U.S. Patent No. 7,598,557 (“Nagai”) is titled *Semiconductor Device And Method For Fabricating A Semicondutor Device Including First And Second Hydrogen Diffusion Preventing Films*. Ex. 1006. Nagai was published on October 6, 2009. I understand that Nagai thus qualifies as prior art under 35 U.S.C. § 102(a)(1).

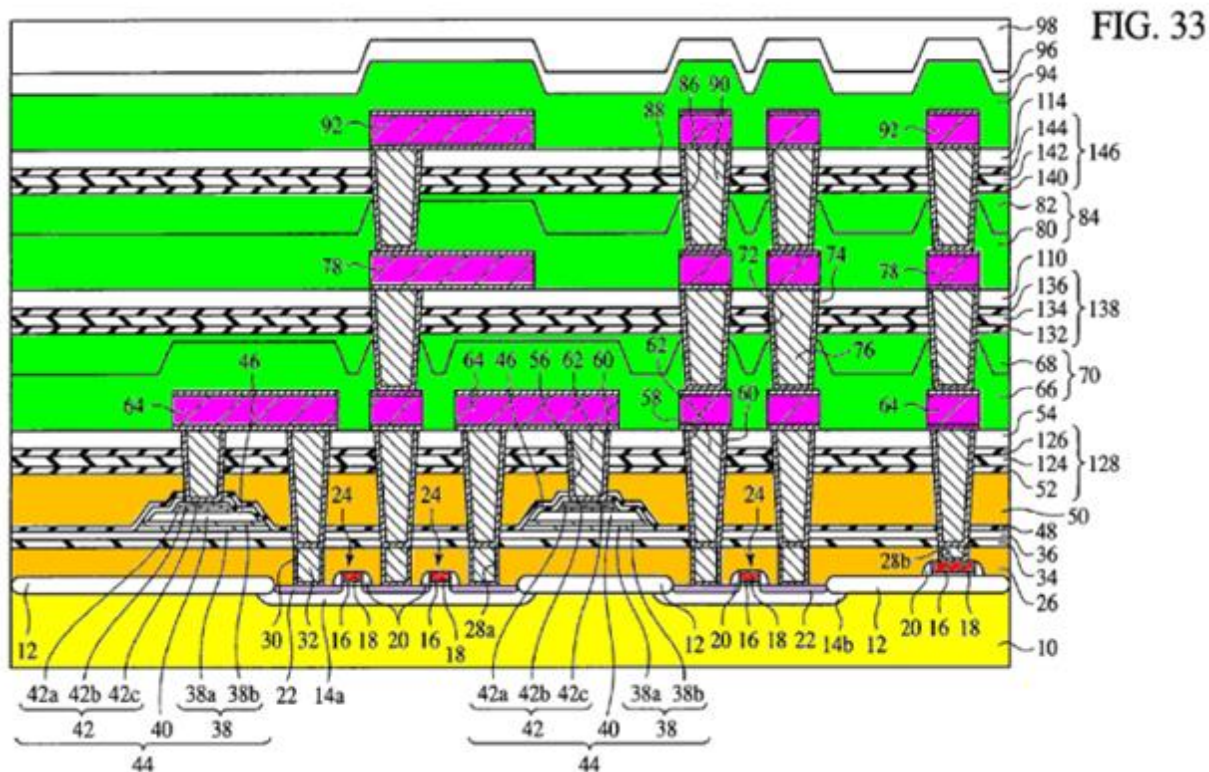
58. Nagai is directed to a semiconductor device comprising multiple stacks of metallization layers, interlayer dielectric layers, and hydrogen diffusion prevention films. *Id.* at Abstract. As shown in Fig. 33, **source/drain diffused layers 22** (purple) are formed in the **silicon substrate 10** (yellow). *Id.* at 6:66–7:2. Over a surface of the substrate, a polycrystal silicon film is patterned to form **gate electrodes 18** (red). *Id.* at 17:39–44. Over the gate electrodes 18, a first interlayer insulation film 26 (SiON and silicon oxide) and a second interlayer insulation film 50 (silicon oxide film formed by plasma TEOS CVD) are deposited. *Id.* at 7:1–3, 17:66–18:3, 20:38–43.



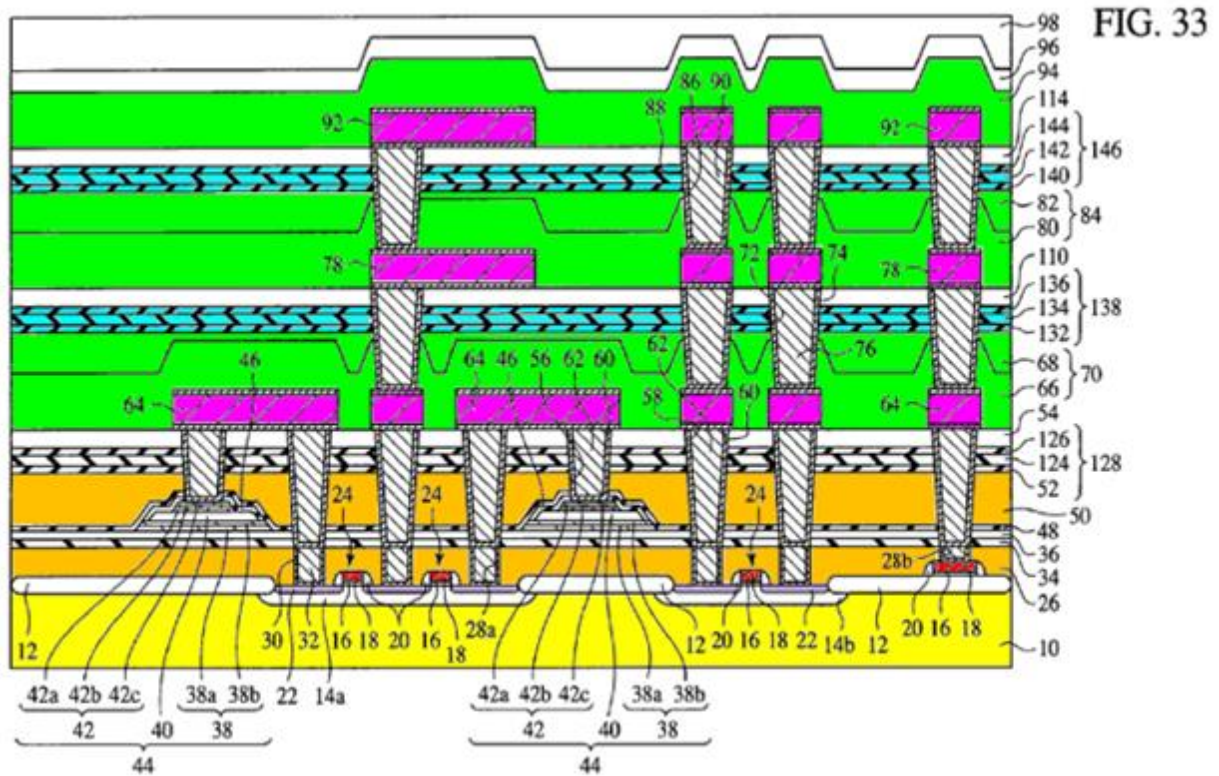
59. In back-end processing, Nagai discloses forming **metal interconnection layers 64, 78, and 92** (magenta) from materials including Ti, TiN, and AlCu. *Id.* at 22:13–20, 23:21–26, 24:33–42.



60. Over each metal interconnection, **silicon oxide films 70, 84, and 94** (green) are formed, each by plasma TEOS CVD. *Id.* at 22:21–34, 23:31–43, 24:43–49. Over the silicon oxide film 94, silicon nitride film 96 and polyimide film 98 are formed.



61. Further, over each **silicon oxide film 70 and 84** (green) (referred to as the first and second inter-layer insulating films), a **barrier film 138 and 146** (cyan) consisting of a pair of hydrogen/water diffusion prevention films and a stress mitigating film is formed, respectively. *Id.* at 34:42–48.



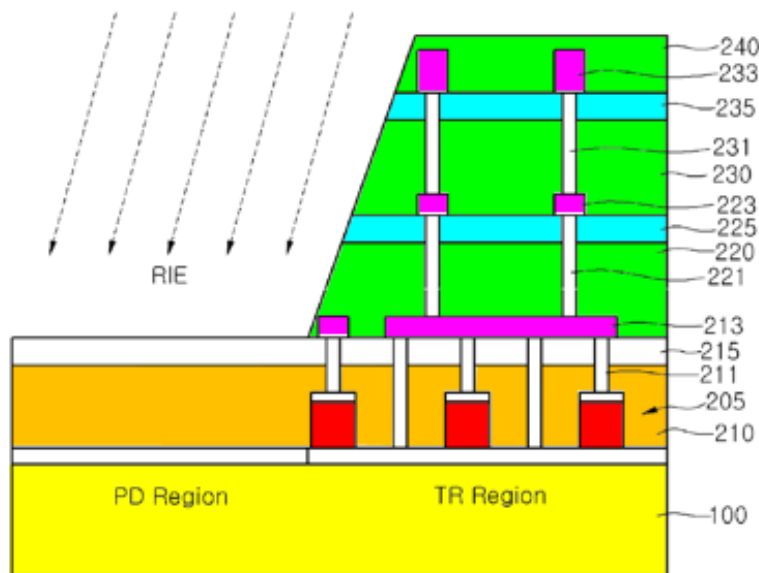
62. Nagai discloses that, unlike conventional hydrogen diffusion preventing film which does not have good coverage, the flat hydrogen diffusion prevention film of its teaching has “very good coverage” and “can barrier the hydrogen and the water without failure.” *Id.* at 8:43–48, 35:37–45.

C. Lee (US 2009/0072282)

63. U.S. Patent Publication No. 2009/0072282 (“Lee”) is titled *Image Sensor And Method For Manufacturing The Same*. Ex. 1007. Lee was published on March 19, 2009. I understand that Lee thus qualifies as prior to the ’455 patent under 35 U.S.C. § 102(a)(1).

64. Lee discloses a method for manufacturing CMOS and CCD image sensors. *Id.* at [0006], [0003]. A cross-sectional view of an embodiment of Lee's image sensor is shown in Fig. 2 below. The image sensor includes a transistor (TR) region and a photodiode (PD) region on a substrate 100. *Id.* [0015], [0024]. A TR region includes a polysilicon gate electrode layer formed by CVD of silicon (e.g., from silane in the presence of a plasma). *Id.* A PD region may be formed by a deep N-type layer and a shallow P-type layer in the substrate. *Id.* at [0025]. The image sensor also includes a **first dielectric layer 210** (orange) formed over the substrate, and second, third, and uppermost **dielectric layers 220, 230, and 240** (green) formed over the **metal lines 213, 223, and 233** (magenta), which may comprise aluminum. *Id.* at [0026]–[0035]. **Capping layers 225, 235** (cyan) are formed on the **dielectric layers 220, 230** (green), respectively; and “comprise, e.g., TEOS, USG, a plasma silane [e.g., silicon dioxide formed by plasma-assisted CVD of silicon dioxide from silane and oxygen], or a combination thereof” *Id.* at [0027], [0031], [0033].

FIG. 2



D. Crook (US9165762)

65. U.S. Patent No. 9,165,762 (“Crook”) is titled, *Method of Depositing Silicone Dioxide Films*. Ex. 1008. Crook was filed on April 24, 2013. I understand that Crook thus qualifies as prior art under 35 U.S.C. § 102(a)(2).

66. Crook is directed to a method of depositing silicon dioxide films using tetraethyl orthosilicate (TEOS), oxygen (or an oxygen source), and hydrogen in a way that reduces moisture reabsorption by TEOS. *Id.* at 1:31–40, cl. 1. Crook further discloses that resulting silicon dioxide films may undergo a post-deposition hydrogen plasma treatment; this treatment, according to Crook, further suppresses reabsorption of moisture. *Id.* at 1:55–59, cl. 2. As disclosed in Crook, its method may be implemented at any suitable temperature; and embodiments implementing

the invention at temperature ranges from 100–500°C, 100–250°C, and 125–175°C, are disclosed. *Id.* at 1:41–48.

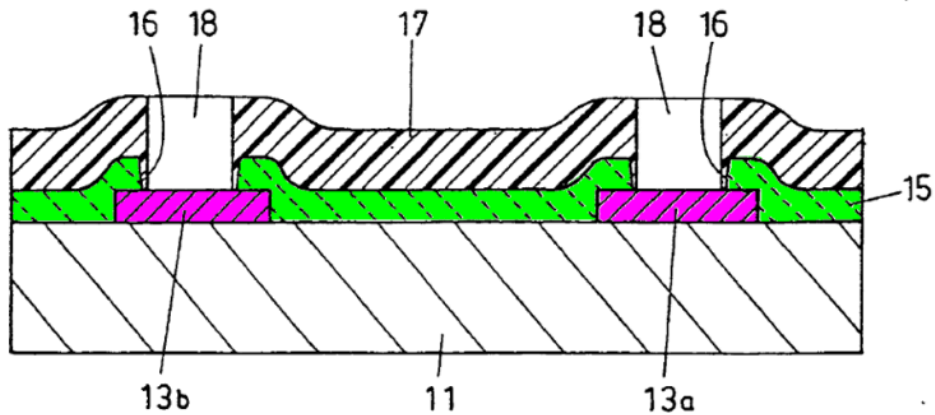
E. Miyazaki (EP1065714)

67. European Patent Publication No. 1,065,714 (“Miyazaki”) is titled *Method of Fabricating Semiconductor Device*. Ex. 1009. Miyazaki was published on March 1, 2001. I understand that Miyazaki thus qualifies as prior art to the ’455 patent under 35 U.S.C. § 102(a)(1).

68. Miyazaki is directed to fabrication of a semiconductor device, particularly to formation of interconnections and interlayer insulation film. *Id.* at [0001].

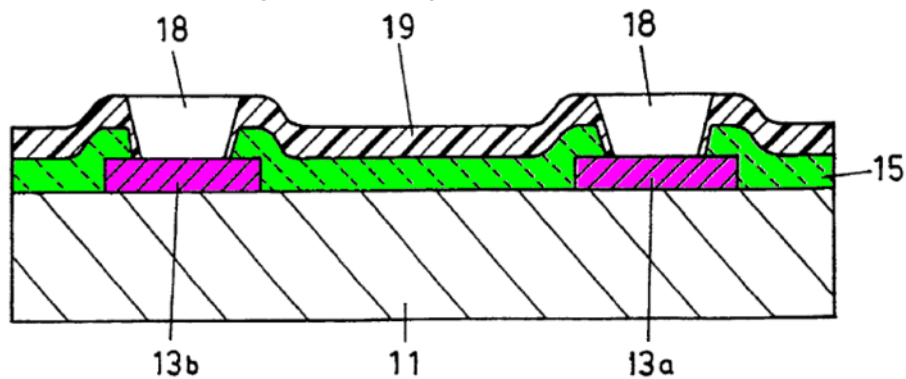
69. Miyazaki notes that, in prior art devices, the insulation resistance between the upper layer interconnections is not sufficiently high, increasing current leakage and deteriorating reliability. *Id.* at [0013]–[0014]. To address such a problem, Miyazaki teaches forming a protection film 15 (made of silicon oxide or silicon nitride) over metal interconnections 13a and 13b, exposing the interconnections with contact holes, forming and opening a polyimide precursor 17, and then performing annealing. Ex. 1009 at [0030]–[0035], Fig. 2.

FIG. 2



70. In particular, annealing is performed over the **protection film 15** (green) and the polyimide precursor 17 for 30 minutes at a temperature of 350°C to 400°C in the air atmosphere or a nitrogen atmosphere using a high-temperature furnace, resulting in the formation of a polyimidized film 19. *Id.* at [0036], Fig. 3.

FIG. 3



F. Wang (US7803647)

71. U.S. Patent No. 7,803,647 (“Wang”) is titled *Optical Transmission Improvement On Multi-Dielectric Structure In Advance CMOS Imager*. Ex. 1010.

Wang was published on September 28, 2010. I understand that Wang thus qualifies as prior art to the '455 patent under 35 U.S.C. § 102(a)(1).

72. Wang is directed to a semiconductor device for image sensors. *Id.* at Abstract. Wang discloses that a substrate in a semiconductor device “may include various p-type doped regions and/or n-type doped regions configured and coupled to form various devices and functional features.” *Id.* at 2:12–15, Fig. 4. In particular, Wang discloses disposing a conventional image sensor element 120 such as a photodiode in a semiconductor substrate 110 and doping, by ion implantation or diffusion, the substrate to form a light-sensing region, which is “operable to receive light (or other form of radiation energy from an object to be imaged).” *Id.* at 2:21–31.

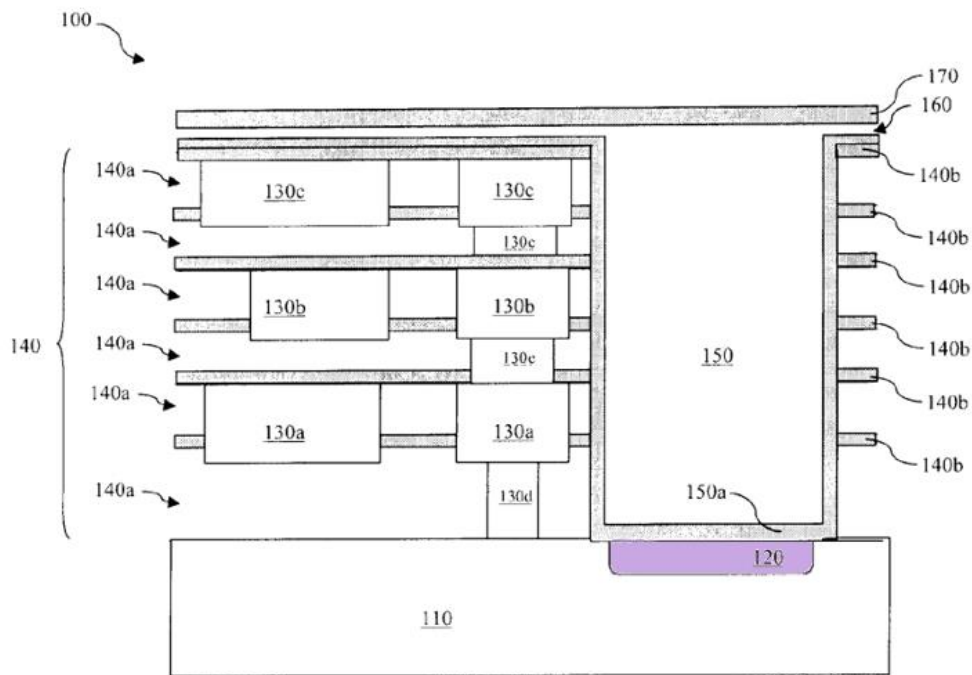


Fig. 4

G. Omi (US7816749)

73. U.S. Patent No. 7,816,749 (“Omi”) is titled *Photoelectric Conversion Device and Method of Producing the Same, and Method of Producing Line Image Sensor IC*. Ex. 1011. Omi was published on October 19, 2010. I understand that Omi thus qualifies as prior to the ’455 patent under 35 U.S.C. § 102(a)(1).

74. Omi is directed to image sensor devices and method for fabrication. *Id.* at Abstract. Omi discloses that a plurality of rectangular line image sensor ICs 110 are formed on a semiconductor substrate 101 with gaps in between the image sensors. *Id.* at 9:28–54; Fig. 5F. In an exemplary embodiment, above the semiconductor substrate 101, light shielding structure 113 made of aluminum and

an **inter-layer TEOS insulating film 103A** (green) are formed. *Id.* at 14:36–56. The insulating film 103A is flattened by chemical mechanical polishing (CMP). *Id.* at 14:52-56.

75. On the surface of the insulating film 103A, light shielding structure 113A (also made of aluminum film) and “dummy interconnects” 120 are simultaneously formed. *Id.* at 14:57-62. Over the light shielding structure 113A and the dummy interconnects 120, a **protective film 104** (grey) of silicon nitride or the like is formed by plasma CVD. *Id.* at 14:63-67, 11:22-23, Fig. 6C. The portions of the protective film 104 that cover the gaps between the dummy interconnects and the light shielding structure 113A are then removed by etching. *Id.* at 14:63–67.

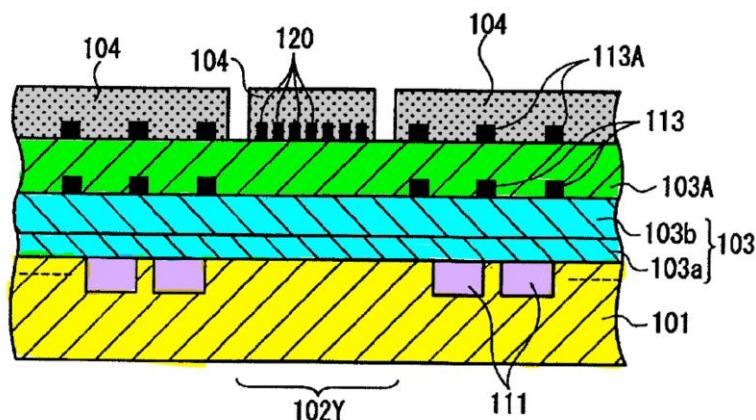


FIG. 6C

X. SPECIFIC GROUNDS FOR PETITION

76. It is my opinion that the Challenged Claims of the '455 patent are invalid on the following grounds:

Ground	Reference(s)	Basis	Claims
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1	Oshima	§ 102	1, 5, 6, 9, and 19
2	Oshima and Lee	§ 103	2, 3, 7
3	Oshima and Crook	§ 103	10
4	Nagai	§ 102	1, 8, and 11
5	Nagai and Miyazaki	§ 103	12
6	Nagai and Lee	§ 103	15
7	Nagai and Wang	§ 103	16
8	Nagai and Omi	§ 103	17, 18

A. Ground 1: Oshima anticipates claims 1, 5, 6, 9, and 19

1. Claim 1

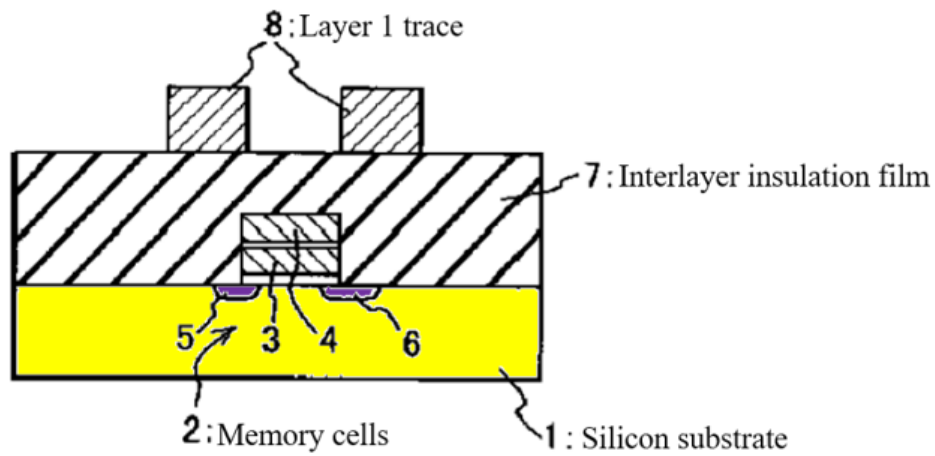
(a) 1[pre] A method for fabricating a semiconductor integrated circuit, the method comprising:

77. In my opinion, Oshima discloses the preamble to the extent it is limiting because Oshima discloses “a semiconductor device” and “a manufacturing method for the same.” Ex. 1005 at [0001].

(b) 1[a] generating front-end structures including one or more doped diffusion regions disposed in a semiconductor substrate, one or more polycrystalline silicon structures disposed over a surface of the substrate, and a pre-metal dielectric layer over the one or more polycrystalline silicon structures;

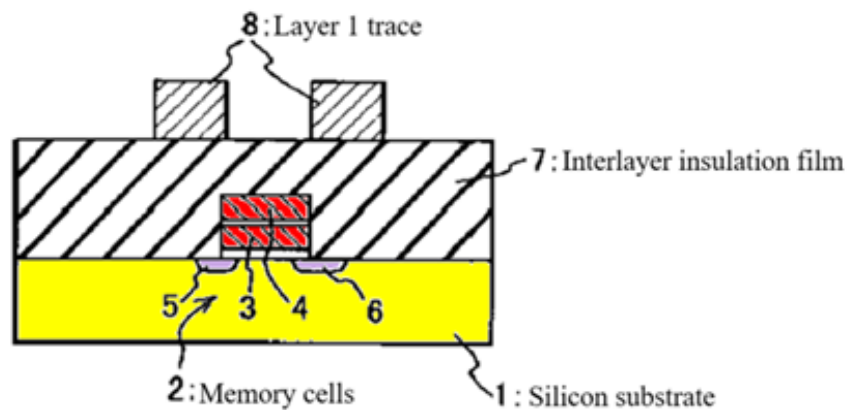
78. In my opinion, Oshima discloses generating front-end structures, including the claimed elements, and this limitation. *First*, Oshima discloses “one or more doped diffusion regions disposed in a semiconductor substrate” because Oshima discloses “forming **source and drain diffusion layers 5, 6**” (purple) disposed in the **silicon substrate 1** (yellow). *Id.* at [0021].

(FIG. 1)



79. *Second*, Oshima discloses “one or more polycrystalline silicon structures disposed over a surface of the substrate.” As part of a “*standard stacked gate [NVM]*,” Oshima discloses “stacking a floating gate 3 and a control gate 4 across gate insulation film.” *Id.* at [0021]; Fig. 1.

(FIG. 1)

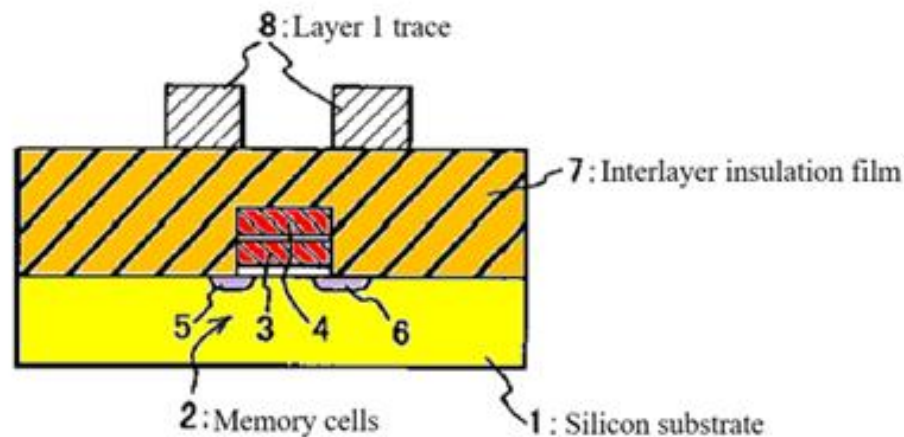


80. A POSITA would have understood that the gate electrode (**floating gate 3 and control gate 4** (red)) is a polycrystalline silicon structure, also known as polysilicon. At the time Oshima was filed (1998), the standard practice for forming a gate electrode was to use polysilicon because it was a readily accessible and cost efficient material that was known to withstand high annealing temperatures and reduce the masks required. *See* Ex. 1014 at 318–319; *see also* Ex. 1016 at 191 (“The reliability of the polysilicon gate with a pre-metallization, high-temperature hydrogen anneal have been important factors in the development of this multidielectric nonvolatile technology.”). Indeed, the ’455 patent admits that “front end processing for a [NVM] transistor **typically** involves . . . forming polycrystalline silicon (polysilicon) gate structures on the gate oxides.” Ex. 1001 at 1:28–34. Oshima thus discloses “one or more polycrystalline silicon structures disposed over a surface of the substrate.”

81. *Third*, Oshima discloses “a pre-metal dielectric layer over the one or more polycrystalline silicon structures.” Before forming any metallization layer, Oshima discloses depositing a BPSG film as an **interlayer insulation film 7** (orange). Ex. 1005 at [0022] (“A first interlayer insulation film 7 in the form of, for example, BPSG film, is deposited over the entire surface above the non-volatile memory cell 2, and then levelled.”). As the ’455 patent acknowledges, “[a] principal component of . . . BPSG is silicon dioxide, which is commonly used as dielectric

material in semiconductor processing” Ex. 1001 at 1:55–62. The interlayer insulation film 7 constitutes the claimed “pre-metal dielectric layer.”

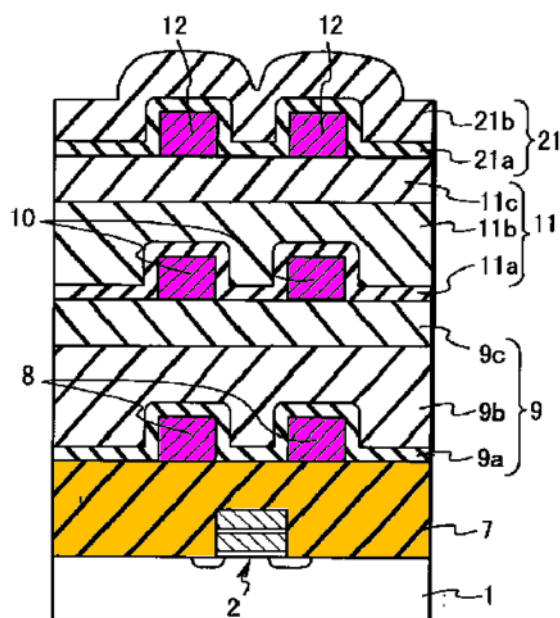
(FIG. 1)



(c) **1[b] forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:**

82. In my opinion, Oshima discloses this limitation. After deposition of the interlayer insulating film 7 discussed above, Oshima discloses depositing “trace material film such as Al or the like” over the insulating film 7 to form a **metal trace 8**, i.e., the claimed “metallization layer,” (magenta). Ex. 1005 at [0022]. Oshima discloses that “[t]he same manner of trace material film is used for the upper trace layer.” *Id.* For example, Oshima discloses a stacked structure in which a “3-layer metal trace” is used. *Id.* at [0044], [0047], Fig. 17. The trace material films from which the **metal traces 8, 10, and 12** (magenta) are patterned thus constitute the claimed “plurality of metallization layers.”

(FIG. 17)



83. Further, Oshima discloses that forming one or more of the trace material films (*i.e.*, the claimed “at least one of said metallization layers”) includes the steps discussed *infra*, with respect to limitations 1[c]–[e].

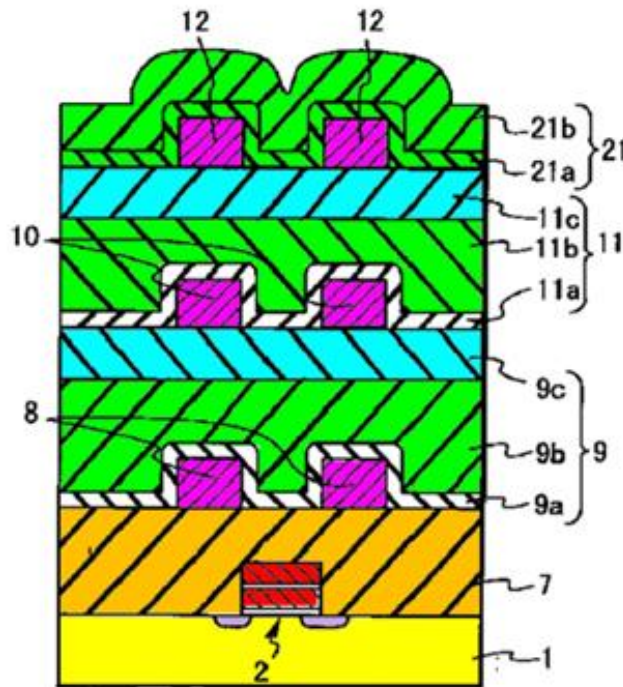
(d) 1[c] forming a patterned metal structure;

84. In my opinion, Oshima discloses this limitation. Oshima discloses patterning trace material films to form the metal traces 8, 10, and 12. Ex. 1005 at [0022] (“[A]fter [] 400 nm of trace material film such as Al or the like is deposited, [] a layer 1 trace 8 is **formed by patterning**.”); *id.* at [0030] (“a layer 2 metal trace 10 is formed by depositing 600 nm of metal trace material such as Al or the like and **patterning** according to the standard method.”); *id.* at [0039] (“**forming a pattern** in the layer 3 trace 12”).

(e) 1[d] forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure; and

85. In my opinion, Oshima discloses this limitation. Oshima teaches depositing **TEOS oxide films 9b, 11b** (green) over the **metal traces 8 and 10** (magenta), respectively. Ex. 1005 at [0023] (“In concrete terms, roughly 150 nm of **TEOS oxide film 9b** is deposited by CVD using Si(OC₂H₅)₄+F₂ as the source gas.”); *id.* at [0038] (TEOS oxide film 11b); Fig. 17. Oshima also describes forming a **passivation film 21** comprising a **TEOS-based oxide 21a**. *Id.* at [0031] (“[A] passivation film 21 is formed by depositing TEOS oxide film 21a over the entire surface to on the order of 300 nm, and then depositing plasma nitride film 21b to on the order of 600 nm.”). The **TEOS oxide films 9b, 11b** and the **passivation film 21** thus each constitute the claimed “interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure.”

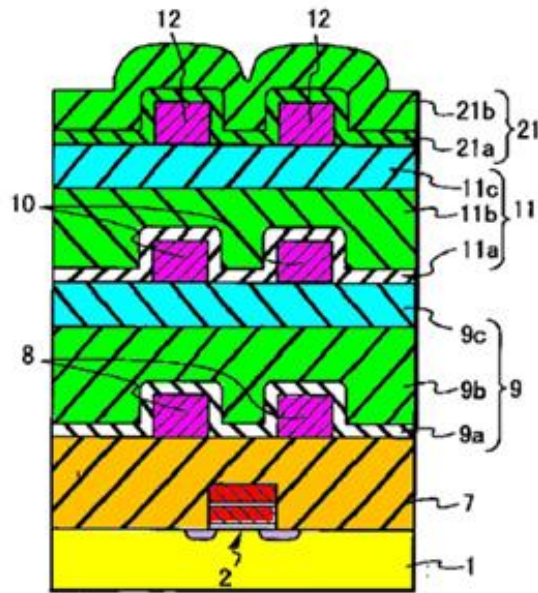
(FIG. 17)



- (f) 1[e] forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer,
- 1[f] wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.

86. In my opinion, Oshima discloses this limitation. Oshima discloses depositing **plasma oxide film 9c** (cyan) on the **TEOS oxide film 9b** (green) to “prevent diffusion of moisture and hydrogen into the non-volatile memory cell area.” Ex. 1005 at [0036]; *see also id.* at [0048], Fig. 17. A plasma oxide film is “silicon oxide film [] deposited . . . by plasma CVD using silane (SiH₄) gas.” *Id.* at [0002]. The plasma oxide film 9c thus constitutes the claimed “cap layer.”

(FIG. 17)



87. In my opinion, Oshima meets these limitations and discloses the claimed cap layer over each ILD layer, except the uppermost. Thus, the claim requirement is satisfied regardless of which ILD layer (besides the uppermost) is construed to require the overlying cap layer. Specifically, Oshima discloses an ILD layer—the TEOS oxide films 9b, 11b, and 21a—over each of the metal traces 8, 10, 12, respectively. Ex. 1005 at [0031], [0047]. And, over the **TEOS oxide films 9b and 11b** (green) of the intermediate metallization layers (*i.e.*, excluding 21a) are **plasma oxide films 9c, 11c** (cyan), respectively. *Id.* at [0045], [0047]. Oshima discloses that these plasma oxide films are deposited to “prevent diffusion of moisture and hydrogen into the non-volatile memory cell area.” Ex. 1005 at [0036]; *see also id.* at [0048], Fig. 17. “The plasma oxide film 9c and 11c formed levelly on

each respective levelly formed TEOS oxide film 9b and 11b is given an adequate thickness to serve the function of **preventing diffusion of hydrogen** from the passivation film.” *Id.* at [0047], [0040]. “By adopting an interlayer insulation film structure” as described in Oshima, “it is possible to reliably suppress hydrogen diffusion from the plasma oxide film into circuit elements.” *Id.* at [0015]. Likewise, the ’455 patent, and its claimed oxide cap layer, concern the same use: “to significantly **reduce** the generation and **migration of hydrogen atoms/ions** into front-end structures.” Ex. 1001 at 11:10–17.

88. The plasma oxide films 9c and 11c are also “low-moisture.” As discussed with respect to limitation 1[e] above, the plasma oxide films 9c and 11c serve to “prevent diffusion of moisture and hydrogen into the non-volatile memory cell area.” *Id.* at [0036], [0048]; *see also id.* at [0040] (plasma oxide film 11c is formed “under the same conditions” and for the same reason as the plasma oxide film 9c). A POSITA would have readily recognized that the plasma oxide films must be low-moisture for them to serve the intended function of preventing hydrogen diffusion. This is further supported by the fact that the plasma oxide films 9c and 11c are silicon oxide films formed using silane as a main gas. Ex. 1006 at [0011]–[0012]. The use of silane results in low-moisture because less water is produced per unit of SiO₂, reducing the amount of water incorporated into the film. Ex. 1012 at 115 (“The SiH₄ based films with their low moisture content still dominate the logic

market”); Section V.B, *supra*. Deposition of a dense film from a gaseous environment containing less water vapor thus results in a low-moisture oxide, as required by the claim.

89. In my opinion, Oshima discloses this limitation. A plasma oxide film is a “**compact** insulating film” with a “thickness of 200 to 600 nm.” Ex. 1005 at [0009]; *id.* at [0050] (“the plasma oxide film is a compact film”); *id.* at [0034] (the plasma oxide film 9c “preferably has a thickness of 200 nm or greater”). The plasma oxide films 9c and 11c are thus “high-density” and have a minimum thickness of 100 Å (which is equal to 10 nm).

90. However, as for the third ILD layer (passivation film 21) associated with the uppermost metallization layer (metal trace 12), Oshima discloses that a cap layer is ***not*** formed, thus satisfying the “except an uppermost said metallization layer” limitation. *Id.* at Fig. 17. Moreover, Oshima teaches that, “as miniaturization progresses and the pitch of the topmost layer of trace consequently becomes narrower, it will **become impossible** to cover the trace in the topmost layer with plasma oxide film, which provides a poor coverage shape,” further supporting that there is no plasma oxide film (i.e., the claimed cap layer) over an uppermost metallization layer. *Id.* at [0034].

91. To the extent PO argues that a plasma nitride layer 21b formed over the TEOS oxide film 21a is a cap layer, such an argument would fail. The plasma nitride

layer 21b is not “oxide material,” which the claim requires of a cap layer. Indeed, a POSITA would have understood that Oshima’s plasma nitride layer 21b is not intended to and does not serve as a cap layer because Oshima is explicit that the plasma nitride film 21b is a source, rather than a blocker, of hydrogen. *Id.* at [0002] (“prevent the diffusion of hydrogen from the nitride film”); *see also id.* at [0005], [0015]. Accordingly, it is my opinion that Oshima discloses forming a cap layer over the ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer.

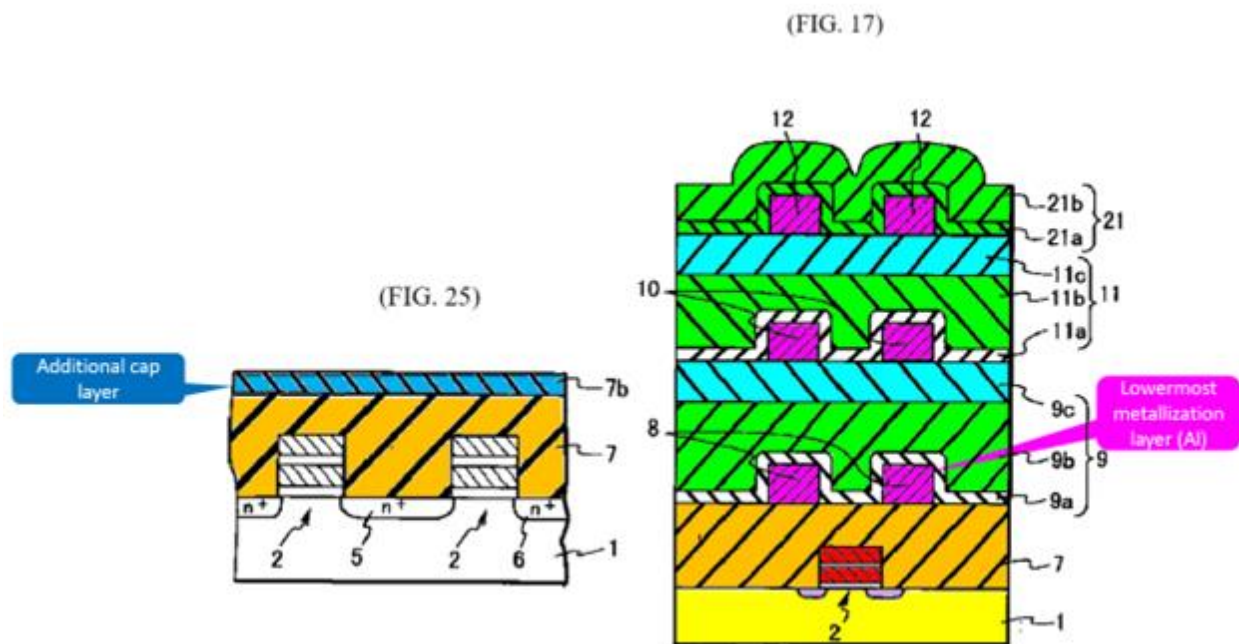
2. Claim 5.

- (a) The method of claim 1, wherein forming the pre-metal dielectric layer comprises forming a layer consisting essentially of one or more of BPSG and a TEOS-based oxide, and**

92. In my opinion, Oshima discloses this limitation because Oshima discloses depositing a BPSG film as an interlayer insulating film 7, which as discussed with respect to limitation 1[a] constitutes the claimed “pre-metal dielectric layer.” Ex. 1005 at [0022] (“A first interlayer insulation film 7 in the form of, for example, BPSG film, is deposited over the entire surface above the non-volatile memory cell 2, and then levelled.”).

- (b) wherein the method further comprises forming an additional cap layer between said pre-metal dielectric layer and a lowermost metallization layer of said plurality of metallization layers, wherein said additional cap layer consists of silane oxide.**

93. In my opinion, Oshima discloses this limitation. Oshima discloses additionally forming a “**plasma oxide film 7b**” (blue) on the surface of **interlayer insulating film 7** (“pre-metal dielectric layer”), which would be under the **metal trace 8** (“a lowermost metallization layer”) (magenta). Ex. 1005 at [0060] (“[I]t is also possible to form a plasma oxide film 7b on the surface of the first interlayer insulation film 7 of BPSG or the like.”); Fig. 25. The purpose of the plasma oxide film 7b, like the other plasma oxide films 9c, 11c, is to “more effectively prevent diffusion of hydrogen from the passivation film to the memory cells.” *Id.* The plasma oxide film 7b thus constitutes “an additional cap layer.”



94. The plasma oxide film 7b also “consists of silane oxide.” The ’455 patent defines “silane oxide” as “SiO₂ formed using silane.” Ex. 1001 at 2:10–11. As discussed above, Oshima discloses that “plasma oxide film” refers to “silicon

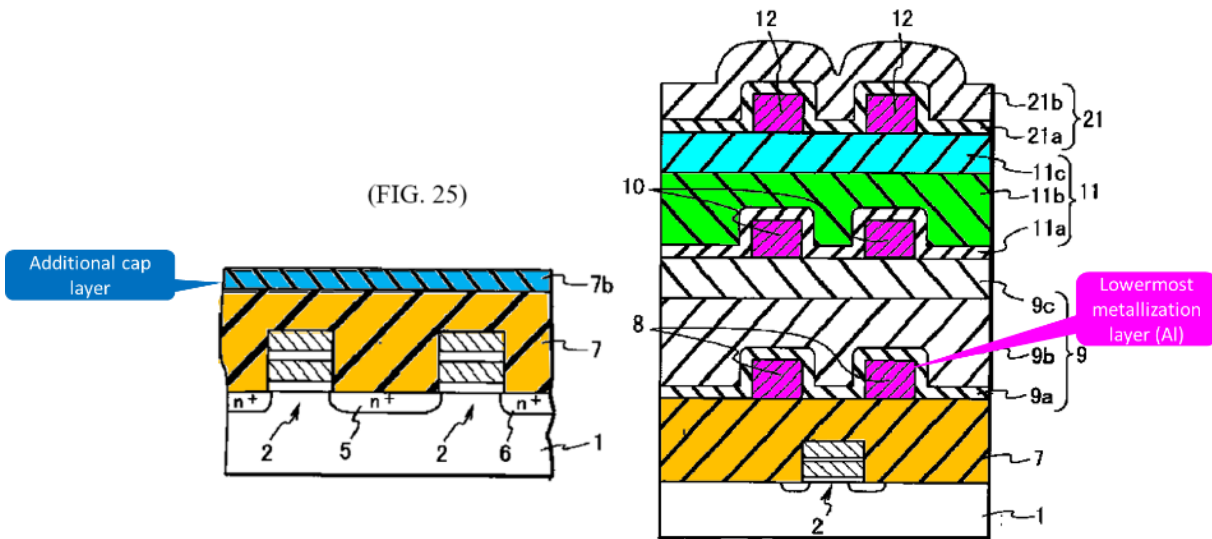
oxide film [] deposited ... by plasma CVD using silane (SiH₄) gas.” Ex. 1005 at [0002]. The plasma oxide film 7b thus “consists of silane oxide.”

3. Claim 6.

- (a) The method of claim 5, wherein forming a first patterned metal structure of a said lowermost metallization layer of said plurality of metallization layers comprises: forming a first aluminum layer on said additional cap layer; and**

95. In my opinion, Oshima discloses this limitation. Oshima teaches patterning a trace material film made of aluminum to form a metal trace 8, which constitutes the lowermost metallization. Ex. 1005 at [0022], Fig. 17. Because the additional cap layer (**plasma oxide film 7b**) is formed “on the surface” of the pre-metal dielectric (**insulation film 7**), it follows that the **metal trace 8** is then formed on the additional cap layer. *Id.* at [0060], Fig. 25. The metal trace 8 thus constitutes the claimed “first aluminum layer on said additional cap layer.”

(FIG. 17)



- (b) **etching a portion of said first aluminum layer such that an etch front passes through said first aluminum layer and enters said silane oxide layer, and such that said etching is terminated when a minimum thickness of said silane oxide layer between an upper surface of said pre-metal dielectric layer and said etch front is greater than 100 Å.**

96. In my opinion, Oshima discloses this limitation. At the time of the invention, the process by which over-etching is used to form metal trace was well-known. Specifically, it was well-known that metal trace (or interconnect) is formed by etching a metal film, whereby etching would continue beyond the metal film and reach the underlying material (*i.e.*, over-etch), but would stop such that some of the underlying material remains. For example, during an aluminum over-etch, some of the silane oxide underlying the aluminum layer is sacrificed to complete the definition of the metal trace of the aluminum layer. *E.g.*, Ex. 1015 at 1426, 1429–

1430 (“The overetch process should remove between 10 and 15 nm of underlying oxide to ensure a good line-to-line shorts yield.”). However, the etching would necessarily preserve sufficient amount of the underlying material (*e.g.*, silane oxide) so that it may serve its intended function (*e.g.*, to prevent hydrogen generation and migration/diffusion). *E.g.*, Ex. 1005 at [0005] (“In short, in order to prevent diffusion of hydrogen . . . it is desirable for the plasma oxide film 107a to have a thickness beyond a certain level.”). It would have been readily recognized that the amount of underlying material that remains after over-etch depends on the amount of underlying material that was initially deposited (before etching).

97. To effectively prevent diffusion of hydrogen and moisture, Oshima teaches the plasma oxide film (cap layer) in “a thickness of on the order of 100–200 nm is required,” and, in particular, “roughly 150 nm of plasma oxide film.” Ex. 1005 at [0023], [0034]. Thus, because a thickness of at least 100–150 nm is required, Oshima teaches that, when patterning a trace material film to form the metal trace 8, it would have been known in the art to over-etch into the silane oxide film (insulation layer 7) but stop the etch such that at least 100 Å (*i.e.*, 10 nm) thickness of the underlying silane oxide material remains between an upper surface of the pre-metal dielectric layer (insulating film 7) and the etch front.

4. Claim 9.

- (a) The method of claim 1, wherein forming said ILD layer of each said metallization layer comprises**

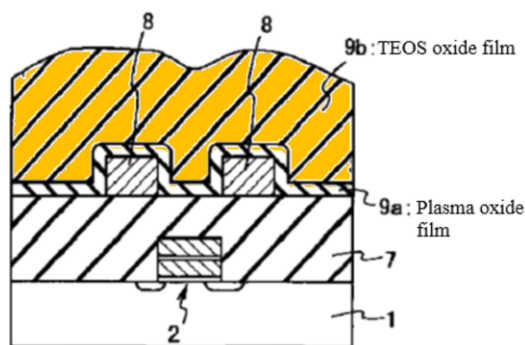
depositing a TEOS-based oxide USG/FSG, then annealing said deposited TEOS-based oxide, and then planarizing said annealed TEOS-based oxide before forming said cap layer.

98. In my opinion, Oshima anticipates claim 9. *First*, Oshima discloses that “forming said ILD layer of each said metallization layer comprises depositing a TEOS-based oxide USG/FSG.” The “said ILD layer of each said metallization layer” of claim 9 refers back to “an interlevel dielectric (ILD) layer” associated with “at least one of said metallization layers,” recited in claim 1. Oshima’s metal traces 8 and 10 constitute “at least one of said metallization layers,” and thus the TEOS oxide films 9b and 11b correspond to the “said ILD layer of each said metallization layer.” To form the TEOS oxide films over metal traces 8 and 10, Oshima discloses supplying fluorine gas (F₂) with TEOS. Ex. 1005 at [0023] (“TEOS oxide film 9b is deposited by CVD using Si(OC₂H₅)₄+F₂ as the source gas.”); *id.* at [0038]. A POSITA would have understood that this reaction requires an oxidizing reactant because, otherwise, no oxide can be deposited. The oxidizing reactant is typically O₂ or O₃ so that a pure oxide—in contrast to compound oxidants such as N₂O or NO, which lead to oxynitrites—can be grown. *See* ¶30, *supra*. The fluorine gas F₂ provides fluorine dopant so that fluorine-doped silicon oxide (*i.e.*, FSG) can be formed.

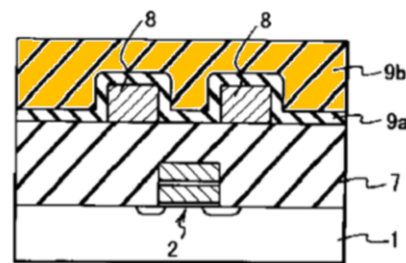
99. *Second*, Oshima discloses annealing the deposited TEOS-based oxide films 9b, and 11b and planarizing them before forming the cap layers (plasma oxide

films 9c and 11c). *Id.* at [0033] (“[A]lthough annealing was performed in the embodiment example after levelling the TEOS oxide film 9b, it is also acceptable to **perform annealing immediately after deposition.**”); *id.* at [0038] (TEOS oxide film 11 is formed “under the same conditions.”). Oshima discloses that CMP (chemical mechanical polishing) is performed to flatten the uneven surface of the TEOS oxide films. *Id.* at [0024], [0054], Figs. 2, 3, 9, 10. Because Oshima discloses performing “annealing immediately after deposition,” that is CMP is performed after annealing because annealing still required. For example, Oshima discloses that “anomalies” will occur if the TEOS oxide layer is not annealed and planarized before applying the plasma oxide film. *Id.* at [0032], [0033]. Therefore, the claim sequence of annealing and planarizing is satisfied.

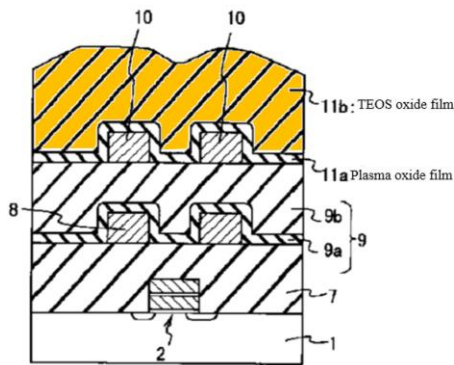
(FIG. 2)



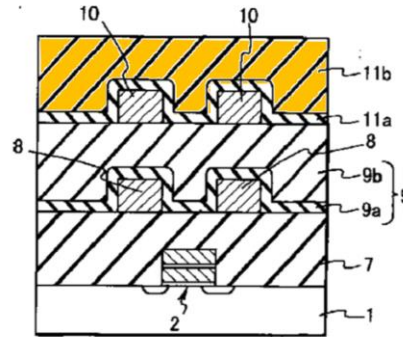
(FIG. 3)



(FIG. 9)



(FIG. 10)



5. Claim 19

(a) 19[pre] An image sensor comprising:

100. I understand that, as discussed in Section VIII.A, the preamble of claim 19 should be construed as not limiting because it merely describes an intended use (*i.e.*, an image sensor) of the claimed device.

(b) 19[a] a semiconductor substrate including a plurality of doped diffusion regions disposed below an upper substrate surface;

101. Oshima discloses this limitation for the same reasons discussed with respect to claim limitation 1[a]. See Section X.A.1(b).

(c) 19[b] a plurality of polycrystalline silicon structures disposed on the semiconductor substrate over the upper substrate surface;

102. Oshima discloses this limitation for the same reasons discussed with respect to claim limitation 1[a]. See Section X.A.1(b).

(d) 19[c] a pre-metal dielectric layer formed over the polycrystalline silicon structures; and

103. Oshima discloses this limitation for the same reasons discussed with respect to claim limitation 1[a]. See Section X.A.1(b).

(e) **19[d] a back-end metallization structure formed on the pre-metal dielectric layer, the back-end metallization structure including a plurality of metallization layers formed in a stack, each of the metallization layers including a patterned aluminum layer and an interlevel dielectric (ILD) layer comprising TEOS-based oxide that is formed over the patterned aluminum layer,**

104. In my opinion, Oshima discloses a back-end metallization structure that includes the claim elements. *First*, Oshima discloses a plurality of metallization layers formed in a stack, namely the trace material layers from which metal traces 8, 10, and 12 are patterned. Ex. 1005 at [0022], [0044], [0047], Fig. 17; see Section X.A.1(c).

105. *Second*, each of the metallization layers includes a patterned aluminum layer because, as discussed above, the metal traces 8, 10, and 12 are patterned from trace material layers made of aluminum. *Id.* at [0022], [0030], [0039]; see Section X.A.1(d).

106. *Third*, over the patterned aluminum layer (metal traces 8, 10, and 12), an interlevel dielectric (ILD) layer comprising TEOS-based oxide is formed. Specifically, TEOS oxide films 9b and 11b, and passivation film 21, are formed over metal traces 8, 10, and 12, respectively. *Id.* at [0023], [0038], [0031]; see Section X.A.1(e).

(f) 19[e] wherein at least one of the plurality of metallization layers includes a cap layer formed on the ILD layer, and,

19[f] wherein the cap layer of all of said plurality of metallization layers except an uppermost said metallization layer comprises a silane oxide layer having a minimum thickness of 100 Å.

107. In my opinion, Oshima discloses these limitations because, as discussed with respect to claim limitation 1[e], cap layers (plasma oxide films 9c and 11c) are formed on the TEOS oxide films 9b and 11b, respectively. Ex. 1005 at [0002], [0040], [0045]; *see* Section X.A.1(f).

108. Additionally, as discussed with respect to claim limitation 1[f], the cap layers of all of the metal traces except the uppermost metallization layer—namely, plasma oxide films 9c and 11c—comprise oxide material having a minimum thickness of 100–150 nm (*i.e.*, 1000–1500 Å). Ex. 1005 at [0002], [0009], [0034], [0036], [0038]; *see* Section 0. In particular, the plasma oxide films 9c and 11c are silicon oxide films formed using silane as a main gas, thus constituting a “silane oxide layer.” Ex. 1006 at [0011]–[0012]. Note, as discussed in Section X.A.1(f), the uppermost layer comprises a TEOS oxide film 21a and plasma nitride oxide 21b, neither of which is a silane oxide layer (or cap layer).

B. Ground 2: Oshima in view of Lee renders obvious claims 2, 3, 7

109. With respect to claims 2, 3, and 7, the only claim limitation that Oshima does not expressly disclose is generation of silane oxide by way of reacting silane

(SiH₄) gas with oxygen gas, which is required by claim limitations 2[c] and 7[b]. As discussed below, in my opinion, Lee discloses that limitation, and it would have been an obvious and trivial substitution to modify Oshima's method to use O₂ gas (instead of the N₂O gas, as Oshima discloses), thus rendering claims 2, 3, and 7 obvious.

1. Claim 2.

(a) 2[a] The method of claim 1, wherein forming said patterned metal structure of each of said plurality of metallization layers comprises forming an aluminum layer and then etching said aluminum layer,

110. In my opinion, Oshima discloses this limitation. *First*, Oshima discloses forming an aluminum layer because the material films from which the metal traces 8, 10, and 12 are patterned are made of aluminum. Ex. 1005 at [0022] (“400 nm of trace material film such as Al or the like is deposited, and a layer 1 trace 8 is formed by patterning.”); [0030] (“a layer 2 metal trace 10 is formed by depositing 600 nm of metal trace material such as Al or the like and patterning according to the standard method.”); [0022] (“The same manner of trace material film is used for the upper trace layer.”). *Second*, because Oshima discloses patterning the aluminum layers to form the metal traces 8, 10, and 12, it follows that Oshima discloses “etching” the aluminum layers. *See* Ex. 1017 (Frank) at 85-86 (describing that wet etching, which was initially used for patterning aluminum, was replaced by plasma-assisted etching processes); *see also* Ex. 1018 (Riley) at 1518

(“broad lines” are defined by wet etching, and “narrow lines must be defined by plasma etching”).

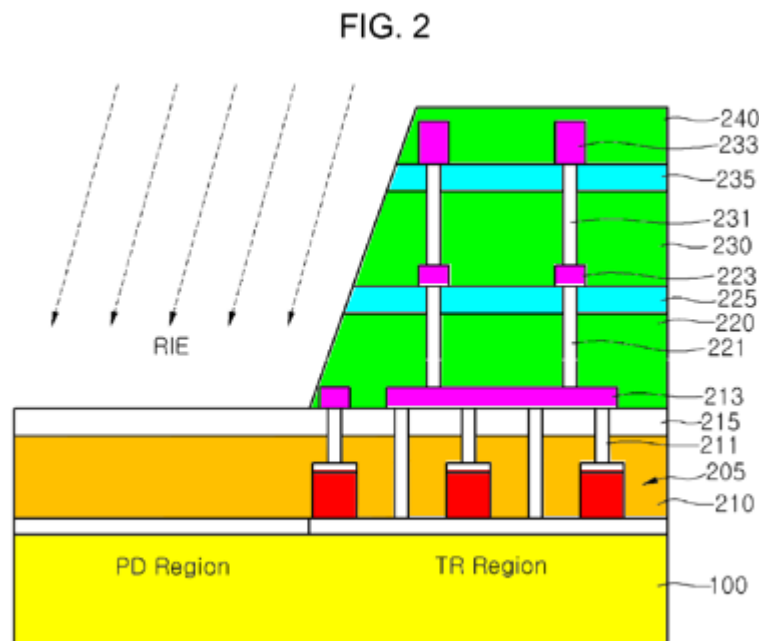
- (b) 2[b] wherein forming said ILD layer of at least one of said metallization layers comprises forming one or more of Undoped silicate glass (USG) and Fluorosilicate glass (FSG), and**

111. In my opinion, Oshima discloses this limitation. Oshima discloses supplying fluorine gas (F_2) with TEOS to form the disclosed TEOS oxide films. Ex. 1005 at [0023] (“TEOS oxide film 9b is deposited by CVD using $Si(OC_2H_5)_4 + F_2$ as the source gas.”), [0038] (same condition for film 11b). A POSITA would have understood that this reaction is performed using an oxidant gas (*e.g.*, N_2O , O_2 , O_3 , etc), resulting in the formation of a fluorine-doped silicon oxide, *i.e.*, FSG. Ex. 1001 at 1:55–61 (“The ILD and topside stack are typically formed using one or more of . . . Fluorosilicate glass (FSG) FSG is essentially SiO_2 containing fluorine”).

- (c) 2[c] wherein forming the cap layer over said ILD layer of said all of said plurality of metallization layers except said uppermost metallization layer comprises generating silane oxide by way of reacting silane (SiH_4) gas and oxygen (O_2) gas.**

112. In my opinion, Oshima discloses depositing the cap layers (plasma oxide film 9a and 9c) by reacting silane (SiH_4) gas with N_2O gas. Ex. 1005 at [0023] (“mixed gas containing at least SiH_4 and N_2O gas as the source gas”); *id.* at [0027] (plasma oxide film 9c is deposited “under the same conditions”).

113. Lee discloses reacting silane gas with oxygen (O₂) gas. Specifically, Lee discloses forming capping layer 225 and 235 (cyan) on dielectric layer 220 and 230 (green), respectively, using “a plasma silane [e.g., silicon dioxide formed by plasma-assisted CVD of silicon dioxide from silane and oxygen].” Ex. 1007 at [0027]; *see also id.* at [0031] (“a second capping layer 225 may be formed on the second dielectric layer 220 using plasma-SiH₄.”).



114. In my opinion, a POSITA would have found it obvious to form Oshima’s plasma oxide films 9a and 9c as silane oxide by reacting silane gas with **oxygen** gas, as disclosed in Lee. Oshima and Lee are in the analogous art of semiconductor fabrication, in particular the formation and arrangement of dielectric layers in a multi-metallization stack. Ex. 1005 at [0008]; Ex. 1007 at [0015], Fig. 3.

A POSITA would have looked to the complementary teachings of Lee when fabricating a stacked semiconductor device using Oshima's method.

115. The modification would have involved simply substituting the N_2O gas in Oshima's gas mixture with an oxygen source (*e.g.*, dioxygen). *Id.* A POSITA would have made the modification with reasonable expectation of success because formation of an oxide from a hydride requires reaction with an oxygen-bearing reactant, and replacing one oxidant (*e.g.*, N_2O) with another (*e.g.*, O_2 , O_3) does not affect the end result, *i.e.*, the formation of silicon oxide. As such, the modification would have been obvious to try.

116. Furthermore, a POSITA would have found such a modification to yield predictable benefits over using N_2O gas. For example, N_2O can cause nitrogen to become incorporated into the oxide, resulting in formation of silicon oxynitride (SiON), which has larger dielectric constant than silicon oxide (SiO_2). As Oshima expressly discloses, larger dielectric constant is disadvantageous because it increases the capacitance between the wirings. Ex. 1005 at [0026]. Moreover, due to its higher dielectric constant, SiON is more likely than SiO_2 to accumulate charges during plasma deposition on patterned interconnect, which is undesirable because the charges can dissipate through the metal interconnects to the underlying gate oxides and damage them (a phenomenon known as "antenna effect"). Ex. 1019 at 154.

Thus, a POSITA would have readily substituted an oxygen source for N₂O gas to ensure formation of SiO₂.

2. Claim 3.

- (a) The method of claim 2, wherein generating said silane oxide comprising forming a layer of said silane oxide having a thickness in the range of 500 Å to 5000 Å.**

117. In my opinion, Oshima discloses using a plasma oxide film as a compact film that has a thickness of 200 to 600 nm (*i.e.*, 2000 Å to 6000 Å). Ex. 1005 at [0009] (“[S]ilicon oxide film deposited by plasma CVD with silane as the primary source gas can be used as compact insulation film. Preferably, the compact insulation film has a film thickness of 200-600 nm”). In particular, Oshima discloses maintaining the plasma oxide films (*i.e.*, the claimed cap layer) at a sufficient thickness (*e.g.*, 500 nm) to prevent hydrogen diffusion. *Id.* at [0027]; *see also id.* at [0045] (film 11 is identical to film 9). Oshima’s method thus generates the silane oxide having a thickness in the claimed range of 500 Å to 5000 Å (which is equal to 50 nm to 500 nm).

3. Claim 7.

- (a) 7[a] The method of claim 6, further comprising: forming a first ILD layer of said lowermost metallization layer over said etched first aluminum layer, said first ILD layer comprising one or more of Undoped silicate glass (USG) and Fluorosilicate glass (FSG), and**

118. In my opinion, Oshima discloses depositing a TEOS based film 9b over the metal trace 8, which is the lowermost metallization layer. Ex. 1005 at [0023]; *see* Section X.A.3(a), *supra*. The TEOS based film 9b comprises FSG because, as discussed in Section X.B.1(b), the disclosed CVD chemistry (using $\text{Si}(\text{OC}_2\text{H}_5)_4 + \text{F}_2$ as the source gas) results in formation of FSG.

(b) 7[b] forming a first cap layer over said first ILD layer by generating silane oxide by way of reacting silane (SiH_4) gas and oxygen (O_2) gas, and

119. In my opinion, Oshima in view of Lee renders this limitation obvious. As discussed in Section X.B.1(c), it would have been obvious to form Oshima's plasma oxide film 9c as silane oxide by reacting silane gas with oxygen gas (rather than N_2O), as disclosed in Lee. The plasma oxide film 9c thus constitutes the claimed "first cap layer."

(c) 7[c] forming a second patterned aluminum structure of a second metallization layer of said plurality of metallization layers on said first cap layer, said forming comprising:

120. In my opinion, Oshima discloses this limitation because Oshima discloses patterning an aluminum film to form metal trace 10 over the first cap layer (plasma oxide film 9c). Ex. 1005 at [0030]. The metal trace 10 constitutes the claimed "second patterned aluminum structure."

(d) 7[d] forming a second aluminum layer on said first cap layer; and

121. As discussed above, Oshima discloses that metal trace 10 is patterned from metal trace material made of aluminum. Ex. 1005 at [0030].

- (e) **7[e] etching a portion of said second aluminum layer such that an etch front passes through said second aluminum layer and enters said first cap layer, and such that said etching is terminated when a minimum thickness of said first cap layer between an upper surface of said first ILD layer and said etch front is greater than 100 Å.**

122. In my opinion, Oshima discloses this limitation for the reasons discussed in Section X.A.3(b).

C. Ground 3: Oshima in view of Crook renders obvious claim 10

1. Claim 10.

- (a) **The method of claim 1, wherein forming said ILD layer of at least one of said metallization layers comprises depositing a TEOS-based oxide, and then processing said TEOS-based oxide in a hydrogen plasma before forming said cap layer.**

123. In my opinion, Oshima discloses depositing TEOS-based oxide films 9b and 11b over the metal traces 8 and 10; and, thus, Oshima discloses “forming said ILD layer of at least one of said metallization layers comprises deposition a TEOS-based oxide.” Sections X.A.1(e), X.A.1(f); Ex. 1005 at [0023], [0038]. Oshima also discloses treatment (*i.e.*, processing) of the TEOS-based oxide films “immediately after deposition,” and before forming the cap layers (*i.e.*, plasma oxide films 9c and 11c) to control moisture absorption by TEOS. *Id.* at [0033], [0038]; *see also id.* at [0024], [0054], Figs. 2, 3, 9, 10.

124. Crook discloses treating TEOS-based oxide with a hydrogen plasma to control moisture reabsorption after deposition at lower temperatures. Ex. 1008 at 1:33–56 (“The present invention provides a method of depositing a silicon dioxide film using PECVD in a chamber including supplying **TEOS, oxygen**, or a source thereof and hydrogen as precursors Whilst the precursors can be used in any suitable quantities, the inventors have used a ratio of **O₂:TEOS** of 10–20:1 based on sccm. The films made by the process disclosed herein **can further undergo a hydrogen plasma post deposition treatment step**”); cls. 1–2 (“A method of forming a silicon dioxide film on a substrate, including the steps of: supplying **TEOS** via a carrier gas, **supplying oxygen or a source of oxygen**” “A method according [to] claim 1 further comprising treating the deposited silicon dioxide with **a hydrogen plasma as a post deposition treatment**.”); *see also id.* at Fig. 2b, 2:15–17, 2:55–61.

125. A POSITA would have been motivated to combine the teachings of Oshima and Crook such that Oshima’s TEOS-based oxide films are treated with a hydrogen plasma, as disclosed by Crook. *First*, the references both relate to the field of semiconductor manufacturing, and the deposition of TEOS-based layers using CVD. Ex. 1005 at [0003], [0023], [0038]; Ex. 1020 at 1:4–7, 1:33–36, 1:52–54, cl. 1. *Second*, Crook provides a further solution to a problem acknowledged by Oshima: moisture absorption by TEOS. That is, Oshima discloses that “TEOS oxide film

tends to absorb moisture,” which has “known . . . adverse[] impact.” Ex. 1005 at [0003], [0036]. Oshima discloses using a source gas of TEOS and F₂ but notes that “[e]xcess fluorine can have the undesirable effect of causing increased absorption of moisture in the TEOS oxide film 9b.” *Id.* at [0023], [0032]. Moreover, while Oshima discloses moisture absorption may be controlled through annealing the TEOS oxide film at 300–450°C, Oshima also discloses that doing so may not be “strictly necessary” in “situations where it is possible to enact controls preventing problematic levels of moisture absorption during the manufacturing process”; thus, suggesting its disclosures to be combined with further moisture absorption control methods. *Id.* at [0033]. Crook provides a method (*i.e.*, post-deposition hydrogen plasma treatment) to control moisture absorption by TEOS during manufacturing; for example, in applications where deposition or treatment temperatures below 200°C are desired. Ex. 1008 at 1:14–32, 1:55–59 (“The films made by the process disclosed herein can further undergo a hydrogen plasma post deposition treatment step This step further suppresses reabsorption of moisture and reduces the leakage current.”); *see also id.* at Fig. 1a, 2:42–53. Thus, a POSITA would have combined Oshima with Crook to achieve the benefit of “further suppress[ing] reabsorption of moisture and reduc[ing] the leakage current,” particularly at a wide range of deposition or treatment temperatures. *Id.*

D. Ground 4: Nagai anticipates claims 1, 8, and 11

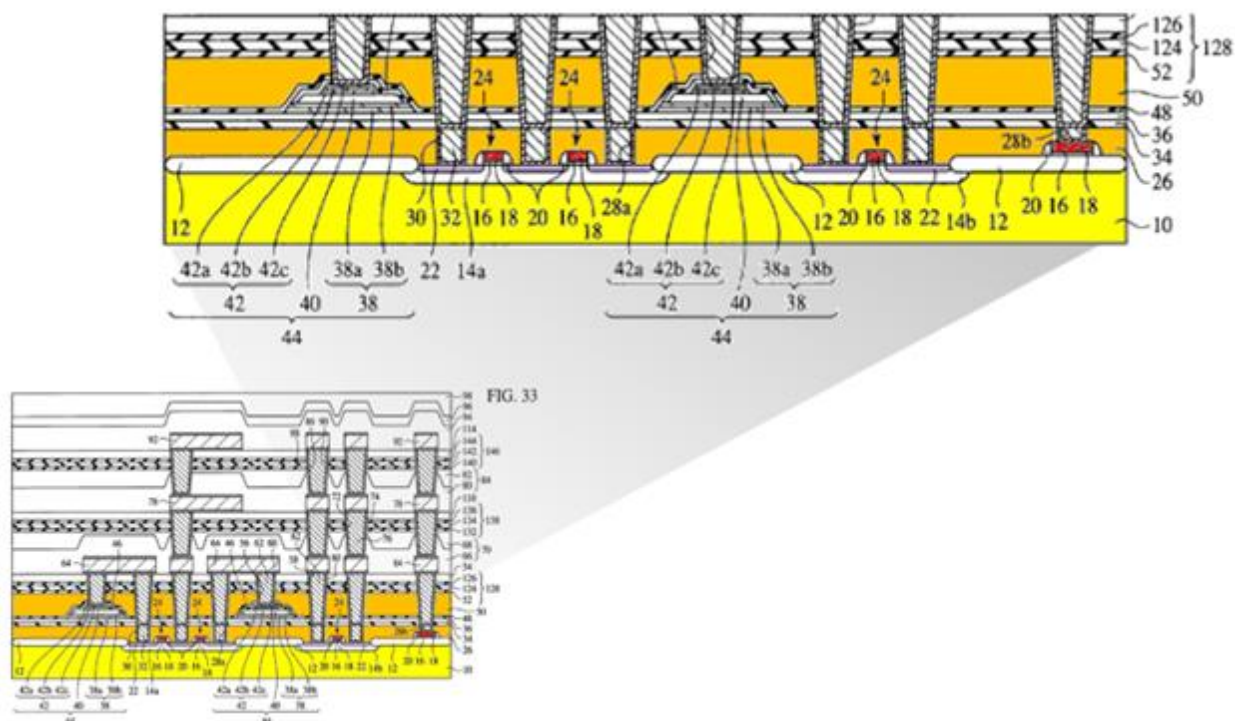
1. Claim 1

- (a) 1[pre] A method for fabricating a semiconductor integrated circuit, the method comprising:**

126. In my opinion, Nagai discloses the preamble to the extent it is limiting because Nagai discloses “a semiconductor device and a method for fabricating the semiconductor device.” Ex. 1006 at 1:18–19.

- (b) 1[a] generating front-end structures including one or more doped diffusion regions disposed in a semiconductor substrate, one or more polycrystalline silicon structures disposed over a surface of the substrate, and a pre-metal dielectric layer over the one or more polycrystalline silicon structures;**

127. In my opinion, Nagai discloses generating front-end structures including the claim elements as discussed below. *First*, Nagai discloses “one or more doped diffusion regions disposed in a semiconductor substrate.” Nagai discloses forming **source/drain diffused layer 22** (purple) in the **semiconductor substrate 10** (yellow). Ex. 1006 at 6:66–7:2, Fig. 33.



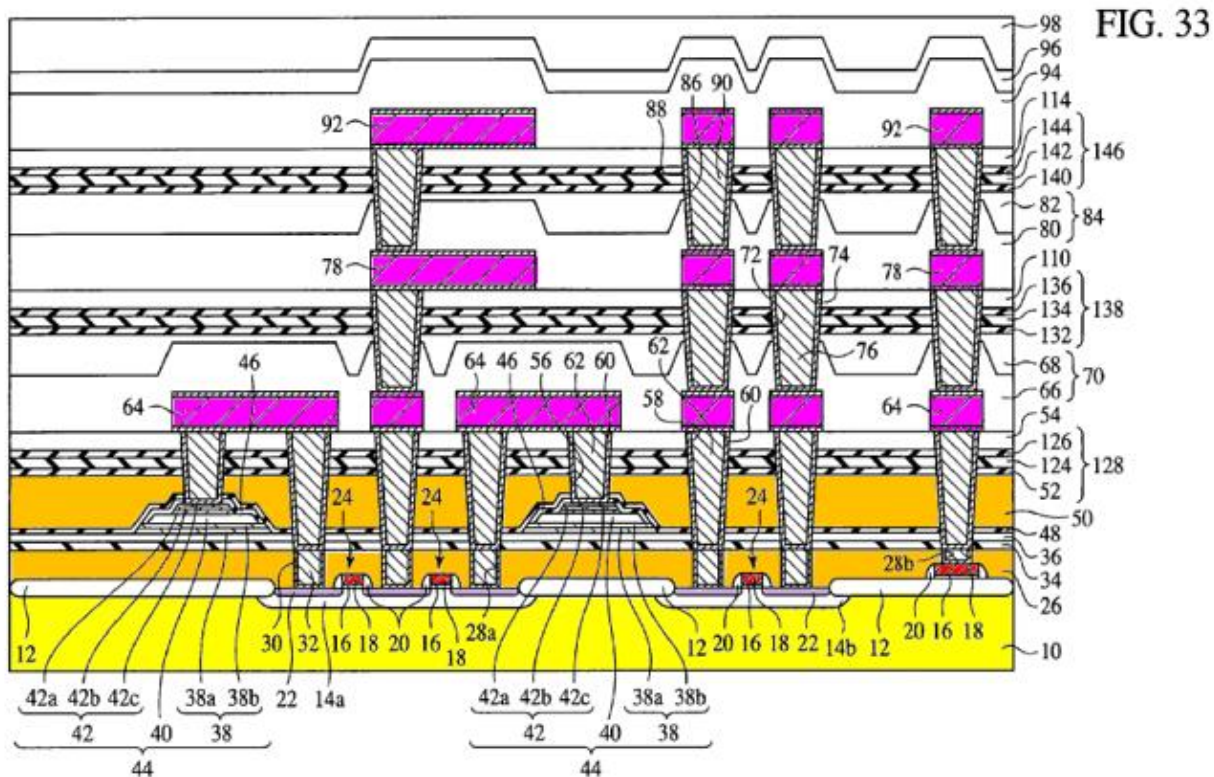
128. *Second*, Nagai discloses “one or more polycrystalline silicon structures disposed over a surface of the substrate.” Nagai discloses forming a **polycrystal silicon film 18** (red) and patterning the film to form gate electrodes. *Id.* at 17:39–44. Nagai thus discloses “one or more polycrystalline silicon structures disposed over a surface of the substrate.”

129. *Lastly*, Nagai discloses “a pre-metal dielectric layer over the one or more polycrystalline silicon structures.” **Inter-layer insulation films 26 and 50** (orange) are formed over the gate electrodes 18. *Id.* at 17:66–18:3, 7:1–3, 20:38–43. The interlayer insulation film 26 is formed from a SiON film and silicon oxide film. *Id.* at 17:66–18:3. The interlayer insulation film 50 is a silicon oxide film formed by plasma TEOS CVD. *Id.* at 20:38–43. The inter-layer insulation films 26

and 50, alone or together, constitute a “pre-metal dielectric layer over the one or more polycrystalline silicon structures.”

(c) 1[b] forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

130. In my opinion, Nagai discloses this limitation. Over the pre-metal dielectric layer (inter-layer insulation films 26 and 50), Nagai discloses forming layer films 64, 78, and 92 (magenta) from metallic materials including Ti, TiN, and AlCu. Ex. 1006 at 22:13–20, 23:21–26, 24:33–42, Fig. 33.



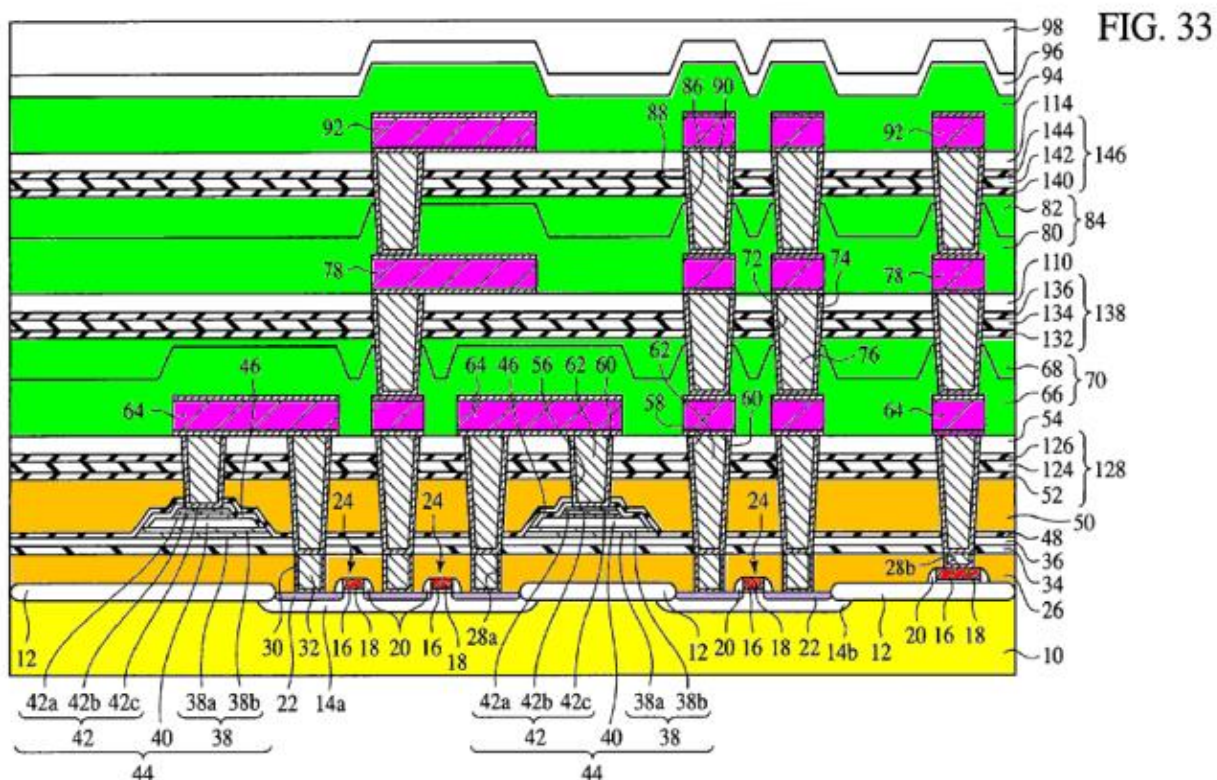
131. Further, as discussed below, Nagai discloses that forming one or more of the metal layers includes the steps discussed below with respect to limitations 1[c]–[e].

(d) 1[c] forming a patterned metal structure;

132. In my opinion, Nagai discloses patterning the layer films discussed above by photolithography to form the first, second, and third metal **interconnection 64, 78, and 92** (magenta). Ex. 1006 at 22:13–20, 23:21–26, 24:33–42, Fig. 33. Each metal interconnection constitutes the claimed “patterned metal structure.”

(e) 1[d] forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure; and

133. In my opinion, Nagai discloses forming an **inter-layer insulation film 70** (green), consisting of silicon oxide films 66 and 68, on the first metal interconnection 64; an **inter-layer insulation film 84** (green), consisting of silicon oxide films 80 and 82, on the second metal interconnection 78; and a **silicon oxide film 94** (green) on the third interconnection 92. Ex. 1006 at 22:21–34, 23:31–43, 24:43–49. Each silicon oxide film is formed by plasma TEOS CVD. *Id.* at 22:21–34, 23:31–43, 24:43–49. Accordingly, inter-layer insulation film 70, inter-layer insulation film 84, and the silicon oxide film 94 each constitute the claimed ILD layer.



- (f) 1[e] forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer,**
- 1[f] wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.**

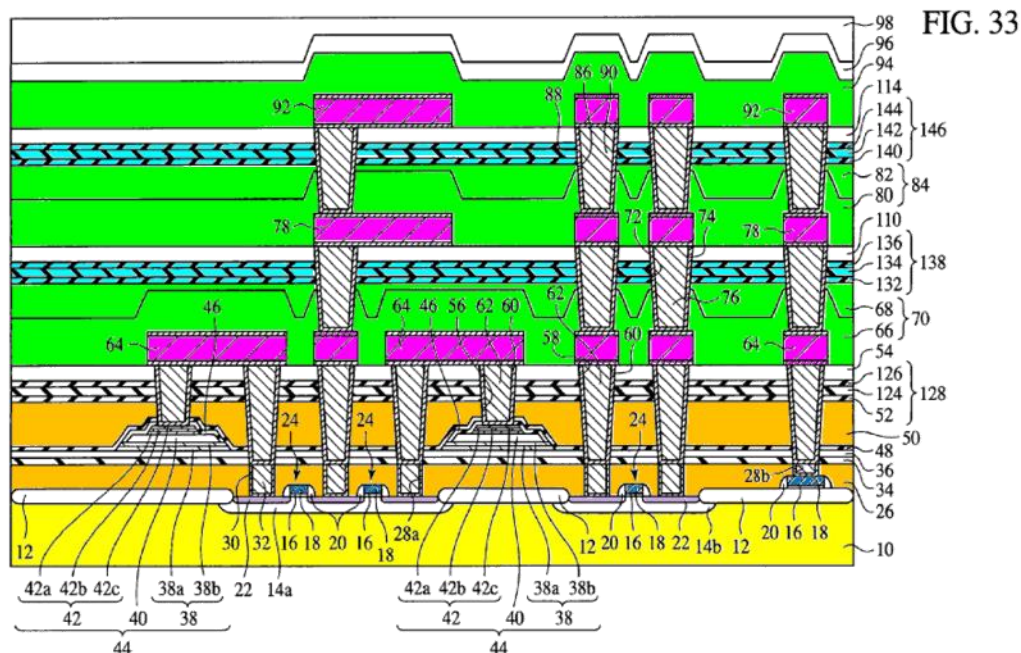
134. Nagai discloses these limitations and discloses the claimed cap layer over each ILD layer, except the uppermost. Thus, the claim requirement is satisfied regardless of which ILD layer (besides the uppermost) is construed to require the overlying cap layer. Specifically, Nagai discloses forming barrier films 138 and 146, over the first and second inter-layer insulating films 70 and 84, respectively. Ex. 1006 at 34:42–48, Fig. 33. Each barrier film 138 and 146 consists of

hydrogen/water diffusion preventing films 132/136 and 140/144 (cyan), which may be aluminum oxide films, that “sandwich” a stress mitigating film 134 and 142 (cyan), which may be silicon nitride oxide. *Id.* at 34:48–35:32.

135. Aluminum oxide, Al_2O_3 , is a “high-density” oxide material that has much higher density than any of the silicon oxides. A POSITA would have recognized that aluminum oxide is generally “low-moisture,” particularly according to Nagai’s teachings, which uses an alumina oxide film to prevent hydrogen/water diffusion. Ex. 1006 at 34:59–64, 35:18–23. Moreover, Nagai discloses the stress mitigating films in the barrier films are silicon nitride oxide (*id.* at 34:65–35:1, 35:24–27), which a POSITA would understand is the same material as silicon oxynitride. Silicon oxynitride (*i.e.*, silicon nitride oxide) is an embodiment of high-density, low-moisture content oxide material according to the claims of the ’455 patent. Ex. 1001 at 10:4–10. The barrier films serve to prevent diffusion of hydrogen and water into the capacitors 44. *Id.* at 35:37–45. Accordingly, in my opinion, the barrier films each constitute the claimed cap layer.

136. Nagai further discloses that each hydrogen/water diffusion preventing film and the stress mitigating film are 20–30 nm thick and 50–100 nm thick, respectively. Ex. 1006 at 34:49–58, 35:9–17. Because each barrier film has two hydrogen/water diffusion preventing films and one stress mitigating film, each

barrier film is 90–160 nm thick, which is equal to 900–1600 Å, thus, in my opinion, satisfying the “minimum thickness of 100 Å” limitation.



137. Moreover, Nagai discloses that a cap layer is **not** formed over the uppermost metallization layer, the third metal interconnection layer 92. *Id.* at Fig. 33. Neither the silicon nitride film 96 nor the polyimide resin film 98 is a cap layer because they are not “oxide material,” which the claim requires of a cap layer. *See* claim limitation 1[f], *infra*. Additionally, as discussed in Section X.A.1(f), it was known in the art that silicon nitride film can potentially create, rather than block, hydrogen, thus further supporting that the silicon nitride film 96 is not the claimed cap layer. Ex. 1005 at [0002] (“prevent the diffusion of hydrogen from the nitride film”), [0005] (plasma nitride film 21b is a source of hydrogen), [0015] (similar).

2. **Claim 8.**

- (a) **The method of claim 1, wherein forming the pre-metal dielectric layer comprises forming a layer consisting essentially of one or more of BPSG and a TEOS-based oxide, and**

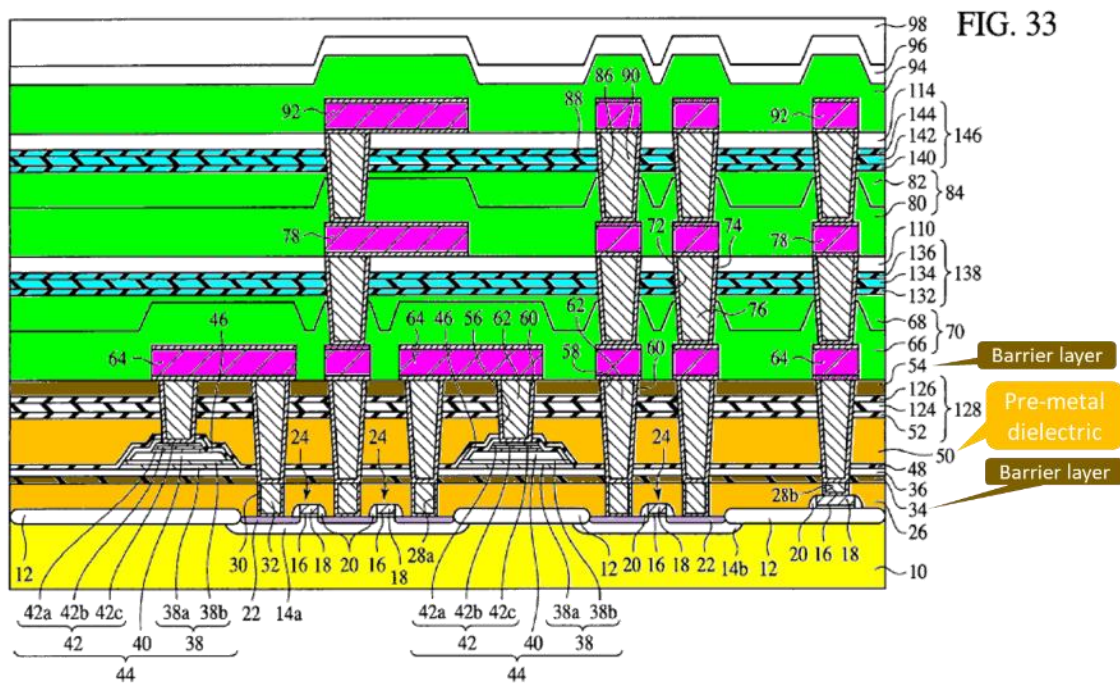
138. In my opinion, Nagai discloses this limitation because, as discussed in Section X.D.1(e), the interlayer insulation film 50 is a silicon oxide film formed by plasma TEOS CVD. Ex. 1006 at 20:38–43. Nagai’s method thus comprises forming a pre-metal dielectric layer that comprises essentially of a TEOS-based oxide.

- (b) **wherein the method further comprises a barrier layer disposed between said polycrystalline silicon structures and a lowermost metallization layer of said plurality of metallization layers, wherein said barrier layer comprises one of silicon nitride and silicon oxy-nitride.**

139. In my opinion, Nagai discloses this limitation. Nagai discloses forming an SiON (silicon oxy-nitride) film 34 on the inter-layer insulation film 26. Ex. 1006 at 7:16–20. SiON 34 serves to protect the underlying transistors and other IC elements by preventing oxidation of the surfaces of the conductor plugs 32. *Id.* at 13:19–29, 18:23–26; Ex. 1001 at 3:27–31. Nagai also discloses forming an insulation film 54 made of SiON film or silicon nitride film. Ex. 1006 at 21:19–25, Fig. 33.

140. The SiON film 34 and the insulation film 54 are both disposed between the polysilicon structures (gate electrodes 18) and a lowermost metallization layer (interconnect 64).

141. Accordingly, it is my opinion that the SiON film 34 and the insulation film 54 each constitute the claimed barrier layer.



3. Claim 11.

- (a) The method of claim 1, further comprising, after forming an uppermost ILD layer of an uppermost metallization layer of said plurality of metallization layers, annealing said uppermost ILD layer at temperature in the range 350-450°C. before performing a pad etch.

142. In my opinion, Nagai anticipates claim 11. Nagai teaches that, after an uppermost ILD layer (silicon oxide film 94) is formed on an uppermost metallization layer (interconnection 92), “thermal processing” is performed “for removing water, etc. from the insulation film 94 while changing the film quality of the insulation film 94 to thereby make the insulation film 94 difficult for water to intrude into.” Ex.

1006 at 24:50–60. The thermal processing is done, *e.g.*, at 350°C. *Id.* Similarly, the '455 patent discloses “anneal[ing] to remove residual water from the underlying TEOS-based oxide” and “to shift the diffusion of residual hydrogen to the outside of the wafer.” Ex. 1001 at 8:19–22, 15:41–42. Nagai’s thermal processing thus constitutes the claimed “annealing” step.

143. Moreover, Nagai discloses that annealing is done “before performing a pad etch.” After annealing of the uppermost ILD layer (film 94), a silicon nitride film 96 and polyimide film 98 are formed, and “openings . . . are formed in the polyimide film [98] down to the electrode pads,” *i.e.*, in both the silicon nitride film 96 and the insulation film 94, by photolithography. *Id.* at 25:8–10.¹ The formation of openings constitutes the claimed “pad etch.” See Ex. 1001 at 1:50–54 (describing that “pad etch” is performed “to make appropriate connections to the underlying IC, typically by way of connections to the uppermost patterned metal structure.”).

E. Ground 5: Nagai in view of Miyazaki renders obvious claim 12

1. Claim 12.

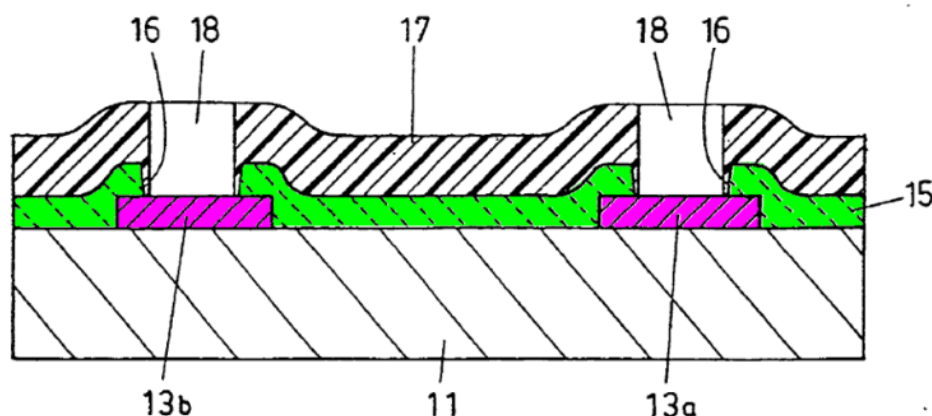
- (a) The method of claim 1, further comprising, after forming an uppermost ILD layer of an uppermost metallization layer of said plurality of metallization layers, performing a pad etch, and then annealing**

¹ Nagai’s reference to “the polyimide film 79” at 25:9 appears to be a typographical error. The context makes clear that the disclosure is about the polyimide film 98, and in fact there is no element (polyimide film or otherwise) that is numbered 79 in Nagai’s disclosures.

said uppermost ILD layer at temperature in the range 350-450°C.

144. In my opinion, Nagai in view of Miyazaki renders claim 12 obvious. As discussed in Section X.D.3, *supra*, Nagai discloses forming an uppermost ILD layer (silicon oxide film 94) of an uppermost metallization layer (interconnection 92) and then performing a pad etch (forming openings to the electrode pads by photolithography). It would have been obvious to combine Nagai with Miyazaki such that Nagai's uppermost ILD layer (silicon oxide film 94) is annealed at temperature in the range 350–450°C. Miyazaki teaches forming a silicon oxide protection film 15 over metal interconnections 13a and 13b and opening the protection film to expose the lower layer interconnections 13a and 13b. Ex. 1009 at [0030], [0033], Fig. 2. After a polyimide precursor 17 is deposited and opened, annealing is performed for 30 minutes at a temperature of 350°C to 400°C in the air atmosphere or a nitrogen atmosphere using a high-temperature furnace. *Id.* at [0034]-[0036], Fig. 3. Miyazaki's annealing step thus constitutes the claimed post-pad etch “annealing” step. It would have been obvious for a POSITA to anneal Nagai's uppermost ILD layer (silicon oxide film 94) after a pad etch, as taught by Miyazaki.

F I G. 2



145. A POSITA would have been motivated to combine the teachings of Nagai and Miyazaki. *First*, the references are analogous art because they are both in the field of manufacturing of a semiconductor device having a multilayer wiring structure and address the formation of an interlayer insulation film. Ex. 1006 at 1:18–19, 24:43–49; Ex. 1009 at [0001], [0015].

146. *Second*, after forming the polyimide film 98 and creating openings (through the films 94, 96, and 98) to the electrode pads on the uppermost metal layer 92 in accordance with Nagai’s method (Ex. 1006 at 25:6–10), a POSITA would have looked to Miyazaki for guidance on subsequent steps to enhance the device’s characteristics. Miyazaki’s teachings about annealing would have naturally followed the formation of openings in Nagai’s polyimide film 98. Indeed, Miyazaki’s annealing step is performed after a polyimide film (polyimide precursor 17) is deposited over the protection film 15 and thus is complementary to the formation of the polyimide film 98 in Nagai’s method.

147. *Third*, the modification would have been trivial. Annealing was a well-known technique that was employed in semiconductor fabrication for over a decade before the alleged invention of the '455 patent. Ex. 1013 at 393–396. The modification would thus have entailed nothing more than adding an annealing step after Nagai's pad etch (through the films 94, 96, and 98) is performed.

148. *Fourth*, a POSITA would have found the modification to yield a predictable benefit. Miyazaki discloses performing post-pad etch annealing to increase the insulation resistance of an interlayer insulation film. Ex. 1009 at [0022]. A POSITA would have understood that adding the annealing step to Nagai's method realizes such a benefit and increases the reliability of a semiconductor device.

F. Ground 6: Nagai in view of Lee renders obvious claim 15

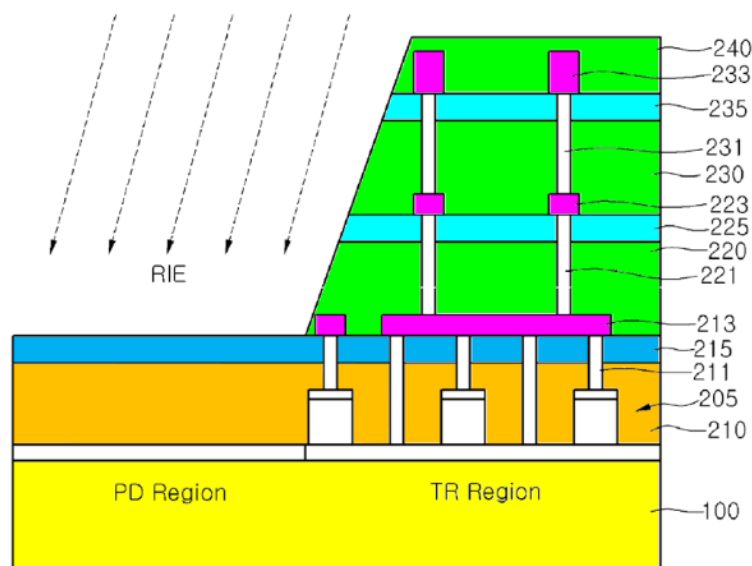
1. Claim 15.

- (a) The method of claim 1, wherein fabricating said semiconductor integrated circuit comprises fabricating one of a CMOS image sensor (CIS) and a charge-coupled device (CCD).**

149. In my opinion, Nagai in view of Lee renders claim 15 obvious. Lee discloses methods for fabricating a semiconductor integrated circuit of a CMOS or CCD image sensor. Ex. 1007 at [0003], [0006]; *see* Section IX.C, *supra*. In particular, Lee discloses forming a transistor region (TR) on a substrate and then forming a photo diode region (PD) at one side of the TR region with a relatively deep N-type ion implantation layer and a relatively shallow P-type ion implantation

layer. *Id.* at [0024]–[0025], Fig. 2. A PD region is where a photodiode is formed to convert a light signal into an electrical signal, and a TR processes the converted electrical signal. *Id.* at [0004]. Dielectric layers are formed over both regions and then selectively removed on the PD region such that only the first **dielectric layer 210** (orange) and the first **capping layer 215** (blue) remain on the PD region. *Id.* at [0026], [0036]–[0038], Fig. 2.

FIG. 2



150. It would have been obvious to modify Nagai's fabrication method such that a PD region, as taught by Lee, is formed at one side of Nagai's device. A POSITA would have been motivated to combine the teachings of Nagai and Lee. *First*, the references are analogous art because they are both in the field of semiconductor fabrication, in particular the formation and arrangement of dielectric

layers in a multi-metallization stack. Ex. 1006 at 1:18–23, Fig. 33; Ex. 1007 at [0015], Fig. 3.

151. *Second*, a POSITA would have applied Lee's teachings to Nagai's method to fabricate a CIS or CCD with reasonable expectation of success. A POSITA would have understood that the techniques Nagai teaches to address hydrogen diffusion are equally applicable to fabrication of CIS or CCD semiconductor devices. This is because CIS and CCD sensors must store accumulated charge until it is read; hydrogen diffusion from the back-end processes will have an adverse effect on the front end, in particular on the sensor's ability to retain charges, just as the multi-metallization layer semiconductor devices of Nagai. A POSITA would have thus found that forming a photodiode region in the semiconductor devices of Nagai in the manner disclosed by Lee yields a predictable result, *i.e.*, a CIS or CCD device less susceptible to hydrogen diffusion.

152. A POSITA would also have found such a modification to be trivial. Lee discloses complementary details on how to form a photodiode region alongside a transistor region such that the semiconductor device can convert an optical image to electrical signals, either as a CCD or CMOS. Ex. 1007 at [0003]–[0004]. It would have been well within the knowledge and expertise of a POSITA to follow Lee's teachings to add photodiodes in Nagai's semiconductor devices to fabricate a CMOS or CCD image sensor. Indeed, there is nothing in the specification or the claims of

the '455 patent suggesting that fabricating a CMOS or CCD image sensor using the recited steps of claim 1 would have involved an additional challenge beyond a POSITA's skillset and knowledge.

G. Ground 7: Nagai in view of Wang renders obvious claim 16

1. Claim 16.

(a) The method of claim 1, wherein fabricating said semiconductor integrated circuit comprises fabricating a radiation detector.

153. In my opinion, Nagai in view of Wang renders this claim obvious. Wang discloses a semiconductor device 100 with a substrate 110, which “may include various p-type doped regions and/or n-type doped regions configured and coupled to form various devices and functional features.” Ex. 1010 at 2:12–15, Fig. 4. For example, Wang discloses disposing an imaging sensor element 120 (purple) in the substrate 110 and diffusing or implanting dopants to form a light-sensing region, which is “operable to receive light (or other form of radiation energy from an object to be imaged).” *Id.* at 2:21–31, Fig. 4. Wang thus discloses “fabricating a radiation detector.”

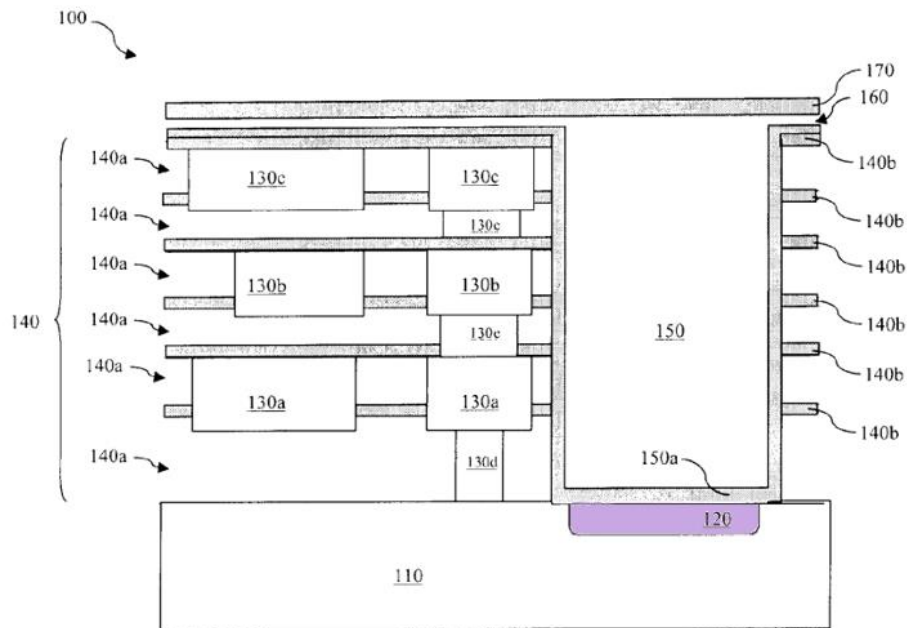


Fig. 4

154. In my opinion, it would have been obvious to modify Nagai's method to fabricate a radiation detector, as disclosed in Wang. Wang is analogous art because it is directed to fabrication of a semiconductor device with multiple metallization and inter-metal dielectric layers. *Id.* at 1:15–20.

155. A POSITA would have modified Nagai's method with a reasonable expectation of success. As discussed with respect to claim 15 above, the invention of Nagai is directly applicable to light sensing semiconductor devices. *See* Section X.F.1, *supra*. Indeed, Wang expressly states that a desire existed to advance light sensing using semiconductor technology. Ex. 1010 at 1:11–13. As such, a POSITA would have understood that employing Nagai's method to fabricate a radiation detector as disclosed in Wang achieves predictable benefits (*i.e.*, reducing adverse

effect of hydrogen diffusion on the front end, in particular on the sensor's ability to retain charges).

156. Furthermore, the modification would have been trivial and readily performed in accordance with Wang's teachings. For example, the modification would have simply entailed adding a conventional sensing device such as a photodiode in Nagai's substrate and doping, either by ion implantation or diffusion, Nagai's source/drain diffused layer 22 to form a light-sensing region. Ex. 1010 at 2:21–38.

H. Ground 8: Nagai in view of Omi renders obvious claims 17 and 18

1. Claim 17.

(a) 17[pre] A method for fabricating a semiconductor integrated circuit, the method comprising:

157. To the extent the preamble is limiting, it is disclosed by Nagai (Section X.D.1).

(b) 17[a] generating front-end structures including one or more doped diffusion regions disposed in a semiconductor substrate, one or more polycrystalline silicon structures disposed over a surface of the substrate, and a pre-metal dielectric layer over the one or more polycrystalline silicon structures;

158. Nagai discloses this limitation for the same reasons discussed in Section X.D.1(b).

(c) 17[b] forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

159. Nagai discloses this limitation for the same reasons discussed in Section X.D.1(c).

(d) 17[c] forming a patterned metal structure;

160. Nagai discloses this limitation for the same reasons discussed in Section X.D.1(d).

161. Omi also discloses depositing at least one aluminum film, from which inter-pixel light shielding aluminum is formed by etching the aluminum film. Ex. 1011 at 14:42–51, 14:57–62. Omi discloses that, when inter-pixel light shielding aluminum is formed from etching the second aluminum film, aluminum dummy interconnects may also be simultaneously formed. *Id.* at 14:57–62.

(e) 17[d] forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure; and

162. Nagai discloses this limitation for the same reasons discussed in Section X.D.1(e), *supra*. Omi also discloses this limitation because Omi discloses forming an **insulating film 103A of TEOS** (green) over the inter-pixel light shielding aluminum 113 (the claimed “patterned metal structure”). *Id.* at 14:33–56; Fig. 6B.

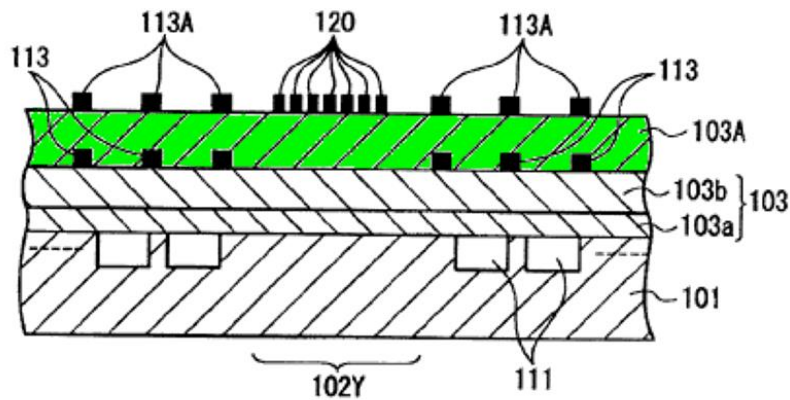


FIG. 6B

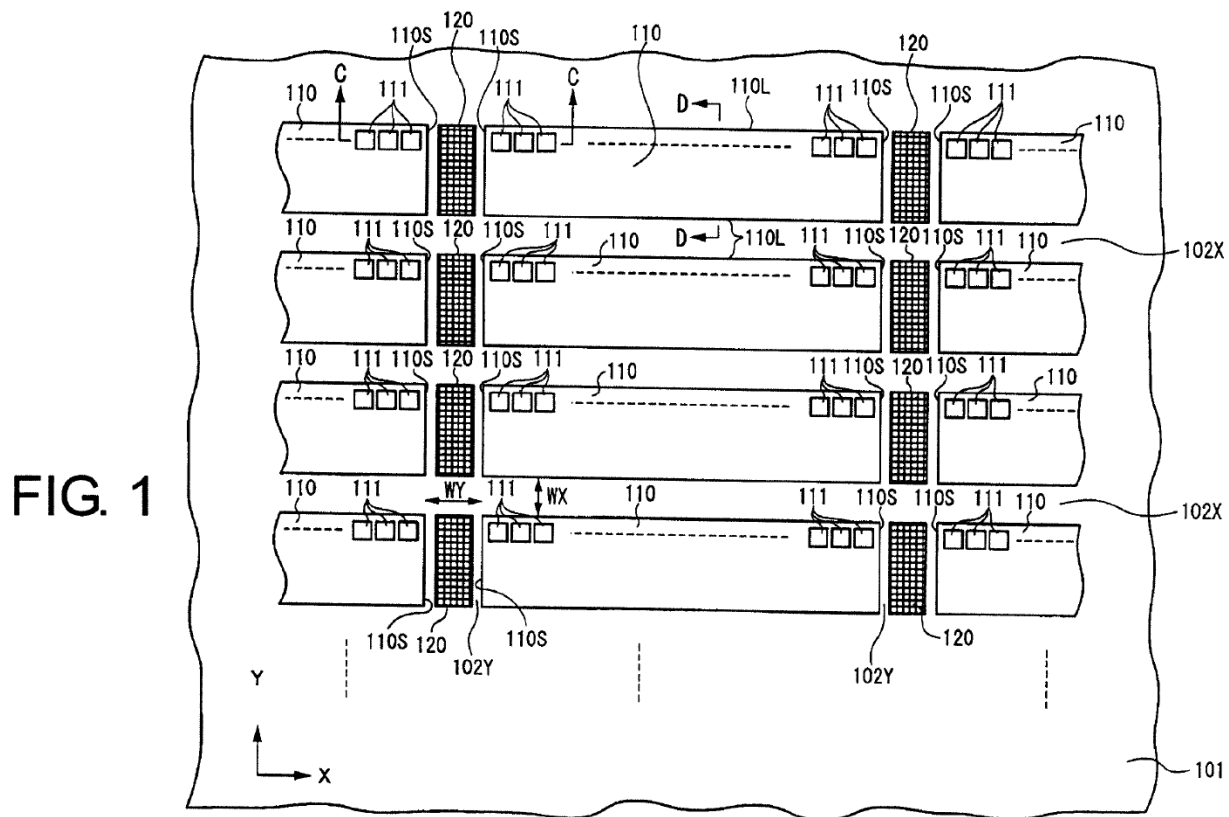
- (f) 17[e] forming a cap layer over the ILD layer,
- 17[f] wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å,

163. Nagai discloses these limitations for the same reasons discussed in Section X.D.1(f).

- (g) 17[g] wherein said semiconductor integrated circuit comprises an array of image sensing pixels disposed inside a rectangular imaging region of said semiconductor substrate, and

164. In my opinion, it would have been obvious to modify Nagai's semiconductor integrated circuit in view of Omi such that it includes "an array of image sensing pixels disposed inside a rectangular imaging region of said semiconductor substrate." Omi discloses a semiconductor integrated circuit in which "a plurality of line image sensor ICs 110 are formed on the surface of a semiconductor substrate (semiconductor wafer) 101." Ex. 1011 at 1:28–31. Image

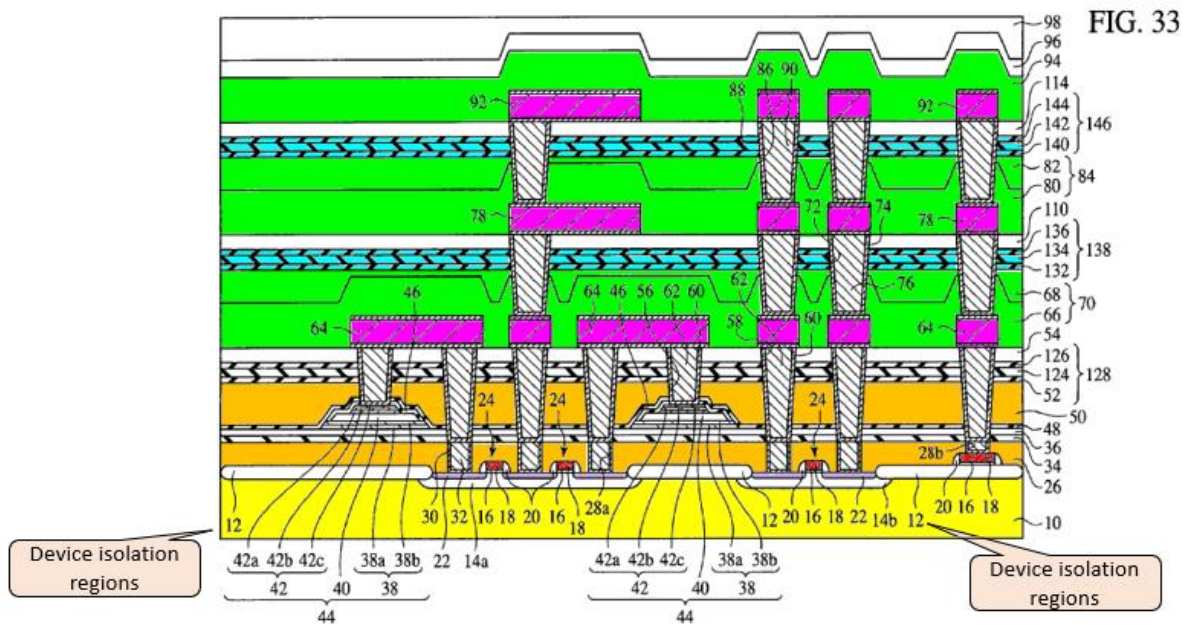
sensor ICs, whether CMOS or CCD (see Ex. 1007 at [0003]), comprise “a plurality of (e.g., 400) photoelectric conversion elements (light-receiving elements, **pixels**),” *i.e.*, an array image sensing pixels. *Id.* at 1:24–32. Furthermore, the photoelectric conversion elements 111 “are placed so as to be aligned in a row in a longitudinal direction,” resulting in the image sensor IC 110 having an “elongated rectangular shape.” Ex. 1011 at 1:54–61; *see also id.* at cls. 1–3 (“a plurality of rectangular line image sensor ICs formed on a surface of the semiconductor substrate”), Fig. 1. Thus, Omi discloses “an array of image sensing pixels disposed inside a rectangular region of said semiconductor substrate.”



165. A POSITA would have been motivated to combine the teachings of Nagai with Omi. Both references are analogous art, directed to semiconductor fabrication, and particularly the formation of metallization layers and inter-layers. *E.g.*, Ex. 1006 at 1:18–23, Fig. 33; Ex. 1011 at 1:11–21. For example, both Nagai and Omi teach depositing insulating/insulation films using TEOS between metal layers. *E.g.*, Ex. 1006 at 21:19–21 (“Then, the insulation film 54 is formed by plasma TEOS CVD.”); Ex. 1011 at 14:46–58 (e.g., “Next, an insulating film 103A of tetra ethoxy silane (TEOS) is deposited . . .”).

166. A POSITA would have made the modification with reasonable expectation of success. A POSITA would have understood that the techniques Nagai teaches to address hydrogen diffusion, *e.g.*, by forming, depositing, and treating film materials, are equally applicable to fabrication of image sensor semiconductor devices. Image sensor devices must store accumulated charge until it is read; hydrogen diffusion from the back-end processes will have an adverse effect on the front end, in particular on the sensor’s ability to retain charges, just as the multi-metallization layer semiconductor devices of Nagai. As such, a POSITA would have found it beneficial to utilize Nagai’s teachings to construct an image sensor IC by disposing image sensing pixels in Nagai’s semiconductor substrate 10, as disclosed in Omi.

167. The modification would have been well within the knowledge and expertise of a POSITA. Omi discloses forming the photoelectric conversion elements 111 by ion implantation and arranging them in a longitudinal direction in an image sensor IC 110. Ex. 1011 at 9:35-47, 13:46-54. Following Omi's teachings, a POSITA would have understood that image pixels could be formed, for example, in the substrate occupied by Nagai's device isolation regions 12, adjacent to wells 14a and 14b.



- (h) 17[h] wherein forming said patterned metal structure of at least one of said plurality of metallization layers comprises forming functional patterned aluminum structures over an interior of said rectangular imaging region, and forming non-functional patterned aluminum structures over an exterior peripheral region surrounding said rectangular imaging region.

168. In my opinion, Omi discloses every element of this limitation, and it would have been obvious to apply Omi's disclosures to Nagai's device. As discussed in Section X.H.1(d), *supra*, Omi discloses forming inter-pixel light shielding aluminum 113 and 113A from etching a first and second aluminum film, respectively. Inter-pixel light shielding aluminum 113 and 113A is "placed at a position . . . in the region where the line image sensor ICs 110 are formed" and, more specifically, "between adjacent photoelectric conversion elements 111." Ex. 1011 at 14:46–51, 14:57–62, Fig. 6C. As discussed in Section X.H.1(g), *supra*, the image sensor ICs are placed in a rectangular formation. Thus, the inter-pixel light shielding aluminum constitutes "functional patterned aluminum structures" formed "over an interior of said rectangular imaging region."

169. Omi further discloses that, simultaneously with the formation of light shielding structure 113A, "[a] pattern of dummy interconnects 120 is formed." *Id.* at Abstract, 14:57–62; *see also id.* at 11:28–34. The dummy interconnects are "made of aluminum" and formed on the side of image sensor ICs that are not facing any other image sensor IC in the array. *Id.*; *id.* at 10:24–32. Specifically, the dummy interconnects 120 are formed on the scribe lines 102Y, which are cut to produce independent image sensor ICs. *Id.* at 12:26–40, 14:61–62, 15:6–9, Fig. 6C. The dummy interconnects 120 thus constitute "non-functional patterned aluminum

structures over an exterior peripheral region surrounding said rectangular imaging region.” Thus, Omi discloses every element of this limitation.

170. In my opinion, in Nagai’s device, after disposing an array of photoelectric conversion elements (pixels) in a rectangular imaging region as discussed with respect to claim limitation 17(g), it would have been obvious to form the claimed “functional” and “non-functional” patterned aluminum structures in view of Omi. Photoconversion in the areas between pixels is problematic because it would result in generation of carriers that can drift into adjacent pixels and alter the light intensity detected. As such, to enable light shielding of the areas between pixels for top-side illumination and prevent unwanted photoconversion, the “functional” patterned aluminum structures (light shielding aluminum 113 and 113A) would have been necessarily added, for example in the silicon oxide layer 94 of Nagai’s device, over an interior of the rectangular imaging region (*i.e.*, where the pixels are disposed).

171. With respect to the “non-functional” patterned aluminum structures, Omi discloses temporarily forming dummy interconnects 120 in the gaps that separate the image sensor ICs to improve evenness of light-receiving surface and hence the performance of an image sensor IC. *Id.* at 3:29-45, 4:1-31, Fig. 1. A POSITA would have obtained the same predictable benefit—*i.e.*, more even light-receiving surface of photoelectric conversion element—by adding the dummy

aluminum structures in, *e.g.*, the silicon oxide layer 94 during the fabrication of Nagai's device.

2. Claim 18.

- (a) The method of claim 17, further comprising, after forming said functional and non-functional patterned aluminum structures, performing an anneal, and then removing said non-functional patterned aluminum structures.**

172. In my opinion, Nagai in view of Omi renders claim 18 obvious. *First*, Omi discloses “after forming said functional and non-functional patterned aluminum structures, performing an anneal” because, after forming the inter-pixel light shielding aluminum 113A and aluminum dummy interconnects 120 (as discussed Section X.H.1(d), *supra*), a protective film made of silicon nitride 104 is formed over the aluminum structures using “plasma CVD.” Ex. 1011 at 14:63-67.

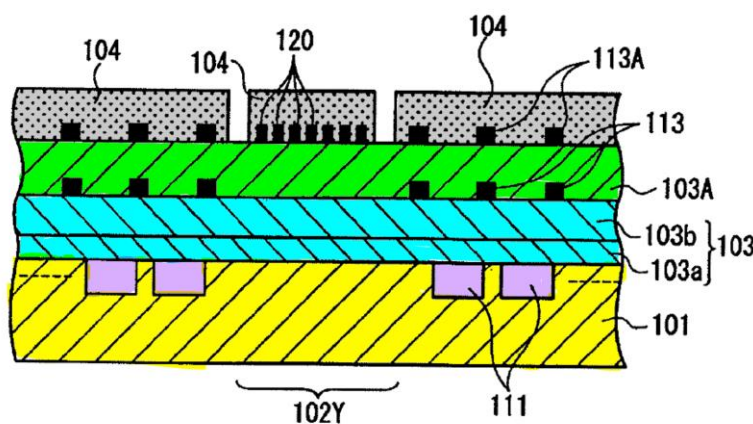


FIG. 6C

173. A POSITA at the time of the '455 patent would have understood that Omi's “plasma CVD” involves annealing, *i.e.*, altering of chemical or physical

properties by energizing (*e.g.*, thermally or electrically) the material. For example, plasma CVD of nitride is done at elevated temperature and involves bombarding of gas ions on the surface where the nitride film is deposited. Plasma CVD includes annealing because the wafer is placed in a heated plasma reactor to cause energetic ions to dissipate energy on the wafer surface.

174. *Second*, Omi discloses the remaining limitation, *i.e.*, “then removing said non-functional patterned aluminum structures,” because Omi discloses that, after the plasma CVD process, the dummy interconnects (*i.e.*, the claimed “non-functional patterned aluminum structures”) are cut to produce independent line image sensor ICs. Ex. 1011 at 15:6-9. When the dummy interconnects are “cut,” they are “removed,” as required by the claim, leaving only the functional patterned aluminum structures. Accordingly, Nagai in view of Omi renders obvious claim 18.

XI. CONCLUSION

175. For the aforementioned reasons, in my opinion, to a person of ordinary skill in the art, the Challenged Claims of the '455 patent are invalid in view of the prior art.

176. I reserve the right to respond to set forth opinions on secondary considerations of non-obviousness, to the extent Patent Owner asserts them.

177. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. § 1001.

Date: December 15, 2022

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Konstantinos P. Giapis', written over a horizontal line.

Dr. Konstantinos P. Giapis