Trials@uspto.gov
571-272-7822

Paper 7
Date: July 12, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,
Petitioner,

v.

ALIDOUBLE, INC.,
Patent Owner.

IPR2023-00373
Patent 9,431,455 B2

Before KRISTINA M. KALAN, CHRISTOPHER M. KAISER, and JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

A. Background and Summary

Taiwan Semiconductor Manufacturing Company Limited ("Petitioner") filed a petition for an *inter partes* review (Paper 1 ("Pet.")) challenging claims 1–3, 5–12, and 15–19 of U.S. Patent No. 9,431,455 B2 (Ex. 1001 ("the '455 patent")). Alidouble, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp.").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2022). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons set forth below, we determine the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Accordingly, we institute an *inter partes* review.

B. Real Parties-in-Interest

Each party identifies itself as the real party-in-interest. Pet. 82; Paper 3, 1.

C. Related Matters

The parties identify *Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Limited*, Case No. 2:21-cv-00452-JRG (E.D. Tex.), and *Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Limited*, Case No. 2:22-cv-00298-JRG (E.D. Tex.), as related matters. Pet. 82; Paper 3, 1.

D. The '455 Patent

The '455 patent, titled "Back-End Processing Using Low-Moisture Content Oxide Cap Layer," issued on August 30, 2016. Ex. 1001, codes (45), (54). The patent "relates to semiconductor fabrications processes, and more particularly to back-end processing in a way that controls hydrogen production." *Id.* at 1:7–9. "Back end processing . . . involves forming a metallization structure including multiple (typically three to eight) metallization layers disposed in a stack," and it is distinguished from the earlier "[f]ront-end processing," which "typically involves implanting dopants in the silicon wafer and depositing materials on the substrate that collectively form individual device components." *Id.* at 1:24–40. "[E]ach metallization layer includes a patterned metal (e.g., aluminum) 'wire' layer and an interlevel dielectric (ILD) layer that serves to electrically isolate the patterned metal wires from the subsequently formed metal wires." *Id.* at 1:40–44.

According to the '455 patent, hydrogen plays an important role in "the performance of CMOS devices." *Id.* at 2:18–19. Specifically, "[a] certain amount of hydrogen at the Silicon-Gate Oxide interface is needed to passivate the surface states," but "excess amounts of hydrogen are responsible for device instabilities" such as "floating gate memory retention loss." *Id.* at 2:19–25. Hydrogen can be generated "if aluminum is disposed over the dielectric, possibly through a reaction with residual moisture contained in the dielectric." *Id.* at 2:54–57. The invention of the '455 patent "is directed to a modified back-end processing method for use in the fabrication of semiconductor integrated circuits (ICs), and in particular to the fabrication of image sensors, that facilitates control over the amount of generated hydrogen." *Id.* at 4:54–58. It does so "by significantly reducing

or eliminating hydrogen production during the formation of at least one metallization layer of the back-end metallization structure." *Id.* at 4:58–61. This control is achieved by ensuring that

> at least one of the lower metallization layers . . . includes a ILD layer consisting of TEOS-based oxide and a cap layer formed on an upper surface of the TEOS-based oxide ILD layer that comprises a high-density, low-moisture content oxide having a minimum thickness of 100 A or greater.

Id. at 4:61–5:12. "The use of TEOS-based oxide to form the ILD layer assures superior coverage of underlying metallization structures due to its excellent gap filling characteristics." *Id.* at 5:12–15. The cap layer "isolat[es] the hydrogen-rich TEOS-based ILD material from the plasma environment generated during aluminum over-etch, whereby production of hydrogen atoms/ions that can migrate toward the front-end structures is minimized." *Id.* at 5:18–26. This "provides a low-cost and highly effective method for controlling the creation of mobile hydrogen species and their migration/diffusion to the front end devices." *Id.* at 5:26–36.

E. Illustrative Claims

Of the challenged claims, claims 1, 17, and 19 are independent. Claim 1 is illustrative and reproduced below.

> 1. A method for fabricating a semiconductor integrated circuit, the method comprising:
>
> generating front-end structures including one or more doped diffusion regions disposed in a semiconductor substrate, one or more polycrystalline silicon structures disposed over a surface of the substrate, and a pre-metal dielectric layer over the one or more polycrystalline silicon structures;
>
> forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

forming a patterned metal structure;

forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure; and

forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer,

wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.

Ex. 1001, 17:56–18:9.

F. Asserted Unpatentability Challenges

Petitioner asserts that claims 1–3, 5–12, and 15–19 are unpatentable based on the following challenges:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 5, 6, 9, 19	102	Oshima[1]
2, 3, 7	103	Oshima, Lee[2]
10	103	Oshima, Crook[3]
1, 8, 11	102	Nagai[4]
12	103	Nagai, Miyazaki[5]
15	103	Nagai, Lee
16	103	Nagai, Wang[6]
17, 18	103	Nagai, Omi[7]

[1] JP H11-284067, published Oct. 15, 1999 (Ex. 1003) (translation provided as Ex. 1005).
[2] US 2009/0072282 A1, published Mar. 19, 2009 (Ex. 1007).
[3] US 9,165,762 B2, issued Oct. 20, 2015 (Ex. 1008).
[4] US 7,598,557 B2, issued Oct. 6, 2009 (Ex. 1006).
[5] EP 1 065 714 A1, published Jan. 3, 2001 (Ex. 1009).
[6] US 7,803,647 B2, issued Sept. 28, 2010 (Ex. 1010).
[7] US 7,816,749 B2, issued Oct. 19, 2010 (Ex. 1011).

Petitioner relies on the declaration of Konstantinos P. Giapis, Ph.D. Ex. 1020 (the "Giapis Declaration").

II. ANALYSIS

A. Legal Standards

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). The burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A claim is unpatentable under 35 U.S.C. § 103 if "the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." 35 U.S.C. § 103. The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when present, objective evidence of nonobviousness.[8] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To show obviousness, it is not enough to merely show that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). "Rather, obviousness requires the additional showing that

[8] Objective indicia of nonobviousness do not appear to be present on this record.

a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention." *Id.* (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007)). "This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR*, 550 U.S. at 418–19. On the other hand, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.* at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). "A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon ex post reasoning." *KSR*, 550 U.S. at 421.

B. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art would have had "a Master's degree in Electrical Engineering, Chemical Engineering, Materials Science, or Physics and three to five years of industry experience in integrated circuit design, layout, packaging or fabrication; or a Ph.D. specializing in the field," as well as that "a greater level of experience in the relevant field may compensate for less education, and vice versa." Pet. 10 (citing Ex. 1020 ¶ 44). Patent Owner does not challenge Petitioner's definition or offer its own but "reserves the right to dispute Petitioner's definition of a [person of ordinary skill in the art] if an IPR is instituted." Prelim. Resp. 9.

In light of the record before us, and for purposes of this Decision, we adopt Petitioner's proposal regarding the level of ordinary skill in the art.

Based on our review of the '455 patent and the prior art of record, we determine that the definition offered by Petitioner comports with the qualifications a person would have needed to understand and implement the teachings of the '455 patent and the prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required "where the prior art itself reflects an appropriate level and a need for testimony is not shown") (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

C. Claim Construction

In an *inter partes* review, we construe claim terms according to the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b). Under *Phillips*, claim terms are afforded "their ordinary and customary meaning." *Phillips*, 415 F.3d at 1312. "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1313. "Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Petitioner argues that the preamble of claim 19 ("[a]n image sensor comprising") should be interpreted as non-limiting, that "silane oxide" should be interpreted as "SiO_2 formed using silane," and that "TEOS-based oxide" should be interpreted as "SiO_2 formed using TEOS." Pet. 10–11. On the present record, Patent Owner does not dispute these proposed constructions. Prelim. Resp. 10.

After considering the arguments and information presented in the Petition and Preliminary Response, we determine that we do not need to expressly construe any terms for purposes of this Decision. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.")).

D. Discretion under 35 U.S.C. § 314(a)

Under 35 U.S.C. § 314(a), the Director has discretion to deny institution. In determining whether to exercise that discretion on behalf of the Director, we are guided by the Board's precedential decision in *NHK Spring Co., Ltd. v. Intri-Plex Technologies, Inc.*, IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (precedential).

In *NHK*, the Board found that the "advanced state of the district court proceeding" was a "factor that weighs in favor of denying" the petition under § 314(a). *NHK*, Paper 8 at 20. The Board determined that "[i]nstitution of an *inter partes* review under these circumstances would not be consistent with 'an objective of the AIA . . . to provide an effective and efficient alternative to district court litigation.'" *Id.* (citing *Gen. Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 16–17 (PTAB Sept. 6, 2018) (precedential as to § II.B.4.i)).

"[T]he Board's cases addressing earlier trial dates as a basis for denial under *NHK* have sought to balance considerations such as system efficiency, fairness, and patent quality." *Apple Inc. v. Fintiv Inc.*, IPR2020-00019, Paper 11 at 5 (PTAB Mar. 20, 2020) (precedential). *Fintiv* sets forth six non-exclusive factors for determining "whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an

earlier trial date in the parallel proceeding." *Id.* at 6. These factors are reproduced below:

> 1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
>
> 2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
>
> 3. investment in the parallel proceeding by the court and the parties;
>
> 4. overlap between issues raised in the petition and in the parallel proceeding;
>
> 5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
>
> 6. other circumstances that impact the Board's exercise of discretion, including the merits.

In evaluating the factors, we take a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review. *Fintiv*, Paper 11 at 6. We are also guided by the Director's Memorandum, *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation*, issued June 21, 2022 ("Guidance Memo"),[9] which provides several clarifications concerning the application of the *Fintiv* factors. One such clarification instructs that "the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB." Guidance Memo 3 (emphasis omitted); *see also id.* at 7–8. Thus, we will not exercise our discretion to deny institution

[9] *Available at* https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

if a petitioner makes the stipulation provided in *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 18–19 (PTAB Dec. 1, 2020) (precedential as to § II.A).

Patent Owner argues that we should exercise discretion to deny institution in light of the advanced stage of the parallel district court litigation. Prelim. Resp. 10–13. Petitioner disagrees, arguing that it has made a *Sotera*-type stipulation that "precludes discretionary denial under § 314(a)." Pet. 25. Patent Owner counters that Petitioner's stipulation is insufficient both (1) because "Petitioner has not filed a stipulation in district court" and (2) because Petitioner's stipulation "is significantly narrower than the [stipulation] that was considered by the Board in *Sotera*." Prelim. Resp. 12–13.

On the present record, we are not persuaded by Patent Owner's first argument. The Guidance Memo provides that "the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding [the relevant grounds]." Guidance Memo 3. This is because, "[w]hen a petitioner stipulates not to pursue in a parallel district court proceeding [the relevant grounds], it mitigates concerns of potentially conflicting decisions and duplicative efforts between the district court and the PTAB." *Id.* at 7. All the Guidance Memo requires, therefore, is that Petitioner "stipulate[]" or "present[] a stipulation," not that the stipulation be filed in district court. *Id.* at 3, 7. Accordingly, we do not discount Petitioner's stipulation because Petitioner failed to file it in district court.

Patent Owner's second argument is more persuasive. According to the Guidance Memo, we should not exercise discretion to deny institution where a petitioner "stipulates not to pursue in a parallel district court

proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition." *Id.* at 7. Here, Petitioner's stipulation makes use of this language but is limited "to the patent claim subject to the instituted IPR." Pet. 25. This leaves open the possibility that Petitioner might still raise in the parallel district court proceeding a ground that it asserted or reasonably could have asserted here with respect to a claim that is not subject to an instituted IPR. There are several such claims here, because the Petition does not challenge claims 4, 13, or 14. *Id.* at 1–82. Each of those claims depends from one or more of the claims challenged here. Ex. 1001, 18:28–39, 19:42–53. Accordingly, the possibility exists that the district court could make findings about the invalidity of the claims not challenged in this IPR, but dependent on claims that are challenged in this IPR, potentially leading to conflicting decisions. The fact that this possibility exists shows that, under these facts, Petitioner's stipulation does not mitigate the risk of duplicative proceedings and conflicting decisions to the same degree as the stipulation in *Sotera*. Accordingly, we do not find that this stipulation implicates the Guidance Memo's prohibition against discretionary denial where a *Sotera*-type stipulation is presented.

Because we are not barred by the terms of the Guidance Memo from exercising discretion to deny institution, we must consider the *Fintiv* factors. Neither party has directed us to any evidence that the district court has stayed or is likely to stay the parallel proceeding, so the first factor is neutral. Trial in the parallel proceeding is scheduled to begin on May 6, 2024, approximately two and a half months before our final written decision would be due, so the second factor is somewhat in favor of exercising discretion to deny institution. Ex. 2010, 1. As of the date when our institution decision is due, there will be significant work left to do in the

parallel proceeding, including claim construction, fact and expert discovery, and dispositive motions, so the third factor weighs against discretionary denial. *Id.* at 1–4. Although, as discussed above, Petitioner's stipulation does not eliminate the possibility of overlapping issues here and in the parallel proceeding, it does minimize that possibility, so the fourth factor weighs somewhat against discretionary denial. Petitioner here is the defendant in the parallel proceeding, so the fifth factor weighs in favor of discretionary denial. Finally, neither party raises additional circumstances impacting our exercise of discretion, so the sixth factor is neutral. Considering these factors as a whole, we are not persuaded the efficiency and integrity of the system would be best served by exercising discretion to deny institution. Accordingly, we do not exercise such discretion.

E. Asserted Anticipation by Oshima

Petitioner contends claims 1, 5, 6, 9, and 19 are unpatentable as anticipated by Oshima. Pet. 26–46.

1. Oshima

Oshima "relates to a semiconductor device having a multilayered trace structure . . . and to a manufacturing method for the same." Ex. 1005 ¶ 1. After forming "a standard stacked gate non-volatile memory cell," Oshima teaches forming a first trace layer from aluminum or a similar trace material. *Id.* ¶¶ 21–22. A "plasma oxide film . . . is deposited on the" first trace layer," and a "TEOS oxide film . . . is further deposited thereupon." *Id.* ¶ 23. "After the TEOS oxide film . . . has been leveled, annealing is performed," and then a "plasma oxide film . . . is deposited over the entire surface of the TEOS oxide film." *Id.* ¶ 27. This film has "the thickness required to prevent hydrogen diffusion without accruing defects." *Id.* Above this layer, Oshima teaches forming a second metal trace layer, then

"a plasma oxide film," "a TEOS oxide film," and "a plasma oxide film." *Id.* ¶¶ 44–45. Finally, Oshima teaches forming a third metal trace layer, then "a passivation film." *Id.* ¶ 46. The passivation film includes a "TEOS oxide film" and a "plasma nitride film." *Id.* ¶ 39.

2. Analysis

a) Claim 1

The preamble of claim 1 of the '455 patent recites "[a] method for fabricating a semiconductor integrated circuit." Ex. 1001, 17:56–57. Petitioner argues that "Oshima discloses the preamble" of claim 1. Pet. 26 (quoting Ex. 1005 ¶ 1). Patent Owner does not dispute Petitioner's argument at this time. Prelim. Resp. 19–22. On the present record, Petitioner shows sufficiently that Oshima discloses the preamble of claim 1. Ex. 1005 ¶ 1 ("This invention relates to a semiconductor device . . . and to a manufacturing method for the same.").

Claim 1 next recites "generating front-end structures including one or more doped diffusion regions disposed in a semiconductor substrate, one or more polycrystalline silicon structures disposed over a surface of the substrate, and a pre-metal dielectric layer over the one or more polycrystalline silicon structures." Ex. 1001, 17:58–63. Petitioner argues that Oshima discloses this limitation, and Patent Owner does not dispute Petitioner's argument. Pet. 26–29 (citing Ex. 1005 ¶¶ 21, 22, Fig. 1; Ex. 1014, 318–319; Ex. 1016, 191; Ex. 1020 ¶¶ 79–81); Prelim. Resp. 19–22. Oshima discusses a semiconductor structure that includes doped regions within a substrate, gate electrodes over the surface of that substrate, and a BPSG film over the gate electrodes. Ex. 1005 ¶¶ 21, 22, Fig. 1. Petitioner directs us to evidence supporting its contention that the gate electrodes would have been made of polycrystalline silicon and that the BPSG film

would be a dielectric layer. Ex. 1014, 318–319; Ex. 1016, 191; Ex. 1020 ¶¶ 80–81. Thus, on the present record, Petitioner shows sufficiently that Oshima discloses this limitation.

Claim 1 recites "forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes: forming a patterned metal structure [and] forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure." Ex. 1001, 17:64–18:3. Petitioner argues that Oshima discloses this limitation, and Patent Owner does not dispute Petitioner's argument. Pet. 29–32 (citing Ex. 1005 ¶¶ 22, 23, 30, 31, 38, 39, 44, 47, Fig. 17); Prelim. Resp. 19–22. Oshima teaches forming three metal trace layers by depositing and patterning metal films, then forming TEOS oxide films over each metal trace layer. Ex. 1005 ¶¶ 22, 23, 30, 31, 38, 39, 44, 47, Fig. 17. Thus, on the present record, Petitioner shows sufficiently that Oshima discloses this limitation.

Claim 1 next recites

> wherein forming at least one of said metallization layers includes . . . forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer, wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.

Ex. 1001, 17:65–18:9. Petitioner argues that Oshima discloses this limitation. Pet. 32–36 (citing Ex. 1005 ¶¶ 2, 5, 9, 15, 31, 34, 36, 40, 45, 47, 48, 50, Fig. 17). Patent Owner does not dispute Petitioner's argument that Oshima discloses the presence of a cap layer over its lower metallization layers, but Patent Owner does dispute Petitioner's argument that Oshima discloses the lack of a cap layer over the uppermost metallization layer.

Prelim. Resp. 19–22. With respect to the lower layers, Oshima teaches forming a plasma oxide layer over each TEOS oxide film, and Oshima teaches that the plasma oxide films are deposited to "prevent diffusion of moisture and hydrogen into the non-volatile memory cell area." Ex. 1005 ¶¶ 36, 45, 47, 48, Fig. 17. The plasma oxide films of Oshima are between 2000 and 6000 angstroms thick. *Id.* ¶¶ 9, 34, 50. Thus, on the present record, Petitioner shows sufficiently that Oshima discloses the recited cap layers over the lower metallization layers.

The parties disagree about whether Oshima discloses the lack of a cap layer over the uppermost metallization layer. Specifically, Oshima teaches an uppermost metallization layer that is overlaid by a TEOS oxide film and a plasma nitride layer, and the parties disagree about whether the plasma nitride layer is a cap layer within the meaning of claim 1. Pet. 35–36; Prelim. Resp. 19–22. Petitioner argues that the plasma nitride layer cannot be a cap layer, both because it is a nitride material when claim 1 requires the cap layer to be oxide material and because Oshima teaches that the plasma nitride layer "is a source, rather than a blocker, of hydrogen." Pet. 36 (citing Ex. 1005 ¶¶ 2, 5, 15). Patent Owner argues that a person of ordinary skill in the art "would have understood that the term 'plasma nitride' is a general term in the semiconductor manufacturing process referring to a variety of nitride compounds that can include . . . oxide material [such as] silicon oxynitride," suggesting that Oshima's description of the material as plasma nitride does not prove that the material is something other than oxide. Prelim. Resp. 20–21 (citing Ex. 2001; Ex. 2002; Ex. 2003; Ex. 2004). Patent Owner's cited evidence describes silicon oxynitride material, but Patent Owner does not explain why this material would have been referred to as plasma nitride. *Id.* Similarly, Patent Owner argues that a person of

ordinary skill in the art "would have understood that Oshima's plasma nitride layer . . . is a cap layer because plasma nitride films, which includes silicon nitride, silicon oxynitride, and other oxynitride films, are well-known to be excellent diffusion barriers." *Id.* at 21 (citing Ex. 2009). Again, though, the cited evidence describes the suppression of hydrogen diffusion through silicon oxynitride but fails to make clear that the silicon oxynitride material would have been referred to as plasma nitride, the term Oshima uses. *Id.* Finally, Patent Owner disputes Petitioner's argument that plasma nitride is a source of hydrogen by arguing that Oshima's statement that the purpose of its oxide films was "to prevent the diffusion of hydrogen from the nitride film," Ex. 1005 ¶ 2, could "mean preventing the diffusion of hydrogen based on (or using) nitride film." Prelim. Resp. 21. Patent Owner does not explain why this interpretation of Oshima's language is warranted, and, on the present record, we see no reason to interpret Oshima's language in this way.

Thus, although the question of whether Oshima's plasma nitride layer is a cap layer within the meaning of claim 1 remains an open issue to be resolved at trial, and although we encourage both parties, to the extent permitted by our rules, to address this issue in future briefing, Petitioner has shown sufficiently on the current record that Oshima discloses this limitation. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that Oshima anticipates claim 1.

b) Claim 5

Claim 5 depends from claim 1 and adds limitations reciting

> wherein forming the pre-metal dielectric layer comprises forming a layer consisting essentially of one or more of BPSG and a TEOS-based oxide, and

> wherein the method further comprises forming an additional cap layer between said pre-metal dielectric layer and a lowermost metallization layer of said plurality of metallization layers, wherein said additional cap layer consists of silane oxide.

Ex. 1001, 18:39–47. Petitioner argues that Oshima discloses these limitations. Pet. 36–38 (citing Ex. 1005 ¶¶ 2, 22, 60, Fig. 25). On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 22–23. We have reviewed Petitioner's argument and the cited evidence, and, on the present record, Petitioner shows sufficiently that Oshima discloses the limitations of claim 5. Ex. 1005 ¶¶ 2, 22, 60, Fig. 25. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that Oshima anticipates claim 5.

c) Claim 6

Claim 6 depends from claim 5 and adds limitations reciting

> wherein forming a first patterned metal structure of a said lowermost metallization layer of said plurality of metallization layers comprises:
>
> forming a first aluminum layer on said additional cap layer; and
>
> etching a portion of said first aluminum layer such that an etch front passes through said first aluminum layer and enters said silane oxide layer, and such that said etching is terminated when a minimum thickness of said silane oxide layer between an upper surface of said pre-metal dielectric layer and said etch front is greater than 100 Å.

Ex. 1001, 18:48–59. Petitioner argues that Oshima discloses these limitations. Pet. 38–41 (citing Ex. 1005 ¶¶ 5, 22, 23, 34, 60, Figs. 17, 25; Ex. 1015, 1426, 1429–30; Ex. 1020 ¶ 96). On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 22–23. We have reviewed Petitioner's argument and the cited evidence, and, on the present record, Petitioner shows sufficiently that Oshima discloses the limitations of

claim 6. Ex. 1005 ¶¶ 5, 22, 23, 34, 60, Figs. 17, 25; Ex. 1015, 1426, 1429–30; Ex. 1020 ¶ 96. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that Oshima anticipates claim 6.

d) Claim 9

Claim 9 depends from claim 1 and adds a limitation reciting

> wherein forming said ILD layer of each said metallization layer comprises depositing a TEOS-based oxide USG/FSG, then annealing said deposited TEOS-based oxide, and then planarizing said annealed TEOS-based oxide before forming said cap layer.

Ex. 1001, 19:22–26. Petitioner argues that Oshima discloses this limitation. Pet. 41–43 (citing Ex. 1005 ¶¶ 23, 24, 32, 33, 38, 54, Figs. 2, 3, 9, 10; Ex. 1020 ¶ 98). On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 22–23. We have reviewed Petitioner's argument and the cited evidence, and, on the present record, Petitioner shows sufficiently that Oshima discloses the limitations of claim 9. Ex. 1005 ¶¶ 23, 24, 32, 33, 38, 54, Figs. 2, 3, 9, 10; Ex. 1020 ¶ 98. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that Oshima anticipates claim 9.

e) Claim 19

The preamble of claim 19 recites "[a]n image sensor." Ex. 1001, 20:37. Petitioner argues that "the preamble of claim 19 is not limiting because it merely describes an intended use . . . of the claimed device." Pet. 43; *see* Pet. 10. Patent Owner does not dispute Petitioner's argument at this time. Prelim. Resp. 23. On the present record, we treat the preamble of claim 19 as non-limiting.

Claim 19 next recites "a semiconductor substrate including a plurality of doped diffusion regions disposed below an upper substrate surface; a

plurality of polycrystalline silicon structures disposed on the semiconductor substrate over the upper substrate surface; [and] a pre-metal dielectric layer formed over the polycrystalline silicon structures." Ex. 1001, 20:38–45. Petitioner argues that Oshima discloses this limitation for the same reasons it discloses the similar limitation in claim 1, and Patent Owner does not dispute Petitioner's argument. Pet. 43–44 (citing Pet. 26–29); Prelim. Resp. 23. As discussed above with respect to claim 1, Oshima discusses a semiconductor structure that includes doped regions within a substrate, gate electrodes over the surface of that substrate, and a BPSG film over the gate electrodes. Ex. 1005 ¶¶ 21, 22, Fig. 1. Petitioner directs us to evidence supporting its contention that the gate electrodes would have been made of polycrystalline silicon and that the BPSG film would be a dielectric layer. Ex. 1014, 318–319; Ex. 1016, 191; Ex. 1020 ¶¶ 80–81. Thus, on the present record, Petitioner shows sufficiently that Oshima discloses this limitation.

Claim 19 recites

> a back-end metallization structure formed on the pre-metal dielectric layer, the back-end metallization structure including a plurality of metallization layers formed in a stack, each of the metallization layers including a patterned aluminum layer and an interlevel dielectric (ILD) layer comprising TEOS-based oxide that is formed over the patterned aluminum layer.

Ex. 1001, 20:46–53. Petitioner argues that Oshima discloses this limitation, and Patent Owner does not dispute Petitioner's argument. Pet. 44–45 (citing Ex. 1005 ¶¶ 22, 23, 30, 31, 38, 39, 44, 47, Fig. 17); Prelim. Resp. 23. Oshima teaches forming three metal trace layers by depositing and patterning metal films, then forming TEOS oxide films over each metal trace layer. Ex. 1005 ¶¶ 22, 23, 30, 31, 38, 39, 44, 47, Fig. 17. Thus, on the

present record, Petitioner shows sufficiently that Oshima discloses this limitation.

Claim 19 next recites

> wherein at least one of the plurality of metallization layers includes a cap layer formed on the ILD layer, and
>
> wherein the cap layer of all of said plurality of metallization layers except an uppermost said metallization layer comprises a silane oxide layer having a minimum thickness of 100 Å.

Ex. 1001, 20:54–59. Petitioner argues that Oshima discloses this limitation. Pet. 45–46 (citing Pet. 32–36; Ex. 1005 ¶¶ 2, 9, 34, 36, 38, 40, 45, Fig. 17). Patent Owner does not dispute Petitioner's argument that Oshima discloses the presence of a cap layer over its lower metallization layers, but Patent Owner does dispute Petitioner's argument that Oshima discloses the lack of a cap layer over the uppermost metallization layer. Prelim. Resp. 23. As discussed above with respect to claim 1, Petitioner sufficiently shows that Oshima discloses this limitation. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that Oshima anticipates claim 19.

F. Asserted Obviousness in View of Oshima and Lee

Petitioner contends claims 2, 3, and 7 are unpatentable as obvious in view of Oshima and Lee. Pet. 46–52.

1. Lee

Lee relates to "an image sensor and a method for manufacturing the same." Ex. 1007 ¶ 2. The image sensor of Lee includes a photo diode region and a transistor region. *Id.* ¶ 4, Fig. 2. In the transistor region, Lee teaches forming metal lines covered by dielectric layers, with some of the dielectric layers covered by capping layers. *Id.* ¶¶ 26–35, Fig. 2. "Each of the capping layers . . . may comprise . . . silicon dioxide formed by plasma-

assisted [chemical vapor deposition] of silicon dioxide from silane and oxygen." *Id.* ¶ 27.

2. Analysis

a) Claim 2

Claim 2 depends from claim 1 and recites three additional limitations. Ex. 1001, 18:10–24. The first of these limitations is "wherein forming said patterned metal structure of each of said plurality of metallization layers comprises forming an aluminum layer and then etching said aluminum layer." *Id.* at 18:10–15. Petitioner argues that Oshima teaches this limitation. Pet. 46–47. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 23. Oshima teaches that a "metal trace" can be "formed by depositing 600 nm of metal trace material such as Al or the like and patterning according to the standard method." Ex. 1005 ¶ 30. Petitioner directs us to evidence that supports a finding that this patterning includes etching. Ex. 1017, 85–86; Ex. 1018, 1518. Thus, Petitioner shows sufficiently that Oshima teaches this limitation.

Claim 2 next recites "wherein forming said ILD layer of at least one of said metallization layers comprises forming one or more of Undoped silicate glass (USG) and Fluorosilicate glass (FSG)." Ex. 1001, 18:16–19. Petitioner argues that Oshima teaches this limitation. Pet. 47. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 23. Oshima teaches supplying fluorine gas with its TEOS to form its TEOS oxide films. Ex. 1005 ¶ 23. Petitioner directs us to evidence that supports a finding that the result of the fluorine-containing reaction of

Oshima would be fluorosilicate glass. Ex. 1001, 1:55–61; Ex. 1020 ¶ 111. Thus, Petitioner shows sufficiently that Oshima teaches this limitation.

Claim 2 recites "wherein forming the cap layer over said ILD layer of said all of said plurality of metallization layers except said uppermost metallization layer comprises generating silane oxide by way of reacting silane (SiH_4) gas and oxygen (O_2) gas." Ex. 1001, 18:20–24. Petitioner argues that Lee teaches this limitation and that a person of ordinary skill in the art would have had a reason to combine the teachings of Lee with those of Oshima. Pet. 47–50. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 23. Lee teaches making its capping layers using "silicon dioxide formed by plasma-assisted CVD of silicon dioxide from silane and oxygen." Ex. 1007 ¶ 27. This contrasts with Oshima's method of reacting silane with N_2O gas. Ex. 1005 ¶ 23. Petitioner directs us to evidence that could support a finding that a person of ordinary skill in the art would have seen a benefit to substituting Lee's oxygen for Oshima's N_2O. Ex. 1005 ¶ 26 (higher dielectric constant is disadvantageous due to increased capacitance); Ex. 1020 ¶ 116 (use of N_2O gas might lead to formation of silicon oxynitride, which has higher dielectric constant, rather than to formation of silicon oxide that would be formed using oxygen). Thus, Petitioner shows sufficiently that Lee teaches this limitation and that a person of ordinary skill in the art would have had reason to combine to the teachings of Lee with those of Oshima with a reasonable expectation of success. Accordingly, Petitioner shows a reasonable likelihood of prevailing

on its argument that claim 2 would have been obvious in light of Oshima and Lee.

b) Claim 3

Claim 3 depends from claim 2 and adds a limitation reciting "wherein generating said silane oxide comprising forming a layer of said silane oxide having a thickness in the range of 500 Å to 5000 Å." Ex. 1001, 18:25–27. Petitioner argues that Oshima teaches this limitation. Pet. 50. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 23. Oshima teaches that its plasma oxide film has a thickness of between 2000 and 6000 Å. Ex. 1005 ¶ 9. Thus, Petitioner shows sufficiently that Oshima teaches this limitation. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claim 3 would have been obvious in light of Oshima and Lee.

c) Claim 7

Claim 7 depends from claim 6 and recites five additional limitations. Ex. 1001, 18:60–19:12. The first of these limitations is "forming a first ILD layer of said lowermost metallization layer over said etched first aluminum layer, said first ILD layer comprising one or more of Undoped silicate glass (USG) and Fluorosilicate glass (FSG)." *Id.* at 18:60–64. Petitioner argues that Oshima teaches this limitation. Pet. 51. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 23. Oshima teaches supplying fluorine gas with its TEOS to form its TEOS oxide films. Ex. 1005 ¶ 23. Petitioner directs us to evidence that supports a finding that the result of the fluorine-containing reaction of Oshima would be

fluorosilicate glass. Ex. 1001, 1:55–61; Ex. 1020 ¶ 111. Thus, Petitioner shows sufficiently that Oshima teaches this limitation.

Claim 7 next recites "forming a first cap layer over said first ILD layer by generating silane oxide by way of reacting silane (SiH_4) gas and oxygen (O_2) gas." Ex. 1001, 18:65–67. Petitioner argues that Lee teaches this limitation for the same reasons it teaches the similar limitation in claim 2. Pet. 51. As discussed above with respect to claim 2, Petitioner shows sufficiently that Lee teaches this limitation and that a person of ordinary skill in the art would have had reason to combine the teachings of Lee with those of Oshima.

Claim 7 recites

> forming a second patterned aluminum structure of a second metallization layer of said plurality of metallization layers on said first cap layer, said forming comprising:
>
> forming a second aluminum layer on said first cap layer; and etching a portion of said second aluminum layer such that an etch front passes through said second aluminum layer and enters said first cap layer, and such that said etching is terminated when a minimum thickness of said first cap layer between an upper surface of said first ILD layer and said etch front is greater than 100 Å.

Ex. 1001, 19:1–12. Petitioner argues that Oshima teaches this limitation. Pet. 51–52. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 23. Oshima teaches that a "metal trace" can be "formed by depositing 600 nm of metal trace material such as Al or the like and patterning according to the standard method." Ex. 1005 ¶ 30. Petitioner directs us to evidence that could support a finding that the etching would stop with at least 100 Å of material between the etch front and the upper surface of the pre-metal dielectric layer. Ex. 1020 ¶ 121. Thus, Petitioner

shows sufficiently that Oshima teaches this limitation. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claim 7 would have been obvious in light of Oshima and Lee.

G. Asserted Obviousness in View of Oshima and Crook

Petitioner contends claim 10 is unpatentable as obvious in view of Oshima and Crook. Pet. 52–55.

1. Crook

Crook "relates to a method of depositing silicon dioxide films . . . using tetraethyl orthosilicate (TEOS)." Ex. 1008, 1:4–7. The method "includ[es] supplying TEOS, oxygen, or a source thereof and hydrogen as precursors." *Id.* at 1:33–36. "The incorporation of hydrogen as an active gas in the deposition cycle results in significant improvements in silicon dioxide film properties when compared to deposition cycles which do not include hydrogen." *Id.* at 1:37–40. In addition, "[t]he films made by the process [of Crook] can further undergo a hydrogen plasma post deposition treatment step," which "further suppresses reabsorption of moisture and reduces the leakage current." *Id.* at 1:55–59.

2. Analysis

Claim 10 depends from claim 1 and adds a limitation reciting "wherein forming said ILD layer of at least one of said metallization layers comprises depositing a TEOS-based oxide, and then processing said TEOS-based oxide in a hydrogen plasma before forming said cap layer." Ex. 1001, 19:27–31. Petitioner argues that the combination of Oshima and Crook teaches this limitation and that a person of ordinary skill in the art would have had reason to combine the teachings of Crook with those of Oshima. Pet. 53–55. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 23. Oshima teaches depositing TEOS oxide films.

Ex. 1005 ¶¶ 23, 38. Crook teaches "treating [a] deposited silicon dioxide with a hydrogen plasma as a post deposition treatment." Ex. 1008, 4:24–26; *see also* Ex. 1008, 1:55–59 ("The films made by the process disclosed herein can further undergo a hydrogen plasma post deposition treatment step . . . . This step further suppresses reabsorption of moisture and reduces the leakage current."). Petitioner directs us to evidence that could support a finding that a person of ordinary skill in the art would have seen a benefit to treating Oshima's TEOS oxide with Crook's hydrogen plasma. Ex. 1005 ¶¶ 3, 36 (teaching that TEOS oxide absorbs moisture which can have adverse impacts); Ex. 1008, 1:55–59 (teaching that treating oxide with hydrogen plasma "suppresses reabsorption of moisture"). Thus, Petitioner shows sufficiently that the combination of Oshima and Crook teaches this limitation and that a person of ordinary skill in the art would have had a reason to combine the teachings of these references with a reasonable expectation of success. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claim 10 would have been obvious in light of Oshima and Crook.

H. Asserted Anticipation by Nagai

Petitioner contends claims 1, 8, and 11 are unpatentable as anticipated by Nagai. Pet. 55–65.

1. Nagai

Nagai "relates to . . . a semiconductor device including a capacitor using as the dielectric film, a high-dielectric constant substance or a ferroelectric substance, and a method for fabricating the semiconductor device." Ex. 1006, 1:18–23. In Nagai's method, source and drain layers are formed in a silicon substrate, a polycrystalline silicon film is patterned to form gate electrodes, and first and second interlayer insulation films are

deposited. *Id.* at 6:66–7:3, 17:39–44, 17:66–18:3, 20:38–43, Fig. 33. Above this, Nagai teaches forming three "metal interconnection layer[s]," with each interconnection layer comprising layers of titanium, titanium nitride, and aluminum-copper alloy that are deposited and then "patterned by photolithography." *Id.* at 22:13–20, 23:21–30, 24:33–42.

Over the lower two of these three interconnection layers, Nagai teaches forming first a silicon oxide layer "formed by, e.g., high density plasma enhanced CVD" and then a silicon oxide layer "formed by plasma TEOS CVD." *Id.* at 22:21–34, 23:31–43. Above each set of silicon oxide layers, Nagai teaches forming "a barrier film," with each barrier film consisting of "a hydrogen/water diffusion preventing film," a "stress mitigating film," and another "hydrogen/water diffusion preventing film." *Id.* at 34:42–51.

Over the uppermost interconnection layer, Nagai teaches forming a single silicon oxide layer that may be formed either "by . . . high density plasma enhanced CVD" or "by plasma TEOS CVD." *Id.* at 24:43–49. Above this last silicon oxide layer, Nagai teaches forming a "silicon nitride film . . . by, e.g., CVD" and a "polyimide film . . . by spin coating." *Id.* at 24:66–25:7.

2. Analysis

a) Claim 1

The preamble of claim 1 recites "[a] method for fabricating a semiconductor integrated circuit." Ex. 1001, 17:56–57. Petitioner argues that "Nagai discloses the preamble" of claim 1. Pet. 55 (quoting Ex. 1006, 1:18–19). Patent Owner does not dispute Petitioner's argument at this time. Prelim. Resp. 24–27. On the present record, Petitioner shows sufficiently that Nagai discloses the preamble of claim 1. Ex. 1006, 1:18–19 ("The

present invention relates to a semiconductor device and a method for fabricating the semiconductor device.").

Claim 1 next recites "generating front-end structures including one or more doped diffusion regions disposed in a semiconductor substrate, one or more polycrystalline silicon structures disposed over a surface of the substrate, and a pre-metal dielectric layer over the one or more polycrystalline silicon structures." Ex. 1001, 17:58–63. Petitioner argues that Nagai discloses this limitation, and Patent Owner does not dispute Petitioner's argument. Pet. 55–57 (citing Ex. 1006, 6:66–7:3, 17:39–44, 17:66–18:3, 20:38–43, Fig. 33); Prelim. Resp. 24–27. Nagai discusses a semiconductor structure that includes diffused regions within a substrate, polycrystal silicon gate electrodes over the surface of that substrate, and inter-layer insulation films. Ex. 1006, 6:66–7:3, 17:39–44, 17:66–18:3, 20:38–43, Fig. 33. Thus, on the present record, Petitioner shows sufficiently that Nagai discloses this limitation.

Claim 1 recites "forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes: forming a patterned metal structure [and] forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure." Ex. 1001, 17:64–18:3. Petitioner argues that Nagai discloses this limitation, and Patent Owner does not dispute Petitioner's argument. Pet. 57–59 (citing Ex. 1006, 22:13–34, 23:21–26, 23:31–43, 24:33–49, Fig. 33); Prelim. Resp. 24–27. Nagai teaches forming three metal trace layers by depositing and patterning metal films, then forming TEOS oxide films over each metal trace layer. Ex. 1006, 22:13–34,

23:21–26, 23:31–43, 24:33–49, Fig. 33. Thus, on the present record, Petitioner shows sufficiently that Nagai discloses this limitation.

Claim 1 next recites

> wherein forming at least one of said metallization layers includes . . . forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer, wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.

Ex. 1001, 17:65–18:9. Petitioner argues that Nagai discloses this limitation. Pet. 59–62 (citing Ex. 1006, 34:42–35:32, 35:37–45, Fig. 33). Patent Owner does not dispute Petitioner's argument that Nagai discloses the presence of a cap layer over its lower metallization layers, but Patent Owner does dispute Petitioner's argument that Nagai discloses the lack of a cap layer over the uppermost metallization layer. Prelim. Resp. 24–27. With respect to the lower layers, Nagai teaches forming an oxide layer over each TEOS oxide film. Ex. 1006, 34:42–35:32, 35:37–45, Fig. 33. The oxide films of Nagai are between 900 and 1600 angstroms thick. *Id.* at 34:49–58, 35:9–17. Thus, on the present record, Petitioner shows sufficiently that Nagai discloses the recited cap layers over the lower metallization layers.

The parties disagree about whether Nagai discloses the lack of a cap layer over the uppermost metallization layer. Specifically, Nagai teaches an uppermost metallization layer that is overlain by a TEOS oxide film and a silicon nitride layer, and the parties disagree about whether the silicon nitride layer is a cap layer within the meaning of claim 1. Pet. 61–62; Prelim. Resp. 24–27. Petitioner argues that the silicon nitride layer cannot be a cap layer, both because it is a nitride material when claim 1 requires the cap layer to be oxide material and because "it was known in the art that

silicon nitride film can create, rather than block, hydrogen." Pet. 61–62 (citing Ex. 1005 ¶¶ 2, 5, 15; Ex. 1006, Fig. 33).

Patent Owner argues that a person of ordinary skill in the art "would have understood that Nagai's silicon nitride film . . . is a cap layer because silicon nitride is well-known to be [an] excellent diffusion barrier[]." Prelim. Resp. 24 (citing Ex. 2005). Patent Owner cites evidence that "silicon nitride . . . [is] impervious to the diffusion of gases such as hydrogen," Ex. 2005, code (57), but, even assuming Patent Owner is correct that Nagai's silicon nitride film could act as a cap layer, the challenged claim still requires a cap layer to be an oxide layer rather than a nitride layer. Ex. 1001, 18:7–9.

Patent Owner also argues that the formation of silicon nitride will inevitably result in the inclusion of some oxide material due to the reaction mechanisms used. Prelim. Resp. 24–25. Patent Owner does not, however, cite any support for the reaction mechanisms it describes. *Id.* Moreover, some of the sources Patent Owner cites for the proposition that silicon nitride inevitably contains some oxide material suggest that, in fact, silicon nitride and silicon oxynitride are different materials. Ex. 2007, 3 (describing "plasma anodization of . . . silicon nitride films to produce silicon oxynitride films"); Ex. 2008, 1 (describing "silicon nitride films [that] have been oxidised in an oxygen plasma . . . to produce oxynitride films").

Thus, although the question of whether Nagai's silicon nitride layer is a cap layer within the meaning of claim 1 remains an open issue to be resolved at trial, and although we encourage both parties, to the extent permitted by our rules, to address this issue in future briefing, Petitioner has shown sufficiently on the current record that Nagai discloses this limitation.

Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that Nagai anticipates claim 1.

b) Claim 8

Claim 8 depends from claim 1 and adds limitations reciting

> wherein forming the pre-metal dielectric layer comprises forming a layer consisting essentially of one or more of BPSG and a TEOS-based oxide, and
>
> wherein the method further comprises a barrier layer disposed between said polycrystalline silicon structures and a lowermost metallization layer of said plurality of metallization layers, wherein said barrier layer comprises one of silicon nitride and silicon oxynitride.

Ex. 1001, 19:13–21. Petitioner argues that Nagai discloses these limitations. Pet. 62–63 (citing Ex. 1006, 7:16–20, 13:19–29, 18:23–26, 20:38–43, 21:19–25, Fig. 33). On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 27. We have reviewed Petitioner's argument and the cited evidence, and, on the present record, Petitioner shows sufficiently that Nagai discloses the limitations of claim 8. Ex. 1006, 7:16–20, 13:19–29, 18:23–26, 20:38–43, 21:19–25, Fig. 33. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that Nagai anticipates claim 8.

c) Claim 11

Claim 11 depends from claim 1 and adds a limitation reciting "after forming an uppermost ILD layer of an uppermost metallization layer of said plurality of metallization layers, annealing said uppermost ILD layer at temperature in the range 350-450°C. before performing a pad etch." Ex. 1001, 19:32–36. Petitioner argues that Nagai discloses these limitations. Pet. 63–65 (citing Ex. 1006, 8:19–22, 15:41–42, 24:50–60, 25:8–10; Ex. 1020 ¶ 143). On the present record, Patent Owner does not dispute this

argument. Prelim. Resp. 27. We have reviewed Petitioner's argument and the cited evidence, and, on the present record, Petitioner shows sufficiently that Nagai discloses the limitations of claim 11. Ex. 1006, 8:19–22, 15:41–42, 24:50–60, 25:8–10; Ex. 1020 ¶ 143. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that Nagai anticipates claim 11.

I. Asserted Obviousness in View of Nagai and Miyazaki

Petitioner contends claim 12 is unpatentable as obvious in view of Nagai and Miyazaki. Pet. 65–67.

1. Miyazaki

Miyazai "relates to a method of fabricating a semiconductor device . . . using an organic interlayer insulation film as an insulation film between interconnections." Ex. 1009 ¶ 1. According to Miyazaki, in prior-art devices, "the measured insulation resistance value between the upper layer interconnections . . . is not a sufficiently high value," which "causes an increase[d] leak in current and an increase in power consumption in the semiconductor device" as well as "deteriorat[ing] reliability." *Id.* ¶¶ 13–14. The method of Miyazaki solves these problems by forming a silicon oxide or silicon nitride protection film, exposing contact holes, forming and opening a polyimide precursor layer, and annealing, forming a polyimidized film. *Id.* ¶¶ 30–36, Figs. 2, 3.

2. Analysis

Claim 12 depends from claim 1 and adds a limitation reciting "after forming an uppermost ILD layer of an uppermost metallization layer of said plurality of metallization layers, performing a pad etch, and then annealing said uppermost ILD layer at temperature in the range 350-450°C." Ex. 1001, 19:37–41. Petitioner argues that the combination of Nagai and

Miyazaki teaches this limitation and that a person of ordinary skill in the art would have had reason to combine the teachings of these references with a reasonable expectation of success. Pet. 65–67. Patent Owner does not dispute this argument. Prelim. Resp. 27. Nagai teaches forming openings "in the polyimide film . . . down to the electrode pads." Ex. 1006, 25:8–10. Miyazaki teaches forming a silicon oxide protection film, depositing and opening a polyimide precursor, and then annealing for 30 minutes at between 350 and 450 degrees Celsius. Ex. 1009 ¶¶ 30, 33–36, Figs. 2, 3. Petitioner directs us to evidence that could support a finding that a person of ordinary skill in the art would have seen a benefit to annealing Nagai's structure according to Miyazaki's method. Ex. 1009 ¶ 22 (stating that post-pad etch annealing increases the insulation resistance of an interlayer insulation film). Thus, Petitioner shows sufficiently that the combination of Nagai and Miyazaki teaches this limitation and that a person of ordinary skill in the art would have had reason to combine the teachings of Miyazaki with those of Nagai. Accordingly, Petitioner shows a reasonable likelihood of prevailing on its argument that claim 12 would have been obvious in light of Nagai and Miyazaki.

J. Asserted Obviousness in View of Nagai and Lee

Petitioner contends claim 15 is unpatentable as obvious in view of Nagai and Lee. Pet. 68–70.

Claim 15 depends from claim 1 and adds a limitation reciting "wherein fabricating said semiconductor integrated circuit comprises fabricating one of a CMOS image sensor (CIS) and a charge-coupled device (CCD)." Ex. 1001, 19:54–57. Petitioner argues that Lee teaches this limitation and that a person of ordinary skill in the art would have had reason to combine the teachings of Lee with those of Nagai, with a

reasonable expectation of success. Pet. 68–70. Patent Owner does not dispute this argument. Prelim. Resp. 27. Lee teaches forming a photo diode region beside a transistor region similar to that of Nagai, and Lee teaches that the photo diode region converts a light signal into an electrical signal. Ex. 1007 ¶¶ 3, 4, 6, 24, 25, Fig. 2. Lee describes its structure as a CMOS image sensor. *Id.* ¶¶ 3, 4.

We are not persuaded that Petitioner sufficiently shows a reason to combine the teachings of Lee with those of Nagai. Petitioner directs us to the testimony of Dr. Giapis to support the argument that a person of ordinary skill in the art would have seen a benefit in constructing Lee's image sensor using Nagai's hydrogen diffusion control techniques. Pet. 69–70 (citing Ex. 1020 ¶ 151). Specifically, Dr. Giapis testifies that Lee's image "sensors must store accumulated charge until it is read [and] hydrogen diffusion from the back-end processes will have an adverse effect on the front end, in particular on the sensor's ability to retain charges." Ex. 1020 ¶ 151. This testimony cites no sources or technical reasoning in support, and it replicates the Petition essentially word-for-word. *Compare id. with* Pet. 69–70. Thus, it is entitled to little or no weight. *Xerox Corp. v. ByteMark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential); 37 C.F.R. 42.65(a). Petitioner does not show sufficiently that a person of ordinary skill in the art would have had reason to combine the teachings of Lee with those of Nagai. Accordingly, Petitioner does not show a reasonable likelihood of prevailing on its argument that claim 15 would have been obvious in light of Nagai and Lee.

K. Asserted Obviousness in View of Nagai and Wang

Petitioner contends claim 16 is unpatentable as obvious in view of Nagai and Wang. Pet. 70–72.

1. Wang

Wang relates to "an image sensor semiconductor device." Ex. 1010, code (57). "The imaging sensor element" of Wang "is disposed in [a] semiconductor substrate" and "includes a light-sensing region . . . having . . . dopants formed . . . by a method such as diffusion or ion implantation." *Id.* at 2:21–26. "The light-sensing region may . . . be[] operable to receive light (or other form of radiation energy from an object to be imaged)." *Id.* at 2:26–31.

2. Analysis

Claim 16 depends from claim 1 and adds a limitation reciting "wherein fabricating said semiconductor integrated circuit comprises fabricating a radiation detector." Ex. 1001, 19:58–60. Petitioner argues that Wang teaches this limitation and that a person of ordinary skill in the art would have had reason to combine the teachings of Wang with those of Nagai. Pet. 70–72. Patent Owner does not dispute this argument. Prelim. Resp. 27–28. Wang teaches an imaging sensor that is "operable to receive light (or other form of radiation energy from an object to be imaged)." Ex. 1010, 2:21–31, Fig. 4.

We are not persuaded that Petitioner shows sufficiently a reason to combine the teachings of Wang with those of Nagai. Petitioner directs us to the testimony of Dr. Giapis to support the argument that a person of ordinary skill in the art would have seen a benefit in constructing Wang's image sensor using Nagai's hydrogen diffusion control techniques. Pet. 72 (citing Ex. 1020 ¶ 155). Specifically, Dr. Giapis testifies that "employing Nagai's method to fabricate a radiation detector as disclosed in Wang achieves predictable benefits (*i.e.*, reducing adverse effect of hydrogen diffusion on the front end, particularly on the sensor's ability to retain charges)."

Ex. 1020 ¶ 155. This testimony cites no sources or technical reasoning in support, and it replicates the wording of the Petition essentially word-for-word. *Compare id. with* Pet. 72. Thus, it is entitled to little or no weight. *Xerox*, IPR2022-00624, Paper 9 at 15; 37 C.F.R. 42.65(a). Petitioner does not show sufficiently that a person of ordinary skill in the art would have had reason to combine to the teachings of Wang with those of Nagai. Accordingly, Petitioner does not show a reasonable likelihood of prevailing on its argument that claim 16 would have been obvious in light of Nagai and Wang.

L. Asserted Obviousness in View of Nagai and Omi

Petitioner contends claims 17 and 18 are unpatentable as obvious in view of Nagai and Omi. Pet. 72–82.

1. Omi

Omi "relates to a photoelectric conversion device and a method of producing the same, and a method of producing a line image sensor IC." Ex. 1011, 1:13–15. In Omi's method, "a plurality of line image sensor ICs . . . are formed on the surface of a semiconductor substrate." *Id.* at 9:28–30. Each image sensor IC "ha[s] an elongated rectangular shape," and there are "gap[s] therebetween." *Id.* at 9:35–46, Fig. 5F. In one embodiment of Omi, "an inter-pixel light shielding aluminum" structure "is formed," and "an insulating film . . . of tetra ethoxy silane (TEOS) is deposited on the surface of [an] intermediate insulating film," then "flattened by chemical mechanical polishing (CMP)." *Id.* at 14:46–56. After this, another "inter-pixel light shielding aluminum" structure and a series of "dummy interconnects . . . are formed." *Id.* at 14:57–62. Above this, "a protective film . . . is formed . . . by plasma CVD." *Id.* at 14:63–65, Fig. 6C. Omi teaches that this film can be made from "silicon nitride (SiN) or the like."

Id. at 11:22–23. The portion of "the protective film . . . between the photoelectric conversion elements . . . and the dummy interconnects . . . is removed by etching." *Id.* at 14:65–67.

2. Analysis

Petitioner argues that a person of ordinary skill in the art would have had a reason to combine the teachings of Omi with those of Nagai. Pet. 75–78. Specifically, Petitioner argues that "[i]mage sensor devices must store accumulated charge until it is read; hydrogen diffusion from the back-end processes will have an adverse effect on the front end, in particular on the sensor's ability to retain charges, just as the multi-metallization layer semiconductor devices of Nagai." *Id.* at 77. "As such," Petitioner argues that a person of ordinary skill in the art "would have found it beneficial to utilize Nagai's teachings to construct an image sensor IC by disposing image sensing pixels in Nagai's semiconductor substrate 10, as disclosed in Omi." *Id.* As support for this argument, Petitioner cites Dr. Giapis's declaration. *Id.* (citing Ex. 1020 ¶ 166). But Dr. Giapis repeats the text of the Petition verbatim without citing any additional support or providing any technical reasoning. *Compare* Ex. 1020 ¶ 166 *with* Pet. 77. Accordingly, his testimony is entitled to little or no weight. *Xerox*, IPR2022-00624, Paper 9 at 15; 37 C.F.R. 42.65(a). Petitioner does not show sufficiently that a person of ordinary skill in the art would have had reason to combine the teachings of Omi with those of Nagai. Accordingly, Petitioner does not show a reasonable likelihood of prevailing on its argument that claims 17 and 18 would have been obvious in light of Nagai and Omi.

III. CONCLUSION

Upon consideration of the Petition, the Preliminary Response, and the evidence presented, we determine that Petitioner has shown a reasonable

likelihood that it will prevail in showing that claims 1–3, 5–12, and 19 are unpatentable, but Petitioner has not shown a reasonable likelihood that it will prevail in showing that claims 15–18 are unpatentable. Instituting review as to the grounds and the limited set of claims on which Petitioner has shown a reasonable likelihood of prevailing requires instituting review as to all claims challenged and all grounds asserted in the Petition. *SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348, 1355–56 (2018); *AC Techs. S.A. v. Amazon.com, Inc.*, 912 F.3d 1358, 1364 (Fed. Cir. 2019); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018). Accordingly, we institute an *inter partes* review of all challenged claims based on all grounds asserted in the Petition.

IV. ORDER

For the reasons given, it is:

ORDERED that an *inter partes* review is instituted with respect to the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

FOR PETITIONER:

James M. Glass
John T. McKee
Andrew M. Holmes
QUINN EMANUEL URQUHART & SULLIVAN, LLP
jimglass@quinnemanuel.com
johnmckee@quinnemanuel.com
drewholmes@quinnemanuel.com

FOR PATENT OWNER:

Eric Cohen
RIMON PC
eric.cohen@rimonlaw.com