

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.,

Patent Owner.

IPR2023-00373

U.S. Patent No. 9,431,455

DECLARATION OF RON MALTIEL

I, **RON MALTIEL**, declare the following to be true:

I. INTRODUCTION

1. I have been retained by Alidouble Inc. through its counsel, to provide my opinions regarding U.S. Patent No. 9,431,455 (Ex. 1001, hereinafter the “’455 Patent”).

2. I make this declaration in support of Alidouble’s Patent Owner’s Response to the Petition in IPR2023-00373.

3. This declaration contains statements of my opinions formed to date regarding the ‘455 Patent and the bases and reasons for those opinions. I may offer additional or different opinions based on further review of materials in this IPR, including review of opinions or testimony of other expert witnesses or future positions taken by Petitioner or its witnesses.

II. PROFESSIONAL EXPERIENCE AND QUALIFICATIONS

4. My educational and professional background, patents, and professional association memberships are listed in my *curriculum vitae* is Exhibit 2012.

5. I am a senior member of the Institute of Electrical and Electronics Engineers (IEEE) with more than 30 years’ experience in all phases of design and implementation of semiconductor manufacturing. I have worked in the development and production of new integrated circuit technologies and semiconductor devices such as CMOS devices, used for products such as Dynamic Ram (DRAM), Flash

(NAND, NOR), EEPROM, ROM, and Static RAM (SRAM) memories which are used in microprocessors, logic, digital, analog, and image sensor products.

6. I graduated in 1977 from Ben Gurion University in Israel with a Bachelor of Science degree in Materials Science & Engineering. In 1978, I earned a Master's Degree in Materials Science & Engineering from Stanford University in Palo Alto, California.

7. In 1980, I was awarded an Engineer Degree from Stanford University in Materials Science & Engineering. At Stanford University, an Engineer Degree is an additional graduate degree that can be earned after a Master's Degree. The degree differs from a Ph.D. in that an Engineer Degree's focus is primarily on professional engineering work as opposed to a Ph.D.'s primary focus on theoretical research or university teaching.¹ An Engineer Degree requires two years of additional study beyond a Master's Degree and the completion of a thesis.² My thesis related to defects in silicon and electrical measurements of their properties and was entitled *Electrical Properties Of Gold And Titanium In Silicon*. My thesis led to my first

¹ See <http://gap.stanford.edu/4-3.html>

² See *id.*

patent.³

8. Following my studies at Stanford, I worked in four semiconductor companies, focusing on the development and manufacturing of new semiconductor devices. Through the years I was responsible for integrating the work product of all the various disciplines into final manufacturing processes.

9. In 1980, my first position was at Intel. I worked to develop the first commercial non-volatile EEPROM devices. NAND memory such as Flash memory was subsequently developed using EEPROM as its basic building block. Among other responsibilities, I analyzed the manufacturing reliability and designed the production and testing of operation flow.

10. In 1982, I left Intel and joined American Micro Systems, where I was in charge of developing the manufacturing process for a new non-volatile memory product line.

11. In 1983, I joined Advanced Micro Devices (AMD) working on a project combining non-volatile with DRAM memories. I developed memory circuitry and its manufacturing process. This work led to three patents where I am named as an inventor. Following this project, I worked on several other technologies at AMD

³ [Gold-doped IC resistor region - #4,432,008, https://www.maltiel.com/ron-maltiels-patents.html](https://www.maltiel.com/ron-maltiels-patents.html)

While at AMD, I was in charge of consolidating the designs of all the test chips made by all of AMD's various divisions into one library. The test chips were used during new technology development and production to monitor the electrical properties of semiconductor products following their fabrication.

12. In 1989, I joined Maxim Integrated Products, Inc. where I was in charge of developing all the CMOS process developments for analog products and introducing them to production. When Maxim bought its first fabrication line, I developed the production process for the diffusion and etch areas.

13. I currently work as an independent consultant providing consulting services in various aspects of semiconductor technology and manufacturing.

14. In 2008, I was recognized as a Senior Member of the IEEE, the leading professional association for electrical engineers.⁴ Senior Member is the highest grade and recognizes a member with at least 10 years of industry experience including 5 years of which the member has shown "significant performance."⁵

15. For more than 20 years, I have been managing a semiconductor industry website (www.maltiel-consulting.com) and providing to the semiconductor industry a resource full of pertinent information about new semiconductor patents as well as

⁴ See <http://www.ieee.org/about/index.html>

⁵ See <http://www.ieee.org/membership/senior/senior-requirements.html>

semiconductor products and their introduction to manufacturing. This resource addresses the informational needs of technology companies, attorneys, and investors and is used regularly by the United States Patent and Trademark Office, the Justice Department, major semiconductor companies, and universities from more than 99 countries.

16. I am the named inventor of six patents. The patents are in the areas of process and circuit development. Three of my patents are related to creating new semiconductor devices and to monitoring the properties of semiconductor lines during fabrication. Two of my patents are related to measurements of wafers during fabrication. One of my patents is related to integrating resistors into doped regions in the semiconductor substrate. My patents have been referenced in other United States patents more than 150 times.

III. COMPENSATION

17. I am compensated at a rate of \$720 per hour for my work. I am also being separately reimbursed for any out-of-pocket expenses. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of any proceeding.

IV. MATERIALS CONSIDERED

18. Among the materials I considered are as follow. If there are materials that I referenced but are not listed below, they should be part of the materials considered.

NO.	DOCUMENT
1	U.S. Patent No. 9,431,455
2	Prosecution history for U.S. Patent No. 9,431,455
3	Japanese Patent Publication No. JPH11-284067
4	Translation Certificate for JPH11-284067
5	Certified English Translation of JPH11-284067
6	U.S. Patent No. 7,598,557
7	U.S. Patent Publication No. 2009/0072282
8	U.S. Patent No. 9,165,762
9	European Patent Publication No. 1,065,714
10	U.S. Patent No. 7,803,647
11	U.S. Patent No. 7,816,749
12	J. Foggiato, Chemical Vapor Deposition of Silicon Dioxide Films, Handbook of Thin Film Deposition Processes and Techniques, <i>Principles, Methods, Equipment and Applications</i> , 2nd Ed. at 111-150 (2001)
13	S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 1: Process Technology</i> , 2nd Ed. (2000)
14	S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 2: the Submicron MOSFET</i> (1990)

15	G. Stojakovic and X.J. Ning, <i>Reactive Ion Etch of 150 nm Al Lines for Interconnections in Dynamic Random Access Memory</i> , Journal of Vacuum Science & Tech. A 18, 1425 (2000)
16	M. H. White et al., A Low Voltage Sonos Nonvolatile Semiconductor Memory Technology, IEEE Part A, Vol. 20, No. 2, at 191 (1997)
17	W. E. Frank, <i>Approaches For Patterning of Aluminum</i> , Microelectronic Engineering 33 (1997)
18	<i>Plasma Etching of Aluminum Metallizations For Ultralarge Scale Integrated Circuits</i> , J. Electrochem. Soc. 140 1518 (1993)
19	<i>Modeling of Charging Damage During Interlevel Oxide Deposition In High-Density Plasma</i> , J. of Applied Physics, Vol. 84, No. 1 (1998)
20	Declaration of Dr. Konstantinos P. Giapis, Ph.D.
21	Curriculum Vitae, Dr. Konstantinos P. Giapis, Ph.D.
22	Petition For <i>Inter Partes</i> Review of U.S. Patent No. 9,431,455
23	Patent Owner's Preliminary Response to Petition For <i>Inter Partes</i> Review of U.S. Patent No. 9,431,455
24	Institution Decision For <i>Inter Partes</i> Review of U.S. Patent No. 9,431,455
25	Characteristics of SiOxNy films deposited by inductively coupled plasma enhanced chemical vapor deposition using HMDS/NH3/O2/Ar for water vapor diffusion barrier (September 2006)
26	SiOxNy thin film deposited by plasma enhanced chemical vapor deposition at low temperature using HMDS–O2–NH3–Ar gas mixtures (September 2006)
27	Formation of size-controlled silicon nanocrystals in plasma enhanced chemical vapor deposition grown SiOxNy/SiO2 superlattices (2011)
28	On the nitrogen and oxygen incorporation in plasma-enhanced chemical vapor deposition (PECVD) SiOxNy films (October 2001)
29	US Patent No. 3,849,204

30	OXIDATION OF SILICON (OXY)NITRIDE AND NITRIDATION OF SILICON DIOXIDE: MANIFESTATIONS OF THE SAME CHEMICAL REACTION SYSTEM? (1990)
31	Oxidation of silicon nitride films in an oxygen plasma (March 1999)
32	Physical and electrical characterisation of oxynitride films produced by plasma oxidation of deposited silicon nitride layers (1995)
33	Suppression of hydrogen-ion drift into underlying layers using plasma deposited silicon oxynitride film during high-density plasma chemical vapor deposition (November 2006)
34	<i>Alidouble Inc., v. Taiwan Semiconductor Manufacturing Company Limited.</i> , Case No. 2:22-cv 00298-JRG (E.D. Tex), Docket Control Order.
35	Curriculum Vitae, Ron Maltiel
36	Xiao, Chapter 10 - CVD and Dielectric Thin Film
37	Stefanov, Design and Performance of a Pinned Photodiode CMOS Image sensor (2018)
38	Plasma-Therm: PECVD and HDPCVD Basics (2015)
39	Wolf & Tauber, Silicon Processing for the VLSI Era, Volume 1: Process Technology

V. LEGAL PRINCIPLES

19. I am not a lawyer and I do not have formal training in patent law. I do, however, have practical experience with patents and the patenting process from my involvement in the prosecution of my U.S. patents. Any representations I make in this declaration regarding the law, however, are as I understand the law to be as explained to me by the lawyers from Rimon, P.C. I have used my understanding of these legal principles when forming my opinions.

A. LEGAL PRINCIPLES OF CLAIM INTERPRETATION

20. I understand that in an IPR petition filed after November 13, 2018, terms of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent. Regarding a POSITA, I understand that a POSITA has ordinary creativity, and is not an automaton.

B. LEGAL PRINCIPLES OF ANTICIPATION

21. I understand that a patent claim is invalid if it is anticipated by a prior art reference. Anticipation requires that every element of a claim be disclosed expressly or inherently in a single prior art reference so that the disclosure effectively puts the public in possession of the invention. For the claim to be anticipated implicitly, I understand that the reference must make clear that the missing descriptive matter in the claim of the patent is necessarily or implicitly present in the allegedly anticipating reference, and that it would be so recognized by one of ordinary skill in the art.

C. LEGAL PRINCIPLES OF OBVIOUSNESS

22. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single

prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

23. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;

- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

24. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

VI. PERSON OF ORDINARY SKILL IN THE ART

25. The ‘455 Patent describes and claims an invention relating to “[a] method for fabricating image sensors and other semiconductor ICs that controls the amount of hydrogen generated during back-end processing. ‘455 Patent, Abstract, 1:7-9.

26. After reviewing the ‘455 Patent’s specification, claims and prosecution history, in my opinion, a POSITA would have at least a bachelor’s degree in electrical engineering, chemical engineering, or material science. A bachelor’s

degree in one of these subjects is necessary to have a foundation in solid state physics and integrated circuit processing technology. A degree in computer science would not include sufficient chemistry and physics to enable a person to learn the integrated circuit process technology sufficiently to be a POSITA for the '455 Patent. In addition, a bachelor's degree in one of these subjects would give a POSITA a sufficient foundation to understand the role of hydrogen and devices properties as the '455 Patent describes. In addition, a POSITA would have 3-5 years' experience that includes some experience in image sensors. Three to five years' experience is necessary for a POSITA to understand the variability of processing and device interactions.

VII. TECHNOLOGY OVERVIEW

A. Semiconductor Manufacturing Processes

27. In the typical fabrication of semiconductor products, transistors are first created on the surface of a silicon substrate. Then, several layers of metal wires are fabricated above the transistors to connect them, with each layer separated from the next layer by an insulating layer.

28. The fabrication of semiconductor products is a complex process that typically begins with the creation of a silicon wafer. The wafer is then subjected to a series of steps, including deposition, lithography, etching, and metallization. These

steps are used to create the transistors, capacitors, resistors, and other components of the semiconductor product.

29. A semiconductor is typically a solid chemical element or compound that conducts electricity under some specific conditions. This makes it an ideal medium to control electrical current for use in electronic products. The most commonly used semiconductor material is silicon. Semiconductor devices, typically referred to as computer chips, image sensors, die or integrated circuits, are made by depositing thin layers of metals and/or dielectrics

30. The structure of semiconductor devices requires numerous processing steps that start with a single crystal silicon wafer, called a substrate. A processed substrate has hundreds of semiconductor products called dies. Each of these dies may have millions of transistors acting as switches. Transistors are fabricated in the substrate by modifying the structure of the substrate and by building up layers of other materials that are deposited and patterned on the substrate. The fabrication processes create active regions, which readily conduct electricity, and passive regions which are non-conducting or insulating.

31. Key substrate processing technologies include the deposition of thin films of materials and also etching patterns in those materials. Deposited dielectric films are used for isolation, passivation, barrier, masking and antireflective-coating applications in ultra-large-scale integrated (ULSI) semiconductor circuits.

32. Thin films of conductors and insulators can be formed into patterns by using the processes of photolithography in combination with etching. Photolithography is used to transfer a mask pattern etched into a photo mask onto a photosensitive film that has been applied on the silicon wafer's surface. The photosensitive film is called photoresist. During substrate exposure with visible or ultraviolet light, the photo mask with a desired opaque pattern prevents penetration of the light through the opaque pattern, while allowing radiation to pass through the mask's clear glass. The chemical structure of photoresist is such that the light changes its solubility in a developing solution. The photoresist can then be locally removed from the surface of the substrate during a subsequent developing process.

33. The process that immediately follows the photolithography process is the removal of material from areas of the substrate unprotected by photoresist. Various etching techniques are used for this purpose. Etching processes are characterized by their selectivity to a specific material and their degree of anisotropy (vertical etching). For example, the etching agent should attack silicon dioxide, but not photoresist or silicon. Upon completion of the etching, the etching mask is removed.

34. The details of the etching process depend on the etching speed and the thickness (and variation in the thickness) of the layer being etched. The etch process

is typically chosen to have a fast etch rate of the layer being etched and a slow etch of the underlining layer. This ensures that we do not penetrate the underlining layer even if a portion of the layer is etched with a minimal thickness.

B. Image Sensor Technology

35. Generally, an image sensor is an electrical device which captures light and converts the light into electric signals to form an electronic representation of an image. Typically, the light receiving portions are analog circuits which, when exposed to light, create number of charges proportionally to the intensity and duration of the light striking the circuit. This charge is then read out by peripheral circuitry and often converted to digital signals usable by modern computing systems to display or store the information.

36. Semiconductor imaging devices, such as described in the '455 patent, are formed on silicon substrates. In its pure, crystalline form, silicon is a poor conductor. However, by introducing specific ions or impurities into the silicon (a process known as “doping”), silicon can be made to conduct electricity in a controlled fashion. Silicon can be doped to form either an “n-type region” (a region that can donate electrons) or a “p-type region” (a region that can accept electrons, which is also referred to as donating “holes”) depending on the specific ions or impurities used, with each region having unique electrical properties. To indicate relative doping concentrations, it is common to use a “+” or “-” following the doping

type. Thus, a “p-type” region would have a lower doping concentration compared to a “p⁺ region,” which in turn would have a lower doping concentration compared to a “p⁺⁺ region.”

37. The n-type and p-type regions in a semiconductor are formed by shooting ions into the silicon substrate. A p-type region can be formed, for example, by implanting boron into the substrate and activating the boron by a heat treatment at a high temperature. An n-type region can be formed, for example, by implanting phosphorus into the substrate and activating the phosphorus by a heat treatment at a high temperature. The ion implantation energy will determine how deep the ions will be embedded in the substrate, and the dose will determine the doping concentration. An additional heat treatment will diffuse the implanted ions deeper and, in every direction, away from the original implant location.

38. A backside-illuminated image sensor (BSI) is an image sensor where light is sensed from the backside of the substrate, unlike the front side, where the circuit that monitors the sensing are located. Backside sensing has the advantage that light can be sensed from the entire backside of the substrate, without being blocked by circuitry that covers part of the front side.

C. Memory Technology

39. Nonvolatile memories require an additional special conductive layer, such as a polysilicon layer underneath the transistor gate. That layer has to be insulated from layers around it. This special layer is called floating gate.

40. The floating gate has to maintain its memory for ten years, even following more than tens of thousands times of transferring electrons into and out of the floating gate.

41. A POSITA would understand, having several years industry experience, that any hydrogen reaching a floating gate can destroy the data stored in the floating gate. While in an image sensor, hydrogen would decrease noise in the device.

42. Capacitive memory is a volatile memory that stores a bit on a capacitor while the memory is connected to a power source. A POSITA would understand, having several years industry experience, that any hydrogen reaching a capacitor will degrade the bit stored in the capacitor – changing its value. While in an image sensor, hydrogen would decrease noise in the device.

D. TECHNICAL OVERVIEW OF THE '455 PATENT

43. The '455 Patent discloses methods and apparatus for improving image sensors with multiple metal layers connecting transistors and photodiodes in a silicon substrate. An exemplary embodiment of an image sensor device cross-section using three metal layers to connect, sense, and control transistors and photodiodes

in a p-type substrate is detailed in Figure 2 and in the specification of the '455 Patent. '455 Patent, 10:24-11:26 & Figure 2. The structure of the embodiment is shown in Figure 2, which is duplicated below.

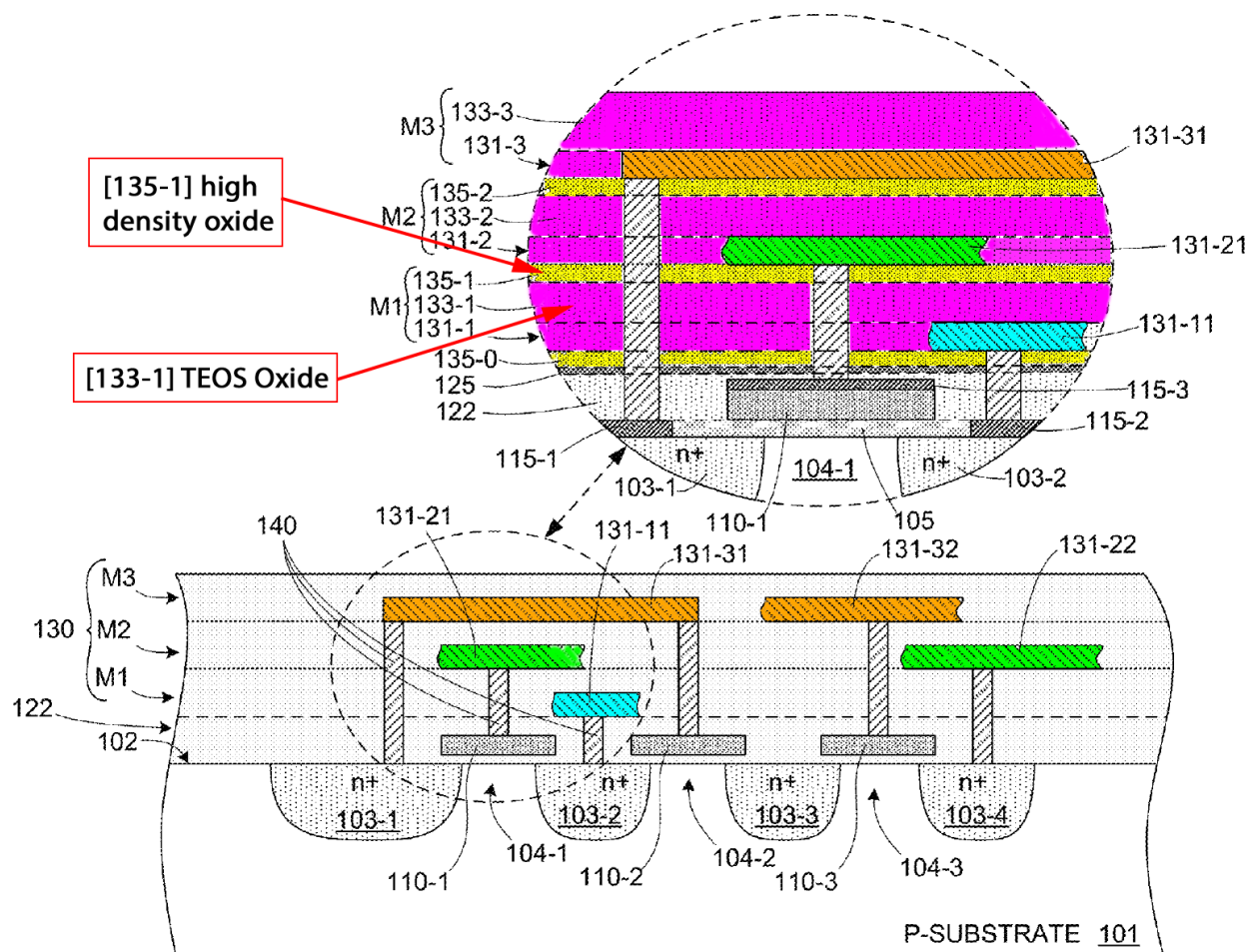


FIG. 2

44. In Figure 2, the metal layers are labeled M1 (blue), M2 (green), and M3 (orange). Each metal layer is coated by an inter-level dielectric insulator (ILD in pink), with a cap layer (yellow) above it, just before the next metal layer is deposited. Only the top metal layer is covered by ILD (pink) without any cap layer above it.

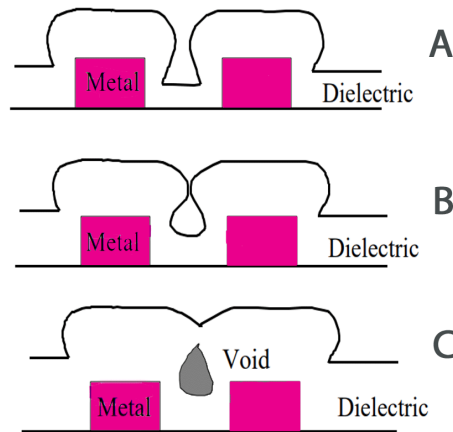
45. In the lower cross-section, all the metal layers are labeled collectively (on the top right) as "131-..." (blue, green, and orange).

46. The '455 Patent overcomes the challenges of image sensors with multiple metal layers and high density of metal lines by covering each layer of the metal lines patterns with TEOS ILD, as depicted in the pink layer in Figure 2. TEOS is Tetraethyloxysilane, $\text{Si}(\text{OC}_2\text{H}_5)_4$ a commonly used source for silicon oxide. TEOS oxide is very conformal oxide, which cover underlying gaps and contours with excellent results makes it a reliable insulator that helps to improve product yield.

47. Poor step coverage can lead to defects such as voids and stringers. Voids are empty spaces that can occur in a semiconductor device. Voids have negative consequences including causing electrical shorts, leaving residue, contaminating the insulator, reducing insulator stability, changing local capacitance, and leading to stringers between metal lines.

48. Figure A, B, C below shows that a void will form between two closely spaced metal lines as the thickness of the deposited layer increases from A to C. This is because the top of the gap will be close to the depositing dielectric before the bottom and sidewalls of the gap are completely filled. I took figures from Ex. Ex. 2013 and modified them to create Figures A – C below.

Void Formation Process



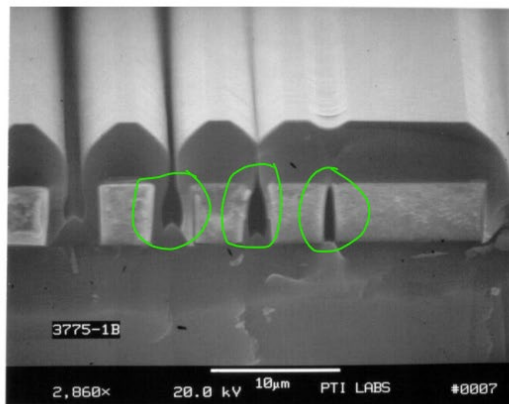
Hong Xiao, Ph. D.

www2.austin.cc.tx.us/HongXiao/Book.htm

I modified figures from Ex. 2013 to create this Figure.

49. The figure below shows several are examples of keyhole voids, which are marked with circles.

- As aspect ratio increases → keyhole more readily formed



Plasma-Therm

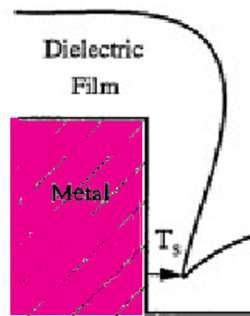
ADVANCED VACUUM
A Plasma-Therm Company

25

I modified a figure from Ex. 2015 to create this Figure.

50. The figure below shows an example of poor step coverage of dielectric on the bottom of metal layer led to non-conformal deposition. The arrow T_s points to the area where the dielectric has not been deposited properly.

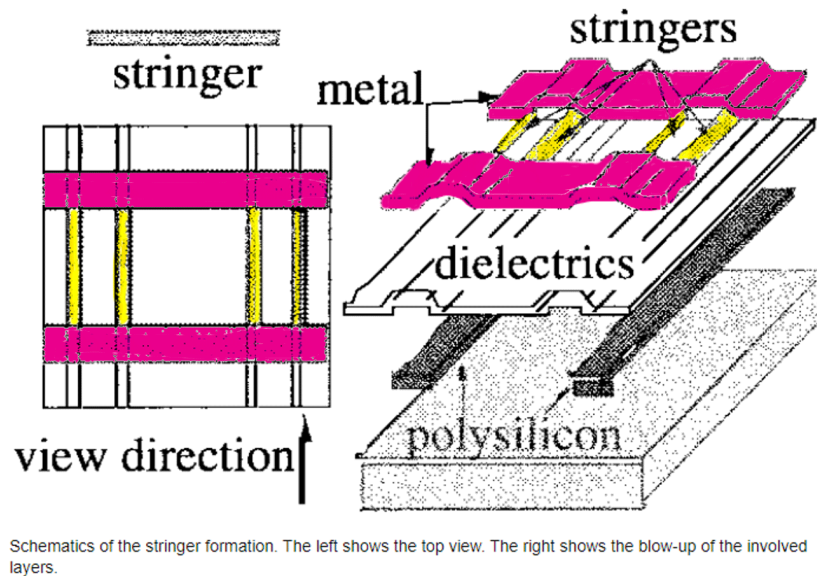
Step Coverage



I modified Figure from Ex. 2013 to create this Figure.

51. Poor step coverage can lead to the formation of stringers in subsequent fabrication steps, when the next metal layer is deposited. Stringers are long, thin lines of material that will form in semiconductor devices due to poor step coverage in a previous fabrication step. Stringers may cause electrical shorts and other problems.

52. The figure below shows stringers, which are residues of metal that remain after the etching of metal lines. The stringers are yellow in the figure, and they are located between two separate metal lines, which are pink:



I modified a figure from Ex. 2016 to create this Figure.

53. TEOS oxide is a silicon oxide dielectric that exhibits excellent conformal deposition it is used as an insulator between metal lines. Undoped silicate glass (USG) has high deposition at low temperatures and similar properties to silicon dioxide. FSG is a fluorine-containing silicon dioxide, which is created by combining $\text{FSi(OC}_2\text{H}_5)_3$ with TEOS and O_2 under plasma environment. FSG improve capacitance between metal lines since its dielectric constant is $\kappa=3.5$, while κ of undoped silicon dioxide is 3.9. Another dielectric that is often used is Borophosphosilicate glass commonly called BPSG. It is silicate glass doped with boron and phosphorus, which is also a conformal glass.

54. TEOS layers, however, can contain trace amounts of hydrogen and water, maintaining a controlled amount of hydrogen accumulation in the transistor channel area is essential for image sensors, as it is a key factor in the performance

and reliability as explained by the ‘455 Patent. The patent discusses the importance of hydrogen for passivating interface states at the silicon/silicon oxide interface and for defects deep in the substrate beneath the transistor layer, as discussed in the patent ‘455:

The importance of hydrogen for the performance of CMOS devices is well known in semiconductor industry. A certain amount of hydrogen at the Silicon-Gate Oxide interface is needed to passivate the Surface States ... At the same time, excess amounts of hydrogen are responsible for device instabilities... Hydrogen atoms are also known to interact with the bulk silicon defects created by ionizing radiation

‘455 Patent, 2:18-34.

55. The ‘455 describes placing a cap layer (yellow in figure 2) of high-density low moisture content oxide material on top of the TEOS layer to prevent hydrogen from diffusing through the TEOS. This cap layer must be thick enough that following next metal etch of the subsequent layer of metal above it, to ensure that at least 100 nm of oxide will remain following over etch of the metal.

56. Every layer deposited in semiconductor manufacturing has a range of thickness values that it will be deposited due to normal fluctuations from day to day. A metal etch that is designed to etch through the full range of allowed metal thicknesses will over-etch into the underlying oxide in areas where the metal is thinnest. As is explained in the ‘455 Patent:

According to the present invention, the amount of hydrogen atoms/ions produced during back-end processing is controlled by forming at least one lower metallization layer by, first, forming an inter-level dielectric

(ILD) layer consisting of a TEOS-based oxide (e.g., one or more of USG or FSG), and then forming a high-density, low-moisture content oxide cap layer Such that the cap layer serves as an etch-stop for subsequent aluminum over-etch (i.e., such that, after Subsequent aluminum etch is completed, the low moisture-content oxide cap layer has a minimum “critical thickness of 100 Å (100 Angstroms) or greater).

‘455 Patent, 2:61- 3:4

57. The ‘455 Patent teaches how to control hydrogen diffusion during fabrication of image sensors through the various metals and inter-level dielectric (ILD) layers that are stacked above the transistor layer, just above the silicon substrate.

58. The ‘455 Patent teaches that using a high-density, low-moisture oxide above every ILD layer up to the topmost ILD will be a barrier to hydrogen diffusion:

According to an exemplary embodiment, cap layers consisting essentially of high-density silane oxide are provided over the ILD layers in each of the lower metallization layers (i.e., the first “M1” layer and all subsequent metallization layers except for the uppermost “last metallization layer). Forming high-density low-moisture (e.g., silane oxide) cap layers on every lower metallization layer minimizes/eliminates hydrogen generation during all back-side aluminum etch processes, thereby maximizing device operating parameters.

‘455 Patent, 6:25-34

59. Several semiconductor processing steps, such as plasma metal etch, can produce hydrogen that subsequently diffuses towards the substrate. This can be mitigated by depositing an oxide cap layer with high density and low moisture

content before depositing the metal layer. The oxide cap layer acts as a barrier to hydrogen diffusion, preventing it from reaching the substrate. This is described in the '455 Patent below:

‘455 Patent, 7:14 – 28.

FIG. 2

60. The oxide cap barrier layer is a critical component of the device. It is deposited over the TEOS ILD layer and must have a final thickness of at least 100 Å. The fabrication process is shown in Figures 3(A)-(C). The process starts with metal deposition (131-A, red) over the cap layer (135, yellow), followed by metal patterning (photoresist 150, orange), and etching. The final remaining thickness of the cap barrier layer underneath the metal in Figure 3(C) must be at least 100 Å. This is critical to ensure the device's performance and reliability, as the oxide cap barrier layer protects the TEOS layer underneath and improves the device's electrical properties.

61. The fabrication sequence starting from cap oxide deposition through metal one etch is described in '455 Patent specification:

Referring to FIG. 3(A), metallization layer 131A (e.g., first metallization layer 131-1) is formed by depositing aluminum using known techniques over pre-metal dielectric layer 122 (i.e., on “additional cap layer 135-0, as indicated in FIG. 2). Cap layer 135A (which in this case represents optional “additional cap layer 135-0 of FIG. 2) is provided with an initial thickness T in the range of 500 Å to 5000 Å, and is formed over pre-metal dielectric layer 122. As indicated in FIG. 3(B), aluminum layer 131A is then deposited on cap layer 135A, and a mask 150 (e.g., photo resist material) is then deposited and patterned using known techniques. As indicated in FIG. 3(C), exposed portions of aluminum layer 131A are then etched using a suitable etchant 155 according to known techniques to form aluminum metallization structures (e.g., aluminum wires 131-11 and 131-12 shown in FIG. 2). Note that cap layer 135A is formed Such that initial thickness T_{CRITICAL} is greater than a Sum of over-etch penetration distance $D_{\text{OVER-ETCH}}$ and a minimum critical thickness T_{CRITICAL} of cap layer 135A.

‘455 Patent, 13:10-28.

62. The fabrication process starting with metal deposition 135 (yellow) followed by patterning the metal with photoresist 150 (orange) and ending with a controlled over etch, leaving a critical thickness of the cap layer of at least 100 Å:

By forming cap layer 135A such that, at the end of the aluminum over-etch the etch portion of cap layer 135A retains a minimum critical thickness T of 100 Å or greater between the etch front and the upper surface of dielectric/ILD layer 122/133A, the generation of hydrogen atoms/ions is greatly reduced

‘455 Patent. 13:41 – 46.

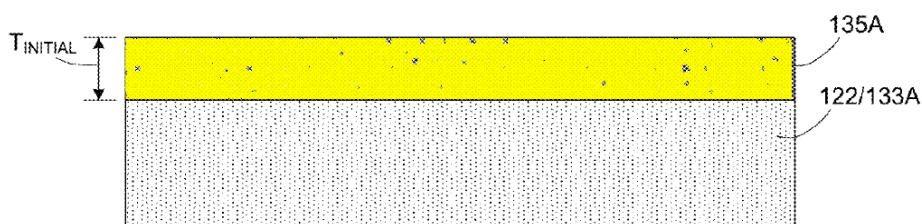


FIG. 3(A)

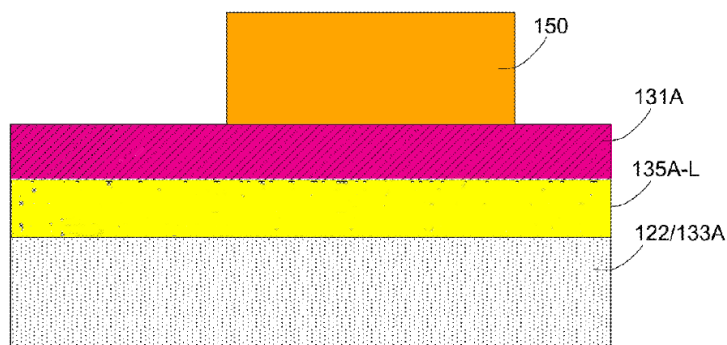


FIG. 3(B)

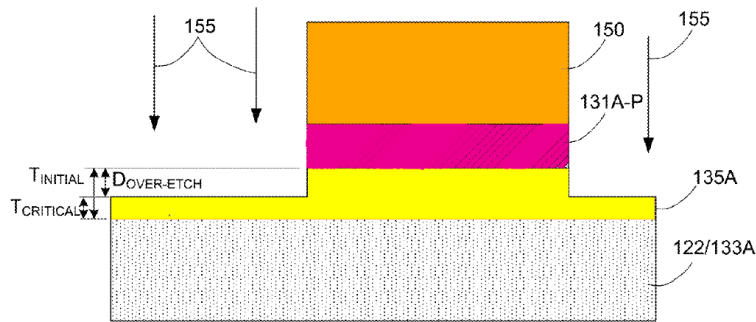


FIG. 3(C)

63. A layer of high density, low moisture oxide between the TEOS oxide layer and the metallization layer would block the migration of hydrogen from the TEOS oxide layer to the gate oxide – silicon interface. The combination of TEOS oxide on the metallization layer with a cap layer of high density, low moisture oxide on the TEOS oxide provides for control – but not elimination – of hydrogen and improved gap filling passivation of the metallization layer. The use of high density, low moisture oxide cap barrier layer is a critical component of the ‘455 Patent invention as it (i) protects the TEOS oxide from a subsequent plasma etching of metal; and (ii) the cap layer above the TEOS oxide layer, does not block the migration of hydrogen from the TEOS oxide layer to the gate oxide – silicon interface. A layer of high density, low moisture oxide between the TEOS oxide layer and the metallization layer would block the migration of hydrogen from the TEOS oxide layer to the gate oxide – silicon interface. The combination of TEOS oxide on the metallization layer with a cap layer of high density, low moisture oxide on

the TEOS oxide provides for control – but not elimination – of hydrogen and improved gap filling passivation of the metallization layer. ‘455 Patent, 5:37 – 6:24.

VIII. CLAIM CONSTRUCTION

A. Claim Interpretation For Claim 1

64. Claim 1 includes the limitations:

forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

forming a patterned metal structure;

forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure; and

forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer;

wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.

‘455 Patent, 17:64-18:7. Based on the language of Claim 1 and based on the specification, a POSITA would understand that Claim 1 requires the “TEOS-based oxide” be in contact with the “patterned metal structure” and be between the “patterned metal structure and the “high-density, low-moisture content oxide material.”

65. First, a POSITA would understand that the ‘455 Patent explains the impact of hydrogen on image sensors and how to control it 34 times in the specification, starting from the first sentence of the abstract:

A method for fabricating image sensors and other semiconductor ICs that controls the amount of hydrogen generated during back-end processing.

‘455 Patent, Abstract.

66. From the specification, a POSITA would understand that the specification explains that hydrogen can diffuse into the transistors of an image sensor and impact its dark current and pattern sensitivity. ‘455 Patent, 2:18-40. The specification then describes, at multiple places, structures that will control the amount of hydrogen in image sensors:

image sensor (CIS) imagers and CCD not always show improvement when the amounts of hydrogen are high. In particular, increased dark current in the outermost pixels of the imager, as well as patterns related to peripheral layout features.

‘455 Patent, 2:61-65. “Dark current” is a problem with image sensors and is not a problem with non-volatile memories or capacitive memories.

67. From the language of Claim 1, a POSITA, who has experience and education in integrated circuit processing would understand that the requirement of “forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure” and then forming a “cap layer over [over the ILD layer] said ILD layer of all of said plurality of metallization layers except for an uppermost said metallization layer” requires by the order of processing that the TEOS layer be between the metallization layer and the cap – high density, low moisture – layer.

68. The POSITA's understanding is consistent with the specification that states the problem to be solved:

What is needed is a modified back-end processing methodology and associated modified back-end metallization structure that facilitates control over the generation and migration of mobile hydrogen atoms/ions, thus improving a semiconductor device's operating performance

'455 Patent, 4:45-50.

69. A POSITA would understand that if the "high density, low moisture" oxide layer were deposited between a TEOS layer and the underlining metallization layer, the order of layers would defeat the purpose of the '455 Patent because, as a POSITA would understand, the high density, low moisture oxide layer would prevent hydrogen atoms/ions from migrating to toward the substrate, underneath transistors gate. '455 Patent, 2:18-24.

70. In addition, a POSITA would understand from the specification that describes the TEOS oxide layer between the high density, low moisture cap layer and the metallization layer and that this description is consistent with the Figures. '455 Patent, 4:53-7:5, Fig. 1 & Fig. 2.

71. A POSITA also would understand an objective of the invention to be to advantageously improve step coverage – gap filling – with TEOS oxide directly over the metallization layer and the high density, low moisture oxide layer over the TEOS oxide layer. '455 Patent, 5:47-52. A POSITA would understand that the

TEOS oxide layers advantageous gap filling characteristic would be lost as the high density, low moisture oxide does not have the advantageous gap filling characteristics of TEOS oxide. ‘455 Patent, 5:53-56. A POSITA would understand that the advantages of the described and claimed combination of TEOS oxide layer and high density, low moisture oxide layer is only obtained if the TEOS oxide layer is deposited first over the metallization layer and the high density, low moisture layer is then deposited second over the TEOS oxide layer. ‘455 Patent, 11:1-16.

72. A POSITA would also understand that there are no disclosures in the prosecution history of the ‘455 Patent that teach a high density, low moisture oxide layer deposited first over a metallization layer followed by a TEOS oxide layer deposition later over the high density, low moisture oxide layer.

B. Claim Interpretation For Claims 17 & 19

73. Claim 17 includes the limitations:

forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structured, and

forming a cap layer of the ILD layer,

wherein forming the cap layer comprises forming a high-density, low moisture content oxide material having a minimum thickness of 100 Å

‘455 Patent, 20:14-20.

74. For the reasons I discuss above, based on the language of Claim 17 and based on the specification, a POSITA would understand that Claim 17 requires the

“TEOS-based oxide” be over the “patterned metal structure” followed by forming of the “high-density, low-moisture content oxide material.”

75. Claim 19 includes the limitations:

a back-end metallization structure formed on the pre-metal dielectric layer, the back-end metallization structure including a plurality of metallization layers formed in a stack, each of the metallization layers including a patterned aluminum layer and an interlevel dielectric (ILD) layer comprising TEOS-based oxide that is formed over the patterned aluminum layer,

wherein at least one of the plurality of metallization layers includes a cap layer formed on the ILD layer, and

wherein the cap layer of all of said plurality of metallization layers except an uppermost said metallization layer comprises a silane oxide layer having a minimum thickness of 100 Å.

‘455 Patent, 20:47-59.

76. For the reasons I discuss above, based on the language of Claim 19 and based on the specification, a POSITA would understand that Claim 19 requires the “TEOS-based oxide” be in contact with the “patterned metal structure” and formed above the TEOS an “high-density, low-moisture content oxide material.”

IX. SUMMARY OF PETITIONER’S CITED REFERENCES

77. I understand that Petitioner cites two references, Ex. 1003 (hereinafter, “Oshima”) and Ex. 1006 (hereinafter “Nagai”), as primary references. Petitioner further cites five references, Ex. 1007 (hereinafter “Lee”), Ex. 1008 (hereinafter “Crook”), Ex. 1009 (hereinafter “Miyazaki”), Ex. 1010 (hereinafter “Wang”, and

Ex. 1011 (hereinafter “Omi”) as secondary references with which Petion combines the primary references.

A. Oshima

78. Where the ‘455 Patent describes and claims methods for fabricating an image sensor, Oshima describes a non-volatile memory. Oshima, Abstract (“A non-volatile memory cell”). Non-volatile memories are not strictly comparable to image sensors. Where the ‘455 Patent discloses the advantage presence and diffusion of hydrogen, ‘455 Patent, 5:63 – 6:24. Oshima seeks to prevent the presence of hydrogen and to prevent the diffusion of any hydrogen that is present. Oshima, ¶¶ 5-7 & 36.

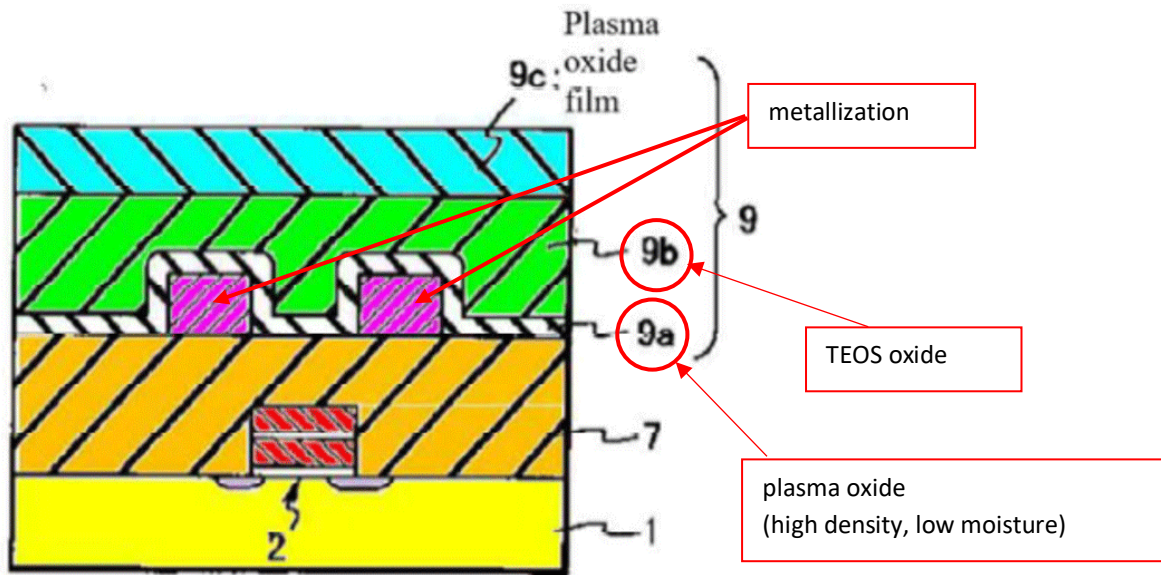
I understand that Petitioner described Oshima:

Next, Oshima teaches forming, in order, *a plasma oxide film 9a*, a TEOS oxide film 9b (green), and a plasma oxide film 9c (cyan).

Petition, at 12 (emphasis added). “Plasma oxide film 9a” is plasma oxide film – that is high density, low moisture oxide. “Plasma oxide 9b,” is TEOS oxide and is in contact with metallization layer.

79. Specifically, Oshima deposits high density, low moisture oxide – “plasma oxide film 9a” – directly on the identified metallization layer. Oshima, Fig. 4, ¶¶ 27 & 36-37.

(FIG. 4)

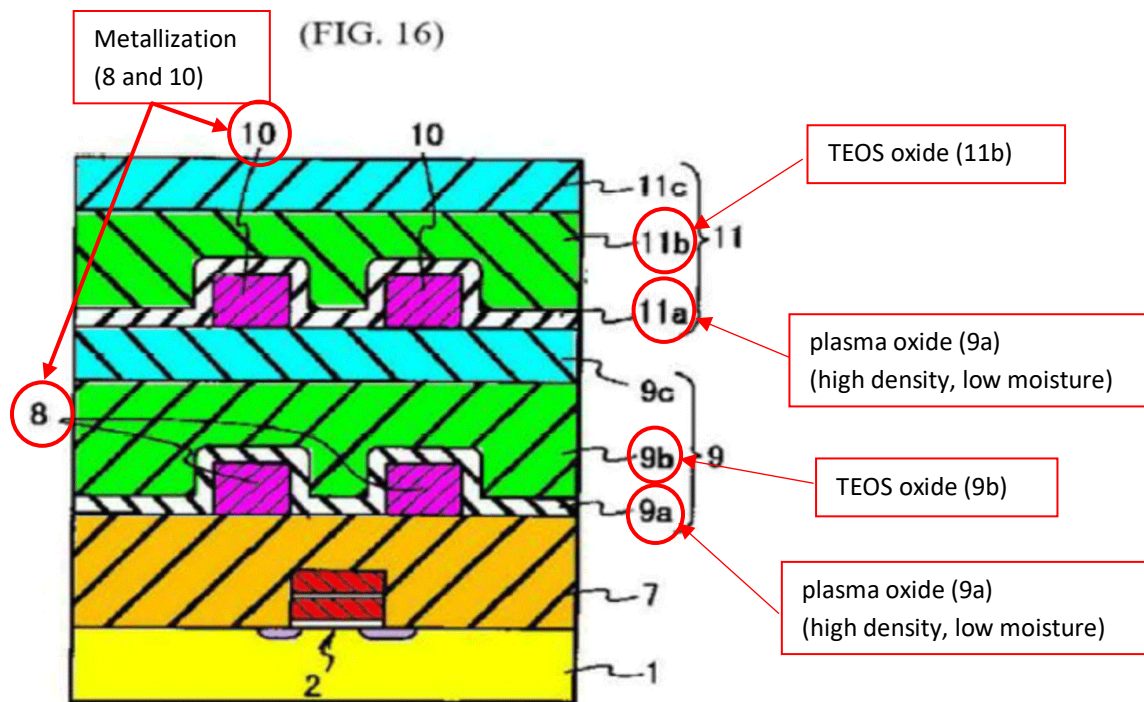


80. Petitioner recreated Figure 4 from Oshima, as Figure 4 shows, layer 9a is plasma oxide film – high density, low moisture silicon oxide. Figure 4 also shows that layer 9b is TEOS oxide. Petitioner, 13. I understand that Petitioner described Oshima:

Next, Oshima teaches forming, *in order*, a plasma oxide film 9a, a TEOS oxide film 9b (green), and a plasma oxide film 9c (cyan). *Id.* at [0023] [0027], Fig. 4; Ex. 1020 ¶52. The plasma oxide film 9a is a silicon oxide film deposited by plasma CVD using mixed gas containing silane (SiH₄) and N₂O gas. *Id.* at [0023], [0002]. The TEOS oxide film 9b is deposited by CVD using a source gas of TEOS and F₂. *Id.* at [0023].

Petition, 13 (emphasis added).

81. The Petitioner again described Oshima's disclosure with reference to Figure 16, high density, low moisture oxide over the metallization layer with TEOS oxide over the high density, low moisture oxide. *Id.* at 13 – 14.



Petition, 14 (annotated); Oshima, ¶¶ 36-40 & 45. Similarly, from Figure 16, and the Petitioner, layer 11a – on the metallization layer 10 is high density, low moisture oxide. Oshima, ¶¶ 0040 & 0045 and layer 11b is TEOS oxide. Petitioner 14; Oshima, ¶ 45.

82. Unlike the '455 Patent, Oshima consistently discloses a plasma oxide layer on the metallization layer with a TEOS oxide layer over the plasma oxide layer.

83. I understand that the Institution Decision characterized Oshima:

Oshima teaches forming a first trace layer from aluminum or a similar trace material. *Id.* ¶¶ 21-22. A “plasma oxide film ... is deposited on the “first trace layer,” and a “TEOS oxide film ... is further deposited thereupon.” *Id.* ¶ 23. “After the TEOS oxide film ... has been leveled, annealing is performed,” and then a “plasma oxide film ... is deposited over the entire surface of the TEOS oxide film.” *Id.* ¶ 27. This film has “the thickness required to prevent hydrogen diffusion without accruing defects.” *Id.* Above this layer, Oshima teaches forming a second metal

trace layer, then “a plasma oxide film, “and “a TEOS oxide film, “and “a plasma oxide film.” *Id.* ¶¶ 44-45. Finally, Oshima teaches forming a third metal trace layer, then “a passivation film.” *Id.* 146. The passivation film includes a “TEOS oxide film” and a “plasma nitride film.” *Id.* 139.

Institution Decision, 13 – 14 (emphasis added).

84. In all in disclosures, Oshima discloses depositing “plasma oxide film” – high density, low moisture oxide – on the metallization layer first, then depositing TEOS oxide. Oshima never discloses or suggests the teaching of the ‘455 Patent of depositing TEOS oxide on the metallization layer, then depositing high density, low moisture oxide on the TEOS oxide layer.

85. Oshima discloses that its objective is to prevent the diffusion of hydrogen, hence the high density, low moisture plasma oxide over the metallization layer – with an objective of no hydrogen from the TEOS oxide layer migrating to the silicon substrate interface. Oshima, Abstract & ¶ 0007. In contrast, one of the ‘455 Patent’s objectives – in both the specification and the claims is to “control” the quantity and migration of hydrogen. ‘455 Patent, Abstract.4:45-50.

B. Nagai

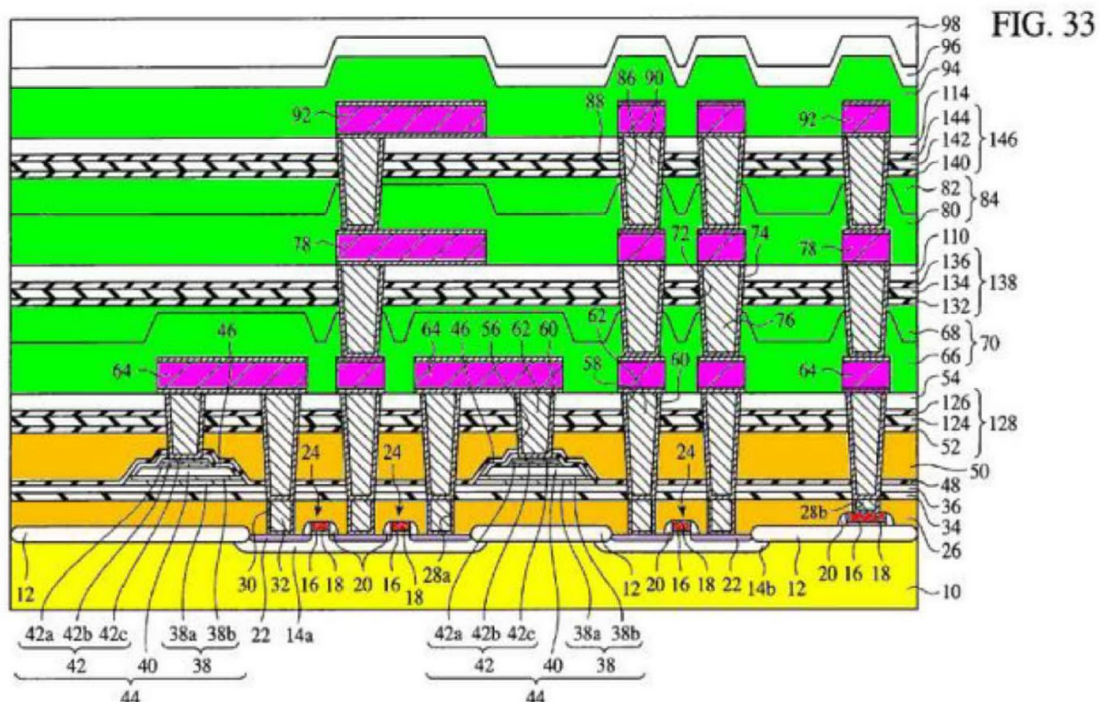
86. Petitioner’s second primary reference Nagai describes a capacitive memory; it does not describe an image sensor. Nagai, 2:7. As Nagai’s description is a capacitive memory, Nagai’s objective is to limit the presence and to prevent the diffusion of hydrogen. Nagai, 2:24.

87. Petitioner describes Nagai:

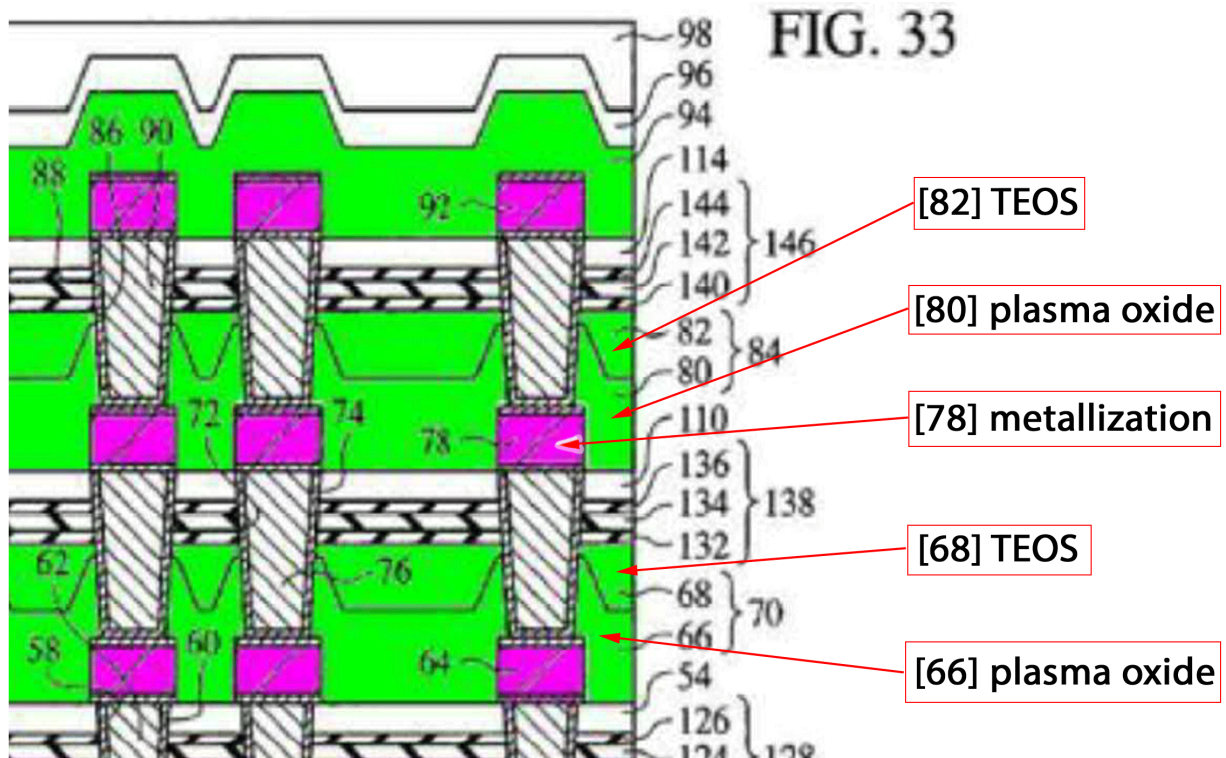
Over each metal interconnection, silicon oxide films 70, 84, and 94 are formed, each by plasma TEOS CVD. Ex. 1006 at 22:21 34, 23:31 43, 24:43 49. Over the silicon oxide film 94, silicon nitride film 96 and polyimide film 98 are formed. Ex. 1020 ¶60.

Petition at 17.

88. Petitioner is neither accurate nor adequately forth coming. Petitioner fails to describe that each of “silicon oxide films 70, 84, and 94” are themselves composed of layers. Taking each in turn, “[I]nter-layer insulation film 70” is composed of “silicon oxide film 66” that is “high density plasma enhanced CVD” and then silicon oxide film 68 that is formed by plasma TEOS CVD.” Nagai, 22:21–34.



Petition, 18 (annotated).



Nagai at Fig. 33 (enhanced portion, annotations added).

89. Nagai at 22:21-34 discloses a high density, low moisture oxide layer directly on the metallization layer that thereby prevents diffusion of hydrogen. Nagai does not disclose the ‘455 Patent’s advantageous use of TEOS oxide on a metallization layer with a cap layer of high density, low moisture oxide on the TEOX oxide.

90. Nagai discloses that “silicon oxide film 84” is composed of multiple, different oxide films:

Next, the layer film 78 is patterned by photolithography. Thus, the interconnection (the second metal interconnection) 78 of the layer film is formed (see FIG. 18).

Next, the silicon oxide film 80 of a 750 nm-thickness is formed by, e.g., high density plasma enhanced CVD.

Next, the silicon oxide film 82 of a 1100 nm-thickness is formed by plasma *TEOS CVD*. The silicon oxide film 80 and the silicon oxide film 82 form the inter-layer insulation film 84.

The silicon oxide film 80 is formed by high density plasma enhanced CVD, and then the silicon oxide film 82 is formed by plasma TEOS CVD here.

Nagai, 23:31-43 (emphasis added). Nagai teaches a high density, low moisture oxide layer directly over the metallization layer with a TEOS oxide layer on the high density, low moisture oxide. Nagai, 23:31-43.

91. Finally, Petitioner is inaccurate and incomplete in its description of “silicon oxide film 94” that Nagai describes as:

Next, the silicon oxide film 94 of a 700 nm-thickness is formed by, e.g., high density plasma enhanced CVD.

The silicon oxide film 94 is formed here by high density plasma enhanced CVD.

Nagai, 24:43-46. As with all Nagai’s disclosures, the disclosure here is high density, low moisture oxide directly on the metallization layer with a TEOS oxide layer on top of the high density, low moisture oxide. *Id.*.

92. Nagai at 24:43-46 does not disclose a TEOS oxide layer directly on the metallization layer with a high density, low moisture oxide cap.

C. Lee

93. I understand that Petitioner includes Lee to close Petitioner’s admitted deficiency in Oshima:

that Oshima does not expressly disclose [generation] of silane oxide by way of reacting silane (SiH_4) gas with oxygen gas, which is required by claim limitations 2[c] and 7[b].

I understand that Petitioner does not contend that Lee discloses any other limitations of any challenged claim. A POSITA would understand that Lee does not disclose, teach, or suggest depositing TEOS oxide on a metallization layer and depositing high density, low moisture oxide on the layer of TEOS oxide.

D. Crook

94. I understand that Petitioner includes Crook to close a deficiency in Oshima:

Crook discloses treating TEOS-based oxide with a hydrogen plasma to control moisture reabsorption after deposition at lower temperatures.

Petition, 53. A POSITA would understand that Crook does not disclose, teach, or suggest depositing TEOS oxide on a metallization layer and depositing high density, low moisture oxide on the layer of TEOS oxide.

E. Miyazaki

95. A POSITA would understand that Miyazaki does not disclose, teach, or suggest depositing TEOS oxide on a metallization layer and depositing high density, low moisture oxide on the layer of TEOS oxide. Miyazaki patent teaches how to create a contact hole in a dielectric. The dielectric is not a TEOS layer deposited above a patterned metal and is not covered by high density, low moisture oxide.

[0029] The aforesaid metal film is patterned by dry etching using an etching gas containing halogen base gas as a major constituent with the patterned photoresist as an etching mask. Thereby, lower layer interconnections 13a, 13b shown in FIG. 1 are formed.

[0030] Next, a protection film 15 made of a silicon oxide film or a silicon nitride film is formed with a film thickness of 800 nm to 1200 nm on the entire top face of the semiconductor substrate 11 including the lower layer interconnections 13a, 13b by a chemical vapor deposition process or the like.

[0031] A photoresist (not shown) is applied on the protection film 15 and thereafter subjected to exposure and development with a photomask in which openings are formed at required positions corresponding to the lower layer interconnections 13a, 13b, so that the photoresist is patterned.

[0032] Subsequently, the protection film 15 is patterned by dry etching using an etching gas containing carbon tetrafluoride gas as a major constituent with the patterned photoresist as an etching mask, thereby forming contact holes 16 shown in FIG. 1.

[0033] The contact holes 16 are formed by opening the protection film 15 to expose the lower layer interconnections 13a and 13b

Miyazaki.

F. Wang

96. I understand that Wang is U.S. Patent 7, 803,647. A POSITA would understand that Wang does disclose, teach, or suggest Wang does not disclose, teach, or suggest depositing TEOS oxide on a metallization layer and depositing high density, low moisture oxide on the layer of TEOS oxide. Wang discloses a copper metallization process that is based on copper and that does not utilize aluminum.

Wang, 3:47-49 (“MLI130 and ILD 140 may be formed in an integrated process referred as a Damascus process such as a dual Damascus process or a single Damascus process”). A POSITA would understand that the metallization process that Wang discloses does not have the same challenges as the process of the ‘455 Patent or of Petition’s primary references Oshima or Nagai.

G. Omi

97. A POSITA would understand that Omi does not disclose, teach, or suggest depositing TEOS oxide on a metallization layer and depositing high density, low moisture oxide on the layer of TEOS oxide.

X. THE CITED REFERENCES AND THE CHALLENGED CLAIMS

98. “High density, low moisture oxide” is a plasma oxide and is the same as or equivalent to “plasma oxide described in Oshima or Nagai. Neither high density, low moisture oxide, nor “plasma oxide” is TEOS oxide. Oshima, ¶ 0002; Nagai, 22:21-34.

A. Ground 1: Oshima - Claims, 1, 5, 6, 9 & 19

99. As a first matter, Oshima discloses a non-volatile memory. Oshima, Abstract (“A non-volatile memory cell . . .”). Non-volatile memories are not strictly comparable to image sensors. An objective of Oshima is to prevent – ideally eliminate – generation or migration, or both, of hydrogen. Oshima, ¶¶ 5-7 & 36. In contrast, the ‘455 Patent discloses an image sensor that advantageously includes

controlled amounts of hydrogen and controlled migration of hydrogen from the TEOS oxide layer to the gate oxide – silicon interface. ‘455 Patent, 5:37 – 6:24. The ‘455 Patent states its objective as, among other things, controlling generation and migration of hydrogen. ‘455 Patent, 4:45-50.

100. For my opinions here, I am applying the claim constructions of Claims 1, 17, and 19 that in Section VIII, I described my understanding.

101. I understand that the language of Claim 1 and Claim 19 require that “forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure” and then forming a “cap layer over [over the ILD layer] said ILD layer of all of said plurality of metallization layers except for an uppermost said metallization layer” requires by the order of processing that the TEOS layer be between the metallization layer and the cap – high density, low moisture – layer.

102. Oshima fails to teach or suggest in any way the layer structure of TEOS oxide over a metallization layer with a high density, low moisture oxide cap over the TEOS oxide. See Section IX.A above.

1. Oshima - Claim 1

103. Oshima does not disclose or suggest the limitations from Claim 1 of:

forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

forming a patterned metal structure;

forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure; and
forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer;
wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.

‘455 Patent, Claim 1; Section IX.A.

2. Oshima - Claim 5

104. I understand that Claim 5 depends from Claim 1. ‘455 Patent, Claim 5. As Oshima does not anticipate Claim 1, I understand that Oshima cannot anticipate Claim 1’s dependent claim, Claim 5. See Section IX.Aabove.

3. Oshima - Claim 6

105. I understand that Claim 6 depends from Claim 5 that in turn depends from Claim 1. ‘455 Patent, Claim 6. As Oshima does not anticipate Claim 1 or Claim 5, I understand that Oshima cannot anticipate dependent Claim 6. See Section IX.Aabove.

4. Oshima - Claim 9

106. I understand that Claim 9 depends from Claim 1. ‘455 Patent, Claim 9. As Oshima does not anticipate Claim 1, I understand that Oshima cannot anticipate dependent Claim 9. See Section IX above.

5. Oshima - Claim 19

107. Oshima does not disclose or suggest the limitations from Claim 19 of:

- a back-end metallization structure formed on the pre metal dielectric layer, the back-end metallization structure including a plurality of metallization layers formed in a stack, each of the metallization layers including a patterned aluminum layer and an interlevel dielectric (ILD) layer comprising TEOS-based oxide that is formed over the patterned aluminum layer,
- wherein at least one of the plurality of metallization layers includes a cap layer formed on the ILD layer, and
- wherein the cap layer of all of said plurality of metallization layers except an uppermost said metallization layer comprises a silane oxide layer having a minimum thickness of 100 Å.

‘455 Patent, Claim 19. See Section IX.A. Accordingly, Oshima does not anticipate Claim 19.

B. Ground 2: Oshima In View Of Lee - Claims 2, 3, Or 7

108. I understand that Petitioner only contends that Lee discloses a method of forming silane oxide. Section IX.C. Petitioner does not contend that Lee discloses the limitations of Claim 1 of:

- forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:
- forming a patterned metal structure;
- forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure;
- and
- forming a cap layer over the ILD layer over said ILD layer of

all of said plurality of metallization layers except an uppermost said metallization layer;

wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.

‘455 Patent, 17:64-18:7. Oshima in view of Lee because the limitations of Claim 1 are not disclosed, taught or suggested in the cited prior art Oshima or Lee. Accordingly, a POSITA would not understand that Claim 1 is obvious by Oshima in View of Lee.

1. Oshima In View Of Lee - Claim 2

109. I understand that Claim 2 depends from Claim 1, and as Oshima in view of Lee does not render Claim 1 obvious, I understand that Oshima in view of Lee cannot render Claim 2 obvious. Oshima in view of Lee does not render Claim 2 obvious.

2. Oshima In View Of Lee Does Not Render Claim 3 Obvious

110. I understand that Claim 3 depends from Claim 2 that in turn depends from Claim 1. I understand that as Oshima in view of Lee does not render Claim 1 or Claim 2 obvious, Oshima in view of Lee cannot render Claim 3 obvious.

3. Oshima In View Of Lee - Claim 7

111. I understand that Claim 7 depends from Claim 1 and as Oshima in view of Lee does not render Claim 1 obvious, Oshima in view of Lee cannot render Claim 7 obvious.

C. Ground 3: Oshima In View of Crook - Claim 10

112. I understand that Petitioner only that Crook discloses a method of treating TEOS oxide. Section IX.D. Petitioner does not contend that Crook discloses the limitations of Claim 1 of:

forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

forming a patterned metal structure;

forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure; and

forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer;

wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.

‘455 Patent, Claim 1.

113. I understand that Claim 10 depends from Claim 1. I understand that as Oshima does not render Claim 1 obvious, Oshima in view of Crook cannot render Claim 10 obvious. Oshima in view of Crook does not render Claim 10 obvious as the limitations of Claim 10 are not within the scope of Oshima or Lee.

D. Ground 4: Nagai - Claims 1, 8, Or 11

114. As a first matter, Nagai discloses a capacitive memory. Nagai, 35:32-34:. An objective of Oshima is to prevent – ideally eliminate – generation or migration, or both, of hydrogen. Nagai, 35:8-23.

115. In contrast, the ‘455 Patent discloses an image sensor that advantageously includes controlled amounts of hydrogen; the ‘455 Patent states its objective as, among other things, controlling generation and migration of hydrogen. ‘455 Patent, Abstract, 2:18-34. When the language of Claim 1 is construed such that Claim 1 and requires that “forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure” and then forming a “cap layer over [over the ILD layer] said ILD layer of all of said plurality of metallization layers except for an uppermost said metallization layer” requires by the order of processing that the TEOS layer be between the metallization layer and the cap – high density, low moisture oxide layer – cap layer.

116. Nagai fails to teach or suggest in any way the layer structure of TEOS oxide over a metallization layer with a high density, low moisture oxide cap over the TEOS oxide. See Section IX above.

1. Nagai - Claim 1

117. Oshima does not disclose or suggest the limitations from Claim 1 of:

forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

forming a patterned metal structure;

forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure;
and

forming a cap layer over the ILD layer over said ILD layer of all of said plurality of metallization layers except an uppermost said metallization layer;

wherein forming the cap layer comprises forming a high-density, low-moisture content oxide material having a minimum thickness of 100 Å.

‘455 Patent, Claim 1; Section IX.B. Accordingly, Nagai does not anticipate Claim 1.

2. Nagai - Claim 8

118. I understand that Claim 8 depends from Claim 1. ‘455 Patent, Claim 8. I understand that as Nagai does not anticipate Claim 1, Nagai cannot anticipate Claim 1’s dependent claim, Claim 8.

3. Nagai - Claim 11

119. I understand that Claim 11 depends from Claim 1. ‘455 Patent, Claim 11. I understand that as Nagai does not anticipate Claim 1, Nagai cannot anticipate dependent Claim 11.

E. Ground 5: Nagai In View Of Miyazaki - Claim 12

120. I understand that Claim 12 depends from Claim 1. I understand that Petitioner only contends that Miyazaki discloses forming protective films generally. Pet., 21; Section IX.E. Petitioner does not contend that Miyazaki discloses the limitations of Claim 1 of:

forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

forming a patterned metal structure;
forming an interlevel dielectric (ILD) layer comprising a
TEOS-based oxide over the patterned metal structure;
and
forming a cap layer over the ILD layer over said ILD layer of
all of said plurality of metallization layers except an
uppermost said metallization layer;
wherein forming the cap layer comprises forming a high-
density, low-moisture content oxide material having a
minimum thickness of 100 Å.

‘455 Patent, Claim 1. Nagai in view of Miyazaki cannot, and does not, render Claim 12 obvious because these limitations of Claim 12 are not disclosed, taught or suggested in the cited prior art of Nagai in view of Miyazaki.

F. Ground 6: Nagai In View Of Lee - Claim 15

121. I understand that Claim 15 depends from Claim 1. Nagai does not teach the limitations of Claim 1. Section IX.B. Nagai in view of Lee does not disclose, teach, or suggest the limitations of Claim 15.

G. Ground 7: Nagai In View Of Wang - Claim 16

1. Motivation To Combine

122. As discussed above in Section IX.F, Wang discloses a Damascus metallization process that does not utilize aluminum and that does not have the same challenges as the aluminum metallization process Nagai discloses. Wang, 3:47-49. Accordingly, a POSITA would not be motivated to combine Nagai with Wang.

2. The Scope Of The Cited Prior Art Does Not Disclose, Teach, Or Suggest Claim 16

123. Claim 16 depends from Claim 1, and Nagai in view of Wang does not disclose, teach, or suggest the limitations of Claim 1. Nagai in view of Wang does not, render Claim 16 obvious because these limitations of Claim 16 are not disclosed, taught or suggested in the cited prior art of Nagai in view of Wang.

H. Ground 8: Nagai In View Of Omi - Claims 17 Or 18

1. Claim 17

124. I understand that Petitioner contends that Omi discloses using TEOS oxide for an “inter-layer TEOS insulating film. Petition, 24. Petitioner does not contend that Omi discloses, teaches, or suggests:

forming a plurality of metallization layers over the pre-metal dielectric layer, wherein forming at least one of said metallization layers includes:

forming a patterned metal structure; forming an interlevel dielectric (ILD) layer comprising a TEOS-based oxide over the patterned metal structure; and

forming a cap layer over the ILD layer, wherein forming the cap layer comprises forming a high density, low-moisture content oxide material having a minimum thickness of 100 Å,

wherein said semiconductor integrated circuit comprises an array of image sensing pixels disposed inside a rectangular imaging region of said semiconductor substrate

‘455 Patent, Claim 1. As discussed above in Section IX.B, Nagai does not disclose these limitations. In addition, I understand that Petitioner does not contend that Omi

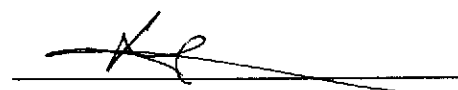
discloses, teaches, or suggests these limitations so Nagai in view of Omi does not, render Claim 17 obvious because these limitations of Claim 17 are not disclosed, taught or suggested in the cited prior art of Nagai in view of Omi.

2. Claim 18

125. Claim 18 depends from Claim 17, and Nagai in view of Omi does not disclose, teach, or suggest the limitations of Claim 17. Accordingly, Nagai in View of Omi does not render Claim 18 obvious because Nagai in view of Omi does not disclose, teach, or suggest the limitations of Claim 17.

126. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of the '455 patent.

Dated: Oct 11, 2023

A handwritten signature in black ink, appearing to be 'RM', is written over a horizontal line.

RON MALTIEL