

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.

Patent Owner.

U.S. Patent No. 6,168,965

PETITION FOR *INTER PARTES* REVIEW

OF U.S. PATENT NO. 6,168,965

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EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 6,168,965 (“the ’965 Patent”)
1002	Prosecution File History for the ’965 Patent
1003	Declaration of Dr. Konstantinos P. Giapis
1004	U.S. Patent No. 6,429,036 (“Nixon”)
1005	U.S. Provisional Patent Application No. 60/116144 (“Nixon Prov.”)
1006	Intentionally omitted
1007	Intentionally omitted
1008	Intentionally omitted
1009	Certified translation of JP H10-116977 (“Muramatsu”)
1010	Certified translation of Sakai, H., <i>CSP Development of ShellCase Type</i> , in THE J. OF JAPAN INST. OF INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS, vol. 12, no. 3, pp. 144-147 (1997) (“Sakai”)
1011	U.S. Pat. No. 5,455,455 (“Badehi I”)
1012	U.S. Pat. No. 5,818,404 (“Lebby”)
1013	Fossum, E., <i>Active Pixel Sensors: Are CCDs Dinosaurs?</i> , in CHARGE-COUPLED DEVICES AND SOLID STATE OPTICAL SENSORS III, SPIE, vol. 1900, pp. 2-14 (1993) (“Fossum II”)
1014	Intentionally omitted
1015	Barbe, F., <i>A Tradeoff Analysis for CCD Area Imagers: Frontside Illuminated Interline Transfer vs. Backside Illuminated Frame Transfer</i> , in PROCS., CCD APPLICATIONS CONF., pp. 13-20 (1973) (“Barbe”)

Exhibit No.	Description
1016	Fossum, E., <i>Ultra-low power imaging systems using CMOS image sensor technology</i> , in ADV. MICRODEVICES AND SPACE SCIENCE SENSORS, SPIE, vol. 2267, pp. 107-111 (Sept. 23, 1994) (“Fossum I”)
1017	Brissot, L., et al., <i>High-definition CCDs for enhanced definition television</i> , in HIGH-RESOLUTION SENSORS AND HYBRID SYSTEMS, SPIE, vol. 1656, pp. 427-436 (Aug. 12, 1992) (“Brissot”)
1018	<i>Introduction to Quantum Efficiency</i> , TELEDYNE, available at https://www.photometrics.com/learn/imaging-topics/quantum-efficiency (“Quantum Efficiency”)
1019	U.S. Patent No. 5,244,817 (“Hawkins”)
1020	U.S. Patent No. 5,270,221 (“Garcia”)
1021	U.S. Patent No. 5,494,833 (“Martin”)
1022	WO1999/040624 (“Badehi II”)
1023	<i>CMOS Fundamentals</i> , SILICON IMAGING, available at http://www.siliconimaging.com/cmos_fundamentals.htm#:~:text=Passive%2Dpixel%20sensors%20(PPS),the%20photosites%20and%20their%20connections (“CMOS Fundamentals”)
1024	U.S. Patent No. 8,063,963 (“Dierickx”)
1025	Intentionally omitted
1026	Intentionally omitted
1027	U.S. Patent No. 5,143,855 (“Pace”)
1028	U.S. Patent No. 4,982,079 (“Yagyu”)
1029	U.S. Patent No. 6,960,795 (“Rhodes”)

Exhibit No.	Description
1030	“Digital camera,” <i>Encyclopedia Britannica</i> (https://www.britannica.com/technology/webcamming) (“Digital camera”)
1031	Sorrell, C., <i>Inside the Nobel Prize: How a CCD Works</i> , WIRED (Oct. 7, 2009), available at https://www.wired.com/2009/10/ccd-inventors-awarded-nobel-prize-40-years-on/ (“How a CCD Works”)
1032	CCD vs. CMOS, TELEDYNE DALSA, available at https://www.teledynedalsa.com/en/learn/knowledge-center/ccd-vs-cmos/ (“CCD vs. CMOS”)
1033	<i>Introduction to Charge-Coupled Devices (CCDs)</i> , NIKON, available at https://www.microscopyu.com/digital-imaging/introduction-to-charge-coupled-devices-ccds (“Intro to CCDs”)
1034	<i>What Is a CMOS Image Sensor?</i> , NANOTEC MUSEUM, available at https://www.tel.com/museum/exhibition/principle/cmos.html (“What is a CMOS Image Sensor”)
1035	Fowler, B., et al., <i>CMOS image sensors – past, present and future</i> , Proceedings ICIS 2006 – International Congress of Imaging Science (2006) (“Fowler”)
1036	Intentionally omitted
1037	Intentionally omitted
1038	U.S. Patent No. 9,257,479 (“Koizumi”)
1039	Intentionally omitted
1040	Intentionally omitted
1041	Intentionally omitted

Exhibit No.	Description
1042	Fossum and Hondongwa, <i>A Review of the Pinned Photodiode for CCD and CMOS Image Sensors</i> , IEEE Journal of the Electron Devices Society (May, 2014) (“Fossum III”)
1043	<i>Back-illuminated sensor</i> , WIKIPEDIA, available at https://en.wikipedia.org/wiki/Back-illuminated_sensor
1044	U.S. Pat. No. 6,642,963 (“Assadi”)
1045	U.S. Pat. No. 5,227,313 (“Gluck”)
1046	U.S. Pat. No. 5,789,774 (“Merrill”)
1047	Shweky, Itzik, et al., <i>CSP optoelectronic package for imaging and light detection applications</i> , SPIE, SENSORS, CAMERAS, AND APPLICATIONS FOR DIGITAL PHOTOGRAPHY, vol. 3650, pp. 63-68 (Mar. 22, 1999) (“Shweky”)
1048	WOLF, STANLEY, SILICON PROCESSING FOR THE VLSI ERA: VOLUME 2 – PROCESS INTEGRATION, LATTICE PRESS (1990) (“Wolf”)
1049	U.S. Pat. No. 3,492,763 (“Walsh”)
1050	“PB-159: Digital Camera On A Chip,” PHOTOBIT (“PB-159 datasheet”)
1051	Curriculum Vitae of Dr. Konstantinos P. Giapis
1052	Declaration of Dr. Sylvia Hall-Ellis
1053	Affidavit of Nathaniel E Frank-White
1101	Badihi, A., <i>ShellCase Ultrathin Chip Size Package</i> , in PROCS. INT’L SYMPOSIUM ON ADV. PACKING MATERIALS, PROCESSES, PROPERTIES AND INTERFACES (IEEE CAT. NO. 99TH8405), IEEE, pp. 236-40 (Mar. 1999) (“Badihi”), attached as Exhibit 1101 to Declaration of Dr. Sylvia Hall-Ellis
1102	Intentionally omitted

Exhibit No.	Description
1103	Sakai, attached as Exhibit 1103 to Declaration of Dr. Sylvia Hall-Ellis
1104	Intentionally omitted

LIST OF CHALLENGED CLAIMS

Claim	Limitation
1pre	1. A method of producing backside illuminated image sensors comprising the steps of:
1a	producing a plurality of image sensor circuits on a wafer having first and second surfaces each of the image sensor circuits being formed on the first surface and including a matrix of light-sensitive pixel regions extending into the wafer from the first surface;
1b	securing the wafer onto a protective substrate such that the first surface faces the protective substrate;
1c	removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface;
1d	securing a transparent substrate onto the second surface of the wafer, thereby producing a waferwise sandwich; and
1e	slicing the waferwise sandwich, thereby defining a plurality of backside illuminated image sensors.
2pre	2. The method according to claim 1, wherein the step of securing the protective substrate onto the first surface comprises
2a	depositing an adhesive onto the protective substrate, and then
2b	placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive.
7pre	7. The method according to claim 1, wherein the step of securing a transparent substrate onto the second surface comprises
7a	depositing an adhesive onto the second surface, and then
7b	placing the transparent substrate onto the deposited adhesive
8pre	8. The method according to claim 7,

Claim	Limitation
8a	wherein the step of removing material includes separating each of the plurality of image sensor circuits; and
8b	wherein the step of depositing the adhesive onto the second surface further comprises depositing adhesive into interstices located between the plurality of image sensor circuits, thereby protecting the image sensor circuits.
9pre	9. The method according to claim 1, further comprising the step of
9a	forming metal leads on the protective substrate after the step of securing the transparent substrate,
9b	wherein the metal leads are connected to metal contact pads located on the first surface of the wafer.
10pre	10. The method according to claim 1, wherein the step of securing the wafer onto a protective substrate further comprises:
10a	forming a passivation layer on the first surface of the wafer;
10b	forming openings in the passivation layer; and
10c	securing the protective substrate onto the passivation layer.

I. INTRODUCTION

Taiwan Semiconductor Manufacturing Company Limited (“TSMC” or “Petitioner”) respectfully requests *inter partes* review of claims 1, 2, 7, 8, 9, and 10 (“the Challenged Claims”) of U.S. Patent No. 6,168,965 (“the ’965 patent”) pursuant to 35 U.S.C. § 311 and 37 C.F.R. § 42.100.

II. TECHNOLOGY BACKGROUND

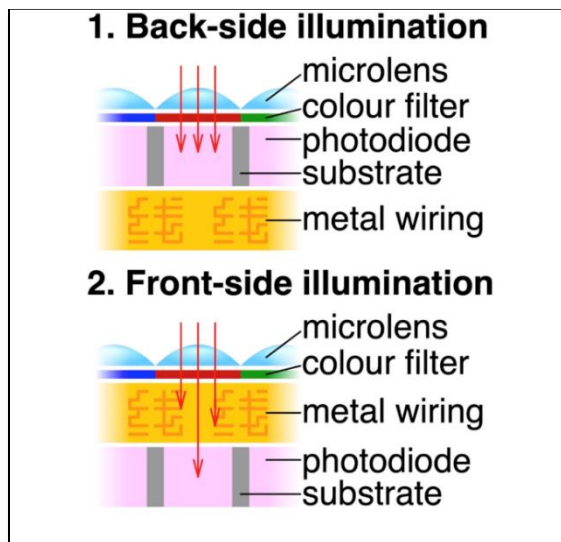
A. CMOS Image Sensors (CIS)

Complementary metal-oxide semiconductor (“CMOS”) image sensors are ubiquitous in today’s electronic devices, such as digital cameras. Ex. 1013, 6; Ex. 1035, 136-137; Ex. 1003, ¶¶37, 41. These devices use CMOS sensors to measure light intensity and color. Ex. 1030; Ex. 1003, ¶¶37, 41. Today, CIS is the industry standard. Ex. 1013, 3; Ex. 1003, ¶¶37-42.

A CIS is comprised of a pixel array, each pixel having a photodetector (e.g., photodiode), a CMOS transistor switch to allow direct access to the pixel, antireflective coating, and microlens. Ex. 1034; Ex. 1003, ¶41. It was common knowledge that such image sensors would have “a matrix of pixels comprising light sensitive elements [that] constitute[] an image sensor.” Ex. 1024, 1:34-41; Ex. 1003, ¶41.

A CIS can be either frontside illuminated (FSI) or backside illuminated (BSI). Ex. 1015, 13 (comparing “backside illuminated” and “frontside illuminated” image sensors); Ex. 1003, ¶¶43-45. The difference between a BSI image sensor and an FSI

image sensor is the arrangement of imaging elements in the sensor with respect to incident light to the pixel.



Ex. 1043; Ex. 1003, ¶43. BSI is preferred because it allows the image sensors to achieve higher quantum efficiency than FSI Ex. 1018; Ex. 1019, 1:10-17; Ex. 1020, 4:7-11; Ex. 1021, 2:26-30; Ex. 1003, ¶¶43-45.

B. Removal of Material from Backside of Wafer

It was common practice during the manufacturing of CIS to attach the frontside of the silicon wafer (i.e., the active side) with BSI image sensors to another wafer for support for further processing of the backside and then using a combination of backside grinding and chemical etching techniques to thin the backside of the BSI image sensors to allow the photons to be absorbed by the thinned substrate closer to the photodiode. Ex. 1020, 2:10-22, 6:10-42; Ex. 1022, 14; Ex. 1003, ¶¶46-48. It was conventional to attach a device wafer to a supporting structure or plate before the device wafer is thinned. Ex. 1049, 3:19-66; Ex. 1003, ¶46. In doing so, it was

common practice to apply the adhesive, such as wax, to the supporting structure or plate first before placing the device wafer to the supporting structure or plate. Ex. 1049, 3:19-4:13, Fig. 1; Ex. 1003, ¶46. It was also conventional to reduce the backside substrate thickness so that light is absorbed near the photodiode and to prevent the photogenerated electrons and holes from recombining before they can be collected by the photodiode. Ex. 1003, ¶¶47-48.

C. Passivation Layer in Image Sensors

The use of a passivation layer on the frontside (active) surface of an image sensor was well-known. Ex. 1003, ¶49. In 1990, Wolf describes that “a passivation layer is deposited over the entire top surface of the wafers. This is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging.” Ex. 1048, 273, Table 4.5. Gluck discloses a “passivation coating” that serves to “protect[] the device on the opposite side of the wafer” when its backside is etched. Ex. 1045, 5:26-34, Fig. 7.

It was also well-known to form openings in the passivation layer. Ex. 1003, ¶50. For example, Gluck discloses passivation coating 260 covers and protects aluminum bond pads 250 during the etching process from the backside of the wafer. Ex. 1045, 5:26-34, Fig. 7. Subsequently, the **bond pad contacts** are opened through **passivation coating 260** using “standard procedures” before “dicing and packaging operations,” as illustrated in Gluck’s Figure 7:

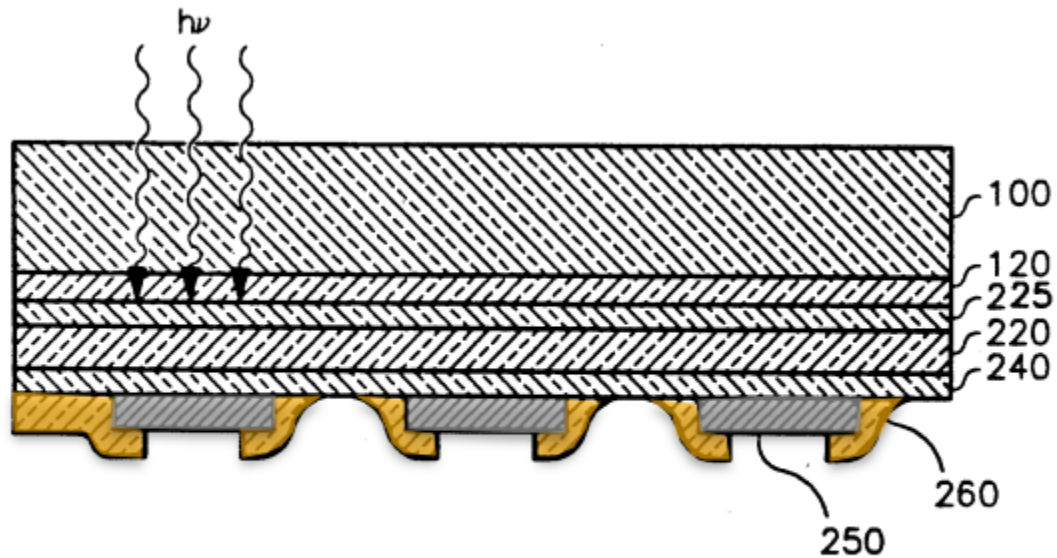


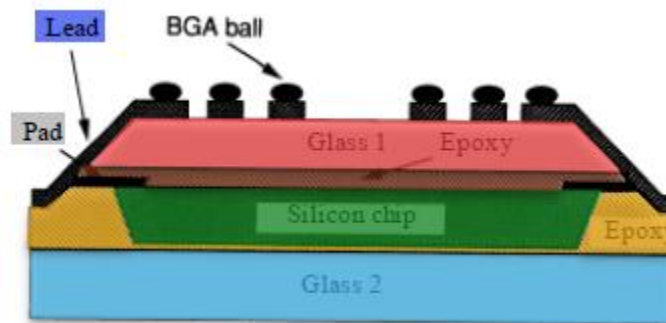
FIG. 7

Id., Fig. 7.

D. Wafer-Level Packaging Process

Wafer-level packaging of BSI image sensors was well known. Ex. 1010, 144-146, Figs. 3, 5; Ex. 1003, ¶51. For example, it was well-known to package a die with a protective shell comprised of glass sheets at the top and bottom of the die. Ex. 1010, 144-146, Figs. 3, 5; Ex. 1003, ¶51. It was also well-known to provide pads in between the top glass sheet covering the top or active surface of the silicon die and the silicon die itself, and to provide electrical leads on the top glass sheet that are connected the pads as part of this conventional packaging process. Ex. 1010, 144, 146, Figs. 3, 5; Ex. 1003, ¶51. Sakai's Figure 3 illustrates the resulting

packaged die, with the **silicon chip** sandwiched by **glass 1** and **glass 2** and the pads connected to the **electrical leads**:



Id., Fig. 3.

III. OVERVIEW OF THE '965 PATENT¹

The '965 patent, titled “Method for making backside illuminated image sensor,” was filed on August 12, 1999.

The '965 patent discloses conventional backside illuminated image (BSI) image sensors are expensive because (1) they are made using nonstandard complementary metal-oxide-semiconductor (CMOS) processes and (2) packaging the BSI image sensors is complex. *Id.*, 4:13-29. To address these problems, the '965 patent discloses a method for making and packaging BSI image sensors using standard wafer processing techniques and equipment. *Id.*, 8:47-50.

The method starts with a wafer having image sensor circuits formed on the wafer's frontside, also known as the active side since that is where all the

¹ Coloration and annotations added to figures unless otherwise noted.

microelectronics of the image sensor circuits are located. *Id.*, 5:19-26, 6:12-16. The frontside of the wafer is secured to a protective substrate and then the backside of the wafer is thinned until the pixels in the image sensor circuits can detect light passing through the backside of the wafer. *Id.*, 6:28-56. The thinning process include a grinding process, such as planar erosion, and a chemical etching process. *Id.*, 6:57-7:37. After thinning, a transparent substrate is secured to the backside of the wafer, forming a waferwise sandwich. *Id.*, 7:57-8:3. The waferwise sandwich is sliced to produce individually packaged image sensors. *Id.*, 8:40-46.

Figures 4(A)-4(I) are cross-sectional views illustrating the process steps of one such method in accordance with one embodiment of the '965 patent. Figure 4(A) shows the method starts with a **wafer 300** having **image sensor circuits 100** extending into the **wafer 300**'s first (frontside) surface 310,² which is secured by an **adhesive layer 420** onto a **protective substrate 410**:

² The first (frontside) surface 310 is mislabeled in Figure 4(A) and should actually point to where the “image sensors 100 [are] formed.” Ex. 1001, 6:27-32, 9:4-8; Ex. 1003, ¶27 n.1. The location of the first (frontside) surface 310 is correctly identified in Figures 3(B) and 4(C)-4(E). Ex. 1001, Figs. 3(B), 4(C)-4(E); Ex. 1003, ¶27 n.1.

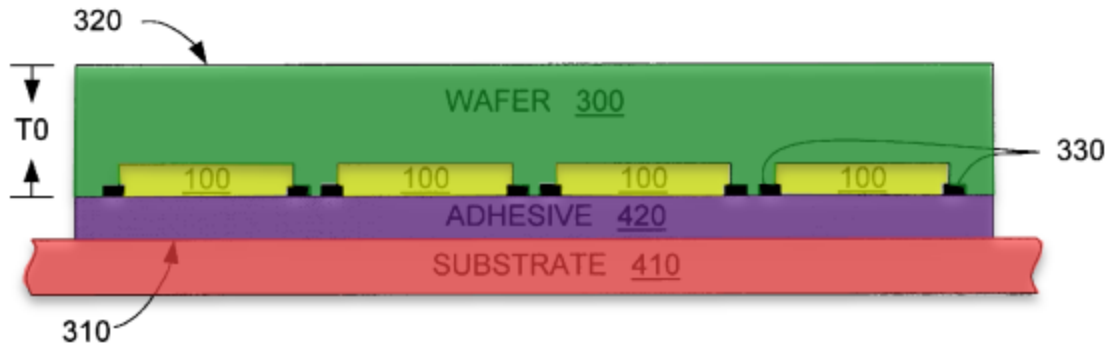


FIG. 4(A)

Id., Fig. 4(A). “Each image sensor circuit 100 also includes ... metal contact pads 330 extending onto first surface 310 of wafer 300” and “metal lines (not shown) are formed on wafer 300 and provide connection between metal contact pads 330 and the matrix of light sensitive pixel regions 110” *Id.*, 6:10-19.

Figures 4(B) and 4(C) illustrate the process steps of removing material from the second (backside) surface 320 of **wafer 300** with a planar erosion process 433 and a chemical etchant 435 “until the light-sensitive pixel region of image sensor circuits 100 are effectively exposed through the second surface 320 [so] that the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through the second surface 320”:

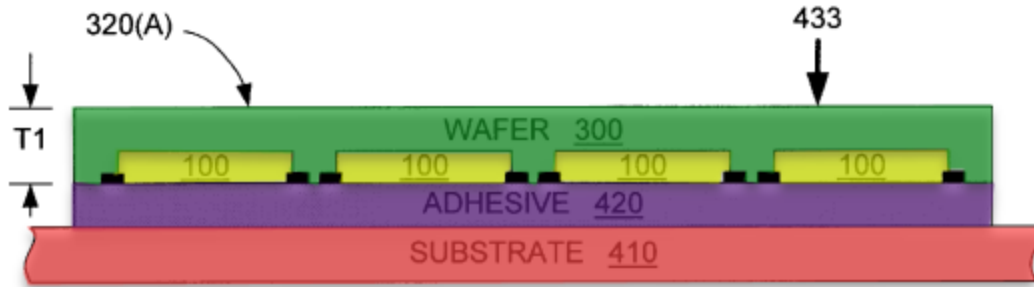


FIG. 4(B)

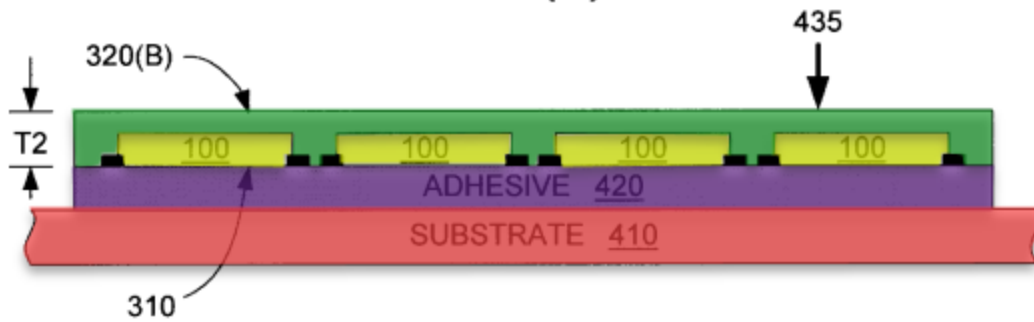


FIG. 4(C)

Id., 6:46-7:19, Figs. 4(B)-(C).

Figure 4(D) illustrates the process step of separating individual image sensor circuits 100 from each other to form dies 300-1 to 300-4 on **protective substrate 410**:
410:

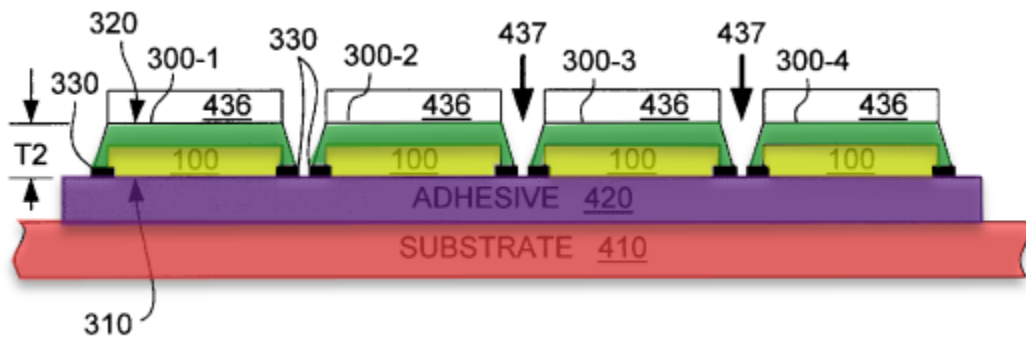


FIG. 4(D)

Id., Fig. 4(D), 7:20-37 (“[S]econd surface 320 is scribed long predetermined dice lines and then etched using an etchant 437 to separate the individual image sensor circuits 100”).

Figure 4(E) illustrates a process step of securing a **transparent (glass) substrate 440** onto the backside surface 320 of **wafer 300** using a **layer 430** of epoxy, producing a waferwise sandwich:

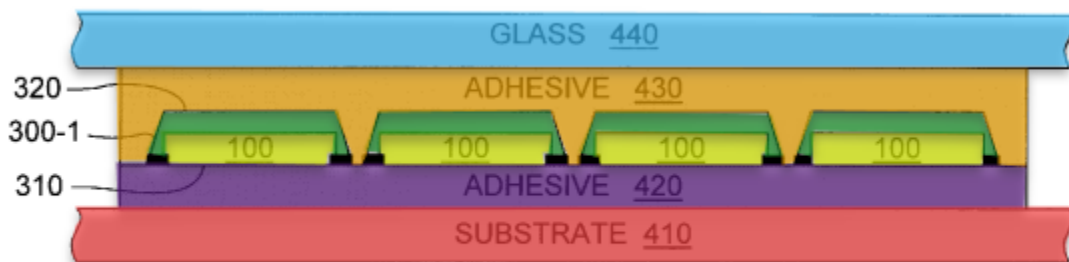


FIG. 4(E)

Id., Fig. 4(E), 7:52-8:3.

Figure 4(F) illustrates a process step of “form[ing] grooves 455 through **protective substrate 410** and **adhesive layer 420** to expose metal contact pads 330”:

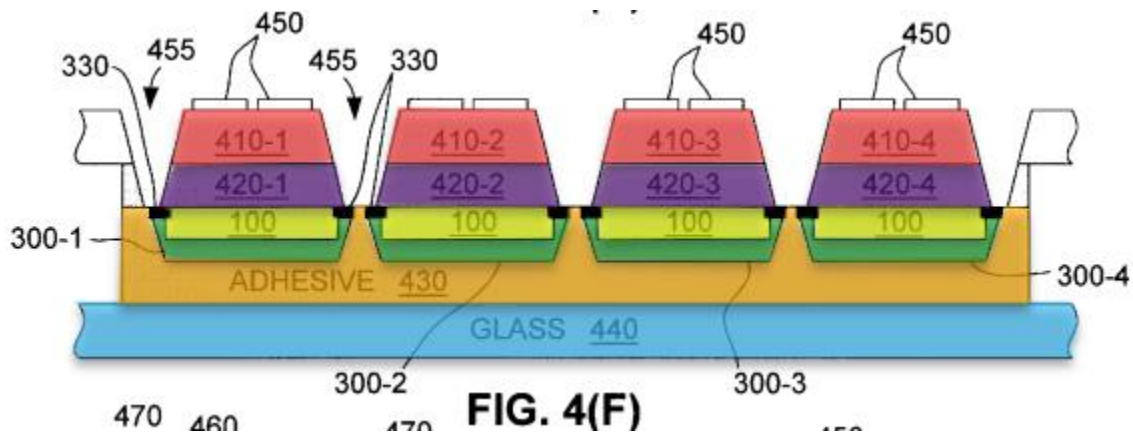
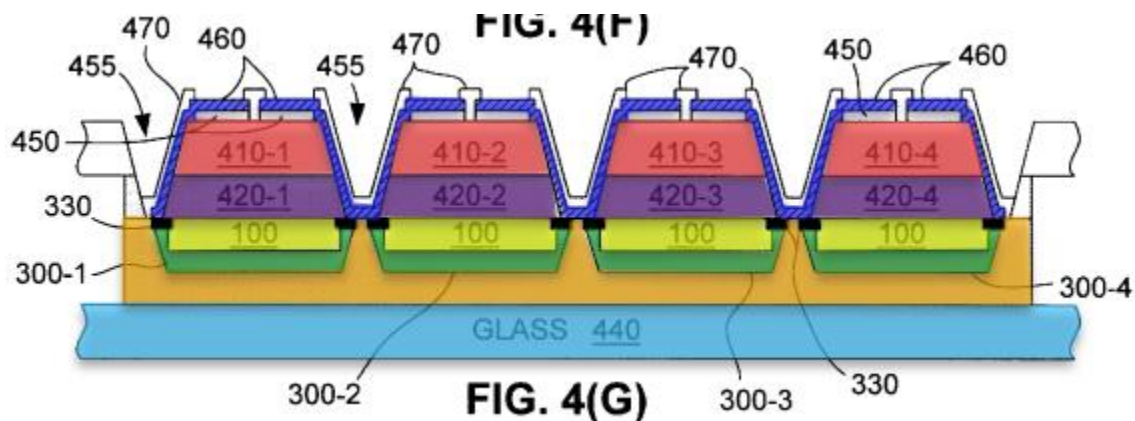


FIG. 4(F)

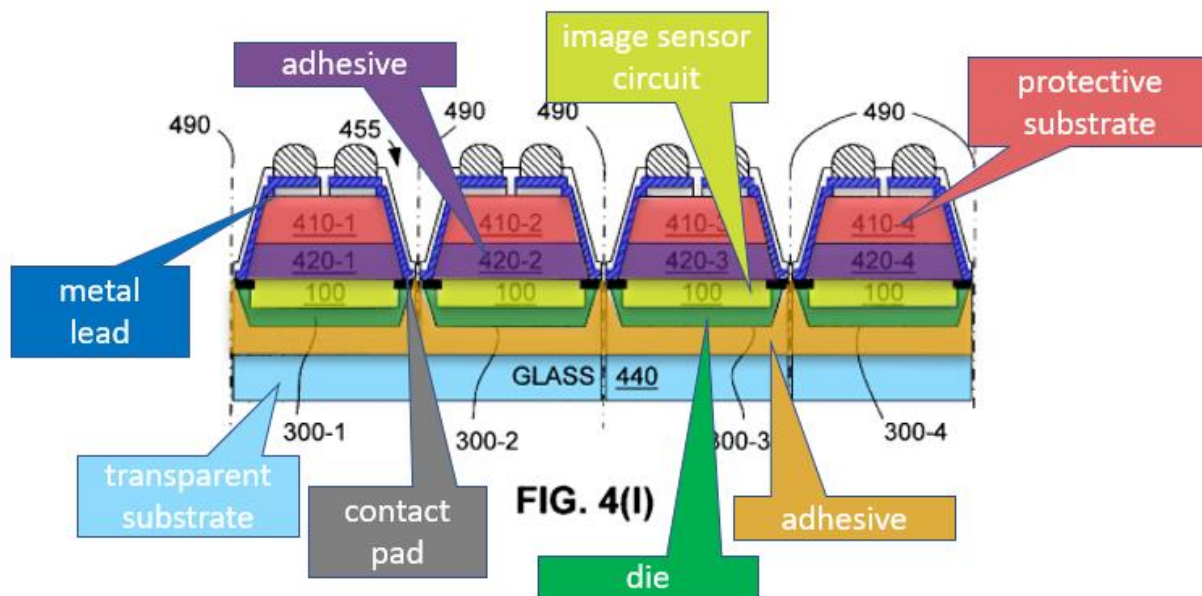
Id., Fig. 4(F), 8:4-26.

Figure 4(G) illustrates a process step of forming **metal leads 460** in grooves 455 to contact the exposed metal contact pads 330:



Id., Fig. 4(G), 8:27-35.

Figure 4(H) illustrates a process step of “form[ing] solder bumps 480 using known ball-gridarray (BGA) technology” on the “exposed portion of an associated **metal lead 460**,” resulting in the CMOS image sensor illustrated in Figure 4(I) below, where BSI image sensors in a waferwise sandwich about to be diced:



Id., Fig. 4(I), 8:36-46. Each BSI image sensor has a **die 300-1** with an **image sensor circuit 100** and **metal contact pads 330**, which provide access to a matrix of light-sensitive pixel regions 110 and control circuitry 120 in image sensor circuit 100. *Id.*, 6:10-16, Fig. 3(B). “Insulation and metal lines (not shown) ... provide connections between metal contact pads 330 and the matrix of light-sensitive pixel regions 110 and control circuitry 120.” *Id.*, 6:16-19.

Each BSI image sensor further has a die-sized section 410-1 of a **protective substrate 410** secured to the frontside surface of **die 300-1** by an **adhesive region 420-1**, a die-sized section of a **transparent substrate 440** secured to the backside surface of **die 300-1** by an **adhesive region**, and **metal leads 460** formed over die-sized section 410-1 and “connected to metal contact pads 330 of each image sensor

circuit 100 to facilitate signal between each image sensor circuit 100 and an external system (not shown).” *Id.*, Figs. 4(H), (I), 8:36-46, 8:4-13.

IV. PROSECUTION OF THE '965 PATENT

The '965 patent issued on January 2, 2001, from U.S. App. No. 09/372,863 (“the '863 Application”), filed on August 12, 1999 with 17 original claims. Ex. 1002. This Petition analyzes invalidity assuming a priority date of August 12, 1999.

In the first office action, dated November 1, 1999, the Examiner issued a restriction requirement because the original claims encompassed two distinct inventions. *Id.*, 46-49. In response, the Patent Owner elected claims 1-11. *Id.*, 52-53.

In a second office action, dated February 18, 2000, the Examiner rejected original claims 1-2, 4-10 as being unpatentable over Patent Owner’s admitted prior art in the '863 Application, i.e., Figures 1 and 2(A)-2(B) and page 7 in view of U.S. Pat. No. 5,455,455 (“Badehi I”) and U.S. Pat. No. 5,818,404 (“Lebby”); original claim 11 as unpatentable over the same admitted prior art in view of Badehi I and Lebby and further in view of the Examiner’s remarks; and original claim 3 as unpatentable over the same admitted prior art in view of Badehi I and Lebby and further in view of the Examiner’s remarks. *Id.*, 54-61. The Patent Owner successfully traversed the Examiner’s rejections based on its arguments that the admitted prior art was not related to backside illuminated image sensors, Badehi I

did not disclose the limitation “removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface,” and Leiby disclosed LED arrays that emit, rather than sense, light. *Id.*, 64-71, 72-75. The Patent Office issued a Notice of Allowance on July 20, 2000. *Id.*, 76.

V. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention would have been a person having a Master’s degree in electrical engineering, computer engineering, or physics with at least two years of industry experience in integrated circuit design, layout, packaging or fabrication. A greater level of experience may compensate for less education, and vice versa. Ex. 1003, ¶¶ 52-55.

VI. CLAIM CONSTRUCTION

For purposes of this proceeding only, Petitioner does not believe the claim terms need to be construed to resolve the prior art issues presented in this Petition. The Challenged Claims are invalid under their plain and ordinary meaning. Ex. 1003 ¶¶ 56.

VII. CITED ART³

A. Nixon

Nixon claims priority to the Nixon Prov., which includes two documents: (1) an Invention Disclosure Technical Description (“IDTD”); and (2) an article entitled “A CSP Optoelectronic Package for Imaging and Light Detection Applications” by Shweky et al. (“Shweky”). Shweky is incorporated in the Nixon Prov. as a prior art reference, upon which the IDTD claims an improvement using wafer level processing and packaging techniques for CMOS imaging, including its backside. Ex. 1003, ¶¶57-58. Accordingly, the disclosures of both Shweky (as the basis upon which the Nixon invention was based) and IDTD (as the disclosure of that improvement) are relevant to the Nixon invention.

Nixon qualifies as prior art at least under pre-AIA § 102(e) because the Nixon Prov. was filed (January 14, 1999) before the presumed priority date (August 12, 1999) of the ’965 patent. *See Dynamic Drinkware, LLC, v. National Graphics, Inc.*, 800 F.3d 1375 (Fed. Cir. 2015). Nixon was not cited during prosecution of the ’965 patent.

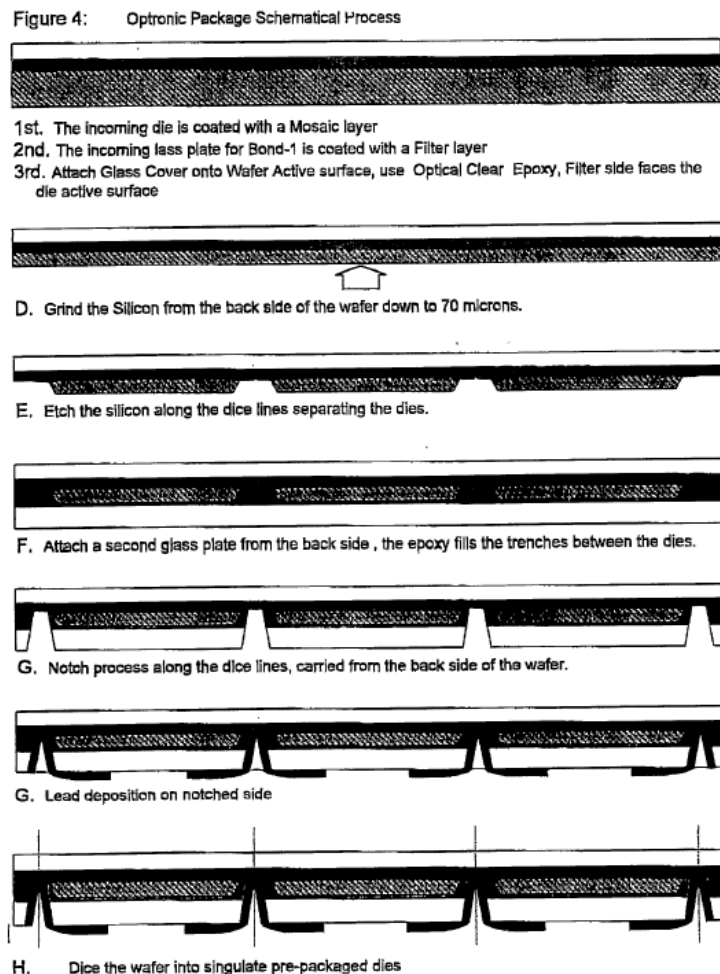
1. *Dynamic Drinkware*

As required by *Dynamic Drinkware*, the Nixon Prov. provides support for at least claim 1 of Nixon. Ex. 1003, ¶¶58-72.

³ Pre-AIA 35 U.S.C. §102 applies. MPEP §2159.02.

Nixon [1pre] A method of manufacturing an image sensor comprising:

The Nixon Prov. provides support for this claim element of Nixon. Ex. 1003, ¶¶59-60. Specifically, the Nixon Prov. discloses the “[b]ackside imaging using wafer level processing techniques to obtain thinning and integrated packaging of the image sensor.” Ex. 1005, IDTD, 4. Shweky’s Figure 4 also provides support for this limitation, as it illustrates a manufacturing process for image sensors:



Id., Shweky, Fig. 4.

Nixon [1a] attaching a first cover layer to an active surface of a silicon wafer;

The Nixon Prov. provides support for claim element of Nixon. Ex. 1003, ¶¶61-63. Shweky discloses a process step of attaching a **(first) glass cover** to the active surface of a **wafer** in Figure 4:

Figure 4: Optronic Package Schematical Process



- 1st. The incoming die is coated with a Mosaic layer
- 2nd. The incoming lass plate for Bond-1 is coated with a Filter layer
- 3rd. Attach Glass Cover onto Wafer Active surface, use Optical Clear Epoxy, Filter side faces the die active surface

Ex. 1005, Shweky, 8, Fig. 4. At the end of the manufacturing process, Shweky discloses dicing the wafer into packaged image sensors. *Id.*, Shweky, 8, Fig. 4.

Relatedly, IDTD also discloses the resulting packaged image sensor has a **glass plate (first glass cover)** attached to the active surface (where **pixels** are located) of a **silicon die** in Figure 1:

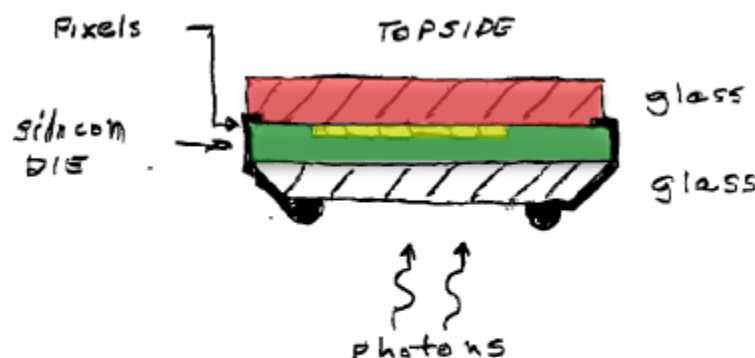


Figure 1.

Id., IDTD, 4-5, Fig. 1.

Nixon [1b] attaching a second cover layer to an opposite surface of the silicon wafer;

The Nixon Prov. provides support for this claim element of Nixon. Ex. 1003, ¶¶64-66. Shweky discloses a process step of attaching a **second glass plate (second glass cover)** to the backside of the **wafer** in Figure 4:



F. Attach a second glass plate from the back side, the epoxy fills the trenches between the dies.

Ex. 1005, Shweky, 8, Fig. 4.

Relatedly, IDTD discloses the resulting packaged image sensor has **another glass plate (second glass cover)** attached to the backside of the **silicon die** in Figure 1:

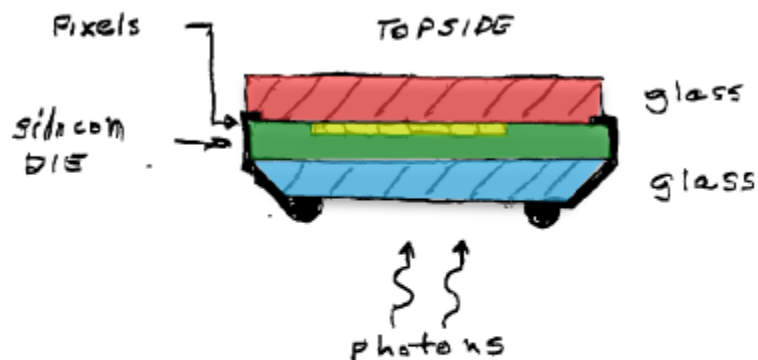


Figure 1.

Id., IDTD, 4-5, Fig. 1.

Nixon [1c] notching the silicon wafer along the second cover layer; and

The Nixon Prov. provides support for this claim element of Nixon. Ex. 1003, ¶¶67-68. Shweky discloses that “[d]eep notches are drawn between the dice, so as to reveal the pads cross section.” Ex. 1005, Shweky, 8. Shweky discloses the process step of forming **notches** along the backside of the **wafer** through the **second glass plate (second glass cover)** in Figure 4:



Id., Fig. 4.

Nixon [1d] forming electrical interconnections on the notched surface of the silicon wafer;

The Nixon Prov. provides support for this claim element of Nixon. Ex. 1003, ¶¶69-70. IDTD discloses that conventionally, the bump contacts and interconnect lines are located on the backside of the wafer for FSI image sensors. Ex. 1005, IDTD, 4, Fig. 1. Shweky discloses a process step of depositing a metal layer “to contact the metal pads at their cross sections.” *Id.*, Shweky, 8. **Leads** are deposited on the notched sides of the **wafer**:



Id., Fig. 4.

Nixon [1e] wherein the image sensor is light sensitive from a back side.

The Nixon Prov. provides support for this claim element of Nixon. Ex. 1003, ¶¶71-72. IDTD illustrates the packaged image sensor receiving photons from the backside:

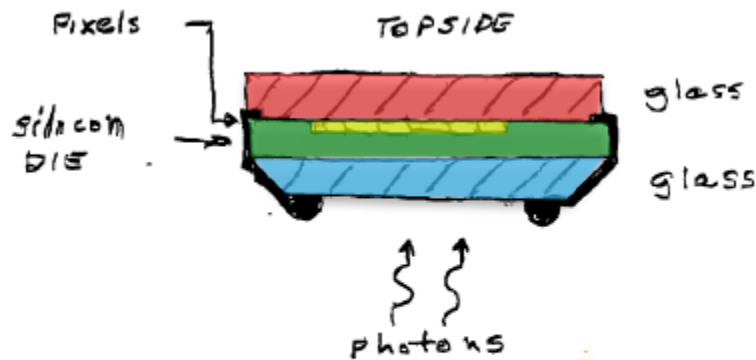


Figure 1.

Id., IDTD, 4-5, Fig. 1.

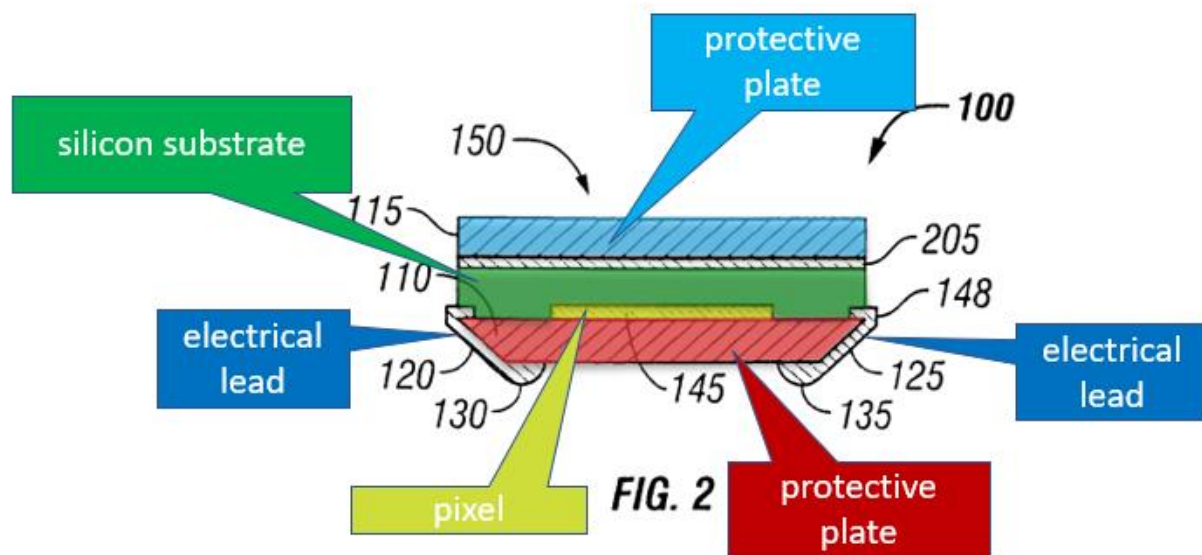
2. Overview of Nixon

Nixon “relates to ... the manufacturing of CMOS image sensors capable of backside illumination.” Ex. 1004, 1:8-10. Nixon’s BSI CMOS image sensors are “packaged at the wafer level using semiconductor manufacturing processes,” and “[t]he manufacturing process ... results in lower cost, particularly for smaller dies.”

Id., 1:65-2:1, 3:16-17.

Nixon’s Figure 1 and 2 illustrate two embodiments of a BSI CMOS image sensor 100 and Nixon’s Figure 4 illustrates the manufacturing process for the image

sensor 100 of Figures 1 and 2. *Id.*, 1:56-57, 1:61-62, Figs. 1, 2, 4. Both embodiments have a **silicon substrate 105** sandwiched between a **protective plate 110** and a **protective plate 115**. *Id.*, 2:1-3, Figs. 1, 2. **Pixels 145** are formed on the active surface of **silicon substrate 105** facing **protective plate 110**. *Id.*, 2:8-10, Figs. 1, 2. Protective plates **110** and **115** are made from glass plates. *Id.*, 2:26-28, 2:49-52. The embodiment in Figure 2 has **electrical leads 120, 125** and pads 130, 135 formed on **protective plate 110** at the frontside of image sensor 100 so light can enter unobstructed through **protective plate 115** at the backside of image sensor 100:



Id., Fig. 2, 2:16-22. Both embodiments disclose notching in order to expose the metal pads 130, 135 to be connected with the electrical leads 120, 125, with Figure 1 illustrating notching from the protective plate 115 and Figure 2 illustrating notching from the protective plate 110. *Id.*, Figs. 1, 2, 1:65-2:10, 2:15-22; Ex. 1003, ¶¶73-74.

B. Badihi

Badihi was published on March 14, 1999 and qualifies as prior art at least under pre-AIA § 102(a). Ex. 1101.

Badihi is a printed publication. As set forth in the accompanying Dr. Hall-Ellis declaration, Badihi qualifies as a printed publication because it was published in the *Proceedings International Symposium on Advanced Packaging Materials, Processes, Properties and Interfaces* and was made available in university libraries including the Kurt F. Wendt Engineering Library at the University of Wisconsin – Madison. Ex. 1052, ¶¶49-56. A copy of that library’s online catalog demonstrates that the conference proceedings were available as of March 30, 1999. *Id.*, ¶52. Further supporting the public availability of these proceedings is that a copy of these conference proceedings was indexed by the Library of Congress on March 30, 1999. *Id.*, ¶53; Ex. 1101.

The well-known nature of this and other similar IEEE publications is confirmed by Dr. Giapis. Dr. Giapis states in his declaration that he was aware of the International Symposium on Advanced Packaging Materials, Processes, Properties and Interfaces and that Badihi, along with the other papers presented at that conference (and published in its proceedings) would have been readily available as of the publication of those proceedings. Ex. 1003, ¶75.

Badihi was presented in an IEEE conference and published by the IEEE. The Badihi conference proceedings bears a publication date of 1999 which is inherently reliable and trustworthy given the publication source, the IEEE. Ex. 1101. Indeed, the Board has stated that the “IEEE is a well-known, reputable compiler and publisher of scientific and technical publications, and we take Official Notice that members in the scientific and technical communities who both publish and engage in research rely on information published on the copyright line of IEEE publications.” *Ericsson Inc. v. Intellectual Ventures I LLC*, IPR 2014-00527, Paper 41, at 11 (PTAB May 18, 2015). The Board has further found that “[a]llowing IPR petitioners to rely on the IEEE publication date in an IPR proceeding ... serves the interests of justice.” *Id.* at 12.

Based on this and other library records, Dr. Hall-Ellis concludes that Badihi “was published and publicly accessible on or shortly after March 30, 1999.” Ex. 1052, ¶56.

Moreover, the copies of Badihi in the record are authentic. Exhibit A to Ex. 1053 is an authentic copy of the document as it was published in 1999. Exhibit A is a color version of Badihi obtained from Internet Archive. As set forth in the accompanying Frank-White affidavit, Exhibit A is a true and correct copy of Badihi that was published at the website <http://shellcase.co/il/utlra.html> and captured on

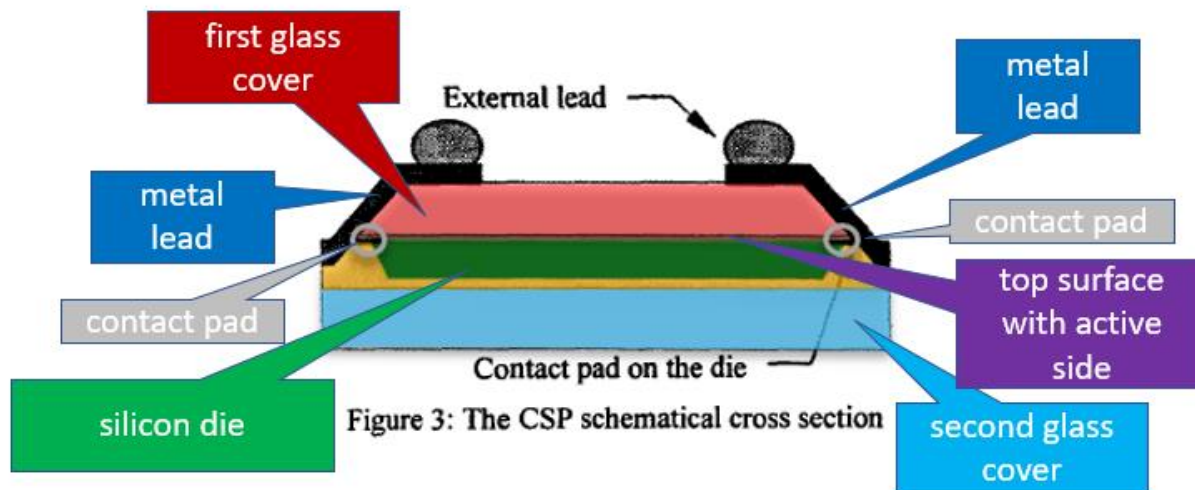
May 23, 2000. Ex. 1053. It is otherwise identical to the other copies of Badihi in the record. This alone establishes its authenticity.

Additionally, Badihi was located in the IEEE database, which is a place it “would likely be,” and as testified to by Dr. Hall-Ellis, is complete, with no visible alterations, and therefore “creates no suspicion about authenticity.” Ex. 1052, ¶49. Additionally, pursuant to FRE § 901(b)(8), Exhibit A of Exhibit 1053 qualifies as an “ancient document,” and is, for this additional reason, authentic.

Badihi discloses a ShellCase Chip Size Package (CSP) for, inter alia, BSI CMOS image sensors. Ex. 1101, 236, 239; Ex. 1003, ¶¶76-77. Badihi’s ShellCase CSPs are made with a “wafer-level packaging process ... [that] can be accomplished with commercial [s]emiconductor wafer processing equipment” and be “based on [s]emiconductor processes.” Ex. 1101, 236, 240. For example, Badihi discloses bonding a first glass cover to the active side of the silicon wafer, etching away the silicon material from the back side of the wafer, bonding a second glass cover to the backside of the wafer, drawing deep notches between dies to expose the bond pads, depositing a metal layer to contact the bond pads, and dicing the wafer to yield individual dies. *Id.*, 237.

Badihi’s Figure 3 illustrates the ShellCase CSP has a **silicon die** (e.g., an **imager die**) sandwiched between a **first glass cover** and a **second glass cover**, with the active side of the **silicon die** facing the **first glass cover**, **contact pads** formed

on the active side of the **silicon die**, and **individuals metal leads** formed on the **first glass cover** to contact the **contact pads**:



Id., 237, Fig. 3; *see also id.*, 237, Fig. 2. Badihi further discloses that the above ShellCase CSP package is a “glass transparent package [that] encases the [i]mager [d]ie in a solid protecting optically clear enclosure,” including, for example, packaged CMOS APS shown in Badihi’s Figure 4. *Id.*, 239, Fig. 4.

C. Assadi

Assadi was filed on June 29, 1998 and qualifies as prior art at least under pre-AIA § 102(e).

Assadi discloses a passivation layer 230 that “[o]verl[ies] the top surface of image sensor 175” and is made, for example, of silicon nitride based on its “particular resistance to environmental contaminants, particularly moisture.” Ex. 1044, 4:35-45, Fig. 3b; Ex. 1003, ¶78. Assadi discloses **bond pads 225**, which may

be on the “top surface of sensor 176” and in bond pad area 240 and that the **passivation layer 230** “overlies the entirety of sensor 175, including ... bond pad area 240,” as illustrated in Assadi’s Figure 3b:

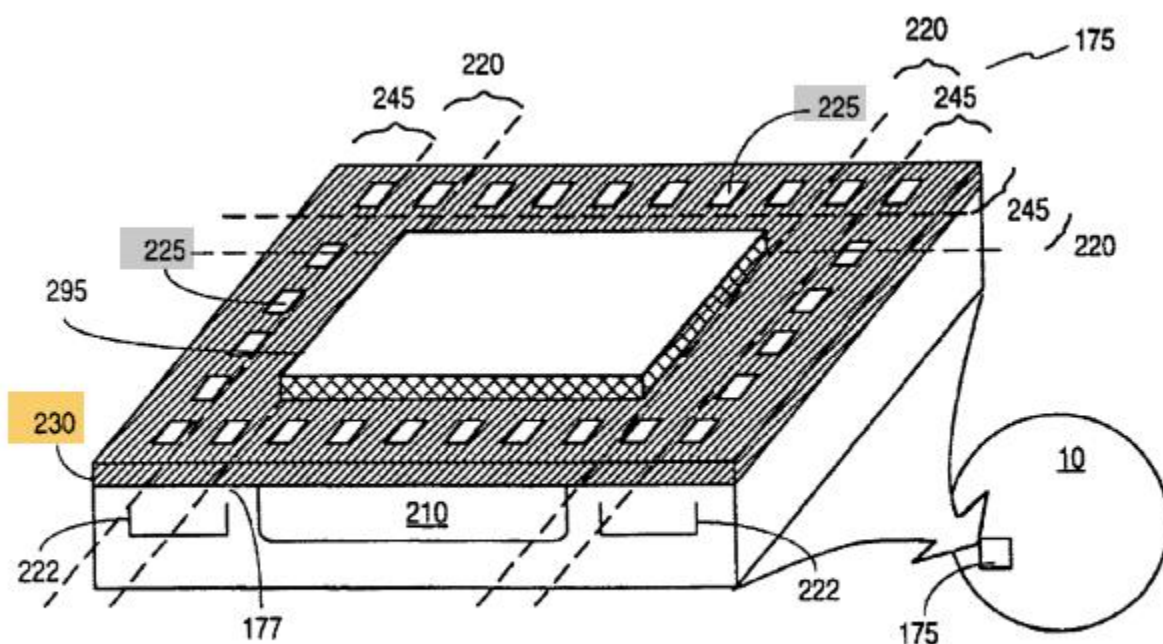


Fig. 3b

Ex. 1044, 4:35-45, Fig. 3b.

VIII. GROUNDS OF CHALLENGE (37 C.F.R. § 42.204(B)(2))

Petitioner requests *inter partes* review and cancellation of the Challenged Claims on the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1	1, 2, 7, 8, 9	§103	Nixon

2	10	§103	Nixon and Assadi
3	1, 2, 7, 8, 9	§103	Badihi
4	10	§103	Badihi and Assadi

These grounds are not duplicative of each other. Grounds 1 and 2 rely on Nixon as a primary reference. To the extent the Patent Owner argues that Nixon is not entitled to the filing date of the Nixon Prov., Grounds 3 and 4 rely on Badihi as a primary reference, which is prior art under pre-AIA § 102(a).

IX. GROUND 1: NIXON RENDERS OBVIOUS CLAIMS 1, 2, 7, 8, AND 9

Nixon renders obvious claims 1, 2, 7, 8, and 9 of the '965 patent. Ex. 1003, ¶¶81-121.

1. Claim 1

[1pre] A method of producing backside illuminated image sensors comprising the steps of:

To the extent the preamble is considered to be a limitation, Nixon discloses a method for producing BSI image sensors. Ex. 1003, ¶¶82-83. Nixon discloses that “[t]his invention relates ... to the manufacturing of CMOS image sensors capable of backside illumination,” such as BSI CMOS image sensors 100 (*i.e.*, ***a method of producing backside illuminated image sensors***). Ex. 1004, 1:8-10, Abstract, Figs. 1, 2, 4A-4G; Ex. 1005, IDTD, 4-5, Fig. 1, Shweky, 7-9, Fig. 4. Nixon’s Figure 3 is a flowchart illustrating a “process 300 for manufacturing image sensors 100 ... with

the image sensor 100 at each stage of the process being shown in FIGS. 4A-4G.”

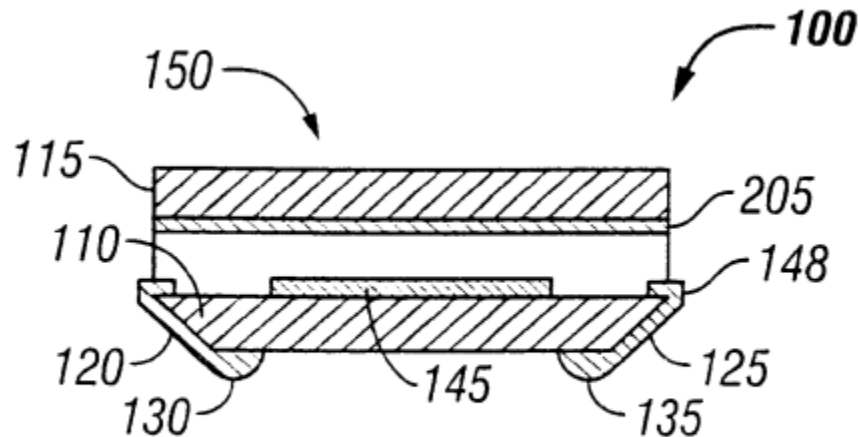
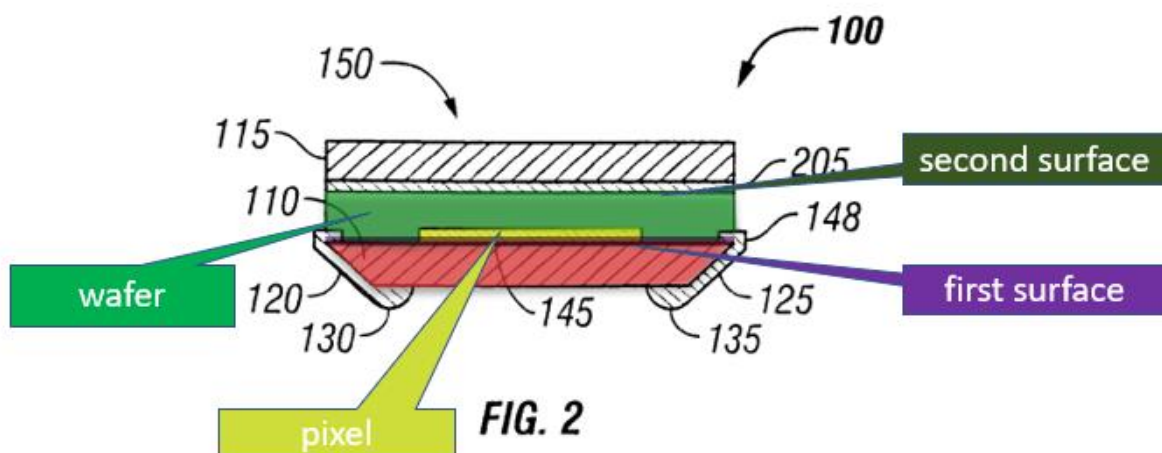


FIG. 2

Ex. 1004, Fig. 2; Ex. 1005, IDTD, Fig. 2.

Nixon discloses or renders obvious a method for producing a plurality of image sensor circuits on a wafer as claimed. Ex. 1003, ¶¶84-86. Nixon discloses a silicon wafer 405 that corresponds to the claimed “wafer.” Ex. 1004, 2:22-35; Ex. 1005, IDTD, 4-5, Shweky, 8, Fig. 4. Specifically, Nixon’s Figure 4A shows process 300 starts with silicon wafer 405 that has a frontside (active) surface and a backside

surface (*i.e.*, **a wafer having first and second surfaces**). Ex. 1004, 2:26-31; 41-42; Ex. 1005, IDTD, Fig. 2, Shweky, 8, Figs. 3, 4. Nixon also discloses that the CMOS image sensor described in Nixon is “achieved using wafer level processing.” Ex. 1004, Abstract, 1:65-2:1; Ex. 1005, IDTD, 4-5, Shweky, 8, Fig. 4. Silicon wafer 405 is prefabricated with pixels on its frontside surface (*i.e.*, **producing image sensor circuits on a wafer; each of the image sensor circuits being formed the first surface**) because it is later diced to form individual silicon substrates 105, each with pixels 145 “positioned at the top surfaces 148 of the silicon substrate 105.” Ex. 1004, 2:1-10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Figs. 3, 4; Ex. 1003, ¶85; *see supra*, §§II.A, D. Pixels 145 are **a matrix of light-sensitive pixel regions**, and Nixon’s Figure 2 illustrates **pixels 145** extending into **silicon substrate 105** from **top surface 148** (*i.e.*, **a matrix of light-sensitive pixel regions extending into the wafer from the first surface**):



Ex. 1004, Fig. 2; Ex. 1005, IDTD, Fig. 2⁴; Ex. 1003, ¶85; *see supra*, §§II.A, D.

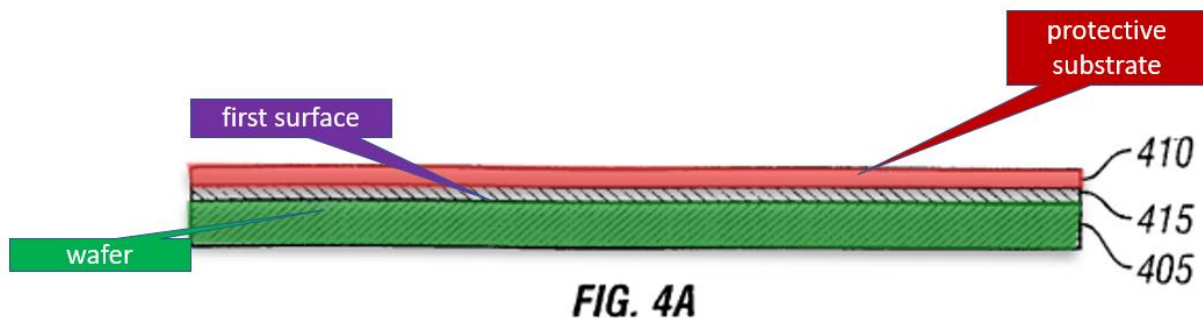
To the extent the Patent Owner argues that Nixon does not expressly disclose this claim element, a POSITA would readily understand that the teachings in Nixon are applied to wafer-level processing of an image sensor where multiple image sensor circuits are manufactured at the same time to achieve cost efficiencies, among other things, as opposed to individually manufacturing each image sensor circuit. Ex. 1003, ¶86; *see supra*, §II.D. A POSITA would also readily understand that Nixon’s pixels 145 are in the wafer, as it was well-known at the time of invention that the active regions of pixels extend into the substrate. Ex. 1003, ¶86; *see also* Ex. 1046, 1:31-45, 5:4-17, Fig. 9B; *see supra*, §§II.A, D. Accordingly, Nixon at a minimum renders this claim limitation obvious. Ex. 1003, ¶86

[1b] securing the wafer onto a protective substrate such that the first surface faces the protective substrate;

Nixon discloses securing the wafer onto a protective substrate such that the first surface faces the protective substrate. Ex. 1003, ¶¶87-89. Nixon’s first glass plate 410 corresponds to the claimed “protective substrate” and the active side of Nixon’s silicon wafer 405 corresponds to the claimed “first surface.” Ex. 1004,

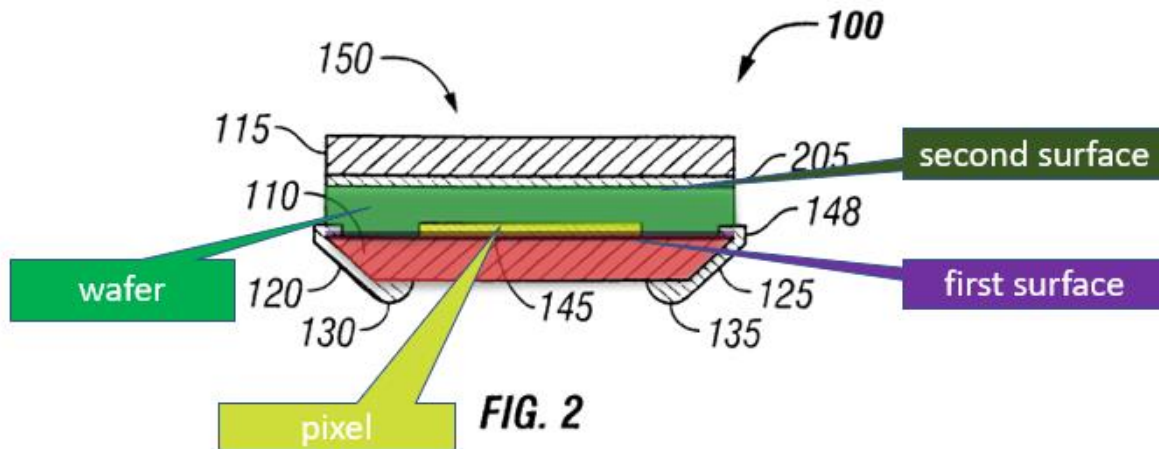
⁴ Nixon’s Figure 2 illustrates an embodiment created using the process depicted in Figures 4A to 4G. Ex. 1004, 1:56-57, 1:61-62; Ex. 1003, ¶85 n.2.

2:22-36; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Specifically, Nixon's Figure 4A illustrates a process step where "**silicon wafer 405** is bonded onto ... **first glass plate 410**" (*i.e., securing the wafer onto a protective substrate*) "while the active surface of the **silicon wafer [405]** is facing up into the encapsulate" (*i.e., such that the first surface faces the protective substrate*):



Ex. 1004, Fig. 4A, 2:26-31; Ex. 1005, Shweky, 8, Fig. 4.

Nixon also discloses the resulting packaged CMOS image sensor 100 has "[a]n epoxy adhesive layer ... [that] attaches" the silicon substrate 105 to the protective plate 110 (*i.e., securing the wafer onto a protective substrate*). Ex. 1004, 2:1-6; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Nixon's Figure 2 shows **top (frontside) surface 148** of **silicon substrate 105** facing **protective plate 110** (*i.e., the first surface faces the protective substrate*):



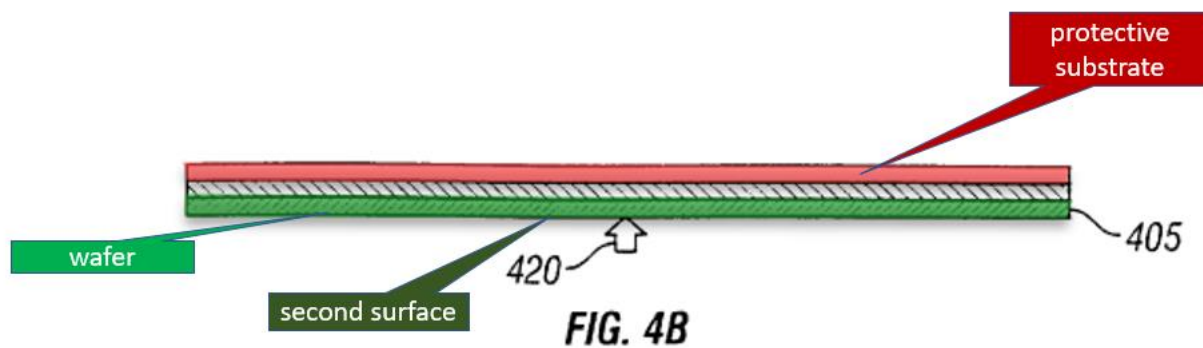
Ex. 1004, Fig. 2; Ex. 1005, IDTD, Fig. 2.

[1c] removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface;

Nixon discloses removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface. Ex. 1003, ¶¶90-91. Nixon discloses “grinding the silicon wafer from the opposite surface of the silicon wafer” (*i.e., removing material from the second surface of the wafer*) to a “predetermined thickness” that “allows for the light sensitive area of the die 430 to be illuminated from . . . the back side” (*i.e., until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface*).⁵ Ex. 1004, 2:36-41, 3:7-17, 1:65-

⁵. Nixon discloses thinning the substrate until it is transparent to visible light like what is described in the '965 patent. Ex. 1003, ¶91 n.3; Ex. 1001, 4:61-5:4.

2:10; Ex. 1005, Shweky, 8, Fig. 4. Nixon’s Figure 4B illustrates a process step of grinding (indicated by arrow 420) the backside surface of **silicon wafer 405** (i.e., *removing material from the second surface of the wafer*):

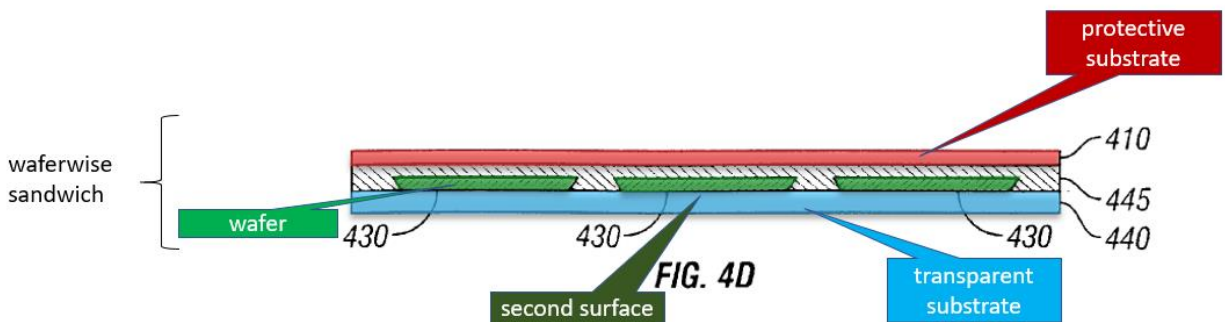


Ex. 1004, Fig. 4B; Ex. 1005, Shweky, 8, Fig. 4.

[1d] securing a transparent substrate onto the second surface of the wafer, thereby producing a waferwise sandwich; and

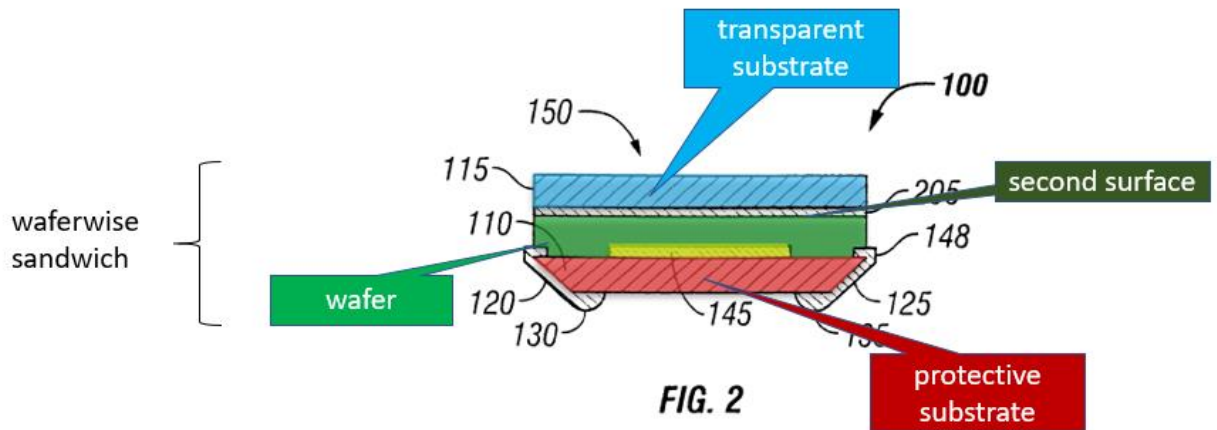
Nixon discloses securing a transparent substrate onto the second surface of the wafer thereby producing a waferwise sandwich. Ex. 1003, ¶¶92-94. Nixon’s protective plate 115 and second glass plate 440 correspond to the claimed “transparent substrate.” Ex. 1004, 2:1-6, Abstract, Figs. 4A-4G; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Indeed, Nixon discloses fabricating and packaging a CMOS image sensor can be illuminated from the back side, where the “die is covered with an optically transparent material.” Ex. 1004, 1:37-47; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Fig. 4 (expressly disclosing “[a]ttach[ing] a second glass plate from the back side”). Protective plate 115 is the resulting die-sized section of

Nixon's second glass plate 440 (*i.e.*, **the transparent substrate is glass**), after it is diced to separate the dies. Ex. 1004, 1:37-47, 2:49-57; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Fig. 4. Specifically, Nixon's Figure 4D illustrates a process step of bonding "**second glass plate 440** ... onto the backside of **silicon dies**" 430 using epoxy adhesive (not depicted), thereby forming a waferwise sandwich with **first glass plate 410** (*i.e.*, **securing a transparent substrate onto the second surface of the wafer, thereby producing a waferwise sandwich**):



Id., Fig. 4D, 2:49-52; Ex. 1005, Shweky, 8, Fig. 4.

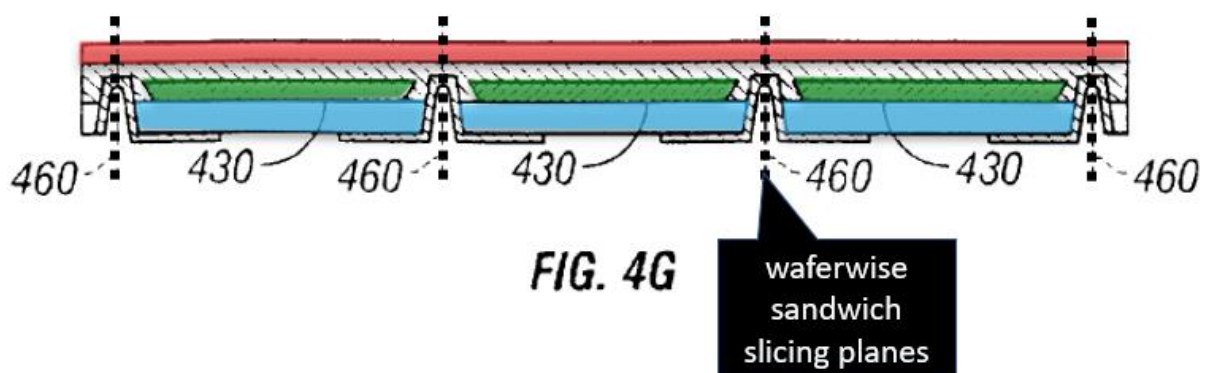
Relatedly, Nixon discloses "[a]n epoxy adhesive layer ... attaches the protective plates 110, 115 to the silicon substrate 105" (*i.e.*, **securing a transparent substrate onto the second surface of the wafer**) and "a thin silicon substrate 105 ... is sandwiched between two thin protective plates 110, 115 on the top and bottom sides" (*i.e.*, **thereby producing a waferwise sandwich**). *Id.*, 1:65-2:10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Nixon's Figure 2 illustrates **protective plate 110** and **protective plate 115** sandwiching **silicon substrate 105**:



Id., Fig. 2; Ex. 1005, IDTD, Fig. 2.

[1e] slicing the waferwise sandwich, thereby defining a plurality of backside illuminated image sensors.

Nixon discloses slicing the waferwise sandwich, thereby defining a plurality of backside illuminated image sensors. Ex. 1003, ¶¶95-96. Nixon's Figure 4G illustrates a process step of dicing the wafer along score lines 460 between **dies 430** (*i.e.*, *slicing the waferwise sandwich*):



Id., Fig. 4G; Ex. 1005, Shweky, 8, Fig. 4.

Specifically, Nixon discloses “[t]he wafer is diced along score lines 460 within the notches 450 between the dies 430,” producing “multiple individual packaged dies 430” (*i.e.*, ***defining a plurality of backside illuminated image sensors***). Ex. 1004, 3:1-6; Ex. 1005, Shweky, 8, Fig. 4.

2. Claim 2

[2pre] The method according to claim 1, wherein the step of securing the protective substrate onto the first surface comprises
--

Nixon discloses 2pre for the same reasons as 1b above. Ex. 1003, ¶¶97.

[2a] depositing an adhesive onto the protective substrate, and then

Nixon discloses or renders obvious depositing an adhesive onto the protective substrate. Ex. 1003, ¶¶98-100. Nixon’s protective plate 110 and first glass plate 410 correspond to the claimed “protective substrate” and Nixon’s epoxy adhesive layer corresponds to the claimed “adhesive.” *See supra*, 1b; Ex. 1004, 2:3-6; Ex. 1005, Shweky, 7-8, Fig. 4. Nixon discloses that “[a]n epoxy adhesive layer ... attaches the protective plates 110, 115 to the silicon substrate 105.” Ex. 1004, 1:65-2:10, Fig. 2; Ex. 1005, Shweky, 7-8, Fig. 4. Nixon further discloses that “a silicon wafer 405 is bonded onto a thin protective layer, or first glass plate 410.” Ex. 1004, 2:26-28; Ex. 1005, Shweky, 8, Fig. 4. It was common practice to use a supporting structure or plate, such as Nixon’s protective plate 110 or first glass plate 410, prior to thinning the silicon substrate 105. Ex. 1003, ¶¶99; *see supra*, §II.B. It was

conventional to apply an adhesive to such supporting structure or plate first before attaching the wafer (*i.e.*, ***depositing an adhesive onto the protective substrate***). Ex. 1003, ¶99; *see supra*, §II.B. A POSITA would know how to deposit or apply such epoxy adhesive in Nixon in the same manner as described for the adhesive in the '965 patent. Ex. 1003, ¶99; Ex. 1004, 1:65-2:10; Ex. 1005, Shweky, 8, Fig. 4; Ex. 1001, 6:35-40, Fig. 4(A).

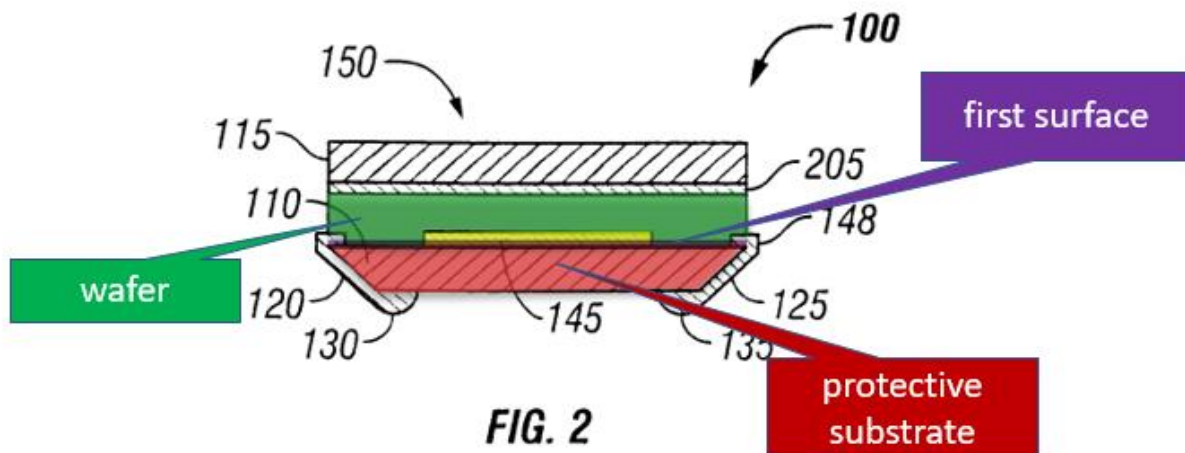
A POSITA would also readily recognize that when bonding two surfaces together, adhesive must first be placed on at least one of those surfaces. Ex. 1003, ¶100. In the context of bonding the wafer to the protective substrate, there are only three choices: the adhesive could be placed on the wafer, the protective substrate, or both. *Id.*; *see supra*, §II.B. Whichever of the three choices is used during the manufacturing process is merely a design choice. Ex. 1003, ¶100; *see supra*, §II.B; *Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1340 (Fed. Cir. 2020) (in choosing between “terminal-side plotting” or “server-side plotting,” “[a] person of ordinary skill would therefore have two predictable choices for when to perform plotting, providing them with a simple design choice... Because a [POSITA] has ‘good reasons to pursue the known options within his or her technical grasp,’ § 103 bars the patentability of such an obviousness combination.”); *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1238 (Fed. Cir. 2010) (holding that a motivation to combine and a reasonable expectation of success exist when “it is simply a matter of common

sense” to combine known elements of the prior art to solve a known problem). Just like in *Uber* and *Wyers*, it would have been obvious to a POSITA to apply the adhesive on the protective substrate (*i.e.*, ***depositing an adhesive onto the protective substrate***). Ex. 1003, ¶100; *see supra*, §II.B. Accordingly, Nixon at a minimum renders this limitation obvious. Ex. 1003, ¶¶98-100.

[2b] placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive.

Nixon discloses placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive. Ex. 1003, ¶¶101-102. Because the epoxy adhesive is applied onto the first glass plate 410, the silicon wafer 405 would be placed onto the first glass plate 410 where the epoxy adhesive is deposited to secure the first glass plate 410 onto the silicon wafer 405 (*i.e.*, ***placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive***). Ex. 1003, ¶102; *see supra*, 2a, §II.B. As Nixon further discloses that the “first glass plate 410 is bonded while the active surface of the silicon wafer is facing up into the encapsulate,” the active surface of the wafer would contact the deposited adhesive on the first glass plate 410 (*i.e.*, ***the first surface contacts the deposited adhesive***). Ex. 1004, 2:29-31; Ex. 1005, IDTD, Fig. 2, Shweky, Fig. 4. Nixon’s Figure 2 illustrates that epoxy adhesive layer (not depicted) attaches the **protective**

plate 110 to the silicon substrate 105 such that the top (frontside) surface 148 contacts the epoxy adhesive layer:



Ex. 1004, Fig. 2; Ex. 1005, IDTD, Fig. 2.

3. Claim 7

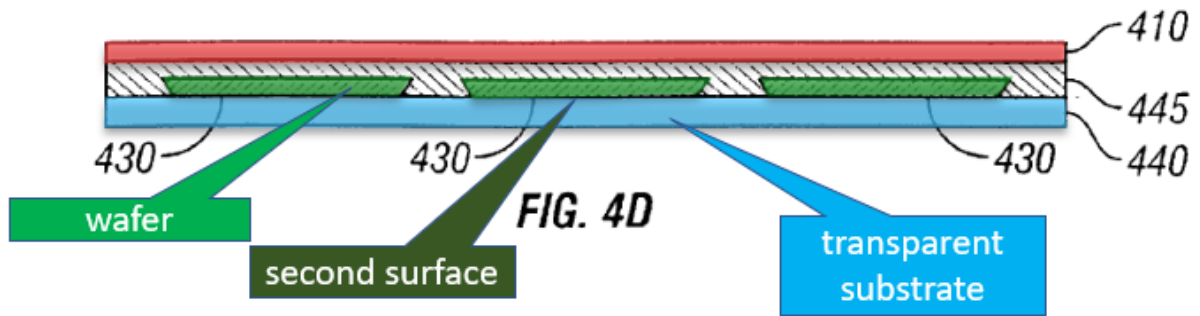
[7pre]. The method according to claim 1, wherein the step of securing a transparent substrate onto the second surface comprises

Nixon discloses 7pre for the same reasons as 1d above. Ex. 1003, ¶¶103-104. Nixon's protective plate 115 and second glass plate 440 correspond to the claimed "transparent substrate." See *supra*, 1d.

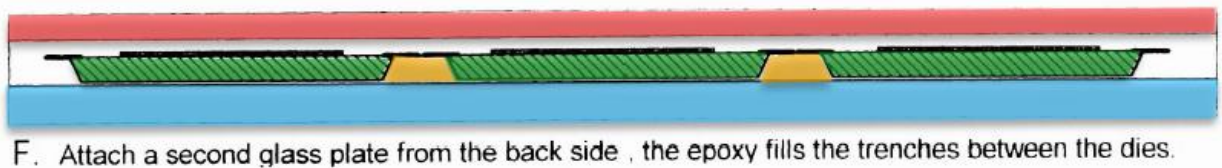
[7a] depositing an adhesive onto the second surface, and then

Nixon discloses or renders obvious depositing an adhesive onto the second surface. Ex. 1003, ¶¶105-107. Nixon's epoxy adhesive layer corresponds to the claimed "adhesive" and the backside of Nixon's silicon wafer 405 corresponds to the claimed "second surface." Ex. 1004, 1:65-2:10, 2:49-57, Figs. 2, 4D; Ex. 1005,

Shweky, 8, Fig. 4. Nixon discloses “[e]poxy may be used to bond the second glass plate 440 to the silicon dies 430” and may be used to “fill the grooves 435 between the dies 430.” Ex. 1004, 2:49-57, Fig. 4D; Ex. 1005, IDTD, Fig. 2, Shweky, 8, Fig. 4. For the epoxy to both fill the grooves 435 and bond second glass plate 440 to the dies 430, the epoxy would have to be applied first to the wafer structure to fill the grooves 435 and cover the backside of the dies 430. Ex. 1003, ¶106. This way, “when combined with the first glass plate 410 creates a complete protective enclosure for each die 430.” Ex. 1004, 2:52-55, Fig. 4D; Ex. 1005, IDTD, Fig. 2, Shweky, 8, Fig. 4. If the epoxy is first applied to second glass plate 440 and then placed on the wafer structure, there may not be enough epoxy to fill the grooves 435 between dies 430. Ex. 1003, ¶106. Alternatively, epoxy could be applied to both the wafer structure and glass plate 440 before they are bonded to ensure the epoxy fill the grooves 435 and cover dies 430 for the best bond and complete enclosure. *Id.* Nixon’s Figure 4D illustrates **second glass plate 440** (*i.e.*, *transparent substrate*) is bonded using an epoxy adhesive (not depicted) (*i.e.*, *adhesive*) to the backside surface of **silicon dies 430**:



Ex. 1004, Fig. 4D, 2:49-57; Ex. 1005, Shweky, 8, Fig. 4. Shweky discloses that the “epoxy fills the trenches” on the backside of the dies (*i.e.*, **depositing an adhesive onto the second surface**), which is illustrated in Shweky’s Figure 4:



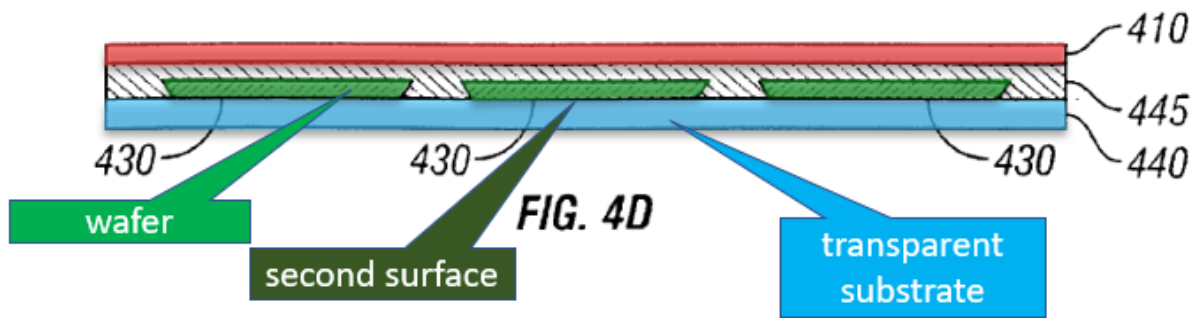
Ex. 1007, Fig. 4. A POSITA would know how to deposit or apply such epoxy adhesive layer in Nixon in the same manner as described for the adhesive in the ’965 patent. Ex. 1003, ¶106; Ex. 1004, 2:49-57; Ex. 1005, Shweky, 8, Fig. 4; Ex. 1001, 7:57-8:3, Fig. 4(E).

A POSITA would also readily recognize that when bonding two surfaces together, adhesive must first be placed on at least one of those surfaces. Ex. 1003, ¶107. In the context of bonding the wafer to the transparent substrate, there are only three choices: the adhesive could be placed on the wafer, on the transparent substrate, or both. *Id.* Whichever of the three choices is used during the manufacturing process is merely a design choice. *Id.*; *see also Uber*, 957 F.3d at

1340; *Wyers*, 616 F.3d at 1238. Just like in *Uber* and *Wyers*, it would have been obvious to a POSITA to apply the adhesive on the backside of the wafer (*i.e.*, ***depositing an adhesive onto the second surface***). Ex. 1003, ¶107. Accordingly, Nixon at a minimum renders this limitation obvious. *Id.*, ¶¶105-107.

[7b] placing the transparent substrate onto the deposited adhesive.
--

Nixon discloses placing the transparent substrate onto the deposited adhesive. Ex. 1003, ¶¶108-109. Because the epoxy adhesive is applied onto the backside of silicon wafer 405, the second glass plate 440 would be placed onto the backside of the silicon wafer 405 where the epoxy adhesive is deposited to secure the second glass plate 440 onto the backside of the silicon wafer 405 (*i.e.*, ***placing the transparent substrate onto the deposited adhesive***). Ex. 1003, ¶109; *see supra*, 7a. Nixon further discloses “attach[ing]” or “bond[ing]” protective plate 115 or second glass plate 440 onto the epoxy adhesive layer (*i.e.*, ***placing the transparent substrate onto the deposited adhesive***). Ex. 1004, 2:3-6, 2:49-57, Fig. 2; Ex. 1005, Shweky, 7-8, Fig. 4. Nixon’s Figure 4D illustrates placing **second glass plate 440** onto epoxy adhesive (not depicted):



Ex. 1004, Fig. 4D; Ex. 1005, Shweky, 8, Fig. 4.

4. Claim 8

[8pre]. The method according to claim 7,

Nixon discloses 8pre for the same reasons as claim 7 above. Ex. 1003, ¶110.

[8a] wherein the step of removing material includes separating each of the plurality of image sensor circuits; and

Nixon discloses separating each of the plurality of image sensor circuits. Ex. 1003, ¶¶111-112. Nixon discloses that “the silicon wafer 405 is ... etched along the dice lines 425” such that “the wafer is separated into individual dies 430” (*i.e., wherein the step of removing material includes separating each of the plurality of image sensor circuits*). Ex. 1004, 2:43-58; Fig. 3, Fig. 4C; Ex. 1005, Shweky, 8, Fig. 4. Nixon’s Figure 4C illustrates etching along dice lines 425 to separate **individual dies 430**:

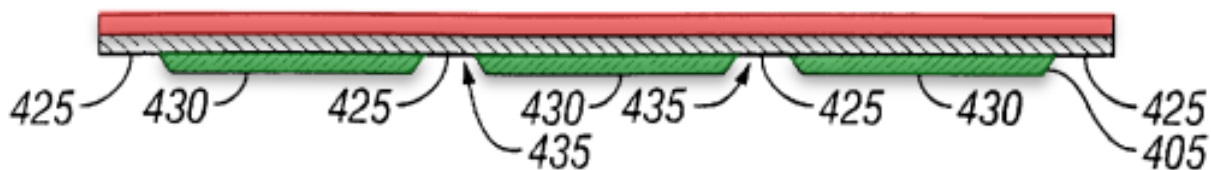
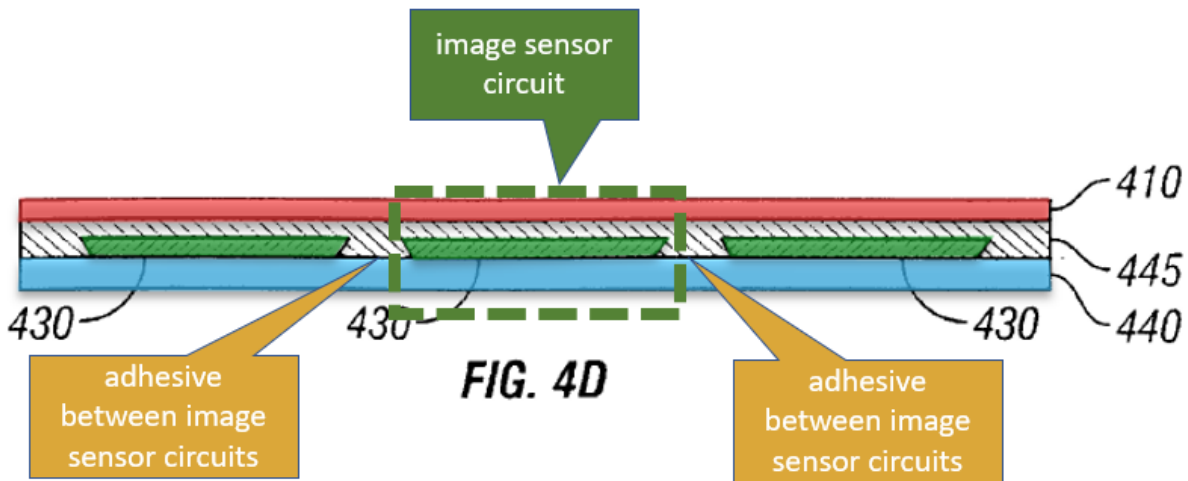


FIG. 4C

Ex. 1004, Fig. 4C; Ex. 1005, Shweky, 8, Fig. 4.

[8b] wherein the step of depositing the adhesive onto the second surface further comprises depositing adhesive into interstices located between the plurality of image sensor circuits, thereby protecting the image sensor circuits.

Nixon discloses depositing adhesive into interstices located between the plurality of image sensor circuits, thereby protecting the image sensor circuits. Ex. 1003, ¶¶113-114. Nixon discloses that “epoxy may fill the grooves 435 between the dies 430 (*i.e.*, **depositing adhesive into interstices located between the plurality of image sensor circuit**). Ex. 1004, 2:49-57, Fig. 4D; Ex. 1005, Shweky, 8, Fig. 4. Shweky also discloses that “epoxy fills the trenches between the dies.” Ex. 1047, Fig. 4. “The image sensor packages assembled according to the present invention ... offer[] a complete mechanical enclosure for the die and does not leave any silicon exposed to the outside. This provides both mechanical and environmental protection” (*i.e.*, **thereby protecting the image sensor circuits**). Ex. 1004, 3:7-17; Ex. 1005, Shweky, 7-8. Nixon’s Figure 4D illustrates epoxy adhesive (not depicted) that is used to fill in grooves 435 (not labeled) between the **individual dies 430**:



Ex. 1004, Fig. 4D; Ex. 1005, Shweky, Fig. 4.

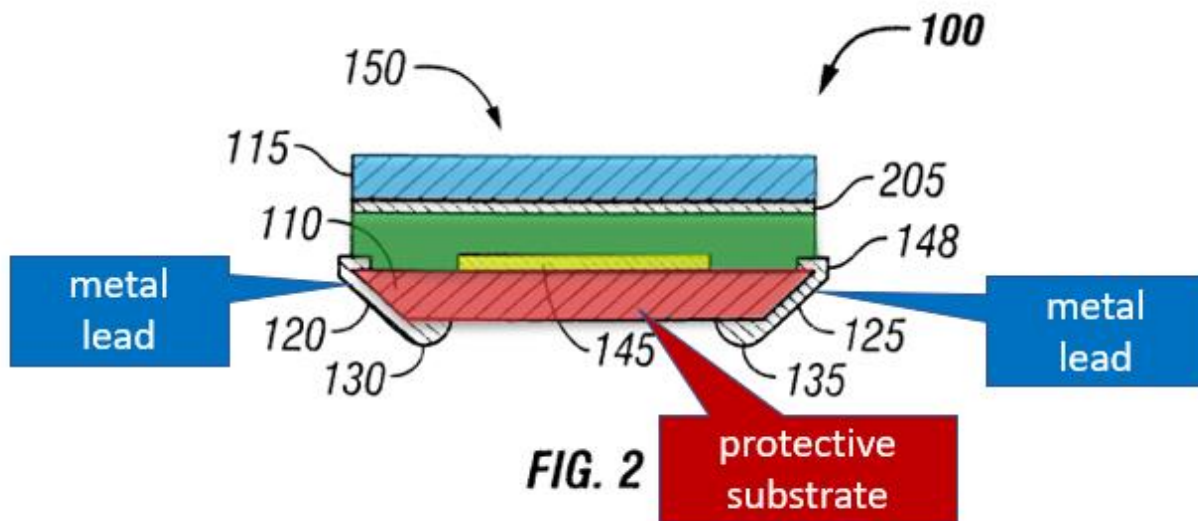
5. Claim 9

[9pre] The method according to claim 1, further comprising the step of

Nixon discloses 9pre for the same reasons as claim 1 above. Ex. 1003, ¶115.

[9a] forming metal leads on the protective substrate after the step of securing the transparent substrate,

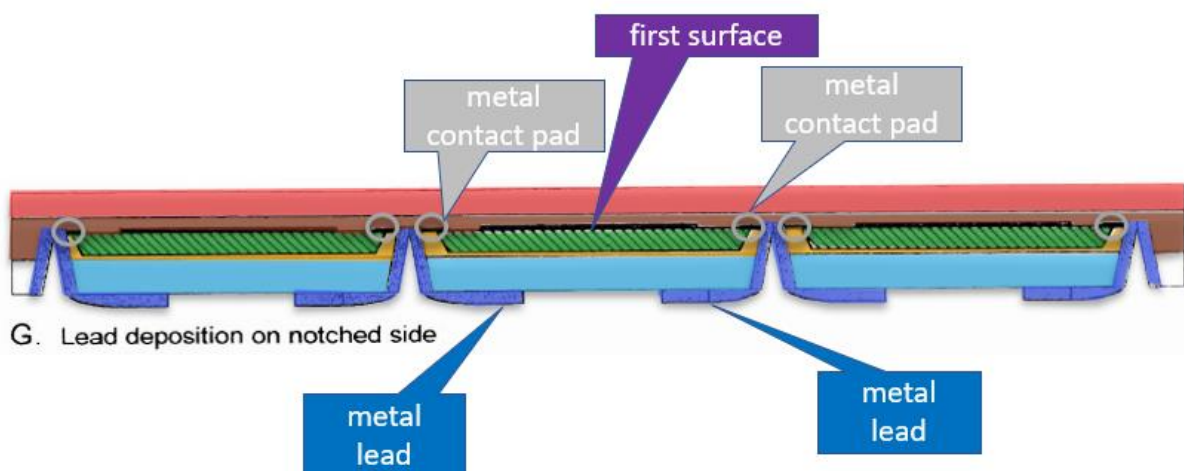
Nixon discloses or renders obvious forming metal leads on the protective substrate after the step of securing the transparent substrate. Ex. 1003, ¶¶116-117. Nixon's electrical leads 120, 125 correspond to the claimed "metal leads." Ex. 1004, 2:6-9, 2:20-22; Ex. 1005, IDTD, 4-5, Fig. 2. Nixon's Figure 2 illustrates **electrical leads 120, 125** formed on **protective plate 110** after the **protective plate 115** is secured to the backside of the **silicon die** (*i.e., forming metal leads on the protective substrate after the step of securing the transparent substrate*):



Ex. 1004, Fig. 2; Ex. 1005, IDTD, Fig. 2.

[9b] wherein the metal leads are connected to metal contact pads located on the first surface of the wafer.

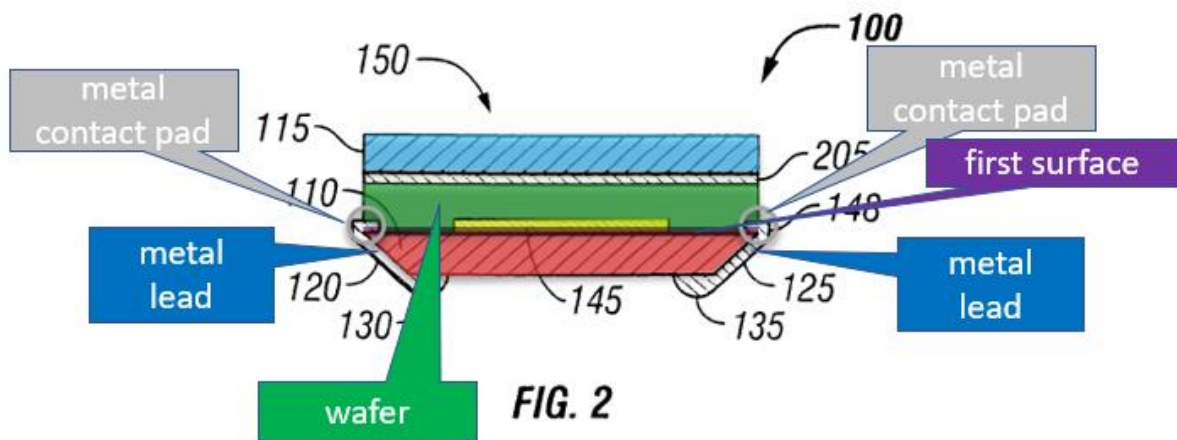
Nixon discloses the metal leads are connected to metal contact pads located on the first surface of the wafer. Ex. 1003, ¶¶118-121. Nixon discloses that deep notches 450 are drawn between dies 430 from the backside of the waferwise sandwich such that “the cross sections of each of the pads are exposed” and then “[t]he metal layer is patterned by a lithography process into individual leads 455 that contact the pads and form a solder pad on the upper surface of each die package.” See *supra*, 9a; Ex. 1004, 2:58-67; Ex. 1005, Shweky, 8, Fig. 4. The Nixon Prov.’s Figure 4 shows the **individual metal leads** are connected to **metal contact pads** that are on the top (frontside) surface of the silicon die (*i.e.*, **wherein the metal leads are connected to metal contact pads**):



Ex. 1047, Fig. 4.

A POSITA would readily understand that Nixon Prov.’s Figure 4 corresponds to Nixon’s Figure 4F and discloses the manufacturing process that results in the image sensor 100 of Nixon’s Figure 1, which is simply one embodiment of Nixon. Ex. 1004, 2:58-67, Figs. 1, 4; Ex. 1005, Shweky, 8, Fig. 4; Ex. 1003, ¶120.

A POSITA would also readily recognize the image sensor 100 of Nixon’s Figure 2 is another embodiment of Nixon, where the notches are drawn from the top surface 148. Ex. 1004, 2:58-61; Ex. 1005, Shweky, 8, Fig. 4; Ex. 1003, ¶121. Nixon’s Figure 2 illustrates that the **metal contact pads** located next to the **top (frontside) surface 148** of **silicon substrate 105** are connected to the **electrical leads 120, 125** (i.e., *the metal leads are connected to metal contact pads located on the first surface of the wafer*):



Ex. 1004, Fig. 2; Ex. 1005, IDTD, Fig. 2.

X. GROUND 2: NIXON IN VIEW OF ASSADI RENDERS OBVIOUS CLAIM 10

Nixon in view of Assadi renders obvious claim 10. Ex. 1003, ¶¶122-138.

1. Reasons to Combine Nixon with Assadi

A POSITA would have been motivated to modify Nixon's manufacturing process for a BSI CMOS image sensor to include a passivation layer to ensure that the frontside (active) surface of the CMOS image sensor where the microelectronics are located are protected from abrasion, moisture, or contaminants. Ex. 1003, ¶¶123-124. Nixon and Assadi both teach CMOS image sensors. Ex. 1004, 2:8-10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-9, Fig. 4; Ex. 1044, 4:15-25. By the priority date of the '965 patent, it was very well-known and highly conventional that passivation layers should be included in CMOS image sensors to protect from, among other things, abrasion, moisture, and contaminants. Ex. 1003, ¶123; see *supra*, §II.C. Assadi provides an example of a passivation layer that provides these

well-known benefits. Ex. 1003, ¶123 Indeed, Assadi explains that passivation layers should be included “over[] the entirety of sensor 176, including sensor area 210 and non-sensor area (logic area 220 and bond pad area 240)” to provide “resistance to environmental contaminants, particularly moisture.” Ex. 1044, 4:26-44, 9:31-32. Including Assadi’s passivation layer in Nixon’s manufacturing process for a BSI CMOS image sensor would have the obvious added benefit of protecting the microelectronics necessary to convert the photons collected into electrical signals. Ex. 1003, ¶123; *see supra*, §§II.A, C-D.

A POSITA would have understood that modifying Nixon’s manufacturing process to include a passivation layer would have been a simple matter of applying well understood semiconductor fabrication techniques. Ex. 1003, ¶124; *see supra*, §§II.C-D. A POSITA would simply add a step to deposit passivation layer before bonding the glass to the active side of the wafer. Ex. 1003, ¶124; *see supra*, §§II.C-D. Nixon contemplates additional layers between active side of wafer and the protective glass substrate. Ex. 1004, Fig 4A (disclosing filter layer 415); Ex. 1003, ¶124. Indeed, Assadi’s passivation layer in a CMOS device is readily applicable to Nixon’s manufacturing process for a BSI CMOS image sensor. *Id.*; *see supra*, §§II.C-D. A POSITA could have modified Nixon’s manufacturing process to include a passivation layer such as taught in Assadi with a reasonable expectation of success. Ex. 1003, ¶124; *see supra*, §§II.C-D. Such a modification to Nixon’s

manufacturing process would have merely required adding additional conventional, well-known, manufacturing process steps. Ex. 1003, ¶124; *see supra*, §§II.C-D.

2. Claim 10

[10pre]. The method according to claim 1, wherein the step of securing the wafer onto a protective substrate further comprises:

Nixon discloses 10pre for the same reasons as 1b above. Ex. 1003, ¶¶125.

[10a] forming a passivation layer on the first surface of the wafer;

Nixon combined with Assadi renders obvious claim 10a's requirement of "forming a passivation layer on the first surface of the wafer." Ex. 1003, ¶¶126-130. It was very well-known and highly conventional that passivation layers should be included in CMOS image sensors to protect from, among other things, abrasion, moisture, and contaminants. *Id.*, ¶127; *see supra*, §II.C. Therefore, a POSITA would readily understand that Nixon's manufacturing process includes a step of "forming a passivation layer on the first surface of the wafer." Ex. 1003, ¶127; *see supra*, §II.C. Nixon discloses that the "[p]ixels 145 are positioned at the top surface 148 of the silicon substrate 105" (*i.e.*, ***first surface of the wafer***). Ex. 1004, 2:8-10; Ex. 1005, IDTD, Fig. 2. Top (frontside) surface 148 is also the active surface of the silicon wafer 405 given that the microelectronics are built into the top (frontside) surface 148. Ex. 1003, ¶127; *see supra*, §§II.A, C.

It would have been conventional to form a passivation layer on top (frontside) surface to protect the microelectronics. Ex. 1003, ¶128; *see supra*, §II.C; *see also* Ex. 1045, 5:26-34 (stating that the passivation coating “acts as a scratch coat and etch mask”); Ex. 1009, ¶¶97, 98, 101, Fig. 4 (disclosing a dielectric film 200 made of “SiN or SiO₂” that “protects the light-receiving elements”).

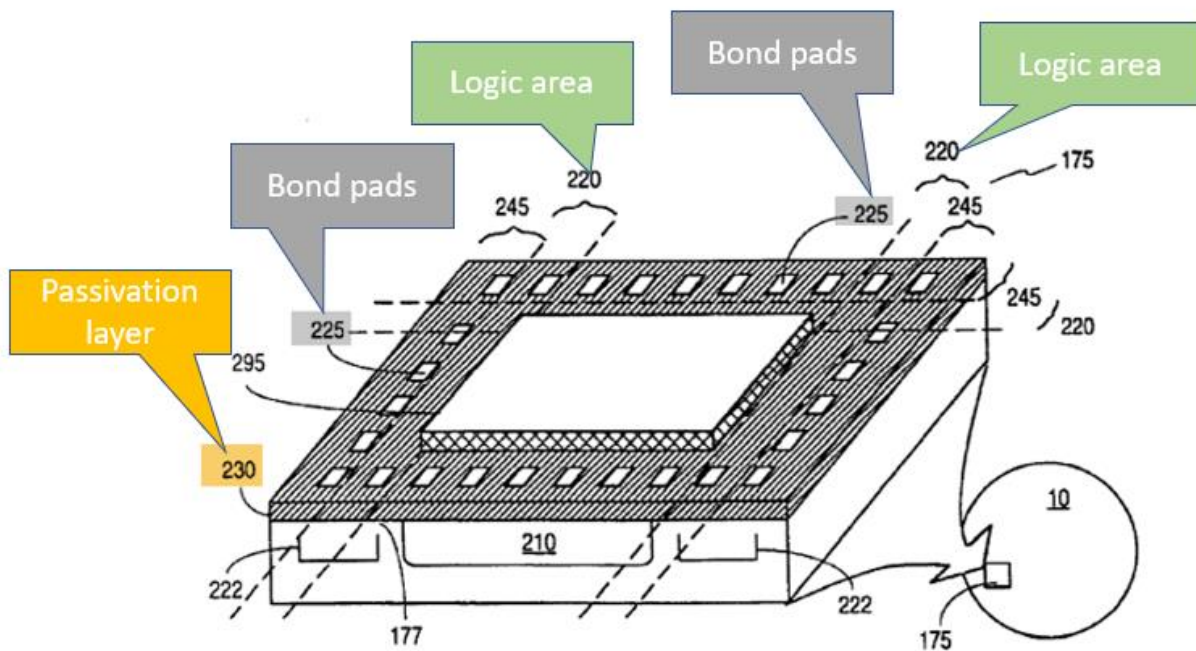
Assadi teaches a conventional mechanism to protect the microelectronics on the active surface. Ex. 1003, ¶129. Assadi’s passivation layer 230, which is made of either silicon nitride (Si₃N₄) or silicon oxynitride (Si_xO_yN_z), corresponds to the claimed “passivation layer.” Ex. 1044, 4:15-45. Assadi discloses an image sensor 175 with sensor area 210 representing “the photosensing region or area” and logic area 220 that “operates the individual pixels and drives signals from the pixels off sensor 175.” *Id.*, 4:15-26. Assadi further discloses a passivation layer 230 “overlies the entirety of sensor 175, including ... logic area 220” (*i.e.*, ***forming a passivation layer on the first surface of the wafer***):

sensor where the pixels 145 are located to protect them from abrasion, moisture, and contaminants. Ex. 1003, ¶¶126-130; *see supra*, §§II.A, C-D.

[10b] forming openings in the passivation layer; and

Nixon combined with Assadi renders obvious claim 10b’s requirement of “forming openings in the passivation layer.” Ex. 1003, ¶¶131-135. Nixon discloses exposing the pads that are next to the top (frontside) surface 148 of the wafer using notching so that the electrical leads 120, 125 may be connected to those pads to transmit electrical signals to the outside world. *See supra*, 9b. A POSITA would have been motivated to modify Nixon’s BSI CMOS image sensor to include Assadi’s passivation layer 230 to protect the pixels 145 on top (frontside) surface 148 of the silicon die. *See supra*, 10a.

Moreover, Assadi discloses a **passivation layer 230** on the frontside (active) surface of image sensor 175, where **openings** for **bond pads 225**, which are “arranged on the ... top surface of sensor 175” and “are electrically linked or coupled to device circuitry 222,” are formed so that the “logic circuitry 220 that operates the individual pixels [can] drive[] signals from the pixels off sensor 175” (*i.e.*, ***forming openings in the passivation layer***), as illustrated in Assadi’s Figure 3b:



Ex. 1044, Fig. 3b, 4:15-45.

A POSITA would readily understand that openings in the passivation layer may be formed before a protective substrate is secured because of the need to connect the metal pads on the frontside (active) surface of the substrate to the outside world to transmit the electrical signals converted from the collected photons. Ex. 1003, ¶134; *see supra*, §II.C; *see also* Ex. 1045, 5:26-37 (describing that bond pad contacts are opened through passivation coating 26 using “standard procedures” before “dicing and packaging operations”), Fig. 7; Ex. 1044, 4:26-45.

Moreover, a POSITA would understand that the passivation layer and the protective substrate may be formed from different materials. Ex. 1003, ¶135; *see also* Ex. 1045, 5:27-34 (describing passivation coating 260 as serving as an etch

mask, among other things). As a result, the use of different etching solutions (and different masks and resists accordingly) is required to expose the contact pads on the first surface, therefore requiring that openings be formed on the passivation layer first prior to a protective substrate being secured to the passivation layer. Ex. 1003, ¶135; *see supra*, §II.C.

Accordingly, this limitation would have been obvious over Nixon in combination with Assadi. *Id.*, ¶¶131-135; *see supra*, §II.C.

[10c] securing the protective substrate onto the passivation layer.

Nixon combined with Assadi renders obvious claim 10c’s requirement of “securing the protective substrate onto the passivation layer.” Ex. 1003, ¶¶136-138. As an initial matter, it would have been obvious to a POSITA to modify Nixon’s BSI CMOS image sensor to include Assadi’s passivation layer. *See supra*, 10a. Passivation layer is conventional component that is deposited on the first surface of the semiconductor substrate to protect the microelectronics there from abrasion, moisture, or contaminants. Ex. 1003, ¶137; *see supra*, §II.C; *see also* Ex. 1045, 5:26-37.

Nixon further discloses a protective plate 110 sandwiching silicon substrate 105 from the top to “create a complete protective enclosure for each die” (*i.e.*, ***securing the protective substrate***). Ex. 1004, 2:49-57; Ex. 1005, Shweky, 7-8. A POSITA would readily understand that Nixon’s protective plate 110 would be

secured onto Assadi's passivation layer, which overlies the entirety of the top (frontside) surface of semiconductor substrate 105 (*i.e.*, ***securing the protective substrate onto the passivation layer***), to further protect the Nixon's BSI CMOS image sensor and provide additional support during the step of removal of material from the backside of the semiconductor substrate. Ex. 1003, ¶138; *see supra*, §§II.B-D.

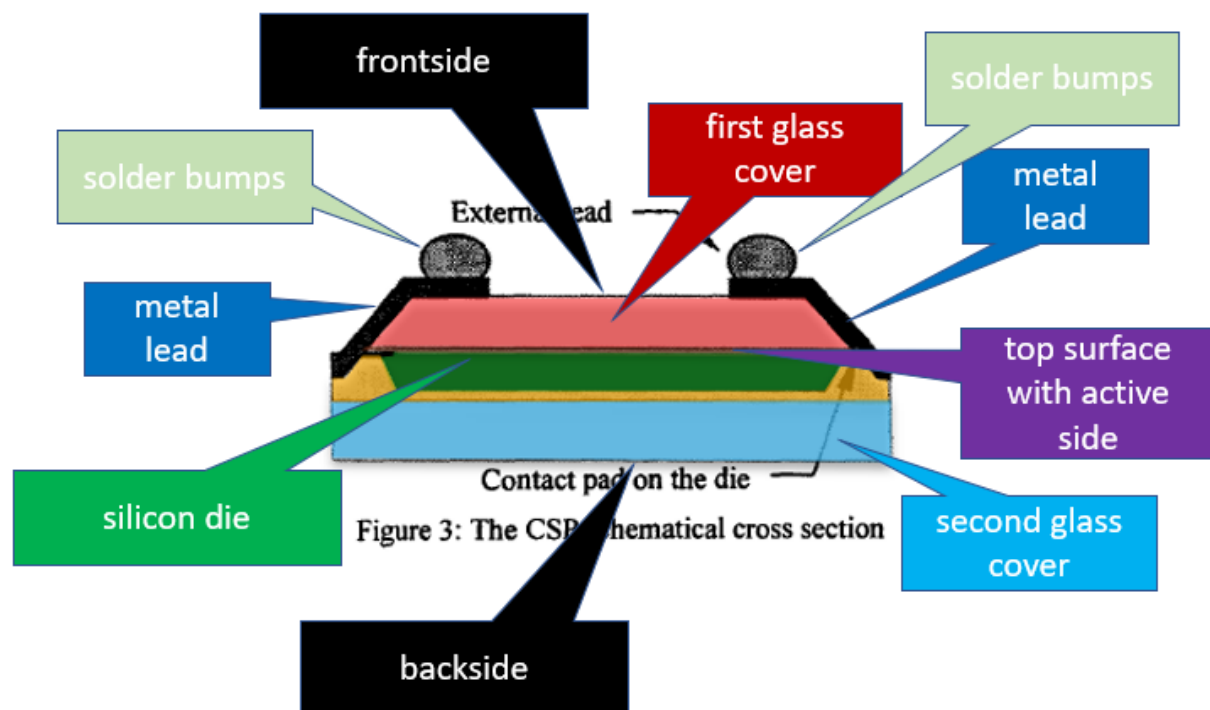
XI. GROUND 3: BADIHI RENDERS OBVIOUS CLAIM 1, 2, 7, 8, AND 9

Badihi renders obvious claims 1, 2, 7, 8, and 9. Ex. 1003, ¶¶139-183.

1. Claim 1

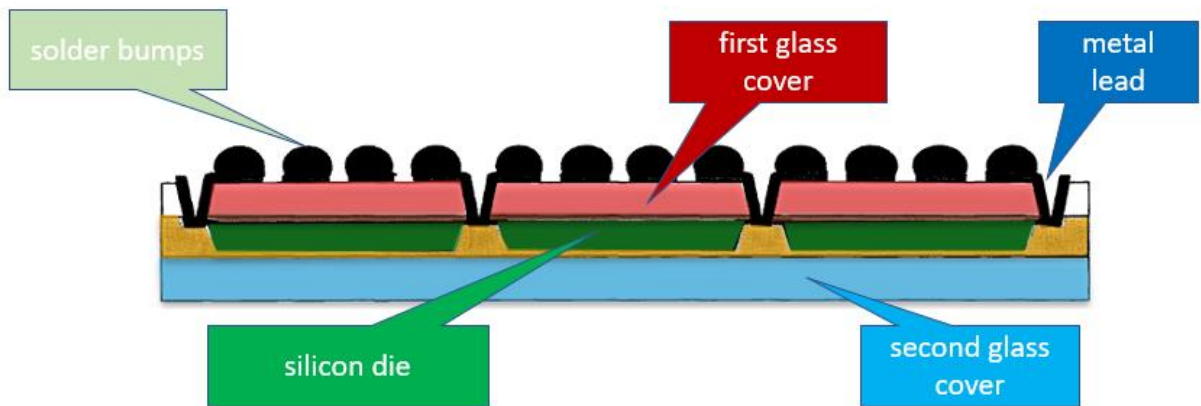
(a) 1pre

To the extent the preamble is considered to be a limitation, Badihi renders obvious a method for producing BSI image sensors. Ex. 1003, ¶¶140-144. Badihi's Figure 2 illustrates a process for packaging semiconductors at the wafer level. Ex. 1101, 237, Fig. 2. Badihi's Figure 3 illustrates the resulting packaged semiconductor where a **first glass cover** is bonded to the frontside of a **silicon die**, with the active side of the **silicon die** facing the **first glass cover**, **metal leads** and solder bumps are formed on the **first glass cover**, and a **second glass cover** is bonded to the backside of the **silicon die**:



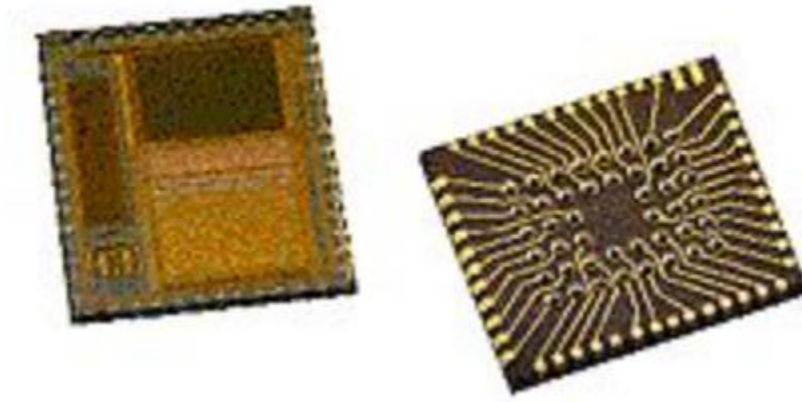
Ex. 1101, Fig. 3. Badihi's disclosures are not specific to image sensors; however, Badihi discloses that its packaging process can be readily applied to silicon light detectors, CMOS image sensors, and CCD devices. *Id.*, 239; Ex. 1003, ¶141. A POSITA would understand that CMOS image sensors include BSI CMOS image sensors and would further understand that the packaging taught by Badihi could be used for BSI CMOS image sensors. Ex. 1003, ¶141.

Badihi's Figure 2 illustrates the resulting packaged semiconductor with metal leads and solder bumps covering top of the frontside (active) surface, indicating that the wafer as packaged would be back-illuminated (*i.e., a method of producing backside illuminated image sensor*):



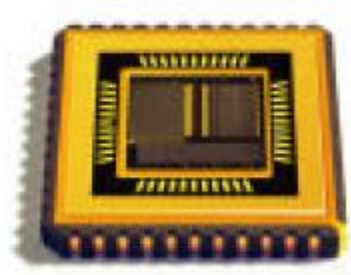
Ex. 1101, Fig. 2, 237.

Badihi's Figure 4 provides an example of a BSI image sensor created using the ShellPack wafer-level packaging process. *Id.*, Fig. 4; Ex. 1003, ¶143. Figure 4 shows photographs of a CMOS APS image sensor, the Photobit PB0159, made with Badihi's wafer-level packaging process:



Ex. 1053, Ex. A, Fig. 4, 239. The photo on the right is the frontside of the packaged image sensor because Badihi specifically teaches metal leads and solder bumps are formed on the glass cover at the frontside of the packaged image sensor (facing the

active surface of the imager die), and the photo on the left is therefore the backside of the packaged image sensor. Ex. 1101, 237; Ex. 1003, ¶143. A Photobit PB-159 datasheet confirms that the Badihi's CMOS APS is comprised of an array of 512x384 pixels:

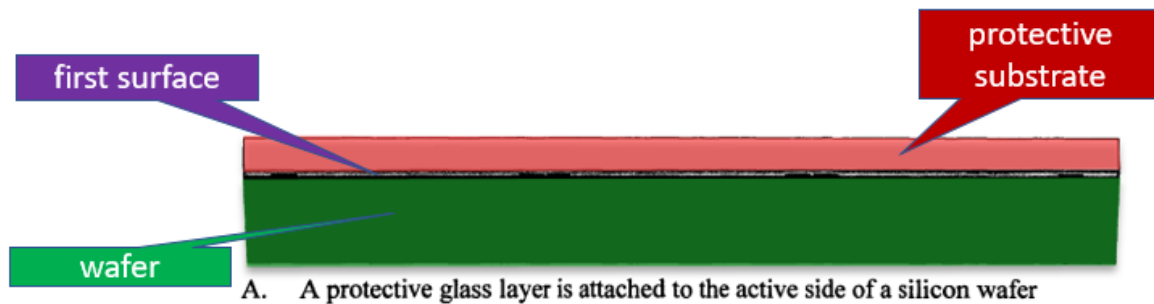


Ex. 1050, 1, 2.

A POSITA would recognize the packaged image sensor is a BSI image sensor because light would enter through its unobstructed backside since its frontside is covered by metal leads and solder bumps. Ex. 1003, ¶144.

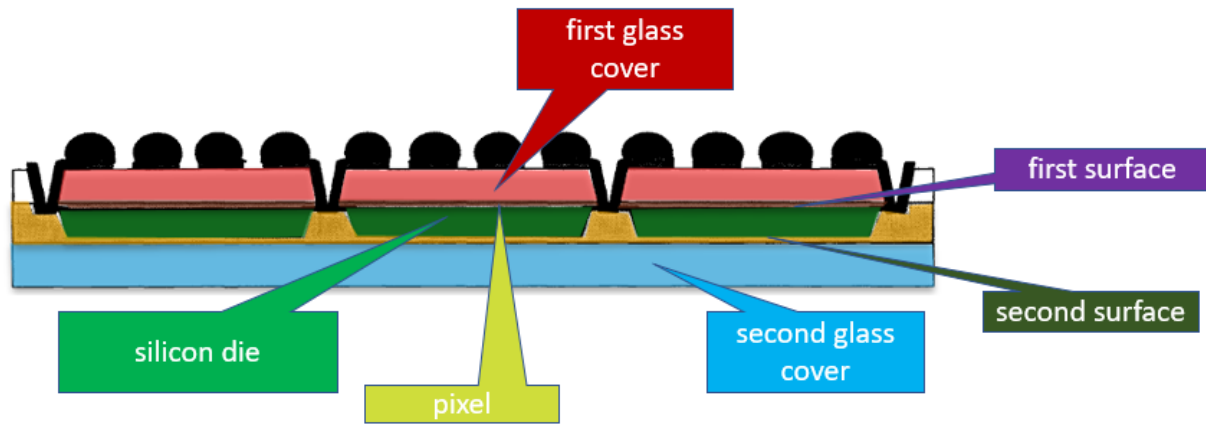
(b) 1a

Badihi discloses or renders obvious a method for producing a plurality of image sensor circuits on a wafer as claimed. Ex. 1003, ¶¶145-147. Badihi's silicon wafer corresponds to the claimed "wafer" and its active side facing the **protective glass layer (first glass cover)** corresponds to the claimed "first surface," which is illustrated in Badihi's Figure 2:



Ex. 1101, 236-237, Fig. 2. Badihi discloses applying its method to package CMOS image sensors, such as the CMOS APS product called Photobit PB0159. *Id.*, Fig. 4. It was well known that each CMOS image sensor contains an array of pixels, including the Photobit PB0159 containing 512x384 pixels. Ex. 1003, ¶146; Ex. 1050, 1-2. Such array of pixels corresponds to the claimed “imaging sensor circuit.” Ex. 1003, ¶146; *see supra*, §II.A. Badihi discloses a “wafer-level manufacturing process” where “the dies are packaged and encapsulated into separate enclosures while still in wafer form” and “enables to package all dies of the entire wafer at the same time” (*i.e.*, ***producing a plurality of image sensor circuits on a wafer***). Ex. 1101, 237, Fig. 2C (showing multiple dies). Indeed, Badihi discloses that “[w]afer [l]evel CSP manufacturing” enables the “packag[ing] [of] ***all the dies*** of the entire wafer at the same time rather than ... one die at a time.” *Id.* Badihi discloses “[a] thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive” (*i.e.*, ***a wafer having a first surface***) and “a second thin glass cover is bonded onto the silicon dies back side” (*i.e.*, ***a wafer having a second surface***). *Id.*,

237. Badihi's Figure 4 illustrates the process step where a **wafer** with a **glass layer** is facing the active side and **another glass layer is** facing the backside:



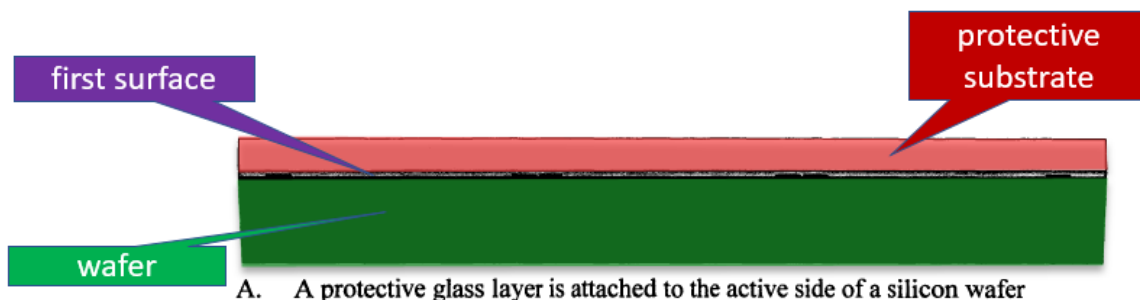
Ex. 1101, Fig. 4. A POSITA would readily understand that the image sensor circuits are formed on the active side of the top surface of the wafer, especially where solder bumps are located on the first glass cover as disclosed in Badihi (*i.e., each of the image sensor circuits being formed on the first surface*). Ex. 1003, ¶146; Ex. 1101, 237, Fig. 3.

It was well-known that in a CMOS process, microelectronics are built on and into the active side of the die. Ex. 1003, ¶147; *see supra*, §§II.A, C. Pixels in a CMOS APS image sensor built using CMOS process are no different. Ex. 1003, ¶147; *see supra*, §§II.A, C. It was also well-known that APS pixels have light-sensitive pixel regions built into the active side of the die (*i.e., a matrix of light-sensitive pixel regions extending into the wafer from the first surface*). Ex. 1003, ¶147; *see supra*, §§II.A, C. Therefore, it would have been obvious there is a matrix

of light-sensitive pixel regions that extend into the wafer from the active side of the wafer. Ex. 1003, ¶147; *see supra*, §§II.A, C.

(c) 1b

Badihi discloses securing the wafer onto a protective substrate such that the first surface faces the protective substrate. Ex. 1003, ¶¶148-150. Badihi's protective glass layer (first glass cover) corresponds to the claimed "protective substrate" and the active side of Badihi's silicon wafer corresponds to the claimed "first surface." Ex. 1101, 237. Badihi discloses the "thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive" (*i.e.*, ***securing the wafer onto a protective substrate***). *Id.* Specifically, Badihi's Figure 2 illustrates a process step of bonding the active (frontside) surface of the **silicon wafer** to the **protective glass layer (first glass cover)**:



Id., 237, Fig. 2.

Relatedly, Badihi's Figure 3 discloses the resulting packaged image sensor where the **protective glass layer (first glass cover)** is **bonded** to the **wafer** such

that it faces the active side of the **wafer** (i.e., *securing the wafer onto a protective substrate such that the first surface faces the protective substrate*):

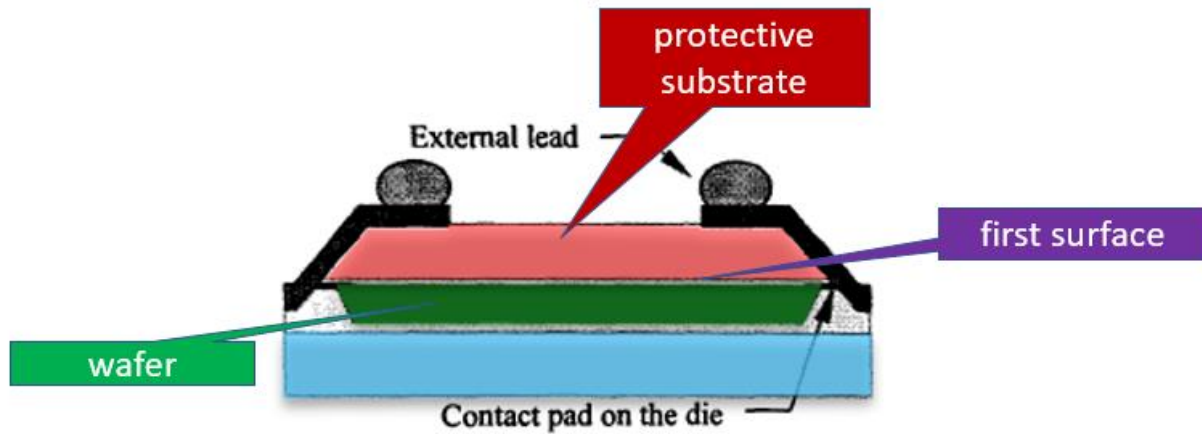
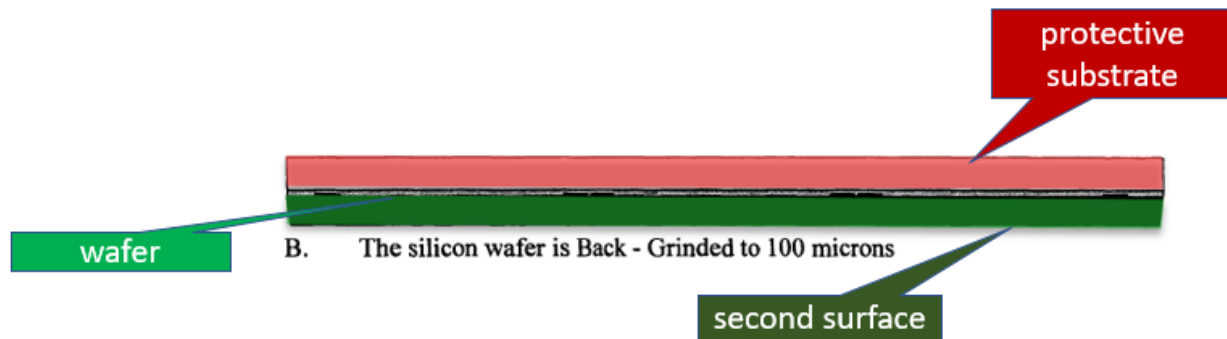


Figure 3: The CSP schematical cross section

Id., Fig. 3.

(d) 1c

Badihi discloses or renders obvious removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface. Ex. 1003, ¶¶151-153. Badihi's Figure 2 illustrates the process step where the **silicon wafer** is grinded from its backside until 100 microns is left (i.e., *removing material from the second surface of the wafer*):



Id., 237, Fig. 2.

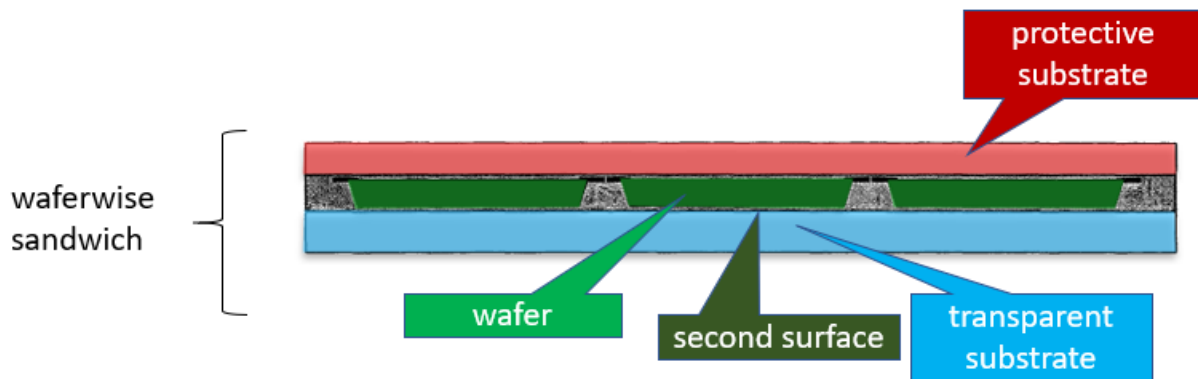
A POSITA would readily understand that the purpose of grinding the silicon wafer from its backside before enclosing it in a glass transparent package is so that the light-sensitive pixel regions are exposed from the backside of the silicon wafer (*i.e.*, ***removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface***).⁶ Ex. 1003, ¶153; *see supra*, §II.B. Accordingly, Badihi at a minimum renders this claim limitation obvious. Ex. 1003, ¶¶152-53.

(e) 1d

Badihi discloses securing a transparent substrate onto the second surface of the wafer thereby producing a waferwise sandwich. Ex. 1003, ¶¶154-156. Badihi's

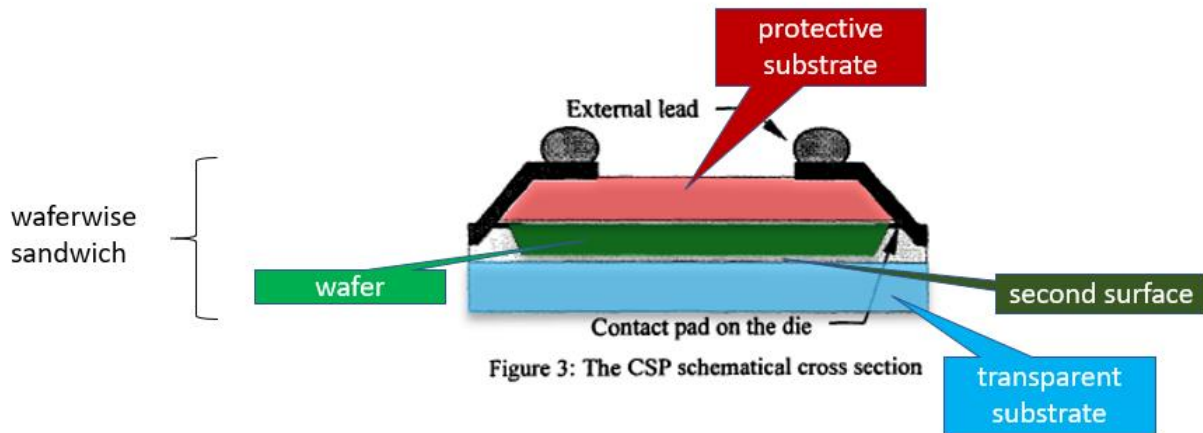
⁶ *See supra*, §II.B; §IX, Ground 1, 1c. Badihi discloses thinning the substrate until it is transparent to visible light like what is described in the '965 patent. Ex. 1003, ¶153 n.4; Ex. 1001, 4:61-5:4.

second glass cover corresponds to the claimed “transparent substrate.” Ex. 1101, 237. Badihi discloses the “second thin glass cover is bonded onto the silicon dies back side to achieve a complete protective enclosure for each die” (*i.e., securing a transparent substrate onto the second surface of the wafer*) resulting in “dies [that] are packaged and encapsulated in separate enclosures while still in wafer form” (*i.e., producing a waferwise sandwich*). *Id.* Specifically, Badihi’s Figure 2 illustrates a waferwise sandwich with the **protective glass layer (first glass cover)** bonded to the active (frontside) surface of the **silicon wafer** and the **second glass cover** bonded to the backside surface of the **silicon wafer**:



Id., 237, Fig. 2.

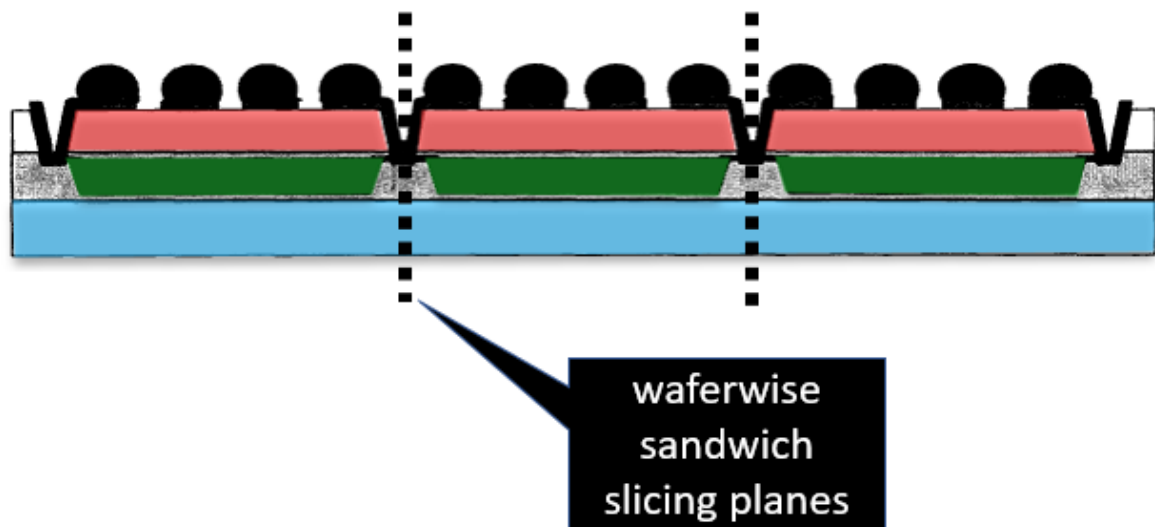
Badihi’s Figure 3 illustrates the resulting packaged image sensor where the **protective glass layer (first glass cover)** and the **second glass cover** sandwich the **silicon wafer** (*i.e., securing a transparent substrate onto the second surface of the wafer, thereby producing a waferwise sandwich*):



Id., Fig. 3.

(f) 1e

Badihi discloses slicing the waferwise sandwich, thereby defining a plurality of backside illuminated image sensors. Ex. 1003, ¶¶157-159. Badihi discloses that “[w]afer [l]evel CSP manufacturing” enables the “packag[ing] [of] all the dies of the entire wafer at the same time rather than ... one die at a time” (*i.e.*, **defining a plurality of backside illuminated image sensors**). Ex. 1101, 237. Specifically, Badihi’s Figure 2 illustrates a process step of “[w]afer dicing” to “yield[] individual packaged dies” (*i.e.*, **slicing the waferwise sandwich, thereby defining a plurality of backside illuminated image sensors**):



Id., 237, Fig. 2.

Badihi's Figure 3 illustrates the resulting packaged image sensor after it is diced:

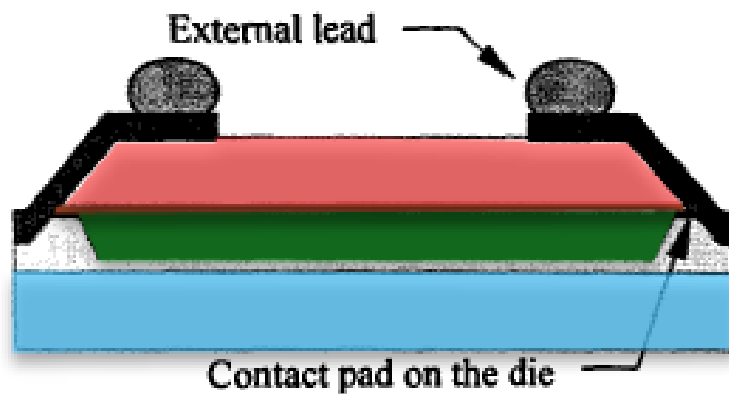


Figure 3: The CSP schematical cross section

Id., Fig. 3.

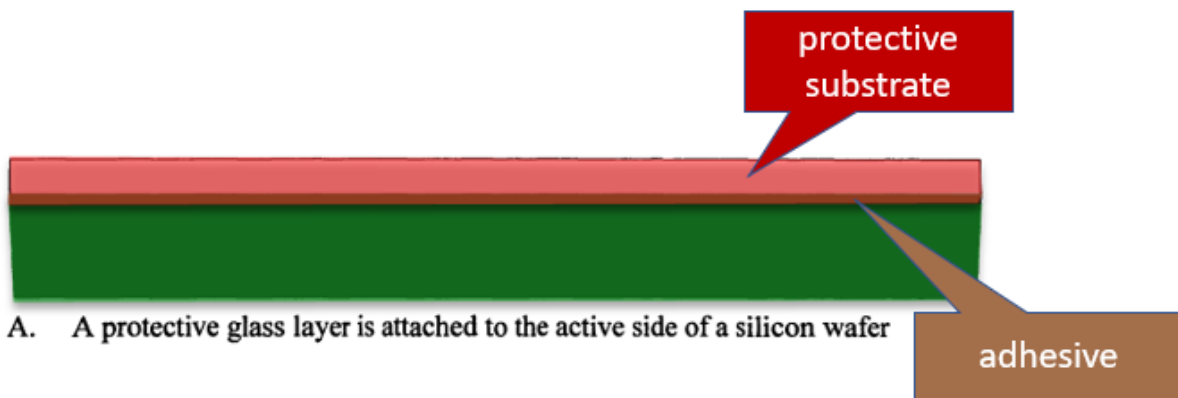
2. Claim 2

(a) 2pre

Badihi discloses 2pre for the same reasons as 1b above. Ex. 1003, ¶160.

(b) 2a

Badihi discloses or renders obvious depositing an adhesive onto the protective substrate. Ex. 1003, ¶¶161-163. Badihi's protective glass layer (first glass cover) and epoxy adhesive correspond to the claimed "protective substrate" and "adhesive," respectively. See *supra*, 1b. Badihi discloses a process step of using an epoxy adhesive to bond a thin protective glass layer to the active side of a silicon wafer. Ex. 1101, 237. Badihi's Figure 2 illustrates the **epoxy adhesive** that is deposited to attach the **protective glass layer** to the active side of a **silicon wafer**:



Id., 237, Fig. 2. It was common practice to use a supporting structure or plate, such as Badihi's protective glass layer, prior to thinning the silicon wafer. Ex. 1003, ¶162; see *supra*, §II.B. It was conventional to apply an adhesive to such supporting structure or plate first before attaching the wafer (*i.e.*, **depositing an adhesive onto the protective substrate**). Ex. 1003, ¶162; see *supra*, §II.B. A POSITA would know how to deposit or apply such epoxy adhesive in Nixon in the same manner as

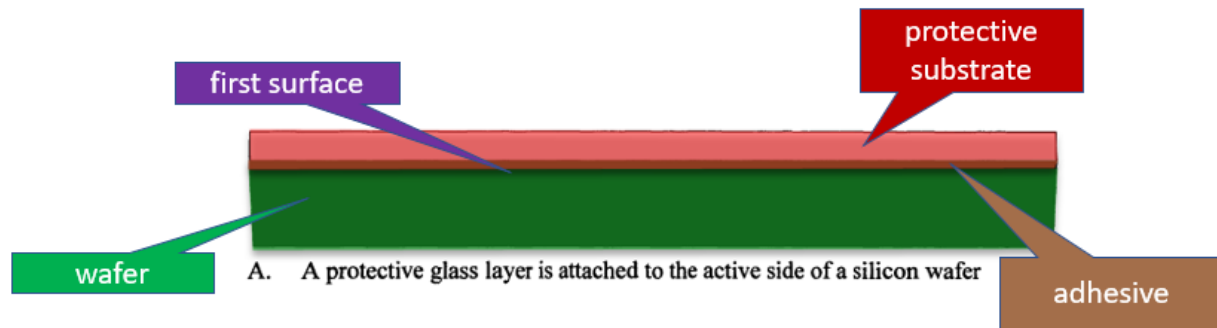
described for the adhesive in the '965 patent. Ex. 1003, ¶162; Ex. 1101, 237, Fig. 2; Ex. 1001, 6:35-40, Fig. 4(A).

A POSITA would also readily recognize that when bonding two surfaces together, adhesive must first be placed on at least one of those surfaces. Ex. 1003, ¶163. In the context of bonding the wafer to the protective substrate, there are only three choices: the adhesive could be placed on the wafer, the protective substrate, or both. *Id.* Whichever of the three choices is used during the manufacturing process is merely a design choice. *Id.*; *Uber*, 957 F.3d at 1340; *Wyers*, 616 F.3d at 1238. Just like in *Uber* and *Wyers*, it would have been obvious to a POSITA to apply the adhesive on the protective substrate. *See supra*, §II.B. Accordingly, Badihi at a minimum renders this limitation obvious. Ex. 1003, ¶¶161-163.

(c) 2b

Badihi discloses placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive. Ex. 1003, ¶¶164-165. Because the epoxy adhesive is applied onto the protective glass layer, the silicon wafer would be placed onto the protective layer where the epoxy adhesive is deposited to secure the protective glass layer onto the silicon wafer (*i.e.*, ***placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive***). Ex. 1003, ¶164; *see supra*, 2a, §II.B. Badihi discloses a process step where “[a] thin protective glass layer is bonded to the active side of a silicon wafer with epoxy

adhesive,” therefore the active side of the silicon wafer would contact the deposited adhesive on the protective glass layer (*i.e.*, ***the first surface contacts the deposited adhesive***). Ex. 1101, 237; *see supra*, 2a. Badihi’s Figure 2 describes that “[a] protective glass layer is attached to the active side of a silicon wafer” and illustrates that the **silicon wafer** is placed onto the **protective glass layer** such that the active side of the **silicon wafer** contacts the **epoxy adhesive** (*i.e.*, ***placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive***):



Id., 237, Fig. 2.

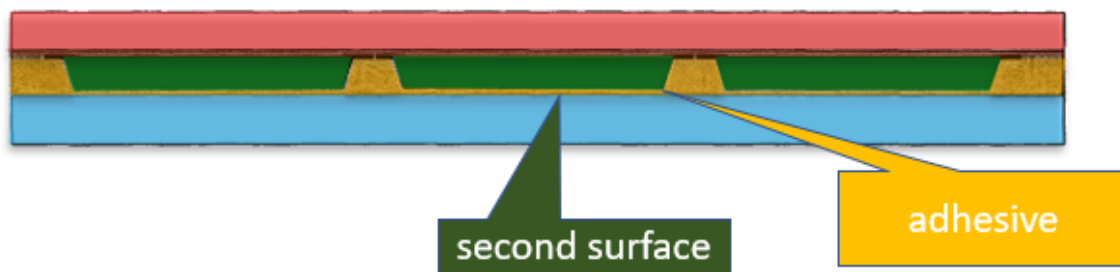
3. Claim 7

(a) 7pre

Badihi discloses 7pre for the same reasons as 1d above. Ex. 1003, ¶¶166-167. Badihi’s second glass cover corresponds to the claimed “transparent substrate.” See *supra*, 1d.

(b) 7a

Badihi discloses or renders obvious depositing an adhesive onto the second surface. Ex. 1003, ¶¶168-170. Badihi's epoxy adhesive corresponds to the claimed "adhesive" and the backside of Badihi's silicon dies correspond to the claimed "second surface." Ex. 1101, 237, Fig. 2. Badihi discloses a process step of bonding the second glass cover to the backside of the silicon dies. *Id.*, 237. For the epoxy adhesive to both fill the grooves and bond second glass cover to the silicon dies, the epoxy would have to be applied first to the wafer structure to fill the grooves and cover the backside of the dies. Ex. 1003, ¶169. This way, the "glass transparent package encases the [i]mager [d]ie in a solid protecting optically clear enclosure." Ex. 1101, 239. If the epoxy is first applied to second glass cover and then placed on the wafer structure, there may not be enough epoxy to fill the grooves between the dies. Ex. 1003, ¶169. Alternatively, epoxy could be applied to both the wafer structure and second glass cover before they are bonded to ensure the epoxy fill the grooves and cover dies for the best bond and complete enclosure. *Id.* Badihi's Figure 2 illustrates depositing an **adhesive** between the grooves and on the backside of the **dies**:



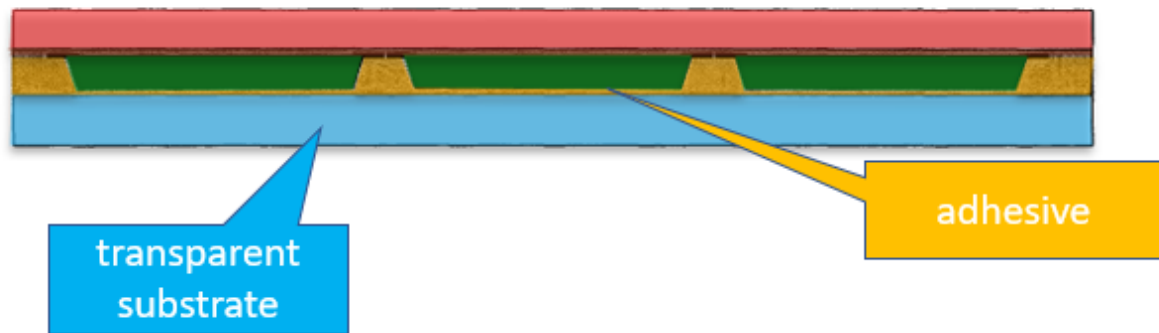
Ex. 1101, 237, Fig. 2. A POSITA would know how to deposit or apply such epoxy adhesive layer in Badihi in the same manner as described for the adhesive in the '965 patent. Ex. 1003, ¶169; Ex. 1101, 237, Fig. 2; Ex. 1001, 7:57-8:3, Fig. 4(E).

A POSITA would readily recognize the three design choices in applying the adhesive on the backside of the wafer, the transparent substrate, or both. Ex. 1003, ¶170. Just like in *Uber* and *Wyers*, it would have been obvious to a POSITA to apply the adhesive on the backside of the wafer (*i.e.*, ***depositing an adhesive onto the second surface***). Ex. 1003, ¶170. Accordingly, Badihi at a minimum renders this limitation obvious. *Id.*, ¶¶168-170.

(c) 7b

Badihi discloses placing the transparent substrate onto the deposited adhesive. Ex. 1003, ¶¶171-172. Because the epoxy adhesive is applied onto the backside of the silicon wafer, the second glass cover would be placed onto the backside of the silicon wafer where the epoxy adhesive is deposited to secure the second glass cover onto the backside of the silicon wafer (*i.e.*, ***placing the transparent substrate onto***

the deposited adhesive). Ex. 1003, ¶171; *see supra*, 7a. Badihi’s Figure 2 illustrates placing the **second glass cover** onto the **adhesive**:



Id., 237, Fig. 2.

4. Claim 8

(a) 8pre

Badihi discloses 8pre for the same reasons as claim 7 above. Ex. 1003, ¶173.

(b) 8a

Badihi discloses separating each of the plurality of image sensor circuits. Ex. 1003, ¶¶174-175. Badihi discloses a process step of removing material from the backside of the silicon wafer. *See supra*, 1c. Badihi further discloses a process step of etching the silicon material between the dies from the backside of the wafer, “yielding individual IC’s attached to the supporting glass layer” (*i.e.*, ***wherein the step of removing material includes separating each of the plurality of image sensor circuits***). Ex. 1101, 237. Badihi’s Figure 2 illustrates etching away the silicon material between the **dies** after the backside is grinded:

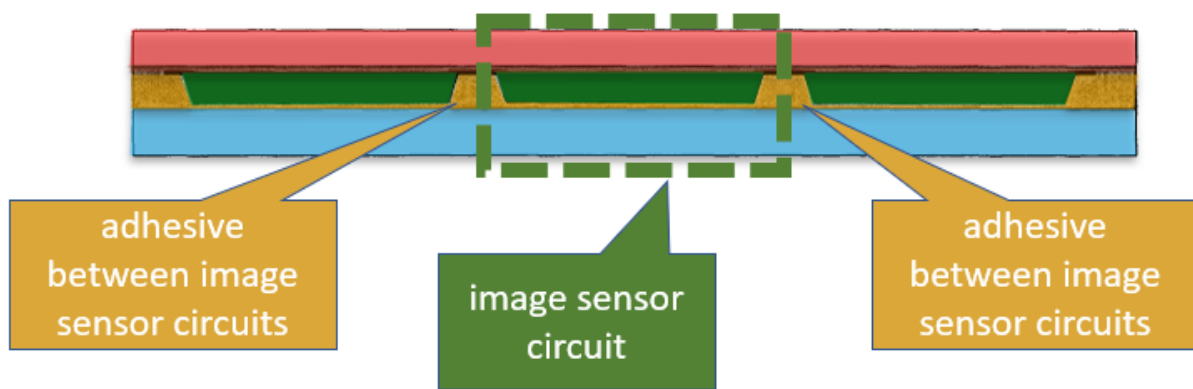


C. The silicon material between the dies (streets) is etched away

Id., 237, Fig. 2.

(c) 8b

Badihi discloses depositing adhesive into interstices located between the plurality of image sensor circuits, thereby protecting the image sensor circuits. Ex. 1003, ¶¶176-177. Badihi discloses a process step of bonding the second glass cover to the backside of the silicon dies “to achieve a complete protective enclosure for each die” (*i.e.*, ***thereby protecting the image sensor circuits***). Ex. 1101, 237. A POSITA would readily recognize that epoxy adhesive may also be used to fill in the grooves or trenches between the dies, which is disclosed in an article also written by the same author for Badihi. Ex. 1003, ¶177; Ex. 1047, Fig. 4 (disclosing that “the epoxy fills the trenches between the dies”). Badihi’s Figure 2 illustrates using **adhesive** to fill in the grooves between the **dies**:



Id., 237, Fig. 2.

5. Claim 9

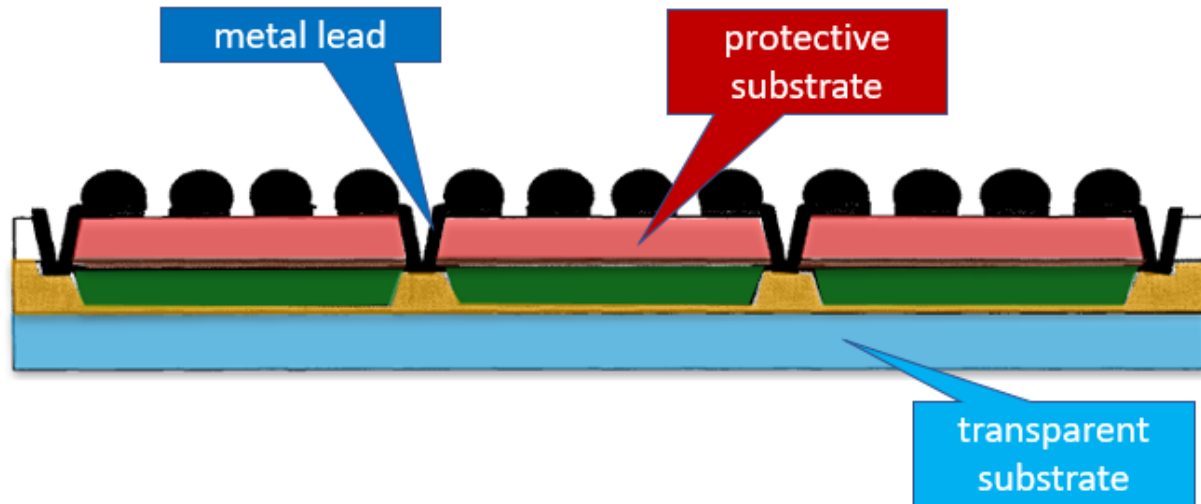
(a) 9pre

Badihi discloses 9pre for the same reasons as claim 1 above. Ex. 1003, ¶178.

(b) 9a

Badihi discloses forming metal leads on the protective substrate after the step of securing the transparent substrate. Ex. 1003, ¶¶179-180. Badihi’s individual leads corresponds to the claimed “metal leads.” Ex. 1101, 237, Figs. 2, 3. Badihi discloses that after the process step where the second glass cover is bonded to the backside of the silicon dies (*i.e., after the step of securing the transparent substrate*), “[d]eep notches are drawn between the dies, revealing the cross-section of the bond pads” and that “[a] metal layer, patterned by lithography to individual leads, is deposited to contact the bond pads at their cross sections” (*i.e., forming metal leads on the protective substrate*). *Id.*, 237. Badihi’s Figure 2 illustrates a

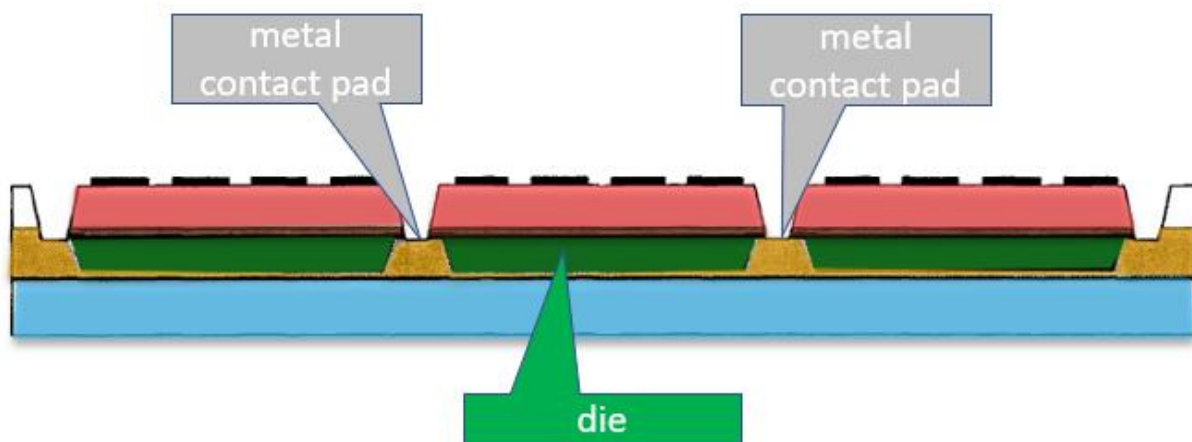
process step of notching between the **dies** from the **protective glass layer (first glass cover)** to expose the bond pads at their cross sections before forming **individual leads** on the **protective glass layer (first glass cover)**:



Id., 237, Fig. 2.

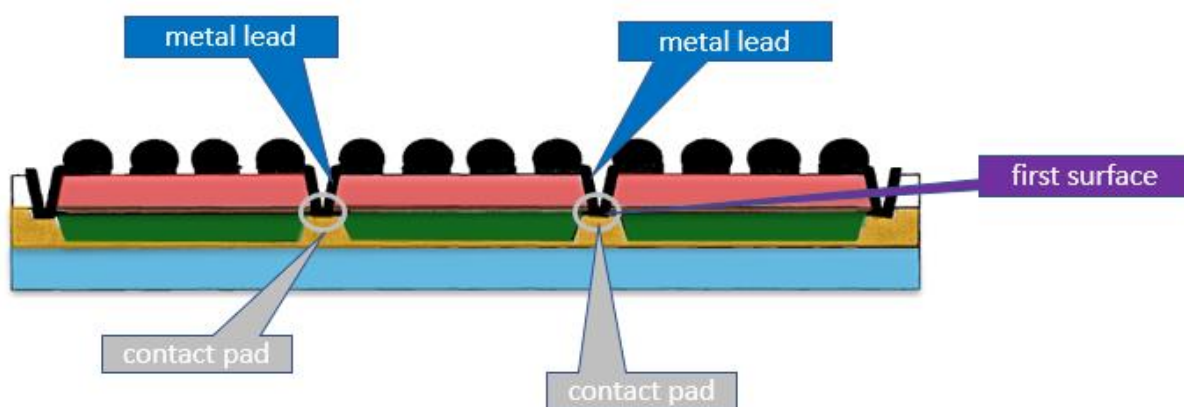
(c) 9b

Badihi discloses the metal leads are connected to metal contact pads located on the first surface of the wafer. Ex. 1003, ¶¶181-183. Badihi discloses a process step where “[a] metal layer, patterned by lithography to individual leads, is deposited to contact the bond pads at their cross sections” (*i.e.*, **wherein the metal leads are connected to metal contact pads**). *See supra*, 9a. Badihi further discloses that “[d]eep notches are drawn between the dies, revealing the cross-section of the **bond pads**,” which is illustrated in one figure in Badihi’s Figure 2: Ex. 1101, 237.



Ex. 1101, 237; Fig. 2.

Another process step in the same figure illustrates **individual leads** that are connected to the **bond pads** on the active side of the wafer through notching (i.e., *wherein the metal leads are connected to metal contact pads located on the first surface of the wafer*):



Id., 237, Fig. 2.

XII. GROUND 4: BADIHI IN VIEW OF ASSADI RENDERS OBVIOUS CLAIM 10

Badihi in view of Assadi renders obvious claim 10. Ex. 1003, ¶¶184-199.

1. Reasons to Combine Badihi with Assadi

A POSITA would have been motivated to modify Badihi's wafer level packaging process for a BSI CMOS image sensor to include a passivation layer to ensure that the frontside (active) surface of the wafer where the microelectronics of the CMOS image sensors are located are protected from abrasion, moisture, or contaminants. Ex. 1003, ¶¶185-186. Badihi teaches a generalized process for manufacturing semiconductor devices, including BSI image sensors. *Id.*, ¶185. Indeed, Badihi's Figure 4 illustrates a packaged image sensor has a frontside blanketed with metal leads and solder bumps and an unobstructed backside to allow light to enter. Ex. 1101, Fig. 4; *see supra*, §II.A, C-D. By the priority date of the '965 patent, it was well-known and highly conventional that passivation layers should be included in CMOS image sensors to protect from, among other things, abrasion, moisture, and contaminants. Ex. 1003, ¶185; *see supra*, §II.C. Assadi provides an example of a passivation layer that provides these well-known benefits. Ex. 1003, ¶185; *see supra*, §II.C. Indeed, Assadi explains that passivation layers should be included "over[] the entirety of sensor 176, including sensor area 210 and non-sensor area (logic area 220 and bond pad area 240)" to provide "resistance to environmental contaminants, particularly moisture." Ex. 1044, 4:26-44, 9:31-32. Including Assadi's passivation layer in Badihi's manufacturing process for a BSI CMOS image sensor would have the obvious added benefit of protecting

the microelectronics necessary to convert the photons collected into electrical signals. Ex. 1003, ¶185; *see supra*, §§II.C-D.

A POSITA would have understood that modifying Badihi’s manufacturing process to include a passivation layer would have been a simple matter of applying well understood semiconductor fabrication techniques. Ex. 1003, ¶186; *see supra*, §§II.C-D. Indeed, Assadi’s passivation layer in a CMOS device is readily applicable to Badihi’s manufacturing process for a BSI CMOS image sensor (as shown in Figure 4). Ex. 1003, ¶186; *see supra*, §§II.C-D. A POSITA could have modified Badihi’s manufacturing process to include a passivation layer such as taught in Merrill with a reasonable expectation of success. Ex. 1003, ¶186; *see supra*, §§II.C-D. Such a modification to Badihi’s manufacturing process would have merely required adding additional conventional, well-known, manufacturing process steps. Ex. 1003, ¶186; *see supra*, §§II.C-D.

2. Claim 10

(a) 10pre

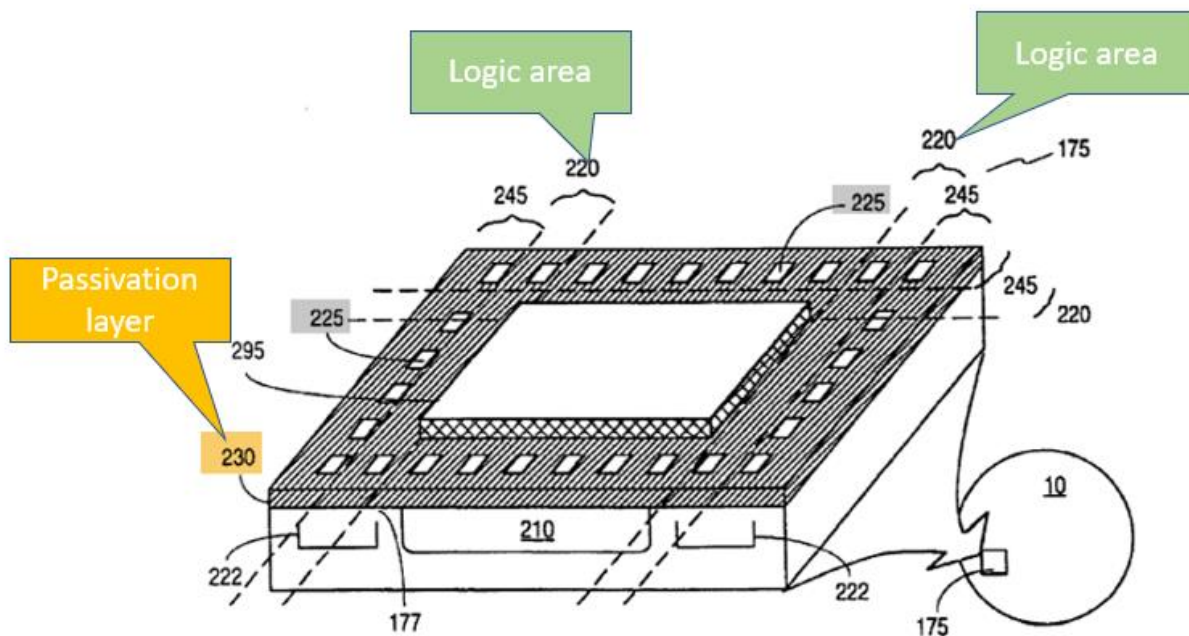
Badihi discloses 10pre for the same reasons as 1b above. Ex. 1003, ¶187.

(b) 10a

Badihi combined with Assadi renders obvious claim 10a’s requirement of “forming a passivation layer on the first surface of the wafer.” Ex. 1003, ¶¶188-190. It was very well-known and highly conventional that passivation layers should be

included in CMOS image sensors to protect from, among other things, abrasion, moisture, and contaminants. Ex. 1003, ¶189; *see supra*, §II.D. Therefore, a POSITA would readily understand that Badihi’s manufacturing process includes a step of “forming a passivation layer on the first surface of the wafer.” Ex. 1003, ¶189; *see supra*, §II.C. Badihi discloses an active side of the silicon wafer, the side of which notches are drawn in order to reveal the bond pads on the active side of the silicon wafer. Ex. 1101, 237, Fig. 2. It would have been conventional to form a passivation layer on the active surface to protect the microelectronics. Ex. 1003, ¶189; *see supra*, §II.C; §X, Ground 2, 10a.

Assadi teaches a conventional mechanism to protect the microelectronics on the active surface. Ex. 1003, ¶190. Assadi’s passivation layer 230 corresponds to the claimed “passivation layer.” Ex. 1044, 4:15-45. Assadi discloses an image sensor 175 with sensor area 210 representing “the photosensing region or area” and logic area 220 that “operates the individual pixels and drives signals from the pixels off sensor 175.” *Id.*, 4:15-26. Assadi further discloses a **passivation layer 230** that “overlies the entirety of sensor 175, including ... logic area 220” (*i.e.*, ***forming a passivation layer on the first surface of the wafer***):



Id., 4:15-45, Fig. 3b (annotated).

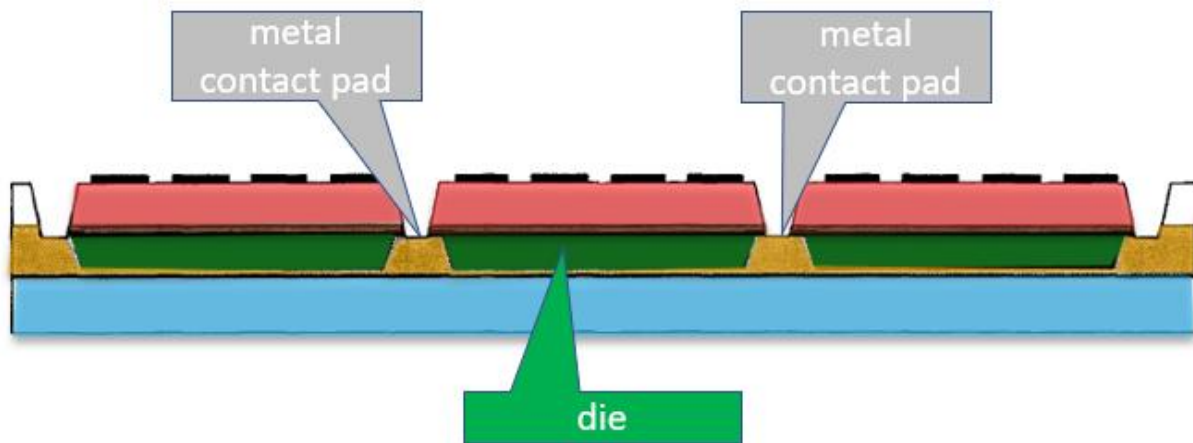
A POSITA would have readily understood at the time of invention the use of a passivation layer equally applies to BSI image sensors and would have been simply a routine, design choice that could easily be implemented by a POSITA. Ex. 1003, ¶191; *see supra*, §II.C. Thus, it would have been obvious for a POSITA to include Assadi’s passivation layer on the active side of Badihi’s wafer-level packaging process of image sensors to protect the pixels from abrasion, moisture, and contaminants. Ex. 1003, ¶191; *see supra*, §§II.C-D.

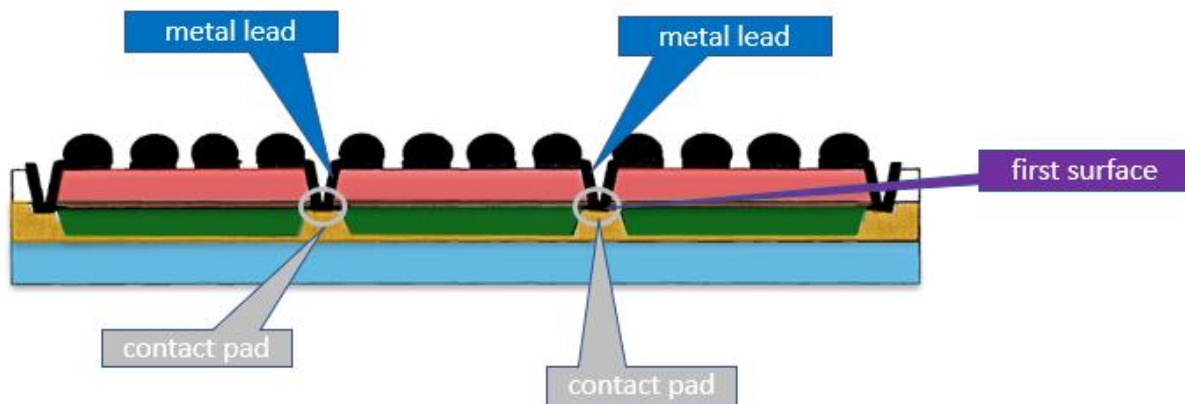
(c) 10b

Badihi combined with Assadi renders obvious claim 10b’s requirement of “forming openings in the passivation layer.” Ex. 1003, ¶¶192-196. A POSITA

would have been motivated to modify Badihi's wafer-level packaging process of image sensors to include Assadi's passivation layer to protect microelectronics on the active side of the silicon wafer. *See supra*, 10a.

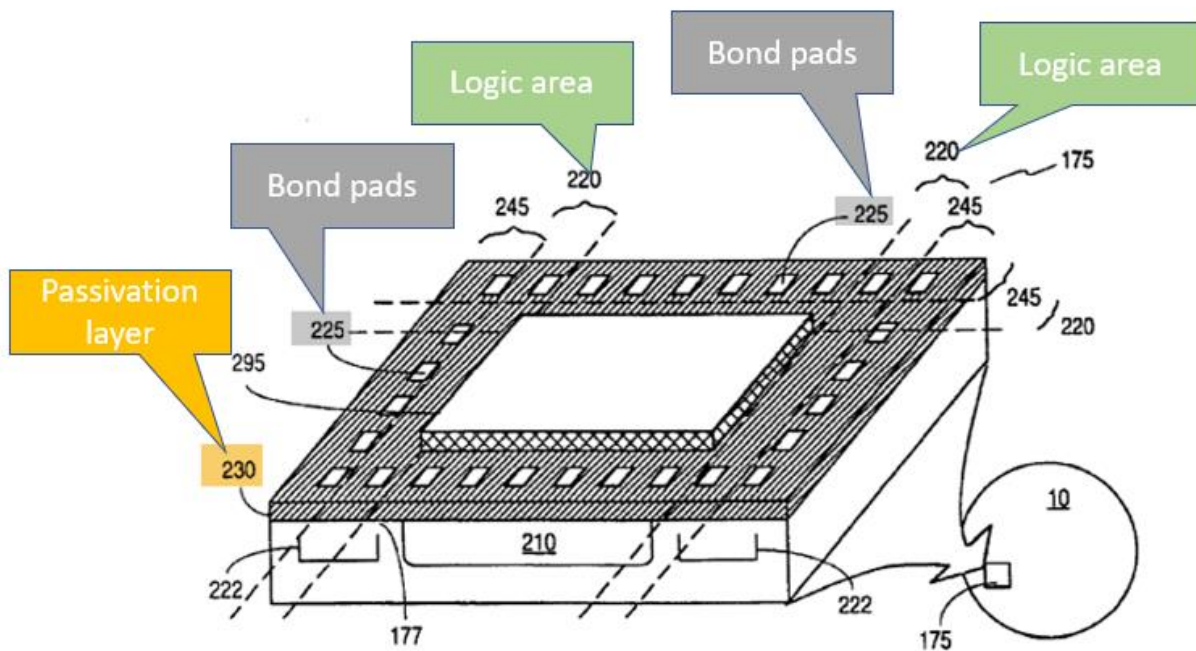
Badihi discloses drawing deep notches from the active side of the silicon wafer to expose the bond pads on the active side of the silicon wafer and then forming individual leads to contact the bond pads. Ex. 1101, 237. Badihi's Figure 2 illustrates that the notching is performed from the active side of the wafer through the **protective glass layer** to reveal the **bond pads** on the active side of the silicon wafer:





Id., 237, Fig. 2.

Assadi discloses a **passivation layer 230** on the frontside (active) surface of image sensor 175, where **openings** for **bond pads 225**, which are “arranged on the ... top surface of sensor 175” and “are electrically linked or coupled to device circuitry 222,” are formed so that the “logic circuitry 220 that operates the individual pixels [can] drive[] signals from the pixels off sensor 175” (i.e., ***forming openings in the passivation layer***), as illustrated in Assadi’s Figure 3b:



Ex. 1044, Fig. 3b, 4:15-45.

A POSITA would readily understand that use of passivation layer would be equally applicable to BSI image sensors and that openings in the passivation layer may be formed before a protective substrate is secured based on the different materials used to form the passivation layer and protective substrate. Ex. 1003, ¶196; *see supra*, §II.C; §X, Ground 2, 10a, 10b.

Accordingly, this limitation would have been obvious over Badihi in combination with Assadi. Ex. 1003, ¶¶192-196.

(d) 10c

Badihi combined with Assadi renders obvious claim 10c's requirement of "securing the protective substrate onto the passivation layer." Ex. 1003, ¶¶197-199.

It would have been obvious to a POSITA to modify Badihi's wafer-level packaging process for image sensors to include Assadi's passivation layer. Ex. 1003, ¶198; *see supra*, 10a. Passivation layer is conventional component that is deposited on the frontside (active) surface of the semiconductor substrate to protect the microelectronics there from abrasion, moisture, or contaminants. Ex. 1003, ¶198; *see supra*, §II.C.

Badihi further discloses a process step where a protective layer is bonded to the silicon wafer using an epoxy adhesive (*i.e.*, ***securing the protective substrate***). Ex. 1101, 237, Fig. 2. A POSITA would also readily understand that Badihi's protective layer would be secured onto Assadi's passivation layer that overlies the frontside (active) surface of the semiconductor substrate (*i.e.*, ***securing the protective substrate onto the passivation layer***) to further protect the Badihi's BSI CMOS image sensor and provide additional support during the step of removal of material from the backside of the semiconductor substrate. Ex. 1003, ¶199; *see supra*, §§II.B-D.

XIII. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies pursuant to Rule 42.104(a) that the '965 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR of the Challenged Claims on the grounds identified in this Petition.⁷

XIV. MANDATORY NOTICES AND FEES

A. Real Party-In-Interest

The real parties-in-interests here is Taiwan Semiconductor Manufacturing Company Limited. No other parties directed, controlled, or funded this *Inter Partes* Review proceeding (IPR).

B. Related Matters

The '965 patent is the subject of the following civil actions and administrative proceedings:

Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Limited, No. 2:22-cv-00298-JRG (E.D. Tex.)

⁷ Alidouble first sued TSMC on the '965 patent on December 14, 2021. *Alidouble Inc. v. Taiwan Semiconductor Manufacturing Company Limited*, No. 2:21-cv-00452-JRG (E.D. Tex.). TSMC was served with the Complaint in that action on December 16, 2021. *Id.*, ECF No. 6. The instant IPR petition is therefore being filed prior to the 1-year bar. 35 U.S.C. § 315(b).

C. Counsel and Service Information

Pursuant to 37 C.F.R. §42.8(b)(3) and 42.10(a), Petitioner provides the following counsel and service information. Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney accompanies this Petition.

LEAD COUNSEL	BACK-UP COUNSEL
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Petitioner consents to electronic service directed to the following email address: qe-tsmc-alidouble-ips@quinnemanuel.com.

D. Payment of Fees

The Office is authorized to charge fees for this Petition to Deposit Account No. 50-5708. Any additional fees that might be due are also authorized.

XV. DISCRETIONARY ANALYSIS FOR REVIEW

The Board has discretion to deny institution under §314(a) and/or §325(d). In addition to the strong merits presented herein, Petitioner also hereby provides a *Sotera*-type stipulation and stipulates that if the PTAB institutes *inter partes* review in relation to any petition filed by TSMC with respect to the '965 patent, Petitioner will not pursue in the district court litigation any ground raised or that could have been reasonably raised in the instituted IPR with respect to the patent claim subject to the instituted IPR. This stipulation precludes discretionary denial under §314(a). See Director Vidal Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, at 3-5, 7-8 (June 21, 2022).

Regarding §325(d), the '965 patent has not previously been challenged at the PTAB. Nor was any reference relied upon herein as part of any ground cited during prosecution or considered by the Examiner. Accordingly, discretionary denial under §325(d) and *General Plastic* is not warranted.

XVI. CONCLUSION

For at least the foregoing reasons, Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Date: December 16, 2022

Respectfully submitted,

By: /s/ James M. Glass

James M. Glass

Counsel for Petitioner

**CERTIFICATE OF COMPLIANCE WITH
TYPE-VOLUME LIMITATION, TYPEFACE REQUIREMENTS,
AND TYPE STYLE REQUIREMENTS**

1. This Petition complies with the type-volume limitation of 14,000 words, comprising 13,768 words, as counted using the Microsoft Word software that was used to prepare this paper, excluding the parts exempted by 37 C.F.R. § 42.24(a).

2. This Petition complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman.

Date: December 16, 2022

By: /s/ James M. Glass

James M. Glass

QUINN EMANUEL URQUHART &
SULLIVAN, LLP

51 Madison Ave, 22nd Floor
New York, New York 10010

Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on December 16, 2022, true and correct copies of the foregoing document and supporting materials were served in its entirety on the Patent Owner at the following address of record listed on the USPTO's Patent Center via FedEx Overnight:

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Date: December 16, 2022

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