

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.

Patent Owner.

U.S. Patent No. 6,168,965

DECLARATION OF DR. KONSTANTINOS P. GIAPIS

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I, Dr. Konstantinos P. Giapis, declare as follows:

1. I have been retained as an expert witness on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) for the above captioned Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 6,168,965 (“the ’965 patent”) (Ex. 1001).

2. I am being compensated for my time in connection with this IPR at my standard consulting rate of \$700 per hour. My compensation is not affected by the outcome of this matter.

3. I have been asked to provide my opinions regarding whether claims 1, 2, 7, 8, 9, and 10 of the ’965 patent (the “Challenged Claims”) are invalid as being anticipated by or obvious over the prior art to a person having ordinary skill in the art at the time of the alleged invention.

4. I am not currently, and have not at any time in the past been, an employee of TSMC. I have no financial interest in TSMC.

I. BACKGROUND AND QUALIFICATIONS

5. I am a professor of chemical engineering at the California Institute of Technology (“Caltech”). I have held that position since 1992.

6. My research relates to processing of semiconductors, dielectrics, and metals, as performed in the fabrication of semiconductor devices, including microprocessors and digital memories. In particular, my work has focused upon

patterning layers of electronic materials to fabricate sub-micron features such as transistor gates, vias, and metal lines found in VLSI circuits. I have also conducted modeling and simulations of the evolution of poly-silicon and metal gate profiles subjected to plasma etching and studied their charging interactions with plasmas. Since the start of my graduate career in 1985, I have accumulated over 35 years of experience on semiconductor materials, devices, and their processing.

7. In my professorial duties at Caltech, I have developed and taught new undergraduate and graduate level courses on semiconductor device physics and their processing. These innovative courses combined solid state physics and electronic materials processing technologies with the more traditional chemical engineering subjects of transport phenomena and chemical thermodynamics. The courses have prepared several generations of students for successful careers in the semiconductor industry.

8. During my research career, I have authored or co-authored 98 peer-reviewed papers, 12 refereed conferences proceedings, two book chapters. Most of my publications relate to semiconductor device processing. My papers on charging damage of high-density integrated devices such as microprocessors, and digital memories are highly cited. I have also been granted 13 patents.

9. My curriculum vitae is provided as Exhibit 1051.

II. MATERIALS REVIEWED AND CONSIDERED

10. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the alleged invention.

11. In forming my opinions, I have reviewed and considered the following documents:

Exhibit No.	Description
1001	U.S. Patent No. 6,168,965 (“the ’965 Patent”)
1002	Prosecution File History for the ’965 Patent
1003	Declaration of Dr. Konstantinos P. Giapis
1004	U.S. Patent No. 6,429,036 (“Nixon”)
1005	U.S. Provisional Patent Application No. 60/116144 (“’144 Nixon Provisional”)
1006	Intentionally omitted
1007	Intentionally omitted
1008	Intentionally omitted
1009	Certified translation of JP H10-116977 (“Muramatsu”)
1010	Certified translation of Sakai, H., <i>CSP Development of Shell Case Type</i> , in THE J. OF JAPAN INST. OF INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS, vol. 12, no. 3, pp. 144-147 (1997) (“Sakai”)
1011	U.S. Pat. No. 5,455,455 (“Badehi I”)

Exhibit No.	Description
1012	U.S. Pat. No. 5,818,404 (“Lebby”)
1013	Fossum, E., <i>Active Pixel Sensors: Are CCDs Dinosaurs?</i> , in CHARGE-COUPLED DEVICES AND SOLID STATE OPTICAL SENSORS III, SPIE, vol. 1900, pp. 2-14 (1993) (“Fossum I”)
1014	Intentionally omitted
1015	Barbe, F., <i>A Tradeoff Analysis for CCD Area Imagers: Frontside Illuminated Interline Transfer vs. Backside Illuminated Frame Transfer</i> , in PROCS., CCD APPLICATIONS CONF., pp. 13-20 (1973) (“Barbe”)
1016	Fossum, E., <i>Ultra-low power imaging systems using CMOS image sensor technology</i> , in ADV. MICRODEVICES AND SPACE SCIENCE SENSORS, SPIE, vol. 2267, pp. 107-111 (Sept. 23, 1994) (“Fossum II”)
1017	Brissot, L., et al., <i>High-definition CCDs for enhanced definition television</i> , in HIGH-RESOLUTION SENSORS AND HYBRID SYSTEMS, SPIE, vol. 1656, pp. 427-436 (Aug. 12, 1992) (“Brissot”)
1018	<i>Introduction to Quantum Efficiency</i> , TELEDYNE, available at https://www.photometrics.com/learn/imaging-topics/quantum-efficiency (“Quantum Efficiency”)
1019	U.S. Patent No. 5,244,817 (“Hawkins”)
1020	U.S. Patent No. 5,270,221 (“Garcia”)
1021	U.S. Patent No. 5,494,833 (“Martin”)
1022	WO1999/040624 (“Badehi II”)
1023	<i>CMOS Fundamentals</i> , SILICON IMAGING, available at http://www.siliconimaging.com/cmos_fundamentals.htm#:~:text=Passive%2Dpixel%20sensors%20(PPS),the%20photosites%20and%20their%20connections (“CMOS Fundamentals”)
1024	U.S. Patent No. 8,063,963 (“Dierickx”)

Exhibit No.	Description
1025	Intentionally omitted
1026	Intentionally omitted
1027	U.S. Patent No. 5,143,855 (“Pace”)
1028	U.S. Patent No. 4,982,079 (“Yagyu”)
1029	U.S. Patent No. 6,960,795 (“Rhodes”)
1030	“Digital camera,” <i>Encyclopedia Britannica</i> (https://www.britannica.com/technology/webcamming) (“Digital camera”)
1031	Sorrell, C., <i>Inside the Nobel Prize: How a CCD Works</i> , WIRED (Oct. 7, 2009), available at https://www.wired.com/2009/10/ccd-inventors-awarded-nobel-prize-40-years-on/ (“How a CCD Works”)
1032	CCD vs. CMOS, TELEDYNE DALSA, available at https://www.teledynedalsa.com/en/learn/knowledge-center/ccd-vs-cmos/ (“CCD vs. CMOS”)
1033	<i>Introduction to Charge-Coupled Devices (CCDs)</i> , NIKON, available at https://www.microscopyu.com/digital-imaging/introduction-to-charge-coupled-devices-ccds (“Intro to CCDs”)
1034	<i>What Is a CMOS Image Sensor?</i> , NANOTEC MUSEUM, available at https://www.tel.com/museum/exhibition/principle/cmos.html (“What is a CMOS Image Sensor”)
1035	Boyd Fowler, X. Liu, P. Vu, <i>CMOS image sensors – past, present and future</i> , Proceedings ICIS 2006 – International Congress of Imaging Science (2006) (“Fowler”)
1036	Intentionally omitted
1037	Intentionally omitted

Exhibit No.	Description
1038	U.S. Patent No. 9,257,479 (“Koizumi”)
1039	Intentionally omitted
1040	Intentionally omitted
1041	Intentionally omitted
1042	Fossum and Hondongwa, <i>A Review of the Pinned Photodiode for CCD and CMOS Image Sensors</i> , IEEE Journal of the Electron Devices Society (May, 2014) (“Fossum III”)
1043	<i>Back-illuminated sensor</i> , WIKIPEDIA, available at https://en.wikipedia.org/wiki/Back-illuminated_sensor
1044	U.S. Pat. No. 6,642,963 (“Assadi”)
1045	U.S. Pat. No. 5,227,313 (“Gluck”)
1046	U.S. Pat. No. 5,789,774 (“Merrill”)
1047	Shweky, Itzik, et al., <i>CSP optoelectronic package for imaging and light detection applications</i> , SPIE, SENSORS, CAMERAS, AND APPLICATIONS FOR DIGITAL PHOTOGRAPHY, vol. 3650, pp. 63-68 (Mar. 22, 1999) (“Shweky”)
1048	WOLF, STANLEY, SILICON PROCESSING FOR THE VLSI ERA: VOLUME 2 – PROCESS INTEGRATION, LATTICE PRESS (1990) (“Wolf”)
1049	U.S. Pat. No. 3,492,763 (“Walsh”)
1050	“PB-159: Digital Camera On A Chip,” PHOTOBIT (“PB-159 datasheet”)
1051	Curriculum Vitae of Dr. Konstantinos P. Giapis
1052	Declaration of Dr. Sylvia Hall-Ellis
1053	Affidavit of Nathaniel E Frank-White

Exhibit No.	Description
1101	Badihi, A., <i>ShellCase Ultrathin Chip Size Package</i> , in PROCS. INT’L SYMPOSIUM ON ADV. PACKING MATERIALS, PROCESSES, PROPERTIES AND INTERFACES (IEEE CAT. NO. 99TH8405), IEEE, pp. 236-40 (Mar. 1999) (“Badihi”), attached as Exhibit 1101 to Declaration of Dr. Sylvia Hall-Ellis
1102	Intentionally omitted
1103	Sakai, attached as Exhibit 1101 to Declaration of Dr. Sylvia Hall-Ellis
1104	Intentionally omitted

III. MY UNDERSTANDING OF PATENT LAW

12. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

13. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the Phillips standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

B. Anticipation

14. I understand that a claim is invalid if it is anticipated. Anticipation of a claim requires that every element of a claim be disclosed expressly or inherently in a single prior-art reference, arranged in the prior-art reference the same way it is arranged in the claim, so that the disclosure effectively puts the public in possession of the invention. For the claim to be anticipated implicitly, I understand that the reference must make clear that the missing descriptive matter in the claim of the patent is necessarily or implicitly present in the allegedly anticipating reference, and that it would be so recognized by one of ordinary skill in the art.

C. Obviousness

15. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed.

16. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

17. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;

- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

18. I understand that a POSITA has ordinary creativity, and is not an automaton.

19. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

20. I understand that prior art to the '965 patent includes patents and printed publications in the relevant art that predate the Priority Date of the '965 patent.

21. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged

invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. OVERVIEW OF THE '965 PATENT

A. Background and Prosecution History

22. The '965 patent is entitled “Method for making backside illuminated image sensor.” The named inventors are Yacov Malinovich and Ephie Koltin. The named assignee of the '965 patent is Alidouble Inc. (“Alidouble”).

23. The '965 patent was filed on August 12, 1999.

24. My opinion analyzes the invalidity of the '965 patent assuming that the Priority Date of the '965 patent is August 12, 1999.

B. Alleged Invention

25. The '965 patent discloses conventional backside illuminated image (BSI) image sensors are expensive because (1) they are made using nonstandard complementary metal-oxide-semiconductor (CMOS) processes and (2) packaging the BSI image sensors is complex. Ex. 1001, 4:13-29. To address these problems,

the '965 patent discloses a method for making and packaging BSI image sensors using standard wafer processing techniques and equipment. *Id.*, 8:47-50.

26. The '965 patent discloses “[a] method for producing a back-illuminated CMOS image sensor including a matrix of pixels (e.g., [complementary metal–oxide–semiconductor] CMOS [active-pixel sensors] APS cells) that are fabricated on a semiconductor substrate.” *Id.*, Abstract. Each pixel “includes a light sensing element that is capable of converting a detected quantity of light into a corresponding electrical signal.” *Id.*, 2:7-10. The method starts with a wafer having image sensor circuits formed on the wafer’s frontside, also known as the active side since that is where all the microelectronics of the image sensor circuits are located. *Id.*, 5:19-26, 6:12-16. The frontside of the wafer is secured to a protective substrate and then the backside of the wafer is thinned until the pixels in the image sensor circuits can detect light passing through the backside of the wafer. *Id.*, 6:28-56. The thinning process may comprise of a grinding process, such as planar erosion, and a chemical etching process. *Id.*, 6:57-7:37. After thinning, a transparent substrate is secured to the backside of the wafer, forming a waferwise sandwich. *Id.*, 7:57-8:3. The waferwise sandwich is sliced to produce individually packaged image sensors. *Id.*, 8:40-46.

27. Figures 4(A)-4(I) are cross-sectional views illustrating the process steps of one such method in accordance with one embodiment of the '965 patent.

Figure 4(A) shows the method starts with a **wafer 300** having **image sensor circuits 100** extending into the **wafer 300**'s first (frontside) surface 310,¹ which is secured by an **adhesive layer 420** onto a **protective substrate 410**:

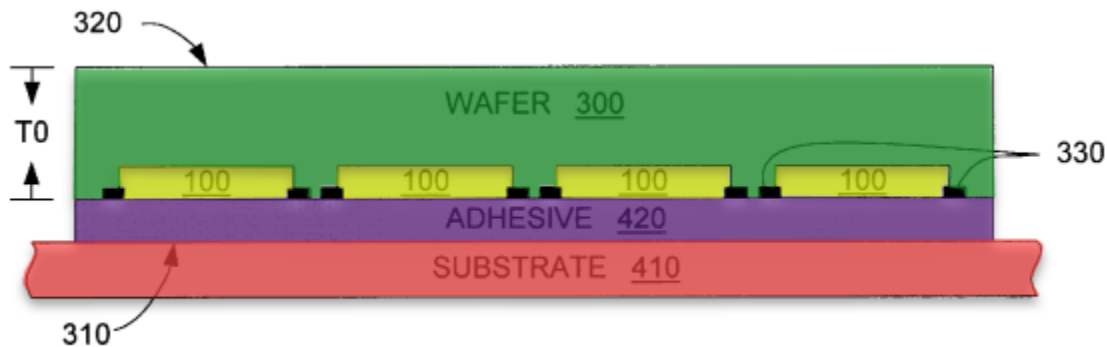


FIG. 4(A)

Id., Fig. 4(A) (annotated). “Each image sensor circuit 100 also includes ... metal contact pads 330 extending onto first surface 310 of wafer 300” and “metal lines (not shown) are formed on wafer 300 and provide connection between metal contact pads 330 and the matrix of light sensitive pixel regions 110” *Id.*, 6:10-19.

¹ The first (frontside) surface 310 is mislabeled in Figure 4(A) and should actually point to where the “image sensors 100 [are] formed,” not in between the adhesive 420 and protective substrate 410. Ex. 1001, 6:27-32, 9:4-8. The location of the first (frontside) surface 310 is correctly identified in Figures 3(B) and 4(C)-4(E). *Id.*, Figs. 3(B), 4(C)-4(E).

28. Figures 4(B) and 4(C) illustrate the process steps of removing material from the second (backside) surface 320 of **wafer 300** with a planar erosion process 433 and a chemical etchant 435 “until the light-sensitive pixel region of image sensor circuits 100 are effectively exposed through the second surface 320 [so] that the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through the second surface 320”:

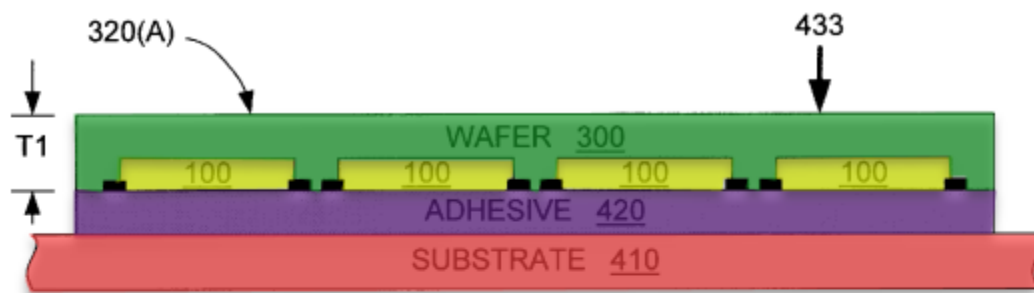


FIG. 4(B)

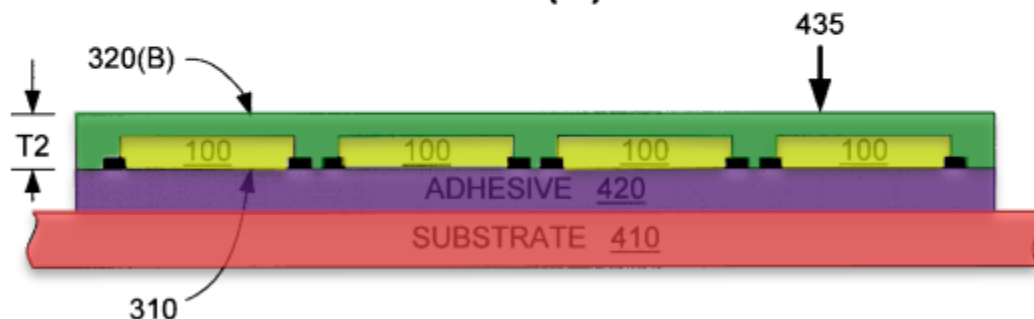


FIG. 4(C)

Id., 6:46-7:19, Figs. 4(B) (annotated)-(C) (annotated).

29. Figure 4(D) illustrates the process step of separating individual image sensor circuits 100 from each other to form dies 300-1 to 300-4 on **protective substrate 410**:

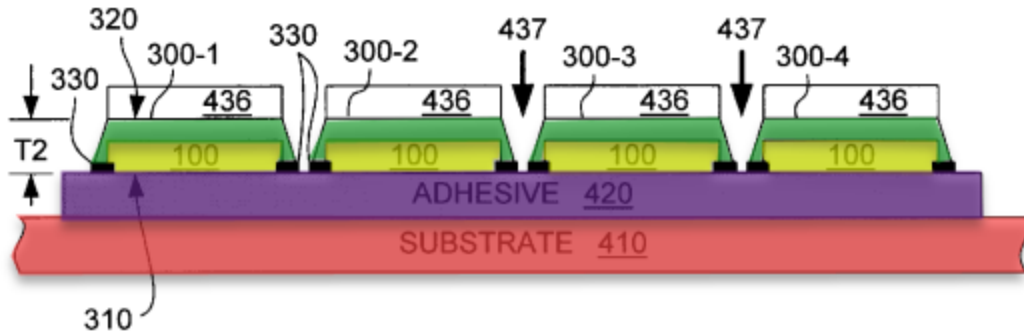


FIG. 4(D)

Id., Fig. 4(D) (annotated), 7:20-37 (“[S]econd surface 320 is scribed long predetermined dice lines and then etched using an etchant 437 to separate the individual image sensor circuits 100”).

30. Figure 4(E) illustrates a process step of securing a **transparent (glass) substrate 440** onto the backside surface 320 of **wafer 300** using a **layer 430** of epoxy, producing a waferwise sandwich:

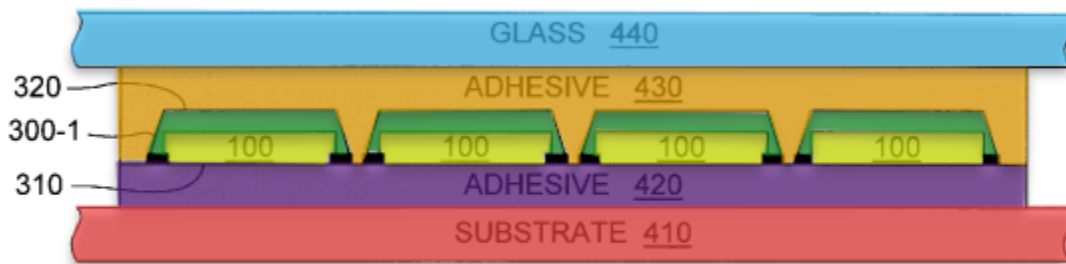
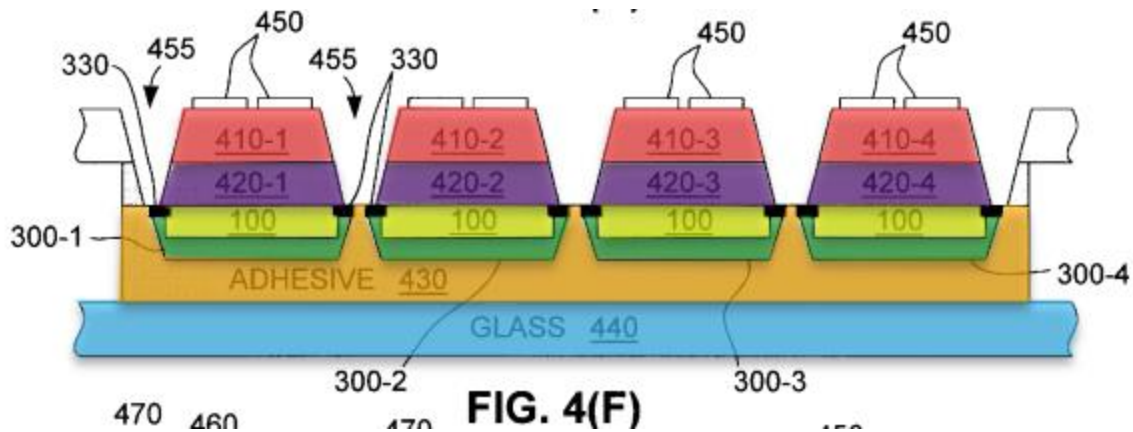


FIG. 4(E)

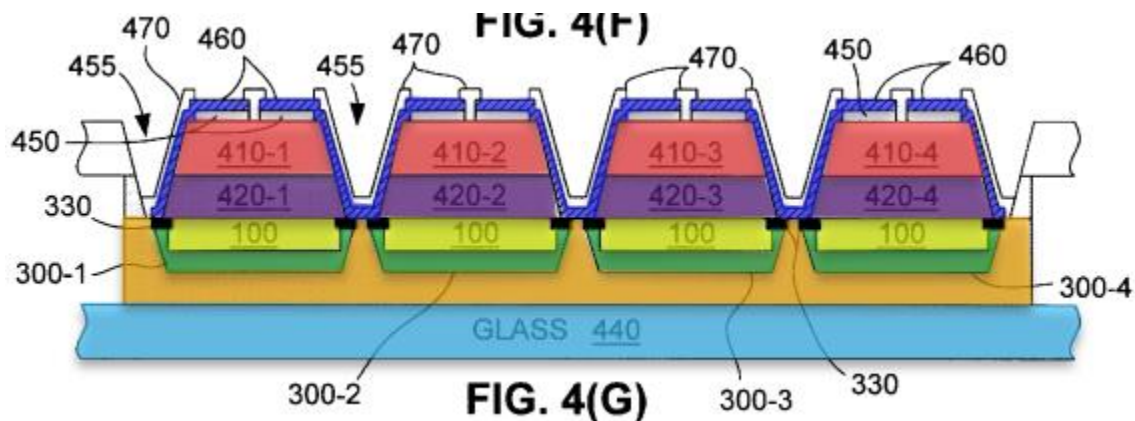
Id., Fig. 4(E) (annotated), 7:52-8:3.

31. Figure 4(F) illustrates a process step of “form[ing] grooves 455 through **protective substrate 410** and **adhesive layer 420** to expose metal contact pads 330”:



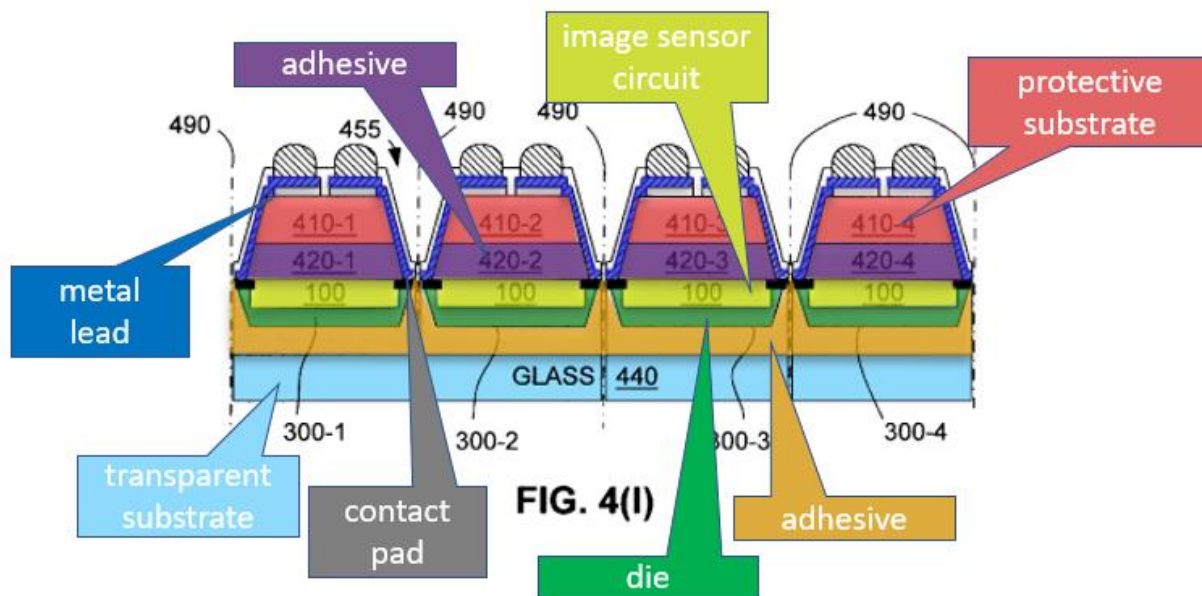
Id., Fig. 4(F) (annotated), 8:4-26.

32. Figure 4(G) illustrates a process step of forming **metal leads 460** in grooves 455 to contact the exposed metal contact pads 330:



Id., Fig. 4(G) (annotated), 8:27-35.

33. Figure 4(H) illustrates a process step of “form[ing] solder bumps 480 using known ball-grid array (BGA) technology” on the “exposed portion of an associated **metal lead 460**,” resulting in the CMOS image sensor illustrated in Figure 4(I) below, where BSI image sensors in a waferwise sandwich about to be diced:



Id., Fig. 4(I) (annotated), 8:36-46. Each BSI image sensor has a **die 300-1** with an **image sensor circuit 100** and **metal contact pads 330**, which provide access to a matrix of light-sensitive pixel regions 110 and control circuitry 120 in image sensor circuit 100. *Id.*, 6:10-16, Fig. 3(B). “Insulation and metal lines (not shown) ... provide connections between metal contact pads 330 and the matrix of light-sensitive pixel regions 110 and control circuitry 120.” *Id.*, 6:16-19.

34. Each BSI image sensor further has a die-sized section 410-1 of a **protective substrate 410** secured to the frontside surface of **die 300-1** by an **adhesive region 420-1**, a die-sized section of a **transparent substrate 440** secured to the backside surface of **die 300-1** by an **adhesive region**, and **metal leads 460** formed over die-sized section 410-1 and “connected to metal contact pads 330 of each image sensor circuit 100 to facilitate signal between each image

sensor circuit 100 and an external system (not shown).” *Id.*, Figs. 4(H), (I), 8:36-46, 8:4-13.

C. Claims

35. The '965 patent has 11 claims. I understand that claims 1, 2, 7, 8, 9, and 10 are the Challenged Claims, with claim 1 as the only independent claim.

36. For convenience, I have reproduced independent claim 1 below and have annotated it with the element numbering that is used in the claim mapping below.

- Preamble: “A method of producing backside illuminated image sensors comprising the steps of:”
- Element [1a]: “producing a plurality of image sensor circuits on a wafer having first and second surfaces each of the image sensor circuits being formed on the first surface and including a matrix of light-sensitive pixel regions extending into the wafer from the first surface;”
- Element [1b]: “securing the wafer onto a protective substrate such that the first surface faces the protective substrate;”
- Element [1c]: “removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface;”

- Element [1d]: “securing a transparent substrate onto the second surface of the wafer, thereby producing a waferwise sandwich; and”
- Element [1e]: “slicing the waferwise sandwich, thereby defining a plurality of backside illuminated image sensors.”

V. OVERVIEW OF THE TECHNOLOGY

A. CCD and CMOS Image Sensors

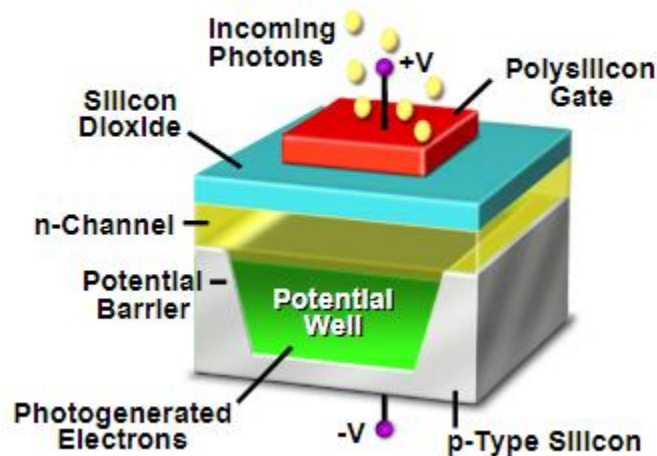
37. Charge-coupled devices (“CCD”) and complementary metal-oxide semiconductor (“CMOS”) image sensors are ubiquitous and typically used in devices that output digital recordings of images. One category of such devices is digital cameras. “At the core of a digital camera is a semiconductor device (CCD) or ... CMOS[], which measures light intensity and colour (using different filters) transmitted through the camera’s lenses. When light strikes the individual light receptors, or pixels, on the semiconductor, an electric current is induced and is translated into binary digits for storage within another digital medium, such as flash memory” Ex. 1030. It was common knowledge that such image sensors would have “a matrix of pixels comprising light sensitive elements [that] constitute[] an image sensor.” Ex. 1024, 1:34-41; Ex. 1038, Abstract.

1. CCDs

38. CCDs were developed in the late 1960s and were the first practical way to let a light-sensitive silicon chip store an image and then digitize it.” Ex.

1031. A CCD sensor is “made up of pixels, each of which is a MOS (metal-oxide semiconductor) capacitor.” *Id.* An illustrative MOS capacitor is shown below:

Figure 2 - Metal Oxide Semiconductor (MOS) Capacitor



Ex. 1033.

39. “As the light falls on each pixel, the photons become electrons ... when photons of light hit the silicon of the pixel and knock electrons out of place.”

Ex. 1031. The electrons are stored in a MOS capacitor or “bucket,” where the charge, or amount of electrons in the bucket, corresponds to the amount of light that has hit that pixel. *Id.* Then, the charge in each row is shifted or transferred from one MOS capacitor to the next down the line until they reach an amplifier and other readout circuitry that convert the analog measurement into a digital value, resulting in a digital grid that describes the image. *Id.*

40. CCDs “were attractive because only three electrodes were required per pixel to make them operate.” Ex. 1013, 6. Initially, “CCD became dominant

[to CMOS], primarily because they gave far superior images with the fabrication technology available.” Ex. 1032.

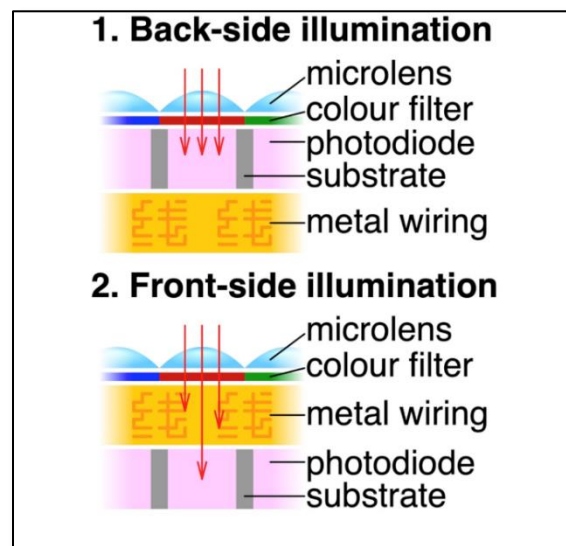
2. CMOS Image Sensor (CIS)

41. CIS were developed around the same time as CCDs but did not become dominant until the 1990s. *See* Ex. 1013, 6; Ex. 1035, 136-137. A CIS is comprised of “a photodiode and a CMOS transistor switch for each pixel, allowing the pixel signals to be amplified individually. By operating the matrix of switches, the pixel signals can be accessed directly and sequentially.” Ex. 1034; Ex. 1016, 2; Ex. 1029, 2:9-41; Ex. 1037. While CIS offered certain advantages over CCDs, such as “smaller size, faster frame rate, lower power consumption, and lower production cost,” they “required more uniformity and smaller features than silicon wafer foundries could deliver at the time.” Ex. 1032; Ex. 1023. Only when microlithography techniques advanced to the point where “pixel size is determined more by scientific imaging optics in the 1990’s than by microlithography constraints” did CIS start becoming more mainstream. Ex. 1013, 6. Indeed, since “[t]he technology push of the semiconductor industry has driven microlithography to the sub-micron regime, and 1.25 micron CMOS is practically an industry standard,” “the fundamental advantage CCDs had over any other imaging technology has been eclipsed.” *Id.*

42. Similarly, the '965 patent also describes that “CMOS image sensors first appeared in 1967,” but that charge coupled devices (CCDs) “have prevailed since their invention in 1970” due to “their superior dynamic range, low fixed-pattern noise (FPN), and high sensitivity to light.” Ex. 1001, 1:20-30. CMOS image sensors only “[m]ore recently ... gained in popularity” due to “advances in CMOS technology. *Id.*, 1:31-52.

3. Frontside Illumination (“FSI”) v. Backside Illumination (“BSI”) CCD

43. There are two fundamental design choices for image sensors: frontside illuminated (FSI) and backside illuminated (BSI). Ex. 1015, 13; Ex. 1017, 428. The difference between a BSI image sensor and a front-side illuminated (FSI) image sensor is the arrangement of imaging elements in the sensor with respect to incident light to the pixel, as shown in the image below:



Ex. 1043 (colors and annotations in original).

44. One important metric for image sensors is quantum efficiency, i.e., “the measure of the effectiveness of an imaging device to convert incident photons into electrons.” Ex. 1018. BSI, as opposed to FSI, allows the image sensors to achieve high quantum efficiency, which is a “desirable feature[.]” Ex. 1019, 1:10-17; Ex. 1020, 4:7-11 (“[O]ne objective of the present invention is to provide a method for fabricating thinned, back-illuminated, solid state image sensors that have an inherently high quantum efficiency over a broad spectral range.”); *see also* Ex. 1021, 2:26-30 (disclosing an “improved Metal Semiconductor Metal (MSM) photodiode device” where “frontside electrodes and backside illumination [is employed] to avoid active area shadowing in the device.”).

45. Similarly, the ’965 patent also discloses that BSI CMOS image sensors “are alternative image sensor structures that address the fill factor problems associated with front illumination.” Ex. 1001, 3:51-4:11 (describing “fill factor” as “the ratio of light sensing area to total pixel areas”).

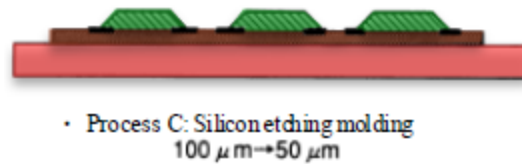
B. Removal of Material from Backside of Wafer

46. Removal of material from the backside of the wafer was well known before the priority date of the ’965 patent. It was common practice during the manufacturing of CIS to attach the frontside of the silicon wafer (i.e., the active side) with BSI image sensors to another wafer for support for further processing of the backside and then using a combination of backside grinding and chemical

etching techniques to thin the backside of the BSI image sensors to allow the photons to be absorbed by the thinned substrate closer to the photodiode. Ex. 1020, 2:10-22, 6:10-42; *see also* Ex. 1022, 14 (describing the wafer being “thinned at its non-active surface” using commercially available grinding apparatus and/or etched using a conventional, commercially available Chemical-Mechanical Planarization (CMP) equipment); Ex. 1037. It was conventional to attach a device wafer to a supporting structure or plate before the device wafer is thinned. Ex. 1049, 3:19-66. In doing so, it was common practice to apply the adhesive, such as wax, to the supporting structure or plate first before placing the device wafer to the supporting structure or plate. *Id.*, 3:19-4:13, Fig. 1.

47. It was also conventional to reduce the backside substrate thickness so that light is absorbed near the photodiode and to prevent the photogenerated electrons and holes from recombining before they can be collected by the photodiode. Ex. 1009, ¶109, Fig. 6(b). Sakai discloses a manufacturing method of a ShellCase-type chip size package (CSP) where one of the steps requires “[g]rinding the silicon wafer down to 100 μm ” and then etching to 50 μm . Ex. 1010, 145, Fig. 5. Sakai’s Figure 5 illustrates **removing material** from the **backside** of the **silicon wafer**:





Id., Fig. 5 (annotated).

48. Similarly, the '965 patent confirms that removing material from the backside of the wafer is a conventional technique. Ex. 1001, 4:36-48 (describing fabrication according to “well-established processing parameters”), 6:57-67 (describing “coarse and fine grinding operations” “using known techniques”).

C. Passivation Layer in Image Sensors

49. The use of a passivation layer on the frontside (active) surface of an image sensor was well-known before the priority date of the '965 patent. In 1990, Wolf describes that “a passivation layer is deposited over the entire top surface of the wafers. This is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging.” Ex. 1048, 273, Table 4.5 (disclosing that a passivation layer “[p]rovides good scratch protection to the underlying circuit structures” and is “[i]mpermeable to moisture” among other things); Ex. 1027, Abstract, 1:13-22; Ex. 1028, 5:43-6:5. Gluck discloses the use of a layer 260 for a BSI CCD image sensor, where layer 260 “represents a passivation coating of deposited silicon dioxide which acts as a scratch coat and etch mask” and serves to “protect[] the device on the opposite side of the wafer” when its backside is etched. Ex. 1045, 5:26-34, Fig. 7.

50. It was also well-known to form openings in the passivation layer in order to connect electrically to the outside world so that electrical signals converted from the collected photons could be transmitted from the image sensor. Ex. 1027, 1:67-2:17. For example, Gluck discloses passivation coating 260 covers and protects aluminum bond pads 250 during the etching process from the backside of the wafer. Ex. 1045, 5:26-34, Fig. 7. Subsequently, the **bond pad contacts** are opened through **passivation coating 260** using “standard procedures” before “dicing and packaging operations,” as illustrated in Gluck’s Figure 7:

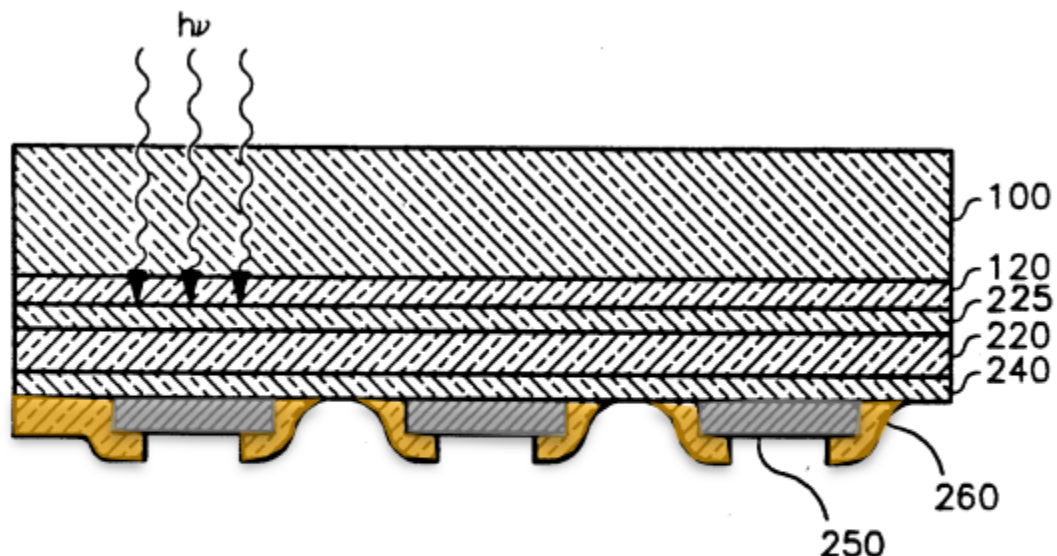
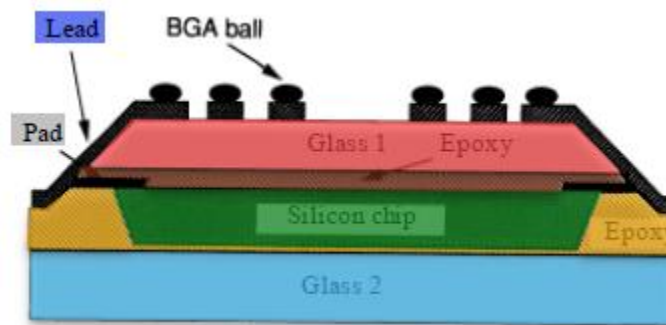


FIG. 7

Id., Fig. 7 (annotated).

D. Wafer-Level Packaging Process

51. Wafer-level packaging of BSI image sensors based on conventional semiconductor process and standard semiconductor manufacturing equipment was well known. Ex. 1010, 144-146, Figs. 3, 5. For example, it was well-known to package a die with a protective shell comprised of glass sheets at the top and bottom of the die. *Id.*, 144-146, Figs. 3, 5. It was also well-known to provide pads in between the top glass sheet covering the top or active surface of the silicon die and the silicon die itself, and to provide electrical leads on the top glass sheet that are connected to the pads as part of this conventional packaging process. *Id.*, 144, 146, Figs. 3, 5. Sakai's Figure 3 illustrates the resulting packaged die, with the **silicon chip** sandwiched by **glass 1** and **glass 2** and the **pads** connected to the **electrical leads**:



Id., Fig. 3 (annotated).

VI. LEVEL OF ORDINARY SKILL IN THE ART

52. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the

technology, the type of problems encountered in the art, and the prior art solutions to those problems.

53. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '965 patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '965 patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

54. Based on the materials I have considered and my own experiences, it is my opinion that a person of ordinary skill in the art ("POSITA") at the time of the alleged invention would have been a person having a master's degree in electrical engineering, computer engineering, or physics with at least two years of industry experience in integrated circuit design, layout, packaging or fabrication. A greater level of experience may compensate for less education, and vice versa.

55. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VII. CLAIM CONSTRUCTION

56. For purposes of this proceeding, the claim terms do not need to be construed to resolve the prior art issues presented in this Petition. This is because, as detailed below, each of the prior art grounds teaches, in relevant part, the exact same combination of features found in the '965 patent.

VIII. OVERVIEW OF THE PRIOR ART

A. Nixon

57. Nixon claims priority to the '144 Nixon Provisional, which includes an Invention Disclosure Technical Description ("IDTD") and an article entitled "A CSP Optoelectronic Package for Imaging and Light Detection Applications" by Shweky et al. ("Shweky"). Shweky is incorporated in the '144 Nixon Provisional as a prior art reference, upon which the IDTD claims an improvement using wafer level processing and packaging techniques for CMOS imaging, including its backside.

58. I was asked to analyze whether the '144 Nixon Provisional supports all aspects of the disclosures of the Nixon reference in this petition. It does. For example, claim 1 of Nixon is supported by the following portions of the '144 Nixon Provisional:

Nixon (Ex. 1004)	Exemplary Support (Ex. 1006)
Claim 1	'114 Prov.

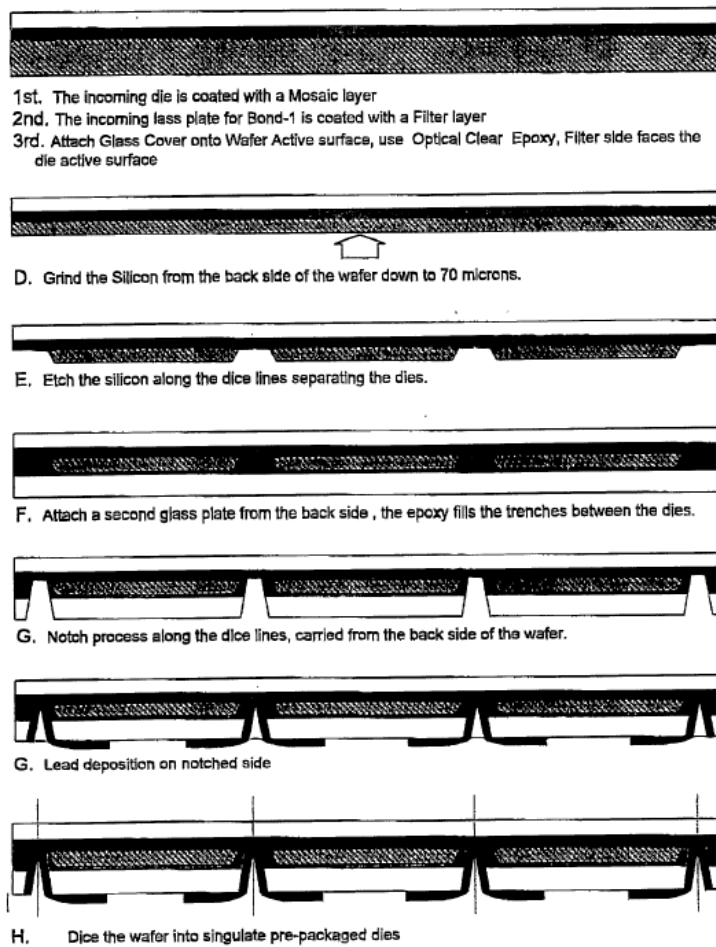
1. A method...comprising:	IDTD, PDF pages 4-5, Figs. 1-2 Shweky, PDF pages 7-9, Fig. 4
attaching a first cover layer...a silicon wafer	IDTD, PDF pages 4-5, Figs. 1-2 Shweky, PDF pages 7-9, Fig. 4
attaching a second cover layer...the silicon wafer	IDTD, PDF pages 4-5, Figs. 1-2 Shweky, PDF pages 7-9, Fig. 4
notching...the second cover layer; and	IDTD, PDF pages 4-5, Fig. 1 Shweky, PDF pages 7-9, Fig 4
forming...the silicon wafer;	IDTD, PDF pages 4-5, Fig. 1 Shweky, PDF pages 7-9, Fig 4
wherein....from a back side.	IDTD, PDF pages 4-5, Fig. 1 Shweky, PDF pages 7-9, Fig 4

Nixon [1pre] A method of manufacturing an image sensor comprising:
--

59. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

60. Specifically, the '144 Nixon Provisional discloses that the “essence of this disclosure,” among other things, is the “[b]ackside imaging using wafer level processing techniques to obtain thinning and integrated packaging of the image sensor.” Ex. 1005, IDTD, 4. Shweky’s Figure 4 also provides support for this limitation, as it illustrates a manufacturing process for image sensors:

Figure 4: Optronic Package Schematical Process



Id., Shweky, Fig. 4.

Nixon [1a] attaching a first cover layer to an active surface of a silicon wafer;

61. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

62. Shweky discloses a process step of attaching a **(first) glass cover** to the active surface of a **wafer** in Figure 4:

Figure 4: Optronic Package Schematical Process



- 1st. The incoming die is coated with a Mosaic layer
- 2nd. The incoming lass plate for Bond-1 is coated with a Filter layer
- 3rd. Attach Glass Cover onto Wafer Active surface, use Optical Clear Epoxy, Filter side faces the die active surface

Ex. 1005, Shweky, 8, Fig. 4 (annotated). At the end of the manufacturing process, Shweky discloses dicing the wafer into packaged image sensors. *Id.*, Shweky, 8, Fig. 4.

63. Relatedly, IDTD discloses each packaged image sensor has a **glass plate (first glass cover)** attached to the active surface (where **pixels** are located) of a **silicon die** in Figure 1:

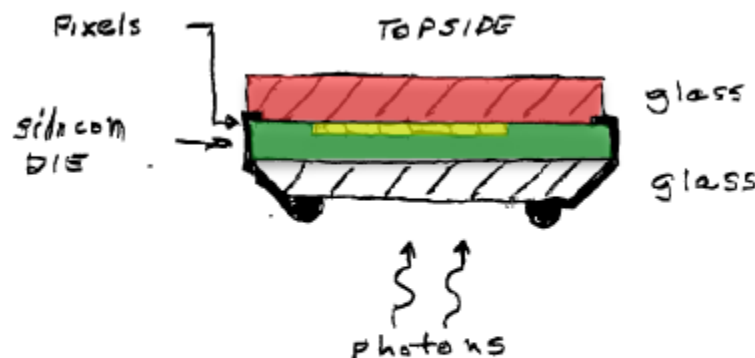


Figure 1.

Id., IDTD, 4-5, Fig. 1 (annotated).

Nixon [1b] attaching a second cover layer to an opposite surface of the silicon wafer;

64. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

65. Shweky discloses a process step of attaching a **second glass plate (second glass cover)** to the backside of the **wafer** in Figure 4:



F. Attach a second glass plate from the back side, the epoxy fills the trenches between the dies.

Ex. 1005, Shweky, 8, Fig. 4 (annotated).

66. Relatedly, the IDTD discloses the resulting packaged image sensor has **another glass plate (second glass cover)** attached to the backside of the **silicon die** in Figure 1:

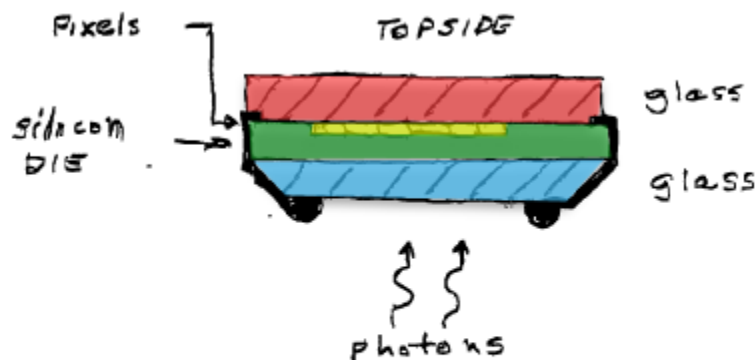


Figure 1.

Id., IDTD, 4-5, Fig. 1 (annotated).

Nixon [1c] notching the silicon wafer along the second cover layer; and

67. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

68. Shweky discloses that “[d]eep notches are drawn between the dice, so as to reveal the pads cross section.” Ex. 1005, Shweky, 8. Shweky discloses the process step of forming **notches** along the backside of the **wafer** through the **second glass plate (second glass cover)** in Figure 4:



Id., Fig. 4 (annotated).

Nixon [1d] forming electrical interconnections on the notched surface of the silicon wafer;

69. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

70. IDTD discloses that conventionally, the bump contacts and interconnect lines are located on the backside of the wafer for FSI image sensors. Ex. 1005, IDTD, 4, Fig. 1. Shweky discloses a process step of depositing a metal layer “to contact the metal pads at their cross sections.” Ex. 1005, Shweky, 8. Shweky’s Figure 4 shows that **leads** are deposited on the notched sides of the **wafer**:



Id., Fig. 4 (annotated).

Nixon [1e] wherein the image sensor is light sensitive from a back side.

71. I am of the opinion that the '144 Nixon Provisional discloses this claim element of Nixon.

72. IDTD discloses the resulting packaged image sensor has “the ability to do backside imaging ... by 1) thinning the silicon ... and 2) relocating the ... bump contacts and interconnect lines away from the image area of the die and covering with optically transparent material to give support.” Ex. 1005, IDTD, 4-5. IDTD’s Figure 1 illustrates the packaged image sensor receiving photons from the backside:

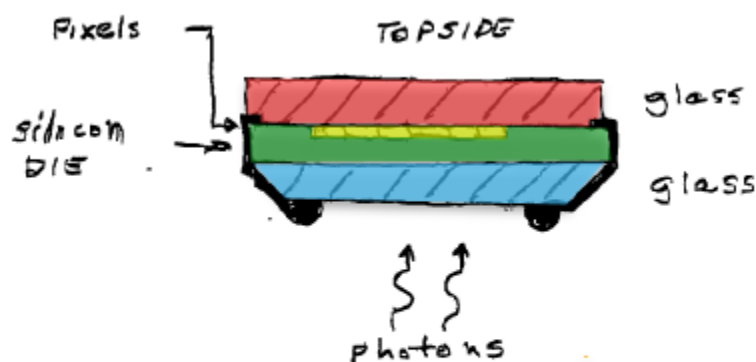


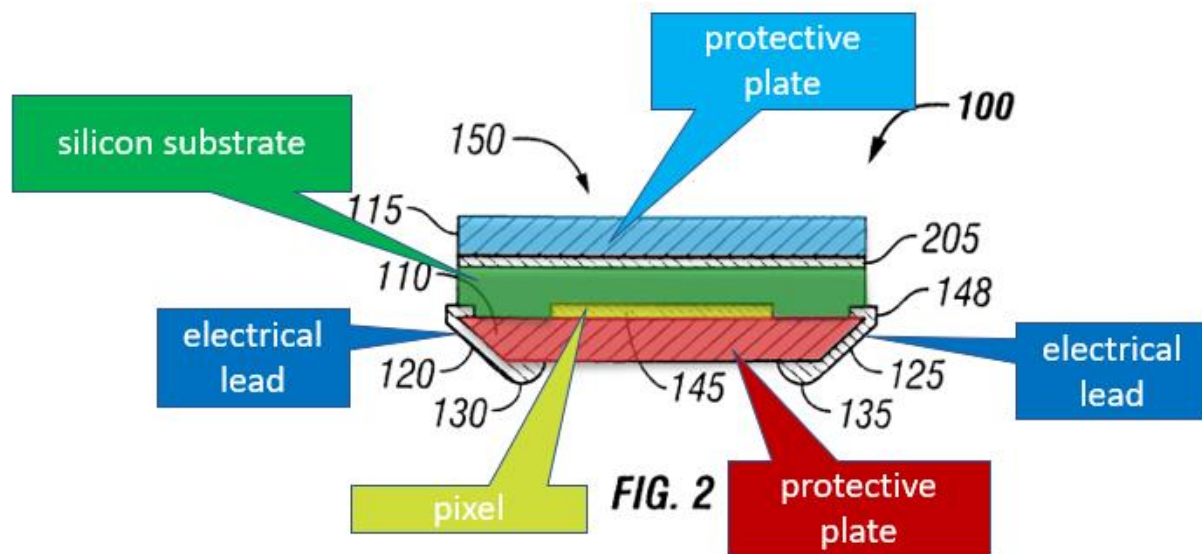
Figure 1.

Id., IDTD, 4-5, Fig. 1 (annotated).

1. Overview of Nixon

73. Nixon discloses “the manufacturing of CMOS image sensors capable of backside illumination.” Ex. 1004, 1:8-10. “[U]sing semiconductor manufacturing processes,” “[t]he image sensor 100 is packaged at the wafer level” and “[t]he manufacturing process ... results in lower cost, particularly for smaller dies.” *Id.*, 1:65-2:1, 3:16-17.

74. Nixon’s Figure 1 and 2 illustrate two embodiments of a BSI CMOS image sensor 100 and Nixon’s Figure 4 illustrates the manufacturing process for the image sensor 100 of Figures 1 and 2. *Id.*, 1:56-57, 1:61-62, Figs. 1, 2, 4. Both embodiments have a **silicon substrate 105** sandwiched between a **protective plate 110** and a **protective plate 115**. *Id.*, 2:1-3, Figs. 1, 2. **Pixels 145** are formed on the active surface of **silicon substrate 105** facing **protective plate 110**. *Id.*, 2:8-10, Figs. 1, 2. Protective plates **110** and **115** are made from glass plates. *Id.*, 2:26-28, 2:49-52. The embodiment in Figure 2 has **electrical leads 120, 125** and pads 130, 135 formed on **protective plate 110** at the frontside of image sensor 100 so light can enter unobstructed through **protective plate 115** at the backside of image sensor 100:



Id., Fig. 2 (annotated), 2:16-22. Both embodiments disclose notching in order to expose the metal pads 130, 135 to be connected with the electrical leads 120, 125, with Figure 1 illustrating notching from the protective plate 115 and Figure 2 illustrating notching from the protective plate 110. *Id.*, Figs. 1, 2, 1:65-2:10, 2:15-22.

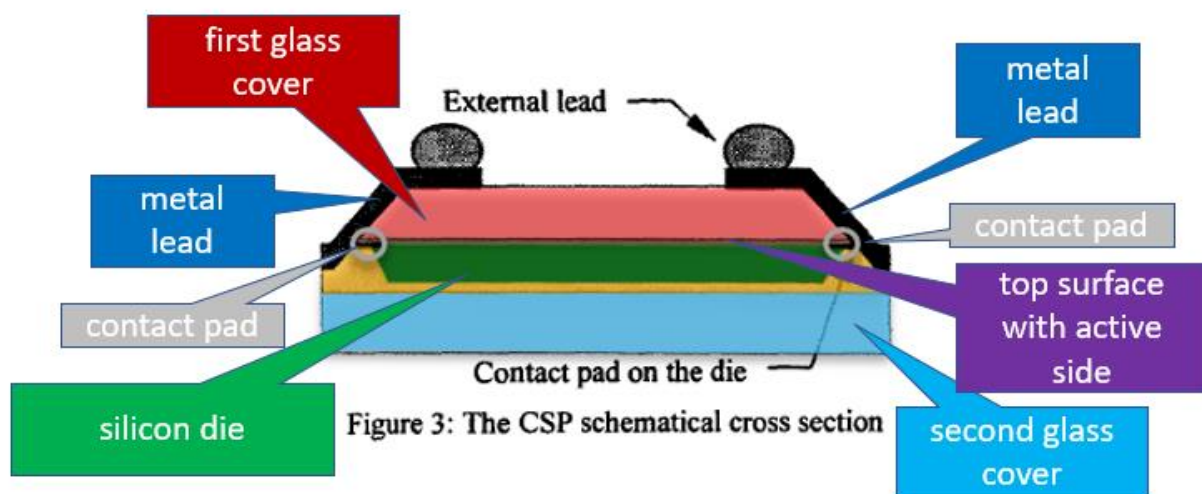
B. Badihi

75. Badihi was published in the *Proceedings International Symposium on Advanced Packaging Materials, Processes, Properties and Interfaces*, which I am aware of. In my experience, Badihi, along with the other papers presented at that conference (and published in its proceedings), would have been available as of the publication of those proceedings.

76. Badihi discloses a ShellCase Chip Size Package (CSP) for, inter alia, BSI CMOS image sensors. Ex. 1101, 236, 239. Badihi's ShellCase CSPs are

made with a “wafer-level packaging process ... [that] can be accomplished with commercial [s]emiconductor wafer processing equipment” and be “based on [s]emiconductor processes.” *Id.*, 236, 240. For example, Badihi discloses bonding a first glass cover to the active side of the silicon wafer, etching away the silicon material from the back side of the wafer, bonding a second glass cover to the backside of the wafer, drawing deep notches between dies to expose the bond pads, depositing a metal layer to contact the bond pads, and dicing the wafer to yield individual dies. *Id.*, 237.

77. Badihi’s Figure 3 illustrates the ShellCase CSP has a **silicon die** (e.g., an **imager die**) sandwiched between a **first glass cover** and a **second glass cover**, with the active side of the **silicon die** facing the **first glass cover**, **contact pads** formed on the active side of the **silicon die**, and **individuals metal leads** formed on the **first glass cover** to contact the **contact pads**:



Id., 237, Fig. 3 (annotated); *see also id.*, 237, Fig. 2. Badihi further discloses that the above ShellCase CSP package is a “glass transparent package [that] encases the [i]mager [d]ie in a solid protecting optically clear enclosure,” including, for example, packaged CMOS APS shown in Badihi’s Figure 4. *Id.*, 239, Fig. 4.

C. Assadi

78. Assadi discloses a passivation layer 230 that “[o]verl[ies] the top surface of image sensor 175” and is made, for example, of silicon nitride based on its “particular resistance to environmental contaminants, particularly moisture.” Ex. 1044, 4:35-45, Fig. 3b. Assadi discloses **bond pads 225**, which may be on the “top surface of sensor 176” and in bond pad area 240 and that the **passivation layer 230** “overlies the entirety of sensor 175, including ... bond pad area 240,” as illustrated in Assadi’s Figure 3b:

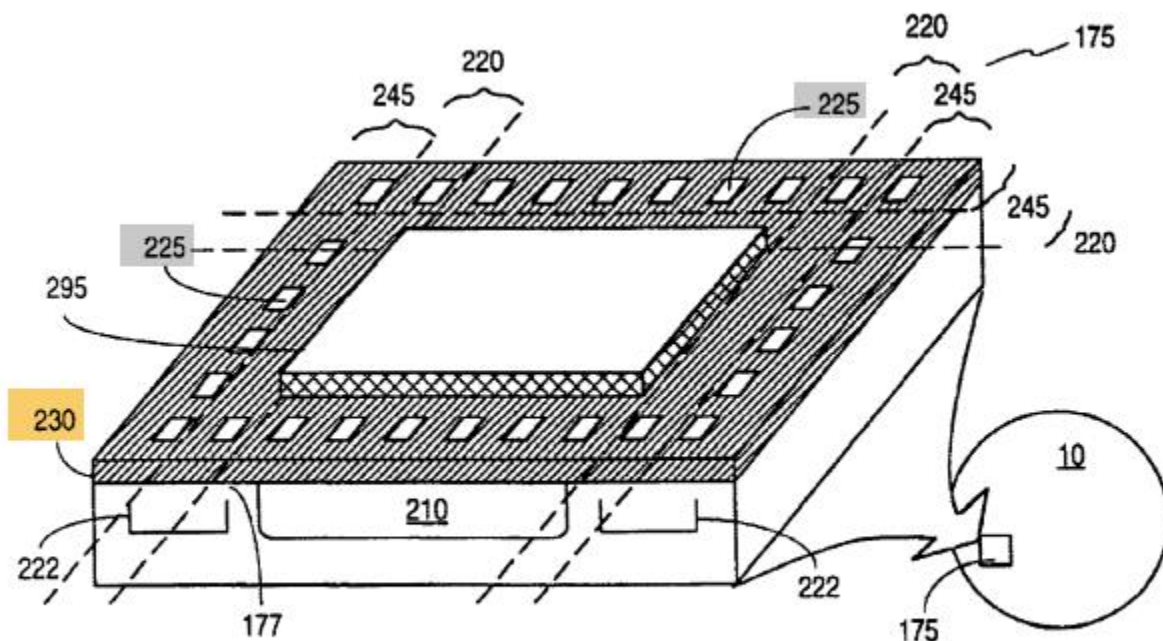


Fig. 3b

Ex. 1044, 4:35-45, Fig. 3b (annotated).

IX. GROUNDS OF CHALLENGE

79. I am of the opinion that the Challenged Claims of the '965 patent are invalid on the following grounds:

Grounds	Claims	Statutory Basis	Prior Art
1	1, 2, 7, 8, 9	§103	Nixon
2	10	§103	Nixon and Assadi
3	1, 2, 7, 8, 9	§103	Badihi
4	10	§103	Badihi and Assadi

80. None of these references relied upon were before or considered by the Examiner during prosecution of the '965 patent. Further, none of the Grounds

above relies on prior art reference combinations that were evaluated during prosecution of the '965 patent.

X. GROUND 1: NIXON RENDERS OBVIOUS CLAIMS 1, 2, 7, 8, AND 9

81. I am of the opinion that Nixon renders obvious claims 1, 2, 7, 8, and 9 of the '965 patent.

1. Claim 1

[1pre] A method of producing backside illuminated image sensors comprising the steps of:

82. To the extent the preamble is considered to be a limitation, I am of the opinion that Nixon discloses this claim element.

83. Nixon discloses that “[t]his invention relates ... to the manufacturing of CMOS image sensors capable of backside illumination,” such as BSI CMOS image sensors 100 (*i.e., a method of producing backside illuminated image sensors*). Ex. 1004, 1:8-10, Abstract, Figs. 1, 2, 4A-4G; Ex. 1005, IDTD, 4-5, Fig. 1, Shweky, 7-9, Fig. 4. Nixon’s Figure 3 is a flowchart illustrating a “process 300 for manufacturing image sensors 100 ... with the image sensor 100 at each stage of the process being shown in FIGS. 4A-4G.” Ex. 1004, Fig. 3, 2:22-26; Ex. 1005, Shweky, 7-9, Fig. 4. Nixon’s Figure 2 illustrates the resulting packaged BSI image sensor 100 that corresponds to the claimed “backside illuminated image sensors”:

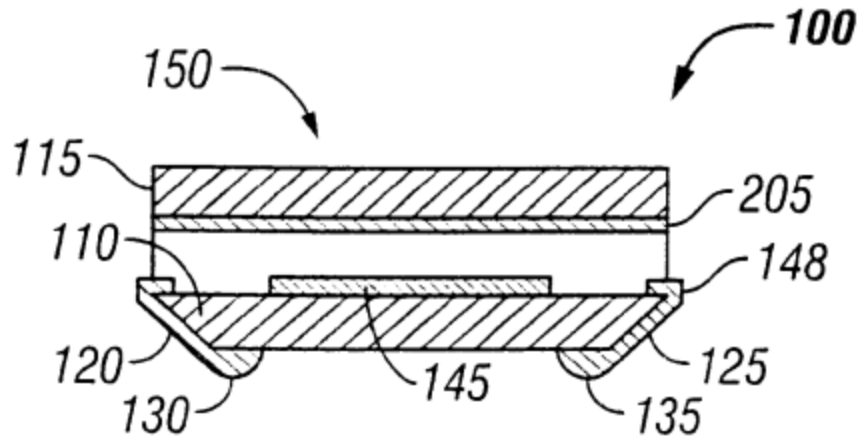


FIG. 2

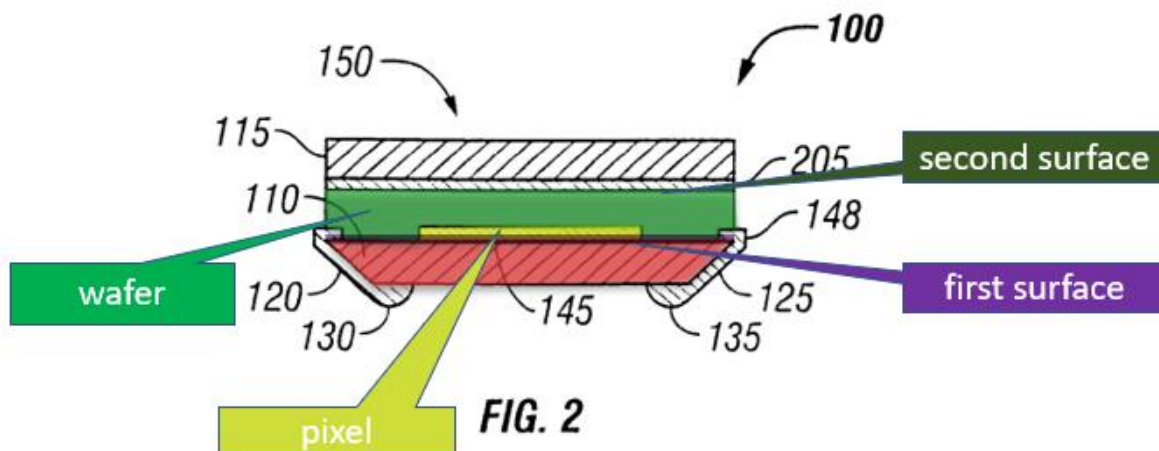
Ex. 1004, Fig. 2; Ex. 1005, IDTD, Fig. 2.

[1a] producing a plurality of image sensor circuits on a wafer having first and second surfaces each of the image sensor circuits being formed on the first surface and including a matrix of light-sensitive pixel regions extending into the wafer from the first surface;

84. I am of the opinion that Nixon discloses or renders obvious this claim element.

85. Nixon discloses a silicon wafer 405 that corresponds to the claimed “wafer.” Ex. 1004, 2:22-35; Ex. 1005, IDTD, 4-5, Shweky, 8, Fig. 4. Specifically, Nixon’s Figure 4A shows process 300 starts with silicon wafer 405 that has a frontside (active) surface and a backside surface (*i.e., a wafer having first and second surfaces*). Ex. 1004, 2:26-31; 41-42; Ex. 1005, IDTD, Fig. 2, Shweky, 8, Figs. 3, 4. Nixon also discloses that the CMOS image sensor described in Nixon is “achieved using wafer level processing.” Ex. 1004, Abstract, 1:65-2:1; Ex. 1005,

IDTD, 4-5, Shweky, 8, Fig. 4. Silicon wafer 405 is prefabricated with pixels on its frontside surface (*i.e.*, **producing image sensor circuits on a wafer; each of the image sensor circuits being formed the first surface**) because it is later diced to form individual silicon substrates 105, each with pixels 145 “positioned at the top surfaces 148 of the silicon substrate 105.” Ex. 1004, 2:1-10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Figs. 3, 4; *see supra*, §§V.A, D. Pixels 145 are **a matrix of light-sensitive pixel regions**, and Nixon’s Figure 2 illustrates **pixels 145** extending into **silicon substrate 105** from **top surface 148** (*i.e.*, **a matrix of light-sensitive pixel regions extending into the wafer from the first surface**):



Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2²; *see supra*, §§V.A, D

² Nixon’s Figures 4A to 4G “illustrate[] the image sensor in various stages of formation.” Ex. 1004, 1:61-62. Nixon’s Figures 2, described as “an image sensor

86. To the extent the Patent Owner argues that Nixon does not expressly disclose this claim element, a POSITA would readily understand that the teachings in Nixon are applied to wafer-level processing of an image sensor where multiple image sensor circuits are manufactured at the same time to achieve cost efficiencies, among other things, as opposed to individually manufacturing each image sensor circuit. *See supra*, §§V.A, D. A POSITA would also readily understand that Nixon’s pixels 145 are in the wafer, as it was well-known at the time of invention that the active regions of pixels extend into the substrate. Ex. 1046, 1:31-45, 5:4-17 (disclosing conventional CMOS APS cell with n+ photodiode 140 and other active regions in substrate 110), Fig. 9B; *see supra*, §§V.A, D. Accordingly, Nixon at a minimum renders this claim limitation obvious.

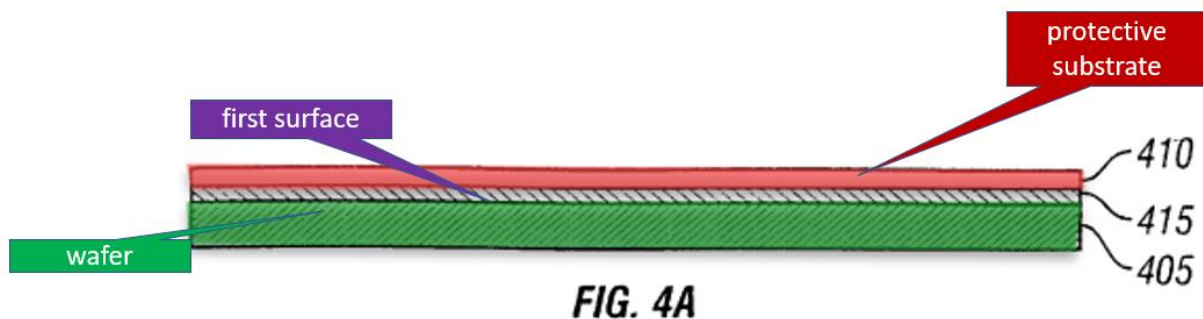
[1b] securing the wafer onto a protective substrate such that the first surface faces the protective substrate;
--

87. I am of the opinion that Nixon discloses this claim element.

88. Nixon’s first glass plate 410 corresponds to the claimed “protective substrate” and the active side of Nixon’s silicon wafer 405 corresponds to the

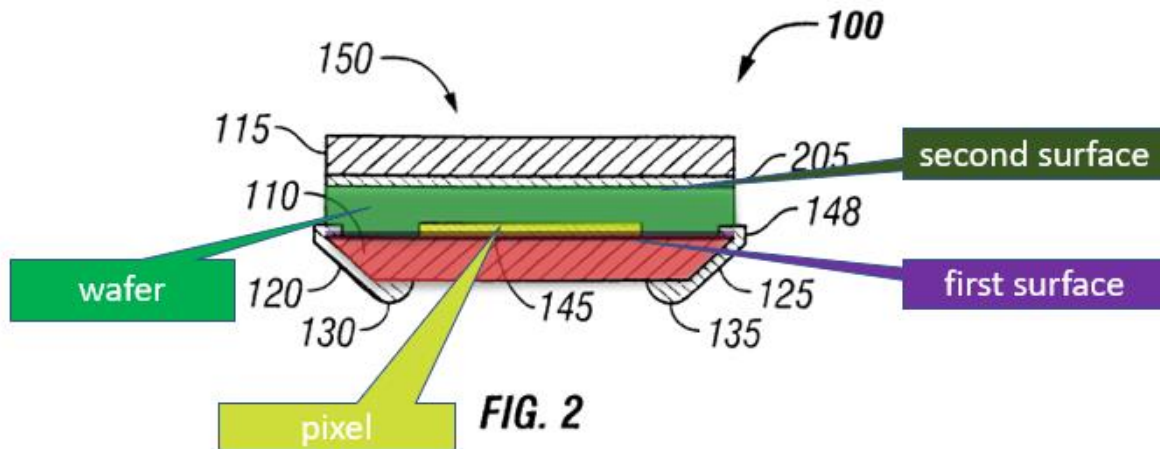
including a color filter array according to the present invention,” illustrates an embodiment created using the process depicted in Figures 4A to 4G. *Id.*, 1:56-57.

claimed “first surface.” Ex. 1004, 2:22-36; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Specifically, Nixon’s Figure 4A illustrates a process step where “**silicon wafer 405** is bonded onto ... **first glass plate 410**” (*i.e., securing the wafer onto a protective substrate*) “while the active surface of the **silicon wafer [405]** is facing up into the encapsulate” (*i.e., such that the first surface faces the protective substrate*):



Ex. 1004, Fig. 4A (annotated), 2:26-31; Ex. 1005, Shweky, 8, Fig. 4.

89. Nixon also discloses the resulting packaged CMOS image sensor 100 has “[a]n epoxy adhesive layer ... [that] attaches” the silicon substrate 105 to the protective plate 110 (*i.e., securing the wafer onto a protective substrate*). Ex. 1004, 2:1-6; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Nixon’s Figure 2 shows **top (frontside) surface 148** of **silicon substrate 105** facing **protective plate 110** (*i.e., the first surface faces the protective substrate*):



Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2.

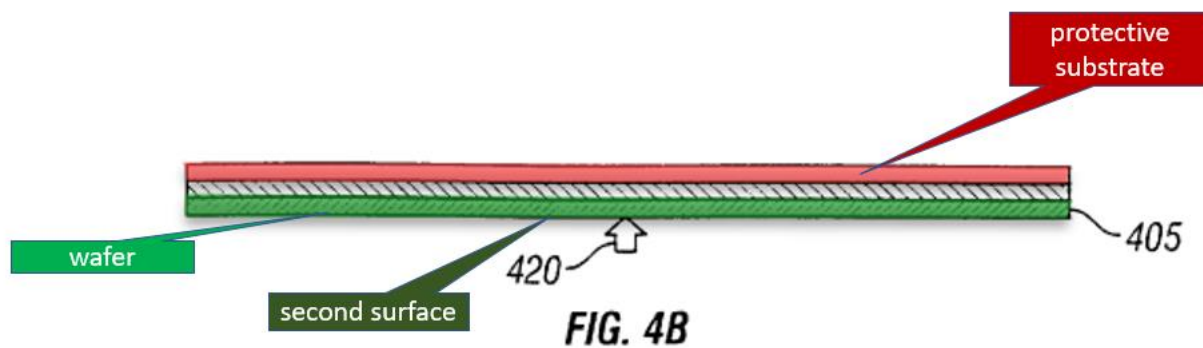
[1c] removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface;

90. I am of the opinion that Nixon discloses this claim element.

91. Nixon discloses “grinding the silicon wafer from the opposite surface of the silicon wafer” (i.e., **removing material from the second surface of the wafer**) to a “predetermined thickness” that “allows for the light sensitive area of the die 430 to be illuminated from . . . the back side” (i.e., **until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface**).³ Ex. 1004, 2:36-41, 3:7-17, 1:65-2:10; Ex. 1005, Shweky, 8, Fig.

³ The '965 patent describes that “effectively exposing the light-sensitive pixel diffusions regions of the image sensor circuit through the backside surface” is achieved when the semiconductor substrate is thinned “until [it] is transparent to

4. Nixon's Figure 4B illustrates a process step of grinding (indicated by arrow 420) the backside surface of **silicon wafer 405** (i.e., *removing material from the second surface of the wafer*):



Ex. 1004, Fig. 4B (annotated); Ex. 1005, Shweky, 8, Fig. 4.

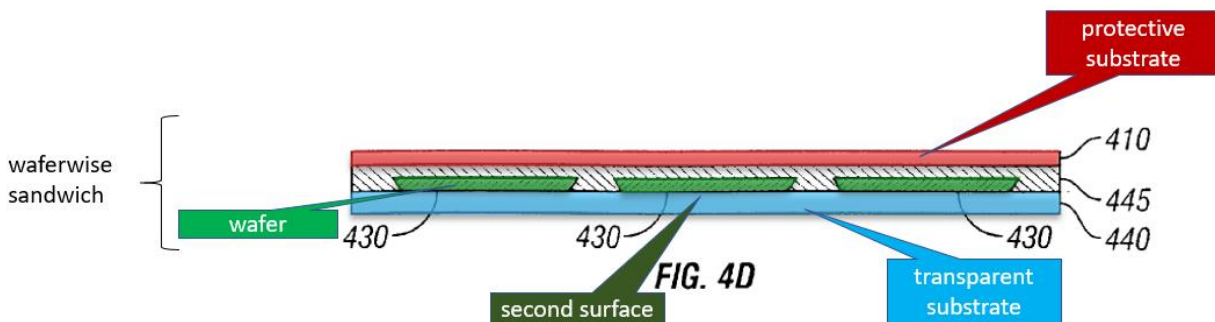
[1d] securing a transparent substrate onto the second surface of the wafer, thereby producing a waferwise sandwich; and

92. I am of the opinion that Nixon discloses this claim element.

93. Nixon's protective plate 115 and second glass plate 440 correspond to the claimed "transparent substrate." Ex. 1004, 2:1-6, Abstract, Figs. 4A-4G; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Indeed, Nixon discloses fabricating and packaging a CMOS image sensor can be illuminated from the back side, where the "die is covered with an optically transparent material." Ex. 1004, 1:37-47; Ex.

visible light." Ex. 1001, 4:61-5:4. Nixon discloses what is described in the '965 patent.

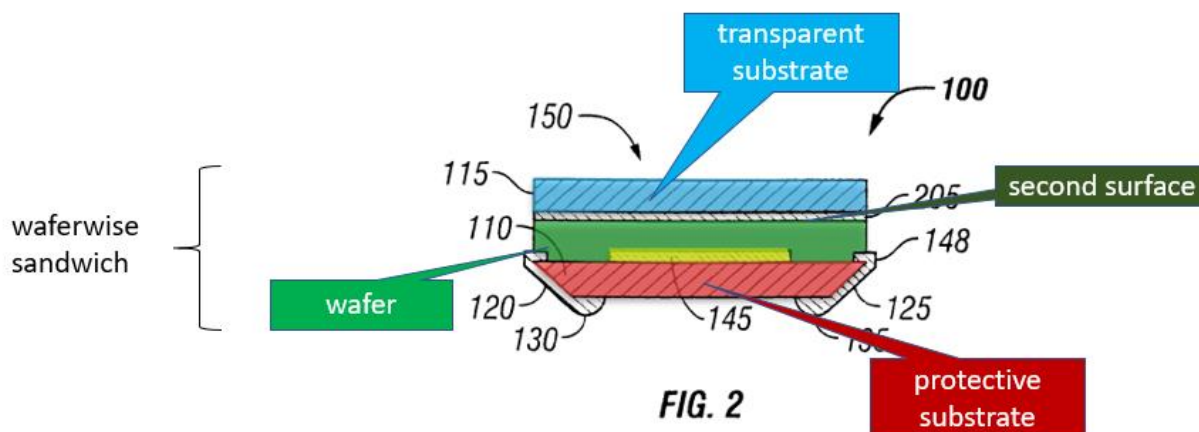
1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Fig. 4 (expressly disclosing “[a]ttach[ing] a second glass plate from the back side”). Protective plate 115 is the resulting die-sized section of Nixon’s second glass plate 440 (*i.e.*, **the transparent substrate is glass**), after it is diced to separate the dies. Ex. 1004, 1:37-47, 2:49-57; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-8, Fig. 4. Specifically, Nixon’s Figure 4D illustrates a process step of bonding “**second glass plate 440** ... onto the backside of **silicon dies**” 430 using epoxy adhesive (not depicted), thereby forming a waferwise sandwich with **first glass plate 410** (*i.e.*, **securing a transparent substrate onto the second surface of the wafer, thereby producing a waferwise sandwich**):



Id., Fig. 4D (annotated), 2:49-52; Ex. 1005, Shweky, 8, Fig. 4.

94. Relatedly, Nixon discloses “[a]n epoxy adhesive layer ... attaches the protective plates 110, 115 to the silicon substrate 105” (*i.e.*, **securing a transparent substrate onto the second surface of the wafer**) and “a thin silicon substrate 105 ... is sandwiched between two thin protective plates 110, 115 on the top and bottom sides” (*i.e.*, **thereby producing a waferwise sandwich**). *Id.*, 1:65-2:10; Ex.

1005, IDTD, 4-5, Fig. 2, Shweky, 8, Fig. 4. Nixon's Figure 2 illustrates **protective plate 110** and **protective plate 115** sandwiching **silicon substrate 105**:

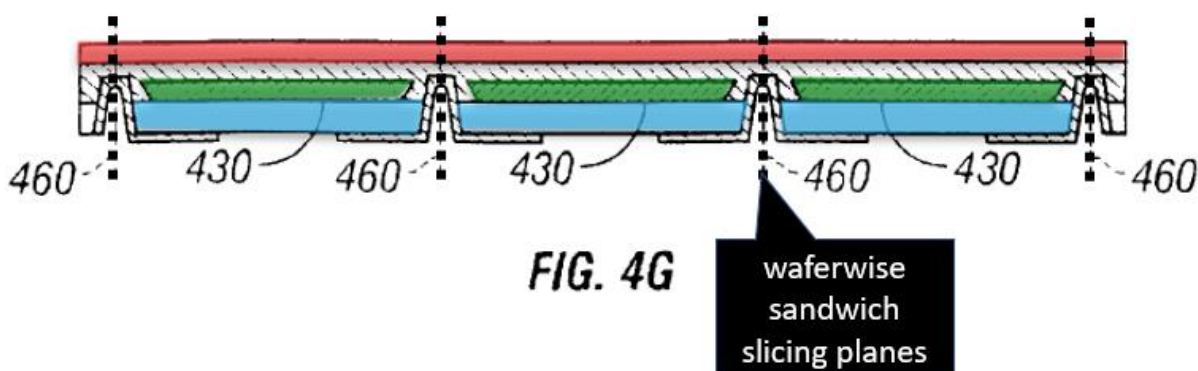


Id., Fig. 2; Ex. 1005, IDTD, Fig. 2.

[1e] slicing the waferwise sandwich, thereby defining a plurality of backside illuminated image sensors.

95. I am of the opinion that Nixon discloses this claim element.

96. Nixon's Figure 4G illustrates a process step of dicing the wafer along score lines 460 between **dies 430** (*i.e.*, *slicing the waferwise sandwich*):



Id., Fig. 4G (annotated); Ex. 1005, Shweky, 8, Fig. 4. Specifically, Nixon discloses “[t]he wafer is diced along score lines 460 within the notches 450 between the dies 430,” producing “multiple individual packaged dies 430” (*i.e.*, ***defining a plurality of backside illuminated image sensors***). Ex. 1004, 3:1-6; Ex. 1005, Shweky, 8, Fig. 4.

2. Claim 2

[2pre] The method according to claim 1, wherein the step of securing the protective substrate onto the first surface comprises

97. I am of the opinion that Nixon discloses claim 2pre for the same reasons as claim 1b above.

[2a] depositing an adhesive onto the protective substrate, and then
--

98. I am of the opinion that Nixon discloses or renders obvious this claim element.

99. Nixon’s protective plate 110 and first glass plate 410 correspond to the claimed “protective substrate” and Nixon’s epoxy adhesive layer corresponds to the claimed “adhesive.” *See supra*, 1b; Ex. 1004, 2:3-6; Ex. 1005, Shweky, 7-8, Fig. 4. Nixon discloses that “[a]n epoxy adhesive layer ... attaches the protective plates 110, 115 to the silicon substrate 105.” Ex. 1004, 1:65-2:10, Fig. 2; Ex. 1005, Shweky, 7-8, Fig. 4. Nixon further discloses that “a silicon wafer 405 is bonded onto a thin protective layer, or first glass plate 410.” Ex. 1004, 2:26-28;

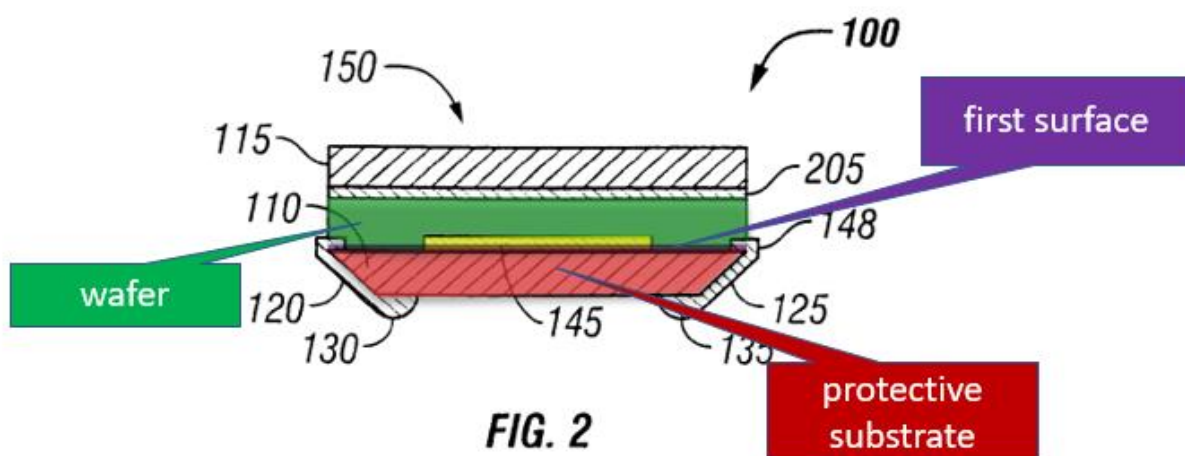
Ex. 1005, Shweky, 8, Fig. 4. It was common practice to use a supporting structure or plate, such as Nixon's protective plate 110 or first glass plate 410, prior to thinning the silicon substrate 105. *See supra*, §V.B. It was conventional to apply an adhesive to such supporting structure or plate first before attaching the wafer (*i.e., depositing an adhesive onto the protective substrate*). *Id.* A POSITA would know how to deposit or apply such epoxy adhesive in Nixon in the same manner as described for the adhesive in the '965 patent. Ex. 1004, 1:65-2:10; Ex. 1005, Shweky, 8, Fig. 4; Ex. 1001, 6:35-40, Fig. 4(A).

100. A POSITA would also readily recognize that when bonding two surfaces together, adhesive must first be placed on at least one of those surfaces. In the context of bonding the wafer to the protective substrate, there are only three choices: the adhesive could be placed on the wafer, the protective substrate, or both. *See supra*, §V.B. Whichever of the three choices is used during the manufacturing process is merely a design choice. *Id.* Therefore, it would have been obvious to a POSITA to apply the adhesive on the protective substrate (*i.e., depositing an adhesive onto the protective substrate*). *See supra*, §V.B. Accordingly, Nixon at a minimum renders this limitation obvious.

[2b] placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive.

101. I am of the opinion that Nixon discloses this claim element.

102. Because the epoxy adhesive is applied onto the first glass plate 410, the silicon wafer 405 would be placed onto the first glass plate 410 where the epoxy adhesive is deposited to secure the first glass plate 410 onto the silicon wafer 405 (*i.e.*, **placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive**). See *supra*, claim 2a, §V.B. As Nixon further discloses that the “first glass plate 410 is bonded while the active surface of the silicon wafer is facing up into the encapsulate,” the active surface of the wafer would contact the deposited adhesive on the first glass plate 410 (*i.e.*, **the first surface contacts the deposited adhesive**). Ex. 1004, 2:29-31; Ex. 1005, IDTD, Fig. 2, Shweky, Fig. 4. Nixon’s Figure 2 illustrates that epoxy adhesive layer (not depicted) attaches the **protective plate 110** to the **silicon substrate 105** such that the **top (frontside) surface 148** contacts the epoxy adhesive layer:



Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2.

3. Claim 7

[7pre]. The method according to claim 1, wherein the step of securing a transparent substrate onto the second surface comprises

103. I am of the opinion that Nixon discloses claim 7pre for the same reasons as claim 1d above.

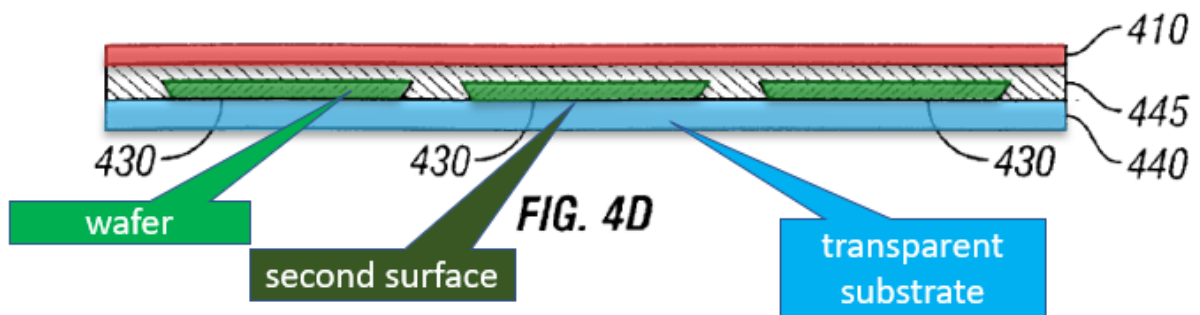
104. Nixon's protective plate 115 and second glass plate 440 correspond to the claimed "transparent substrate." *See supra*, claim 1d.

[7a] depositing an adhesive onto the second surface, and then

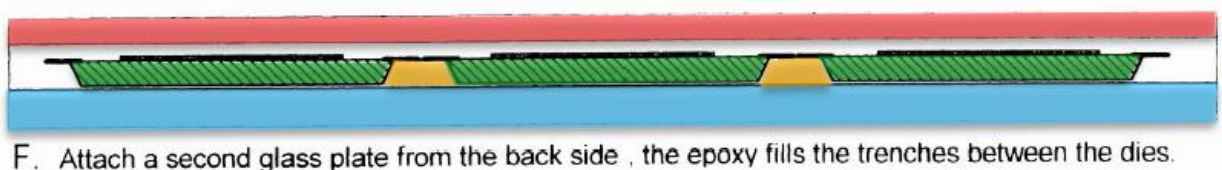
105. I am of the opinion that Nixon discloses or renders obvious this claim element.

106. Nixon's epoxy adhesive layer corresponds to the claimed "adhesive" and the backside of Nixon's silicon wafer 405 corresponds to the claimed "second surface." Ex. 1004, 1:65-2:10, 2:49-57, Figs. 2, 4D; Ex. 1005, Shweky, 8, Fig. 4. Nixon discloses that "[e]poxy may be used to bond the second glass plate 440 to the silicon dies 430" and may be used to "fill the grooves 435 between the dies 430." Ex. 1004, 2:49-57; Fig. 4D; Ex. 1005, IDTD, Fig. 2, Shweky, 8, Fig. 4. For the epoxy to both fill the grooves 435 and bond second glass plate 440 to the dies 430, the epoxy would have to be applied first to the wafer structure to fill the grooves 435 and cover the backside of the dies 430. This way, "when combined with the first glass plate 410 creates a complete protective enclosure for each die

430.” Ex. 1004, 2:52-55, Fig. 4D; Ex. 1005, IDTD, Fig. 2, Shweky, 8, Fig. 4. If the epoxy is first applied to second glass plate 440 and then placed on the wafer structure, there may not be enough epoxy to fill the grooves 435 between dies 430. Alternatively, epoxy could be applied to both the wafer structure and glass plate 440 before they are bonded to ensure the epoxy fill the grooves 435 and cover dies 430 for the best bond and complete enclosure. Nixon’s Figure 4D illustrates **second glass plate 440** (*i.e.*, **transparent substrate**) is bonded using an adhesive (not depicted) (*i.e.*, **adhesive**) to the backside surface of **silicon dies 430**:



Ex. 1004, Fig. 4D (annotated), 2:49-57; Ex. 1005, Shweky, 8, Fig. 4. Shweky discloses that the “epoxy fills the trenches” on the backside of the dies (*i.e.*, **depositing an adhesive onto the second surface**), which is illustrated in Shweky’s Figure 4:



Ex. 1007, Fig. 4. A POSITA would know how to deposit or apply such epoxy adhesive layer in Nixon in the same manner as described for the adhesive in the '965 patent. Ex. 1004, 2:49-57; Ex. 1005, Shweky, 8, Fig. 4; Ex. 1001, 7:57-8:3, Fig. 4(E).

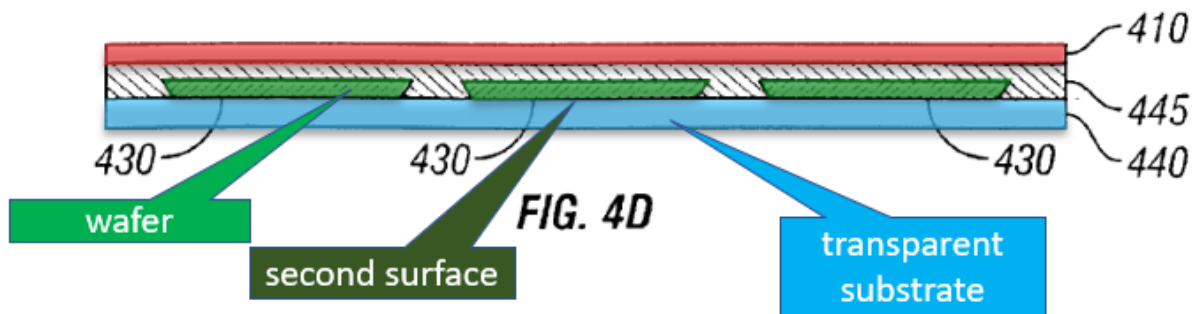
107. A POSITA would also readily recognize that when bonding two surfaces together, adhesive must first be placed on at least one of those surfaces. In the context of bonding the wafer to the transparent substrate, there are only three choices: the adhesive could be placed on the wafer, on the transparent substrate, or both. Whichever of the three choices is used during the manufacturing process is merely a design choice. Therefore, it would have been obvious to a POSITA to apply the adhesive on the backside of the wafer (*i.e.*, ***depositing an adhesive onto the second surface***). Accordingly, Nixon at a minimum renders this limitation obvious.

[7b] placing the transparent substrate onto the deposited adhesive

108. I am of the opinion that Nixon discloses this claim element.

109. Because the epoxy adhesive is applied onto the backside of silicon wafer 405, the second glass plate 440 would be placed onto the backside of the silicon wafer 405 where the epoxy adhesive is deposited to secure the second glass plate 440 onto the backside of the silicon wafer 405 (*i.e.*, ***placing the transparent substrate onto the deposited adhesive***). *See supra*, claim 7a. Nixon further

discloses “attach[ing]” or “bond[ing]” protective plate 115 or second glass plate 440 onto the epoxy adhesive layer (*i.e.*, **placing the transparent substrate onto the deposited adhesive**). Ex. 1004, 2:3-6, 2:49-57, Fig. 2; Ex. 1005, Shweky, 7-8, Fig. 4. Nixon’s Figure 4D illustrates placing **second glass plate 440** onto epoxy adhesive (not depicted):



Ex. 1004, Fig. 4D (annotated); Ex. 1005, Shweky, 8, Fig. 4.

4. Claim 8

[8pre]. The method according to claim 7,

110. I am of the opinion that Nixon discloses claim 8pre for the same reasons as claim 7 above.

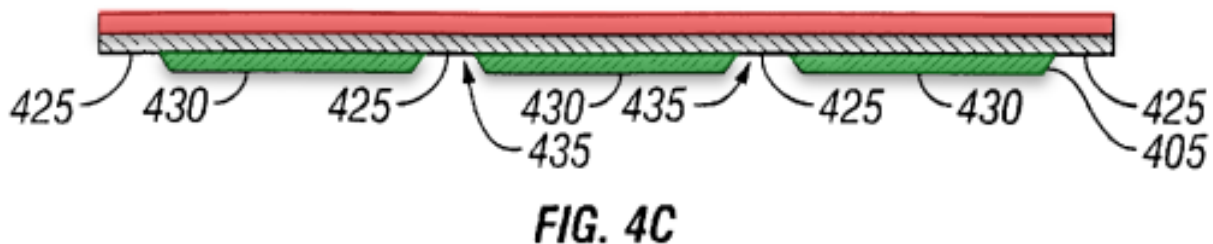
[8a] wherein the step of removing material includes separating each of the plurality of image sensor circuits; and

111. I am of the opinion that Nixon discloses this claim element.

112. Nixon discloses that “the silicon wafer 405 is ... etched along the dice lines 425” such that “the wafer is separated into individual dies 430” (*i.e.*, **wherein the step of removing material includes separating each of the plurality of image**

sensor circuits). Ex. 1004, 2:43-58; Fig. 3, Fig. 4C; Ex. 1005, Shweky, 8, Fig. 4.

Nixon's Figure 4C illustrates etching along dice lines 425 to separate **individual dies 430**:



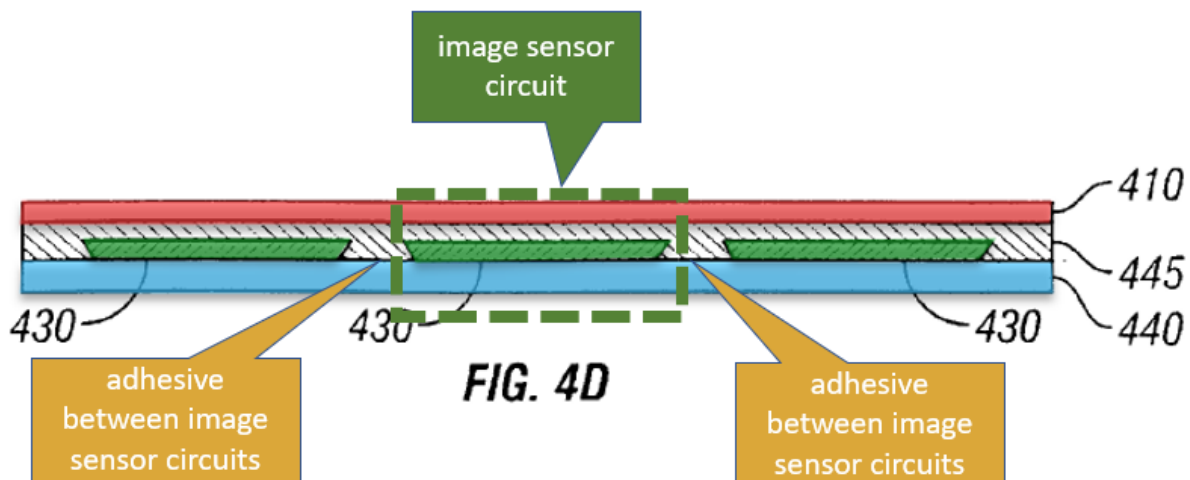
Ex. 1004, Fig. 4C (annotated); Ex. 1005, Shweky, 8, Fig. 4.

[8b] wherein the step of depositing the adhesive onto the second surface further comprises depositing adhesive into interstices located between the plurality of image sensor circuits, thereby protecting the image sensor circuits.

113. I am of the opinion that Nixon discloses this claim element.

114. Nixon discloses that “epoxy may fill the grooves 435 between the dies 430 (*i.e., depositing adhesive into interstices located between the plurality of image sensor circuit*). Ex. 1004, 2:49-57, Fig. 4D; Ex. 1005, Shweky, 8, Fig. 4. Shweky also discloses that “epoxy fills the trenches between the dies.” Ex. 1047, Fig. 4. “The image sensor packages assembled according to the present invention ... offer[] a complete mechanical enclosure for the die and does not leave any silicon exposed to the outside. This provides both mechanical and environmental protection” (*i.e., thereby protecting the image sensor circuits*). Ex. 1004, 3:7-17; Ex. 1005, Shweky, 7-8. Nixon's Figure 4D illustrates epoxy

adhesive (not depicted) that is used to fill in grooves 435 (not labeled) between the individual dies 430:



Ex. 1004, Fig. 4D (annotated); Ex. 1005, Shweky, Fig. 4.

5. Claim 9

[9pre] The method according to claim 1, further comprising the step of

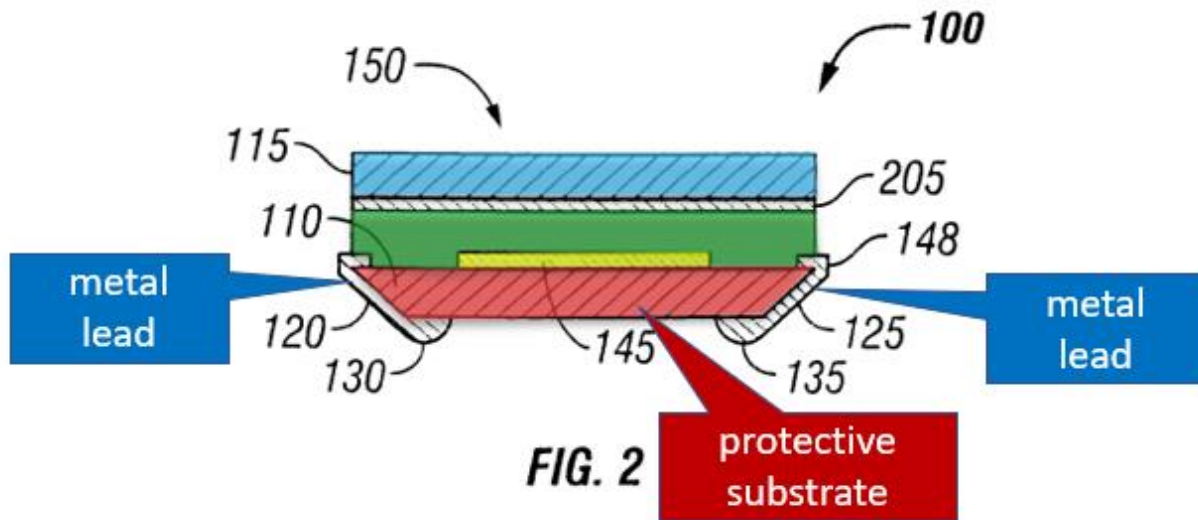
115. I am of the opinion that Nixon discloses 9pre for the same reasons as claim 1 above.

[9a] forming metal leads on the protective substrate after the step of securing the transparent substrate,

116. I am of the opinion that Nixon discloses or renders obvious this claim element.

117. Nixon's electrical leads 120, 125 correspond to the claimed "metal leads." Ex. 1004, 2:6-9, 2:20-22; Ex. 1005, IDTD, 4-5, Fig. 2. Nixon's Figure 2 illustrates electrical leads 120, 125 formed on protective plate 110 after the

protective plate 115 is secured to the backside of the **silicon die** (i.e., *forming metal leads on the protective substrate after the step of securing the transparent substrate*):



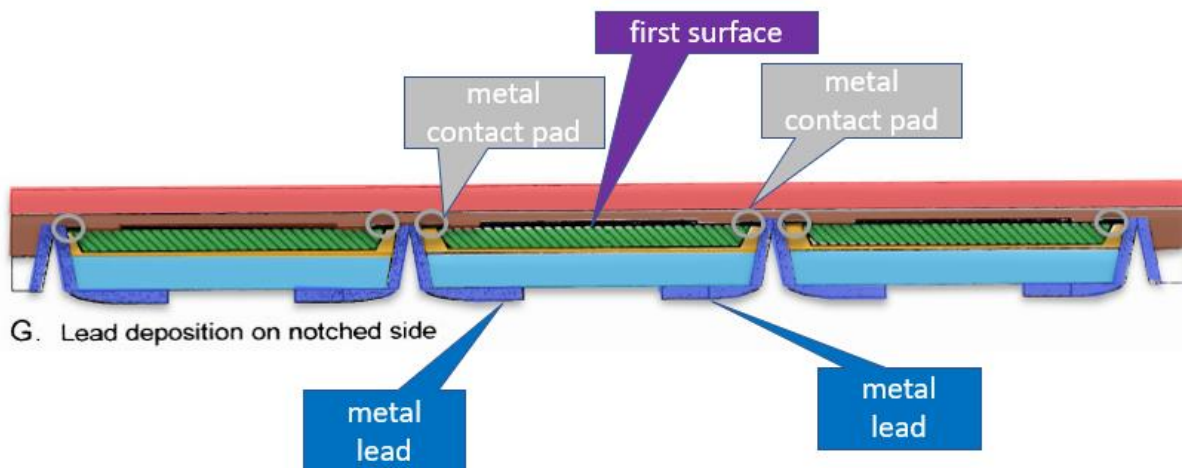
Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2.

[9b] wherein the metal leads are connected to metal contact pads located on the first surface of the wafer.

118. I am of the opinion that Nixon discloses this claim element.

119. Nixon discloses that deep notches 450 are drawn between dies 430 from the backside of the waferwise sandwich such that “the cross sections of each of the pads are exposed” and then “[t]he metal layer is patterned by a lithography process into individual leads 455 that contact the pads and form a solder pad on the upper surface of each die package.” *See supra*, claim 9a; Ex. 1004, 2:58-67; Ex. 1005, Shweky, 8, Fig. 4. The ’144 Nixon Provisional’s Figure 4 shows the

individual metal leads are connected to **metal contact pads** that are on the top (frontside) surface of the silicon die (*i.e., wherein the metal leads are connected to metal contact pads*):



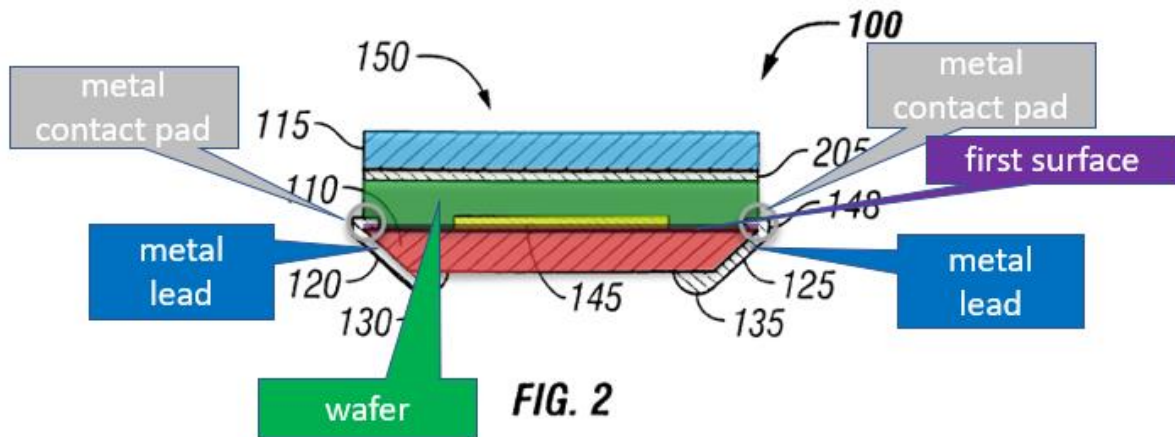
Ex. 1047, Fig. 4 (annotated).

120. A POSITA would readily understand that the '144 Nixon Provisional's Figure 4 corresponds to Nixon's Figure 4F and discloses the manufacturing process that results in the image sensor 100 of Nixon's Figure 1, which is simply one embodiment of Nixon. Ex. 1004, 2:58-67, Figs. 1, 4; Ex. 1005, Shweky, 8, Fig. 4.

121. A POSITA would also readily recognize the image sensor 100 of Nixon's Figure 2 is another embodiment of Nixon, where the notches are drawn from the top surface 148. Ex. 1004, 2:58-61; Ex. 1005, Shweky, 8, Fig. 4.

Nixon's Figure 2 illustrates that the **metal contact pads** located next to the **top (frontside) surface 148** of **silicon substrate 105** are connected to the **electrical**

leads 120, 125 (i.e., the metal leads are connected to metal contact pads located on the first surface of the wafer):



Ex. 1004, Fig. 2 (annotated); Ex. 1005, IDTD, Fig. 2.

XI. GROUND 2: NIXON IN VIEW OF ASSADI RENDERS OBVIOUS CLAIM 10

122. I am of the opinion that Nixon in view of Assadi renders obvious claim 10 of the '965 patent.

1. Reasons to Combine Nixon with Assadi

123. A POSITA would have been motivated to modify Nixon's manufacturing process for a BSI CMOS image sensor to include a passivation layer to ensure that the frontside (active) surface of the CMOS image sensor where the microelectronics are located are protected from abrasion, moisture, or contaminants. Nixon and Assadi both teach CMOS image sensors. Ex. 1004, 2:8-10; Ex. 1005, IDTD, 4-5, Fig. 2, Shweky, 7-9, Fig. 4; Ex. 1044, 4:15-25. By the

priority date of the '965 patent, it was very well-known and highly conventional that passivation layers should be included in CMOS image sensors to protect from, among other things, abrasion, moisture, and contaminants. *See supra*, §V.C. Assadi provides an example of a passivation layer that provides these well-known benefits. Indeed, Assadi explains that passivation layers should be included “over[] the entirety of sensor 176, including sensor area 210 and non-sensor area (logic area 220 and bond pad area 240)” to provide “resistance to environmental contaminants, particularly moisture.” Ex. 1044, 4:26-44, 9:31-32. Including Assadi’s passivation layer in Nixon’s manufacturing process for a BSI CMOS image sensor would have the obvious added benefit of protecting the microelectronics necessary to convert the photons collected into electrical signals. *See supra*, §§V.A, C-D.

124. In addition to being motivated to do so, a POSITA would have understood that modifying Nixon’s manufacturing process to include a passivation layer, as taught by Assadi’s, would have been a simple matter of applying well understood semiconductor fabrication techniques using standard semiconductor processing tools. *See supra*, §§V.C-D. A POSITA would simply add a step to deposit passivation layer before bonding the glass to the active side of the wafer. *See supra*, §§V.C-D. contemplates additional layers between active side of wafer and the protective glass substrate. Ex. 1004, Fig 4A (disclosing filter layer 415).

Indeed, Assadi's passivation layer in a CMOS device is readily applicable to Nixon's manufacturing process for a BSI CMOS image sensor. *See supra*, §§V.C-D. A POSITA could have modified Nixon's manufacturing process to include a passivation layer such as taught in Assadi with a reasonable expectation of success. *Id.* Such a modification to Nixon's manufacturing process would have merely required adding additional conventional, well-known, manufacturing process steps. *Id.*

2. Claim 10

[10pre]. The method according to claim 1, wherein the step of securing the wafer onto a protective substrate further comprises:
--

125. I am of the opinion that Nixon discloses claim 10pre for the same reasons as claim 1b above.

[10a] forming a passivation layer on the first surface of the wafer;

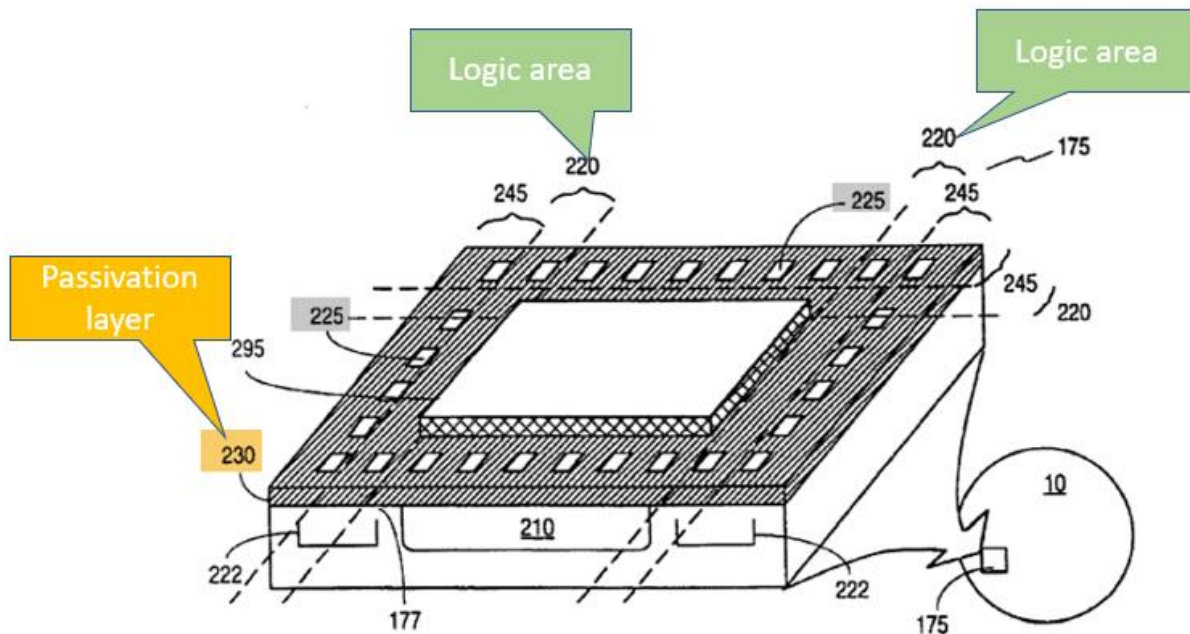
126. I am of the opinion that Nixon combined with Assadi renders obvious this claim element.

127. It was very well-known and highly conventional that passivation layers should be included in CMOS image sensors to protect from, among other things, abrasion, moisture, and contaminants. *See supra*, §V.C. Therefore, a POSITA would readily understand that Nixon's manufacturing process includes a step of "forming a passivation layer on the first surface of the wafer." *See supra*,

§§V.C, D. Nixon discloses that the “[p]ixels 145 are positioned at the top surface 148 of the silicon substrate 105” (*i.e., first surface of the wafer*). Ex. 1004, 2:8-10; Ex. 1005, IDTD, Fig. 2. Top (frontside) surface 148 is also the active surface of the silicon wafer 405 given that the microelectronics are built into the top (frontside) surface 148. *See supra*, §§V.A, C.

128. It would have been conventional to form a passivation layer on top (frontside) 148 surface to protect the microelectronics. *Id.*; *see also* Ex. 1045, 5:26-34 (stating that the passivation coating “acts as a scratch coat and etch mask”); Ex. 1009, ¶¶97, 98, 101, Fig. 4 (disclosing a dielectric film 200 made of “SiN or SiO₂” that “protects the light-receiving elements”).

129. Assadi teaches a conventional mechanism to protect the microelectronics components on the active surface. Assadi’s passivation layer 230, which is made of either silicon nitride (Si₃N₄) or silicon oxynitride (Si_xO_yN_z), corresponds to the claimed “passivation layer.” Ex. 1044, 4:15-45. Assadi discloses an image sensor 175 with sensor area 210 representing “the photosensing region or area” and logic area 220 that “operates the individual pixels and drives signals from the pixels off sensor 175.” *Id.*, 4:15-26. Assadi further discloses a passivation layer 230 “overlies the entirety of sensor 175, including ... logic area 220” (*i.e., forming a passivation layer on the first surface of the wafer*):



Id., 4:15-45, Fig. 3b (annotated).

130. While Assadi discloses a FSI image sensor, a POSITA would also readily understand that the teachings in Assadi related to passivation layer 230 are equally applicable to BSI image sensors, which have the same concerns regarding abrasion, moisture, and contaminants. *See supra*, §§V.A, C; *see also* Ex. 1045, 5:26-34; Ex. 1044, 4:35-45. Use of a passivation layer in a BSI CMOS image sensor would have been a routine design choice that could easily be implemented by a POSITA. *See supra*, §§V.A, C; *see also* Ex. 1045, Abstract, 1:18-40, 5:26-34. Thus, it would have been obvious for a POSITA to include Assadi's passivation layer 230 to the top (frontside) surface 148 of Nixon's BSI CMOS image sensor

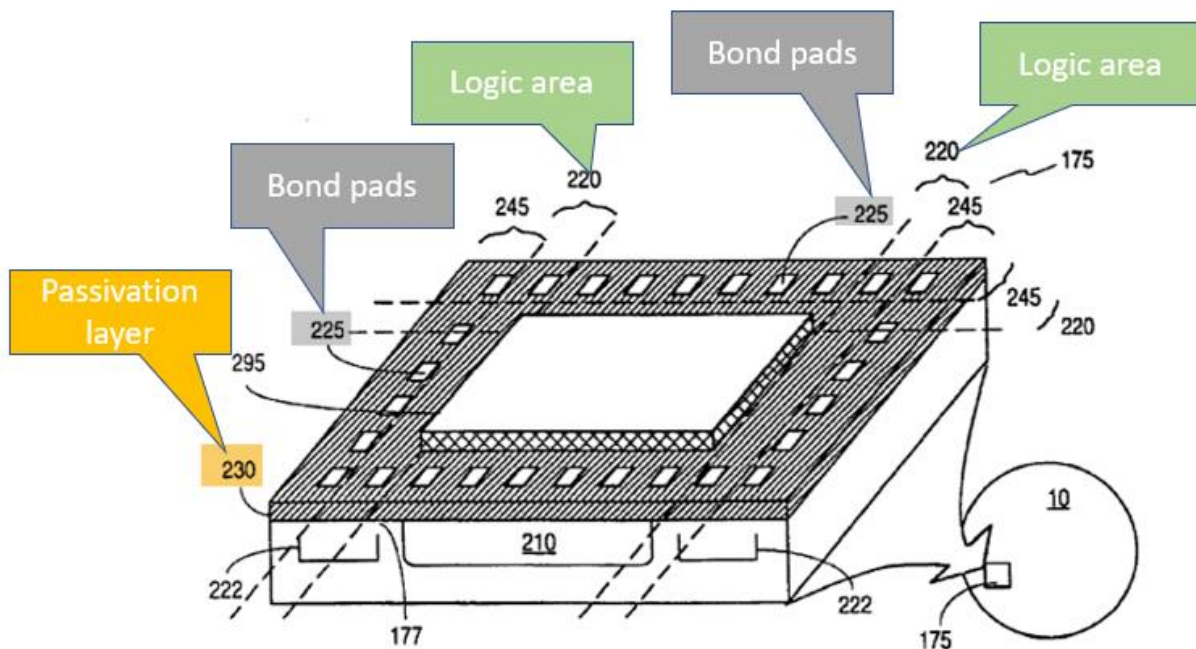
where the pixels 145 are located to protect them from abrasion, moisture, and contaminants. *See supra*, §§V.A, C-D.

[10b] forming openings in the passivation layer; and

131. I am of the opinion that Nixon combined with Assadi renders obvious claim element.

132. Nixon discloses exposing the pads that are next to the top (frontside) surface 148 of the wafer using notching so that the electrical leads 120, 125 may be connected to those pads to transmit electrical signals to the outside world. *See supra*, claim 9b. A POSITA would have been motivated to modify Nixon's BSI CMOS image sensor to include Assadi's passivation layer 230 to protect the pixels 145 on top (frontside) surface 148 of the silicon die. *See supra*, claim 10a.

133. Moreover, Assadi discloses a **passivation layer 230** on the frontside (active) surface of image sensor 175, where **openings** for **bond pads 225**, which are "arranged on the ... top surface of sensor 175" and "are electrically linked or coupled to device circuitry 222," are formed so that the "logic circuitry 220 that operates the individual pixels [can] drive[] signals from the pixels off sensor 175" (*i.e., forming openings in the passivation layer*), as illustrated in Assadi's Figure 3b:



Ex. 1044, Fig. 3b (annotated), 4:15-45.

134. A POSITA would readily understand that openings in the passivation layer may be formed before a protective substrate is secured because of the need to connect the metal pads on the frontside (active) surface of the substrate to the outside world to transmit the electrical signals converted from the collected photons. *See supra*, §§V.C, D; *see also* Ex. 1045, 5:26-37 (describing that bond pad contacts are opened through passivation coating 26 using “standard procedures” before “dicing and packaging operations”), Fig. 7; Ex. 1044, 4:26-45.

135. Moreover, a POSITA would understand that the passivation layer and the protective substrate may be formed from different materials. *See also* Ex. 1045, 5:27-34 (describing passivation coating 260 as serving as an etch mask, among other

things). As a result, the use of different etching solutions (and different masks and resists accordingly) is required to expose the contact pads on the first surface, therefore requiring that openings be formed on the passivation layer first prior to a protective substrate being secured to the passivation layer. *See supra*, §V.C. Accordingly, this limitation would have been obvious over Nixon in combination with Assadi. *See supra*, §V.C.

[10c] securing the protective substrate onto the passivation layer.

136. I am of the opinion that Nixon combined with Assadi renders obvious claim element.

137. As an initial matter, it would have been obvious to a POSITA to modify Nixon’s BSI CMOS image sensor to include Assadi’s passivation layer. *See supra*, claim 10a. The passivation layer is a conventional component that is deposited on the first surface of the semiconductor substrate to protect the microelectronics there from abrasion, moisture, or contaminants. *See supra*, §V.C; *see also* Ex. 1045, 5:26-37.

138. Nixon further discloses a protective plate 110 sandwiching silicon substrate 105 from the top to “create a complete protective enclosure for each die” (*i.e., securing the protective substrate*). Ex. 1004, 2:49-57; Ex. 1005, Shweky, 7-8. A POSITA would readily understand that Nixon’s protective plate 110 would be secured onto Assadi’s passivation layer, which overlies the entirety of the top

(frontside) surface of semiconductor substrate 105 (*i.e.*, ***securing the protective substrate onto the passivation layer***), to further protect the Nixon's BSI CMOS image sensor and provide additional support during the step of removal of material from the backside of the semiconductor substrate. *See supra*, §§V.B-D.

XII. GROUND 3: BADIHI RENDERS OBVIOUS CLAIM 1, 2, 7, 8, AND 9

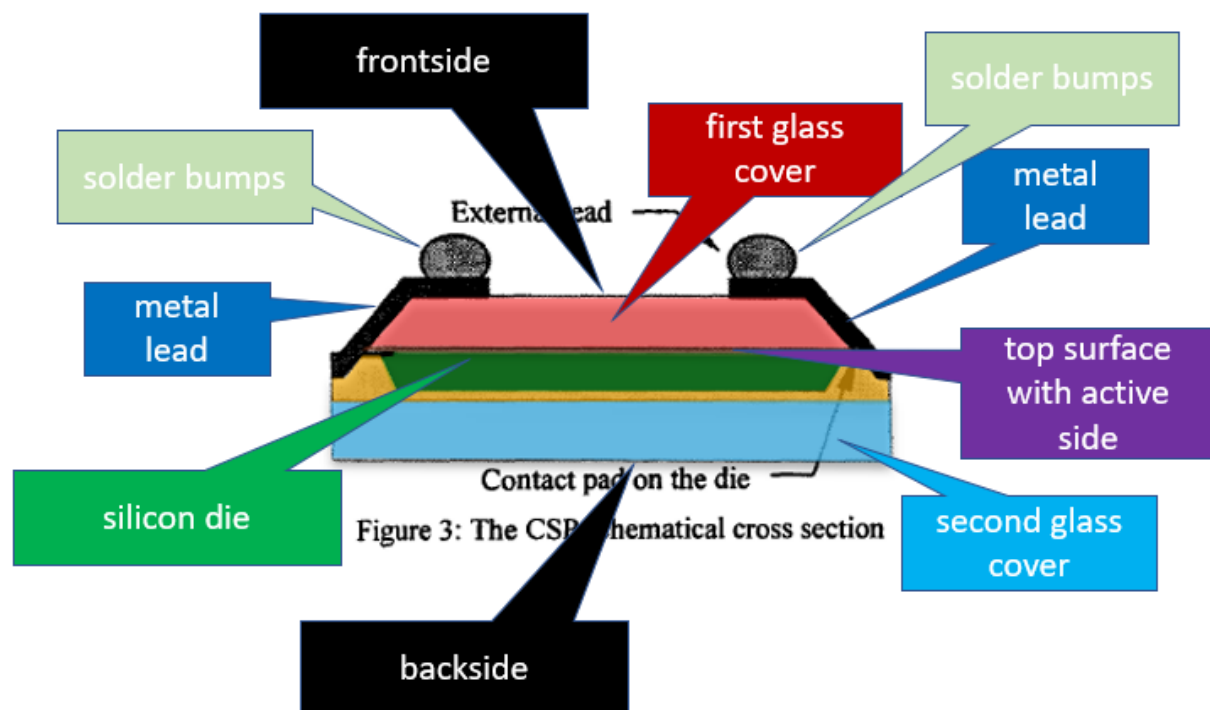
139. I am of the opinion that Badihi renders obvious claims 1, 2, 7, 8, and 9 of the '965 patent.

1. Claim 1

[1pre] A method of producing backside illuminated image sensors comprising the steps of:

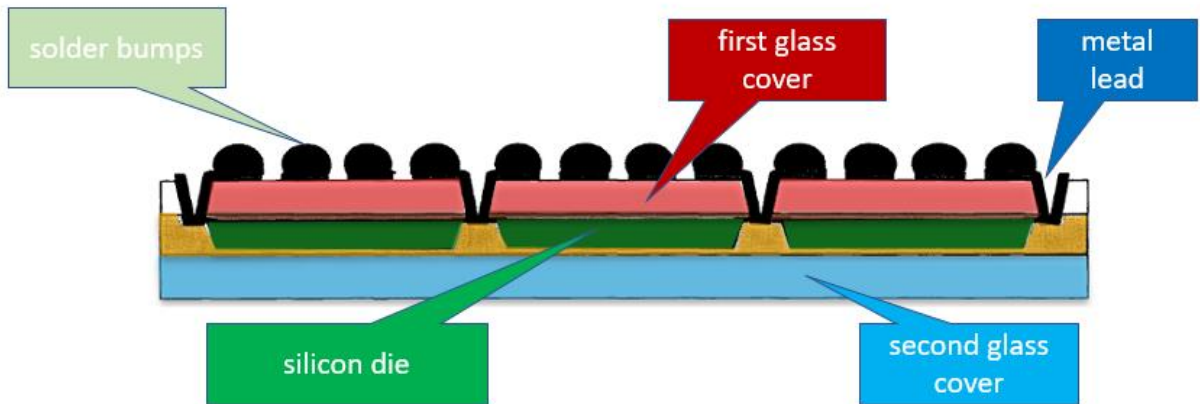
140. To the extent the preamble is considered to be a limitation, I am of the opinion that Badihi discloses this claim element.

141. Badihi's Figure 2 illustrates a process for packaging semiconductors at the wafer level. Ex. 1101, 237, Fig. 2. Badihi's Figure 3 illustrates the resulting packaged semiconductor where a **first glass cover** is bonded to the frontside of a **silicon die**, with the active side of the **silicon die** facing the **first glass cover**, **metal leads** and solder bumps are formed on the **first glass cover**, and a **second glass cover** is bonded to the backside of the **silicon die**:



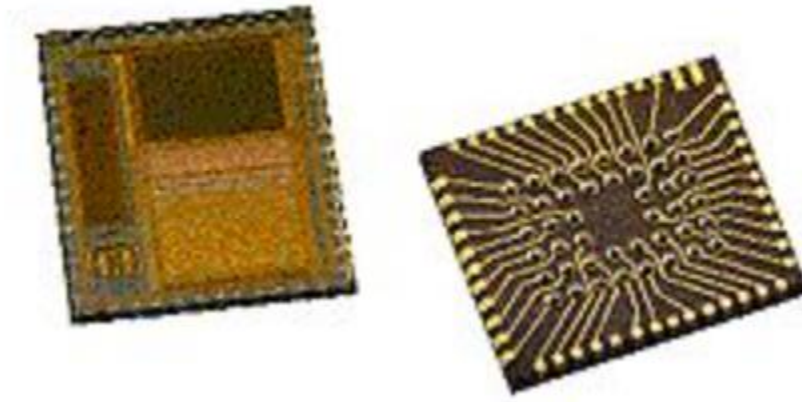
Ex. 1101, Fig. 3 (annotated). Badihi's disclosures are not specific to image sensors; however, Badihi discloses that its packaging process can be readily applied to silicon light detectors, CMOS image sensors, and CCD devices. *Id.*, 239. A POSITA would understand that CMOS image sensors include BSI CMOS image sensors and would further understand that the packaging taught by Badihi could be used for BSI CMOS image sensors.

142. Badihi's Figure 2 illustrates the resulting packaged semiconductor with metal leads and solder bumps covering top of the frontside (active) surface, indicating that the wafer as packaged would be back-illuminated (*i.e.*, ***a method of producing backside illuminated image sensor***):



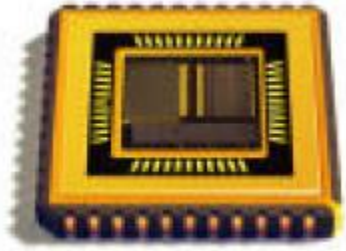
Id., Fig. 2 (annotated), 237.

143. Badihi's Figure 4 provides an example of a BSI image sensor created using the ShellPack wafer-level packaging process. *Id.*, Fig. 4. Figure 4 shows photographs of a CMOS APS image sensor, the Photobit PB0159, made with Badihi's wafer-level packaging process:



Ex. 1053, Ex. A, Fig. 4, 239. The photo on the right is the frontside of the packaged image sensor because Badihi specifically teaches metal leads and solder bumps are formed on the glass cover at the frontside of the packaged image sensor (facing the

active surface of the imager die), and the photo on the left is therefore the backside of the packaged image sensor. Ex. 1101, 237. A Photobit PB-159 datasheet confirms that the Badihi's CMOS APS is comprised of an array of 512x384 pixels:



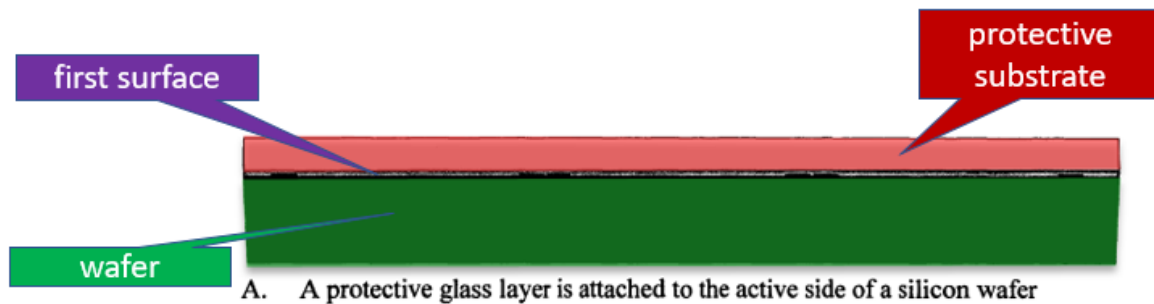
Ex. 1050, 1, 2.

144. A POSITA would recognize the packaged image sensor is a BSI image sensor because light would enter through its unobstructed backside since its frontside is covered by metal leads and solder bumps.

[1a] producing a plurality of image sensor circuits on a wafer having first and second surfaces each of the image sensor circuits being formed on the first surface and including a matrix of light-sensitive pixel regions extending into the wafer from the first surface;

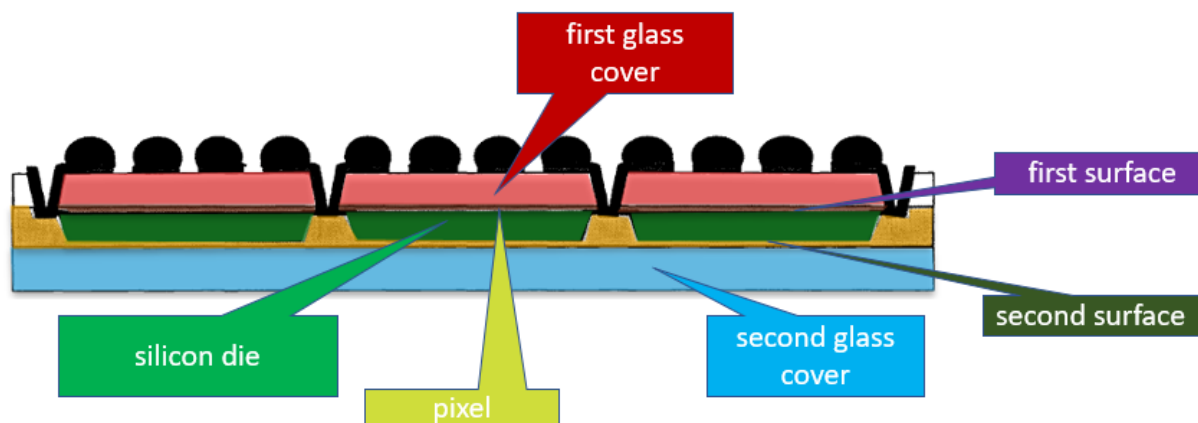
145. I am of the opinion that Badihi discloses or renders obvious this claim element.

146. Badihi's silicon wafer corresponds to the claimed "wafer" and its active side facing the **protective glass layer (first glass cover)** corresponds to the claimed "first surface," which is illustrated in Badihi's Figure 2:



Ex. 1101, 236-237, Fig. 2 (annotated). Badihi discloses applying its method to package CMOS image sensors, such as the CMOS APS product called Photobit PB0159. *Id.*, Fig. 4. It was well known that each CMOS image sensor contains an array of pixels, including the Photobit PB0159 containing 512x384 pixels. Ex. 1050, 1-2. Such array of pixels corresponds to the claimed “imaging sensor circuit.” See *supra*, §V.A. Badihi discloses a “wafer-level manufacturing process” where “the dies are packaged and encapsulated into separate enclosures while still in wafer form” and “enables to package all dies of the entire wafer at the same time” (i.e., ***producing a plurality of image sensor circuits on a wafer***). Ex. 1101, 237, Fig. 2C (showing multiple dies). Indeed, Badihi discloses that “[w]afer [l]evel CSP manufacturing” enables the “packag[ing] [of] ***all the dies*** of the entire wafer at the same time rather than ... one die at a time.” *Id.* Badihi discloses “[a] thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive” (i.e., ***a wafer having a first surface***) and “a second thin glass cover is bonded onto the silicon dies back side” (i.e., ***a wafer having a second surface***). *Id.*, 237. Badihi’s

Figure 4 illustrates the process step where a **wafer** with a **glass layer** is facing the active side and **another glass layer is** facing the backside:



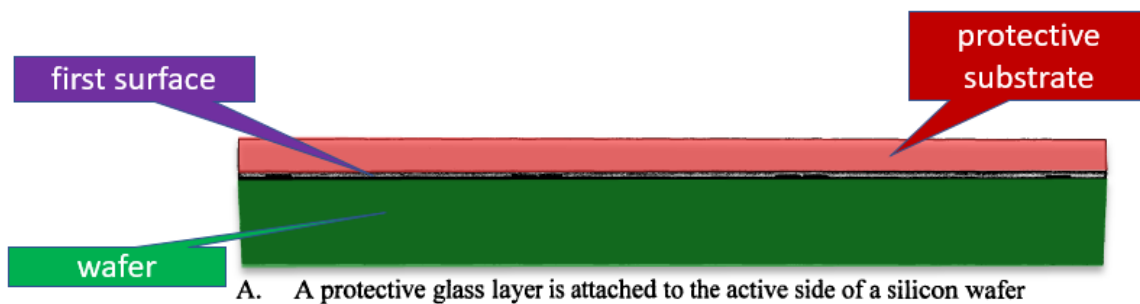
Ex. 1101, Fig. 4 (annotated). A POSITA would readily understand that the image sensor circuits are formed on the active side of the top surface of the wafer, especially where solder bumps are located on the first glass cover as disclosed in Badihi (*i.e.*, ***each of the image sensor circuits being formed on the first surface***). *Id.*, 237, Fig. 3.

147. It was well-known that in a CMOS process, microelectronics are built on and into the active side of the die. *See supra*, §§V.A, C. Pixels in a CMOS APS image sensor built using CMOS process are no different. *See supra*, §§V.A, C. It was also well-known that APS pixels have light-sensitive pixel regions built into the active side of the die (*i.e.*, ***a matrix of light-sensitive pixel regions extending into the wafer from the first surface***). *See supra*, §§V.A, C. Therefore, it would have been obvious there is a matrix of light-sensitive pixel regions that extend into the wafer from the active side of the wafer. *See supra*, §§V.A, C.

[1b] securing the wafer onto a protective substrate such that the first surface faces the protective substrate;

148. I am of the opinion that Badihi discloses this claim element.

149. Badihi's protective glass layer (first glass cover) corresponds to the claimed "protective substrate" and the active side of Badihi's silicon wafer corresponds to the claimed "first surface." Ex. 1101, 237. Badihi discloses the "thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive" (*i.e., securing the wafer onto a protective substrate*). *Id.* Specifically, Badihi's Figure 2 illustrates a process step of bonding the active (frontside) surface of the **silicon wafer** to the **protective glass layer (first glass cover)**:



Id., 237, Fig. 2 (annotated).

150. Relatedly, Badihi's Figure 3 discloses the resulting packaged image sensor where the **protective glass layer (first glass cover)** is **bonded** to the **wafer** such that it faces the active side of the **wafer** (*i.e., securing the wafer onto a protective substrate such that the first surface faces the protective substrate*):

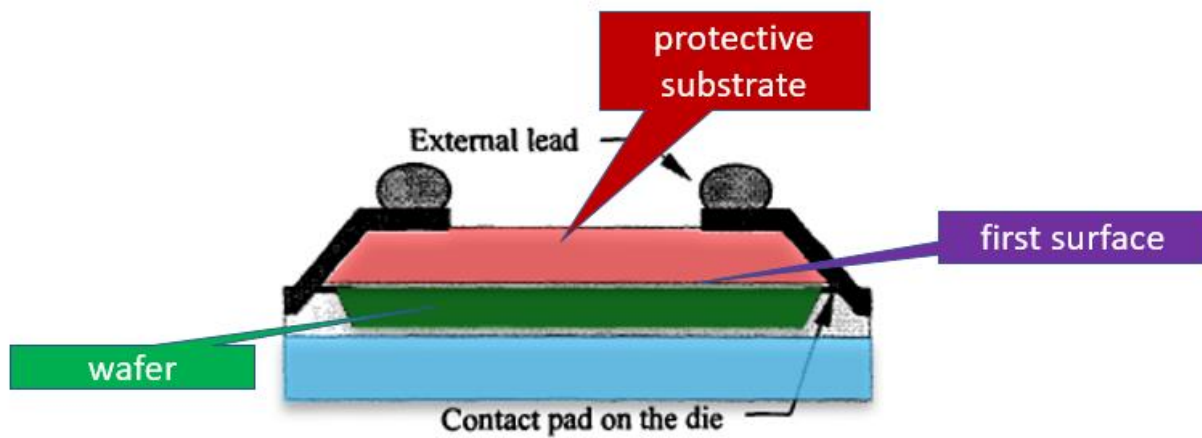


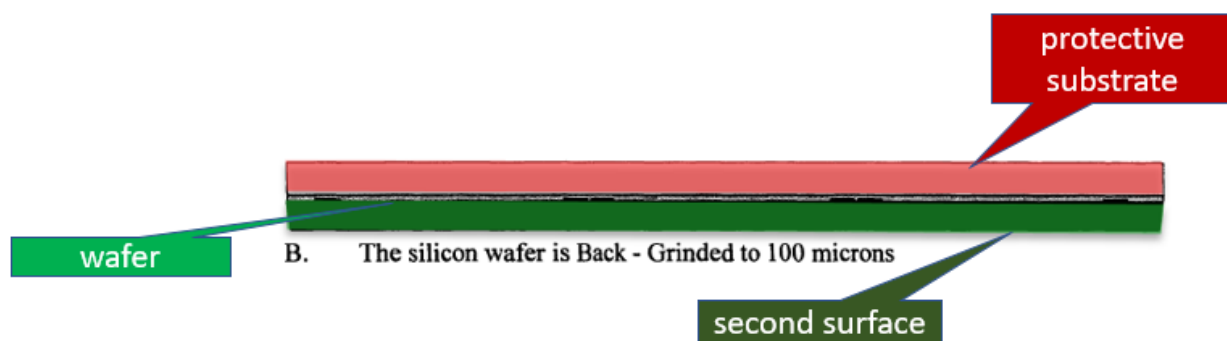
Figure 3: The CSP schematical cross section

Id., Fig. 3 (annotated).

[1c] removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface;

151. I am of the opinion that Badihi discloses or renders obvious this claim element.

152. Badihi's Figure 2 illustrates the process step where the **silicon wafer** is grinded from its backside until 100 microns is left (*i.e., removing material from the second surface of the wafer*):



Id., 237, Fig. 2 (annotated).

153. A POSITA would readily understand that the purpose of grinding the silicon wafer from its backside before enclosing it in a glass transparent package is so that the light-sensitive pixel regions are exposed from the backside of the silicon wafer (*i.e., removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface*).⁴ See *supra*, §§V.A-B. Accordingly, Badihi at a minimum renders this claim limitation obvious.

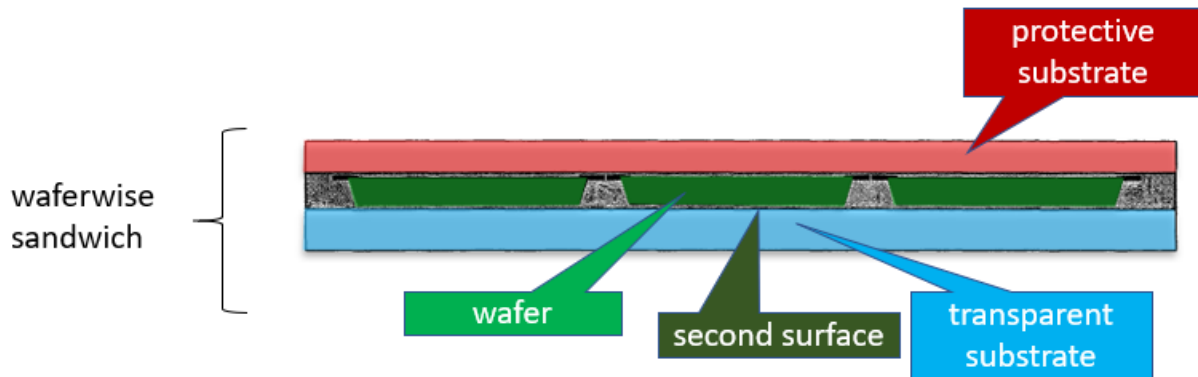
[1d] securing a transparent substrate onto the second surface of the wafer, thereby producing a waferwise sandwich; and
--

154. I am of the opinion that Badihi discloses this claim element.

155. Badihi’s second glass cover corresponds to the claimed “transparent substrate.” Ex. 1101, 237. Badihi discloses the “second thin glass cover is bonded onto the silicon dies back side to achieve a complete protective enclosure for each die” (*i.e., securing a transparent substrate onto the second surface of the wafer*) resulting in “dies [that] are packaged and encapsulated in separate enclosures while still in wafer form” (*i.e., producing a waferwise sandwich*). *Id.* Specifically, Badihi’s Figure 2 illustrates a waferwise sandwich with the **protective glass layer**

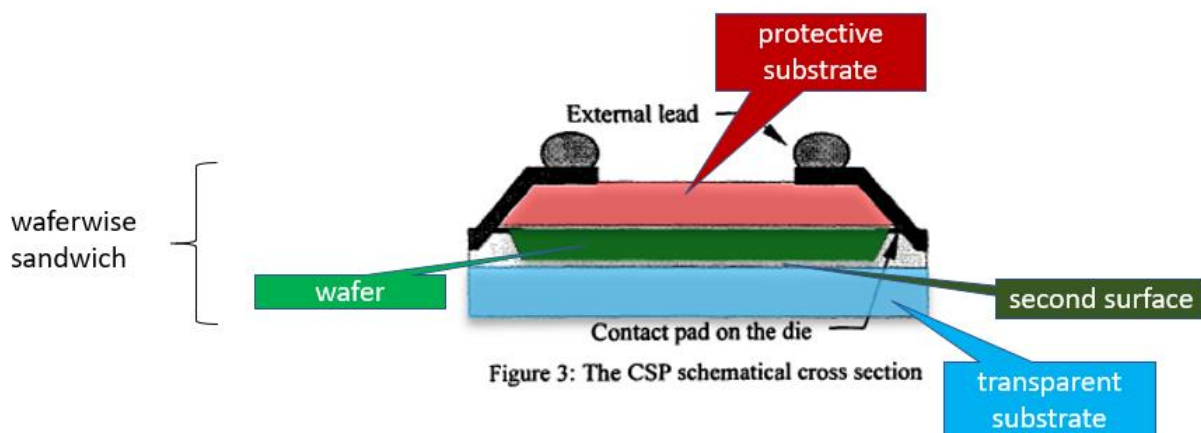
⁴ See *supra*, §V.B; §X, Ground 1, claim 1c. A POSITA would readily understand that Badihi discloses what is described in the ’965 patent.

(**first glass cover**) bonded to the active (frontside) surface of the **silicon wafer** and the **second glass cover** bonded to the backside surface of the **silicon wafer**:



Id., 237, Fig. 2 (annotated).

156. Badihi's Figure 3 illustrates the resulting packaged image sensor where the **protective glass layer (first glass cover)** and the **second glass cover** sandwich the **silicon wafer** (*i.e., securing a transparent substrate onto the second surface of the wafer, thereby producing a waferwise sandwich*):

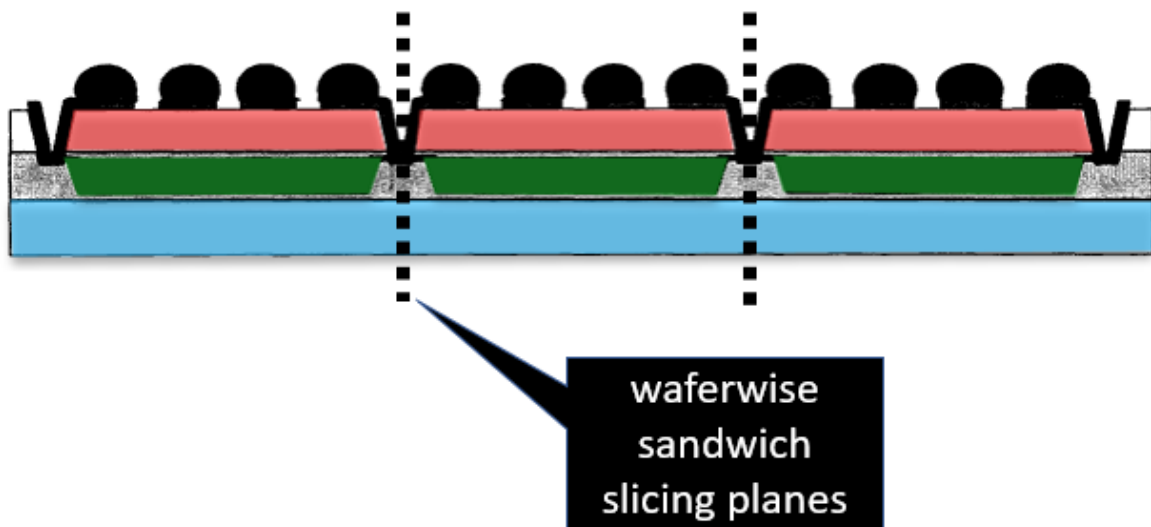


Id., Fig. 3 (annotated).

[1e] slicing the waferwise sandwich, thereby defining a plurality of backside illuminated image sensors.

157. I am of the opinion that Badihi discloses this claim element.

158. Badihi discloses that “[w]afer level CSP manufacturing” enables the “packag[ing] [of] all the dies of the entire wafer at the same time rather than ... one die at a time” (i.e., **defining a plurality of backside illuminated image sensors**). Ex. 1101, 237. Specifically, Badihi’s Figure 2 illustrates a process step of “[w]afer dicing” to “yield[] individual packaged dies” (i.e., **slicing the waferwise sandwich, thereby defining a plurality of backside illuminated image sensors**):



Id., 237, Fig. 2 (annotated).

159. Badihi’s Figure 3 illustrates the resulting packaged image sensor after it is diced:

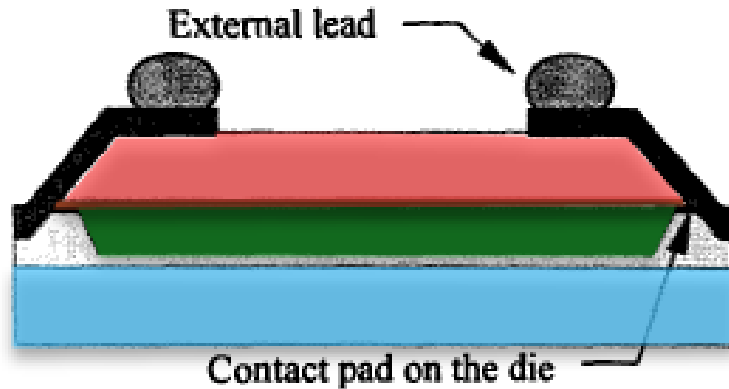


Figure 3: The CSP schematical cross section

Id., Fig. 3 (annotated).

2. Claim 2

[2pre] The method according to claim 1, wherein the step of securing the protective substrate onto the first surface comprises

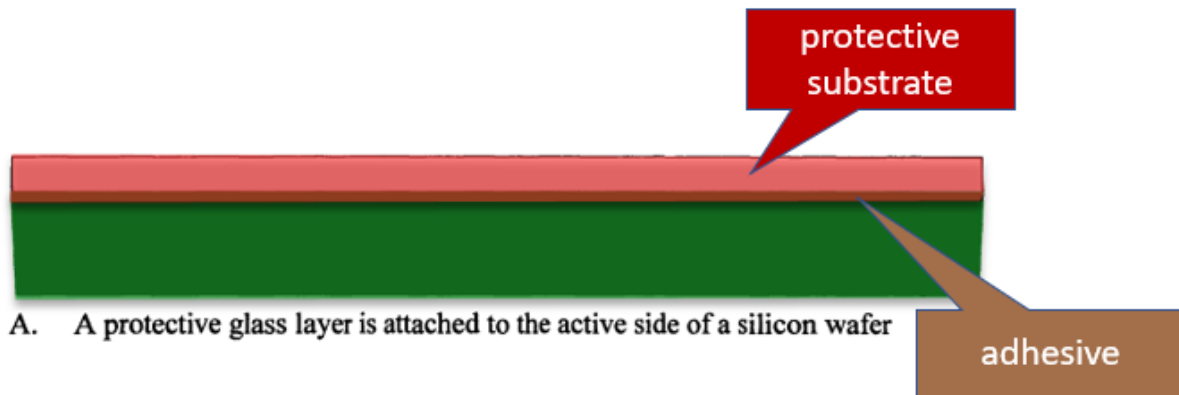
160. I am of the opinion that Badihi discloses claim 2pre for the same reasons as claim 1b above.

[2a] depositing an adhesive onto the protective substrate, and then

161. I am of the opinion that Badihi discloses or renders obvious this claim element.

162. Badihi's protective glass layer (first glass cover) and epoxy adhesive correspond to the claimed "protective substrate" and "adhesive," respectively. See *supra*, claim 1b. Badihi discloses a process step of using an epoxy adhesive to bond a thin protective glass layer to the active side of a silicon wafer. Ex. 1101,

237. Badihi's Figure 2 illustrates the **epoxy adhesive** that is deposited to attach the **protective glass layer** to the active side of a **silicon wafer**:



Id., 237, Fig. 2 (annotated). It was common practice to use a supporting structure or plate, such as Badihi's protective glass layer, prior to thinning the silicon wafer. *See supra*, §V.B. It was conventional to apply an adhesive to such supporting structure or plate first before attaching the wafer (*i.e.*, **depositing an adhesive onto the protective substrate**). *Id.* A POSITA would know how to deposit or apply such epoxy adhesive in Nixon in the same manner as described for the adhesive in the '965 patent. Ex. 1101, 237, Fig. 2; Ex. 1001, 6:35-40, Fig. 4(A).

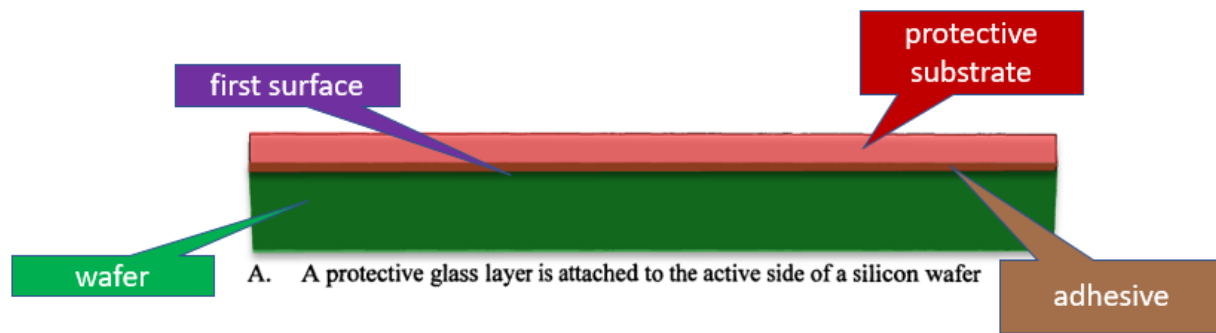
163. A POSITA would also readily recognize that when bonding two surfaces together, adhesive must first be placed on at least one of those surfaces. In the context of bonding the wafer to the protective substrate, there are only three choices: the adhesive could be placed on the wafer, the protective substrate, or both. Whichever of the three choices is used during the manufacturing process is

merely a design choice. Therefore, it would have been obvious to a POSITA to apply the adhesive on the protective substrate. *See supra*, §V.B. Accordingly, Badihi at a minimum renders this limitation obvious.

[2b] placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive.

164. I am of the opinion that Badihi discloses this claim element.

165. Because the epoxy adhesive is applied onto the protective glass layer, the silicon wafer would be placed onto the protective layer where the epoxy adhesive is deposited to secure the protective glass layer onto the silicon wafer (*i.e., placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive*). *See supra*, claim 2a, §V.B. Badihi discloses a process step where “[a] thin protective glass layer is bonded to the active side of a silicon wafer with epoxy adhesive,” therefore the active side of the silicon wafer would contact the deposited adhesive on the protective glass layer (*i.e., the first surface contacts the deposited adhesive*). Ex. 1101, 237; *see supra*, claim 2a. Badihi’s Figure 2 describes that “[a] protective glass layer is attached to the active side of a silicon wafer” and illustrates that the **silicon wafer** is placed onto the **protective glass layer** such that the active side of the **silicon wafer** contacts the **epoxy adhesive** (*i.e., placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive*):



Id., 237, Fig. 2 (annotated).

3. Claim 7

[7pre]. The method according to claim 1, wherein the step of securing a transparent substrate onto the second surface comprises

166. I am of the opinion that Badihi discloses claim 7pre for the same reasons as claim 1d above.

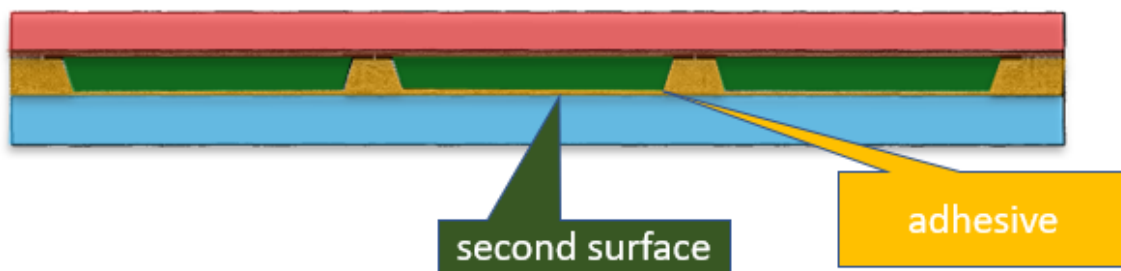
167. Badihi’s second glass cover corresponds to the claimed “transparent substrate.” *See supra*, claim 1d.

[7a] depositing an adhesive onto the second surface, and then

168. I am of the opinion that Badihi discloses or renders obvious this claim element.

169. Badihi’s epoxy adhesive corresponds to the claimed “adhesive” and the backside of Badihi’s silicon dies correspond to the claimed “second surface.” Ex. 1101, 237, Fig. 2. Badihi discloses a process step of bonding the second glass cover to the backside of the silicon dies. *Id.*, 237. For the epoxy adhesive to both

fill the grooves and bond second glass cover to the silicon dies, the epoxy would have to be applied first to the wafer structure to fill the grooves and cover the backside of the dies. This way, the “glass transparent package encases the [i]mager [d]ie in a solid protecting optically clear enclosure.” *Id.*, 239. If the epoxy is first applied to second glass cover and then placed on the wafer structure, there may not be enough epoxy to fill the grooves between the dies. Alternatively, epoxy could be applied to both the wafer structure and second glass cover before they are bonded to ensure the epoxy fills the grooves and covers dies for the best bond and complete enclosure. Badihi’s Figure 2 illustrates depositing an **adhesive** between the grooves and on the backside of the **dies**:



Id., 237, Fig. 2 (annotated). A POSITA would know how to deposit or apply such epoxy adhesive layer in Badihi in the same manner as described for the adhesive in the '965 patent. Ex. 1101, 237, Fig. 2; Ex. 1001, 7:57-8:3, Fig. 4(E).

170. A POSITA would readily recognize the three design choices in applying the adhesive on the backside of the wafer, the transparent substrate, or

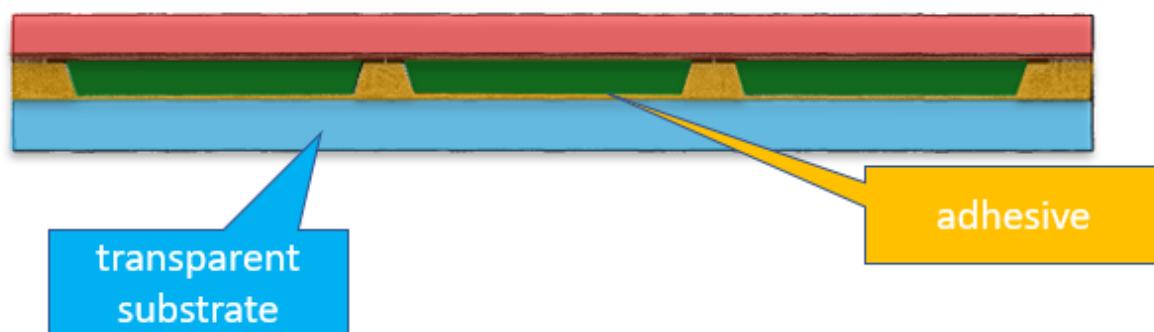
both. Therefore, it would have been obvious to a POSITA to apply the adhesive on the backside of the wafer (*i.e., depositing an adhesive onto the second surface*).

Accordingly, Badihi at a minimum renders this limitation obvious.

[7b] placing the transparent substrate onto the deposited adhesive

171. I am of the opinion that Badihi discloses this claim element.

172. Because the epoxy adhesive is applied onto the backside of the silicon wafer, the second glass cover would be placed onto the backside of the silicon wafer where the epoxy adhesive is deposited to secure the second glass cover onto the backside of the silicon wafer (*i.e., placing the transparent substrate onto the deposited adhesive*). See *supra*, claim 7a. Badihi's Figure 2 illustrates placing the **second glass cover** onto the **adhesive**:



Id., 237, Fig. 2 (annotated).

4. Claim 8

[8pre]. The method according to claim 7,

173. I am of the opinion that Badihi discloses claim 8pre for the same reasons as claim 7 above.

[8a] wherein the step of removing material includes separating each of the plurality of image sensor circuits; and

174. I am of the opinion that Badihi discloses this claim element.

175. Badihi discloses a process step of removing material from the backside of the silicon wafer. *See supra*, claim 1c. Badihi further discloses a process step of etching the silicon material between the dies from the backside of the wafer, “yielding individual IC’s attached to the supporting glass layer” (*i.e.*, *wherein the step of removing material includes separating each of the plurality of image sensor circuits*). Ex. 1101, 237. Badihi’s Figure 2 illustrates etching away the silicon material between the **dies** after the backside is grinded:



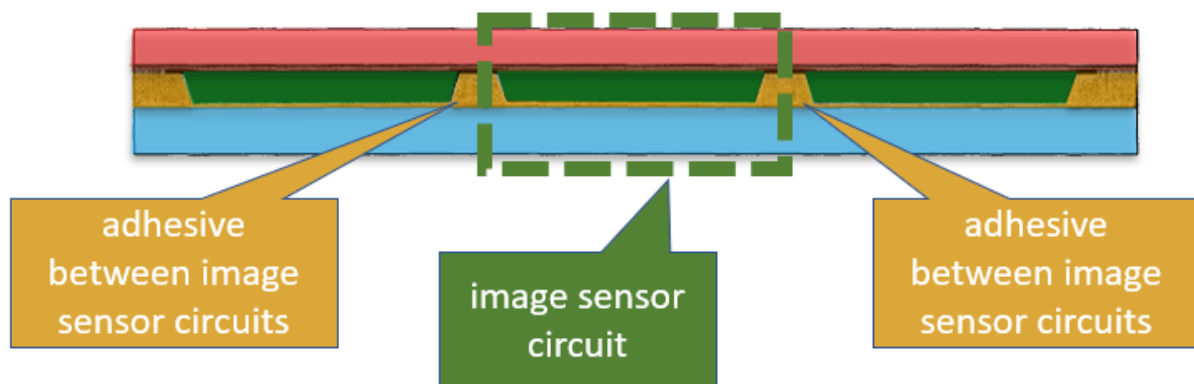
C. The silicon material between the dies (streets) is etched away

Id., 237, Fig. 2 (annotated).

[8b] wherein the step of depositing the adhesive onto the second surface further comprises depositing adhesive into interstices located between the plurality of image sensor circuits, thereby protecting the image sensor circuits.

176. I am of the opinion that Badihi discloses this claim element.

177. Badihi discloses a process step of bonding the second glass cover to the backside of the silicon dies “to achieve a complete protective enclosure for each die” (*i.e.*, ***thereby protecting the image sensor circuits***). Ex. 1101, 237. A POSITA would readily recognize that epoxy adhesive may also be used to fill in the grooves or trenches between the dies, which is disclosed in an article also written by the same author for Badihi. Ex. 1047, Fig. 4 (disclosing that “the epoxy fills the trenches between the dies”). Badihi’s Figure 2 illustrates using **adhesive** to fill in the grooves between the **dies**:



Id., 237, Fig. 2 (annotated).

5. Claim 9

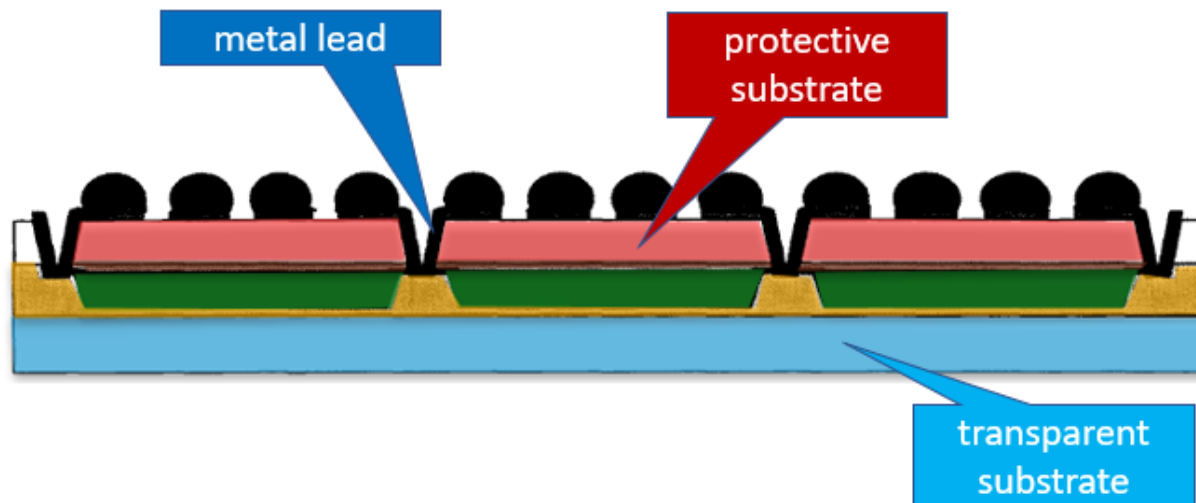
[9pre] The method according to claim 1, further comprising the step of

178. I am of the opinion that Badihi discloses claim 9pre for the same reasons as claim 1 above.

[9a] forming metal leads on the protective substrate after the step of securing the transparent substrate,

179. I am of the opinion that Badihi discloses this claim element.

180. Badihi's individual leads corresponds to the claimed "metal leads." Ex. 1101, 237, Figs. 2, 3. Badihi discloses that after the process step where the second glass cover is bonded to the backside of the silicon dies (*i.e., after the step of securing the transparent substrate*), "[d]eep notches are drawn between the dies, revealing the cross-section of the bond pads" and that "[a] metal layer, patterned by lithography to individual leads, is deposited to contact the bond pads at their cross sections" (*i.e., forming metal leads on the protective substrate*). *Id.*, 237. Badihi's Figure 2 illustrates a process step of notching between the **dies** from the **protective glass layer (first glass cover)** to expose the bond pads at their cross sections before forming **individual leads** on the **protective glass layer (first glass cover)**:

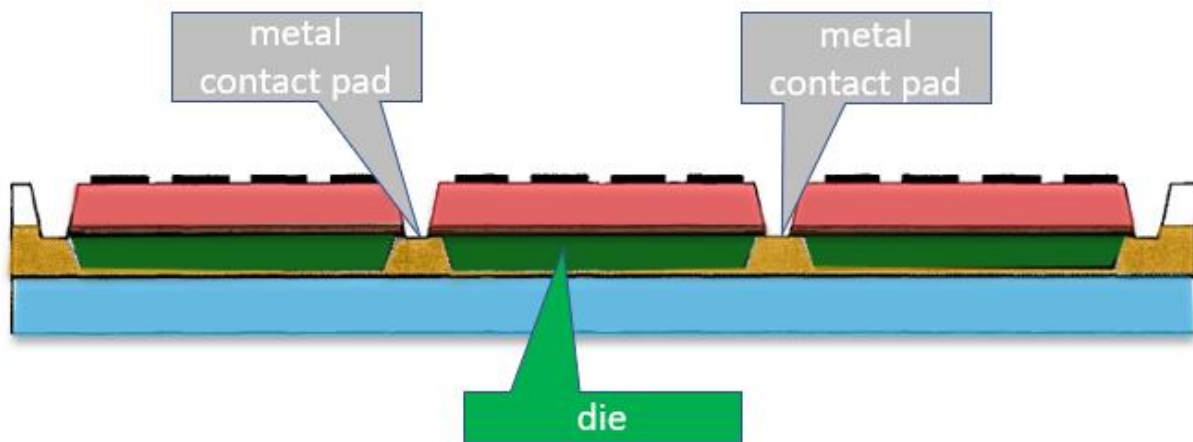


Id., 237, Fig. 2 (annotated).

[9b] wherein the metal leads are connected to metal contact pads located on the first surface of the wafer.

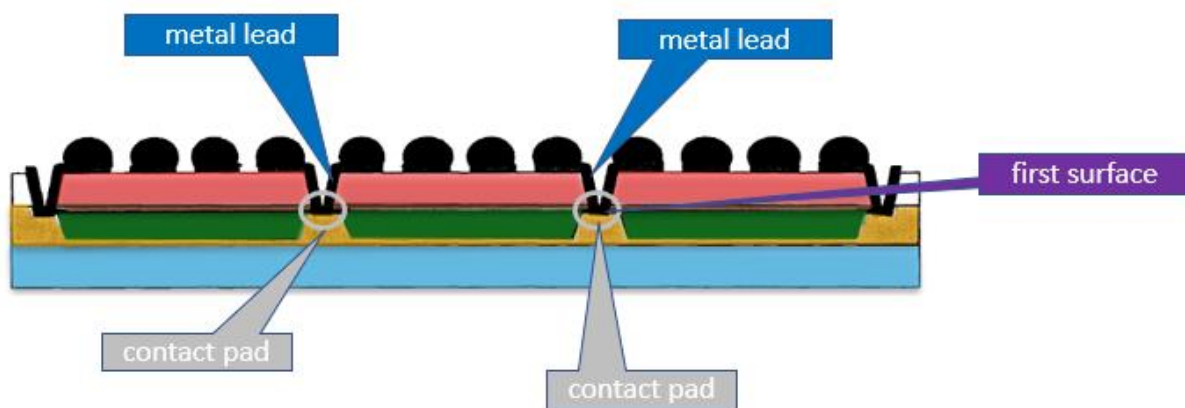
181. I am of the opinion that Badihi discloses this claim element.

182. Badihi discloses a process step where “[a] metal layer, patterned by lithography to individual leads, is deposited to contact the bond pads at their cross sections” (*i.e.*, ***wherein the metal leads are connected to metal contact pads***). See *supra*, claim 9a. Badihi further discloses that “[d]eep notches are drawn between the dies, revealing the cross-section of the **bond pads**,” which is illustrated in one figure in Badihi’s Figure 2:



Ex. 1101, 237; Fig. 2 (annotated).

183. Another process step in the same figure illustrates **individual leads** that are connected to the **bond pads** on the active side of the wafer through notching (i.e., *wherein the metal leads are connected to metal contact pads located on the first surface of the wafer*):



Id., 237, Fig. 2 (annotated).

XIII. GROUND 4: BADIHI IN VIEW OF ASSADI RENDERS OBVIOUS CLAIM 10

184. I am of the opinion that Badihi in view of Assadi renders obvious claim 10 of the '965 patent.

1. Reasons to Combine Badihi with Assadi

185. A POSITA would have been motivated to modify Badihi's wafer level packaging process for a BSI CMOS image sensor to include a passivation layer to ensure that the frontside (active) surface of the wafer where the microelectronics of the CMOS image sensors are located are protected from abrasion, moisture, or contaminants. Badihi teaches a generalized process for manufacturing semiconductor devices, including BSI image sensors. Indeed, Badihi's Figure 4 illustrates a packaged image sensor has a frontside blanketed with metal leads and solder bumps and an unobstructed backside to allow light to enter. Ex. 1101, Fig. 4; *see supra*, §§V.A, C-D. By the priority date of the '965 patent, it was well-known and highly conventional that passivation layers should be included in CMOS image sensors to protect from, among other things, abrasion, moisture, and contaminants. *See supra*, §V.C. Assadi provides an example of a passivation layer that provides these well-known benefits. Indeed, Assadi explains that passivation layers should be included "over[] the entirety of sensor 176, including sensor area 210 and non-sensor area (logic area 220 and bond pad area 240)" to provide "resistance to environmental contaminants, particularly moisture." Ex. 1044, 4:26-

44, 9:31-32. Including Assadi's passivation layer in Badihi's manufacturing process for a BSI CMOS image sensor would have the obvious added benefit of protecting the microelectronics necessary to convert the photons collected into electrical signals. *See supra*, §§V.C-D.

186. In addition to being motivated to do so, a POSITA would have understood that modifying Badihi's manufacturing process to include a passivation layer, as taught in Assadi's, would have been a simple matter of applying well understood semiconductor fabrication techniques. *See supra*, §§V.C-D. Indeed, Assadi's passivation layer in a CMOS device is readily applicable to Badihi's manufacturing process for a BSI CMOS image sensor (as shown in Figure 4). *See supra*, §§V.C-D. A POSITA could have modified Badihi's manufacturing process to include a passivation layer such as taught in Merrill with a reasonable expectation of success. *See supra*, §§V.C-D. Such a modification to Badihi's manufacturing process would have merely required adding additional conventional, well-known, manufacturing process steps. *See supra*, §§V.C-D.

2. Claim 10

[10pre]. The method according to claim 1, wherein the step of securing the wafer onto a protective substrate further comprises:

187. I am of the opinion that Badihi discloses claim 10pre for the same reasons as claims 1 and 1b above.

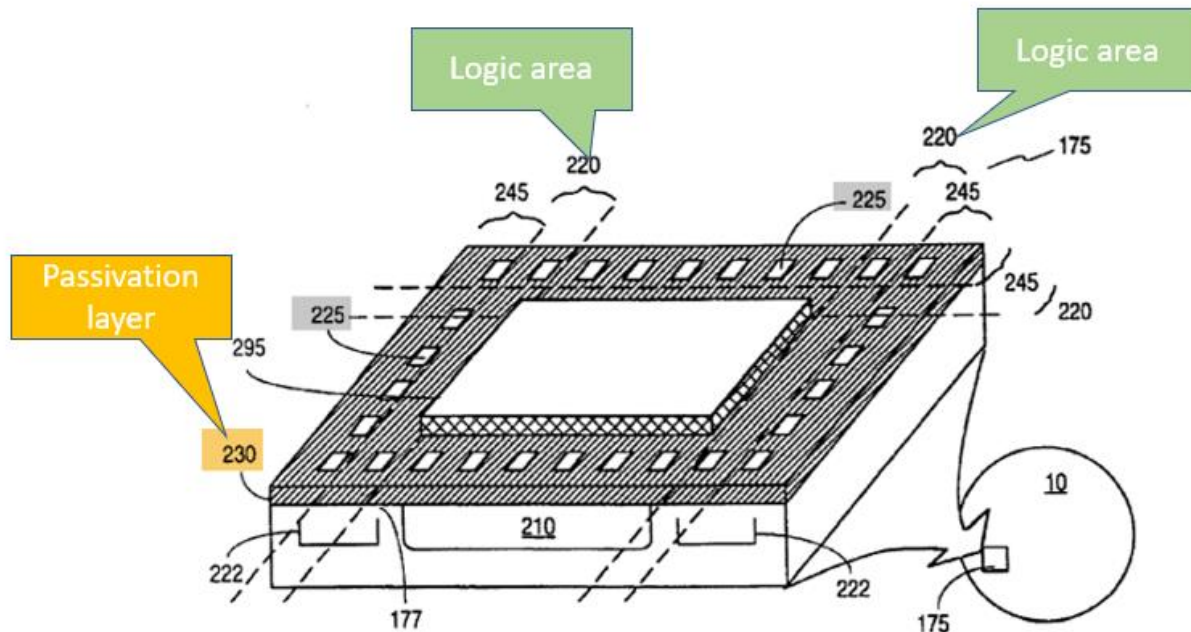
[10a] forming a passivation layer on the first surface of the wafer;

188. I am of the opinion that Badihi combined with Assadi renders obvious this claim element.

189. It was very well-known and highly conventional that passivation layers should be included in CMOS image sensors to protect from, among other things, abrasion, moisture, and contaminants. *See supra*, §V.C. Therefore, a POSITA would readily understand that Badihi’s manufacturing process includes a step of “forming a passivation layer on the first surface of the wafer.” *See supra*, §§V.C, D. Badihi discloses an active side of the silicon wafer, the side of which notches are drawn in order to reveal the bond pads on the active side of the silicon wafer. Ex. 1101, 237, Fig. 2. It would have been conventional to form a passivation layer on the active surface to protect the microelectronics. *See supra*, §V.C; §XI, Ground 2, 10a.

190. Assadi teaches a conventional mechanism to protect the microelectronics components on the active surface. Assadi’s passivation layer 230 corresponds to the claimed “passivation layer.” Ex. 1044, 4:15-45. Assadi discloses an image sensor 175 with sensor area 210 representing “the photosensing region or area” and logic area 220 that “operates the individual pixels and drives signals from the pixels off sensor 175.” *Id.*, 4:15-26. Assadi further discloses a

passivation layer 230 that “overlies the entirety of sensor 175, including ... logic area 220” (i.e., *forming a passivation layer on the first surface of the wafer*):



Id., 4:15-45, Fig. 3b (annotated).

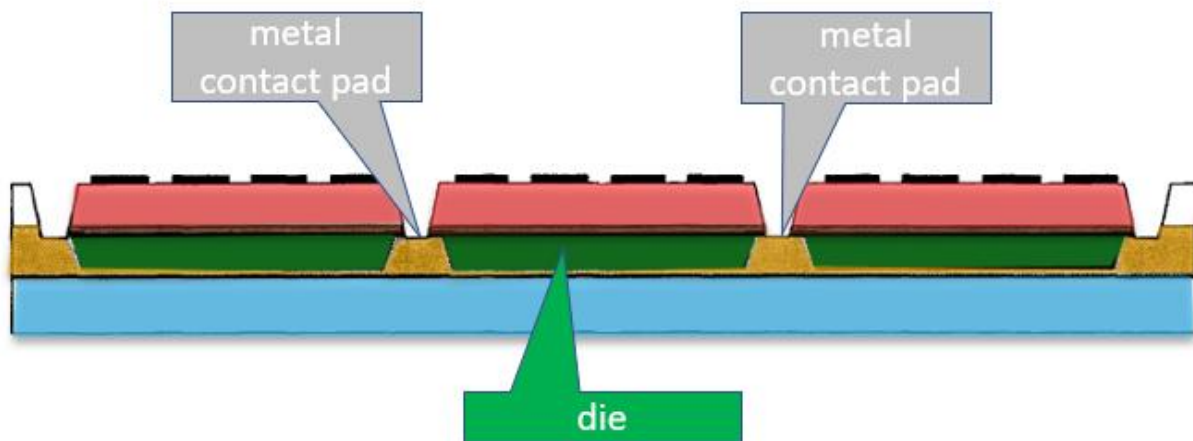
191. A POSITA would have readily understood at the time of invention the use of a passivation layer equally applies to BSI image sensors and would have been simply a routine, design choice that could easily be implemented by a POSITA. *See supra*, §V.C. Thus, it would have been obvious for a POSITA to include Assadi’s passivation layer on the active side of Badihi’s wafer-level packaging process of image sensors to protect the pixels from abrasion, moisture, and contaminants. *See supra*, §§V.C-D.

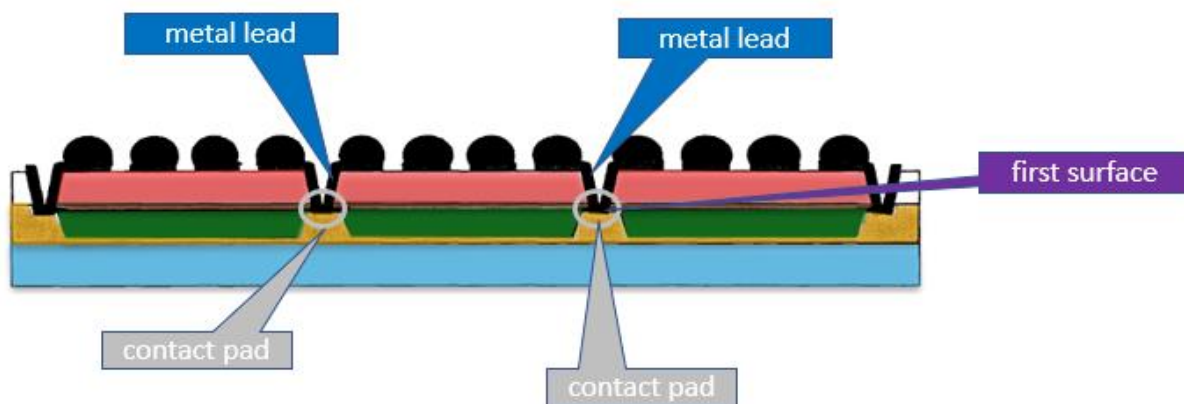
[10b] forming openings in the passivation layer; and

192. I am of the opinion that Badihi combined with Assadi renders obvious this claim element.

193. A POSITA would have been motivated to modify Badihi's wafer-level packaging process of image sensors to include Assadi's passivation layer to protect microelectronics on the active side of the silicon wafer. *See supra*, claim 10a.

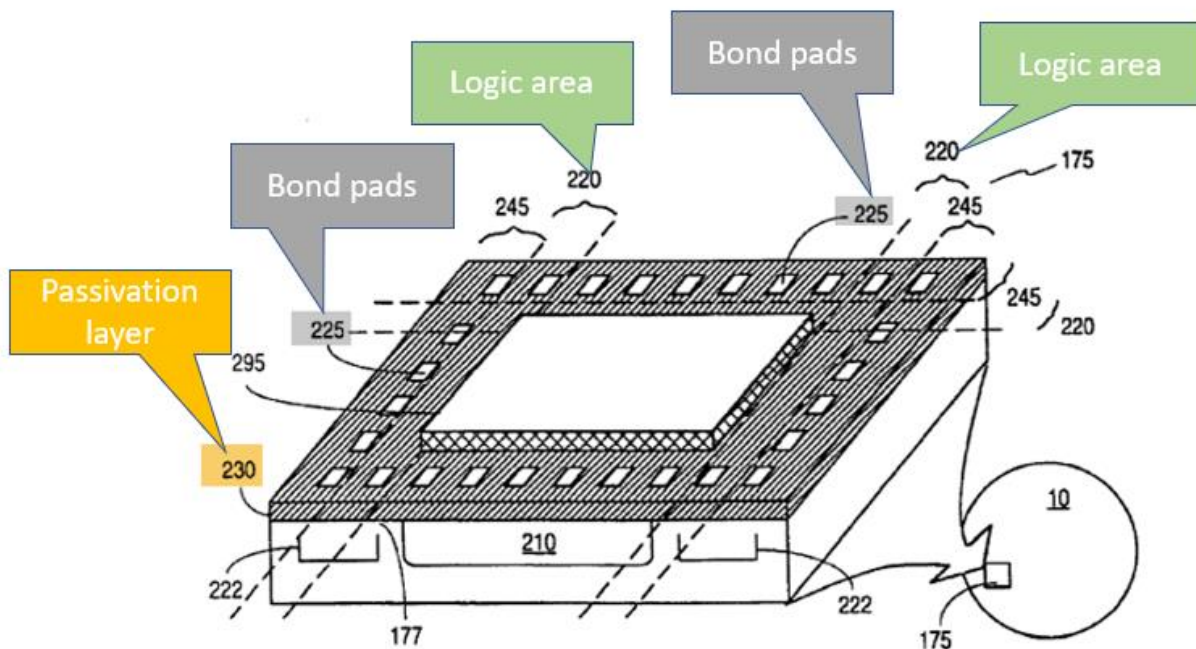
194. Badihi discloses drawing deep notches from the active side of the silicon wafer to expose the bond pads on the active side of the silicon wafer and then forming individual leads to contact the bond pads. Ex. 1101, 237. Badihi's Figure 2 illustrates that the notching is performed from the active side of the wafer through the **protective glass layer** to reveal the **bond pads** on the active side of the silicon wafer:





Ex. 1101, 237, Fig. 2 (annotated).

195. Assadi discloses a **passivation layer 230** on the frontside (active) surface of image sensor 175, where **openings** for **bond pads 225**, which are “arranged on the ... top surface of sensor 175” and “are electrically linked or coupled to device circuitry 222,” are formed so that the “logic circuitry 220 that operates the individual pixels [can] drive[] signals from the pixels off sensor 175” (*i.e., forming openings in the passivation layer*), as illustrated in Assadi’s Figure 3b:



Ex. 1044, Fig. 3b (annotated), 4:15-45.

196. A POSITA would readily understand that use of passivation layer would be equally applicable to BSI image sensors and that openings in the passivation layer may be formed before a protective substrate is secured based on the different materials used to form the passivation layer and protective substrate. *See supra*, §V.C; §XI, Ground 2, claims 10a, 10b. Accordingly, this limitation would have been obvious over Badihi in combination with Assadi.

[10c] securing the protective substrate onto the passivation layer.

197. I am of the opinion that Badihi combined with Assadi renders obvious this claim element.

198. It would have been obvious to a POSITA to modify Badihi's wafer-level packaging process for image sensors to include Assadi's passivation layer. *See supra*, claim 10a. The passivation layer is a conventional component that is deposited on the frontside (active) surface of the semiconductor substrate to protect the microelectronics there from abrasion, moisture, or contaminants. *See supra*, §V.C.

199. Badihi further discloses a process step where a protective layer is bonded to the silicon wafer using an epoxy adhesive (*i.e.*, ***securing the protective substrate***). Ex. 1101, 237, Fig. 2. A POSITA would also readily understand that Badihi's protective layer would be secured onto Assadi's passivation layer that overlies the frontside (active) surface of the semiconductor substrate (*i.e.*, ***securing the protective substrate onto the passivation layer***) to further protect the Badihi's BSI CMOS image sensor and provide additional support during the step of removal of material from the backside of the semiconductor substrate. *See supra*, §§V.B-D.

XIV. CONCLUSION

200. For the aforementioned reasons, in my opinion, to a person of ordinary skill in the art, the Challenged Claims of the '965 patent are invalid in view of the prior art.

201. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. 1001.

Date: December 16, 2022

Respectfully Submitted

A handwritten signature in black ink, appearing to read 'Konstantinos P. Giapis', written in a cursive style.

Dr. Konstantinos P. Giapis