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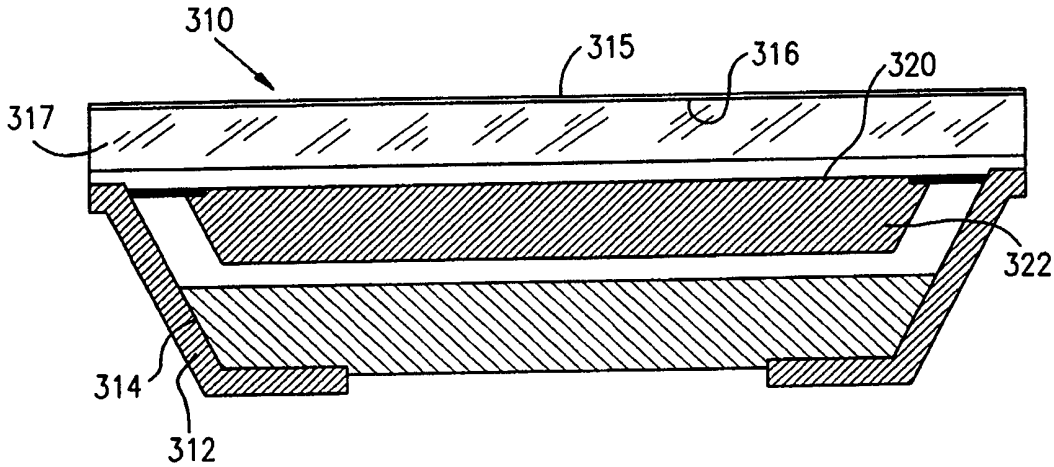

(57) Abstract

An integrally packaged optronic integrated circuit device (310) including an integrated circuit die (322) containing at least one of a radiation emitter and radiation receiver and having top and bottom surfaces formed of electrically insulative and mechanically protective material, at least one of the surfaces (317) being transparent to radiation, and electrically insulative edge surfaces (314) having pads.

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INTEGRATED CIRCUIT DEVICE

FIELD OF THE INVENTION

The present invention relates to methods and apparatus for producing integrated circuit devices and to integrated circuit devices produced thereby and more particularly to an optronic integrally packaged die.

BACKGROUND OF THE INVENTION

An essential step in the manufacture of all integrated circuit devices is known as "packaging" and involves mechanical and environmental protection of a silicon chip which is at the heart of the integrated circuit as well as electrical interconnection between predetermined locations on the silicon chip and external electrical terminals.

At present three principal technologies are employed for packaging semiconductors: wire bonding, tape automatic bonding (TAB) and flip chip.

Wire bonding employs heat and ultrasonic energy to weld gold bonding wires between bond pads on the chip and contacts on the package.

Tape automatic bonding (TAB) employs a copper foil tape instead of bonding wire. The copper foil tape is configured for each specific die and package combination and includes a pattern of copper traces suited thereto. The individual leads may be connected individually or as a group to the various bond pads on the chip.

Flip chips are integrated circuit dies which have solder bumps formed on top of the bonding pads, thus allowing the die to be "flipped" circuit side down and directly soldered to a substrate. Wire bonds are not required and considerable savings in package spacing may be realized.

The above-described technologies each have certain limitations. Both wire bonding and TAB bonding are prone to bad bond formation and subject the die to relatively high temperatures and mechanical pressures. Both wire bond and TAB technologies are problematic from a package size viewpoint, producing integrated circuit devices having a die-to-package area ratio ranging from about 10% to 60%.

The flip-chip does not provide packaging but rather only interconnection. The interconnection encounters problems of uniformity in the solder bumps as well as in thermal expansion mismatching, which limits the use of available substrates to silicon or materials which have thermal expansion characteristics similar to those of silicon.

Optronic packages for semiconductors are known. Conventional optronic packages used for imaging employ a ceramic housing onto which is sealingly mounted a transparent window. Optronic packages used for low level imaging, light emission and radiation detection, including light detection, employ a clear plastic enclosure.

Described in applicant's published PCT Application WO 95/19645 are methods and apparatus for producing integrated circuit devices, including, inter alia, integrally packaged dies having a radiation transparent protective layer.

SUMMARY OF THE INVENTION

The present invention seeks to provide optronic integrated circuit devices which are extremely compact as well as apparatus and techniques for the production thereof.

There is thus provided in accordance with a preferred embodiment of the present invention an integrally packaged optronic integrated circuit device including:

an integrated circuit die containing at least one of a radiation emitter and radiation receiver and having top and bottom surfaces formed of electrically insulative and mechanically protective material, at least one of the surfaces being transparent to radiation, and electrically insulative edge surfaces having pads.

Preferably, the device also includes at least one spectral filter associated with a radiation transparent protective surface thereof.

Additionally in accordance with a preferred embodiment of the present invention, the device includes a semiconductor substrate which is sufficiently thin as to enable to device to be responsive to back illumination.

Preferably, the device also includes at least one color filter associated with a radiation transparent protective surface thereof.

Further in accordance with a preferred embodiment of the present invention, lenses may be integrally formed on a transparent protective surface of the device.

Additionally in accordance with a preferred embodiment of the present invention, light coupling bumps may be integrally formed on a transparent protective surface of the device.

Further in accordance with a preferred embodiment of the present invention a waveguide and other

optical components integrally formed on a transparent protective surface of the device.

Additionally in accordance with a preferred embodiment of the present invention, an optical grating may be integrally formed on a transparent protective surface of the device.

Further in accordance with a preferred embodiment of the present invention a polarizer may be formed on a transparent protective surface of the device.

There is also provided in accordance with a preferred embodiment of the present invention an integrally packaged optronic integrated circuit device including:

an integrated circuit die containing at least one of a radiation emitter and radiation receiver and having top and bottom surfaces formed of electrically insulative and mechanically protective material, at least one of the surfaces being transparent to radiation, the integrally packaged optronic integrated circuit device being characterized in that its longest dimension does not exceed the longest dimension of the die by more than 20%. Preferably the integrally packaged optronic integrated circuit device is characterized in that its longest dimension does not exceed the longest dimension of the die by more than 10%. More preferably the integrally packaged optronic integrated circuit device is characterized in that its longest dimension does not exceed the longest dimension of the die by more than 5%.

There is also provided in accordance with a preferred embodiment of the present invention a method for producing an integrally packaged optronic integrated circuit device comprising the steps of:

forming electrical circuits onto a semiconductor wafer;

forming at least one transparent mechanical protective layer onto said semiconductor wafer over said

electrical circuits;

forming solderable contacts onto said semiconductor wafer; and

thereafter, dicing said wafer into individual packaged dies.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description, taken in conjunction with the drawings in which:

Figs. 1A and 1B are respective top view and bottom view simplified pictorial illustrations of an integrally packaged optronic integrated circuit device constructed and operative in accordance with a preferred embodiment of the present invention;

Fig. 1C is a bottom view simplified pictorial illustration of an integrally packaged optronic integrated circuit device of the type shown in Figs. 1A and 1B, constructed and operative in accordance with another preferred embodiment of the present invention;

Fig. 2 is a simplified pictorial illustration of the attachment of a transparent protective packaging layer to a wafer containing a plurality of integrated circuit dies;

Fig. 3 is a simplified pictorial illustration of showing the individual dies on the wafer as seen through the transparent protective packaging layer attached thereto;

Figs. 4A, 4B, 4C and 4D are sectional illustrations of various stages in the manufacture of integrally packaged optronic integrated circuit devices in accordance with a preferred embodiment of the present invention;

Fig. 5 is a partially cut away detailed pictorial illustration of an integrally packaged optronic integrated circuit device produced from the wafer of Fig. 4D;

Figs. 6, 7A, 7B, 8A and 8B are sectional illustrations of various stages in the manufacture of the integrally packaged optronic integrated circuit device shown in Figs. 1A, 1B, 1C & 5;

Figs. 9, 10A and 10B together provide a simplified block diagram illustration of apparatus for carrying out the method of the present invention;

Figs. 11A, 11B, 11C, 11D and 11E are simplified pictorial illustrations of five alternative embodiments of an integrated circuit device constructed and operative in accordance with yet another preferred embodiment of the present invention and including spectral filters and/or anti-reflective coatings;

Figs. 12A, 12B and 12C are simplified pictorial illustrations of three alternative embodiments of an integrally packaged optronic integrated circuit device which is designed for back illumination;

Figs. 13A, 13B and 13C are simplified pictorial illustrations of three alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with still another preferred embodiment of the present invention wherein color array filters are integrated with the integrally packaged optronic integrated circuit device;

Figs. 14A, 14B, 14C and 14D are simplified pictorial illustrations of four alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with another preferred embodiment of the present invention having lenses integrally formed on a transparent protective surface thereof;

Figs. 15A and 15B are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with another preferred embodiment of the present invention having light coupling bumps integrally formed on a transparent protective surface thereof;

Figs. 16A and 16B are simplified pictorial illustrations of two alternative embodiments of an inte-

grally packaged optronic integrated circuit device constructed and operative in accordance with yet another preferred embodiment of the present invention having a waveguide and other optical components integrally formed on a transparent protective surface thereof;

Figs. 17A and 17B are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with still another preferred embodiment of the present invention wherein a polarizer is integrated with the integrally packaged optronic integrated circuit device;

Figs. 18A and 18B are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with still another preferred embodiment of the present invention wherein an optical grating is integrated with the integrally packaged optronic integrated circuit device.

Figs. 19A and 19B are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with yet another preferred embodiment of the present invention wherein the package is formed with a desired geometrical configuration;

Figs. 20A and 20B are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with yet another preferred embodiment of the present invention wherein edges of the package are coated with an opaque coating;

Fig. 21 is a simplified pictorial illustration of an integrally packaged optronic integrated circuit device constructed and operative in accordance with still another preferred embodiment of the present invention and

having an octagonal configuration; and

Fig. 22 is a simplified pictorial illustration of a cutting pattern employed to produce integrated circuits of the type shown in Fig. 21.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference is now made to Figs. 1A - 22, which illustrate the production of integrated circuit devices in accordance with a preferred embodiment of the present invention.

Figs. 1A and 1B together illustrate a preferred embodiment of integrated circuit device constructed and operative in accordance with a preferred embodiment of the present invention. The integrated circuit device includes a relatively thin and compact, environmentally protected and mechanically strengthened integrated circuit package 10 having a multiplicity of electrical contacts 12 plated along the edge surfaces 14 thereof.

In accordance with a preferred embodiment of the invention, contacts 12 extend over edge surfaces onto the planar surfaces 16 of the package. This contact arrangement permits both flat surface mounting and edge mounting of package 10 onto a circuit board. It is noted that the integrated circuit package 10 may include one or more of the following elements (not shown): an integrally formed dichroic filter, color filter, antireflective coating, polarizer, optical grating, integrated wave guide and optical coupling bumps.

Fig. 1C illustrates an alternative embodiment of the present invention wherein solderable bumps 17 are provided at the ends of each contact 12. Preferably, the solderable bumps 17 are arranged in a predetermined array.

In accordance with a preferred embodiment of the present invention, and as illustrated in Fig. 2 and Fig. 4A, a complete silicon wafer 20 having a plurality of finished dies 22 formed thereon by conventional techniques, is bonded at its active surface 24 to a radiation transparent protective insulating cover plate 26 via a layer 28 of epoxy. The insulating cover plate 26 typical-

ly comprises glass, quartz, sapphire or any other suitable radiation transparent insulative substrate.

The cover plate 26 may be colored or tinted in order to operate as a spectral filter. Alternatively, a dichroic or colored spectral filter may be formed on at least one surface of the cover plate 26.

It is a particular feature of the present invention that cover plate 26 and epoxy layer 28 are preferably transparent to radiation in a spectral region useful for optronic applications.

It is appreciated that certain steps in the conventional fabrication of silicon wafer 20 may be eliminated when the wafer is used in accordance with the present invention. These steps include the provision of via openings above pads, wafer back grinding and wafer back metal coating.

The complete silicon wafer 20 may be formed with an integral color filter array by conventional lithography techniques at any suitable location therein. Prior to the bonding step of Fig. 4A, a filter may be formed and configured by conventional techniques over the cover plate 26, such that the filter plane lies between cover plate 26 and the epoxy layer 28.

Following the bonding step described hereinabove, the silicon wafer is preferably ground down to a decreased thickness, typically 100 microns, as shown in Fig. 4B. This reduction in wafer thickness is enabled by the additional mechanical strength provided by the bonding thereof of the insulating cover plate 26.

Following the reduction in thickness of the wafer, which is optional, the wafer is etched, using a photolithography process, along its back surface along predetermined dice lines which separate the individual dies. Etched channels 30 are thus produced, which extend entirely through the thickness of the silicon substrate, typically 100 microns. The etched wafer is shown in Fig.

4C.

The aforementioned etching typically takes place in conventional silicon etching solution, such as a combination of 2.5% hydrofluoric acid, 50% nitric acid, 10% acetic acid and 37.5% water, so as to etch the silicon down to the field oxide layer, as shown in Fig. 4C.

The result of the silicon etching is a plurality of separated dies 40, each of which includes silicon of thickness about 100 microns.

As seen in Fig. 4D, following the silicon etching, a second insulating packaging layer 42 is bonded over the dies 40 on the side thereof opposite to insulating packaging layer 26. A layer 44 of epoxy lies between the dies 40 and the layer 42 and epoxy also fills the interstices between dies 40. In certain applications, such as the embodiment of Figs. 12A - 12C, the packaging layer 42 and the epoxy layer 44 are both transparent.

The sandwich of the etched wafer 20 and the first and second insulating packaging layers 26 and 42 is then partially cut along lines 50, lying along the interstices between adjacent dies 40 to define notches along the outlines of a plurality of pre-packaged integrated circuits. It is a particular feature of the invention that lines 50 are selected such that the edges of the dies along the notches are distanced from the outer extent of the silicon 40 by at least a distance d, as shown in Figs. 4D and 5, to which reference is now additionally made.

It is a particular feature of the present invention that partial cutting of the sandwich of Fig. 4D along lines 50 exposes edges of a multiplicity of pads 34 on the wafer 20, which pad edges, when so exposed, define contact surfaces 51 on dies 40.

Referring now particularly to Fig. 5, at least one insulating layer, including the field oxide layer, is shown at reference numeral 32 and metal pads are shown

at reference numeral 34. An over-metal insulating layer is shown at reference numeral 36. The color filter plane is shown at reference numeral 38.

Reference is now made to Figs. 6, 7A, 7B, 8A and 8B, which illustrate further steps in the manufacture of integrated circuit devices in accordance with a preferred embodiment of the present invention.

Fig. 6 illustrates at reference numeral 54, a preferred cross sectional configuration of a notch produced by partially cutting as described hereinabove in connection with Fig. 5. Vertical lines 56 indicate the intersection of the notch 54 with the pads 34, defining exposed sectional pad surfaces 51. Vertical lines 58 indicate the location of a subsequent final cut which separates the dies into individual integrated circuits at a later stage.

Figs. 7A and 7B illustrate the formation of metal contacts 12 along the inclined edges 14 and part of the top surface 16. These contacts, which may be formed by any suitable metal deposition technique, are seen to extend inside notch 54, thus establishing electrical contact with surfaces 51 of pads 34. Fig. 7A shows a configuration corresponding to that of Figs. 1A and 1B without solderable bumps, while Fig. 7B shows the provision of solderable bumps 17 on contacts 12, as illustrated in Fig. 1C.

It is a particular feature of the present invention that metal contacts are formed onto the dies in electrical contact with surfaces 51 of pads 34 without first separating the dies into individual chips.

Figs. 8A and 8B illustrate subsequent dicing of the individual dies on the wafer, subsequent to metal contact formation thereon, into individual pre-packaged integrated circuit devices. Fig. 8A shows a configuration corresponding to that of Figs. 1A and 1B without solderable bumps, while Fig. 8B shows the provision of

solderable bumps 17 on contacts 12, as illustrated in Fig. 1C.

Reference is now made to Figs. 9, 10A and 10B, which together illustrate apparatus for producing integrated circuit devices in accordance with a preferred embodiment of the present invention. A conventional wafer fabrication facility 180 provides complete wafers 20. Individual wafers 20 are bonded on their active surfaces to protective layers, such as glass layers 26, using epoxy 28, by bonding apparatus 182, preferably having facilities for rotation of the wafer 20, the layer 26 and the epoxy 28 so as to obtain even distribution of the epoxy.

The bonded wafer (Fig. 3) is thinned at its non-active surface as by grinding apparatus 184, such as Model 32BTGW using 12.5A abrasive, which is commercially available from Speedfam Machines Co. Ltd. of England.

The wafer is then etched at its non-active surface, preferably by photolithography, such as by using conventional spin-coated photoresist, which is commercially available from Hoechst, under the brand designation AZ 4562.

The photoresist is preferably mask exposed by a suitable UV exposure system 185, such as a Karl Suss Model KSMA6, through a lithography mask 186 to define etched channels 30.

The photoresist is then developed in a development bath (not shown), baked and then etched in a silicon etch solution 190 located in a temperature controlled bath 188. Commercially available equipment for this purpose include a Chemkleen bath and an WHRV circulator both of which are manufactured by Wafab Inc. of the U.S.A.. A suitable conventional silicon etching solution is Isoform Silicon etch, which is commercially available from Micro-Image Technology Ltd. of England. The wafer is conventionally rinsed after etching. The resulting etched

wafer is shown in Fig. 4C.

Alternatively, the foregoing wet chemical etching step may be replaced by dry plasma etching.

The etched wafer is bonded on the non-active side to another protective layer 42 by bonding apparatus 192, which may be essentially the same as apparatus 182, to produce a doubly bonded wafer sandwich as shown in Fig. 4D.

Notching apparatus 194 partially cuts the bonded wafer sandwich of Fig. 4D to a configuration shown in Fig. 5.

The notched wafer is then subjected to anti-corrosion treatment in a bath 196, containing a chromating solution 198, such as described in any of the following U.S. Patents: 2,507,956; 2,851,385 and 2,796,370, the disclosure of which is hereby incorporated by reference.

Conductive layer deposition apparatus 200, which operates by vacuum deposition techniques, such as a Model 903M sputtering machine manufactured by Material Research Corporation of the U.S.A., is employed to produce a conductive layer on one or more surfaces of each die of the wafer as shown in Fig. 7.

Configuration of contact strips, as shown in Fig. 7, is carried out preferably by using conventional electro-deposited photoresist, which is commercially available from DuPont under the brand name Primecoat or from Shipley, under the brand name Eagle. The photoresist is applied to the wafers in a photoresist bath assembly 202 which is commercially available from DuPont or Shipley.

The photoresist is preferably light configured by a UV exposure system 204, which may be identical to system 185, using a mask 205 to define suitable etching patterns. The photoresist is then developed in a development bath 206, and then etched in a metal etch solution 208 located in an etching bath 210, thus providing a

conductor configuration such as that shown in Figs. 1A and 1B.

The exposed conductive strips shown in Fig. 7 are then plated, preferably by electroless plating apparatus 212, which is commercially available from Okuno of Japan.

The wafer is then diced into individual prepackaged integrated circuit devices. Preferably the dicing blade 214 should be a diamond resinoid blade of thickness 4 - 12 mils. The resulting dies appear as illustrated generally in Figs. 1A and 1B.

Fig. 10A shows apparatus for producing an integrated circuit configuration corresponding to that of Figs. 1A and 1B without solderable bumps, while Fig. 10B shows apparatus for producing an integrated circuit configuration corresponding to that of Fig. 1C having solderable bumps. The embodiment of Fig. 10B is identical to that of Fig. 10A, apart from the additional provision of bump forming apparatus 213 downstream of the electroless plating apparatus 212.

Reference is now made to Figs. 11A - 11E, which illustrate five alternative preferred embodiments of integrated circuit device constructed and operative in accordance with another preferred embodiment of the present invention and includes a relatively thin and compact, environmentally protected and mechanically strengthened integrated circuit package 310 having a multiplicity of electrical contacts 312 plated along the edge surfaces 314 thereof.

Fig. 11A shows a dichroic filter and/or anti-reflective coating 315 formed on an outer facing surface 316 of a transparent protective layer 317. Fig. 11B illustrates a coating 318, which may be identical to coating 315, which is formed on an inner facing surface 319 of transparent protective layer 317. Fig. 11C shows both coatings 315 and 318 on respective surfaces 316 and

319 of transparent protective layer 317. Optronic components are formed on a surface 320 of a silicon substrate 322 of conventional thickness, typically 100 microns. Surface 320 faces transparent protective layer 317.

Fig. 11D shows an absorption filter 323 formed on outer facing surface 316 of transparent protective layer 317. Fig. 11E shows an absorption filter 323, having formed thereon an anti-reflective coating 324, formed on outer facing surface 316 of transparent protective layer 317.

Reference is now made to Figs. 12A - 12C, which illustrate three alternative preferred embodiments of integrated circuit device which include a relatively thin and compact, environmentally protected and mechanically strengthened integrated circuit package 330 having a multiplicity of electrical contacts 332 plated along the edge surfaces 334 thereof.

In contrast to the embodiments of Figs. 11A - 11E, the integrated circuit devices of Figs. 12A - 12C are designed for back illumination and therefore employ a thinned silicon substrate 336, typically having a thickness of 12 - 15 microns.

Whereas in the embodiment of Figs. 11A - 11E, the optronic components are formed on a surface 320 which faces a transparent protective layer 317, in the embodiment of Figs. 12A - 12B, the components may be formed on a surface 340 of substrate 336, which surface 340 faces away from the corresponding transparent protective layer 337. The extreme thickness of the substrate 336 in the embodiments of Figs. 12A - 12C enables the optronic components on surface 340 to be exposed to light impinging via transparent protective layer 337 by back exposure.

It is appreciated that silicon is transparent to certain radiation spectra, such as IR radiation. When

an IR responsive device is provided, the embodiment of Figs. 12A - 12C can be constructed without a thinned silicon substrate.

Fig. 12A shows a dichroic filter and/or anti-reflective coating 345 formed on an outer facing surface 346 of the transparent protective layer 337. Fig. 12B illustrates a coating 348, which may be identical to coating 345, which is formed on an inner facing surface 349 of transparent protective layer 337. Fig. 12C shows both coatings 345 and 348 on respective surfaces 346 and 349 of transparent protective layer 337.

The modifications shown in Figs. 11D and 11E may also be embodied in the configuration of Figs. 12A - 12C.

Reference is now made to Figs. 13A, 13B and 13C, which illustrate three alternative preferred embodiments of integrated circuit device constructed and operative in accordance with another preferred embodiment of the present invention and includes a relatively thin and compact, environmentally protected and mechanically strengthened integrated circuit package 350 having a multiplicity of electrical contacts 352 plated along the edge surfaces 354 thereof.

Fig. 13A shows a color filter, such as an RGB or masking filter, 355 formed on an outer facing surface 356 of a transparent protective layer 357. Fig. 13B illustrates a filter 358, which may be identical to filter 355, which is formed on an outer facing surface 359 of a silicon substrate 362. Fig. 13C shows both filters 355 and 358 on respective surfaces 356 and 359.

It is appreciated that filter 356 may alternatively be located on an inner facing surface of transparent protective layer 357.

Reference is now made to Figs. 14A, 14B, 14C and 14D, which illustrate four alternative embodiments of an integrally packaged optronic integrated circuit device

constructed and operative in accordance with another preferred embodiment of the present invention having lenses integrally formed on a transparent protective surface thereof.

The embodiment of Fig. 14A may be identical to that of Fig. 11A without the coating and is further distinguished therefrom in that it has a transparent protective layer 370 which is formed with an array of microlenses 372 on an outer facing surface 374 thereof.

The embodiment of Fig. 14B may be identical to that of Fig. 12A without the coating and is further distinguished therefrom in that it has a transparent protective layer 380 which is formed with an array of microlenses 382 on an outer facing surface 384 thereof.

In the illustrated embodiment of Figs. 14A and 14B, the microlenses 372 and 382 respectively are formed of the same material as than of transparent protective layers 370 and 380 respectively. Alternatively, microlenses 372 and 382 may be formed of a material different from that of respective transparent protective layers 370 and 380.

The embodiment of Fig. 14C corresponds to that of Fig. 14A. However in the embodiment of Fig. 14C, an array of microlenses 385 is formed on an inner facing surface of transparent protective layer 370. In the illustrated embodiment of Fig. 14C, the microlenses 385 are formed of a different material than of transparent protective layer 370. Alternatively, microlenses 385 may be formed of the same material as that of transparent protective layer 370.

The embodiment of Fig. 14D corresponds to that of Fig. 14B. However in the embodiment of Fig. 14D, similarly to the embodiment of Fig. 14C, an array of microlenses 387 is formed on an inner facing surface of transparent protective layer 380. In the illustrated embodiment of Fig. 14D, the microlenses 387 are formed of

a different material than of transparent protective layer 380. Alternatively, microlenses 387 may be formed of the same material as that of transparent protective layer 380.

In the embodiments of Figs. 14C and 14D, the index of refraction of the microlenses 385 and 387 respectively must exceed that of an epoxy layer 388 underlying them.

Reference is now made to Figs. 15A and 15B, which are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with another preferred embodiment of the present invention having light coupling bumps integrally formed on a transparent protective surface thereof.

The embodiment of Fig. 15A may be identical to that of Fig. 11A without the coating and is further distinguished therefrom in that it has a light coupling bump 390 formed on a transparent protective layer 392. A waveguide 394 is shown optically coupled to the transparent protective layer 392 via bump 390. Preferably the bump 390 is formed of a transparent organic material which is somewhat compliant such that mechanical pressure produces a slight deformation thereof and enables an evanescent light wave to pass through an interface defined therewith.

The embodiment of Fig. 15B may be identical to that of Fig. 12A without the coating and is further distinguished therefrom in that it has a light coupling bump 396 formed on a transparent protective layer 398. A waveguide 399 is shown optically coupled to the transparent protective layer 398 via bump 396.

Reference is now made to Figs. 16A and 16B which are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in

accordance with yet another preferred embodiment of the present invention having a waveguide and other optical components integrally formed on a transparent protective surface thereof.

The embodiment of Fig. 16A may be identical to that of Fig. 11A without the coating and is further distinguished therefrom in that it has a wave guide 400 and possibly other optical elements (not shown) formed on a transparent protective layer 402, as by conventional integrated optics techniques. This arrangement enables optical communication between an optronic component formed on a silicon substrate 404 via the transparent protective layer 402 and the wave guide 400.

The embodiment of Fig. 16B may be identical to that of Fig. 12A without the coating and is further distinguished therefrom in that it has a wave guide 410 and possibly other optical elements (not shown) formed on a transparent protective layer 412, as by conventional integrated optics techniques. This arrangement enables optical communication between an optronic component formed on a silicon substrate 414 via the transparent protective layer 412 and the wave guide 410.

Reference is now made to Figs. 17A and 17B, which are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with still another preferred embodiment of the present invention wherein a polarizer is integrated with the integrally packaged optronic integrated circuit device.

The embodiment of Fig. 17A may be identical to that of Fig. 11A without the coating and is further distinguished therefrom in that it has a polarizer 420 which is on an outer facing surface 422 of a transparent protective layer 424.

The embodiment of Fig. 17B may be identical to

that of Fig. 12A without the coating and is further distinguished therefrom in that it has a polarizer 430 which is on an outer facing surface 432 of a transparent protective layer 434.

Reference is now made to Figs. 18A and 18B, which are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optronic integrated circuit device constructed and operative in accordance with still another preferred embodiment of the present invention wherein an optical grating is integrated with the integrally packaged optronic integrated circuit device.

The embodiment of Fig. 18A may be identical to that of Fig. 11A without the coating and is further distinguished therefrom in that it has a transparent protective layer 440 which is formed with an optical grating 442 on an outer facing surface 444 thereof.

The embodiment of Fig. 18B may be identical to that of Fig. 12A without the coating and is further distinguished therefrom in that it has a transparent protective layer 450 which is formed with an optical grating 452 on an outer facing surface 454 thereof.

Reference is now made to Figs. 19A and 19B which may be generally similar in all relevant respects to respective Figs. 11A and 12A respectively. The embodiment of Figs. 19A and 19B is characterized in that a transparent protective layer 460 is provided with a particular edge configuration, preferably to enable it to be located in an aperture. In Figs. 19A and 19B, the transparent protective layer 460 is shown with a peripheral edge defining a step 462. It is appreciated that any other suitable configuration may also be provided for the transparent protective layer 460.

Reference is now made to Figs. 20A and 20B, which are simplified pictorial illustrations of two alternative embodiments of an integrally packaged optron-

ic integrated circuit device constructed and operative in accordance with yet another preferred embodiment of the present invention wherein edges of the package are coated with an opaque coating.

The embodiment of Fig. 20A may correspond to that of Fig. 19A wherein the transparent protective layer 460 may be provided with an opaque coating 464 at its peripheral edge which may cover step 462 and may also cover the edge of the outer facing surface adjacent thereto.

The embodiment of Fig. 20B may correspond generally to that of Fig. 11A wherein a transparent protective layer 470 may be provided with an opaque coating 472 at its peripheral edge which may also cover the edge of the outer facing surface adjacent thereto.

Reference is now made to Fig. 21, which is a simplified pictorial illustration of an integrally packaged optronic integrated circuit device constructed and operative in accordance with still another preferred embodiment of the present invention and having an octagonal configuration. This configuration is preferred for compact applications, such as endoscopes which a high density of focal plane sensors and electronics is required.

Fig. 22 is a simplified pictorial illustration of a cutting pattern employed to produce integrated circuits of the type shown in Fig. 21. The cutting pattern of Fig. 22, which is shown overlaid on a wafer 480, comprises six consecutive cuts for each die.

It will be appreciated by persons skilled in the art that the present invention is not limited to what has been particularly shown and described hereinabove. Rather the scope of the present invention includes both combinations and subcombinations of the various features described hereinabove as well as modifications and variations thereof as would occur to a person of skill in

the art upon reading the foregoing specification and which are not in the prior art.

C L A I M S

1. An integrally packaged optronic integrated circuit device including:

an integrated circuit die containing at least one of a radiation emitter and radiation receiver and having top and bottom surfaces formed of electrically insulative and mechanically protective material, at least one of the surfaces being transparent to radiation, and electrically insulative edge surfaces having pads.

2. An integrally packaged optronic integrated circuit device according to claim 1 and also including at least one spectral filter associated with a radiation transparent protective surface thereof.

3. An integrally packaged optronic integrated circuit device according to claim 1 or claim 2 and including a semiconductor substrate which is sufficiently thin as to enable the device to be responsive to back illumination.

4. An integrally packaged optronic integrated circuit device according to any of the preceding claims and also including color array filters.

5. An integrally packaged optronic integrated circuit device according to any of the preceding claims and also having lenses integrally formed on a transparent protective surface thereof.

6. An integrally packaged optronic integrated circuit device according to any of the preceding claims and also including light coupling bumps formed on a transparent protective surface thereof.

7. An integrally packaged optronic integrated circuit device according to any of the preceding claims and also including a waveguide and other optical components integrally formed on a transparent protective surface thereof.

8. An integrally packaged optronic integrated circuit device according to any of the preceding claims and also including an optical grating formed onto a transparent protective surface thereof.

9. An integrally packaged optronic integrated circuit device according to any of the preceding claims and also including a polarizer integrated therewith.

10. An integrally packaged optronic integrated circuit device including:

an integrated circuit die containing at least one of a radiation emitter and radiation receiver and having top and bottom surfaces formed of electrically insulative and mechanically protective material, at least one of the surfaces being transparent to radiation, said integrally packaged optronic integrated circuit device being characterized in that its longest dimension does not exceed the longest dimension of the die by more than 20%.

11. An integrally packaged optronic integrated circuit device according to claim 10 and being characterized in that its longest dimension does not exceed the

longest dimension of the die by more than 10%.

12. An integrally packaged optronic integrated circuit device according to claim 10 and being characterized in that its longest dimension does not exceed the longest dimension of the die by more than 5%.

13. An integrally packaged optronic integrated circuit device according to claim 5 and wherein said lenses are formed of the same material as that of the transparent protective surface.

14. An integrally packaged optronic integrated circuit device according to claim 5 and wherein said lenses are not formed of the same material as that of the transparent protective surface.

15. An integrally packaged optronic integrated circuit device according to any of claims 5, 13 and 14 and wherein said lenses are formed on an outer facing surface of the transparent protective surface.

16. An integrally packaged optronic integrated circuit device according to any of claims 5, 13 and 14 and wherein said lenses are formed on an inner facing surface of the transparent protective surface.

17. An integrally packaged optronic integrated circuit device according to any of the preceding claims and wherein said circuit device is formed with an octagonal shape.

18. A method for producing an integrally packaged optronic integrated circuit device comprising the steps of:

forming electrical circuits onto a semiconductor wafer;

forming at least one transparent mechanical protective layer onto said semiconductor wafer over said electrical circuits;

forming solderable contacts onto said semiconductor wafer; and

thereafter, dicing said wafer into individual packaged dies.

19. Apparatus according to any of the preceding claims, substantially as shown and described hereinabove.

20. Apparatus according to any of the preceding claims, substantially as illustrated in any of the drawings.

21. A method, substantially as shown and described hereinabove.

22. A method, substantially as illustrated in any of the drawings.

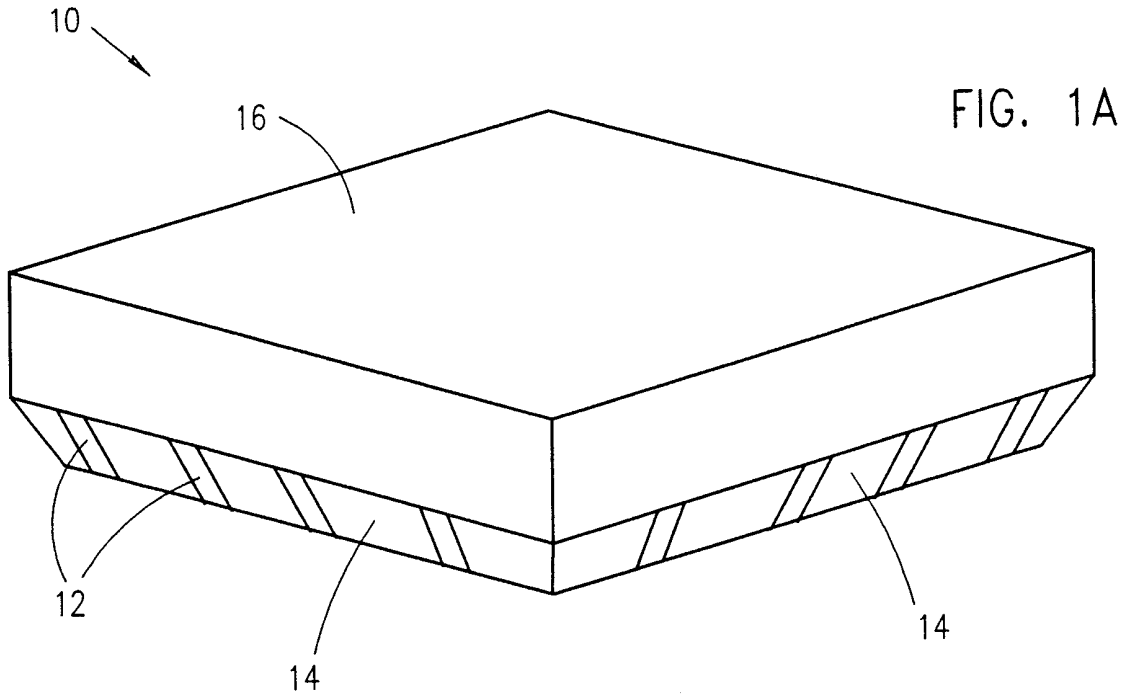


FIG. 1A

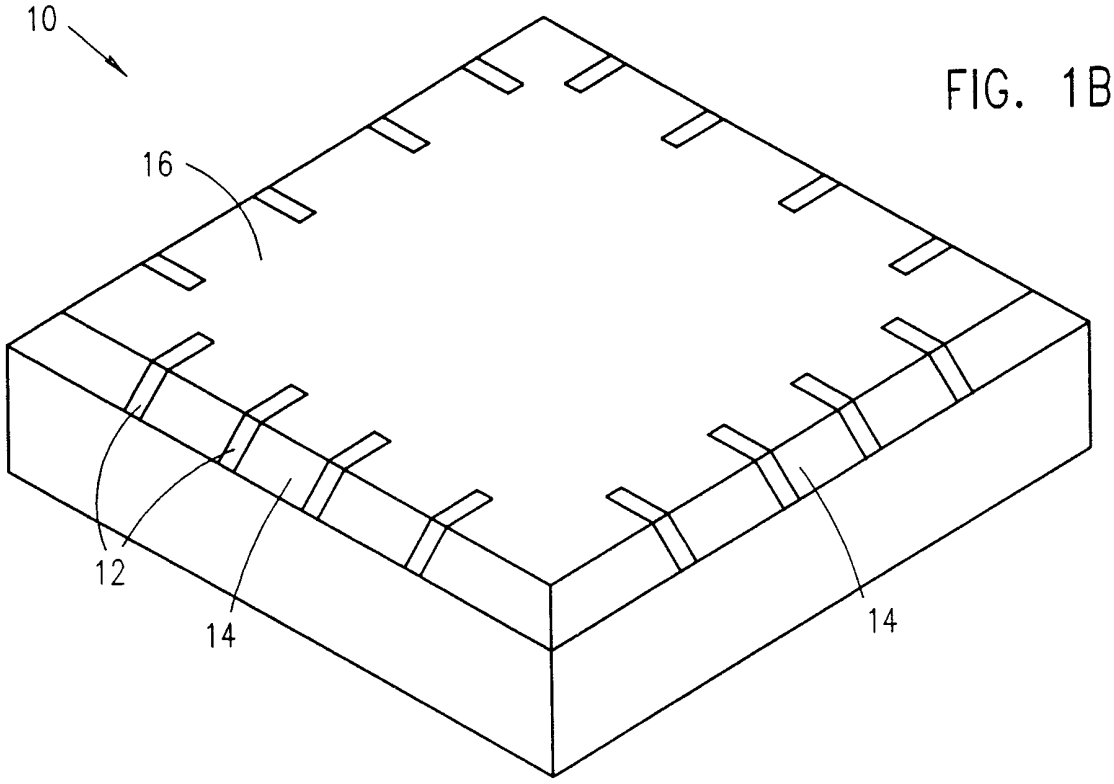


FIG. 1B

FIG. 1C

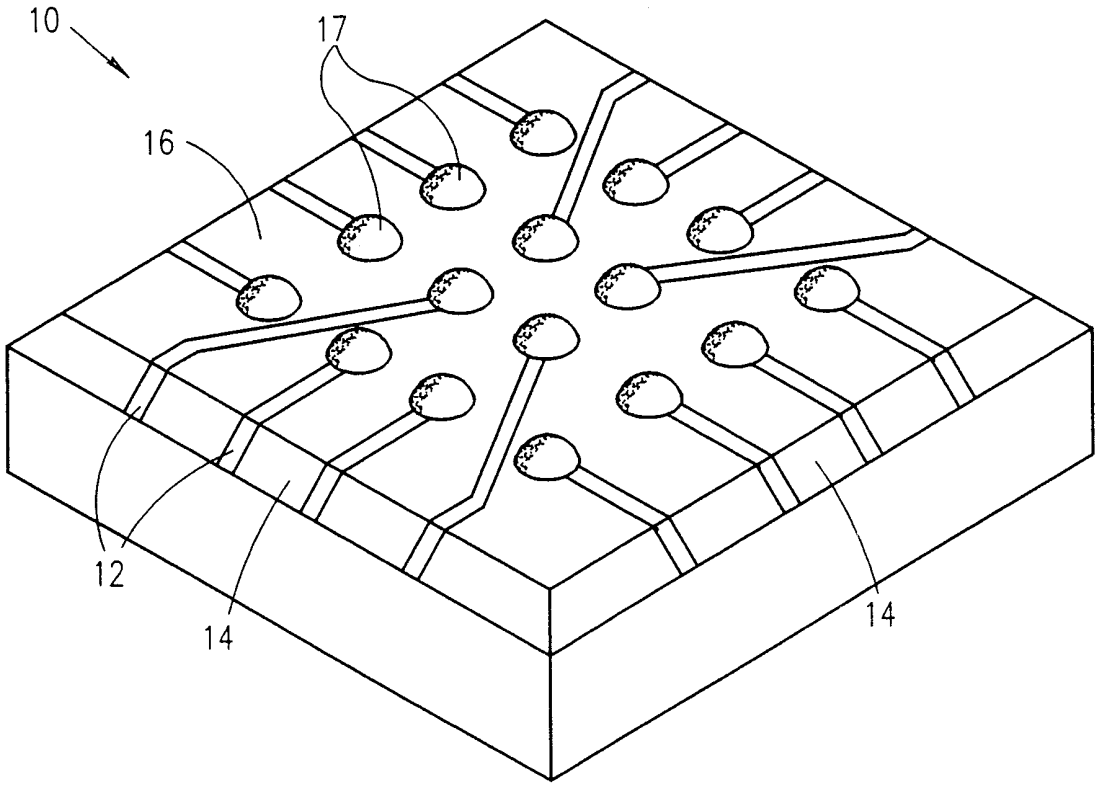


FIG. 2

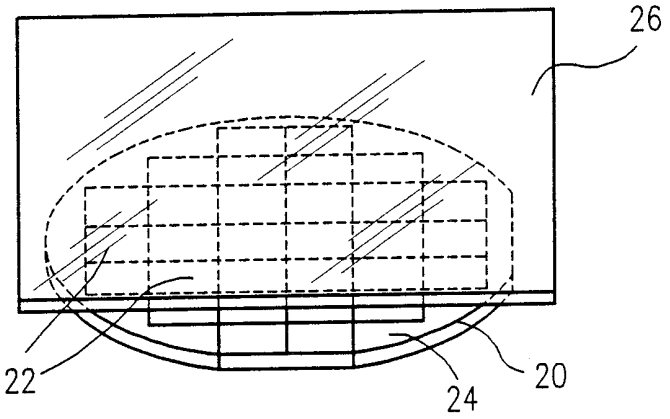
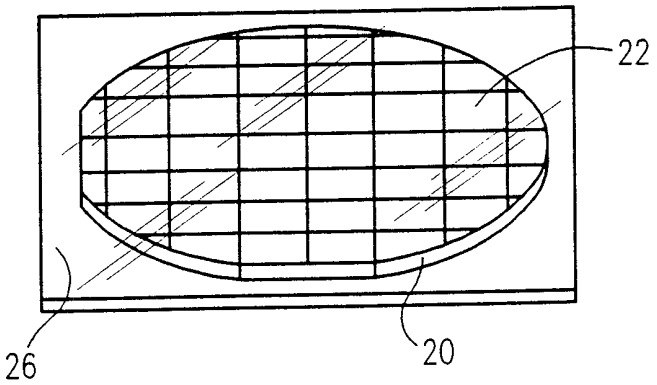


FIG. 3



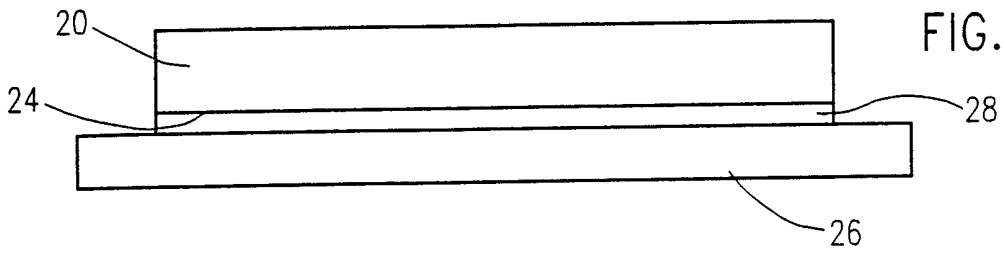


FIG.4A

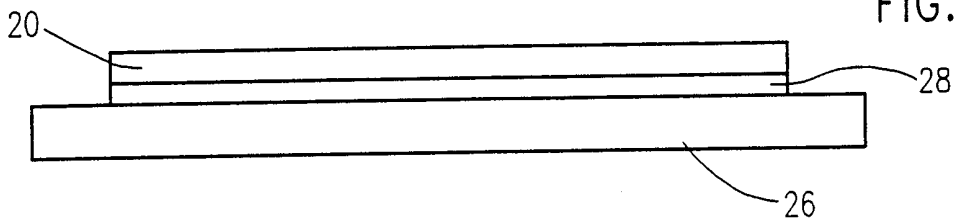


FIG.4B

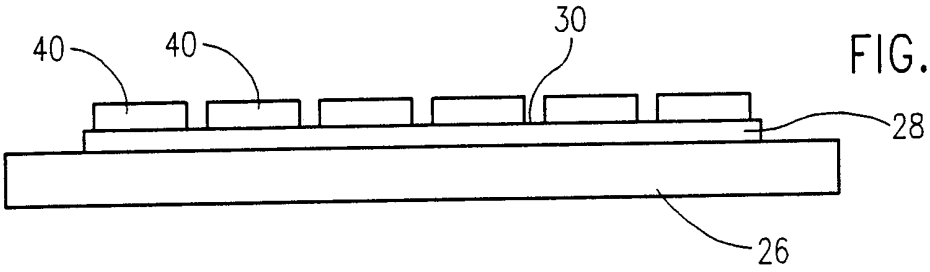


FIG.4C

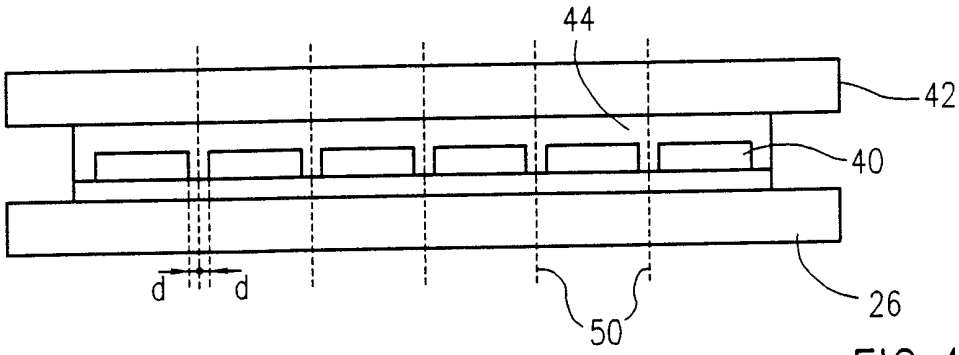


FIG.4D

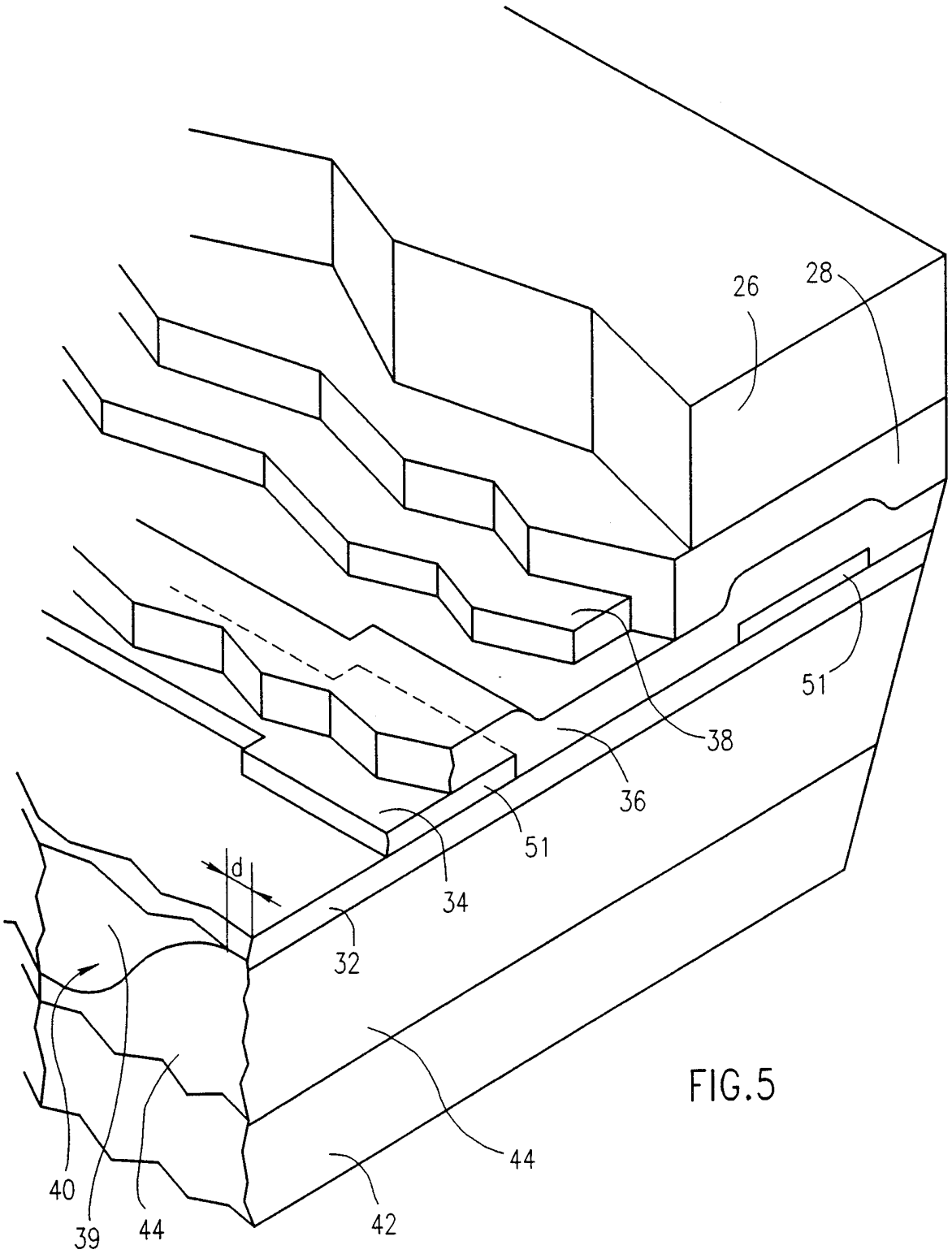


FIG.5

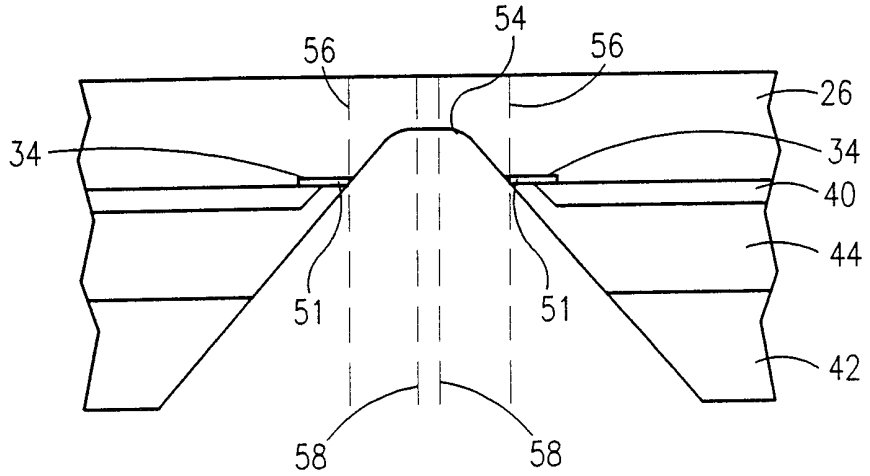


FIG. 6

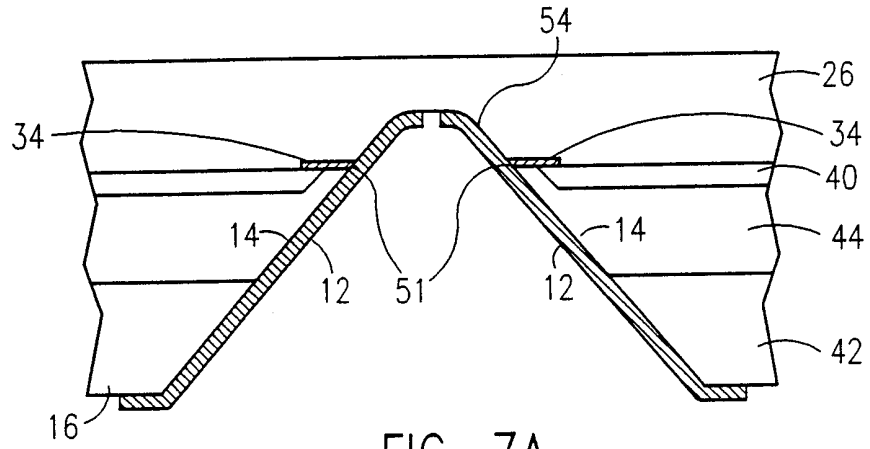


FIG. 7A

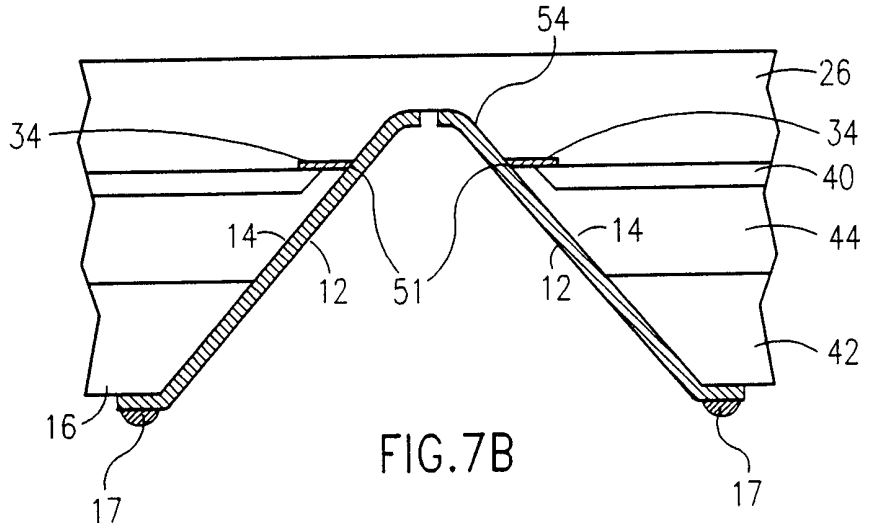


FIG.7B

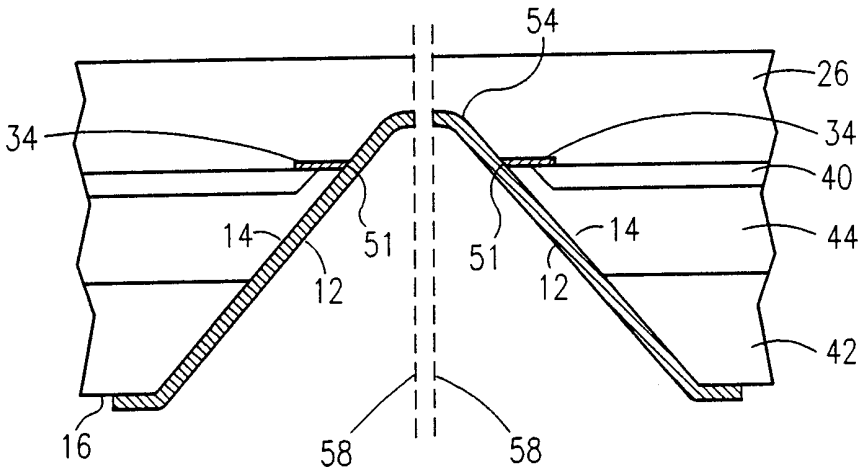

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FIG. 8A

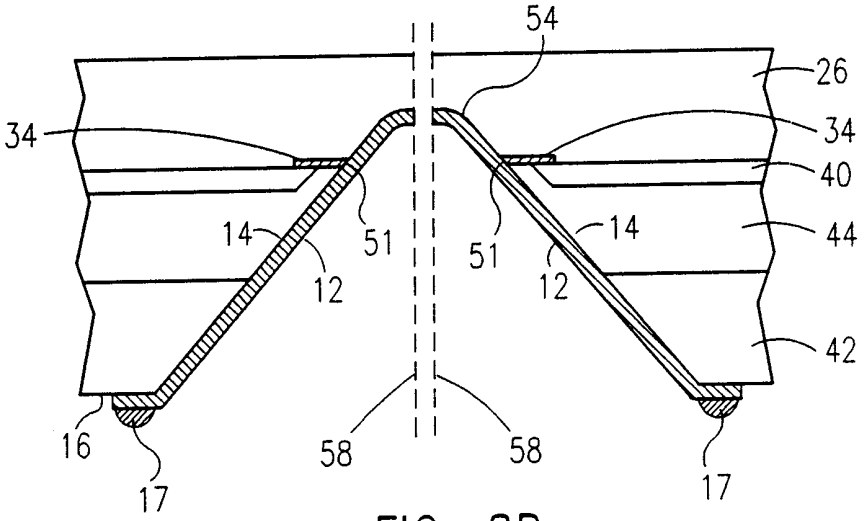
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FIG. 8B

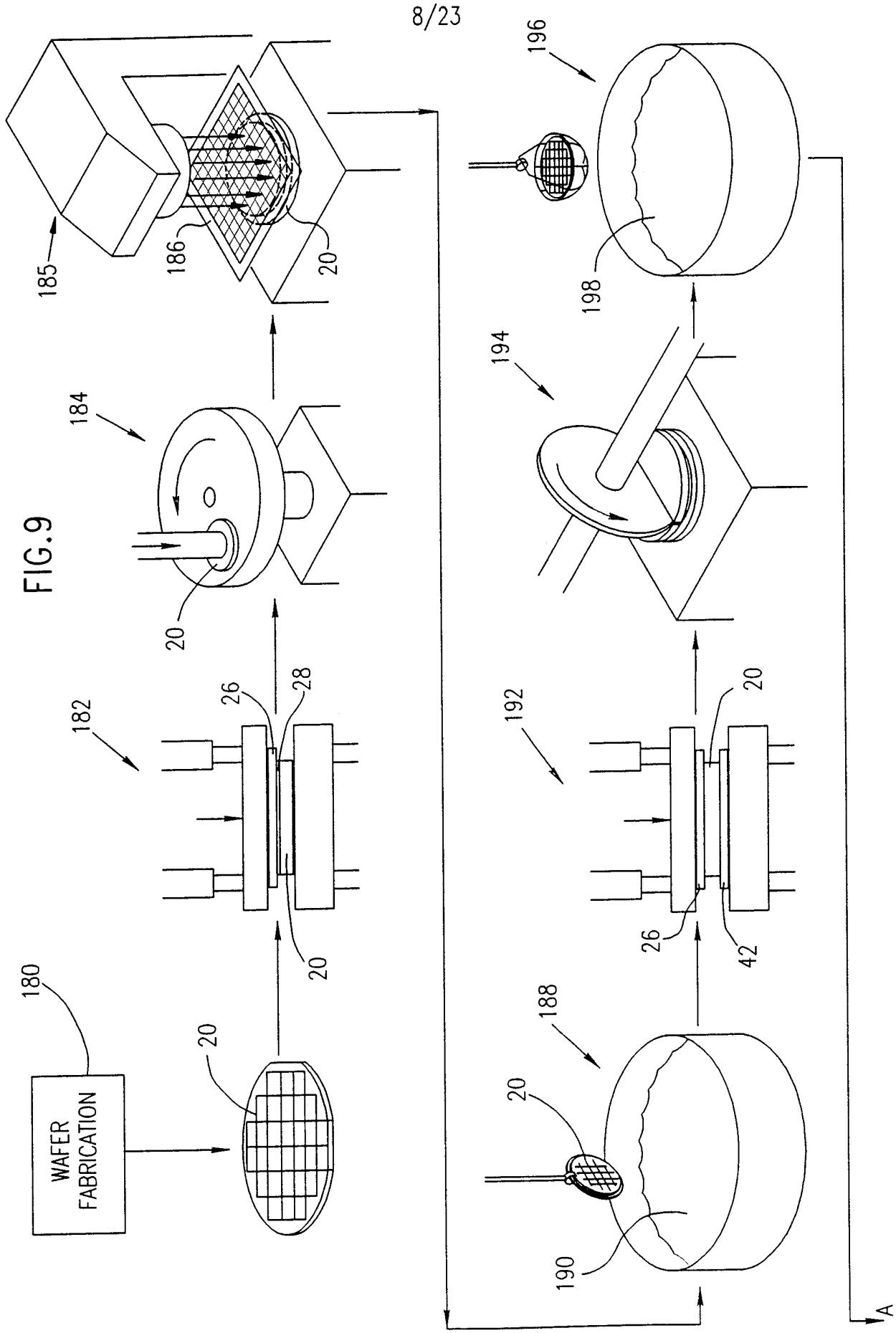
WAFER FABRICATION
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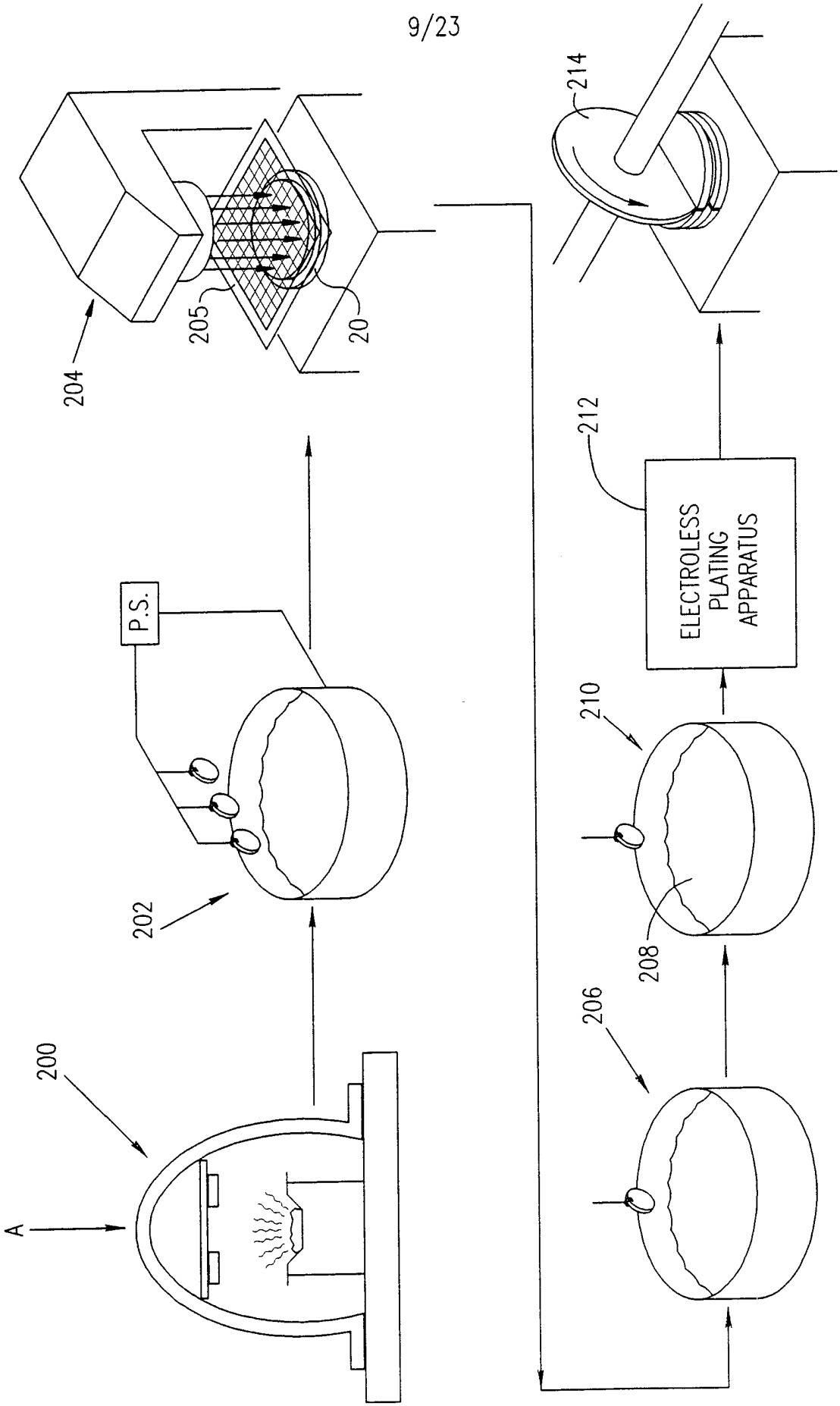
FIG. 9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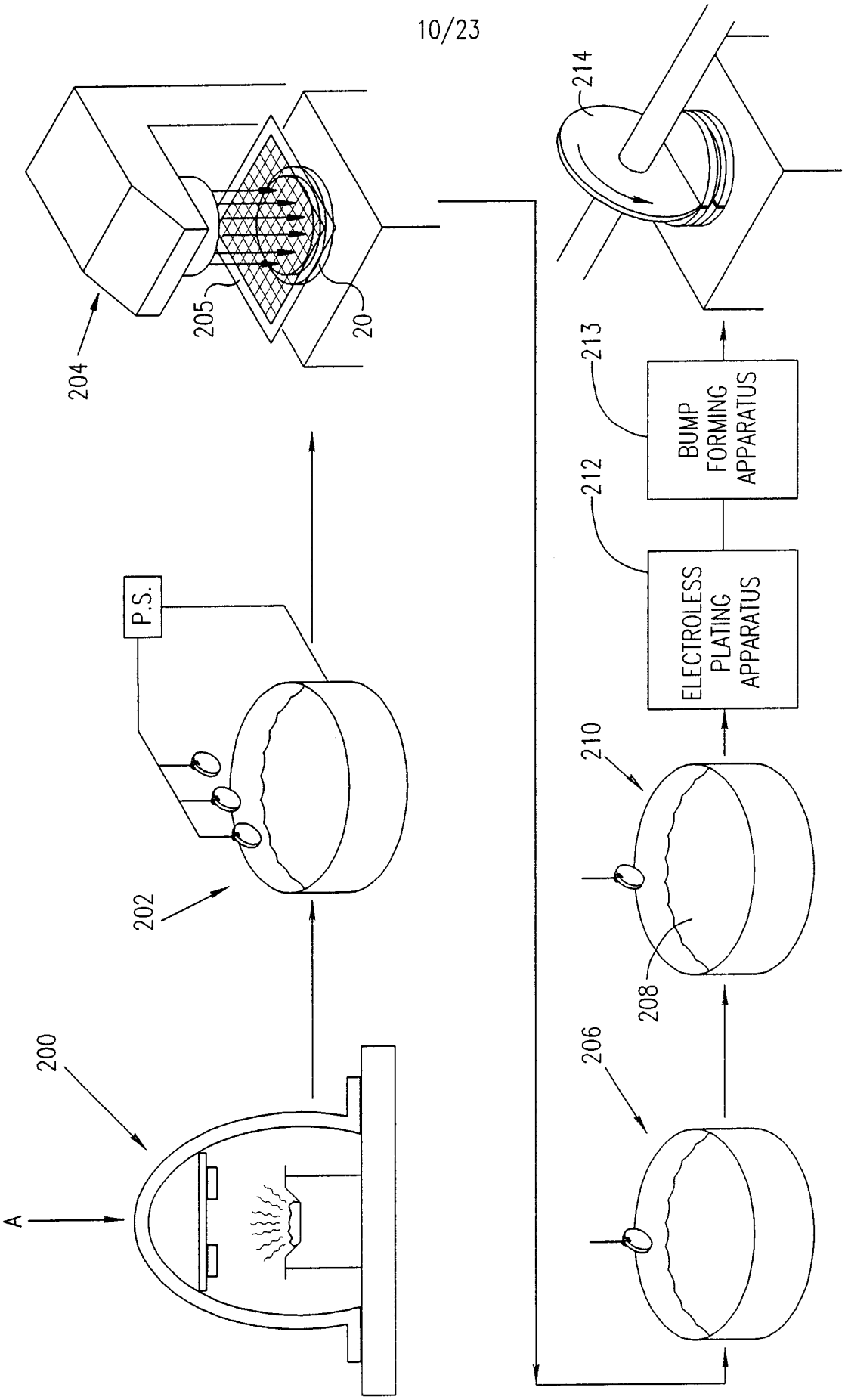
212
ELECTROLESS PLATING APPARATUS
214

FIG. 10A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ELECTROLESS PLATING APPARATUS
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BUMP FORMING APPARATUS
214

FIG. 10B

FIG. 11A

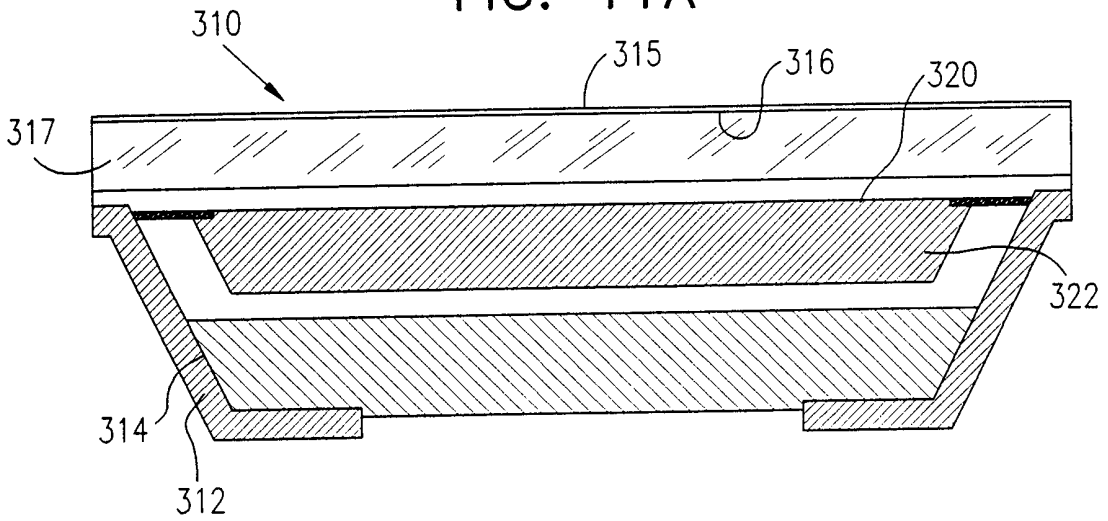


FIG. 11B

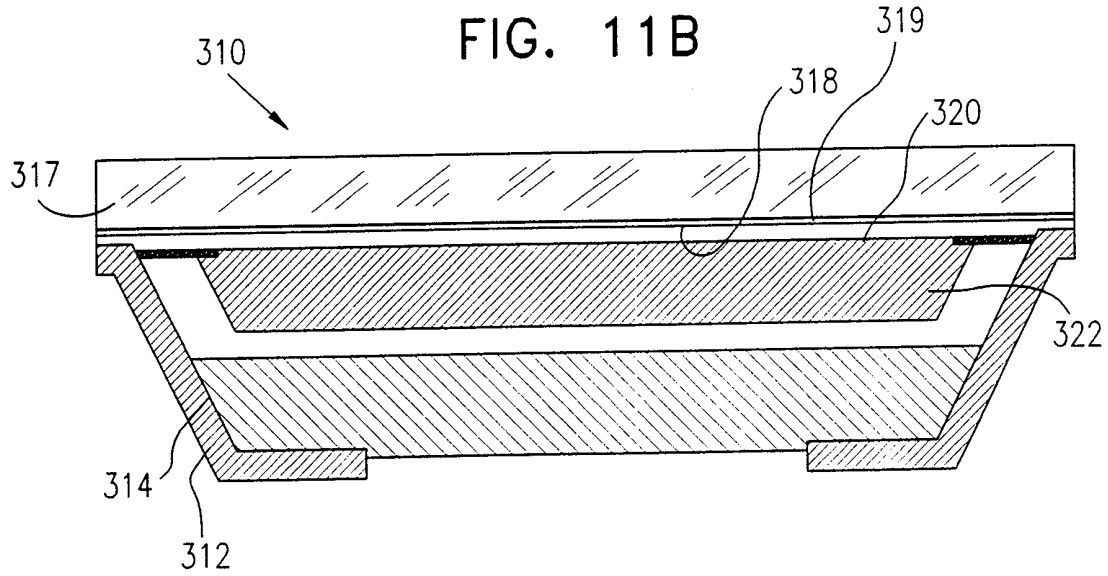


FIG. 11C

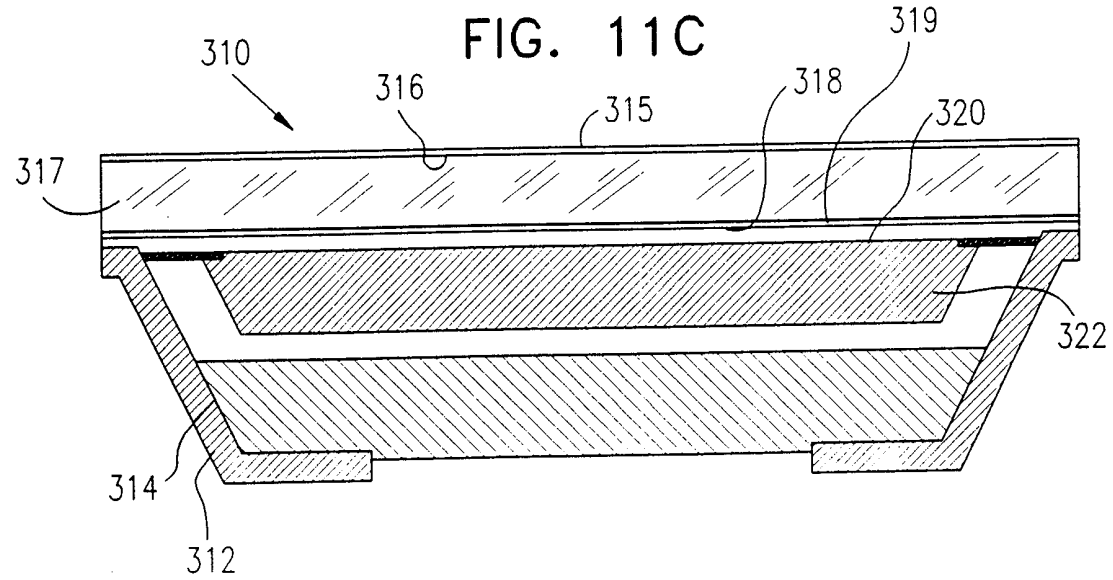


FIG. 11D

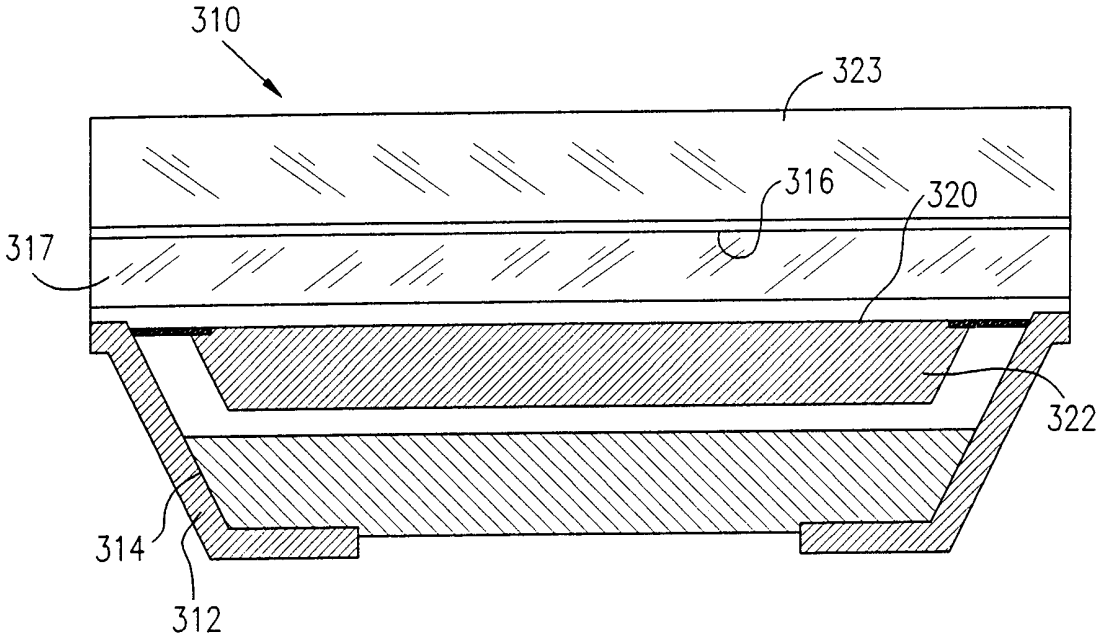


FIG. 11E

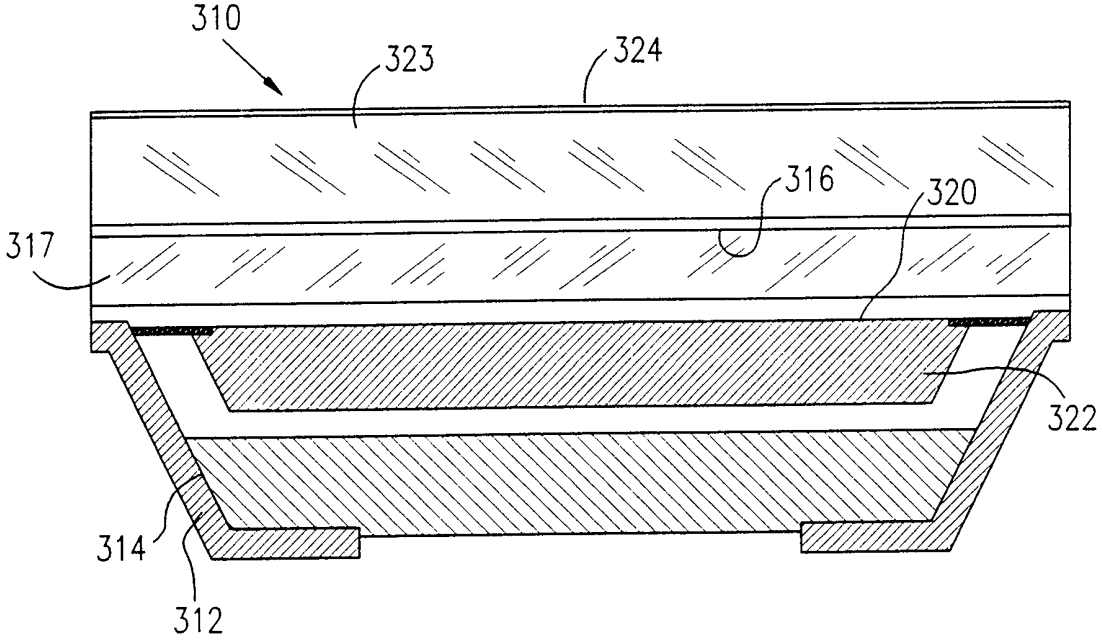


FIG. 12A

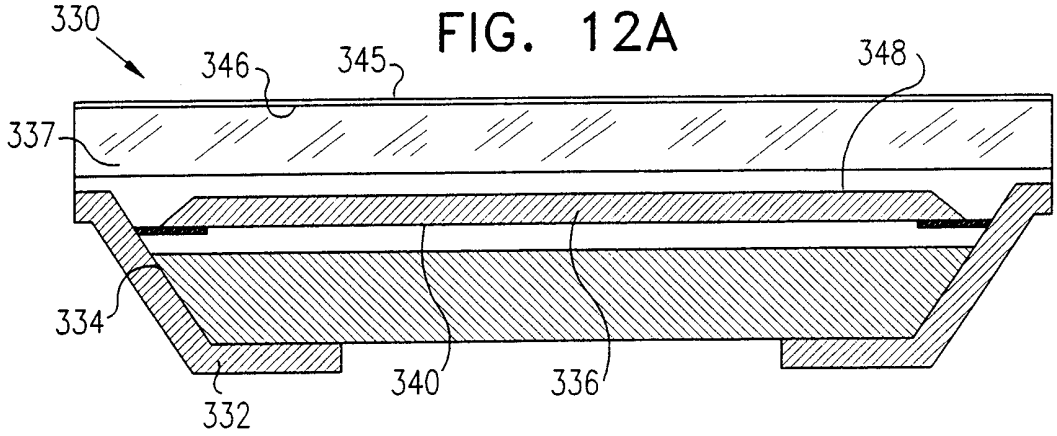


FIG. 12B

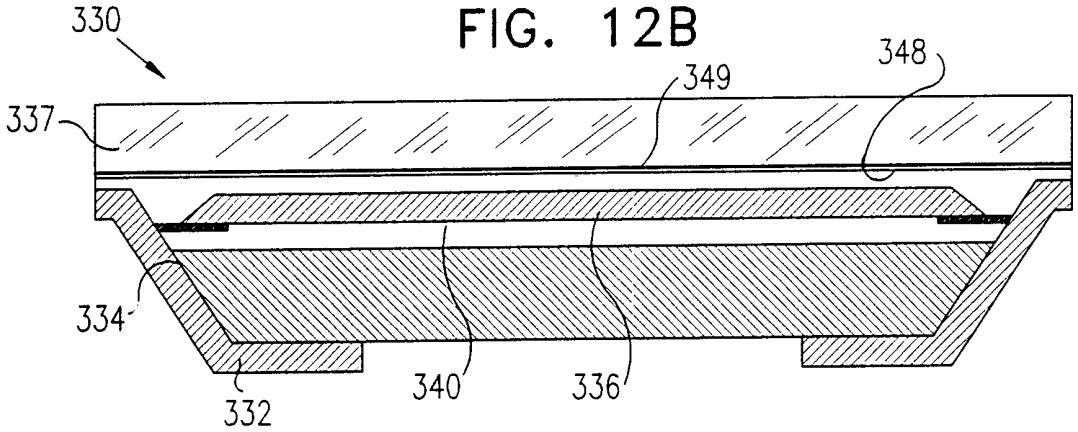


FIG. 12C

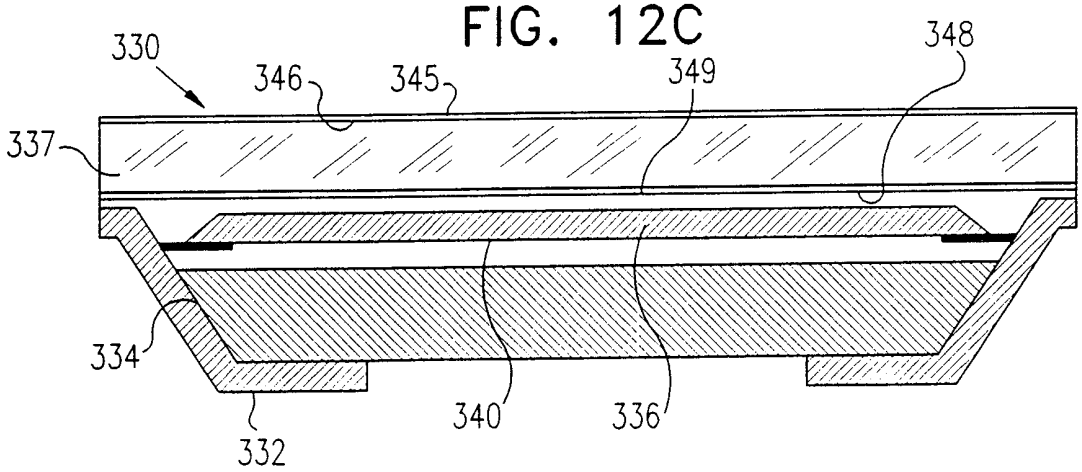


FIG. 13A

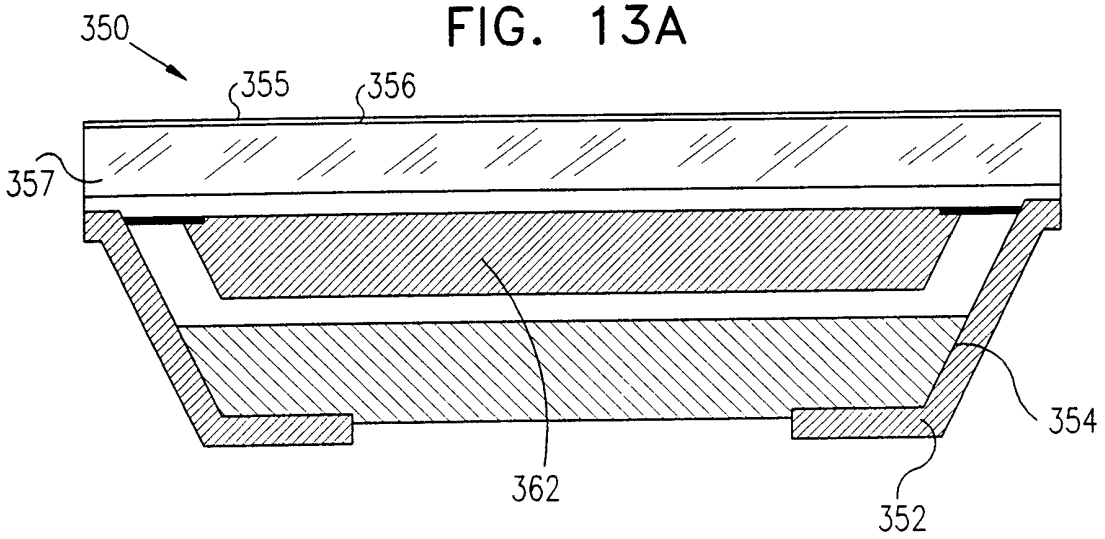


FIG. 13B

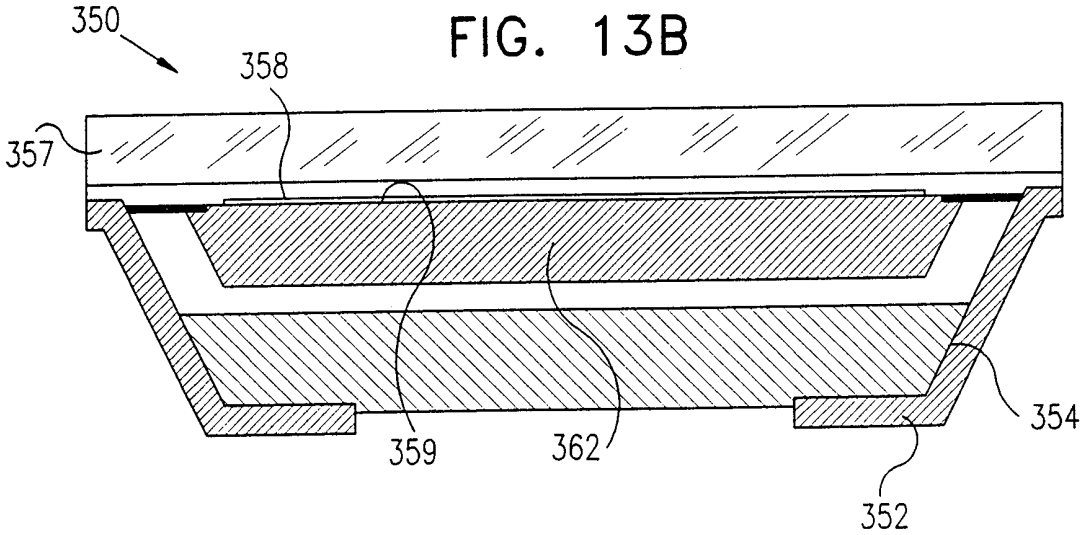


FIG. 13C

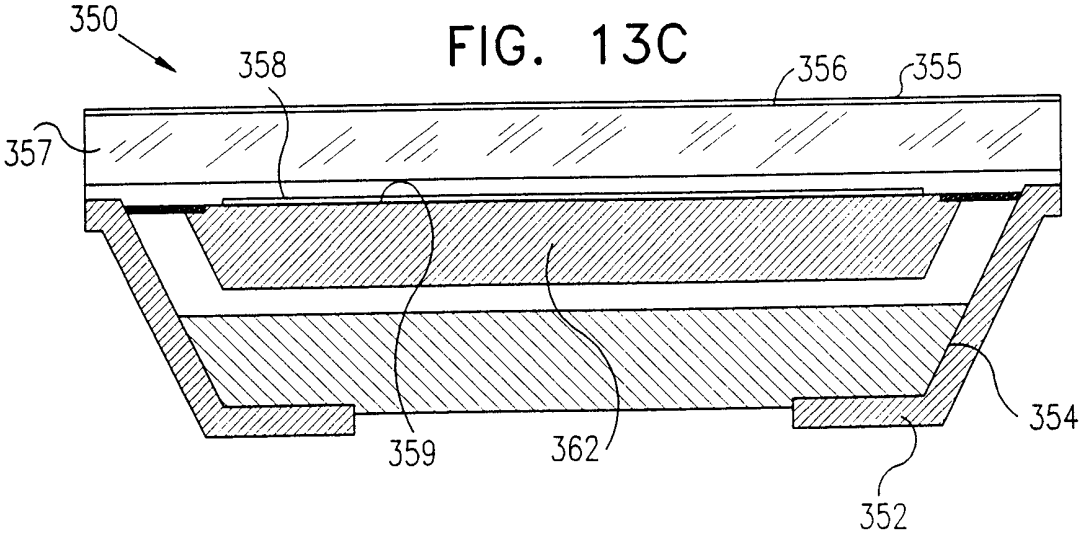


FIG. 14A

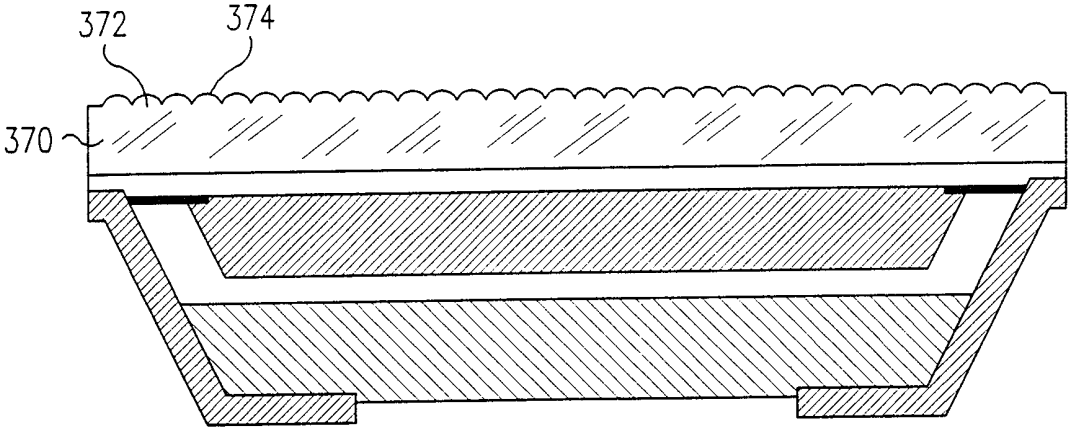


FIG. 14B

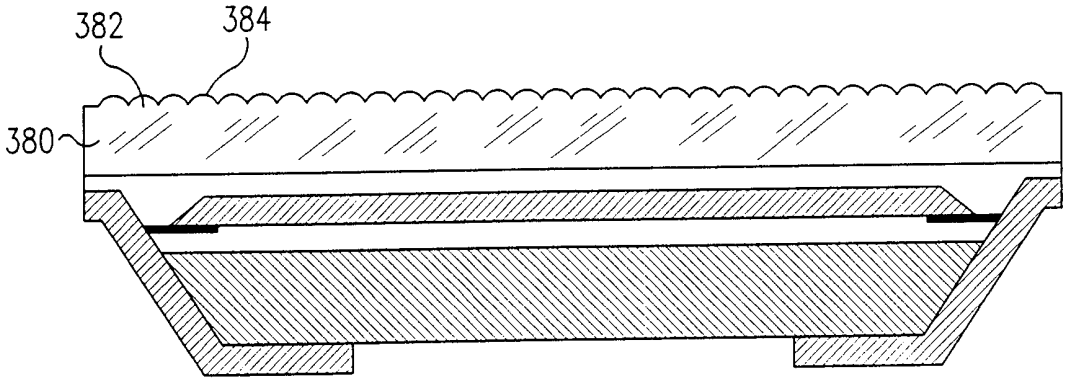


FIG. 14C

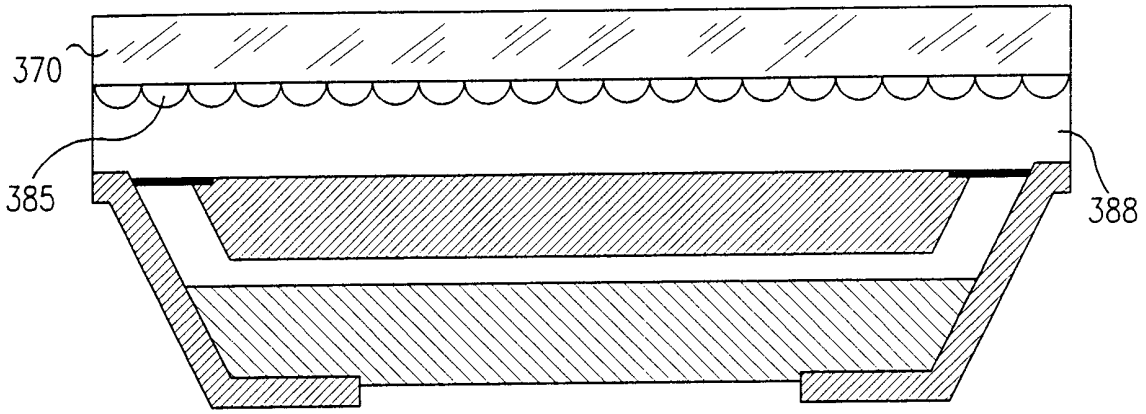


FIG. 14D

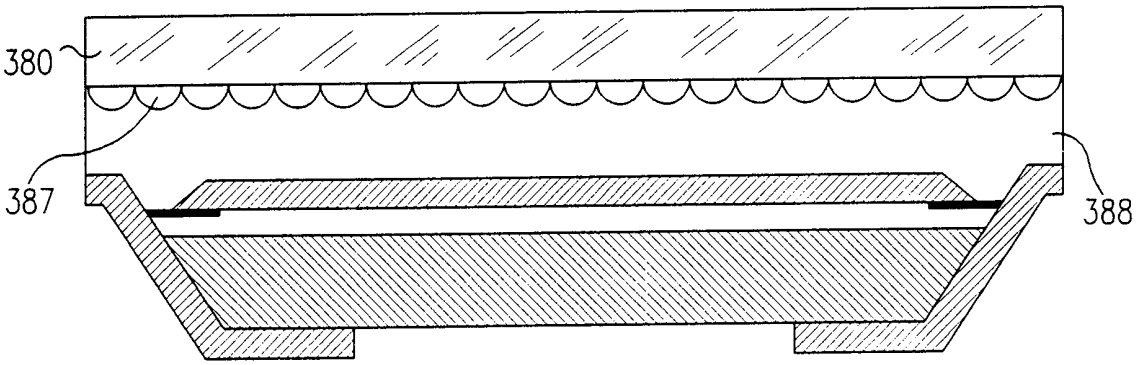


FIG. 15A

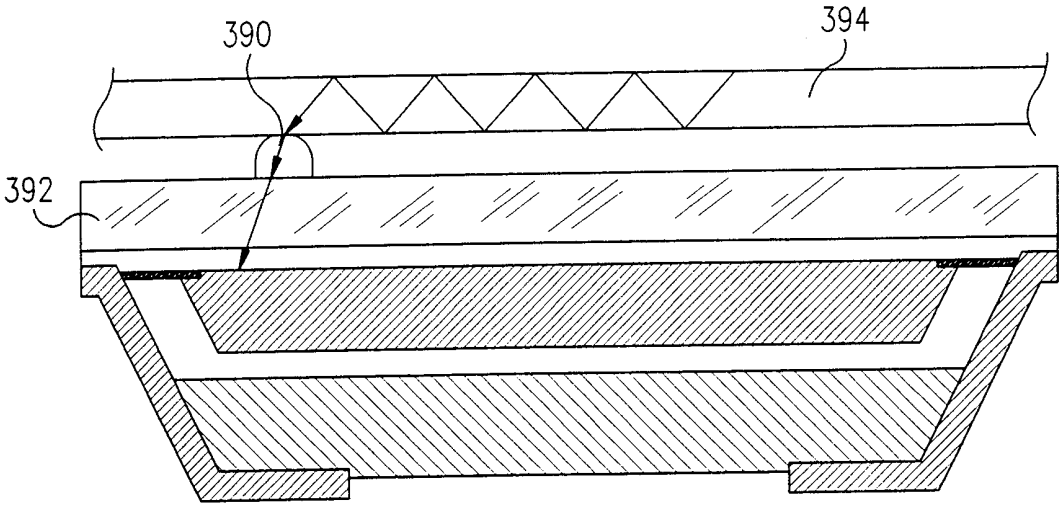


FIG. 15B

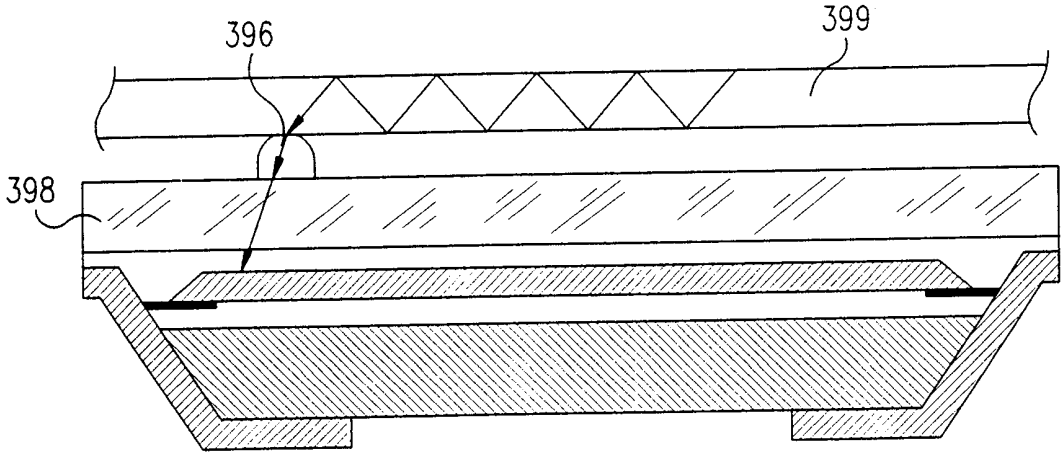


FIG. 16A

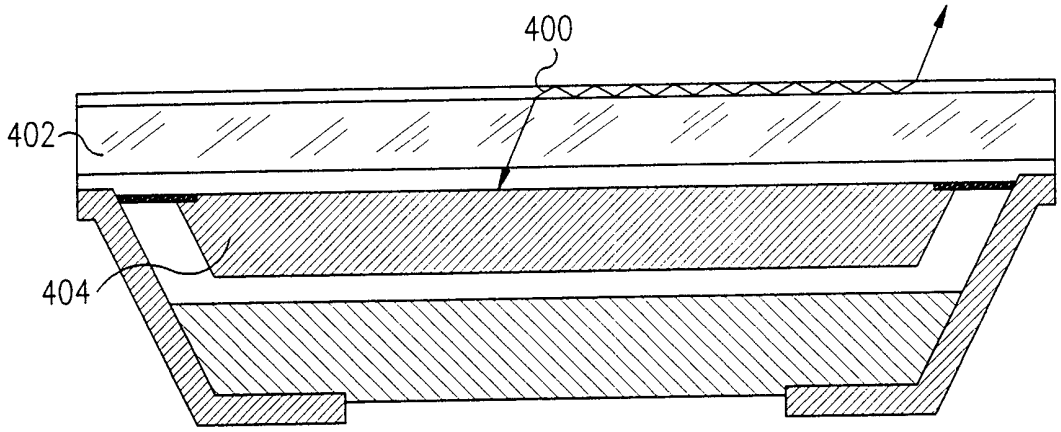


FIG. 16B

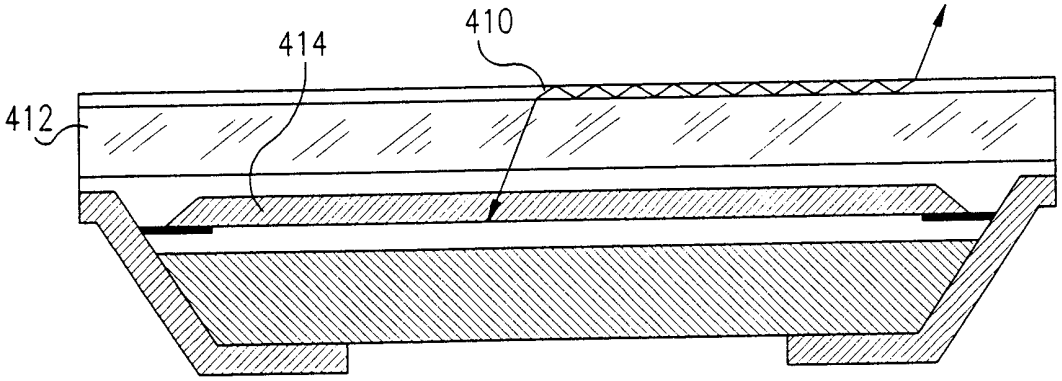


FIG. 17A

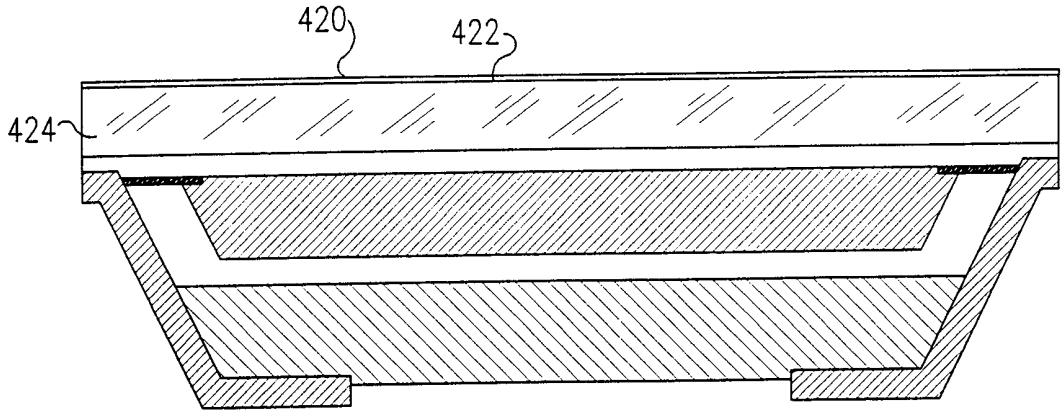


FIG. 17B

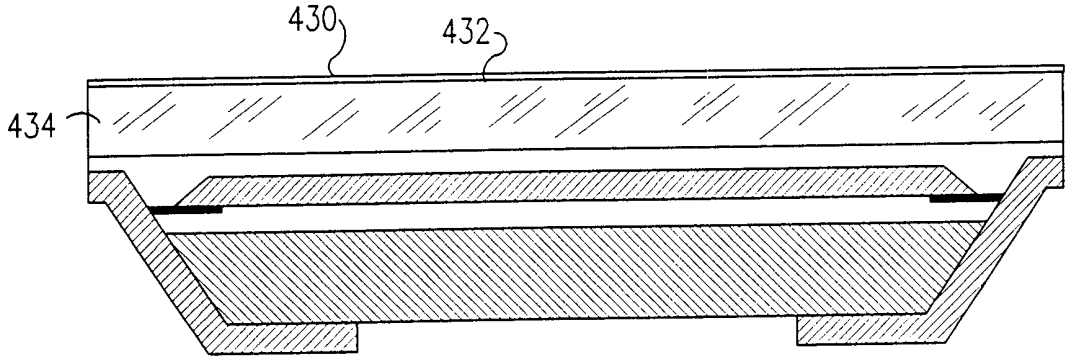


FIG. 18A

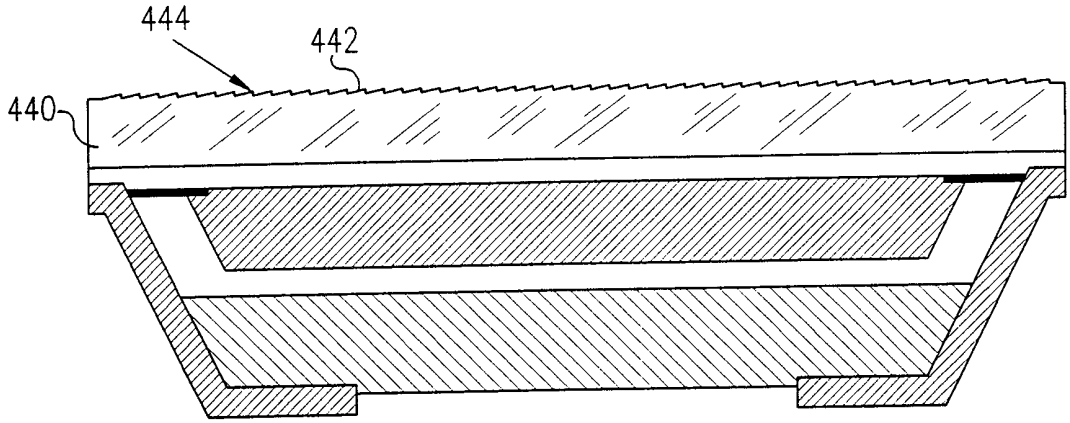


FIG. 18B

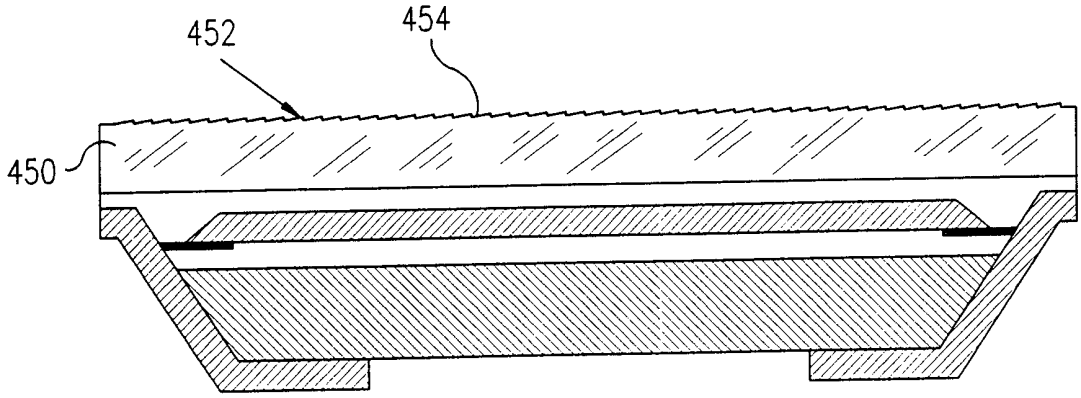


FIG. 19A

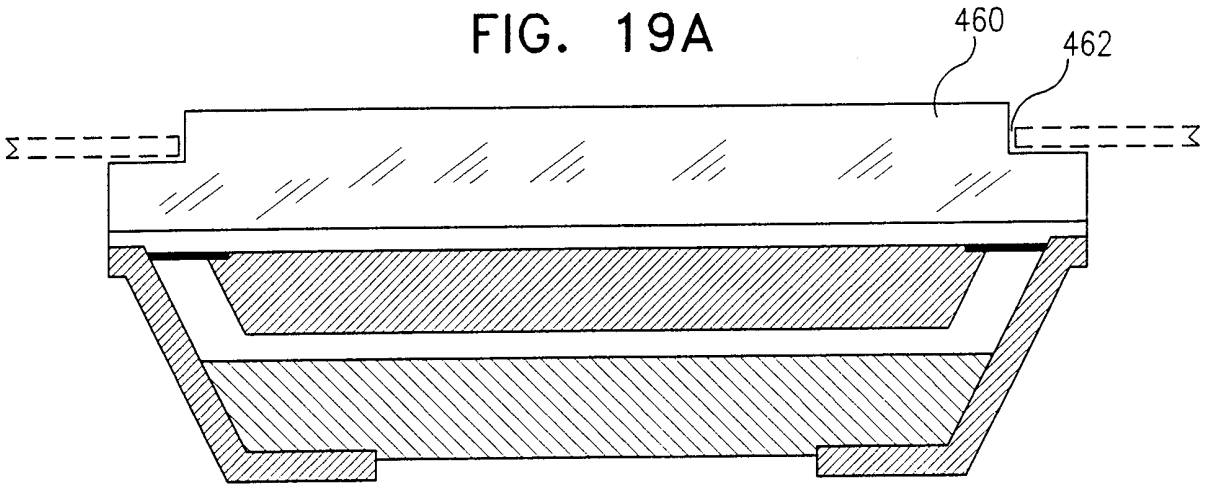


FIG. 19B

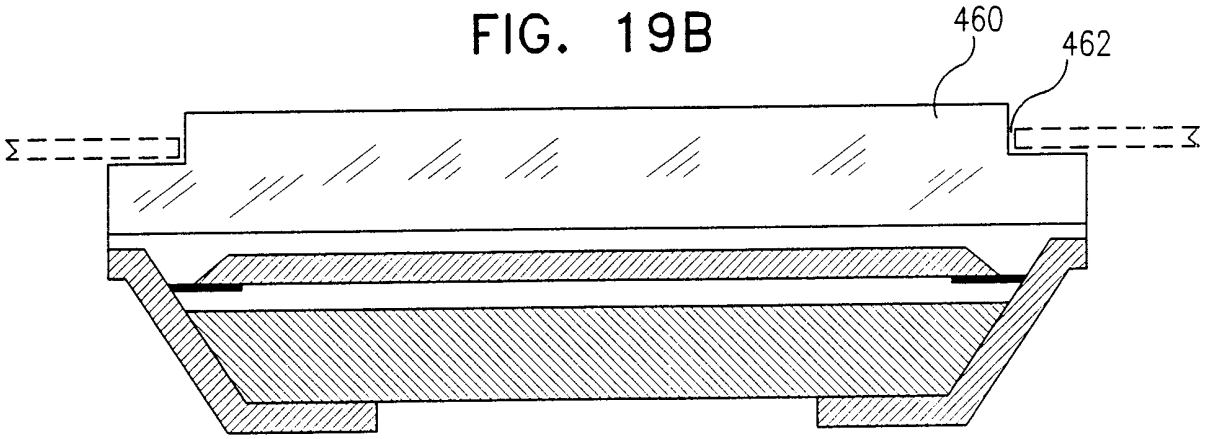


FIG. 20A

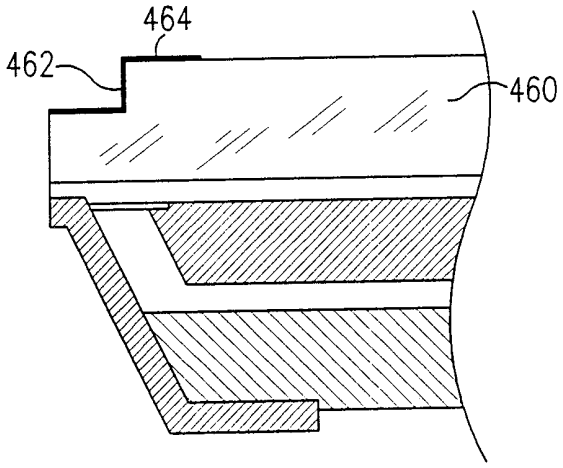


FIG. 20B

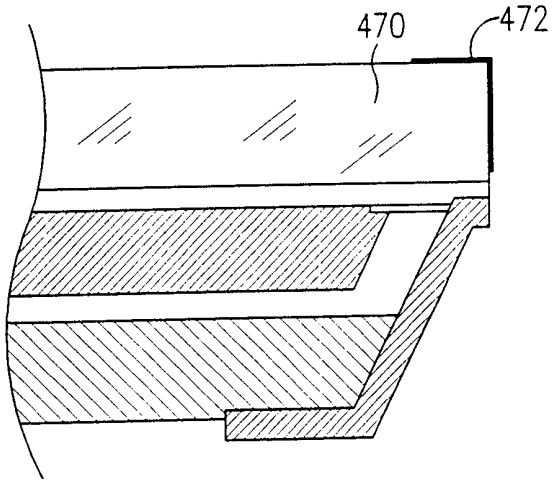


FIG. 21

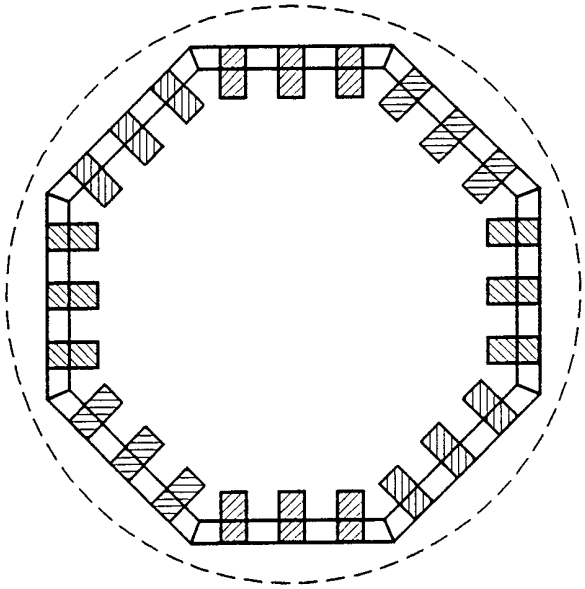
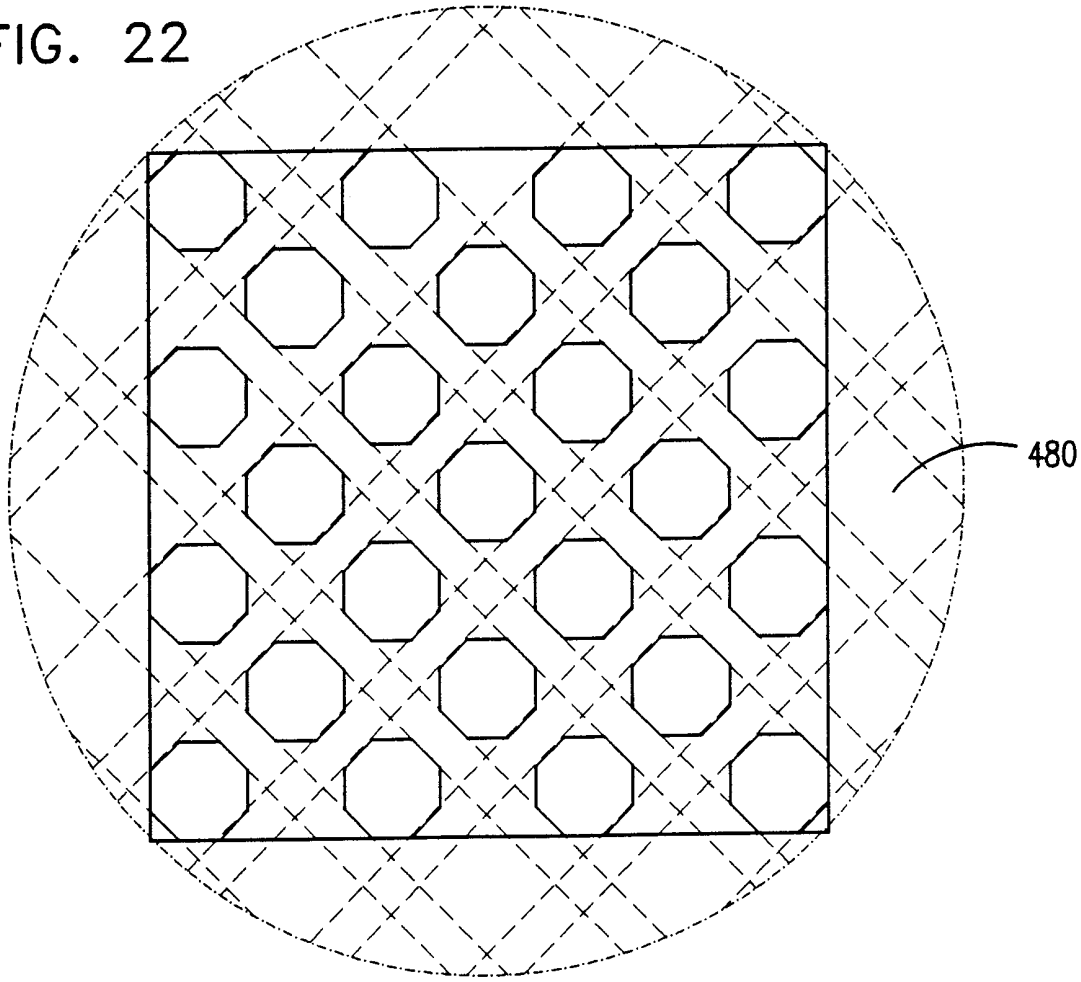


FIG. 22



INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL99/00071

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/70
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

STN
search terms: integral lens, pads

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,250,462 A (SASAKI et al) 05 October 1993, entire document.	ALL
A	US 5,677,200 A (PARK et al.) 14 October 1997, entire document.	ALL
A	US 5,672,519 (SONG et al.) 30 September 1997, entire document.	ALL
A	US 5,595,930 (BAEK) 21 January 1997, entire document.	ALL
A	US 4,259,679 A (KNIBB et al) 31 March 1981, entire document.	ALL
A	US 4,339,689 A (YAMANAKA et al) 13 July 1982, entire document.	ALL

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 04 MAY 1999	Date of mailing of the international search report 26 MAY 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer for DAVID E. GRAYBILL Telephone No. (703) 308-1782

Form PCT/ISA/210 (second sheet)(July 1992)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL99/00071

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,279,690 A (DIERSCHKE) 21 July 1981, entire document.	ALL
X	US 3,981,023 A (KING et al) 14 September 1976, col. 1, lines 48-52, and col. 3, lines 31-40.	1-3, 10-12
A	US 5,118,924 A (MEHRA et al) 02 June 1992, entire document.	ALL
A	US 5,526,449 A (MEADE et al) 11 June 1996, entire document.	ALL
X	US 5,266,501 A (IMAI) 30 November 1993, col. 3, line 29 to col. 4, line 30.	1-3, 10-12, 18
X	US 4,797,179 A (WATSON et al) 10 January 1989, col. 6, lines 19-66.	1-3, 10-12, 18
X	US 4,933,601 A (SAGAWA et al) 12 June 1990, col. 3, line 30 to col. 4, line 35; and col. 6, lines 24-32.	1-3, 10-12, 18

Form PCT/ISA/210 (continuation of second sheet)(July 1992)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL99/00071

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. [X] Claims Nos.: 19 and 20
because they relate to subject matter not required to be searched by this Authority, namely:

Claims 19 and 20 are apparatus claims that are improperly dependent on process and product claims.

2. [ ] Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. [X] Claims Nos.: 4-9, 13-17, 19 and 20
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. [ ] As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. [ ] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

[ ] The additional search fees were accompanied by the applicant's protest.

[ ] No protest accompanied the payment of additional search fees.

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

257/81, 98, 99, 225, 228, 294, 323, 432, 434, 447, 448, 460, 466, 680, 681; 438/27, 29-33, 38, 61, 65, 68-72, 113, 114, 116, 125, 464, 465, 763, 780, 928, 956, 958, 978

B. FIELDS SEARCHED
Minimum documentation searched
Classification System: U.S.

257/81, 98, 99, 225, 228, 294, 323, 432, 434, 447, 448, 460, 466, 680, 681; 438/27, 29-33, 38, 61, 65, 68-72, 113, 114, 116, 125, 464, 465, 763, 780, 928, 956, 958, 978