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Itzik Shweky, Avner Badihi

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# A CSP Optoelectronic Package For Imaging And Light Detection Applications

I. Shweky, A. Badihi

ShellCase, POB 48328, Jerusalem 96251, Israel.

Tel: +972 2 6798890, Fax: +972 2 6798850, Email: avnerb@shellcase.com

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## INTRODUCTION:

Portability and miniaturization are key factors in the electronic product market.

A fast growing market is Digital Photography, with a variety of small size and low weight electronic products, for professional and personal photography, medical and video conferencing

The development of low cost imaging devices drives the market for low cost Packages for Opto-Electronic imaging dice.

A recent packaging technology development (1,2) offers a substantial reduction of both costs and physical dimension of the Opto-electronic package.

## The Digital Imaging Market:

The popular use of consumer digital camera is fast becoming common place. It's two major drivers and contributors are: the Web, and computer based digital photography.

The use of digital cameras is compelling. The elimination of consumables (films, paper) and the immediate imaging capability of digital photography seems to be a strong attraction for the product. Recent introduction of low cost yet high quality color printers that produce "photo quality" images is serving to further inspire the market.

The recent evolution of CMOS imaging devices has fueled a new wave of optronic imaging devices. This trend is dominated by the US semiconductor companies, identifying a new market opportunity, well fit to their core technology.

## Price and Technology Trends

Diverse competitors, ranging from traditional camera manufacturers and consumer electronics manufacturers, to PC peripheral manufacturers, are battling to define

the future of digital imaging. This results in significant price

reductions while digital image resolutions continue to soar to new levels.

Furthermore, the use of digital CMOS makes it possible to integrate signal-conditioning elements DSP's, analog signal conditioners and communications interface-on the same substrate with the light-sensing elements, farther reducing the electronics cost.

As has been typical in the consumer electronics markets, consumer market growth will drive aggressive cost reduction to expand the market even farther. For the optronic imaging devices, a major element in that cost reduction will be in the packaging of the imager die.

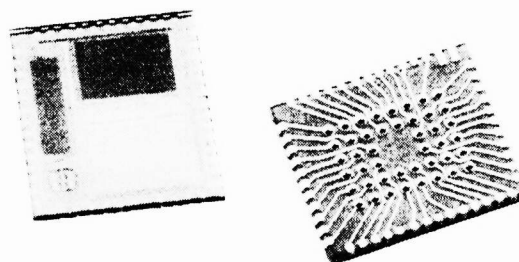


Figure 1: Photobit PB0159 CMOS Active Pixel Image Sensor packaged in the Shell-OP Optronic CSP

## The Opto-Electronic CSP:

A Die Size, Ultra Thin Opto-Electronic Package was developed. The Assembly process extends the semiconductor processing to the packaging of Integrated Circuits (Figure 1).

The glass transparent package encases the Imager Die. The assembly is held using a clear epoxy. A selective

spectral filter can be embedded within the package close to the active layer of the die

The package has special features both in relation to conventional Opto-Electronic packaging and Chip Size Packaging.

- True Die Size package.
- Configurable Spectral transparency.
- Ability to integrate Absorption or interference (dichroic) optical filters into the package
- Ability to integrate Color Filter Array (CFA) into the package.
- Extremely low thickness: 0.6 to 2.0 mm.
- Peripheral or area array configuration.
- The package, even as thin as 0.6 mm, offers a complete mechanical enclosure to the die. It does not leave any exposed Silicon, and seals the Silicon from the outside world, providing mechanical and environmental protection.
- Low cost -- particularly for small dies.

The packaging is implemented at the wafer level, where an optronic device is completely packaged using semiconductor manufacturing processes. The very small form factor, in comparison to the conventional optronic package, (see Figure 2).

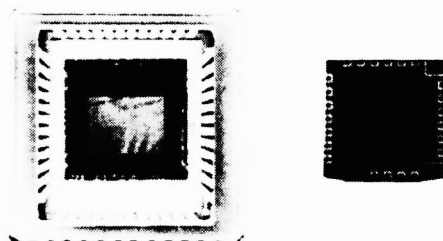


Figure 2: A comparative view, a regular Optronic Package LCC type, and a die size Optronic CSP

The schematical cross sectional view of the package (Figure 3) shows a thin silicon substrate, which is sandwiched between two thin protective plates on the top and bottom sides. An epoxy adhesive layer attaches the glass plates to the Silicon and surrounds and protects the edges of the Silicon die. Electrical leads connect to the pads of the die by a non-bonding technique.

The package is available with either perimeter or area array leaded configurations. Solderable leads have pitches down to 0.5 mm in the peripheral configuration and 0.8 mm in the area array configurations.

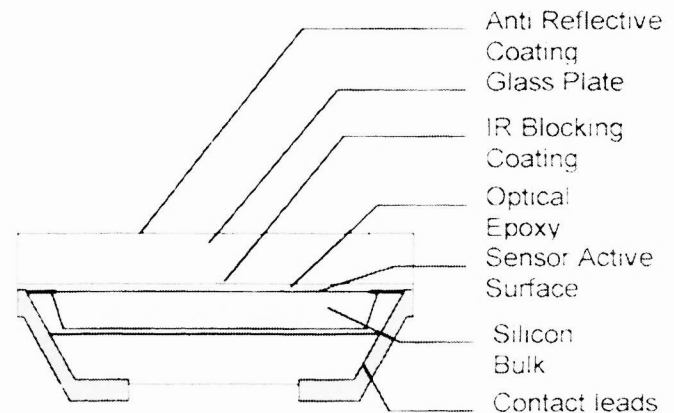


Figure 3: The Optronic CSP-Schematical

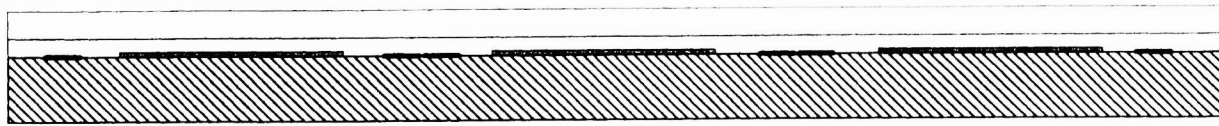
#### The Manufacturing Process:

The package manufacturing uses thin film and related processes that are commonly in use to manufacture Semiconductors. The Optronic CSP is thus an extension of the IC manufacturing processes. The dies are packaged and encapsulated into separate enclosures while still in wafer form.

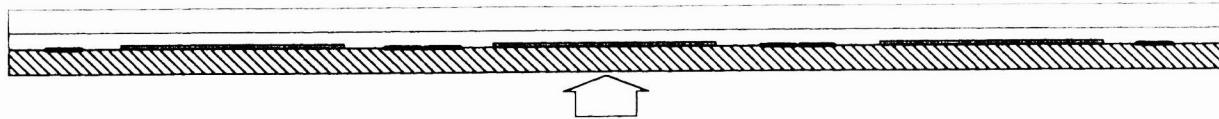
The basic steps in the manufacturing process are as follows (Figure 4):

- A thin protective layer is bonded on to a silicon wafer bearing active devices while the active surface of the IC is facing up into the encapsulate.
- The silicon material between the dies is etched away (back side), yielding individual IC's attached to the supporting cover.
- The grooves between the dies are filled with an inert material, and a second thin cover is bonded onto the silicon dies back side to achieve a complete protective enclosure for each die.
- Deep notches are drawn between the dice, so as to reveal the pads cross section.
- A metal layer is deposited so as to contact the metal pads at their cross sections. The metal layer is patterned by a lithography process to individual leads, contacting the pads and forming a soldering pad on the upper surface of the package. Finally, contacts are plated by either gold or lead-tin.
- Wafer dicing yields individual packaged dies.

Figure 4: Optronic Package Schematical Process



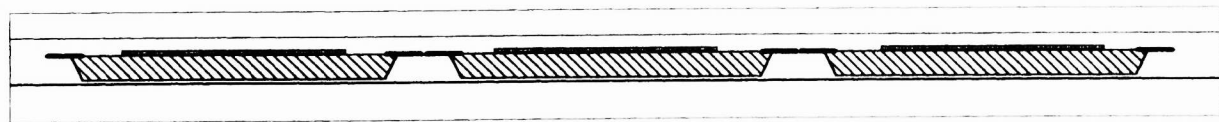
- A. The incoming die is coated with a Mosaic layer
- B. The incoming lass plate for Bond-1 is coated with a Filter layer
- C. Attach Glass Cover onto Wafer Active surface, use Optical Clear Epoxy. Filter side faces the die active surface



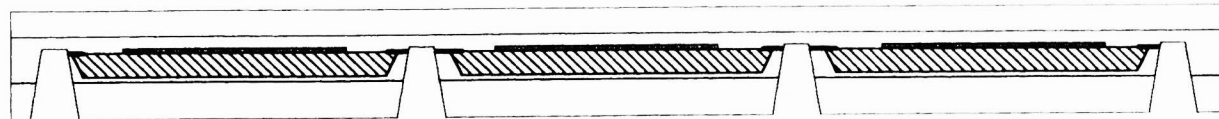
- D. Grind the Silicon from the back side of the wafer down to 70 microns.



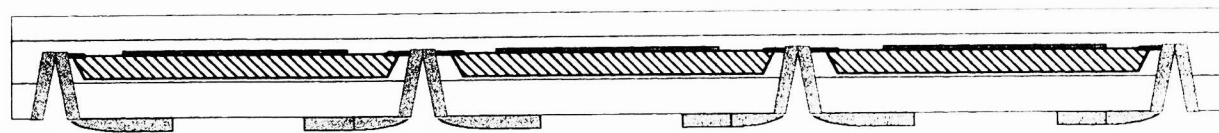
- E. Etch the silicon along the dice lines separating the dies.



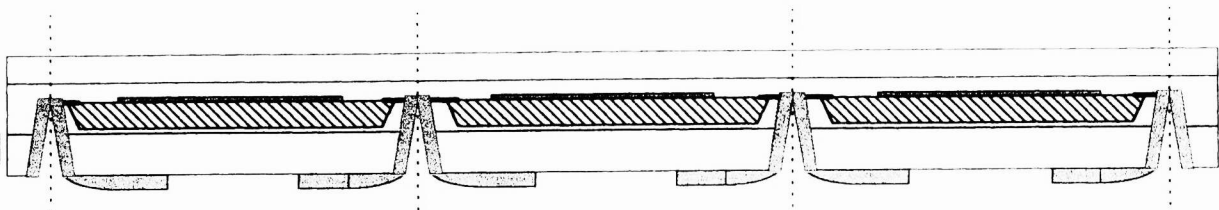
- F. Attach a second glass plate from the back side, the epoxy fills the trenches between the dies.



- G. Notch process along the dice lines, carried from the back side of the wafer.



- G. Lead deposition on notched side



- H. Dice the wafer into singulate pre-packaged dies

### Optical characteristics of the Package Components:

Refraction indexes for the glass and epoxy are shown on the following table.

| Material | Index of Refraction |
|----------|---------------------|
| Glass    | 1.5275              |
| Epoxy    | 1.5400              |

Figures 5 and 6 show the absorption spectra of the glass and the epoxy.

The figures indicate little absorption throughout the visible range (see APPENDIX 1).

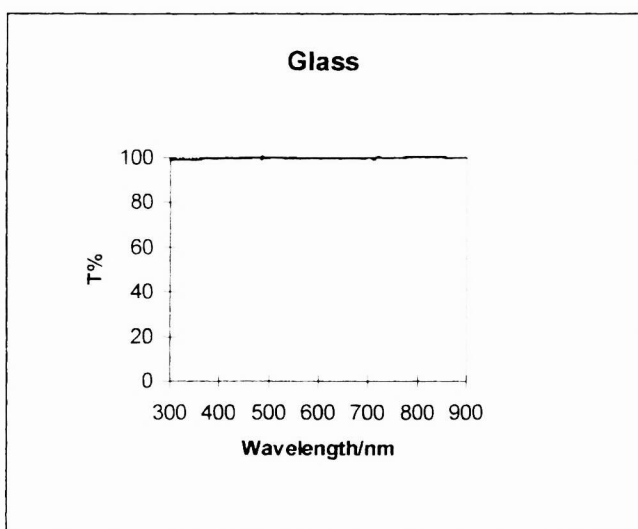


Figure 5: Transmission characteristics of the glass plate used.

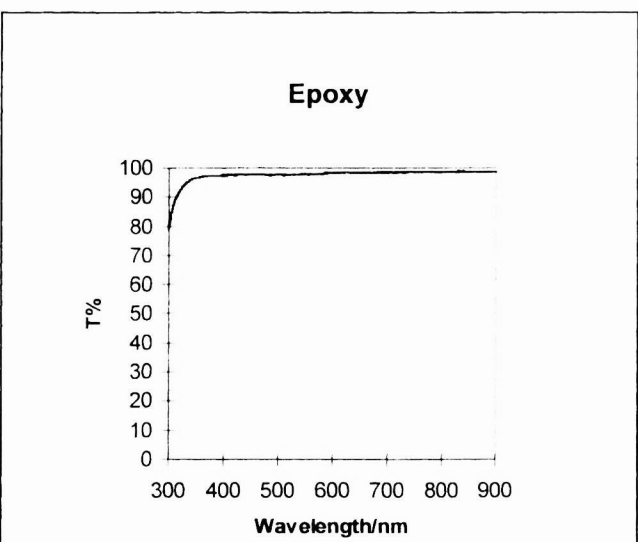


Figure 6: Transmission characteristics of the optically clear epoxy .

### The optronic dimensional accuracies and tolerances.

The dimensional and assembly tolerances and accuracies of the Electro-Optical imager die assembly in the package is a major issue, far more sensitive than for ordinary IC packaging.

Accurate optical assembly of the device package at the system level depends on the assembly process accuracy, and reproducibility.

These mechanical tolerances, translation of the imager, rotation and tilt of the imager die in relation to the reference plan, are all critical for the effective implementation of the imager in the next level system.

Table 1, compares the mechanical accuracies between the Wafer Level Optical Package, and two regular, mechanically assembled, optical packages.

Note the excellent accuracies of the wafer level process, in comparison to mechanical assembly.

**Table 1: Mechanical features and Dimensional tolerance comparison for different Packages.**

| Mechanical Feature                                      | Package A            | Package B           | Opto-CSP                      |
|---------------------------------------------------------|----------------------|---------------------|-------------------------------|
| Center                                                  | $\pm 150\mu$         | $0 \pm 85\mu$       | $\pm 35\mu$                   |
| Translation of effective image area (X, Y)              |                      |                     |                               |
| Rotation angle of effective image area (in focal plane) | $< \pm 1^\circ$      | $< +0.25^\circ$     | $< +0.01^\circ$               |
| Tilt of effective Image area (Z-axis)                   | $< 60\mu$            | $< \pm 25\mu$       | $< 10\mu$                     |
| Thickness of cover glass & refractive index             | 0.75 mm<br>$n = 1.5$ | 0.55 mm<br>$+ 0.05$ | $> 0.4$ to 1 mm<br>$n = 1.53$ |
| Self Centering                                          | No                   | No                  | Yes                           |

#### Self Centering.

One of the main advantage of Bump Solder Array interconnects is the "self centering" phenomenon that occurs during solder reflow.

The solder bumped Optical CSP (see Figure 7) is placed on the pad with solder paste. Exact placement is not required, in fact, a placement of only 50% of the sphere on the soldering pad will still allow the self adjustment action.



**Figure 7: Solder Bump Array on the Optical CSP.**

For many optical assemblies, the accurate alignment of the optical components is critical, and thus requires special care as well as specialized assembly tools.

With the "self centering" process, the device even loosely placed on the board, will align itself to exact placement in relation to the pads and trace patterns on the board. The surface tension of the molten solder drives the self alignment.

Alignment in the lateral dimensions is not the only "self centering" action that occurs. There is vertical alignment as well, that occurs as part of the setting of the component, balanced with the surface tension of the molten solder.

This vertical alignment can compensate for some of the warpage and irregularities that might be seen in the board, again improving and simplifying the accurate assembly of the Optical system (3).

#### **The integrated filter:**

The Optronics CSP allows the integration of a filter or color layer in the package.

Two alternatives for the filter integration are available:

1. Coated filter for IR Blocking (Figure 3)
2. Absorption filter for IR Blocking (Figure 8)

The purpose of integrating the Infra - Red blocking filter in the package is to compensate for the different spectral response of the Silicon detector and the human retina. Not only does the silicon detect in the Ultra Violet and Infra Red range beyond the visual range, but

the spectral response in the visible spectra is different for the eye and the silicon detector.

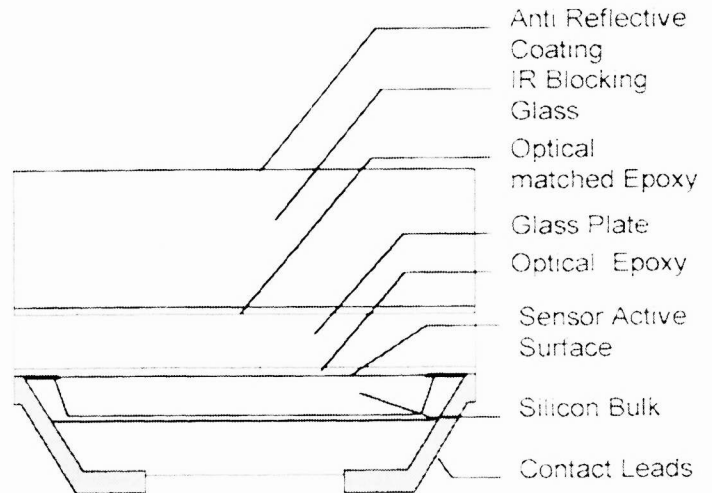


**Figure 8: Optronics CSP - with IR Blocking Glass Filter**

Correcting Filters such as the one shown on Figure 9, correct the Silicon detection response to match the eye response.

These filters are commercially available as either interference, thin film type or absorption type, and are an essential part of every Solid state imaging element.

The integration of the filter into the package allows the use of the minimal filter plate area (silicon detector size). Thus saving costs, by reducing the number of optical components required. Furthermore, filter integration saves costs, by reducing the filter size required.

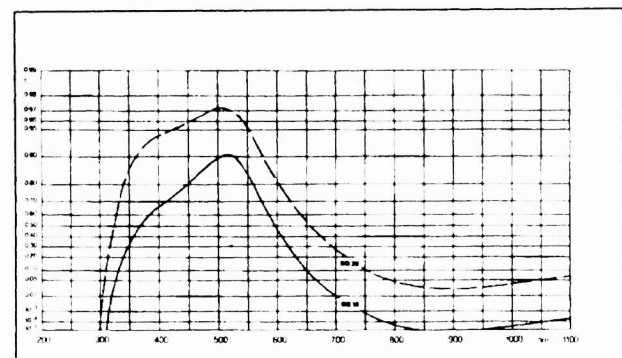


**Figure 9: IR Blocking Glass Filter type BG 18 and BG 38 (source SCHOTT GLAS, Optics Div.)**

**Reliability and environmental Testing:**

The Shell-OP package is undergoing reliability tests, using custom test dies. Tests are performed with the packaged die SMT mounted to a Printed Circuit Board. Table 2 details the test program.

| Test            | Conditions                                                 |
|-----------------|------------------------------------------------------------|
| THB             | 85°C; 85% RH; 5V Bias                                      |
| Endurance       | 125°C, 50 mA/Lead,<br>$J = 3.3 \times 10^4 \text{ A/cm}^2$ |
| Thermal Cycling | -40°C to +85°C, air to air,<br>1000 cycles                 |
| Popcorn         | JEDEC A112, level 2                                        |

**Summary:**

An Optronic CSP package has been developed, achieving a reduction of size as well as a reduction in the manufacturing costs. The manufacturing process is carried out at the wafer level, and extends IC manufacturing processes into device packaging. CMOS Imager dice have already been packaged with the optical CSP, and are currently undergoing both optical qualification and reliability tests.

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