

Silicon Processing

for the VLSI Era

Volume 2 - Process Integration

**SILICON PROCESSING
FOR
THE VLSI ERA**

**VOLUME 2:
PROCESS INTEGRATION**

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- PECVD TEOS film, deposited at 330°C. (Figure 4-54c shows that the resulting hillock size and density are both small.)¹⁷²
- ECR deposition (see section 4.4.10).
- Photo-CVD SiO₂.¹⁸³
- Afterglow-CVD of SiO₂.²⁴
- Anodized Al deposition.¹⁸⁴

Once such dielectric films are in place, they suppress hillock growth during later thermal cycling.

- *Use of refractory metal films such as W or Mo (which exhibit much less propensity to form hillocks at 400°-500°C) in place of Al.*
- *Use of an ionized cluster beam deposition process to deposit smooth Al/CaF₂/Si films.* According to the report on this process, the films remained hillock free up to temperatures of 500°C.¹⁸⁵

4.7.4.2 Dielectric Void Reliability Problems. If the voids are opened following an etchback step, they can trap moisture or photoresist residues that can cause long term reliability problems. In addition, metal may be deposited into the voids that can be very difficult to remove by etching, thus producing shorting between neighboring metal lines.

4.8 PASSIVATION LAYERS

Following patterning of the final metal layer, a passivation layer is deposited over the entire top surface of the wafers. This is an insulating, protective layer that prevents mechanical and chemical damage during assembly and packaging. The desired properties of the passivation materials are given in Table 4-5. In general, the thicker the passivation layer the better, since a thicker layer will provide better protection and improve the electromigration resistance of underlying Al lines. On the other hand, because thicker CVD films (especially silicon nitride films) have a higher tendency to crack, there is normally an upper limit to the thickness.

The final mask, called the pad mask or bonding contact mask, is used to define patterns corresponding to the regions in which electrical contact to the finished circuit will be made. These patterns in a resist layer allow openings in the passivation layer to be etched down to Al areas on the circuit called bonding pads (see chap. 5, Fig. 5-16). Either wet or dry etching can be used to etch the passivation layer. Since the dimensions of the pads are so large (i.e., normally 100 x 100 μm), wet etching is still frequently used to etch PSG films, while silicon nitride films are more easily etched by means of a dry etching process.

Phosphorus-doped, low-temperature CVD SiO₂ films were the first passivation layers to be used. The phosphorus is added to the SiO₂ to reduce the stresses in the film (and to thereby decrease the tendency of the film to crack), as well as to improve the gettering

properties of the film (with respect to sodium ions and other fast-diffusing metallic contaminants). The higher the phosphorus concentration, the better these characteristics will be.

On the other hand, if more than 6 wt% phosphorus is added to the film, corrosion can become a serious problem, especially in the case of chips mounted in plastic, nonhermetic packages. Water vapor can rapidly penetrate the plastic packaging material, transporting with it contaminants from the surface of the package. If the PSG contains excess phosphorus, the moisture can react with it to form phosphoric acid (HPO_3), which will eventually penetrate the film. As noted earlier, electrochemical corrosion of the Al lines can lead to metallization failure. While the transport of contaminated moisture through the PSG is a relatively slow process, if cracks or defects (e.g., pinholes) exist in the film, the water vapor will be able to penetrate it much more rapidly.

Silicon nitride has also been used as a passivation-layer material because it provides an impermeable barrier to moisture and mobile impurities (e.g., sodium) and also forms a tough coat that protects the chips against scratching. Its high dielectric constant is not a disadvantage for this application, since the passivation layer is deposited on top of the last metal layer.

However, because the passivation layer must be deposited over Al films, only PECVD silicon nitride can be used for this application (since it is deposited at $\sim 300^\circ\text{C}$). Unfortunately, PECVD nitride films normally exhibit a high mechanical stress ($\sim 6-8 \times 10^8$ Pa), which can cause cracks in the film during heating after deposition (especially at steps). The high compressive stresses in the films have also been shown to enhance void formation in Al interconnects (see section 4.7).

In addition, PECVD silicon nitride tends to be nonstoichiometric and contains substantial quantities of atomic hydrogen (10-30 at%). Large quantities of hydrogen have been found to accelerate hot-electron aging effects in MOS devices (see section 5.6.6). It has also been reported that the hydrogen from PECVD nitride is responsible for the formation of bubbles or cavities at the metal-plasma nitride interface when Al:Si alloys are used as the metallization. These appear after the 450°C anneal that is carried out following nitride deposition. It is supposed that the hydrogen reacts with the Si precipitates in the Al film to form gaseous compounds that produce the bubbles.^{186,187} It has been recommended that a low-hydrogen-content passivation film be used, if nitride passivation is selected for MOS technologies with gate lengths of less than $1.5 \mu\text{m}$ (in which hot-electron degradation is significant).

Work has been done to develop processes for growing nitride films with low hydrogen concentration and stress, and more is now understood about the relationship of the film properties to such deposition conditions as rf frequency, power, and bias.¹⁸⁸ Lower H_2 concentrations in the nitride have been obtained when the film is formed with $\text{SiH}_4\text{-N}_2$ mixtures rather than with conventional $\text{SiH}_4\text{-NH}_3$ mixtures.¹⁸⁹ Fluorinated nitride (F-SiN) films have been developed that exhibit only 0.6% of hydrogen (in the form of Si-H).^{190,191}

The use of PECVD silicon-oxynitride films (deposited with SiH_4 , NH_3 , N_2 , and N_2O mixtures) as alternative passivation materials has also been investigated, since they exhibit nearly the same the moisture and sodium barrier characteristics of nitrides.

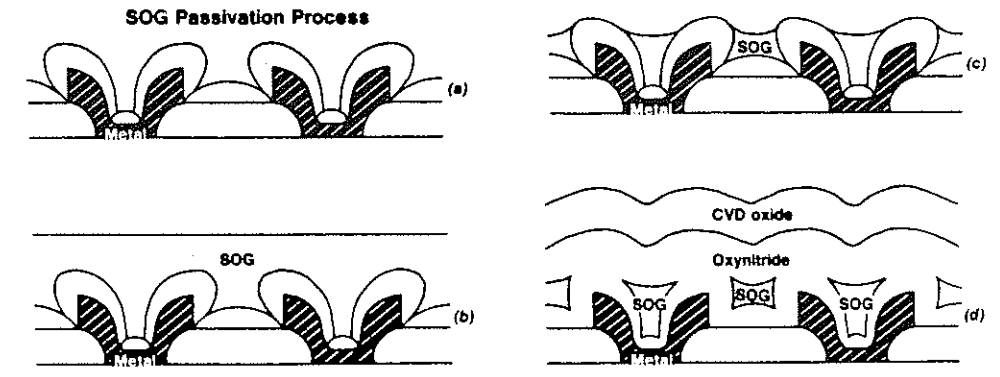


Fig. 4-56 SOG Passivation Process. (a) Deposition of the first oxynitride layer. (b) SOG applied. (c) after SOG etch back, and (d) finished passivation process after second oxynitride and CVD oxide depositions.

Fig. 4-56 Using SOG film as a part of the passivation overcoat improves EPROM reliability.²⁵⁶ Reprinted with permission of Semiconductor International.

While not quite as good as those of nitrides, the characteristics are better than those of oxides.¹⁹² However, their stress is between that of APCVD oxide (tensile) and plasma nitride and oxide (compressive).¹⁹³ In addition, because the stress is a function of applied rf power, pressure, and bias, it is possible to optimize the stress by using bias. Ideally, a very low-stress dielectric oxynitride film can be formed that will still maintain good diffusion-barrier properties. (It is important to characterize the stress over the entire temperature range of operation to which the dielectric film will be subjected, since the stress can exhibit hysteresis effects. These may be due to structural changes in the film due to loss of material during heating.) Finally, it is reported that PECVD oxynitride films can be formed that contain considerably less H_2 ($\sim$ one-half, in one report) than do PECVD nitrides.¹⁹⁴

Another, more recently adopted approach to the formation of passivation layers involves multilayer passivation coating. An initial coating of PECVD oxide is deposited, followed by a PECVD nitride. The oxide layer reduces the mechanical stress ($\sim 40\%$) and the hydrogen content of the passivation layer, while the nitride protects the device against handling, humidity, and mobile ions. This inorganic bilayer may be followed by a polyimide layer that is several microns thick (especially useful in automated bump-bonding processes) and a thick layer of silicone gel, or similar material, for cushioning and for void elimination during die bonding.

In a second variation of this technique applied to EPROMs, a sandwich oxynitride-etchedback SOG-oxynitride layer is first formed. This film is then covered with a low phosphorus-content CVD-oxide layer to complete the composite passivation film (Fig. 4-56). Sandwiching the SOG film between the two oxynitride layers reduces the occurrence of voids and seams in the passivation layer. These voids and seams caused degraded passivation film coverage, which in turn correlated with increased EPROM array failures after steam stressing.²⁵⁶

Table 4.5 Desired Properties of a Passivation-Layer Material

1. Provides good scratch protection to underlying circuit structures. In general, the thicker the passivation layer the better, subject to cracking and patterning restrictions.
2. Impermeable to moisture, as moisture is one of the main catalysts for corrosion.
3. Exhibits low stress, preferably compressive ($\sim 5 \times 10^8$ dynes/cm²).
4. Conformal step coverage.
5. High thickness uniformity.
6. Impermeable to sodium atoms and other highly mobile impurities.
7. Easily patterned.
8. Good adhesion to conductors, as well as to the interlevel dielectric beneath the last level of metal.

4.9 SURVEY OF MULTILEVEL METAL SYSTEMS

As noted earlier, with NMOS IC technology it was possible to exploit the polysilicon layer as an extra level of interconnect, while in bipolar technology it was necessary to develop a two-level-metal system in order to obtain comparable flexibility of interconnect routing. As a result, the problems of two-level-metal systems (primarily, the implementation of low-temperature planarization techniques) first had to be tackled by bipolar IC manufacturers. When CMOS replaced NMOS as the dominant MOS VLSI technology, CMOS ICs also required a two-level-metal system, since the polysilicon could not perform the function of a local interconnect level as effectively as it had in NMOS (see chaps. 2 and 6). However, the polysilicon gate structures and the nonrecessed LOCOS field-oxide steps in CMOS created an even more difficult topography for two-level-metal CMOS systems than for bipolar systems.

4.9.1 Bipolar Double-Level-Metal Systems

The first example we present is that of a structure described in 1984 by Ghatte et al. of Texas Instruments.¹⁹⁵ The Metal-1 pitch is 4 μm , and the Metal-2 pitch is 6 μm . Metal 1 is a 575-nm-thick bilayer film of Ti:W covered with Al:Cu, and the contact to silicon is made by self-aligned PtSi formed in the contact holes. Metal 2 is also a bilayer film of Ti:W and Al:Cu, 775 nm thick. The intermetal-dielectric layer is a 600-nm-thick PECVD oxide layer in which 1.1- μm vias are opened to allow contact between Metal 2 and Metal 1. No planarization of the intermetal dielectric was reported for this DLM process.

A second example, detailed by Bergeron et al. of IBM, uses a bilayer PECVD silicon-nitride/polyimide film as the intermetal dielectric. Smoothing of the underlying metal topography is achieved through use of the polyimide.¹⁹⁶ The Metal-1 pitch is 5 μm and the Metal-2 pitch is 7.0 μm . Metal 1 and Metal 2 are both Al:4%Cu films defined by lift-off, and Metal 2 is 2 μm thick. The bilayer intermetal-dielectric film is etched by

means of two masking and etching steps. In the first, an oversized via opening in the polyimide is defined and etched through an isotropic dry-etch step. In the second, a smaller via in the nitride is defined and dry etched.

4.9.2 CMOS Double-Level-Metal Systems

The following DLM processes are listed according to the generation of CMOS technology for which they were reported to be designed, as specified by the minimum MOS device gate length.

4.9.2.1 Nonplanarized DLM (2.0- μm CMOS). An example of a two-level-metal CMOS interconnect structure that does not rely on any planarization methods was presented by Smith et al. of Intel (Fig. 4-57a).¹⁹⁷ The Metal-1 pitch is 5.0 μm , and the Metal-2 pitch is 6.0 μm . Metal 1 and Metal 2 are Al:Si films, and the intermetal dielectric is an oxynitride composite film. Metal 2 is used to strap the polysilicon lines in order to reduce the word line delay in SRAMs built with this technology. Via-hole sloping is achieved by implanting the top surface of the oxynitride. Note that contact between poly and the Si substrate is made with *butted contacts* (see chap. 3).

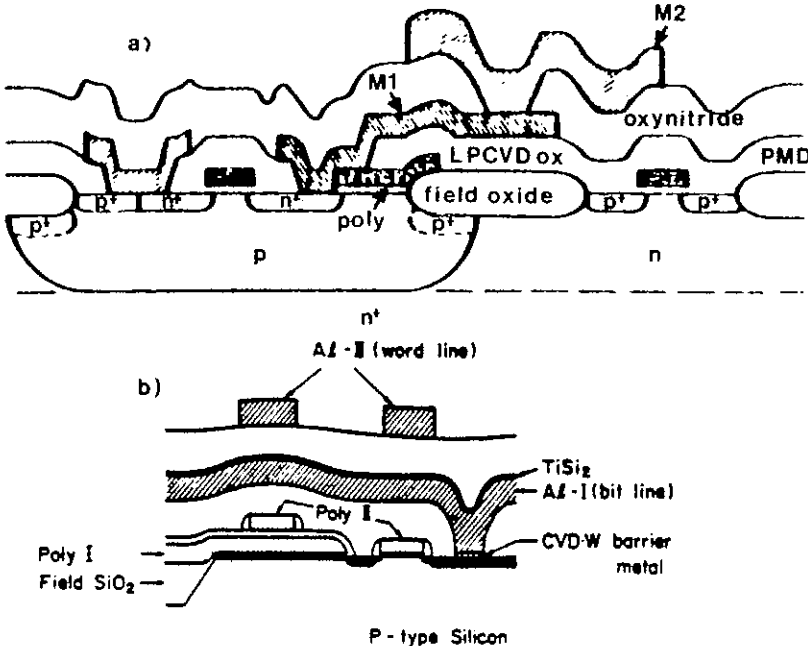


Fig. 4-57 (a) Example of a double-level-metal CMOS process with no planarization.¹⁹⁷ (© 1984 IEEE). (b) DLM process with a CVD W barrier metal and TiSi₂ hillock-suppression layer on top of the Metal-1 Al layer.²⁰⁰ (© 1984 IEEE).