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Die level thinning after bonding on the substrate in 3D packaging

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Abstract: This paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in packaging, i.e., A technology for processing silicon dies with a thickness of 100 um or less and a technology for handling thinning ultrasmall dies. We combine wet etching with dry etching to fit an effective and practical experimental plan. Anisotropic etching in KOH solutions and ICP etching of silicon die bonding on a glass substrate are investigated. Die with copper wiring is fabricated and pasted on the substrate to achieve selective etching of the whole device. The topography of the die surface and corner is analyzed to prevent the influence on the second layer stacking process.

1. Introduction

High-speed Ethernet signal transmission technology is essential in situations where the volume of data traffic is increasing exponentially, such as data centers, Internet exchange centers, and high-performance servers. To address this problem, heterogeneous integration package technology is focused on, which can reduce integration and power consumption. Ultra-thin-chip processing and interconnection (including wafer bonding) through the silicon through holes (TSV) are key technologies to implement the heterogeneous integration platform. To realize heterogeneously integrated packaging, the die-thinning of chips is fundamental [1,2]. The thickness of the silicon wafer used as the substrate is reduced, resulting in a thinner device. At the same time, the bandwidth is increased, and the occupied space is reduced. This thickness thinning can facilitate the implementation of multilayer stacking[3,4]. Second, it is simple to realize via making and interconnecting in the back end, and it is advantageous for sawing finished devices[5,6].

The existing packaging process was executed by die thinning first and then bonding on a substrate. This process is difficult to control when the intermediate die becomes thinner to a certain level during die bonding, resulting in a defect in the suction step of lifting the die[7–9]. In addition, this method is limited because the size of the die varies for heterogeneously integrated packaging. To address this problem, the process of thinning the entire sample after bonding was studied.

Here, the die was manufactured by creating a copper circuit on a silicon substrate and then deicing it to the desired size [10–12]. The silicon etching method must be used for all samples to study die thinning formed in this manner. The etching method is primarily divided into dry etching and wet etching, and common wet cleaning methods include pressure spray, imaging, ultrasonic, vibrational/rotational, and vapor degreasing cleaning[13–17]. Typically, dry etching and wet etching are used in tandem. In this study, selective etching should be performed on the entire sample, and damage to each layer caused by

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this cleaning method must be evaluated. Thus, most of the damages were minor, and simple imaging and rotational methods were used.

In the dry-cleaning process, a lift-off method is used in which contaminants are either sputtered, converted to volatiles, or removed by removing the material from the underlying layer[18–20]. The chemical dry-cleaning method that converts contaminants into volatiles has a high selection ratio and can reduce the reattachment of contaminants. To improve the selectivity, the chemical reaction gases that react with the contaminants to produce volatile compounds must be appropriately reacted.

In the study, a silicon wafer-based device was manufactured to reduce the thickness and size of the chip, and it was intended to be applied to MEMS device packaging or die-level packaging by dipping and bonding in various die sizes.

Table 1. Etching conditions

Wet Etching		Dry Etching	
Solution	Weight %	Plasma Pro System 133 ICP380	
Potassium hydroxide (KOH)	30 %	SF6 60 Sccm	O2 5 Sccm
Hydroxylamine (NH2OH)	15%	Power 750 W	
Temperature 80 °C		Temperature 20 °C	

2. Experimental

In this study, a 2-inch glass wafer was used as the substrate, and etching was performed by attaching a 2 × 2 × 0.2 mm die to it, as shown in Figure 1. The epoxy resin CTB-BF17X16 was used as an adhesive, and the thickness of 10±1 um was controlled using the spin coating (9000rpm) method. After that, the prepared dies were attached to the glass wafer substrate using the MD-P200US2~NM-EFF1D (Panasonic) equipment, and then it was cured for 30 min to solidify the adhesive while pressing with a constant pressure of 12.5 Mpa. The attached equipment conditions are pressure 1N, time 0.3 s, and temperature 25℃. Finally, for the etching, KOH was used as the wet etching method, and ICP was used as the dry etching method. Etching conditions are shown in Table 1. Whether wet or dry etching is used, the entire sample must be etched without additional protective film. The etching process only etches the silicon surface of the die without affecting the adhesive viscosity or CTE. In the wet etching process, although room-temperature etching is the least harmful to the samples except for the die surface, the etching rate is too slow, so tests have been made on different problems.

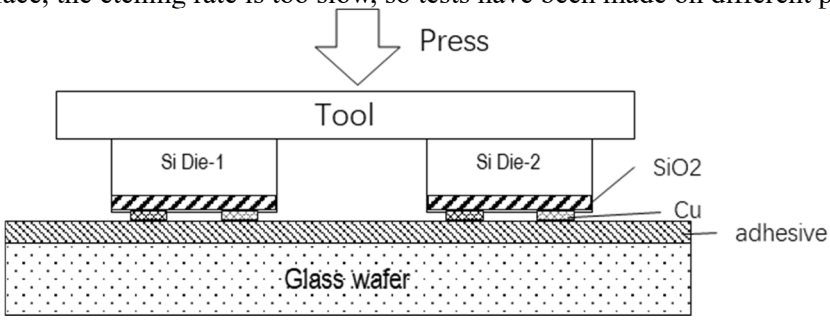

Figure 1. Schematic of die bonding

Die fabrication: We used a 4-inch silicon oxide wafer (p-type (100) Si with a thermal oxide layer (300 nm) on it) in the die fabrication process. UV-positive photoresist AZ4620 was used as the mask. After forming a pattern, exposure, and development, it was deposited to a Ti/Cu sputtering thickness at 20/480 nm to form a metal wiring pattern. After that, it was diamond-diced to finally form a die with an adhesive pattern having a size of 2 × 2 × 0.2 mm.

3. Result

Etching rate, roughness after etching, and undercutting corners of wet and dry etching samples are investigated. The etching temperature is a critical factor affecting the etching rate; therefore, the etching characteristics at different temperatures are analyzed. The detailed data are shown in figures 1

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and 2. Etching rates of the die surface in pure and 15 wt% hydroxylamines (NH2OH) with 20 wt% KOH added in solutions at various temperatures are shown in Figure 2. The etching rate increases as the temperature increases. Without NH2OH, the etching rate reached 4.45 μm/min at 100℃, while the temperature below barely changed. Considering that the entire sample is subjected to etching, a temperature that is too high will affect the properties of other layers, and an etching rate that is too fast will lead to the core finishing etching and exposing the metal line before the middle. This stage will lead to a short circuit, and a too-slow etching speed will prolong the etching time. The extension of time causes inconvenience in the process and affects the viscosity of the adhesive, causing the die to fall off during the etching process. Therefore, controlling the proper technique is crucial.

When NH2OH is added, the etching rate is significantly increased. At 60℃, the etching rate is multiplied by 23; at 80℃, it is multiplied by 72 because the decomposition of $NH2O^-$ and OH^- from NH2OH promotes reaction equilibrium[21,22]. Surface morphology is essential for determining if subsequent encapsulation can be successfully performed. Figure 3 shows the flatness of the etched die surface. The flatness gradually increases from 40° to 80°, yet the error bar shows between 0.6 and 1 um. However, when the temperature approaches 100℃, the flatness will exceed 1 um, and excessive foaming will eventually affect the flatness. Figure 4 shows the surface of sample and figure 5 shows the corner angle of the die after wet etching and dry etching. The results show that wet etching is 67° and dry etching is 90° because wet etching is isotropic, and dry etching is anisotropic. So finally, the surface of the sample forms the same appearance as the figure 4 and figure 5, that is, the edges and corners will be etched faster than the middle side.

Figure 6 shows the scanning electron microscopy and microscope images of chips after the etching process. Combining wet and dry etching is the most suitable solution for the above method.

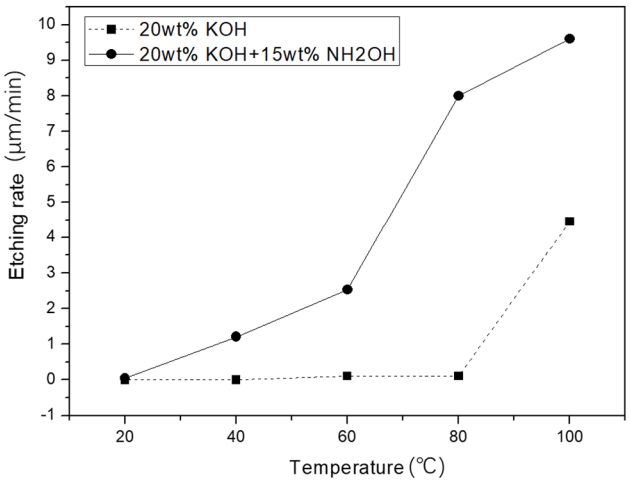

Figure 2. Wet etching rate using 20wt% KOH solution and 20wt% KOH+15wt% NH2OH solution at different temperatures. (SEM Cross section)

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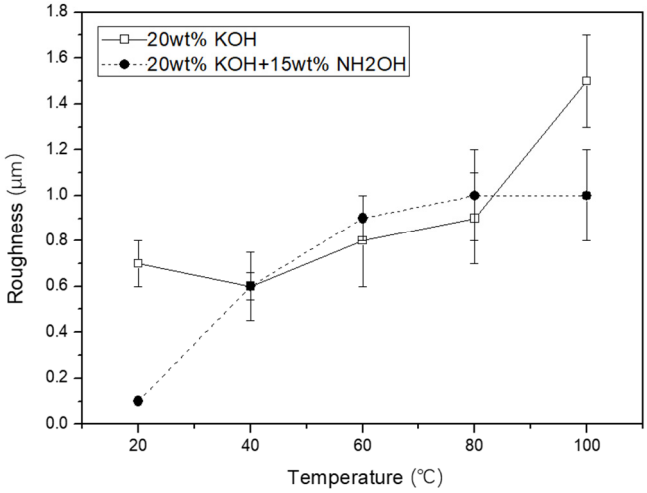

Figure 3. The roughness of die backside surface

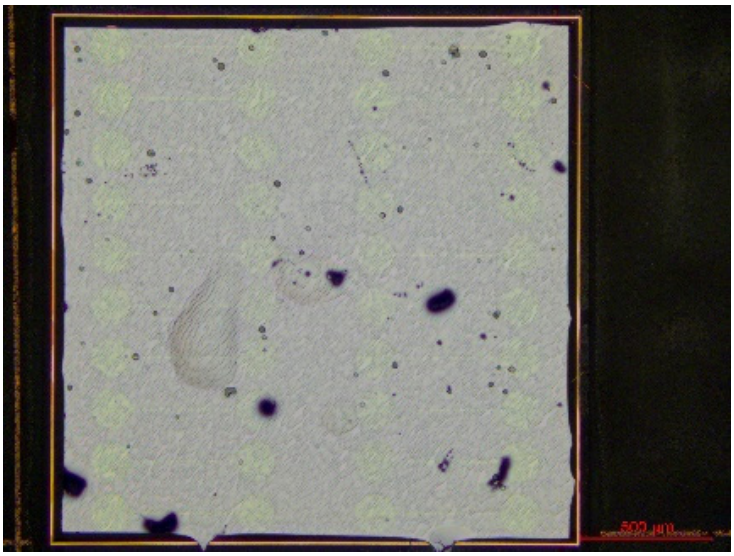

Figure 4. Surface of the die backside

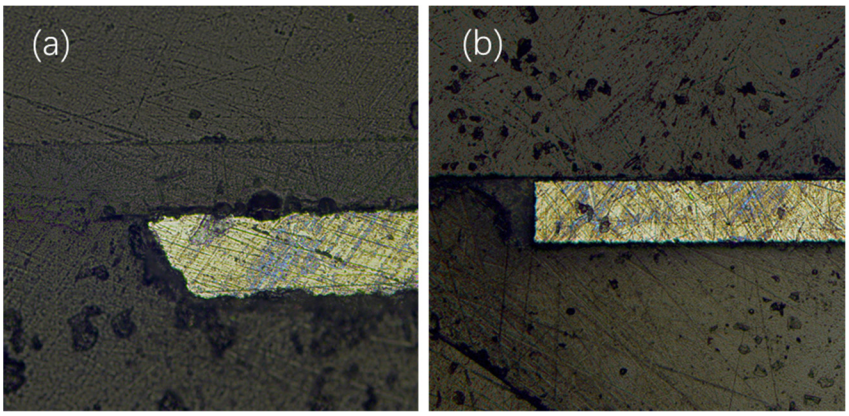

Figure 5. The corner of the die backside of (a) after wet etching and (b) after dry etching

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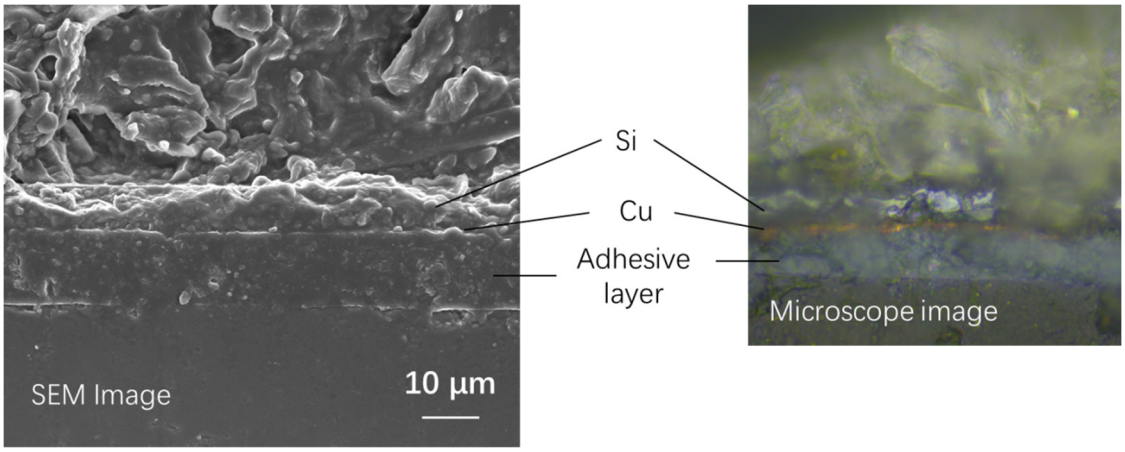

Figure 6. The cross-sectional scanning electron microscopic (SEM) image of chips after the etching process

4. Conclusion

Chip-to-wire and wafer-to-wafer are used to complete bonding and die bonding is the packing stage after die thinning. However, this wafer-level thinning bonding can only be used for isomorphism. If the wafer thickness is less than 150 um, it will become flexible and fragile, making it difficult to control and lowering the yield. Second, dies with metal wiring cannot be thinned using CMP and other operations, as this would destroy the internal structure and cause a short circuit.

Therefore, achieving die-level thinning is essential for heterogeneous integration. As long as die-level thinning can be realized, manufacturability can be improved, real high-density can be achieved, and heterogeneous broadband integration can be implemented. This study combines wet etching and dry etching to provide a preliminary foundation for reducing heterogeneous chips.

Acknowledgments

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