

# A New MOS Imager Using Photodiode as Current Source

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**Abstract**—We have developed a MOS linear image sensor having a high-voltage-gain amplifier in photodiode pixels. The only difference between the amplified MOS imager (AMI) and our new device is the transfer gate added between the photodiode pixel and the source follower. In this structure, the photo-induced charge loss in video-line parasitic capacitance is compensated to improve the sensitivity. The realization of a high-voltage-gain amplifier is implemented to control the input voltage of the transfer gate so as to maintain an unchanged bias voltage of the photodiode and by operating the photodiode cell as a current source. In our device, the photoinduced charge is not divided by the photodiode capacitance  $C_d$  or the capacitive load  $C_l$ . Therefore, it is possible to enlarge the photodiode size, and the sensor has a large saturation exposure as well as a large photocurrent/dark-current ratio of about 30:1. The device operates on a single 5-V power supply. These features make the device suitable for applications in low light levels.

## I. INTRODUCTION

DYNAMIC ranges in CCD [1]–[4] or MOS image sensors [5] are limited by various noises arising from their operation. In CCD's, these noises are mainly caused by reset noise, while in the MOS image sensor, they are caused by switching noise or random noise due to high output impedance.

Recently, in order to reduce these noise levels, several new image devices in which signal charges generated by light are stored in a control electrode region of photodiode cells used to amplify the output signal are investigated.

Tanaka *et al.* demonstrated a BiCMOS linear image sensor called the base stored image sensor (BASIS) [6], [7] and Yamashita *et al.* [8] and Hyneczek [9] advanced the amplified MOS imager (AMI). In these devices, since the output signals are amplified without the additional video-line noise included during readout operation, it is possible to obtain fundamentally high sensitivity and high performance of the  $S/N$  ratio.

Therefore, these devices cannot easily affect the generation current and are good for operation in low light levels.

However, in an AMI, as a result of amplifying signal charges individually, a new type of noise called fixed-pattern noise, caused by the variation of offset voltage in a

source-follower amplifier, arose. In BASIS, a similar fixed-pattern noise, which originated from dimensional and impurity fluctuation, appeared.

Furthermore, the sensitivity obtained by the above devices is poor compared to the sensitivity obtained with CCD's. In a CCD, as signal charges are transferred to a low-capacitance collection diode, it is possible to raise the sensitivity above unity voltage gain.

In an AMI, the sensitivity cannot exceed unity voltage gain because of the limitation by its parasitics. In BASIS, although it has higher charge gain, the output voltage is forcibly divided with video-line capacitance.

This paper describes an advanced AMI with high sensitivity equivalent to CCD's and noise reduction capability equivalent to conventional AMI's, which is realized by maintaining a constant photodiode bias voltage by applying the constant gate-source voltage to the transfer gate between the photodiode and the capacitive load and by transferring charges with no charge loss.

As this capacitive load is smaller than that of parasitics in the photodiode cell, a high-voltage amplification was obtained from this signal charge. It is also possible to control the output gain automatically and nondestructively by using the source-follower output.

The only disadvantage with this sensor is the discharge time lag. However, this feature is not a problem in the case of slow-charging illumination and can be applied to many systems.

This paper describes the operating principle, fixed-pattern noise characteristics, and the influence of dark-current generation in the second and third sections. Section IV describes the design description. Section V describes the experimental results. Finally, we will discuss the significance of this device.

## II. BASIC CIRCUIT CONFIGURATION AND OPERATIONAL PRINCIPLE

### A. Circuit Configuration

The conventional unit cell of an amplified MOS imager is shown in Fig. 1(a), which is constructed with an  $n^+$ -p photodiode with the parasitic capacitance  $C_d$ , reset gate  $Q_4$ , and the source-follower circuit.

This unit cell operates fundamentally as follows. The photodiode is reversely biased, and after resetting the bias voltage to the initial value  $V_{rs}$ , the charges stored in

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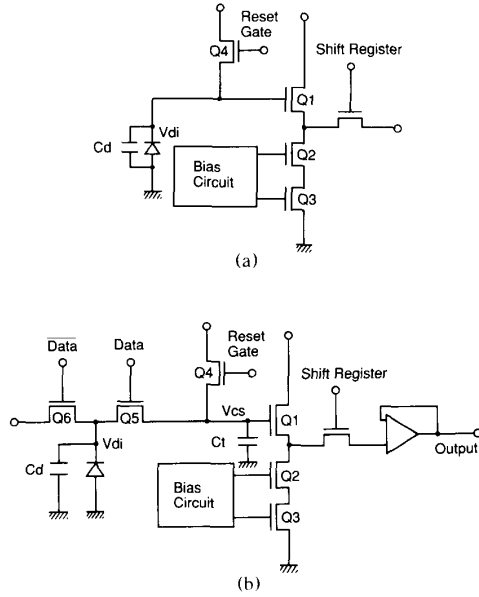


Fig. 1. The configuration of a unit cell in amplified MOS imager: (a) the conventional device and (b) the new device.

parasitic capacitance  $C_d$  are discharged by the photocurrent during the discharge time. Next, its voltage drop is read out by the source-follower circuit.

The voltage gain in this unit cell is determined by  $I_p \cdot t / C_d$ , where  $I_p$  is the photocurrent and  $t$  is the discharge time, and cannot exceed unity voltage gain.

In order to increase the above gain, we insert additional transfer gates  $Q5$  and  $Q6$ , and capacitive load  $C_t$  between the photodiode and the source follower, which are shown in Fig. 1(b). The role of  $Q6$  is to maintain a constant bias voltage during the whole time except during the discharge period and to protect the photodiode from overflowing charges. The role of  $Q5$  is to separate the capacitive load from parasitic capacitance. These transistors are controlled by DATA and  $\overline{\text{DATA}}$  signals.

### B. Discharge Operation

Discharge operation was performed by turning on  $Q5$ . We assume that the photocurrent does not fluctuate during discharge time and the gate voltage of  $Q5$  is controlled to be constant and always below the capacitive load voltage. The drain current of  $Q5$  equals the photocurrent and is constant during the discharge time. Therefore, the bias voltage of the photodiode is determined by  $V_g - V_{gs}$ , where  $V_g$  is the gate voltage of  $Q5$  and  $V_{gs}$  is the gate-source voltage. As the gate-source voltage is modulated by the drain voltage shown in Fig. 2(a), the bias voltage of the photodiode changes slightly from the initial value, the relation of which is shown in Fig. 2(b).

According to the discharge operation, the drain voltage of  $Q5$  is changed from the initial value  $V_{rs}$  to the final value  $V_{cs}$ , the gate-source voltage from  $V_{gs}$  to  $V'_{gs}$ , and, at

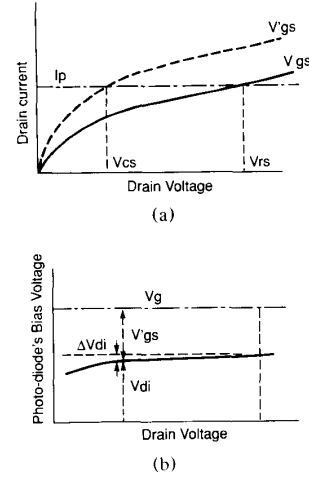


Fig. 2. Relation between drain voltage of  $Q5$  and the bias voltage in photodiode. (a) The  $V$ - $I$  characteristics of the transistor.  $V_{rs}$  and  $V_{cs}$  show the drain voltage when the gate-source voltage shifts from  $V_{gs}$  to  $V'_{gs}$ . (b) The bias voltage shift when the drain voltage shifts from  $V_{rs}$  to  $V_{cs}$ .

the same time, the bias voltage shift  $\Delta V_{di}$  of the photodiode is induced.

Therefore, the capacitive load voltage shift per unit time and unit photocurrent from reset voltage,  $\Delta V_s (= V_{rs} - V_{cs})$ , is given by

$$\Delta V_s = (I_p \cdot t - C_d \cdot \Delta V_{di}) / C_t \quad (1)$$

because the product  $C_d \cdot \Delta V_{di}$  does not contribute to the capacitive load voltage shift.

The bias voltage shift  $\Delta V_{di}$  depends on the effective channel-length modulation. The drain current in the saturation region is given by [10]

$$I_d = (L / (L - L_j)) \cdot I_{d\text{sat}} \quad (2)$$

where  $L$  is the channel length,  $I_{d\text{sat}}$  the drain saturation current, and  $L_j$  the depletion length of the drain side. Therefore,  $\Delta V_{di}$  is given by

$$\Delta V_{di} = (2 \cdot I_d / \beta \cdot L)^{1/2} \cdot \left\{ (L - L_j)^{1/2} - (L - L'_j)^{1/2} \right\} \quad (3)$$

where  $\beta$  is the transconductance and  $L_j$  and  $L'_j$  are the depletion lengths when the drain voltage equals  $V_{rs}$  and  $V_{cs}$ , respectively.

In practical devices, the concentration of the substrate is about  $1 \times 10^{15} / \text{cm}^3$ , the channel length of  $Q5$  is  $15 \mu\text{m}$ , the width is  $8 \mu\text{m}$ , and the transconductance is  $30 \mu\text{A}/\text{V}^2$ . The parasitic capacitance of the photodiode is  $2 \text{ pF}$  because its area is  $8400 \mu\text{m}^2$ , and the capacitive load is  $0.11 \text{ pF}$ .

Under the illumination range from  $20 \text{ mlx}$  to  $1000 \text{ lx}$ , the photocurrent falls into the range from  $20 \text{ fA}$  to  $1.0 \text{ nA}$ . Therefore, the bias voltage shift  $\Delta V_{di}$  is calculated as less than  $0.1 \text{ mV}$ , which corresponds to the  $2\text{-mV}$  capacitive load voltage shift.



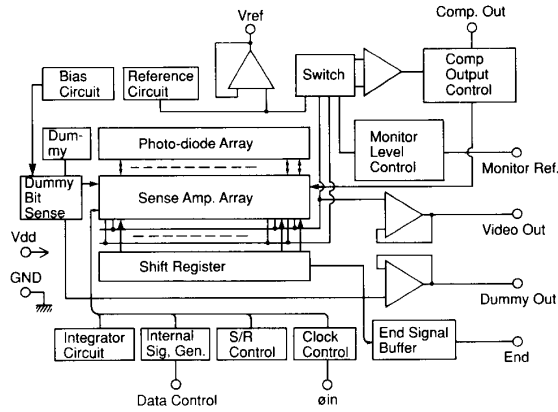


Fig. 5. Block diagram of amplified MOS imager.

controlling the diffusion current. In this structure, the N diffusion is enclosed by a P-implanted isolation diffusion. The impurity concentration in the P layer is controlled to minimize the diffusion current in the overlapping area.

#### IV. DESIGN DESCRIPTION

##### A. Overview

A block diagram of the sensor is shown in Fig. 5. The four blocks on the lower side of the figure—integration circuit, internal signal generator, shift-register control, and clock control—are of a digital circuit design. The four blocks on the upper side of the figure—bias circuit, reference circuit, comparator, and monitor level control—are of an analog circuit design.

The center blocks (photodiode array, sense-amplifier array, and shift register) are image sensor blocks. We can understand the operation of this chip by observing three sequential steps: initial reset, discharge, and readout. These steps are controlled automatically by a DATA control signal. In the initial step, an individual voltage reference is supplied sequentially and the comparator-out terminal becomes “L.” In the next step, each pixel stores the charge until one of the output voltages in the pixels reaches the setup level in the comparator. Then, the comparator-out terminal voltage becomes “H.” After that, the start pulse is entered in the shift register and video signals are output sequentially.

After the final readout step, the END signal is output. Diagrams illustrating the timing of these operations are shown in Fig. 6.

##### B. Autoresponse Control Circuit

In order to obtain an appropriate response, it is necessary to monitor the outputs of every pixel simultaneously and nondestructively. This operation is possible in our sensor. Fig. 7 shows the autoresponse control circuit. The method of monitoring the source-follower output is established by monitoring the levels of  $Q8$ .

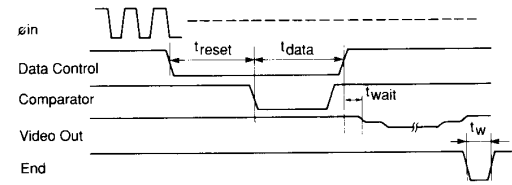


Fig. 6. Timing diagrams.

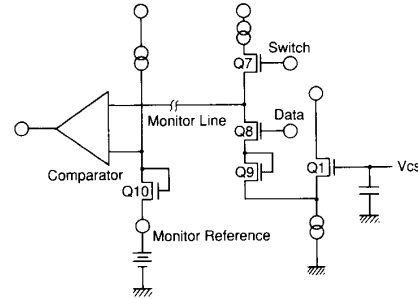


Fig. 7. Monitor control circuits.

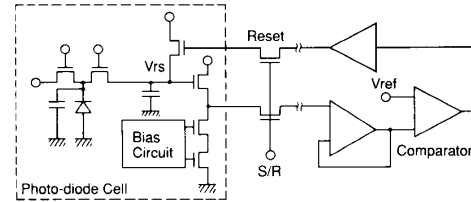


Fig. 8. Fixed-pattern reduction circuits.

The total bias current of  $Q8$  is set to a smaller value than that of the source-follower circuit. When one of the output voltages in the source-follower circuit decreases, the level of the monitor line also decreases through  $Q8_m$  (the subscript means the  $m$ th number of photodiode cells), and the other transistors begin to turn off spontaneously.

Therefore, the monitor-line voltage  $V_M$  is given by

$$V_M = (1/m) \cdot \sum_{m=1}^n [I_m + V_{0(m)}] + V_{th}$$

and

$$I_t = \sum_{m=1}^n I_m \quad (7)$$

where  $V_{0(m)}$  is the source-follower output of the  $m$ th cell,  $I_m$  is the drain current of  $Q8_m$ , and  $n$  is the cell number. When the monitor-line voltage is close to the reference voltage, the discharge operation is then turned off.

##### C. Fixed-Pattern Reduction Circuit

In the previous section, several methods of improving the device parameters concerning the reduction of the fixed-pattern noise were discussed. Although these methods were effective for normal application, in the case of

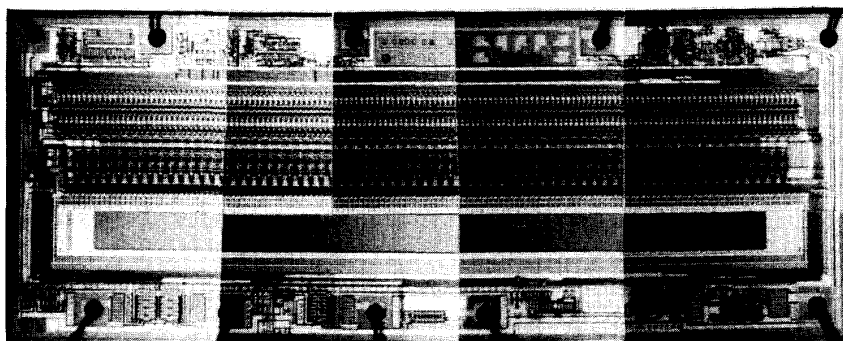


Fig. 9. Chip layout of amplified MOS imager.

low light levels, the signal-to-fixed-pattern-noise ratio cannot be ignored.

In our sensor, this ratio is reduced by controlling the initial voltage  $V_{rs}$  of the capacitive load of every pixel which is supplied until the source-follower output is equal to the reference voltage  $V_{ref}$ , as shown in Fig. 8.

The comparator output is then inverted and the transmission circuit is turned off. Then the reset voltage is stored until the next operation.

The reference voltage of every pixel is set up in this manner. This circuit reduces the fixed-pattern noise from 5–10 mV to 1–3 mV.

#### D. Layout Consideration

Since the devices in the analog section of this chip suffer from the influence of the digital section, the device design, layout, and arrangement are especially critical to obtaining a successful design. In addition, since the recombination of the excess photocarriers produced in the photodiode pixels is not stimulated, these carriers flow to other circuits and alter the operation. Therefore, factors such as common impedance, digital noise, and protection of overflow carriers had to be carefully considered in the overall layout.

Fig. 9 shows a photomicrograph of the extended amplified MOS image sensor with a  $5.89 \times 1.91\text{-cm}^2$  die size. The digital section can be clearly seen in the upper side, and an analog section can be seen in the lower side. The digital ground and analog ground are separated. The  $N^+$  diffusions of about  $50\text{ }\mu\text{m}$  width around each pixel and also the reset gates of the photodiode are prepared as the overflow drains.

The final item of interest concerning the layout is that it is necessary to minimize the capacitive load  $C_i$  to maximize the sensitivity.

In this design, the capacitance associated with the gate in the source follower and the  $N^+$  diffusion in the reset transistor dominates the layout parasitics. Therefore, the physical layout of pixels is the main consideration. The photodiode cell size is determined as  $35 \times 240\text{ }\mu\text{m}$  by the sensitivity, saturation exposure, and optical limitations. In order to enhance the sensitivity under low light levels, the

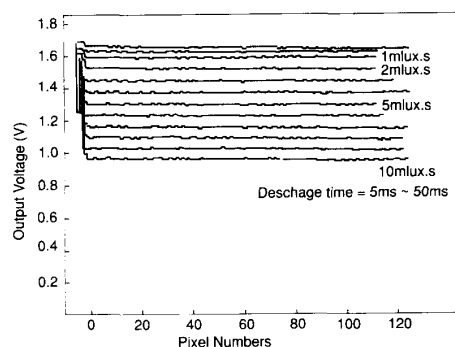


Fig. 10. Sensitivity and uniformity characteristics of amplified MOS imager.

photodiode is made as large as possible. Consequently, the parasitic photodiode capacitance  $C_d$  becomes  $2.0\text{ pF}$ . The capacitive load  $C_i$  is made as small as possible, which results in  $0.11\text{ pF}$ .

#### V. EXPERIMENTAL RESULTS

A 128-b linear MOS image sensor was fabricated and operated with a 5-V single power supply. The sensitivity is expected to be  $60\text{ V/lx}\cdot\text{s}$  for a fluorescent light with IR cut filter (CM500) and  $180\text{ V/lx}\cdot\text{s}$  for a halogen lamp. The characteristics of this sensor were measured under the low light levels of about  $0.02\text{ lx}$ .

In order to measure the dynamic characteristics, the relevant voltage is subtracted from the output, and the remainder is converted to digital values by an 8-b A/D converter. These values are stored in the CPU memory. The measured accuracy is derived with the A/D converter's resolution and accuracy, which corresponds to about  $3\text{ mV}$ . The discharge time was varied from 5 to 50 ms and the readout time was  $10\text{ }\mu\text{s}$ .

Fig. 10 shows the experimental results under the above conditions. The measured sensitivity was  $58\text{ V/lx}\cdot\text{s}$ . The saturation exposure was  $0.14\text{ C}$ , linearity was within 95%, and the uniformity was within 3%. The output saturation voltage was  $1.3\text{ V}$  and the power consumption was  $70\text{ mW}$ . The influence of dark current on the sensitivity was almost unrecognizable in this figure. The photoelectric

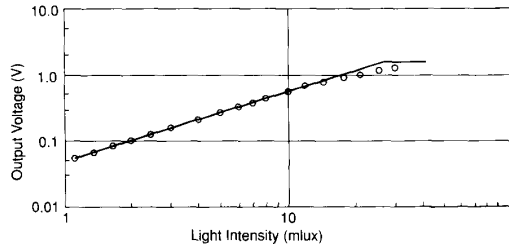


Fig. 11. The photoelectric conversion characteristics of amplified MOS imager.

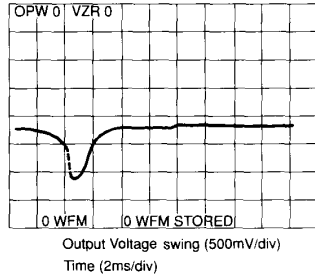


Fig. 12. The waveform of video output. This output is controlled by a monitor control circuit.

conversion characteristics are shown in Fig. 11. A photocurrent/dark-current ratio of 30:1 was obtained at a discharge time of 100 ms.

Fig. 12 shows the output voltage swing during actual operation. The autoreponse control circuit was operated and the minimum output voltage was controlled in spite of changing exposure light intensity.

## VI. CONSIDERATIONS

Our sensor has several advantages such as high sensitivity, relatively weak influence by dark current, large saturation exposure, and autoreponse control. The reason for the high sensitivity was mentioned in Section II. The operating principle of the sensor circuit is similar to that of the CCD in that it transfers charges from the photodiode to the collecting capacitance. Therefore, the sensitivity is equivalent to the CCD.

The difference in the dark current's influence in the CCD and this sensor is based on its operation. In the CCD, according to Saks,  $Q_{\text{loss}}$  is given by [12]

$$Q_{\text{loss}} = A \cdot q \cdot k \cdot T \cdot D_{it} \cdot \ln(t_b / T_t) \quad (8)$$

where  $A$  is the total CCD area,  $D_{it}$  is the density of the interface state,  $T_t$  is the CCD transfer time, and  $t_b$  is the time between bursts. The relation between the dark current and  $D_{it}$  is given by [4]

$$J1 = q \cdot n_i \cdot V_{th} (\sigma_p \cdot \sigma_n) \pi \cdot k \cdot T \cdot D_{it} / 2 \quad (9)$$

where  $n_i$  is the intrinsic carrier density,  $V_{th}$  is the thermal velocity of free carriers, and  $\sigma_p$  and  $\sigma_n$  are the interface-state capture cross sections for electron and holes, respectively. This equation indicates that in the CCD the dark-current generation area spreads not only over the photodiode cells. Therefore, in the case of low light levels, this sensor has better photocurrent/dark-current ratio characteristics than the CCD.

Another advantageous characteristic is the saturation exposure. This characteristic depends on the photodiode area and its bias voltage. In a CCD, this area is restricted by the size of the CCD shift register and its bias voltage.

On the other hand, in our sensor, this factor is restricted by only the photodiode area and the switching noise. Thus, it is possible to employ larger photodiode cells.

With respect to the autoreponse control, the details are mentioned in Section III. The autoreponse control is accomplished by having a multisensor amplifier circuit. The disadvantage of this sensor is the response time lag in the case of sudden illumination change. This phenomenon is caused by the voltage change in capacitance  $C_d$  in Fig. 1 with a sudden change in the illumination. In the case of a slow illumination change, this phenomenon is not a problem. Therefore, this device is suitable for the application of a slow illumination change.

## VII. CONCLUSIONS

We have developed a sensitive amplified MOS image sensor. The advantage of this sensor is achieved by the charge transfer technique using the transmission gate to maintain a constant photodiode bias voltage and to reduce the voltage in capacitive load. This performance results in the operation of a MOS transmission gate with a constantly controlled gate voltage so as to bias the photodiode voltage. As a result, the photocurrent is transferred to reduce the voltage in the capacitive load  $C_i$  and high sensitivity was obtained. The advantage of this sensor is not only the high sensitivity, but also the relatively weak influence of the dark current, large saturation exposure, and autoreponse control.

These advantages resulted in the operation of an amplified MOS image sensor. Although the response time lag is a disadvantage, in the case of a slow illumination change, this phenomenon is not a problem and thus this device is suitable for application in low light levels.

In the experiments, the obtained sensitivity is  $58 \text{ V/lx} \cdot \text{s}$  for a fluorescent light with IR cut filter, CM500, and 180 V/lx·s for a halogen lamp. The saturation exposure is 0.14 C, the linearity is within 95%, the nonuniformity is within 3%, and the output saturation voltage is 1.3 V. These characteristics are equal to or greater than those of the CCD.

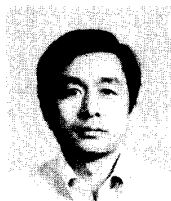
Although our demonstration was restricted to only a linear image sensor, this technology can be applied to an area sensor, and the charge transfer technology is also useful for several types of low-current MOS amplifiers.

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