A Dielectrically Isolated Photodiode Array by Silicon-Wafer Direct Bonding

J. OHURA, T. TSUKAKOSHI, K. FUKUDA, M. SHIMBO, AND H. OHASHI

Abstract—**A dielectrically isolated silicon photodiode array was successfully fabricated by a silicon-wafer direct-bonding method. A thermally oxidized wafer and another bare silicon wafer were placed in close contact at room temperature and bonded by heat treatment at 1100°C applied for 4 h. A series-connected 23-photodiode array, with a 1.6 × 1.6-mm chip size, produced a 13-V open-circuit voltage and a 7.7-μA short-circuit current at a 10-mA GaAlAs infrared-light-emitting diode current. Enough voltage was obtained to drive power MOSFET's for switching applications, photocoupled solid-state relays, and other uses.**

I. Introduction

PHOTODIODE serial arrays realize optical activation of power-field-effect transistors with current and voltage capabilities that are increasing year by year. These devices serve as new solid-state relays, which are noiseless, arcless, and reliable in comparison with conventional electromechanical relays. It is necessary to apply full dielectric-isolation technology for fabrication of such series-connected photodiode arrays. Junction isolation, familiar for bipolar integrated circuits, is ineffective under light illumination circumstances, because leakage photocurrents appear across the isolation regions.

A great deal of attention has been attracted by dielectric-isolation (DI) technology for high-density VLSI devices and for high-voltage integrated circuits (HVIC's), by which technology bipolar, MOS, power, photosensitive, and other semiconductor devices can be integrated. It is well known that a DI structure is feasible [1] in which silicon single-crystal tubs are embedded in polycrystalline silicon, but the substrates are very expensive because the thickness to which polycrystalline silicon is to be deposited is extraordinarily large.

Several other DI methods are under extensive development. They are zone-melting recrystallization [2], oxygen ion implantation [3], and oxidation for porous silicon [4]. However, especially for zone-melting recrystallization, sub-boundaries may degrade the characteristics of devices with submicrometer dimensions, probably due to enhanced dopant diffusion along the sub-boundaries [5]. Silicon on insulator (SOI) formed by oxygen ion implantation contains oxygen precipitates, which are not removed even after annealing for 2 h at temperatures of up to 1200°C [6]. Low-energy implantation would result in a better SOI crystalline quality, but both SOI and stoichiometric silicon-dioxide layers become thin. Full oxidation of porous silicon has resulted in wafer bending, which is hardly compatible with wafer processing and is a drawback of the method [7].

Recently, a silicon-wafer direct-bonding method was proposed [8], [9]. Wafer bonding is achieved simply by placing the oxidized surfaces of two wafers in close contact and inserting them into an oxidizing ambient at temperatures greater than 700°C. In the early stages of the experiment, voids were observed by thermography after the heat treatment. Advanced wafer processes in a clean environment realized voidless wafers with high production yields [10]. In the present work, the authors fabricated a silicon photodiode serial array using the wafer direct-bonding method. Single-crystal tubs, in which photodiodes are installed, are separated by sidewall oxidized V grooves filled with polycrystalline silicon.

II. Device Fabrication

The silicon single-crystal tub thickness is designed to be 50 μm in combination with the illumination source. A GaA1As infrared-light-emitting diode is a suitable illumination source, because its emission efficiency is high and its emission wavelength, near 860 nm, is in the region where the quantum efficiency for silicon is the highest. The absorption coefficient for silicon at this wavelength is 6.3×10^2 cm^{-1} [11].

A typical silicon photodiode array fabrication sequence is illustrated in Fig. 1. A 400-μm-thick n-type 9–12 Ω·cm silicon wafer, cut parallel to the (100) plane, was mirror polished and thermally oxidized in wet oxygen at 1100°C. After growth of 1 μm of the thermal oxide the wafer and another mirror-polished bare wafer of 550-μm thickness were bonded by heat treatment at 1100°C applied for 4 h. One side of the SOI wafer was lapped and chemically polished until the SOI residual thickness became 70 μm . The thickness was controlled within ±5 μm by state-of-the-art technology. V grooves were formed by anisotropic chemical etching (Fig. 1(c)), oxidized in wet oxygen, and filled with polycrystalline silicon (Fig. 1(d)). The top surface was lapped and mirror polished again until the SOI thickness became 50 μm. Full dielectric isolation for each single-crystal tub was performed, and the wafer then was ready for conventional silicon device fabrication processes. Boron and phosphorus were diffused selectively in the photosensitive regions and in the substrate contact regions, respectively. Fig. 2 shows a microphotograph of a monolithically integrated silicon p-n junction photodiode array, where 23 photodiodes are connected serially, with a 1.6 × 1.6-mm chip size. The photodiode array and a GaA1As LED were built into a dual inline package, with optically transparent epoxy resin between them. These were then molded, using

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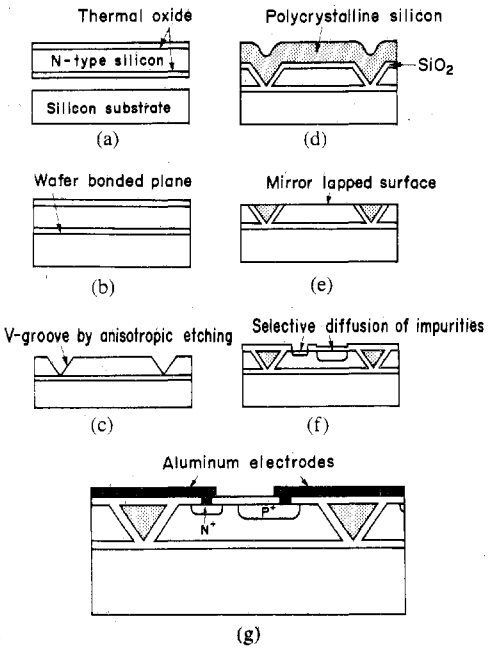

Fig. 1. (a)–(g) Dielectric isolation process by silicon-wafer direct bonding.

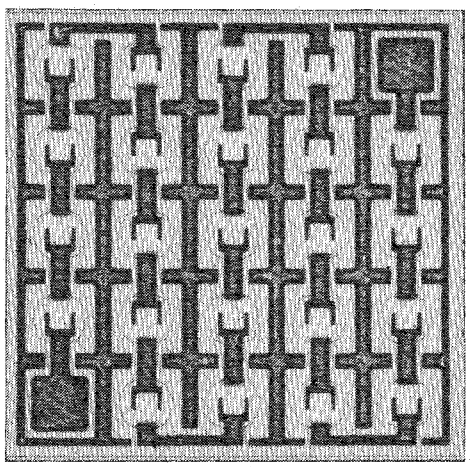

Fig. 2. Dielectrically isolated silicon 23-photodiode array microphotograph.

white epoxy resin, which prevents light absorption on the inner surface of the resin and improves the output photocurrent.

III. Experimental Results and Discussion

The output short-circuit current I_{sc} and open-circuit voltage V_{oc} for a series-connected n photodiode array are the same and n times larger than for a unit cell, respectively, under uniform illumination conditions. The I_{sc} and V_{oc} characteristics for the fabricated silicon photodiode array are shown in Fig. 3 as functions of illumination current I_{LED}. I_{sc} and V_{oc} are 7.7 μA and 13 V, respectively, at 10-mA illumination current. The output current and voltage are sufficient to drive diffusion self-aligned power MOSFET's with threshold voltages lower than 5 V. The 100-μW output power P_o is obtained under the same conditions, where P_o is defined as the product of I_{sc} and V_{oc} and is independent of the number of photodiodes used.

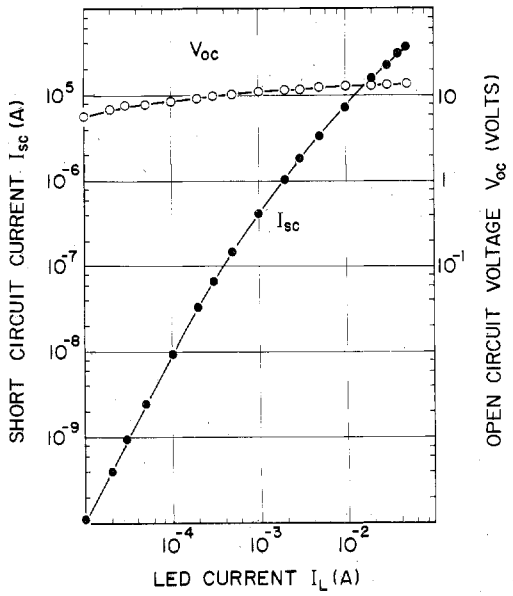

Fig. 3. Photodiode array output current and voltage versus LED illumination current.

Full dielectric isolation was performed with high production yield, using the wafer direct-bonding method. No enhanced wafer warpage appeared in the substrate formation process. The most attractive feature of the wafer direct-bonding method is that the DI wafers are free from wafer-bending troubles. Degradation of electrical characteristics was not expected because the active semiconductor devices are installed in single-crystal tubs free from excess crystalline defects related to the isolation process. Neighboring tubs are isolated from each other by V grooves with oxidized sidewalls and filled with polycrystalline silicon. The window width for V-groove anisotropic etching is about two times greater than the single-crystal tub thickness. Therefore, V-groove separation is not always profitable from the viewpoint of area utilization. Recent progress in reactive ion etching (RIE) technology has realized narrow and deep trenches with an aspect ratio larger than 5 [12]. This RIE technology could be applied for DI in neighboring tubs and could improve the packing density considerably.

In the anisotropic etching process, an undercut appeared at the corner of the rectangular mask patterns due to enhanced etching of the (211) faces. However, it is found that the undercut is prevented by employing a horn-shaped corner pattern with angles smaller than 90°.

The polycrystalline silicon area on the top surface was estimated to be about 55 percent in the photodiode array designation. To eliminate light absorption in this region and to improve output power, aluminum light reflectors were formed over it, made from the same material as the electrodes.

IV. Conclusions

A dielectrically isolated silicon p-n junction photodiode array was fabricated on a (100) silicon substrate, isolated from the handle wafer, using the wafer direct-bonding method. Neighboring single-crystal tubs were fully isolated dielectri-

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cally by V grooves along the ⟨110⟩ direction formed by anisotropic chemical etching. The V grooves, whose sidewalls were oxidized, were filled by polycrystalline silicon. The top surface was planarized by a chemical polishing process. No excess wafer warpage appeared in this DI method. Following the substrate formation, p-n junction photodiodes were installed, one in each tub, by conventional impurity diffusion technologies.

The series-connected silicon 23-photodiode array, coupled with a GaA1As infrared LED, produces a 13-V open-circuit voltage and a 7.7-μA short-circuit current at 10-mA illumination current. A 100-μW output power, the product of the open-circuit voltage and the short-circuit current, is obtained under the same conditions. The open-circuit voltage is sufficient to drive power MOSFET's with threshold voltages lower than 5 V.

It is expected that the new DI method, by wafer direct bonding, will be applicable to forthcoming high-voltage integrated circuits for industrial use and for household appliances.

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