

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,

Petitioner,

v.

ALIDDOUBLE, INC.,

Patent Owner.

IPR2023-00374

U.S. Patent No. 6,168,965

PATENT OWNER'S RESPONSE

UNDER 37 C.F.R. § 42.107

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Exhibit No.	Exhibit Name
2014	Declaration of Ron Maltiel
2015	Curriculum Vitae, Ron Maltiel

I. INTRODUCTION

Alidouble, Inc. (“Alidouble” or “Patent Owner”) submits this Patent Owner’s Response to Taiwan Semiconductor Manufacturing Company Ltd.’s (“Petitioner” or “TSMC”) Petition challenging Claims 1, 2, 7-10 of U.S. Patent No. 6,168,965. Ex. 1001 (hereinafter, the “’965 Patent”). For the reasons discussed below, the Petitioner has not shown that the references or combinations of references upon which Petitioner relies satisfies Petitioner’s burden to establish by a preponderance of the evidence that claims 1, 2, 7-10 of the ‘965 Patent are unpatentable. *See* 35 U.S.C. § 316(e).

II. THE ‘965 PATENT

The ‘965 Patent is entitled *Method For Making Backside Illuminated Image Sensor*, was filed on August 12, 1999, and issued to Yacov Malinovich and Ephie Tivon as inventors on January 2, 2001. ‘965 Patent, Cover Sheet.

A. The Technology Of Backside Illuminated Image Sensors

Solid state image sensors are used in video cameras and are in integrated circuits using a complementary metal oxide semiconductor (“CMOS”) technology. These image sensors are based on a two-dimensional array of pixels where each pixel includes a sensing element – a photo diode - that is capable of converting a portion of an optical image into an electronic signal and includes circuitry to measure the intensity of light detected by the sensing element and then to generate electronic

signals are then used by other circuitry to regenerate the optical image on a display. Ex. 2014 (Declaration of Ron Maltiel, ¶42 (hereinafter “Maltiel Decl.”)). CMOS image sensors were first developed in 1967 and utilize the photovoltaic response. *Id.* at ¶42. The photovoltaic response occurs when silicon is exposed to light and photons in the visible and near-IR regions of the spectrum impinge on a silicon surface and have sufficient energy to break covalent bonds to create an electron-hole pair. *Id.* at ¶42. The number of electrons generated is proportional to the light intensity. *Id.* at ¶42.

CMOS image sensors (“CIS”) have benefited from advances in CMOS technology for microprocessors and application specific integrated circuits. *Id.* at ¶43. Shrinking lithography, coupled with advanced signal-processing algorithms provide for sensor arrays, sensor array control, and image processing on one integrated circuit manufactured using well-established CMOS techniques. *Id.* at ¶43.

In frontside illuminated image sensors (“FSI”), the frontside surface of the semiconductor substrate includes the image sensor, the CMOS circuitry, and metal lines, manufactured of metals or polysilicon, that connect the image sensors to the CMOS circuitry and that connect both to peripheral circuitry that controls the image sensor in general, that transmits signals off the image sensor, that receive, interpret, and implement control signals from off the image sensor, and that provide power and power control to all the circuits and sensors. Maltiel Decl., ¶44.

CMOS Image Sensors (CIS) may be either FSI or BSI; the difference between a BSI image sensor and an FSI image sensor is the arrangement of imaging elements in the sensor with respect to incident light to the pixel. In FSI, the photons pass through the metal wiring layer before they reach the image sensors (e.g., photo diodes):

[i]n a frontside illuminated (FSI) sensor (see Fig. 4. 1A), the light reaches the PD active region through the passivation, metallization, and inter-dielectric layers. Several are the loss mechanisms associated with the coupling of light from the frontside of the sensor the reflection of light from the metal control lines which surround the PD [photodiode]

Ex. 2001 at 95; Maltiel Decl., ¶45. In contrast, in a BSI image sensor, the photons reach image sensors directly from the backside without passing through the metal wiring layer on the front side:

[a] BSI sensor contains the same components as a FSI sensor but the sensor's metals are located behind the PD [photodiode]

Id. at 96; Maltiel Decl., ¶46.

In BSI image sensors, the photons reach photodiodes directly without passing through metal wiring layer. Maltiel Decl., ¶46.

Although BSI image sensors contain the same components as FSI, the BSI's metal wiring layers are located behind the photodiode with respect to the direction of photons. Maltiel Decl., ¶¶ 42-46. The main technological challenge associated with producing BSI is the bonding of the original wafer to a protective substrate to

provide structural support while the semiconductor substrate is being grinded down to a thickness of a few microns. Maltiel Decl., ¶¶ 42-46.

B. The Invention Of The ‘965 Patent

The '965 patent is directed generally to methods of manufacturing BSI image sensors. Maltiel Decl., ¶47. The ‘965 patent discloses that the traditional BSI image sensors are expensive because:

(1) they are made using nonstandard complementary metal-oxide-semiconductor (CMOS) processes and

(2) packaging the BSI image sensors is complex.

’965 Patent, 4:13-29. To address these problems, the '965 patent discloses an innovative method for making and packaging BSI image sensors using standard wafer processing techniques and equipment. *Id.* at 8:47-50; Maltiel Decl., ¶47.

The ‘965 Patent discloses and claims a method for producing a back-illuminated CMOS image sensor that includes a matrix of pixels that are fabricated on a semiconductor substrate that utilizes conventional CMOS fabrication processes and that minimizes the fabrication and production costs associated with conventional CMOS fabrication processes. Maltiel Decl., ¶48.

The ‘965 Patent discloses the semiconductor substrate is secured to a protective substrate by an adhesive so that the frontside surface of the semiconductor substrate – the surface that is processed to fabricate the CMOS image sensor,

including the matrix of pixels – so that the frontside surface faces the protective substrate. ‘965 Patent, 4:54-61; Maltiel Decl., ¶49.

The protective substrate provides structural support to the semiconductor substrate and exposes the backside surface of the semiconductor substrate. The ‘965 Patent discloses grinding, chemical etching, or both the exposed backside of the semiconductor substrate to thin the semiconductor substrate advantageously to a range of 10 to 15 microns. ‘965 Patent, Abstract, 5:2-4, 7:33-37, 9:19-22, and 11:44-46; Maltiel Decl., ¶¶ 50.

The ‘965 Patent then discloses securing a transparent substrate to the backside surface of the semiconductor substrate so that light may transmit through the transparent substrate. Thus, the ‘965 Patent discloses sandwiching the semiconductor substrate between the transparent substrate and the protective substrate. ‘965 Patent, Abstract, 5:8-1-2, 8:40-42, 9:12-15, 10:60-63, 11:28-33; Maltiel Decl., ¶51.

III. PERSON OF ORDINARY SKILL

The ‘965 Patent describes and claims an invention relating to “[a] method for producing a back-illuminated CMOS image sensor” ‘965 Patent, Abstract. In view of the ‘965 Patent’s specification, claims and prosecution history, in my opinion, a POSITA would have at least a bachelor’s degree in electrical engineering, chemical engineering, or material science. Maltiel Decl., ¶¶ 25-26. In addition, a

POSITA would have 3-5 years' experience that includes some experience in image sensors. *Id.* at ¶¶ 25-26.

IV. CLAIM CONSTRUCTION

A. Claim Construction Standard

In *inter partes* review, patent claims are construed under the *Phillips* standard, 37 C.F.R. § 42.100, according to their “ordinary and customary.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005) (*en banc*); 37 C.F.R. § 42.100(b). Under *Phillips*, “the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Id.* at 1313. “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

B. Terms for Construction

1. “Effectively Exposed” – Claim 1

Claim 1 is the only independent claim and includes the limitation “effectively exposed.” ‘965 Patent, 11:24-28. “Effectively exposed” is properly interpreted as the specification defines it:

the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through second surface.

Ex. 1001, 6:48-51 ("The term 'effectively exposed' herein is used to indicate ...").

An inventor may define specific terms used to describe invention. *See In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994); *Commscope Tech. LLC v. Dali Wireless, Inc.*, 20223 WL 5053347 (Patent Tr. & App. Bd. July 21, 2023) (citing *In re Paulsen*, 30 F.3d at 1480). In addition, the Manual for Patent Examining Practice states:

an applicant is entitled to be his own lexicographer; where an explicit definition is provided by the applicant for a term, that definition will control interpretation of the term as it is used in the claim

Manual for Patent Examining Practice 2111.01.IV.A.

2. “Protective Substrate” – Claim 1

Claim 1 includes a limitation, “a protective substrate,” that should be construed to require that the protective substrate provide structural support to the semiconductor substrate.

The abstract of the ‘965 patent discloses that “the *protective substrate provid[es] structural support*” ‘965 Patent, Abstract (emphasis added). The specification explains that “because the method utilizes *a protective substrate to support the semiconductor substrate*, the thinning process is less expensive to perform.” *Id.* at 4:48-50 (emphasis added). The intrinsic disclosure is consistent with the plain and ordinary meaning as understood by a POSITA that the protective substrate is configured to provide structural support to the semiconductor substrate. Ex. 2001 at 2 (disclosing that the main technological challenge associated with

producing BSI is the bonding of the original wafer containing photodiodes to a protective substrate to provide structural support while the original wafer is being grinded down to a thickness of a few microns); Ex. 2002 at 476 (discussing the challenges that backside grinding increases chip failures because of die cracks by stating “[h]owever, die cracks still originate from flaws on the back side due to backgrinding operations used to manufacture thin packages.”); Ex. 2003 at 1 (discussing backside grinding induces damage in the wafer that leads to crack propagation by stating “[g]rind processes will induce damage in the wafer backsurface that can lead to crack propagation, growth, and fracture).

3. Claim 2

Petitioner would interpret Claim 2 to eliminate the effect of the limitations.

Claim 2 states:

2. The method according to claim 1, wherein the step of securing the protective substrate onto the first surface comprises *depositing an adhesive onto the protective substrate, and then placing the wafer onto the protective substrate* such that the first surface contacts the deposited adhesive.

‘965 Patent, 11:33-38 (Claim 2, emphasis added). Petitioner has read the limitations out of Claim 2:

A POSITA would also readily recognize that when bonding two surfaces together, adhesive must first be placed on at least one of those surfaces. . . . In the context of bonding the wafer to the protective substrate, there are only three choices: the adhesive could be placed on the wafer, the protective substrate, or both. . . . *Whichever of the three choices is used during the manufacturing process is merely a design*

choice. Uber Techs., Inc. v. X One, Inc., 957 F.3d 1334, 1340 (Fed. Cir. 2020) (in choosing between “terminal-side plotting” or “server-side plotting,” “[a] person of ordinary skill would therefore have two predictable choices for when to perform plotting providing them with a simple design choice Because a [POSITA] has ‘good reasons to pursue the known options within his or her technical grasp,’ § 103 bars the patentability

Petition, 36 (emphasis added).

Petitioner is wrong and is attempting to eliminate the requirements of Claim

2. As a first matter, claims are to be interpreted with an “eye toward giving effect to all terms in the claim.” *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006); *Cat Tech LLC v. TubeMaser, Inc.*, 528 F.3d 871, 885 (Fed. Cir. 2008); *Apple, Inc. v. Memory Integrity LLC*, 2015 WL 2251216, *7 (Patent Tr. & App. Bd. 2015); *Commscope Tech LLC v. Dali Wireless, Inc.*, 2023 WL 5053347, *7 (Patent Tr. & App. Bd. 2023).

V. SUMMARY OF PETITIONER’S CITED REFERENCES

Petitioner cites three references, Nixon, Assadi, and Badihi, as primary references.

A. Nixon

Nixon is a U.S. patent, Ex. 1004 (hereinafter, “Nixon”), claiming priority to the Nixon Provisional Application. Ex. 1005 (hereinafter, “Nixon Prov.”). The Nixon Provisional Application includes two documents: (1) an Invention Disclosure Technical Description (“IDTD”); and (2) an article entitled “A CSP Optoelectronic

Package for Imaging and Light Detection Applications" by Shweky *et al.* ("Shweky"). Ex. 1047 (hereinafter, "Shweky"). The IDTD has very limited information with an only one and half page written description and two hand-sketched figures. Nixon Prov., 4-6.

Nixon includes no disclosure of order of applying adhesive to a protective substrate or to a semiconductor substrate. Maltiel Decl., ¶¶ 67-71.

While in Nixon, metal leads are connected to pads on the back side as described in Fig. 3 steps 335 "Apply lead deposition to backside" and described in the specification:

Proceeding to state 335, a metal layer is deposited to contact each pad at its cross section as seen in FIG. 4F. The metal layer is patterned by a lithography process into individual leads 455 that contact the pads

Nixon, 2:63-65.

Nixon does not disclose how the metal leads are connecting to the pads on the die. In figures 4C we are shown how the dies (430, green) are separated along 435, in 4D a second glass (440, yellow) is attached. In Figure 4E opening for metal leads along 450 are created, and in Figure 4F, metal leads are deposited.

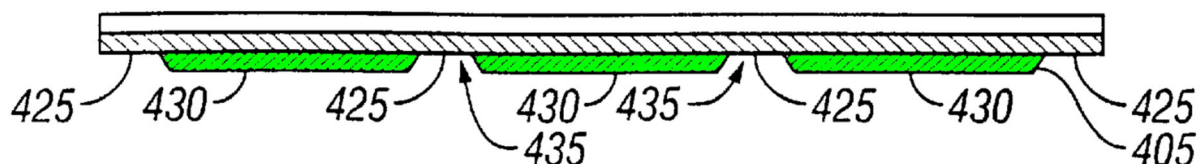


FIG. 4C

Nixon, Fig. 4C.

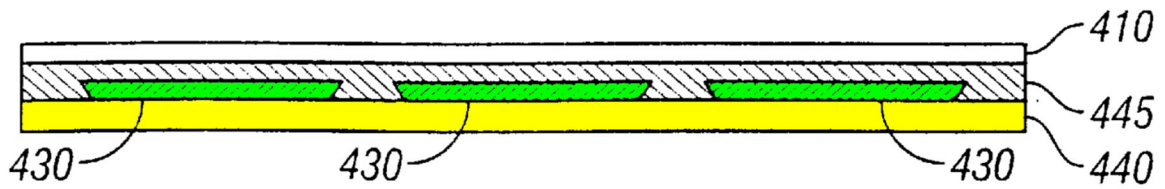


FIG. 4D

Nixon, Fig. 4D.

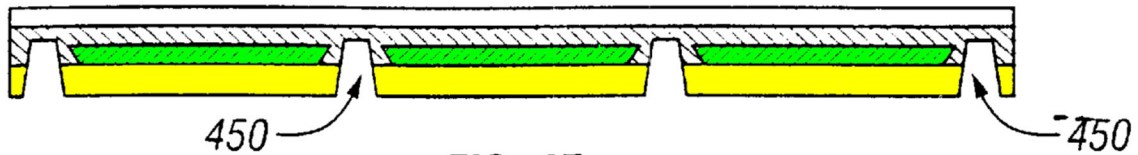


FIG. 4E

Nixon, Fig. 4E.

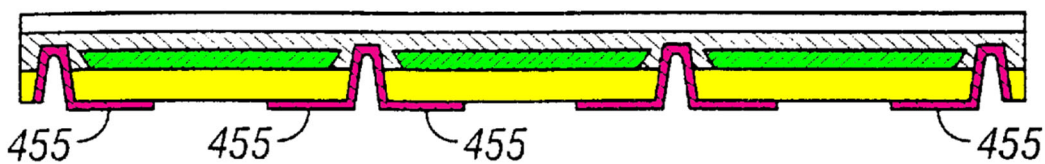


FIG. 4F

Nixon, Fig. 4F.

However, none of the metal leads (455, pink) are connected to any of the dies (430, green).

Also, figures 1 and 2 below do not show how metal leads 120 (pink) and 125 (pink) connecting pads 130 and 135 to the pixel dies 145 (green).

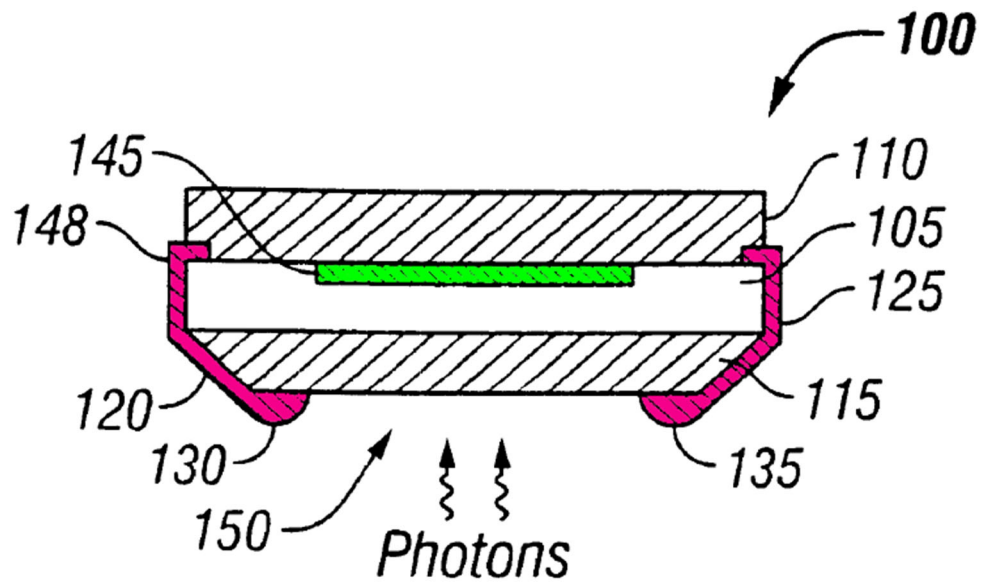


FIG. 1

Nixon, Fig. 1.

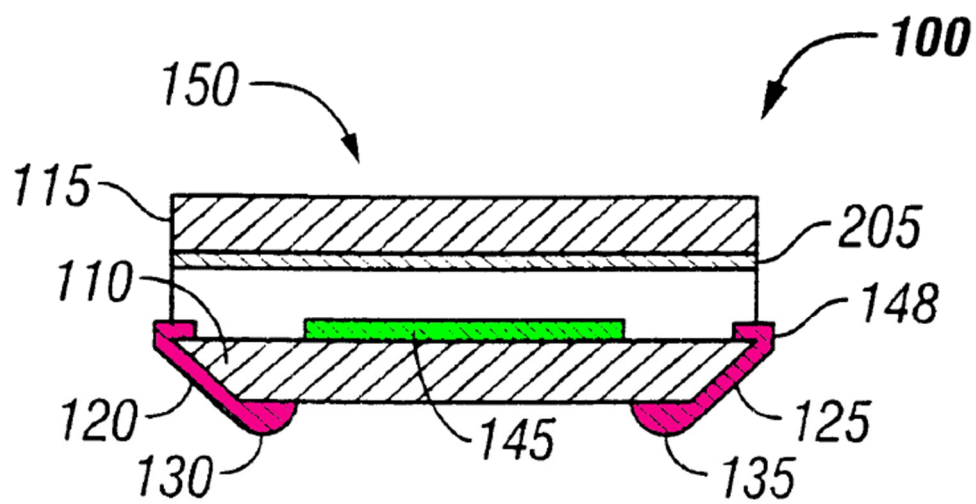


FIG. 2

Nixon, Fig. 2

Thus, Nixon does not disclose, teach, or suggest the “forming” limitation.

Maltiel Decl., ¶¶ 67-71.

B. Assadi

Assadi is a U.S. patent that Petitioner contends discloses a passivation layer 230 that “[o]verlie[ies] the top surface of image sensor 175” and is made, for example, of silicon nitride based on its “particular resistance to environmental contaminants, particularly moisture.” Ex 1044, 4:35-45, Fig. 3b; Ex. 1003 ¶78. (hereinafter, “Assadi”). Petitioner also contends that Assadi discloses bond pads 225 which may be on the “top surface of sensor 176” and in bond pad area 240 and that the passivation layer 230 “overlies the entirety of sensor 175, including . . . bond pad area 240.” Assadi, ¶¶ 151 - 53.

Assadi does not include disclosure of an order of applying adhesive to a protective substrate or to a semiconductor substrate. Maltiel Decl., ¶¶ 72-73.

C. Badihi

Badihi is a printed publication published in the Proceedings International Symposium of Advanced Packaging Materials, Processes, Properties and Interfaces. Ex. 1101 (hereinafter, “Badihi”). The paper is entitled: *Shell Case Ultrathin Chip Size Package*, and is not related to backside image sensor processing. *Id.*; Maltiel Decl., ¶¶ 74-75. A POSITA would not understand or be motivated to not apply the method disclosed in Badihi to manufacturing BSI image sensors because any disclosure by Badihi relating to thinning a wafer does not take into account the requirements of maintaining the wafer properties that would allow for electron flow

generation. Maltiel Decl., ¶¶ 74-75.

Badihi includes no disclosure of order of applying adhesive to a protective substrate or to a semiconductor substrate. Maltiel Decl., ¶¶ 74-75

VI. APPLICABLE LEGAL STANDARD

Petitioner only asserts grounds based on obviousness, 35 U.S.C. Section 103. The Supreme Court has determined that when analyzing a claim for validity under Section 103:

a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 418-19 (2007). For this reason:

it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does

Id. at 418. "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art." *In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988).

[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.

KSR Int'l Co., 550 U.S. at 418. "This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries

almost of necessity will be combinations of what, in some sense, is already known.” *Id.* at 418-419. For this reason, “it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.” *Id.* at 418. “One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art.” *In re Fine*, 837 at 1075.

“[M]ere conclusory statements” are not sufficient. *Wowza Media Sys., LLC v. Adobe Sys. Inc.*, IPR2013-00054, 2013 WL 5653113, at *8 (Patent Tr. & App. Bd. April 8, 2013). “In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). The burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

To carry its burden, a petitioner must both:

clearly point out the differences between the claimed invention and [the prior art] and

explain why a person of ordinary skill in the art would have found the claimed subject matter obvious in spite of those differences.

Synopsys, Inc. v. Mentor Graphics Corp., IPR2012-00041, 2013 WL 3355865 at *8 (Patent Tr. & App. Bd. Feb. 22, 2013). A petitioner must specifically recite where the challenged limitation is found in the secondary reference(s) and must explain

why a POSITA would have modified the primary reference with the recited limitation from the secondary reference(s). *See Microsoft Corp. v. Secure Web Conf Corp.*, IPR2014-00745, 2014 WL 4925718, at *6-7 (P.T.A.B. Sept. 29, 2014).

VII. THE CITED PRIOR ART DOES NOT INVALIDATE THE CHALLENGED CLAIMS

A. Ground 1: Nixon Does Not Render Claims 1, 2, 7, 8, Or 9 Obvious

1. Claim 1

Petitioner has failed to carry its burden of establishing that Nixon renders Claim 1 obvious. *Harmonic Inc.*, 815 F.3d at 1363; *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d at 1378.

Claim 1 recites “effectively exposed”:

removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are *effectively exposed* through the second surface.

‘965 Patent, 11:24-27 (emphasis added). As explained above in Section IV.B.1, the inventors define the “effectively exposed” to require “the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through second surface.”

Petitioner asserts that this limitation is disclosed because Nixon discloses:

removing material from the second surface of the wafer to "a predetermined thickness that allows for the light sensitive area of the die 430 to be illuminated from ... the back side."

Pet. at 31. Petitioner, however, has presented no evidence that Nixon discloses that

electron flow is generated with the light sensitive pixel regions (*i.e.*, the image sensor) is exposed to light (photons) after the grinding/thinning process. Maltiel Decl., ¶¶ 77-80. A POSITA would have known that the grinding/thinning process is not exclusively for exposing light-sensitive pixel regions to generate electron flow. *See e.g.*, Ex. 2002 at 20, 66, 71, 74 (discussing flip-chip, *i.e.*, back-side processed chips, have general advantages in decreasing electromagnetic effects, increasing interconnection capability, and their applications in high performing I/O packaging, all of which have nothing to do with effectively exposing CMOS photodiodes); *see also* Ex. 2005 (in its Abstract: "[t]his paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in packaging, *i.e.*, A technology for processing silicon dies with a thickness of 100 um or less and a technology for handling thinning ultrasmall dies."); *see also* Exs. 2006, 2007, 2008 (where the grinding/thinning process is performed in general semiconductor packaging rather than image sensors); *see also* Ex. 2003 at 1 (discussing dies with back-grinding are routinely used for its advantage of better heat dissipation, which is important for high-power RF chips. Maltiel Decl., ¶¶ 77-80. A POSITA would know that back-grinding process is routinely used in packaging technology that is not related to "effectively exposing" CMOS photodiodes.) The grinding/thinning process is not just exclusively for image sensors, *i.e.*, for exposing light-sensitive pixel regions to

generate electron flow. Maltiel Decl., ¶¶ 77-80.

A POSITA would understand that electron flow would not necessarily be generated when the light-sensitive pixel regions of each image sensor circuit are illuminated because, for example, there may be an illumination threshold that has to be reached before electron flow is generated. See *e.g.*, Ex. 2009 (discussing how the threshold of silicon photodiodes should be designed to reduce noise interference and yet preserve high sensitivity); *see also* Ex. 2010 (discussing how to improve threshold uniformity among photodiodes in an array to increase the quality of imaging); Ex. 2011 (discussing how to tune thresholds of photodiodes to reduce current contamination to neighboring photodiodes, *e.g.*, antiblooming photodiodes); *see also* Ex. 2012 (indicating the threshold of the photodiodes used in the research is lower than 5V); Maltiel Decl., ¶¶ 77-80.

Accordingly, Nixon does not disclose, teach, or suggest the “effectively exposed.” So Nixon does not render Claim 1 obvious.

2. Claim 2

Claim 2 depends from Claim 1.

First, Nixon does not render Claim 2 obvious because Nixon does not render Claim 1 obvious. *See Rembrandt Wireless Techs., LP v. Samsung Elecs. Co.*, 853 F.3d 1370, 1380 (Fed. Cir. 2017) (citing, *In re Fine*, 837 F.2d at 1076 (“Dependent claims are nonobvious under section 103 if the independent claims from which they

depend are nonobvious.”).

Second, Claim 2 states:

The method according to Claim 1, wherein the step of securing the protective substrate onto the first surface comprises depositing an adhesive onto the protective substrate, and then placing the wafer onto the protective substrate such that the first surface contacts the deposited adhesive.

‘965 Patent, 11:34-40 (Claim 2).

Nixon has no disclosure, teaching, or suggestion relating to applying adhesive to the wafer - semiconductor substrate - or to the protective substrate. Maltiel Decl., ¶¶54-55. Claim 2 is to be applied to give effect to all limitations. *Bicon, Inc.*, 441 F.3d at 950; *Cat Tech LLC*, 528 F.3d at 885; *Apple, Inc.*, 2015 WL 2251216, *7; *Commscope Tech*, 2023 WL 5053347, *7.

In addition, Claim 2 is not a “simple design choice.” Maltiel Decl., ¶¶ 54-55; *contra* Petition, 36. It is important sequence for several reasons. Keeping the wafer surface away from the adhesive and the protective substrate reduces the chance of particles landing on the surface of the semiconductor substrate. Maltiel Decl., ¶¶ 54-55. Particles landing on the wafer will cause image sensor failures and malfunctions. *Id.* Applying the adhesive to the protective substrate minimizes exposure of the surface of the wafer, keeping it clean and free of particles. *Id.* Further, applying adhesive to both protective substrate and the wafer surface would make it difficult to control the total thickness, flatness, and level of the adhesive

layer across the semiconductor substrate. *Id.* Uneven adhesive thickness will cause non-uniformities and failures in grinding and etching the second surface of the semiconductor substrate. *Id.* Finally, applying the adhesive to the semiconductor substrate first or applying to both the semiconductor substrate and the protective substrate may, in subsequent masking steps, cause the dies – across the semiconductor substrate - the not to have the same length for the field of focus because the height of each die's surface will vary depending on the local adhesive thickness. *Id.*

3. Claim 7

Claim 7 depends from Claim 1. Nixon does not render Claim 7 obvious because Nixon does not render Claim 1 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

4. Claim 8

Claim 8 depends from Claim 7. Nixon does not render Claim 8 obvious because Nixon does not render Claim 7 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

5. Claim 9

Claim 9 depends from Claim 1. Nixon does not render Claim 9 obvious because Nixon does not render Claim 1 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

In addition, Claim 9 includes the limitation:

Forming the metal on the protective substrate after the step of securing the transparent substrate, wherein the metal leads are connected to the metal contact pads located on the first surface of the wafer

‘965 patent, 12:33-36. Nixon fails to disclose, teach, or suggest this limitation.

Maltiel Decl., ¶¶87-91.

Nixon discloses metal leads are connected to pads on the back side as described in Fig. 3 steps 335 “Apply lead deposition to backside” and described in the specification:

Proceeding to state 335, a metal layer is deposited to contact each pad at its cross section as seen in FIG. 4F. The metal layer is patterned by a lithography process into individual leads 455 that contact the pads

Nixon, 2:63-65. Nixon, however, does not disclose how the metal leads are connecting to the pads on the front surface of the die. Maltiel Decl., ¶¶ 88-89. In Figure 4C Nixon shows the dies (430, green) are separated along 435, in 4D a second glass (440, yellow) is attached. Maltiel Decl., ¶¶ 88-89. In Figure 4E, Nixon shows openings for metal leads along 450 are created, and in Figure 4F, metal leads are deposited. Nixon, Figs. 4E & 4F; Maltiel Decl., ¶¶ 88-89.

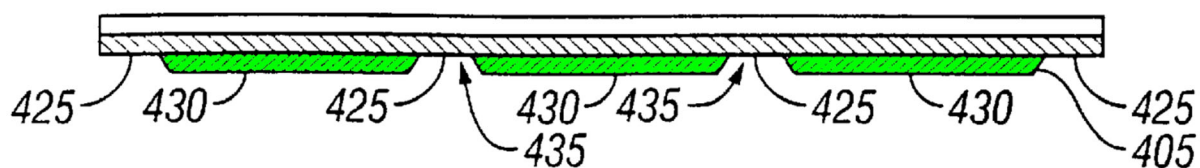


FIG. 4C

Nixon, Fig. 4C.

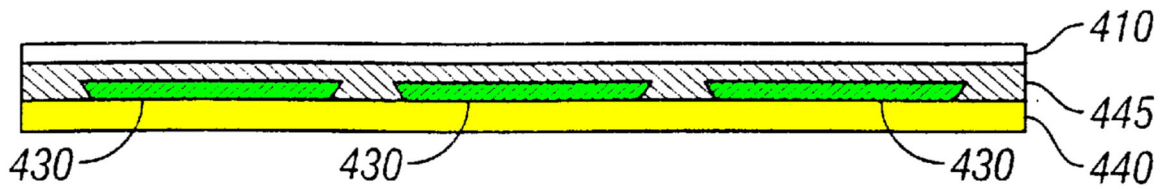


FIG. 4D

Nixon, Fig. 4D.

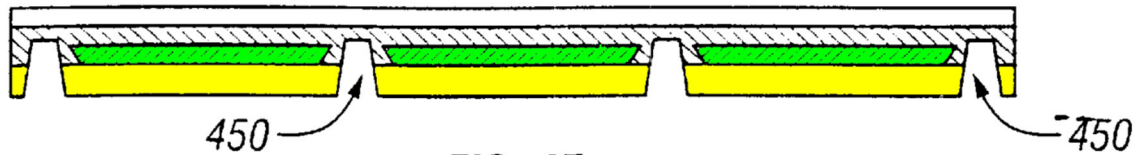


FIG. 4E

Nixon, Fig. 4E.

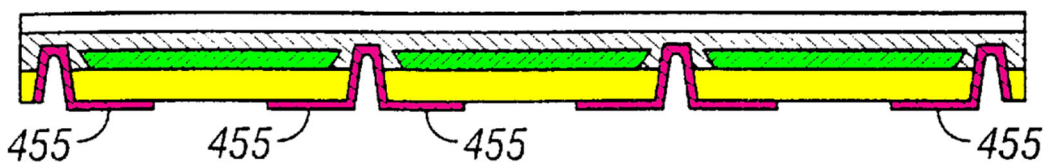


FIG. 4F

Nixon, Fig. 4F.

However, none of the metal leads (455, pink) are connected to any of the dies (430, green). Maltiel Decl., ¶¶ 88-89.

Also figures one and two below do not show how metal leads 120 (pink) and 125 (pink) connecting pads 130 and 135 to the pixel dies 145 (green).

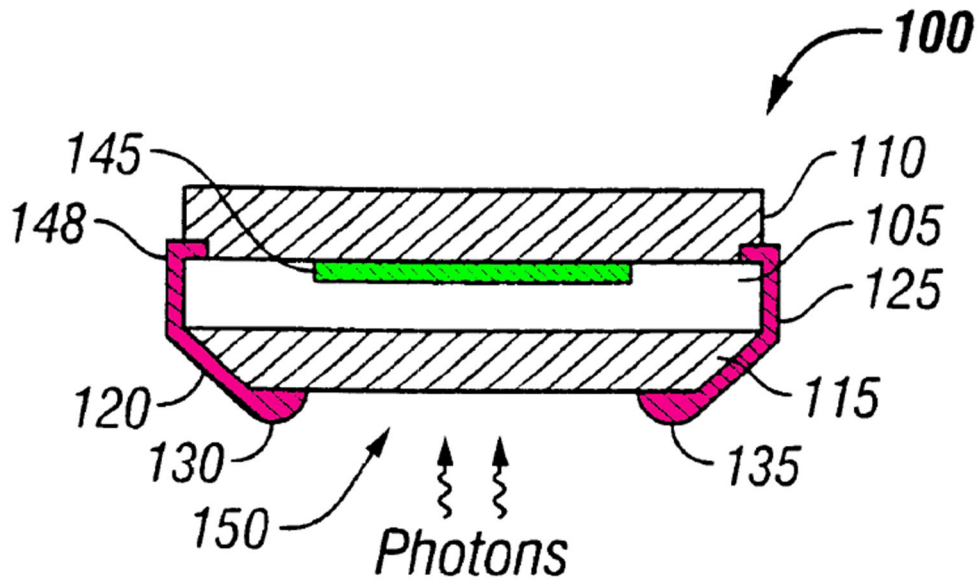


FIG. 1

Nixon, Fig. 1.

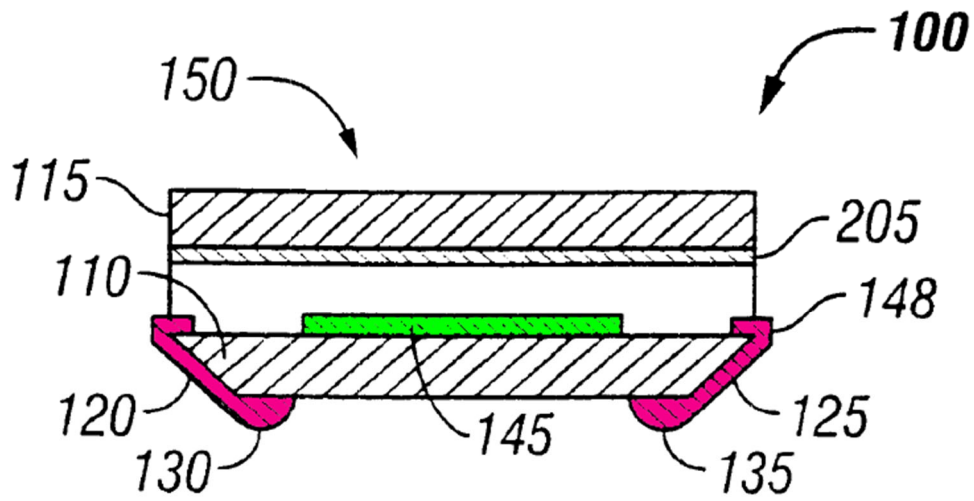


FIG. 2

Nixon, Fig. 2.

Thus, Nixon does not disclose, teach, or suggest the “forming” limitation.

Maltiel Decl., ¶¶ 90-91.

B. Ground 2: Nixon In View of Assadi Does Not Render Claim 10 Obvious

Petitioner has failed to carry its burden of establishing that Nixon in view of Assadi renders Claim 10 obvious. *Harmonic Inc.*, 815 F.3d at 1363; *Dynamic Drinkware*, 800 F.3d at 1378.

Claim 10 depends from Claim 1. Nixon fails to render claim 1 obvious, and Petitioner has not cited Assadi against Claim 1. Thus, Petitioner has not carried its burden of establishing that Nixon in view of Assadi renders Claim 10 obvious. *See Rembrandt Wireless Techs.*, 853 F.3d at 1380.

C. Ground 3: Badihi Does Not Render Claims 1, 2, 7, 8, 9 Obvious

Petitioner has failed to carry its burden of establishing that Badihi renders Claims 1, 2, 7, 8, or 9 obvious. *Harmonic Inc.*, 815 F.3d at 1363; *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d at 1378.

1. Claim 1

a. “Backside Illuminated Image Sensors”

Claim 1 includes the limitation “backside illuminated sensors.” ‘965 Patent, 11:32. Badihi does not disclose or render obvious the “backside illuminated image sensors” limitation. Maltiel Decl., ¶¶ 93-96. Petitioner admits that Badihi’s disclosures are not specific to producing image sensors. Pet. at 56. Badihi is directed to general backside grinding and packaging of wafer that may not have any implication to BSI image sensors. *See e.g.*, Ex. 2002 at 20, 66, 71, 74 (discussing

flip-chip, i.e., back-side processed chips, have general advantages in decreasing electromagnetic effects, increasing interconnection capability, and their applications in high performing 1/0 packaging, all of which have nothing to do with BSI image sensors); *see also* Ex. 2005 (in its Abstract: "[t]his paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in packaging, i.e., A technology for processing silicon dies with a thickness of 100 um or less and a technology for handling thinning ultrasmall dies."); *see also* Exs. 2006, 2007, 2008 (where the grinding/thinning process is performed in general semiconductor packaging rather than image sensors); Ex. 2003 at 1 (discussing dies with back-grinding are routinely used for its advantage of better heat dissipation, which is important for high-power RF chips; Maltiel Decl., ¶¶ 93-96. Thus back-grinding process is routinely used in packaging technology and is not related to BSI image sensors). *Id.* at ¶¶ 93-96.

Petitioner asserts that a POSITA would understand that Badihi could be used for BSI CMOS image sensors. Pet. at 56. Petitioner's citation is merely to its own expert. The Petition and Petitioner's expert's argument is a mere conclusory statement that cannot establish that a POSITA would understand that the general packaging process taught by Badihi could be used for BSI image sensors. *Compare* Pet. at 56 with Ex. 1003, 141 (parroting same argument with the use of same

annotated Figures). Petitioner's argument is a mere parroting of a conclusory statement from its expert, it should be given no weight. *Xerox Corp. et al. v. Bytemark, Inc.*, IPR2022-00624, Paper 12 at 4-5 (Patent Tr. & App. Bd. Feb. 10, 2023) (expert declaration that offered conclusory assertions without underlying factual support and repeated, verbatim, Petitioner's conclusory arguments given little weight); *Unirac, Inc. v. Ecofasten Solar, LLC*, IPR2021-00532, 2021 WL 3116853, at *7 (Patent Tr. & App. Bd. July 22, 2021) (denying institution where "Petitioner's witness merely parrots the conclusory statements of Petitioner"); *Unified Patents Inc. v. GE Video Compression, LLC*, IPR2019-00726, 2019 WL 3714386, at *11 (Patent Tr. & App. Bd. Aug. 6, 2019) (giving little weight to expert testimony that "simply parrots the Petition without providing any basis for his opinion" and denying institution); *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) ("conclusory expert testimony is inadequate to support an obviousness determination"); *Elbit Sys. of Am., LLC v. Thales Visionix, Inc.*, 881 F.3d 1354, 1359 (Fed. Cir. 2018) ("Attorney argument is not evidence.") (quoting *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017)); *Free-Flow Packaging Int'l, Inc. v. Automated Packaging Sys., Inc.*, IPR2016-00447, Paper 7, at 10 (Patent Tr. & App. Bd. June 22, 2016) (denying institution where the petitioner's expert did "nothing more than parrot the language of the Petition word for word").

Moreover, Badihi does not disclose, teach, or suggest that its packaging

process could be applied to BSI image sensors. Maltiel Decl., ¶¶ 93-96. Although Badihi discloses that its packaging process can be readily applied to silicon light detectors, CMOS image sensors, and CCD devices, Pet. at 56; Ex. 1101 at 239, "a claimed species or subgenus is encompassed by a prior art genus is not sufficient by itself to establish a *prima facie* case of obviousness." *In re Baird*, 16 F.3d 380, 382, 29 USPQ2d 1550, 1552 (Fed. Cir. 1994); *see also* MPEP 2144.08 - Obviousness of Species When Prior Art Teaches Genus. Because a claimed species (*e.g.*, BSI image sensors) may be encompassed by a disclosed genus (*e.g.*, CMOS image sensors) does not render that species obvious, Petitioner has presented no evidence that a POSA would be motivated to apply the packaging method disclosed in Badihi for producing BSI image sensors. In this regard, Badihi does not disclose how its packaging process should be applied to BSI image sensors, and there is nothing in the prior art that even suggests how to do it. Maltiel Decl., ¶¶ 93-96. Thus, Petitioner has presented no evidence that a POSA would be motivated to apply the packaging method disclosed in Badihi for producing BSI image sensors.

b. "Protective Substrate"

Claim 1 includes a limitation "protective substrate," '965 Patent, 11:22-23, specifically, "securing the wafer onto a protective substrate such that the first surface faces the protective substrate." Badihi does not disclose, teach, or suggest the "protective substrate," so does not render Claim 1 obvious.

The alleged glass layer in Badihi does not provide any structural support. Maltiel Decl., ¶¶ 98-101.

Contrary to Petitioner's arguments, Badihi does not disclose a “protective substrate.” In Badihi, the supposed "protective substrate" asserted by Petitioner is just a thin layer of glass permitting light to go through. *See* Pet. at 61. Petitioner has presented no evidence that the identified thin layer of glass in Badihi provides any structural support. In contrast, the protective substrate in the '965 patent would have been designed to be thick enough to fulfill the purpose of providing structural support.

Badihi does not disclose, teach, or suggest a protective substrate that provides structural support according to Claim 1. Maltiel Decl., ¶¶ 98-101. A POSITA would readily know that a thin glass layer disclosed by Badihi is not a protective substrate providing structural support. Accordingly, Badihi does not render Claim 1 obvious.

c. “Effectively Exposed”

Badihi does not disclose or render obvious the “effectively exposed” limitation of Claim 1.

Claim 1 recites:

removing material from the second surface of the wafer until the light-sensitive pixel regions of each image sensor circuit are effectively exposed through the second surface.

‘965 Patent, 11:24-28. As explained above in Section IV.B.1, the inventors define

the "effectively exposed" limitation in the '965 patent to require "the pixel of each light-sensitive pixel region generates electron flow in response to light (photons) passing through second surface."

Petitioner asserts that Badihi discloses that:

the process step where the silicon wafer is grinded from its backside until 100 microns is left . . . A POSIT A would readily understand that the purpose of grinding the silicon wafer from its backside before enclosing it in a glass transparent package is so that the light-sensitive pixel regions are exposed from the backside of the silicon wafer.

Pet. at. 62-63 (citing Ex. 1003). Petitioner's argument is a conclusory statement that should be ignored because it is without any support.

First, as previously discussed, Badihi is directed to general backside grinding and packaging of wafer. *See* Section VII.C.1.a. Backside grinding was routinely known in the semiconductor packaging industry for advantages not related to image sensing. Maltiel Decl., ¶¶ 105-108; *see e.g.*, Ex. 2002 at 20, 66, 71, 74 (discussing flip-chip, *i.e.*, back-side processed chips, have general advantages in decreasing electromagnetic effects, increasing interconnection capability, and their applications in high performing I/O packaging, all of which have nothing to do with effectively exposing CMOS photodiodes whatsoever); *see also* Ex. 2005 (in its Abstract: "[t]his paper aims to realize heterogeneous integrated packaging technology for high integration by applying a thinning process technology for controlling the thickness of chipsets used in packaging, *i.e.*, A technology for processing silicon dies with a

thickness of 100 um or less and a technology for handling thinning ultrasmall dies."); *see also* Ex. 2006, 2007, 2008 (where the grinding/thinning process is performed in general semiconductor packaging rather than image sensors); *see also* Ex. 2003 at 1 (discussing dies with back-grinding are routinely used for its advantage of better heat dissipation, which is important for high-power RF chips. Thus, back-grinding process is routinely used in packaging technology that has nothing to do with effectively exposing CMOS photodiodes); Maltiel Decl., ¶¶ 105-108. Second, Badihi does not, teach, or suggest CMOS photodiodes or BSI sensors, or both. No POSITA reading Badihi would understand the general back-side grinding disclosed in Badihi is to "effectively expose" the BSI image sensors such that electron flow is generated with the light sensitive pixel regions (i.e., the image sensor) being exposed to light (photons). Maltiel Decl., ¶¶ 105-108.

Indeed, electron flow would not necessarily be generated when the light-sensitive pixel regions of each image sensor circuit are illuminated because, for example, there may be an illumination threshold that has to be reached before electron flow is generated. *See e.g.*, Ex. 2009 (discussing how the threshold of silicon photodiodes should be designed to reduce noise interference and yet preserve high sensitivity); *see also* Ex. 2010 (discussing how to improve threshold uniformity among photodiodes in an array to increase the quality of imaging); *see also* Ex. 2011 (discussing how to tune thresholds of photodiodes to reduce current contamination

to neighboring photodiodes, e.g., antiblooming photodiodes); *see also* Ex. 2012 (indicating the threshold of the photodiodes used in the research is lower than 5V); Maltiel Decl., ¶¶ 105-108..

Further for Badihi, the disclosed step of thinning/grinding is just for reducing the thickness of the silicon substrate for achieving a chip size packaging instead of illuminating the image sensor, which further eliminate the possibility of generating electron flow. Ex. 1101, 237. In summary, the thinning/ grinding process in the cited references is totally different from that of the '965 patent. Maltiel Decl., ¶¶ 105-108..

Thus, Badihi does not disclose, teach, or suggest the invention of claim 1 of the '965 patent. As stated above, Petitioner's expert report, which simply parrots the Petition, is insufficient to establish that the limitations not disclosed in Badihi would be obvious to a POSITA. *Xerox Corp*, IPR2022-00624 at Paper 12 at 4-5; *Unirac*, IPR2021-00532, 2021 WL 3116853 at *7; *Unified Patents Inc.*, IPR2019-00726, 2019 WL 3714386, at *11; *TQ Delta*, 942 F.3d at 1359; *Elbit Sys. of Am.*, 881 F.3d at 1359; *Free-Flow Packaging Int'l*, IPR2016-00447, Paper 7, at 10.

2. Claim 2

Claim 2 depends from Claim 1. Bahidi does not render Claim 2 obvious because Nixon does not render Claim 1 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

3. Claim 7

Claim 7 depends from Claim 1. Bahidi does not render Claim 1 obvious because Nixon does not render Claim 7 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

4. Claim 8

Claim 8 depends from Claim 7. Bahidi does not render Claim 7 obvious because Nixon does not render Claim 8 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

5. Claim 9

Claim 9 depends from Claim 1. Bahidi does not render Claim 1 obvious because Nixon does not render Claim 9 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380.

D. Ground 4: Badihi In View Of Assadi Does Not Render Claim 10 Obvious

Petitioner has failed to carry its burden of establishing that Badihi in view of Assadi renders Claims 1, 2, 7, 8, or 9 obvious. *Harmonic Inc.*, 815 F.3d at 1363; *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d at 1378.

Claim 10 depends from Claim 1, as Badihi fails to render claim 1 obvious, Badihi in view of Assadi does not render Claim 10 obvious. *See Rembrandt Wireless Techs*, 853 F.3d at 1380. In addition, Petitioner did not cite Assadi against Claim 1, so Petitioner has not established that Badihi in view of Assadi renders Claim 10

obvious. *Id.*

VIII. CONCLUSION

For these reasons, Patent Owner submits that Petitioner has failed to meet its burden of proving that any challenged claim of the '965 patent is unpatentable.

DATE: October 11, 2023

Respectfully Submitted,

/s/ Eric Cohen
Eric Cohen
Registration No. 27,429

Counsel for Patent Owner Alidouble Inc.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24, I hereby certify that the foregoing Patent Owner Response contains 6503 words as measured by the word processing software used to prepare the document, excluding the cover page, signature block, and portions exempted under 37 C.F.R. § 42.24.

DATE: October 11, 2023

Respectfully Submitted,

/s/ Eric Cohen
Eric Cohen
Registration No. 27,429

Counsel for Patent Owner Alidouble Inc.

CERTIFICATE OF SERVICE

Pursuant to 37 CFR § 42.6(e), the undersigned hereby certifies that a copy of the Patent Owner's Response Under 37 C.F.R. §42.107 by P-TACS electronic notification and electronic mail to each of the following individuals on the date indicated below:

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