R O N M A L T I E L

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PROFESSIONAL SUMMARY:

Mr. Maltiel is a senior member of IEEE with more than 30 years experience in all phases of design and implementation of computer semiconductor devices. He has worked in the development and production of storage technology and semiconductor devices such as Dynamic Ram (DRAM), Flash (NAND, NOR), SSD, EEPROM, ROM, and Static RAM (SRAM) memories which were used in microprocessors, logic, digital, and analog products.

Mr. Maltiel studied semiconductors at Stanford University graduate school and went on to work at Intel, AMI, AMD, and Maxim. His teams included circuit, process, and device engineers and was responsible for integrating all of the various disciplines into one working product. Mr. Maltiel holds six semiconductor device, process, and measurement patents which have been cited more than 130 times.

Currently, Mr. Maltiel is an independent consultant in the areas of semiconductor design, process and manufacturing and has been retained as an expert witness on many patent cases. In addition, Mr. Maltiel maintains an informational website and database which is regularly visited by USPTO, US Department of Justice, technology departments, attorneys, and investors from 99 countries. He is also fluent in Hebrew.

EXPERTISE:

Circuit and Process Development:
- Analog
- DRAM
- Flash / EEPROM and ROM
- SRAM
- pMOS, nMOS, and CMOS
- High voltage BICMOS

Process Steps Development:
- Process flow design
- Gate and polysilicon oxidation steps
- Metal deposition and barrier layers steps
- Etching, laser definition, poly or metal deposition and planarization process steps such as Chemical Mechanical Polishing (CMP)
- Plasma and Trench etching steps
- Cleaning and wafer gettering methods

Devices Development:
- DRAM memory cells
- SRAM memory cells
- Flash / EEPROM and ROM memory cells
- Precision resistors and capacitors
- Transistors/ resistors/capacitors/JFET in FinFET, pMOS, nMOS, CMOS, and BICMOS processes
- Polysilicon - polysilicon capacitors
- PNP and NPN transistors

Test Chip Development:
- Created a library of test chip structures for process, ESD circuits, design rules, and device evaluation using GDS tools.
- Measured test structures and evaluated their device properties

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PROFESSIONAL EXPERIENCE

INDEPENDANT CONSULTANT, 1993 - present

- Provides consulting in various aspects of semiconductor technology and semiconductor manufacturing.
- Provides expert technical consultations and has testified at trials.
- Designs and operates a popular semiconductor technology web site which includes current developments in the digital and analog fields such as DRAM, Flash (NAND, NOR), SSD, EEPROM, ROM, and SRAM. The site includes tutorials and educational information, industry news and resources, acronym and technical word definitions, and patent search or patent application information, and is regularly visited by major technology companies and universities from 99 countries.

MAXIM INTEGRATED PRODUCTS , 1989 - 1993

- Personally developed a high voltage BICMOS device, introduced it to production, and proved the feasibility of adding an EEPROM element to it.
- Established MAXIM processes in a newly purchased fab, developed the company's newest analog process, installed MAXIM's production in a new foundry, and managed the relationship.

ADVANCED MICRO DEVICES , 1983 -1989

- Managed consolidation of test chip development through the building of a company-wide standard test chip library. As a direct result of this project, the time needed to build test chips was reduced by 60%, structures were improved, and test program generation was accelerated.
- Contributed to development of 256k SRAM, including process flow, a backend planarization scheme, and overseeing the building of generic test chip library.
- Participated in defining 1M CMOS DRAM memory and proved feasibility of integrating trenches in the process. Coordinated the development of post groove planarization process and double poly module. The project ended successfully with a working first silicon.
- Developed and proved feasibility of integrating EEPROM with DRAM CMOS process and devices. Reduced cell size by 40%, process steps by 15%, and improved EEPROM programming operation.

AMERICAN MICROSYSTEMS, INC., 1982 - 1983

- Introduced and established the EEPROM device. Directed the design of the test chip, process flow determination, manufacture of several working runs and measurement of the electrical parameters.
- Created a new process approach that improves poly dielectric strength and founded a new cell structure with multiple benefits over existing cells.

INTEL , 1980 - 1982

Participated in the development of EEPROM technology with particular emphasis on the reliability aspects such as charge retention and cycling endurance. Work involved the study of failure mechanisms, making the necessary process changes, and evaluating the results. Regular interaction with fab and technology development was required. Improved operator utilization by 20%.

STANFORD UNIVERSITY , 1978 - 1980

- E.E. research group on metallic impurities and their electrical behaviors.
- Independent research included manufacturing of Si devices and electrical measurements of their properties.

EDUCATION

Engineer Degree, Material Science Engineering, Stanford University, 1980
MS, Material Science and Engineering, Stanford University, 1978
BS, Material Science and Engineering, Ben-Gurion University, 1977

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PATENTS

Mr. Maltiel's patents have been cited more than 130 times

- Electrical measurements of profile of semiconductor devices during their manufacturing process - #4,978,923
- Method and apparatus for non-destructive data in a shadow memory array - #4,716,552
- Electrical measurements of properties of semiconductor devices during their manufacturing process - # 4,956,611
- Memory cell providing simultaneous non-destructive access to volatile and non-volatile data - #4,672,580
- Non-volatile dynamic ram cell - #4,611,309
- Gold-doped IC resistor region - #4,432,008

PROFESSIONAL AFFILIATIONS

IEEE Senior Member
IEEE Device Society
IEEE Circuits Society
IEEE Communications Society
IEEE-USA Consultants Database
Jewish High Tech

LITIGATION RELATED EXPERIENCE

Expert Engagements

Patent Infringement
Semiconductor Design and Analysis Firm: MOSAID Technologies
Case Name: **MOSAID Technologies** arbitration with TSMC.
Services Provided: Technical consulting expert on semiconductor processes and manufacturing. Reviewed infringing patents. Wrote declarations. The case was settled successfully.
Date: 2021

Type of Matter: Patent Infringement
Law Firm: Devlin Law Firm
Case Name: **Ocean Semiconductor** vs Analog Devices, Infineon, MediaTek, NVIDIA, NXP, Renesas, Silicon Labs, STMicroelectronics, Western Digital and Huawei.
Services Provided: Technical consulting expert on semiconductor development and manufacturing cases. Reviewed infringing patents. Wrote declarations and was deposed.
Date: 2020-2

Type of Matter: Patent Infringement
Law Firm: Quinn Emanuel
Case Name: **IP Bridge** vs Micron.
Services Provided: Technical consulting expert on semiconductor development and manufacturing case. Reviewed infringing patents, contact and metallization manufacturing processes, and layout files. Wrote a declaration and the case was settled successfully.
Date: 2020

Type of Matter: Patent Infringement
Law Firm: Mintz Levin
Case Name: **Innovative Foundry Technologies** Inc. vs TSMC.
Services Provided: Technical consulting expert on semiconductor development and manufacturing case. Reviewed infringing patents, defendant's FinFET, contact and metallization manufacturing processes, and GDS layout files. Assisted in overseas depositions where the case was settled successfully following the depositions.
Date: 2018-9