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That I possess advanced knowledge of the Japanese and English languages. The attached Japanese into English translation has been translated by me and to the best of my knowledge and belief, it is a true and accurate translation of JP2006-339566 (Yanagida).

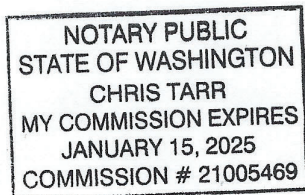
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I declare (or certify, verify, or state) under penalty of perjury that the foregoing is true and correct.

Executed on October 12, 2022 in Camas, Washington.

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Chris Tarr

Notary Public

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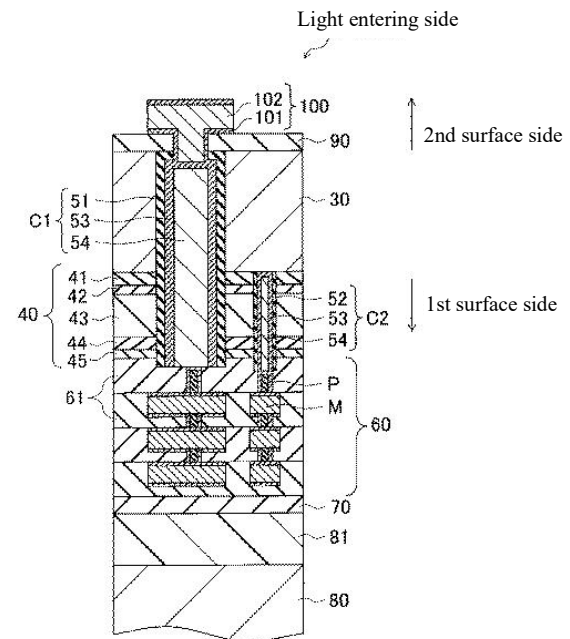
(54) [Name of Invention] Solid-state imaging device and its manufacturing method

(57) [Abstract]

[Problem to Be Solved] To provide a solid-state imaging device capable of forming a pad without causing a large level difference on a surface opposite to a wiring layer side of a substrate, and improving imaging characteristics and yield, and to provide its manufacturing method.

[Means for Solving the Problem] A solid-state imaging device having a wiring layer 60 on a 1st surface side of the substrate 30 for letting light enter from a 2nd surface side of the substrate 30 includes an interlayer insulation film 40 formed on the 1st surface side of the substrate 30 for covering a photoelectric conversion element and an active element, the wiring layer 60 formed on the interlayer insulation film 40, a support substrate 80 provided on the wiring layer 60, a 1st contact C1 formed penetrating through the interlayer insulation film 40 and the substrate 30 to connect with the wiring layer 60, and a pad 100 provided on the 2nd surface side of the substrate 30 to connect with the 1st contact C1.

[Selected representative figure] Fig. 4



[Scope of patent claims]

[Claim 1]

A method for manufacturing a solid-state imaging device having a wiring layer on the 1st surface side of a substrate and letting light enter thereon from the 2nd surface side of the aforesaid substrate, and this method for manufacturing a solid-state imaging device comprises the following steps:

- a step of forming a photoelectric conversion element and an active element on the aforesaid substrate;
- a step of forming an interlayer insulation film covering the aforesaid photoelectric conversion element and the aforesaid active element on the 1st surface side of the aforesaid substrate;
- a step of forming a 1st contact that penetrates through the aforesaid interlayer insulation film and reaches a depth halfway up the aforesaid substrate;
- a step of forming a wiring layer on the aforesaid interlayer insulation film;
- a step of affixing the support substrate on the aforesaid wiring layer;
- a step of making the aforesaid substrate thin by polishing the aforesaid substrate from the aforesaid 2nd surface side;
- a step of forming openings on the 2nd surface side of the aforesaid substrate to reach the aforesaid 1st contact;
- and a step of forming a pad on the 2nd surface side of the aforesaid substrate that is connected to the aforesaid 1st contact via the aforesaid opening.

[Claim 2]

The method for manufacturing a solid-state imaging device as described in Claim 1, further comprising a step of forming a color filter on the 2nd surface side of the aforesaid substrate after the step of forming the aforesaid pad.

[Claim 3]

The method for manufacturing a solid-state imaging device as described in Claim 1, further comprising a step of forming an on-chip lens on the 2nd surface side of the aforesaid substrate after the step of forming the aforesaid pad.

The method for manufacturing the solid-state imaging device according to Claim 1.

[Claim 4]

The method for manufacturing a solid-state imaging device as described in Claim 1, wherein the step of forming the aforesaid 1st contact comprises

- a step of forming a 1st through-hole that penetrates through the aforesaid interlayer insulation film and reaches a depth halfway up the aforesaid substrate;
- and a step of embedding the conductive layer in the aforesaid 1st through-hole.

[Claim 5]

The method for manufacturing a solid-state imaging device as described in Claim 1, further comprising a step of forming a 2nd contact in the aforesaid interlayer insulation film, after the step of forming the aforesaid interlayer insulation film and before the step of forming the aforesaid wiring layer.

[Claim 6]

The method for manufacturing a solid-state imaging device as described in Claim 5, wherein the step of forming the aforesaid 1st contact and aforesaid 2nd contact comprises

- a step of forming the 1st through-hole that penetrates through the aforesaid interlayer insulation film and reaches a depth halfway up the aforesaid substrate;
- a step of forming the 2nd through-hole that penetrates through the aforesaid interlayer insulation film;
- and a step of embedding the aforesaid conductive layer in the aforesaid 1st through-hole and the aforesaid 2nd through-hole, forming the 1st contact in the aforesaid 1st through-hole and forming the 2nd contact in the aforesaid 2nd through-hole.

[Claim 7]

A solid-state imaging device having a wiring layer on the 1st surface side of the substrate and letting light enter from the 2nd surface side of the aforesaid substrate, and this solid-state imaging device includes

- a photoelectric conversion element and an active element formed on the aforesaid substrate;
- an interlayer insulation film formed on the 1st surface side of the aforesaid substrate and covering the aforesaid photoelectric conversion element and the aforesaid active element;
- a wiring layer formed on the aforesaid interlayer insulation film;
- a support substrate provided on the aforesaid wiring layer;

a contact that is formed penetrating through the aforesaid interlayer insulation film and the aforesaid substrate and is connected with the aforesaid wiring layer;  
and a pad that is provided on the 2nd surface side of the aforesaid substrate and is connected to the aforesaid contact.

[Detailed description of the invention]

[Technical field]

[0001]

This invention is related to a solid-state imaging device and its manufacturing method, and is particularly related to a back-illuminated solid-state imaging device and its manufacturing method for letting light enter from a side opposite to the side on which the wiring layer is formed.

[Background technology]

[0002]

In CMOS image sensors, each pixel contains a photodiode and various transistors for readout, reset, amplification, etc. The signal photoelectrically converted by the photodiode is processed by the relevant transistor. On top of each pixel, a wiring layer containing multilayer metal wires is formed, and on top of the wiring layer, a color filter that defines the wavelength of light entering into the photodiode and an on-chip lens that focuses the light onto the photodiode are formed.

[0003]

However, in the CMOS image sensor described above, there was a problem that light is blocked by the wiring at the top of each pixel, resulting in reduced sensitivity of each pixel. In addition, when light reflected from these wires enters neighboring pixels, it causes color mixing and other problems.

[0004]

For this reason, a back-illuminated solid-state imaging device has been proposed in which the backside of a silicon substrate on which a photodiode or various types of transistors are formed is thinned by polishing, and light is entered from the backside of the substrate for photoelectric conversion (see, for example, Patent Documents 1 and 2). In this backside-illuminated solid-state imaging device, since the substrate needs to be polished at the wafer level, it is necessary to laminate a support substrate made of silicon substrate or the like to reinforce the strength of the substrate.

[Patent Document 1] Japanese Patent Publication No. 2003-31785

[Patent Document 2] Japanese Patent Publication No. 2003-273343

[Disclosure of the invention]

[Problem to be solved by the invention]

[0005]

In back-illuminated solid-state imaging devices, since the substrate is laminated to the wiring layer side of the substrate, the formation and placement of pads for input/output of signals to/from the outside are problematic. There are two methods of pad placement: pad placement on the support substrate side (surface side) of the substrate, and pad placement on the back side of the substrate. In both of the above-mentioned Patent Documents, the pad is placed on the support substrate side of the substrate.

[0006]

In the case of placing the pad on the back side of the substrate, the method below can be considered: after processing on the front side of the substrate is done, the back side of the substrate is polished to make it thinner, and then a through-hole is made to reach the wiring layer from the back side of the substrate. In this case, the wiring layer closest to the substrate is used as a pad and connected to the external device by wire bonding.

[0007]

However, since a through-hole is formed through the substrate to reach the wiring layer, a large level difference occurred on the back side of the substrate. If a large level difference occurs on the backside of the substrate, uneven film application will occur in the formation of color filters and on-chip lenses, and the desired optical characteristics cannot be obtained. If the desired optical characteristics cannot be obtained, the imaging characteristics will be degraded, and if the degradation of imaging characteristics is significant, the product will be defective.

[0008]

This invention was made in view of the above circumstances, and its purpose is to provide a method for manufacturing a solid-state imaging device in which a pad can be formed on the opposite side of the substrate from the wiring layer side

without causing a large level difference, thereby improving reliability and yield.

[0009]

Another purpose of this invention is to provide a solid-state imaging device with improved imaging characteristics and reliability by forming a pad on the opposite side of the substrate from the wiring layer without a large level difference.

[Means for solving the problem].

[0010]

In order to achieve the above-mentioned purpose, this invention provides a method for manufacturing a solid-state imaging device having a wiring layer on the 1st surface side of a substrate and letting light enter thereon from the 2nd surface side of the aforesaid substrate, and this method for manufacturing a solid-state imaging device comprises the following steps: a step of forming a photoelectric conversion element and an active element on the aforesaid substrate; a step of forming an interlayer insulation film covering the aforesaid photoelectric conversion element and the aforesaid active element on the 1st surface side of the aforesaid substrate; a step of forming a 1st contact that penetrates through the aforesaid interlayer insulation film and reaches a depth halfway up the aforesaid substrate; a step of forming a wiring layer on the aforesaid interlayer insulation film; a step of affixing the support substrate on the aforesaid wiring layer; a step of making the aforesaid substrate thin by polishing the aforesaid substrate from the aforesaid 2nd surface side; a step of forming openings on the 2nd surface side of the aforesaid substrate to reach the aforesaid 1st contact; and a step of forming a pad on the 2nd surface side of the aforesaid substrate that is connected to the aforesaid 1st contact via the aforesaid opening.

[0011]

In the above-mentioned manufacturing method of the solid-state imaging device of this invention, after forming the 1st contact that penetrates through the interlayer insulation film and reaches the depth halfway up the substrate, the step of forming the wiring layer and the step of laminating the support substrate are performed. Then, the substrate is polished from the 2nd surface side to make the substrate thinner. As a result, the tip of the 1st contact is positioned near the 2nd surface side of the substrate. After that, an opening is formed on the 2nd surface side of the substrate to reach the 1st contact, and a pad connected to the 1st contact is formed. In this way, there is no need to create a large through-hole to reach the wiring layer in the process on the 2nd surface side of the substrate, and thus, a large level difference will not occur on the 2nd surface side of the substrate.

[0012]

In order to achieve the above-mentioned purpose, this invention provides a solid-state imaging device having a wiring layer on the 1st surface side of the substrate and letting light enter from the 2nd surface side of the aforesaid substrate, and this solid-state imaging device includes a photoelectric conversion element and an active element formed on the aforesaid substrate; an interlayer insulation film formed on the 1st surface side of the aforesaid substrate and covering the aforesaid photoelectric conversion element and the aforesaid active element; a wiring layer formed on the aforesaid interlayer insulation film; a support substrate provided on the aforesaid wiring layer; a contact that is formed penetrating through the aforesaid interlayer insulation film and the aforesaid substrate and is connected with the aforesaid wiring layer; and a pad that is provided on the 2nd surface side of the aforesaid substrate and is connected to the aforesaid contact.

[0013]

In the solid-state imaging device of this invention, the pad formed on the 2nd surface side of the substrate is connected to the wiring layer through the interlayer insulation film and the contact penetrating the substrate. The signal that drives the active element is supplied through this pad. Since the pad is formed near the surface of the 2nd surface side of the substrate, there is no large level difference on the 2nd surface side of the substrate due to pad formation.

[Effect of the invention]

[0014]

According to the manufacturing method for solid-state imaging devices of this invention, a pad can be formed on the opposite side of the substrate from the wiring layer side without causing a large level difference, and this method can improve the reliability and yield of the solid-state imaging device.

According to the solid-state imaging device of this invention, the pad is formed on the opposite side of the substrate from the wiring layer without a large level difference, which enables the realization of a solid-state imaging device with improved imaging characteristics and reliability.

[Best form for implementing the invention]

[0015]

The following is a description of the embodiments of this invention with reference to the drawings.

(1st embodiment)

[0016]

Fig. 1 shows a schematic diagram of the solid-state imaging device pertaining to this embodiment.

[0017]

The solid-state imaging device has a pixel section 11 and peripheral circuits, which are mounted on the same semiconductor substrate. In this example, the peripheral circuits include a vertical selection circuit 12 and S/H (Sample/Hold) and CDS (Correlated Double Sampling) circuit 13, a horizontal selection circuit 14, a timing generator (TG) 15, an AGC (Automatic Gain Control) circuit 16, an A/D conversion circuit 17, and a digital amplifier 18.

[0018]

In the pixel section 11, a number of unit pixels, described below, are arranged in rows and columns, with address lines, etc. in rows and signal lines, etc. in columns.

[0019]

The vertical selection circuit 12 selects pixels in order by row and reads out the signal of each pixel in each pixel column through the vertical signal line to the S/H and CDS circuit 13. The S/H and CDS circuit 13 performs signal processing such as CDS, etc. on the pixel signals read from each pixel column.

[0020]

The horizontal selection circuit 14 takes out the pixel signals held in the S/H and CDS circuit 13 in sequence and outputs them to the AGC circuit 16. The AGC circuit 16 amplifies the signal input from the horizontal selection circuit 14 with an appropriate gain and outputs it to the A/D conversion circuit 17.

[0021]

The A/D conversion circuit 17 converts the analog signal input from the AGC circuit 16 into a digital signal and outputs it to the digital amplifier 18. The digital amplifier 18 amplifies the digital signal input from the A/D conversion circuit 17 appropriately and outputs it from the pad (terminal) described below.

[0022]

The operations of the vertical selection circuit 12, S/H and CDS circuit 13, horizontal selection circuit 14, AGC circuit 16, A/D conversion circuit 17, and digital amplifier 18 are based on various timing signals output from the timing generator 15.

[0023]

Fig. 2 shows an example of the circuit configuration of the unit pixel in the pixel section 11.

[0024]

The unit pixel has, for example, a photodiode 21 as a photoelectric conversion element, and for this one photodiode 21, there are four transistors: transfer transistor 22, amplifying transistor 23, address transistor 24, and reset transistor 25 as active elements.

[0025]

The photodiode 21 photoelectrically converts the incident light into an amount of charge (in this case, electrons) corresponding to the light intensity. The transfer transistor 22 is connected between the photodiode 21 and the floating diffusion FD, and when a drive signal is given to its gate through the drive wiring 26, the electrons photoelectrically converted by the photodiode 21 are transferred to the floating diffusion FD.

[0026]

The floating diffusion FD is connected to the gate of an amplifying transistor 23. The amplifying transistor 23 is connected to the vertical signal line 27 via the address transistor 24 and constitutes a constant current source I and a source follower outside the pixel section. Then, when the address signal is given to the gate of the address transistor 24 through the drive wiring 28, and the said address transistor 24 turns on, the amplifying transistor 23 amplifies the potential of the floating diffusion FD and outputs the voltage corresponding to that potential to the vertical signal line 27. The voltage output from each pixel is output to the S/H and CDS circuit 13 through the vertical signal line 27.

[0027]

The reset transistor 25 is connected between the power supply Vdd and the floating diffusion FD. When a reset signal

is given to the gate, the potential of the floating diffusion FD is reset to the potential of the power supply Vdd. These operations are performed simultaneously for each pixel in a row, since the gates of the transfer transistor 22, address transistor 24, and reset transistor 25 are connected on a row basis.

[0028]

Fig. 3 shows a schematic cross-sectional view of the pixel section of the solid-state imaging device.

[0029]

The silicon layer 30 consists of, for example, a p-type silicon substrate, and corresponds to the substrate of this invention. Multiple photodiodes 21, which constitute a unit pixel, are formed in the silicon layer 30. The photodiodes 21 are composed of pn junctions formed by introducing n-type impurities into the silicon layer 30. The silicon layer 30 is thinned so that light can enter from the backside. The thickness of the silicon layer 30 depends on the type of solid-state imaging device, but is 4 to 6  $\mu\text{m}$  for visible light and 6 to 10  $\mu\text{m}$  for near-infrared light.

[0030]

The silicon layer 30 has n-type semiconductor regions 34 that serve as source or drain regions for the transistors 22-25 shown in Fig. 2 or as floating diffusion FDs, and p-type channel stop section 35 that prevents signal charge from flowing in and out between pixels.

[0031]

On the 1st side (surface) of the silicon layer 30, gate electrodes 37 of the transistors 22-25 shown in Fig. 2 are formed via a gate insulating film 36 made of, for example, silicon oxide, etc.

[0032]

On the 1st side of the silicon layer 30, covering the above-mentioned transistors, an interlayer insulation film 40 is formed. On top of the interlayer insulation film 40, a wiring layer 60 containing multiple layers of metal wiring is formed. On top of the wiring layer 60, a protective film 70 is formed.

[0033]

On the protective film 70, a support substrate 80 is provided via an adhesive layer 81. The support substrate 80 is provided to reinforce the strength of the silicon layer 30. The support substrate 80 comprises, for example, a silicon substrate.

[0034]

On the 2nd surface side (back side, light-entering side) of the silicon layer 30, an anti-reflection film 90 is formed, and on the anti-reflection film 90, a light shielding film 100a is formed to open each photodiode 21. On the anti-reflection film 90, a protective film 110 is formed to cover the light shielding film 100a. The protective film 110 is made of, for example, TEOS film with a film thickness of 150 nm. In addition, the TEOS film is a silicon oxide film deposited from TEOS as a raw material.

[0035]

On the protective film 110, a color filter 111 is formed to pass only light in a desired wavelength region. In addition, on the color filter 111, an on-chip lens 112 is formed to focus the incident light onto the photodiode 21.

[0036]

The solid-state imaging device shown in Fig. 1 is surrounded by pads for signal input/output to/from the outside. Fig. 4 shows a detailed cross-sectional view of the solid-state imaging device at the periphery where the pads are placed. In Fig. 4, it is illustrated by reversing up and down with respect to Fig. 3.

[0037]

As shown in Fig. 4, an interlayer insulation film 40 is formed on the 1st side of the silicon layer 30. The interlayer insulation film 40, for example, consists of a laminated structure with a TEOS film 41, a silicon nitride film 42, a TEOS film 43, a PSG film 44, and a TEOS film 45. PSG film 44 is a silicon oxide film containing phosphorus (P). The thickness of TEOS film 41 is 10 nm, the thickness of silicon nitride film 42 is 50 nm, the thickness of TEOS film 43 is 400 nm, the thickness of PSG film 44 is 100 nm, and the thickness of TEOS film 45 is 100 nm. However, the thickness of each film

is an example and is not limited.

[0038]

1st contact C1 is formed penetrating through silicon layer 30 and interlayer insulation film 40. 1st contact C1 electrically connects pad 100, which is described later, to pixel section 11 and peripheral circuits. A sidewall insulation film 51 is formed around the 1st contact C1 to electrically insulate the silicon layer 30 and the 1st contact C1. 1st contact C1 comprises a barrier metal 53 and a conductive layer 54.

[0039]

Within the interlayer insulation film 40, a 2nd contact C2 is further formed. The 2nd contact C2 is connected to the gate electrode 37 of the transistor formed in the silicon layer 30 and the semiconductor region 34. The 2nd contact C2 connects the transistors in the pixel section 11 and peripheral circuits. A sidewall protective film 52 is formed around the 2nd contact C2 to protect the interlayer insulation film 40. The 2nd contact C2 consists of a barrier metal 53 and a conductive layer 54.

[0040]

A wiring layer 60 is formed on the interlayer insulation film 40. The wiring layer 60 has plug P and wiring M formed in interlayer insulation film 61. Each interlayer insulation film 61 is made of TEOS film with a thickness of, for example, 600 nm. Fig. 4 shows an example of 3-layer wiring. The wiring M is connected to 1st contact C1 and 2nd contact C2 via plug P.

[0041]

A protective film 70 is formed on the wiring layer 60. The protective film 70 comprises a silicon nitride film with a thickness of, for example, 500 nm.

[0042]

On the protective film 70, a support substrate 80 is provided via an adhesive layer 81. The adhesive layer 81 is, for example, a thermosetting organic adhesive layer, and its film thickness is about several  $\mu\text{m}$ . The support substrate 80 is made of silicon substrate. However, a TEOS film, for example, can also be used as the adhesive layer 81.

[0043]

On the 2nd surface side of the silicon layer 30, an anti-reflection film 90 is formed. The anti-reflection film 90 comprises two layers, for example, a TEOS film and a silicon nitride film. The thickness of the TEOS film is 15 nm and the thickness of the silicon nitride film is 60 nm.

[0044]

On the anti-reflection film 90, a pad 100 that connects to the 1st contact C1 is formed. Pad 100 is formed by barrier metal 101 and conductive layer 102. The pad 100 is formed at the same time as the light shielding film 100a in the pixel section 11.

[0045]

In addition, although it is not shown in the figure, a protective film 110 is formed on the anti-reflection film 90.

[0046]

Next, the manufacturing method of the solid-state imaging device according to the above embodiment will be described with reference to Fig. 5 to Fig. 10. Fig. 5 to Fig. 10 correspond to the cross-sectional view of the step of the pad placement region shown in Fig. 4.

[0047]

As shown in Fig. 5(a), SOI substrate 300 is used in this embodiment. The SOI substrate 300 is a silicon layer 30 formed on a silicon substrate 32 via a silicon oxide film 31. Various types of transistors and photodiodes that constitute pixel section 11 and peripheral circuits are formed on silicon layer 30 of SOI substrate 300. After that, the interlayer insulation film 40 is formed on the 1st surface side of the silicon layer 30 to cover the transistors and photodiodes. In the formation of interlayer insulation film 40, TEOS film 41, silicon nitride film 42, TEOS film 43, PSG film 44, and TEOS film 45 are formed in sequence. In the formation of TEOS film, for example, the LPCVD method is used. Thereafter, the resist pattern R1 for forming 1st contact C1 is formed on interlayer insulation film 40 by lithography technique.

[0048]

Next, as shown in Fig. 5(b), the interlayer insulation film 40 is dry etched using the resist pattern R1 as a mask. As a result, the 1st through-hole CH1 is formed through the interlayer insulation film 40. Thereafter, the resist pattern R1 is removed.

[0049]

Next, as shown in Fig. 6(a), the silicon layer 30 is dry etched using the interlayer insulation film 40 as a hard mask. This results in the 1st through-hole CH1 that penetrates through the interlayer insulation film 40 and silicon layer 30. The silicon oxide film 31 is used as an etch stopper. Wet etching is then applied to remove etch residue in the 1st through-hole CH1.

[0050]

10 Next, as shown in Fig. 6(b), the sidewall insulation film 51 is formed on the interlayer insulation film 40 to cover the inner wall of the 1st through-hole CH1. Silicon nitride film is formed as the sidewall insulation film 51 by the LPCVD method. The sidewall insulation film 51 is provided to insulate the silicon layer 30 from the 1st contact C1, which is to be formed later.

[0051]

Next, as shown in Fig. 7(a), barrier metal 53 is formed on the sidewall insulation film 51 to cover the inner wall of the 1st through-hole CH1, and a conductive layer 54 is formed on top of the barrier metal 53 to embed the 1st through-hole CH1. As the barrier metal 53, a titanium nitride (TiN) film is formed by sputtering or CVD method. As the conductive layer 54, a tungsten film is formed by CVD method.

[0052]

20 Next, as shown in Fig. 7(b), excess conductive layer 54, barrier metal 53, and sidewall insulation film 51 deposited on areas other than 1st through-hole CH1, i.e., interlayer insulation film 40, are removed by etch-back. In addition to etch-back, a CMP method may also be used. As a result, 1st contact C1, consisting of barrier metal 53 and conductive layer 54 embedded via the sidewall insulation film 51 in 1st through-hole CH1, is formed.

[0053]

Next, as shown in Fig. 8(a), the interlayer insulation film 40 is etched using a resist pattern that is not shown in the figure to form the 2nd through-hole CH2 at the position where the 2nd contact C2 is formed. After that, the resist pattern is removed.

[0054]

30 Next, as shown in Fig. 8(b), the 2nd contact C2 is formed in the 2nd through-hole CH2 via sidewall protective film 52. In this step, after forming the sidewall protective film 52 made of TEOS film on the sidewall of the 2nd through-hole CH2, wet etching is performed to remove etch residues in the 2nd through-hole CH2. The sidewall protective film 52 is provided to prevent the PSG film 44 from being removed during this wet etching. After that, the conductive layer 54 is embedded via barrier metal 53 in the 2nd through-hole CH2 to etch back unwanted barrier metal 53 and conductive layer 54 deposited on the interlayer insulation film 40. This forms the 2nd contact C2 consisting of barrier metal 53 and conductive layer 54 embedded via the sidewall protective film 52 in the 2nd through-hole CH2.

[0055]

40 Next, as shown in Fig. 9(a), the wiring layer 60 is formed on the interlayer insulation film 40. In the formation of the wiring layer 60, the following steps are repeated: a step of forming the interlayer insulation film 61, a step of forming the through-hole in the interlayer insulation film 61, a step of forming the plug P in the through-hole, and a step of forming the wiring M on the interlayer insulation film 61. In this example, an example of 3-layer wiring is shown. The plug P is composed of a conductive layer 63 and a barrier metal 62 that covers the periphery of the conductive layer 63. TiN is used as the barrier metal 62 and tungsten is used as the conductive layer 63. The wiring M is composed of a conductive layer 65 and a barrier metal 64 that covers the top and bottom of the conductive layer 65. TiN is used as the barrier metal

64, and AlCu or Cu is used as the conductive layer 65. Each wiring M is connected to the 1st contact C1 and 2nd contact C2 via plug P.

[0056]

Next, the protective film 70 is formed on the wiring layer 60. As the protective film 70, silicon nitride film is formed by the plasma CVD method. Then, the support substrate 80 is laminated to the 1st surface side of SOI substrate 300 via the adhesive layer 81. As a result, the support substrate 80 is provided on the protective film 70 via the adhesive layer 81. In addition, it is also possible to form a TEOS film on the protective film 70 of the SOI substrate 300 and a TEOS film on the support substrate 80 side, so that the TEOS films face each other and the SOI substrate 300 and support substrate 80 can also be laminated together.

[0057]

Next, as shown in Fig. 9(b), after thinning the silicon substrate 32 of SOI substrate 300 by grinding, the remaining silicon substrate 32 is removed by wet etching. The silicon oxide film 31 is used as an etch stopper. In addition, from Fig. 9(b) onward, the figure is illustrated by reversing up and down with respect to Fig. 9(a).

[0058]

Next, as shown in Fig. 10(a), after removing the silicon oxide film 31 using, for example, hydrofluoric acid, an anti-reflection film 90 is formed on the silicon layer 30. In the formation of an anti-reflection film 90, TEOS film and silicon nitride film are formed by the plasma CVD method.

[0059]

Next, as shown in Fig. 10(b), the resist pattern R2 is formed on the anti-reflection film 90 by a lithography technique, and the anti-reflection film 90 and sidewall insulation film 51 are etched using resist pattern R2 as a mask. As a result, the opening CH3 that reaches 2nd contact C2 is formed. After that, the resist film is removed.

[0060]

Next, the barrier metal 101, conductive layer 102, and barrier metal 101 are deposited in sequence to embed the opening CH3, and the barrier metal 101 deposited on the anti-reflection film 90, the conductive layer 102, and the barrier metal 101 are then patterned to form pad 100 (see Fig. 4). In this step of forming the pad 100, the light shielding film 100a of the pixel section 11 is also formed at the same time.

[0061]

Next, on the anti-reflection film 90, a protective film 110 is formed to cover the pad 100 and the light shielding film 100a (see Fig. 3). In formation of the protective film 110, a TEOS film with a thickness of 150 nm is formed by the plasma CVD method. Then, the color filter 111 is formed in the pixel section 11 by coating the entire surface with color filter material and patterning. Furthermore, a lens material is applied to the entire surface and patterned to form an on-chip lens 112 in the pixel section 11. In addition, the color filter material and on-chip lens material are applied to the pixel section 11 and the peripheral area where the pad 100 is placed, but after patterning, color filter 111 and on-chip lens 112 are formed only on the pixel section 11.

[0062]

As a result, the solid-state imaging device pertaining to this embodiment is manufactured.

[0063]

Next, the effect of this embodiment of solid-state imaging device and its manufacturing method pertaining to this embodiment will be explained with reference to a comparative example.

[0064]

Fig. 11 shows a cross-sectional view of the pad placement region of the solid-state imaging device pertaining to the comparative example. In addition, the same components as in Fig. 4 are marked with the same reference numerals, so their descriptions are omitted.

[0065]

For example, after the 1st surface side process of the silicon layer 30 (formation of the interlayer insulation film 40, wiring layer 60, protective film 70, adhesive layer 81, support substrate 80), when forming the 1st through-hole CH1 in the process on the 2nd surface side of the silicon layer 30, the 1st layer wiring M (wiring closest to the silicon layer 30 side) in the wiring layer 60 is used as a pad.

[0066]

In this case, a large level difference occurs on the 2nd surface side of the silicon layer 30 due to the 1st through-hole CH1, which penetrates silicon layer 30 and interlayer insulation film 40 to a depth of about 6  $\mu\text{m}$ . In this case, a large level difference occurs on the 2nd surface side of the silicon layer 30 due to the 1st through-hole CH1, which penetrates silicon layer 30 and interlayer insulation film 40 to a depth of about 6  $\mu\text{m}$ . When the color filter and on-chip lens are formed in this condition, uneven application of color filter material and lens material occurs on the surface, and the desired optical characteristics cannot be obtained.

[0067]

10 In contrast, in the solid-state imaging device pertaining to this embodiment, in the process of the 1st surface side of the silicon layer 30, before forming the wiring layer 60, the 1st contact C1 that penetrates through the interlayer insulation film 40 and the silicon layer 30 is formed (see Fig. 7(b)). Then, in the process of the 2nd surface side of the silicon layer 30, the opening CH3 that reaches the 1st contact C1 is formed (see Fig. 10(b)), and since the pad 100 is formed to embed the said opening CH3, the level difference on the 2nd surface side of the silicon layer 30 is only the thickness of the pad 100.

[0068]

As a result, uneven application of the color filter material and lens material will not occur within the surface, so the color filter 111 and on-chip lens 112 with the desired optical characteristics can be formed. As a result, the imaging characteristics and yield of the solid-state imaging device can be improved. In addition, in this embodiment, an example of a solid-state imaging device equipped with both color filter 111 and on-chip lens 112 was described, but a solid-state imaging device with only color filter 111 or on-chip lens 112 may also be used.

20 [0069]

In addition, since the pad 100 can be provided on the 2nd surface side of the silicon layer 30, the light shielding film 100a provided on the 2nd surface side of the silicon layer 30 can be connected to the pad 100, and the light shielding film 100a can be fixed at a constant potential. For this reason, it is possible to avoid the effects of light shielding film charging on electron accumulation, readout, etc., and it is possible to improve the imaging characteristics.

[0070]

(2nd embodiment)

Below, the manufacturing method of the solid-state imaging device according to the 2nd embodiment will be described with reference to Fig. 12.

[0071]

30 First, in the same manner as the 1st embodiment, the steps shown in Fig. 5 to Fig. 6 are performed. As a result, the 1st through-hole CH1 which penetrates through the interlayer insulation film 40 and silicon layer 30, and the sidewall insulation film 51 which covers the inside of the 1st through-hole C1 are formed.

[0072]

Next, as shown in Fig. 12(a), the interlayer insulation film 40 is etched using a resist pattern that is not shown in the figure to form the 2nd through-hole CH2 at the position where the 2nd contact C2 is formed. After that, the resist pattern is removed.

[0073]

40 Next, as shown in Fig. 12(b), after forming the sidewall protective film 52 on the sidewall of the 2nd through-hole CH2, wet etching is performed to remove the etching residue in the 2nd through-hole CH2. Then, a conductive layer 54 is embedded in the 1st through-hole CH1 and the 2nd through-hole CH2 via the barrier metal 53. As the barrier metal 53, a titanium nitride (TiN) film is formed by sputtering or the CVD method. As the conductive layer 54, a tungsten film is formed by the CVD method.

[0074]

Next, as shown in Fig. 12(c), excess conductive layer 54, barrier metal 53, and sidewall insulation film 51 deposited on interlayer insulation film 40 are removed by etching back. In addition to etch-back, a CMP method may also be used. As a result, the 1st contact C1 is formed, consisting of barrier metal 53 and conductive layer 54 embedded via the sidewall insulation film 51 in the 1st through-hole CH1. In addition, the 2nd contact C2 is formed in the 2nd through-hole CH2, consisting of a barrier metal 53 and a conductive layer 54 embedded via a sidewall protective film 52.

[0075]

Thereafter, the same as in the 1st embodiment, the solid-state imaging device is completed through the steps from Fig. 9(a) onward.

[0076]

In this embodiment, the 1st contact C1 and the 2nd contact C2 are formed simultaneously by embedding the barrier metal 53 and the conductive layer 54 in the 1st through-hole CH1 and the 2nd through-hole CH2 simultaneously. For this reason, compared to the 1st embodiment, the manufacturing steps can be reduced.

[0077]

In addition, the same as in the 1st embodiment, the pad 100 can be formed on the 2nd surface side of the silicon layer 30 without a large level difference. For this reason, the same effect as in the 1st embodiment can be achieved.

[0078]

This invention is not limited to the description of the above embodiments.

For example, the numerical values and materials mentioned in this embodiment are examples and are not limited thereto. For example, the example of using SOI substrate 300 is described in this embodiment, but an ordinary silicon substrate may also be used. For example, in the 1st embodiment, the 1st contact C1 may also be formed after the 2nd contact C2 is formed. In addition, in the 2nd embodiment, it is also fine to form the 1st through-hole CH1 after forming the 2nd through-hole CH2, and after that, simultaneously form the 1st contact C1 and the 2nd contact C2 in the 1st through-hole CH1 and the 2nd through-hole CH2.

Various other changes are possible to the extent that they do not depart from the main idea of this invention.

[Brief description of the figures]

[0079]

[Fig. 1] A schematic diagram of the solid-state imaging device pertaining to this embodiment.

[Fig. 2] A diagram showing an example of the circuit configuration of a unit pixel of the pixel section.

[Fig. 3] A schematic cross-sectional view of the pixel section of the solid-state imaging device.

[Fig. 4] A cross-sectional view of the peripheral part of the solid-state imaging device.

[Fig. 5] A cross-sectional view of the manufacturing process of the solid-state imaging device according to the 1st embodiment.

[Fig. 6] A cross-sectional view of the manufacturing process of the solid-state imaging device according to the 1st embodiment.

[Fig. 7] A cross-sectional view of the manufacturing process of the solid-state imaging device according to the 1st embodiment.

[Fig. 8] A cross-sectional view of the manufacturing process of the solid-state imaging device according to the 1st embodiment.

[Fig. 9] A cross-sectional view of the manufacturing process of the solid-state imaging device according to the 1st embodiment.

[Fig. 10] A cross-sectional view of the manufacturing process of the solid-state imaging device according to the 1st embodiment.

[Fig. 11] A cross-sectional view of the peripheral part of a comparative example of the solid-state imaging device.

[Fig. 12] A cross-sectional view of the manufacturing process of the solid-state imaging device according to the 2nd embodiment.

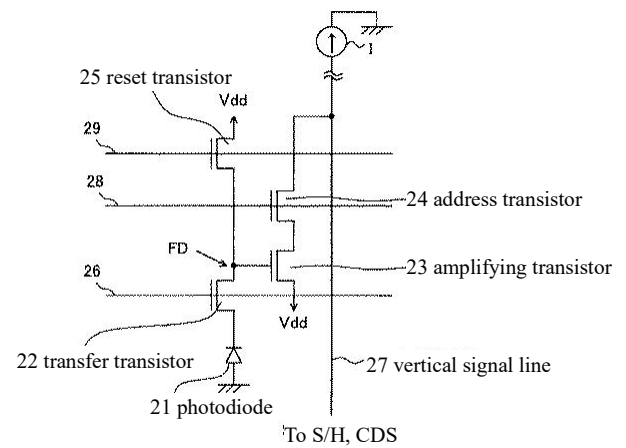
[Description of the reference numerals]

[0080]

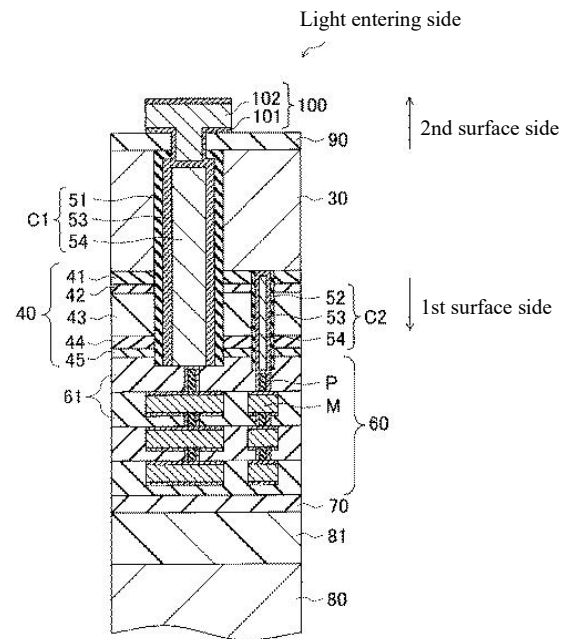
11 ... pixel section; 12 ... vertical selection circuit; 13 ... S/H, CDS circuit; 14 ... horizontal selection circuit; 15 ... timing generator; 16 ... AGC circuit; 17 ... A/D conversion circuit; 18 ... digital amplifier; 21 ... photodiode; 22 ... transfer transistor; 23 ... amplifying transistor; 24 ... address transistor; 25 ... reset transistor; 26; 28; 29 ... drive wiring; 27 ... vertical signal line; 30 ... silicon layer; 31 ... silicon oxide film; 32 ... silicon substrate; 34 ... semiconductor region; 35 ... channel stop section; 36 ... gate insulating film; 37 ... gate electrode; 40 ... interlayer insulation film; 41 ... TEOS film; 42 ... silicon nitride film; 43 ... TEOS film; 44 ... PSG film; 45 ... TEOS film; 51 ... sidewall insulation film; 52 ... sidewall protective film; 53 ... barrier metal; 54 ... conductive layer; 60 ... wiring layer; 61 ... interlayer insulation film; 62 ... barrier metal; 63 ... conductive layer; 64 ... barrier metal; 65 ... conductive layer; 70 ... protective film; 80 ... support substrate; 81 ... adhesive layer; 90 ... antireflection film; 100 ... pad; 100a ... light shielding film; 101 ... barrier metal;

102 ... conductive layer; 110 ... protective film; 111 ... color filter; 112 ... on-chip lens; 300 ... SOI substrate; C1 ... 1st contact; C2 ... 2nd contact; CH1 ... 1st through-hole; CH2 ... 2nd through-hole; P Plug; M ... wiring; R1; R2 ... resist pattern

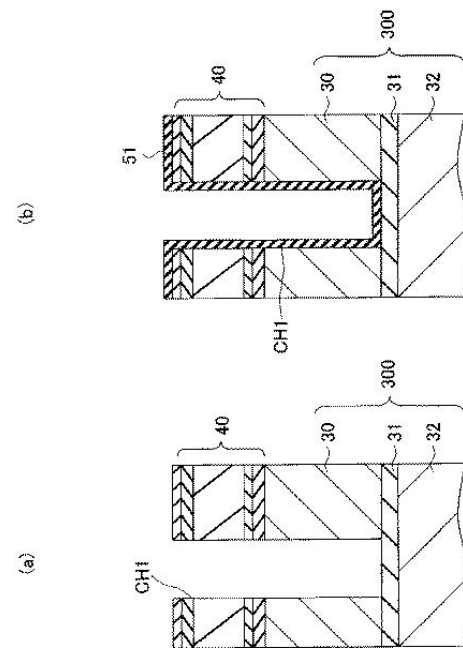
[Fig 2]



[Fig 4]



[Fig 6]





[Fig 12]

