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An Overview of Buried Oxides on Silicon: New Processes and Radiation Effects

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interfaces and thin films

Abstract. — This paper presents a review of the main properties of the two types of buried oxides that currently dominate the Silicon-On-Insulator (SOI) technologies: SIMOX (Separation by IMplantation of OXYgen) and BESOI (Bond and Etch-Back SOI) materials. After examining the main advantages of SOI structures for radiation-hardened electronics, we present different advanced technological processes of such buried oxides and review their physical characteristics as well as their charge trapping properties under ionizing radiations.

Résumé. — Cet article présente une revue des principales propriétés des deux types d'oxyde enterrés qui dominent actuellement les technologies Silicium-sur-Isolant (Silicon-On-Insulator, SOI) de la microélectronique : le matériau SIMOX (Separation by IMplantation of OXYgen) et le matériau BESOI (Bond and Etch-Back SOI). Après avoir rappelé les principaux avantages d'une architecture Silicium-sur-Isolant pour une électronique dédiée aux environnements radiatifs, nous présentons les différents procédés de fabrication actuels de ces couches d'oxyde enterrées et passons en revue leurs caractéristiques physiques ainsi que leurs propriétés de piégeage de charge sous rayonnement ionisant.

1. Introduction

Demonstrated for the first time in the early 1960's, the concept of Silicon-On-Insulator (SOI) material [1] has mostly progressed during the last decade and will continue to progress in the frame of new specific application area, such as low power, high frequency, high temperature or very radiation-hardened electronics [2, 3].

The main interest of Buried Oxides (BOX) [4] essentially comes from their ability to electrically isolate elementary devices (integrated on a same substrate) from one another. This isolation provides several benefits in terms of cross-coupling by parasitic capacitance [5], leakage currents [6] and radiation-induced problems [7], as we shall see next. Another interest of

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Table I. — *Some significant dates of the main SOI technologies.*

Date	Main Achievements	Comments
30's	The Metal-Insulator-Semiconductor (MIS) transistor historical patent.	Semiconductor processing not mature, searching for purity.
40's-50's	First bipolar devices.	Oxide processing not mature, electrically unstable and contaminated.
60's	Monocrystalline Silicon-On-Sapphire (SOS) and related materials (MgAl_2O_4 , CaF_2 , SrF_2 , BaF_2).	Heteroepitaxy. Thin Film Transistor. Demonstration of the Silicon-On-Insulator (SOI) Concept
70's	Zone Melting Recrystallization (ZMR) by laser and electron beams. Epitaxial Lateral Overgrowth (ELO).	Limited recrystallization. Limited seed growth.
80's	Separation by IMplantation of OXYgen (SIMOX). Full-Isolation by Porous Oxidized Silicon (FIPOS).	Additive synthesis of SiO_2 Selective oxidation
85's	Bond and Etch-Back SOI (BESOI)	Adaptation of pressure and bonding by hydrophilisation.
90's	Ultra-thin (low dose) SIMOX.	Silicon thickness of 50 nm with small roughness on 80 nm buried oxide.
95's	3D structures with bonded wafers. Vertical bonding interconnects	

these insulator films buried between two layers of semiconductors is the possibility they offer to etch selectively one of the two material layers. This advantages can be of great interest for micromachine [8], sensor technology and integrated optics [9–13].

A very significant effort has been made to develop SOI materials. The goal of all these methods is to obtain a film of semiconductor on top of an insulator with the highest possible thickness uniformity and the lowest possible defect density. Table I summarizes the main methods that have successively emerged in the past decades and for which a large number of technological solutions have been considered [1,3,14]. Historically, some simple ideas have been introduced: the deposition and recrystallization of silicon on an insulator (ZMR, Zone-Melting Recrystallization [15–17]), the epitaxial growth of silicon on a silicon substrate partially covered with an insulator (homoepitaxial techniques, such as ELO, Epitaxial Lateral Overgrowth [18, 19]), the epitaxial growth of silicon on a crystalline insulator (heteroepitaxial techniques, such as SOS, Silicon-On-Sapphire [20–23]) and also the oxidation of porous silicon (FIPOS, Full-Isolation by Porous Oxidized Silicon [24,25]). Beside these methods, new concepts have been introduced to directly obtain an insulating layer underneath the silicon surface by implantation of oxygen ions in a silicon wafer (SIMOX, Separation by IMplanted Oxygen [26–31]) or by direct

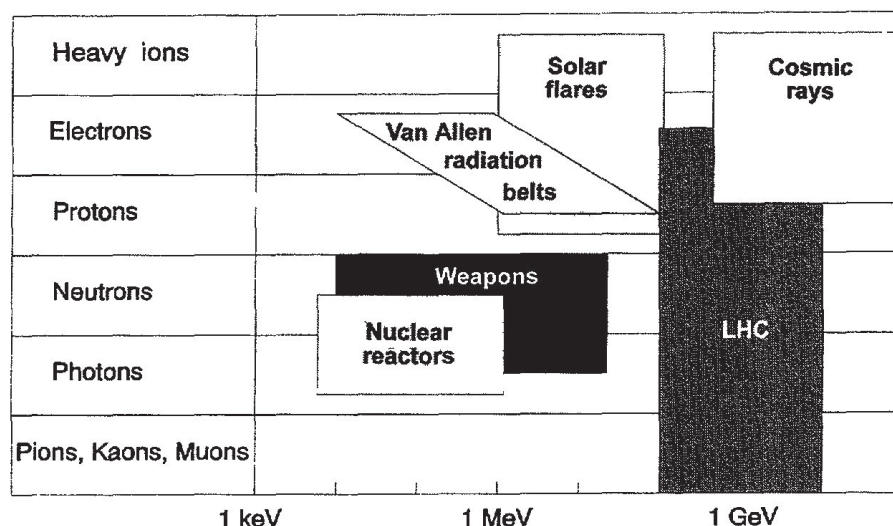


Fig. 1. — Some typical radiation environments as a function of the energy of particles. The acronym LHC stands for Large Hadron Collider (high energy physics domain).

bonding of two oxidized silicon wafers, with subsequent thinning of the upper wafer to obtain a thin silicon film on a buried oxide (BESOI, Bond and Etchback SOI [32–40]).

All these techniques have been widely explored, but the requirements for large scale integrated microelectronics during the two last decades (in terms of film thickness uniformity, oxide quality, *etc.*) have lead to the emergence of three main technologies (SOS, SIMOX and BESOI). Since the end of the 1980's, one can consider that only SIMOX and BESOI BOX families have really dominated the SOI market, essentially because their fabrication processes are based on standard silicon wafers and silicon-compatible equipment [41].

In this paper, we present a review of the main properties of these last two BOX families in the specific frame of radiation-hardened electronics. The advantages of SOI design for electronics working in radiation environments, its benefits and its limits, are briefly exposed in Section 2. Section 3 is devoted to a description of SIMOX and BESOI materials and their elaboration processes. Finally, in Section 4, we investigate their charge trapping which determine the electrical response of such materials under ionizing irradiation.

2. Advantages of SOI Design in Radiation Environments

2.1. BACKGROUND. — Radiation hardness is a key parameter for electronics devoted to work in hostile environments, such as the one encountered in space or nuclear contexts. A rapid survey of the potential sources of radiation shows that a large energy spectra has to be considered for long-term reliability study of electronics (Fig. 1).

The space radiation environment mainly consists of isolated cosmic rays (ions or protons), and of electrons trapped in the Van Allen Belts [42]. Shielding of high energy particles is almost inefficient or impractical. It results that energetic particle flux (muons, neutrons, pions) induced by the decay of cosmic rays go through any material.

Specific ground-level radiations are basically the product of fusion or fission nuclear reactions (nuclear weapons and reactors), and consist of gamma-rays, X-rays and neutrons. Another source of instability eventually comes from the natural radioactive background. For packaged electronics, a supplemental source of ionizing particles can originate from the alpha emission

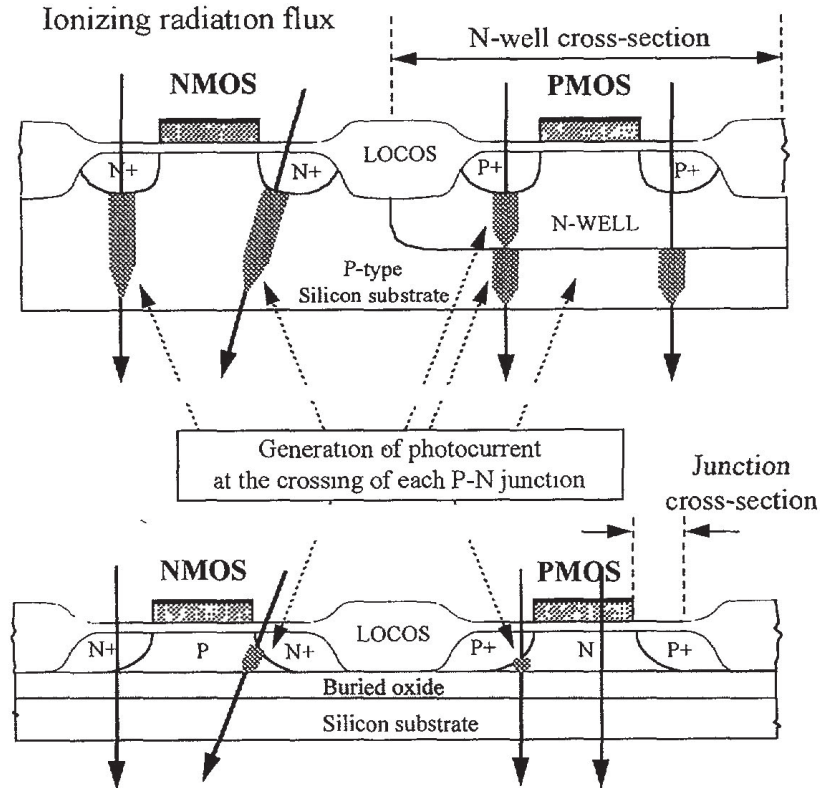


Fig. 2. — SOI design assets for transient radiation-induced phenomena: a drastic reduction of ionizing tracks (i.e. charge collection length) and cross-sections against the ionizing particle flux.

generated by the fission of radioactive species of the chip carrier (especially the ceramics) or from the chip itself (especially the metal layers).

2.2. IONIZING EFFECTS. — Along their tracks, all the ionizing particles generate electron-hole pairs in the silicon and silicon dioxide active layers. For the muons commonly encountered at ground level (about one particle per cm^2 per hour), 1 to 10 fC are generated per micron. In space, protons or heavy ion cosmic rays can generate much more, from $10 \text{ fC } \mu\text{m}^{-1}$ to $1 \text{ pC } \mu\text{m}^{-1}$. As detailed below, this ionization phenomenon leads to the buildup of a trapped charge in insulators and of interface traps at the semiconductor-insulator interface (permanent effects) as well as the production of photocurrents in semiconductor junctions (transient effects).

2.2.1. Transient Effects. — The carriers generated by ionization are swept away by the electric fields due to applied voltages or doping gradients, and diffuse towards P-N junctions (Fig. 2). As a result, the collected photocurrents (from microamps to milliamps) can cause single-event upsets (SEU or “soft errors”) in circuit nodes; these currents are proportional to the junction areas.

These values of generated charge have to be compared to the order of magnitude of the charge N_e stored under a typical transistor gate issued from an advanced CMOS technology (area $W \times L = 0.1 \mu\text{m}^2$, oxide thickness $T_{\text{ox}} = 5 \text{ nm}$, applied drain voltage $V_D = 1.5 \text{ V}$, threshold voltage $V_T = 0.5 \text{ V}$): $N_e = C_{\text{ox}} \times W \times L \times (V_D - V_T) = 0.067 \text{ fC} \approx 420 \text{ electrons}$. Such a rough evaluation shows that N_e can be upset by the natural particle flux (1 fC represents

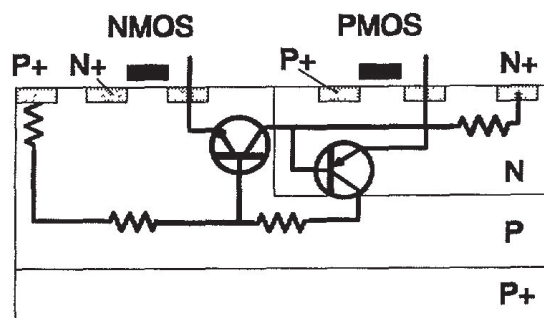


Fig. 3. — Parasitic Silicon-Controlled-Rectifier (thyristor) structure inherent to CMOS bulk design and responsible of the latchup of circuits (from Flament *et al.* [44]).

~ 6240 electrons), unless the collection length in the silicon is reduced, as illustrated in Figure 2 for SOI structures. In this case, the presence of the buried oxide layer between the active silicon film and the substrate drastically reduces the charge collection zone to the thickness of the silicon film (in the worst case) which is typically in the range 100 – 300 nm.

Another advantage of SOI over bulk design is the complete elimination of the latchup in CMOS technologies [43]. This problem generally occurs in bulk CMOS where the complementary MOS structure exhibits a parasitic NPNP Silicon-Controlled-Rectifier (thyristor) structure (Fig. 3) [44]. When a photocurrent is injected in this structure, a positive feed back loop is triggered and the device is then latched. The device may be destroyed by thermal dissipation if the supply voltage is not rapidly shut down. In SOI technology, the complete isolation of each elementary transistor suppresses the parasitic structure and prevents the appearance of such functionality failure [43].

The specific radiation-hardness of SOI structures has thus been extensively exploited during the three last decades and leads to major improvements of electronics in terms of: i) assurance against circuit latchup, ii) reduction of the leakage photocurrents by two or three orders of magnitude, and iii) reduction of the interaction cross sections of transistors (against a given particle flux) by one or two orders of magnitude.

2.2.2. Permanent Effects in Dielectrics. — The irradiation of an insulating layer generates electron-hole pairs in the material. If no electric field is applied, these pairs recombine and no current flows. If an electric field is applied, most pairs are separated and the carriers can be collected at either electrode unless they get trapped during their drift and diffusion.

When a positive bias is applied to the gate while the MOS structure is being irradiated, a fraction of the electron-hole pairs generated by the incident radiation are separated by the applied field (Fig. 4) [45]. In this bias case, holes are driven to the Si/SiO₂ interface, while electrons are swept toward the gate. During their transport to the electrodes, the holes can get trapped on centers supposed to be electrically neutral before irradiation, leading to the buildup of a positive charge in the oxide [46]. Carriers which have not been trapped reach the oxide interfaces and can be swept away at the collecting electrodes. The presence of holes at the Si/SiO₂ interface has been extensively studied and invoked in the formation of interface traps [47].

This charge trapping phenomenon is common to any insulating layers, including gate oxides, lateral insulators and BOX layers. After irradiation, SOI structures thus could exhibit a specific

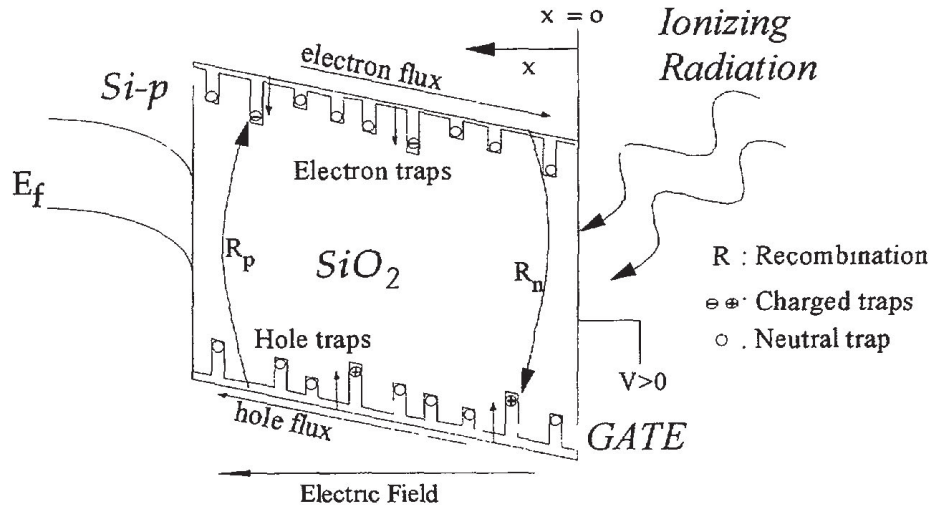


Fig. 4. — Illustration of charge transport and trapping in the MOS structure for positive gate bias (from Hervé *et al.* [45]).

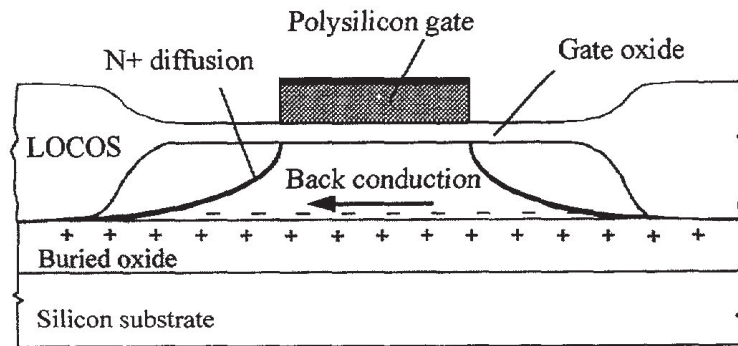


Fig. 5. — Schematic illustration of the radiation-induced back transistor in SOI technology. This parasitic structure is based on a back-gate conduction induced by the presence of trapped charge in the buried oxide.

parasitic structure due to the presence of the buried oxide, called back parasitic transistor and represented in Figure 5. In the case of thin BOX layers, the electrostatic influence of their trapped charge on the back-gate conduction is reduced.

2.3. NON-IONIZING EFFECTS: ATOMIC DISPLACEMENTS. — Particles passing through electronic materials can deposit a portion of their energy into atomic displacements. This is particularly true for heavy particles, such as heavier ions and neutrons. Damages created by atomic displacements mainly affect crystalline materials [48]. The defects created in a crystal lattice may be vacancies, interstitials or complexes of vacancies and interstitials with impurities atoms, or even more complex clusters of defects. They may cause an alteration of the electrical properties of the semiconductor crystal and lead to degradation or failure of the device. For example, additional recombination centers may be introduced which can shorten the minority carrier lifetimes and consequently degrade the gain of bipolar transistors.

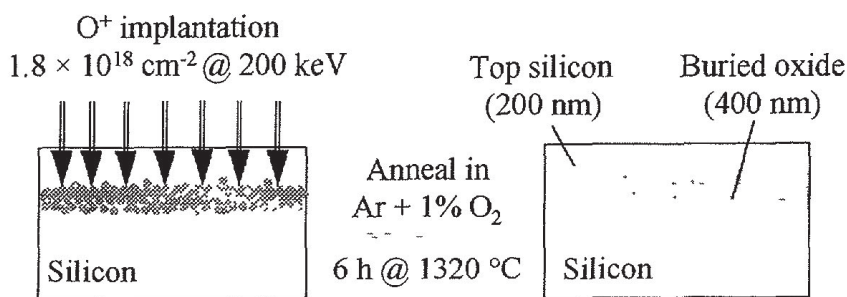


Fig. 6. — Basic principle of the Separation by IMplantation of OXYgen (SIMOX) method. The implantation and anneal conditions refer to the standard SIMOX process (After SOITEC manufacturer).

3. Silicon On-Insulator: Processing Techniques of Current Buried Oxides

3.1. THE SIMOX METHOD

3.1.1. The Standard Process. — A buried layer of SiO₂ in silicon can be obtained by directly introducing oxygen ions underneath the surface of the silicon wafer (Fig. 6) [26]. The energy of O⁺ ions directly determines the range and profile of the implanted layer. In order to reach the stoichiometry of SiO₂ in this zone, two oxygen atoms must be implanted for every silicon, thus requiring a very high ion dose, typically in the range $10^{17} - 10^{19} \text{ cm}^{-2}$.

After this implantation step, the top silicon film is damaged and an ultra high temperature treatment is then required to anneal this degradation. In the same time, this anneal step helps the redistribution of oxygen atoms, thereby leading to a uniform SiO₂ layer [31].

The thicknesses of both the top silicon layer and the buried oxide are determined by the ion energy (giving the implantation peak and range in silicon), and by the oxygen fluence. These parameters can be varied to some extent [27]. It was shown in the late 70's that the parameters giving the best results required high doses (1.5 to $1.8 \times 10^{18} \text{ cm}^{-2}$) of oxygen ions implanted at an energy of 200 keV at elevated temperature [28]. Early implantations (1980-87) were long (24 hours) due to limited flux of oxygen beams available from high-flux implanters at that time. After 1987, a new generation of very-high-flux implanters was produced, able to deliver ion beam intensities up to 80 – 100 mA, thus allowing the production of wafer batches in a shorter time and at a reasonable cost. This technical improvement was a major achievement for the development of SIMOX technology.

The most important step in the SIMOX process is that the wafer temperature during implantation is kept high (500 – 700 °C) and well controlled [29]. Damage in the silicon layer due to the oxygen implantation can be continuously annealed during the implantation. In 1985, the SOI team in Grenoble noticed that very abrupt interfaces and a high quality of silicon film could be obtained using a higher temperature anneal (6 hours anneal at 1300 °C in Ar + 1%O₂ ambient, with deposited SiO₂ capping layer) [28, 31]. Figure 7 shows the steps by which the layers gradually improved during this annealing operation.

Other buried oxide variants have been envisaged, using nitrogen implantation (SIMNI) [49–52]. Nitrogen was also implanted after oxygen, the idea being to get a buried oxynitride layer.

3.1.2. Low-Dose SIMOX Processes. — In the late 80's, other implant conditions were found and excellent BOX layers have been also obtained using lower energy (typically in the range 30 – 80 keV) O⁺ implants [53–57]. Recently, low dose implantation at an energy of 120 keV has been successfully developed, leading to the formation of thin (~ 80 nm) SIMOX buried

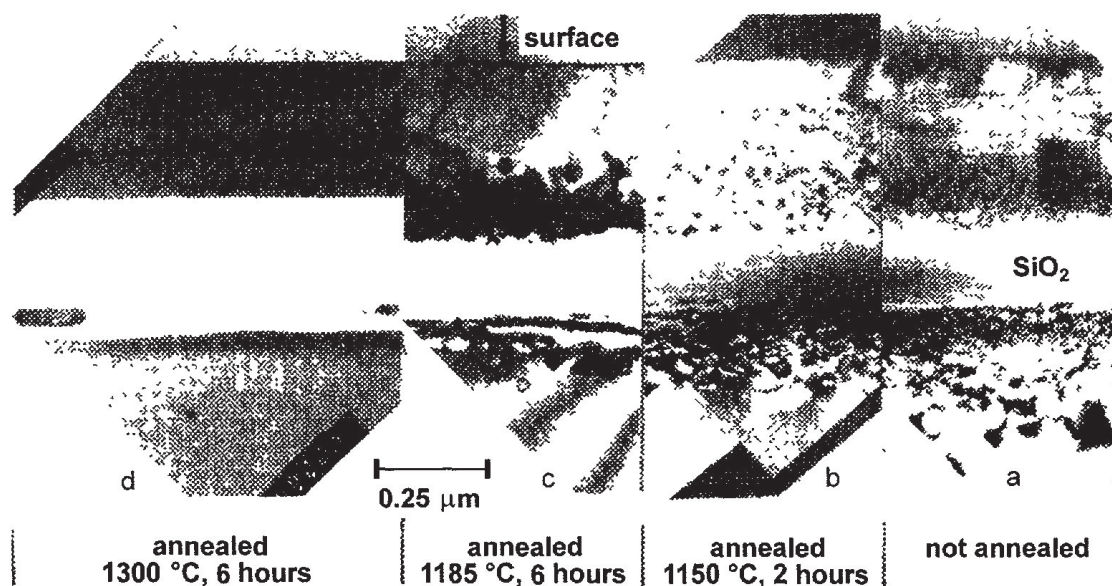


Fig. 7. — Cross-sectional XTEM micrographs showing the effect of different ultra-high temperature anneals on SIMOX layers (reprinted with permission from Ref. [31]). The micrograph labelled (a) corresponds to an as-implanted structure and the one labelled (d) to a post-anneal standard SIMOX material.

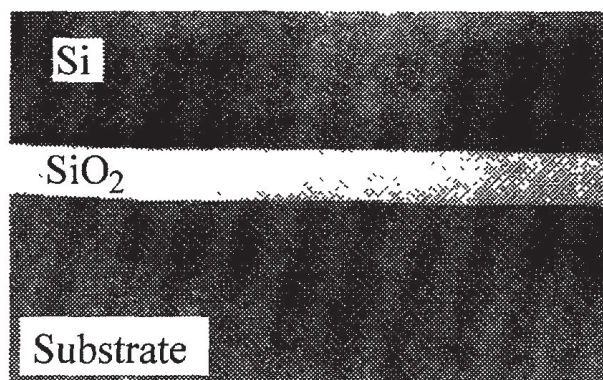


Fig. 8. — Cross-sectional XTEM micrograph of *low-dose* SIMOX (oxide thickness ~ 80 nm). Conditions: dose $4 \times 10^{17} \text{ cm}^{-2}$, energy 120 keV, (reprinted with permission from Ref. [59]).

oxides (Fig. 8) [58, 59]. Such thin materials are required for low voltage and low power technologies, since short channel effects are reduced and heat dissipation through the buried oxide is improved. Moreover, the thickness of these buried oxides can be increased with an additional oxygen implant (a second ultra-high temperature anneal is then required), giving the flexibility to adjust both the buried oxide and silicon film thicknesses. Note that a sacrificial thermal oxidation of the top silicon layer can also provide a thinner silicon film with good uniformity (~ 8 nm across wafer, ~ 50 nm from wafer to wafer).

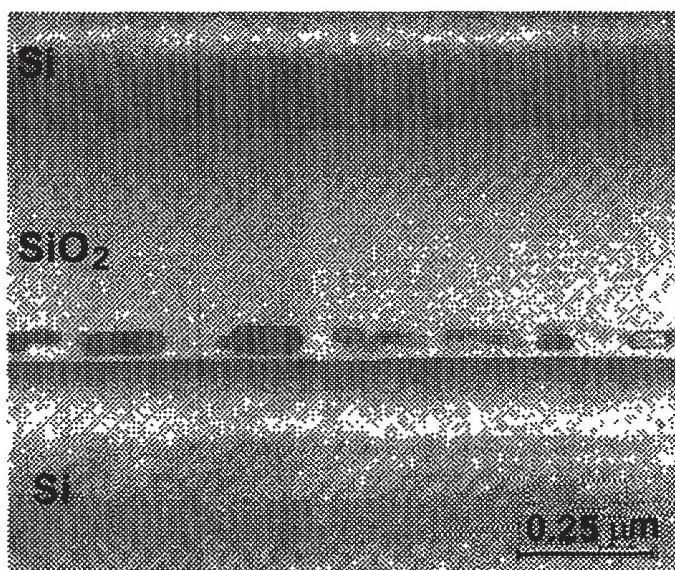


Fig. 9. — Cross-sectional XTEM micrograph of commercial SIMOX material showing an unusually high density of silicon islands in the buried oxide near the bottom Si/SiO₂ interface (reprinted with permission from Ref. [41]).

3.1.3. Main Defects in the SIMOX Buried Oxide

Silicon Islands. — Figure 9 represents an XTEM (X-ray Transmission Electron Microscopy) micrograph of residual silicon islands included in the buried oxide film [41]. Although impressive by their size, these particles are not harmful, for at least two reasons: i) they are much thinner than the oxide thickness, and therefore do not impact on the breakdown properties, and ii) they are always located close to the bottom Si/SiO₂ interface, making their net charge state of negligible influence on the top silicon layer.

Whereas the silicon islands can be considered as 3-dimensional defects, by opposition to point-defects such as oxygen vacancies, two other defect classes seem to exist in SIMOX:

One-Dimensional Silicon Columns (the So-Called Pipes). — The origin of these pipes is linked to the presence of particles at the silicon surface during the ion implantation, leaving columns of unoxidized silicon in the oxide layer [60,61]. The main consequence of the presence of these defects is a local leakage current across the oxide (in the nanoampere range) which can lead to a premature breakdown [62]. It has been recognized to have a determining impact on the manufacturing process yield of circuits.

Diluted Silicon Nanoclusters. — This type of defect (size ranging between a few and some tens of silicon atoms) occurs mainly in single implant material, and certainly results of an uncompleted oxidation [63]. The consequences are more hidden, since the silicon atoms are too far from each other to influence the electrical conduction or the electric breakdown. However, it can provide trapping sites of large capture cross-section which might play an active role during exposure to ionizing radiation. The use of multiple implantation (*i.e.* implanting the same ion dose in multiple steps, each being annealed), drastically reduces the presence of this type of defects.

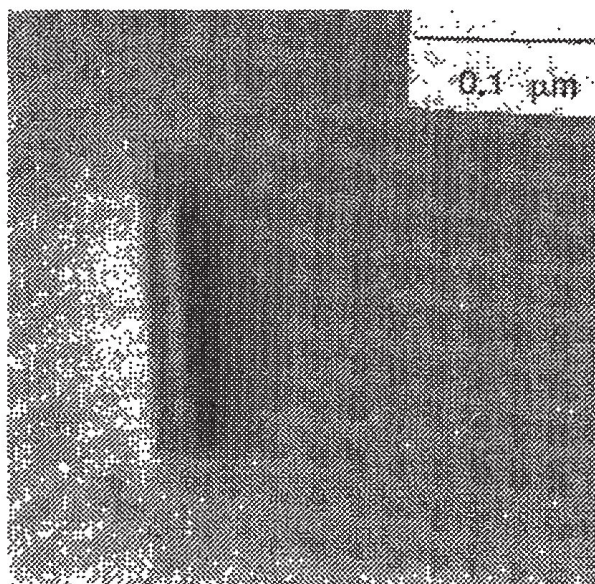


Fig. 10. — Plan view TEM micrograph of a typical Stacking Fault Tetrahedra (SFT) having a mean length of $0.1 \mu\text{m}$ (reprinted with permission from Ref. [64]).

3.1.4. Defects in the Top Silicon Film. — As far as advanced MOS technologies or Bipolar transistors are concerned, defects in the silicon film are detrimental, since they all affect the minority carrier lifetime. Improvements in the quality of the top silicon film can be obtained by drastically reducing the densities of structural defects, such as dislocations and micro-stacking faults (Fig. 10) [64,65]. Note that significant decreases of dislocation density have been obtained by optimizing implant and anneal procedures: densities in the range $\sim 10^2 \text{ cm}^{-2}$ (for the low dose material) to $\sim 10^4 \text{ cm}^{-2}$ (for the standard SIMOX) are typically measured on commercial materials [66]. Minority carrier lifetimes greater than 10 ms have been measured in top silicon layers of standard SIMOX. Conversely, the surface recombination velocity at the buried Si/SiO₂ interface was found to be in the range $10 - 100 \text{ cm s}^{-1}$. These good characteristics allow the processing of bipolar transistors with excellent characteristics.

3.1.5. Variety and Quality of SIMOX Silicon Layer and Buried Oxide. — The SIMOX material made tremendous progresses in the decade 1985-1995, due to a series of factors, mainly the use of a “clean” implanter column (avoiding metallic contamination and dust particles projection on the wafer during implantation) [67]. Other factors are due to improvements in the anneal conditions [68].

Another factor of progress is the use of fractional implantation (the so-called “multiple implantation”) [63]. Instead of implanting the whole oxygen dose in one single step, in the case of the “triple-implant” the oxygen dose ($1.8 \times 10^{18} \text{ cm}^{-2}$) is implanted in three steps of $0.6 \times 10^{18} \text{ cm}^{-2}$ each. As a result, a decrease of about one decade in the silicon dislocation density is observed as well as the disappearance of the silicon islands in the oxide. Of course the process is much more tedious in this case, since the wafers are annealed after each fractional implant step.

The new low dose SIMOX process, combined with the use of multiple implantations, has led to major improvements in the quality of both the top silicon film and the buried oxide layers. Beside the flexibility in oxide thickness, the defect densities (silicon islands, pipes, dislocations and micro stacking faults) are drastically reduced in this new and promising material.

Table II. — Summary of the practical implantation conditions and the state of the art for different SIMOX materials in mid-1995 (After SOITEC manufacturer).

Type of SIMOX	Oxygen energy (keV)	Oxygen fluence (cm ⁻²)	Silicon thickness (nm)	BOX thickness (nm)	Silicon dislocation density (cm ⁻²)	BOX pipe density (cm ⁻²)
Single implant	190	1.8×10^{18}	50 to 205	400	$< 5 \times 10^5$	< 0.2
Medium	120	4×10^{17} $+3 \times 10^{17}$	50 to 150	150	$< 1 \times 10^4$	< 2
Low dose	120	4×10^{17}	50 to 180	80	$< 1 \times 10^4$	< 2
Low dose +epitaxial Si (4 μ m)	120	4×10^{17}	4000	80	2×10^2	< 2

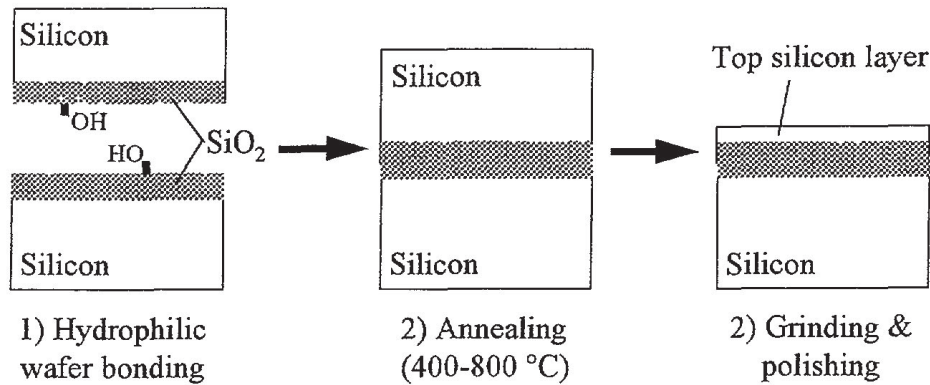


Fig. 11. — Schematic illustration of the Bond and Etch-back SOI process (BESOI).

Table II, due to the SOITEC manufacturer, summarizes the practical implantation conditions and the state of the art of the production in mid-1995 (maximum values obtained with production wafers from 4 to 6 inches in diameter).

3.2. INSULATORS BONDING (BESOI, BOND AND ETCHBACK SOI)

3.2.1. The Basics of Bonding. — This method uses a glue-less bonding process to the surface adhesion of two wafers, as illustrated in Figure 11. The layers can be as varied as Si, SiO₂, Si₃N₄, SiC, etc., each one being prepared in the best conditions, and are then brought together in a second time. However, one of the two bonded wafers has to be thinned afterwards in order to meet the top Si thickness needed by the SOI concepts and architecture. In the 80's, continuous improvements have been made in bonding pre-oxidized wafers.

Bonding mainly occurs through the formation of hydrogen bonds at Si-OH...HO-Si groups (weak bonding) or of covalent Si-O-Si bonds. Such bonding was not achieved without externally applied forces until 1985 [32]. The surfaces must exhibit a very small microroughness (less than 10 nm). They have to be cleaned in order to avoid the presence of contaminants (metallic particles, alkali ions...) at the bonding interface, and need generally to be prepared before contact, for instance by hydrophilization in NH₄OH + H₂O₂ + H₂O and rinsing in

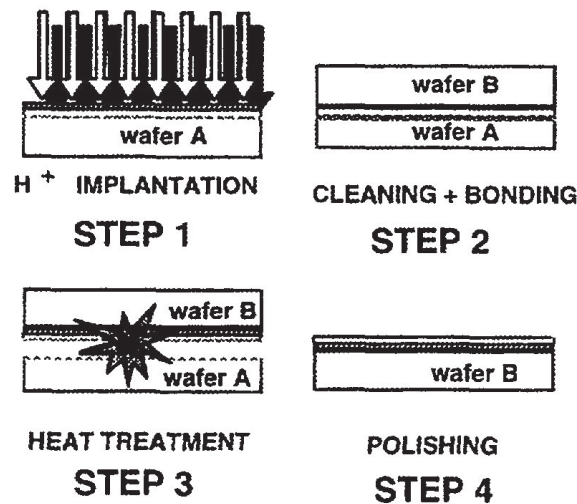


Fig. 12. — Main steps of the [®]Smart-Cut process (reprinted with permission from Ref. [70]).

desionized water [35]. Current processes mainly differ by the bonding temperature, ambient, and the subsequent treatments used [33]. Below 130 °C, fragile hydrogen bond dominates. The adhesion force is approximately insensitive to annealing temperature between 200 °C and 800 °C for hydrophilic surfaces, due to the predominant silanol condensation allowing transformation of hydrogen bonds into siloxane bonds. This bond formation is accompanied by an elastic deformation of the wafers [33]. For hydrophobic surfaces, bonding becomes efficient only beyond 600 °C [40]. Beyond 800 °C, the formation of Si–O–Si is supported by a plastic flow of the oxide. These properties allow a variety of applications, especially in the low temperature domain, but most of the problems come from the formation of voids or from the incorporation of particles or contaminating adsorbates.

3.2.2. Thinning of the Top Silicon Layer. — After bonding two oxidized silicon wafers, one of the two wafers has to be thinned down to the appropriate thickness required for the formation of the device film. Different methods have been proposed, mainly grinding and polishing or etching [69]. The first one involves removal of most of the seed wafer by grinding (which is a time-consuming operation). The surface quality is then improved by a final polishing. The surface roughness obtained with this method is typically in the range ± 300 nm. In the case of etching, usually an etch-stop layer is used to control the efficiency of the chemical etchant solution which dissolves the top silicon wafer. A second etchant solution is then employed to dissolve the etch-stop. Uniformity of the thickness films is much better in this case, below ± 10 nm.

Recently, a new process combining proton implantation and polishing has been proposed and is referred to as [®]Smart-cut (Fig. 12) [70]. It consists of implanting hydrogen ions (dose in the range $2 \times 10^{16} - 10^{17} \text{ cm}^{-2}$) into one of the two oxidized wafers before the bonding operation. After hydrophilic bonding at room temperature, the structure submits a two-phase heat treatment. During the first phase (400–600 °C), the implanted wafer splits into two parts and a thin layer of monocrystalline silicon remains bonded to the second wafer. The second phase (1100 °C) aims to strengthen the chemical bonds. Finally, the roughness of top silicon layer is reduced by performing a fine polishing. A significant save of time is also obtained with the [®]Smart-cut process (which only uses a single wafer for each produced SOI substrate) in so far as the complete thinning operation of the top silicon layer (usually time-consumable) is reduced to a single fine polishing.

3.2.3. Defects and Properties of BESOI Material. — Defects related to the top silicon layer are basically the same as that of the starting bulk silicon. Nevertheless, the complete bonding operation can induce several types of defects issued from bonding (voids, mechanical strains, contamination of the BOX) and/or thinning process (dislocations, roughness, contamination of the top silicon) [41, 69].

Voids in BOX layers can be generated by particles present on the wafer surfaces before contacting (extrinsic voids) or induced after this operation by the outgassing of surface contaminants (like hydrocarbons) and/or gas precipitation probably around small structural defects at the wafer surfaces (intrinsic voids). In the two cases, the size of the voids (10^{-2} to several millimeters in diameter in the extreme cases) is strongly affected by the conditions of bonding and by the temperature and the ambient of the annealing process. Specific annealing procedures have been proposed to try to reduce the void density in BOX layers. It has been found that intrinsic voids can be eliminated by high-temperature annealing (900 – 1100 °C) whereas only the smaller extrinsic voids can decrease in size after an extensive annealing at 1150 °C [69].

Another type of defects related to BESOI material is the bond contamination which can induce trapped charges and defect precursors (later revealed by irradiation) at the bond interface, in the depth of the BOX film. Species such as carbon, oxygen, chlorine and fluorine have been measured in significant concentrations at the bond. Carbon and boron contaminations have been also frequently reported and can lead to catastrophic degradation of BOX insulating properties [69].

3.2.4. New BESOI-Based Materials and Designs. — Other SOI structures have been obtained by wafer bonding, such as SiC on SiO₂ on Si [71]. In this bonding approach, SiC is epitaxied on Si and the SiC layer is then oxidized before bonding and thinning operations. Gallium Arsenide has also been bonded to silicon by CVD-depositing a thin phosphosilicate glass (PSG) layer at 400 °C on the surface of a polished wafer [72]. The phosphorous content in PSG is adjusted to match the combined thermal expansion of GaAs and Si. GaAs is then back etched. This method tries to avoid the difficulty of a direct epitaxy of GaAs on silicon, which is possible but leads to a strained interface. InP bonded to Si has been obtained using a similar deposited SiO₂ bonding layer. Beside III-V's, other wafer bonding have been envisaged, such as Ge on Si, and Si on fused quartz, using a buffer SiO₂ layer [73]. In another field of interest, wafer bonding allows evolution towards 3D integration of active layers [2, 74]. Since 1986, some CMOS circuits have been designed using inverters obtained from stacked PMOS and NMOS transistors, each of them made apart on two different wafers (ELVIC method: Elementary Level Vertically Integrated Circuit [75]). In this new approach, the two wafers, capped with a polyimide layer, are bonded together and transistors are wired by means of Al/Au vias. The wafer bonding method can be generalized to circuit bonding, thus allowing to double the integration density or to combine two different types of circuits. Recently, this approach has been successfully employed to design high density circuits, such as 64 Mbit Dynamic Random Access Memories (DRAM's) [76], as detailed in Figure 13. Further improvement would come from the capability to develop multiple-stacking processes in order to achieve higher densities of integration.

4. Radiation Behaviors of Advanced SOI Materials

4.1. SIMOX BURIED OXIDES. — At the origin, the main driving force for the evolution of SIMOX technology was first concentrated in improving the quality of the top silicon film, where the devices are fabricated. Little attention was paid to the quality of the buried oxide until device performance was sufficiently enhanced. It then appeared that the properties of

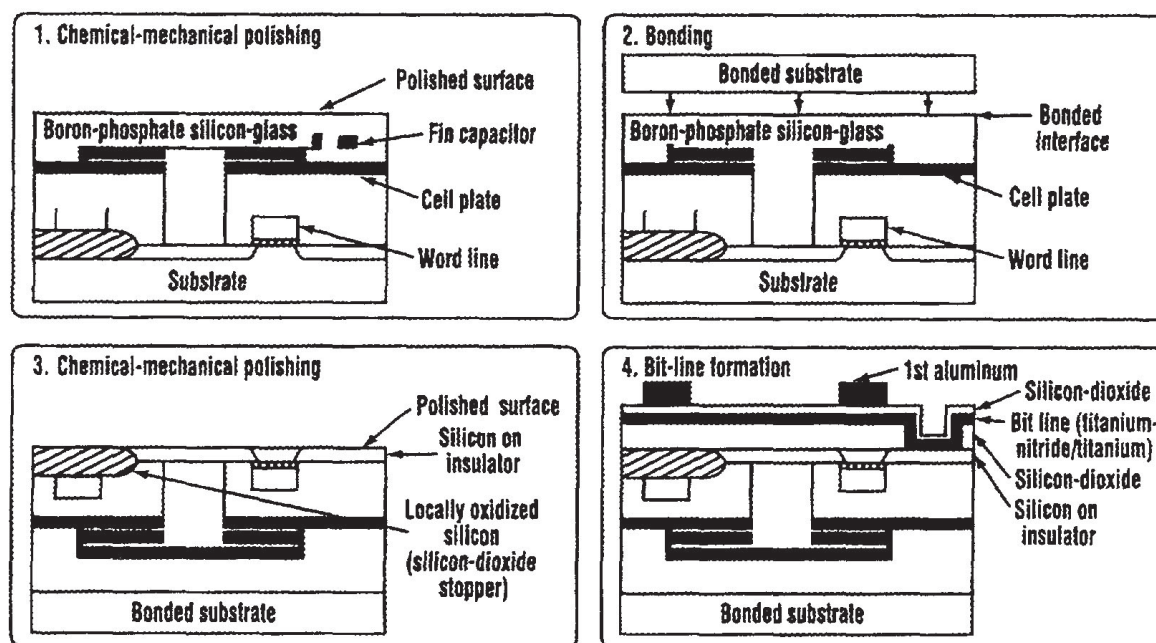


Fig. 13. — Schematic process sequence of a 64 Mbit DRAM memory by using bonded SOI technology and reversed stacked capacitor cells (reprinted with permission from Ref. [76]).

the buried oxide are very different from thermal oxide, and can greatly influence the device process yield, as well as the radiation-induced behavior. Defect buildup in SIMOX buried oxide has thus been extensively studied since then, and different methods have been used in the literature: X [77] or γ [78] irradiation; UV or VUV illumination [79]; charge injection [80].

X-ray irradiation of a MOS device leads to electric charge trapping in the insulating layer. The radiation-induced trapping behavior appears to depend upon the oxidation process. Recent studies [77, 78, 81–83] have shown the discrepancy between thermal oxide and SIMOX buried oxide: the former seems to be dominated by interface hole trapping, and the latter is interpreted in terms of large bulk trapping. Furthermore, SIMOX buried oxides show no evidence of interface state creation until very high ionizing doses [84], but it has recently been shown that large electron trapping can also occur in X-ray irradiated SIMOX oxides [85, 86]. Some general observations and characteristics of SIMOX buried oxide are found whatever the characterization method used.

4.1.1. Electron Paramagnetic Resonance (EPR) Measurements. — Electron paramagnetic resonance measurements show an important creation of paramagnetic defects in this SIMOX material [77–79, 87].

By irradiation (X or γ), E'_γ center generation grows up linearly with irradiation dose [77, 79], and does not exhibit any saturation, at least up to a dose of 200 Mrad (SiO_2). This result suggests the presence of a large quantity of precursors (estimated around 10^{18} cm^{-3}). Moreover, this paramagnetic defect creation is greatly enhanced by the application of an electric field across the oxide during exposure to the radiation, whatever the sign of the applied field. Etchback measurements of irradiated samples reveal that the E' center generation is uniformly distributed in the oxide volume.

By charge injection, E'_γ center generation is also observed, as well as the appearance of a new type of paramagnetic defect, namely the E'_δ center [78, 80]. This paramagnetic center differs

Table III. — Summary of measured trap densities and capture cross sections extracted from electrical measurements using an exponential fit method described in reference [89].

BOT Type	T_{ox}	Hole Traps		Electron Traps	
		N_t	σ_t	N_t	σ_t
		cm^{-2}	cm^2	cm^{-2}	cm^2
Thin SIMOX	80	$2.7 \pm 0.3 \times 10^{12}$	$2.9 \pm 0.3 \times 10^{-13}$	$7.1 \pm 0.1 \times 10^{11}$	$28 \pm 16 \times 10^{-15}$
Medium I SIMOX	95	$4.3 \pm 0.2 \times 10^{12}$	$2.8 \pm 0.2 \times 10^{-13}$	$2 \pm 0.2 \times 10^{12}$	$15 \pm 10 \times 10^{-15}$
Medium II SIMOX	121.5	$5.6 \pm 2.2 \times 10^{12}$	$3.7 \pm 1.7 \times 10^{-13}$	$2.4 \pm 0.3 \times 10^{12}$	$7.9 \pm 3.3 \times 10^{-15}$
Thick SIMOX	400	$1.3 \pm 0.4 \times 10^{13}$	$5.2 \pm 1.3 \times 10^{-14}$	$2.5 \pm 0.3 \times 10^{12}$	$5.4 \pm 3.2 \times 10^{-15}$
Thick SIMOX	400	$1.5 \pm 0.2 \times 10^{13}$	$6.3 \pm 0.8 \times 10^{-14}$	$9.2 \pm 0.3 \times 10^{11}$	$35.5 \pm 1.1 \times 10^{-15}$

from classical E' center, since the spin (unpaired electron) is delocalized in this case. The model proposed to account for its microscopic structure is based upon the existence of clusters of five silicon atoms in the oxide, upon which the unpaired electron is shared. Actually, this defect seems only observable after a selective hole injection in the oxide, and not by X irradiation, or UV and VUV illumination. These two types of E' centers, induced by hole injection, become diamagnetic after electron injection. Both centers (E'_δ and E'_γ) seem to be positively charged when paramagnetic. It is actually reasonably thought that the E'_δ center should have a large capture cross-section for electrons than the E'_γ center, which would explain why it is not observed after irradiation. In this case, electrons and holes are created simultaneously, so the E'_δ can rapidly capture an electron, and thus become neutral and diamagnetic.

4.1.2. Electrical Measurements. — Electrical measurements of the net trapped charge in the material [77,88], do not agree with EPR measurements. Indeed, the net trapped charge exhibit a saturation behavior *versus* irradiation dose, and even in certain cases (negative bias during irradiation) shows the buildup of a net negative trapped charge at high doses. Nevertheless, some characteristics are common between trapped charge and E' signal measurements: i) both the trapped charge and the EPR signal do increase with the applied electric field amplitude, whatever its sign; ii) the evolution of E'_γ signal and midgap voltage shift is similar during an isochronal anneal at zero bias.

The various SIMOX processes described in the previous sections have been investigated in terms of radiation-induced charge trapping properties. The aim is naturally to compare the different oxides, and to try to derive a common tendency for this material. The method of extraction of trap densities and capture cross sections, reported in Table III, has been described elsewhere [89]. It basically consists of fitting a theoretical model for the variation of the characteristic voltage (midgap voltage) of the MOS device due to the presence of the oxide trapped charge (ΔV_{ot} for oxide trapped charge voltage shift), to experimental data obtained in the limiting cases of strong positive (+1 MV cm^{-1} for hole trap parameters) or negative (−1 MV cm^{-1} for electron trap parameters) biases applied during irradiation. This variation has been theoretically shown to be exponential with irradiation dose [89]. Saturation values of

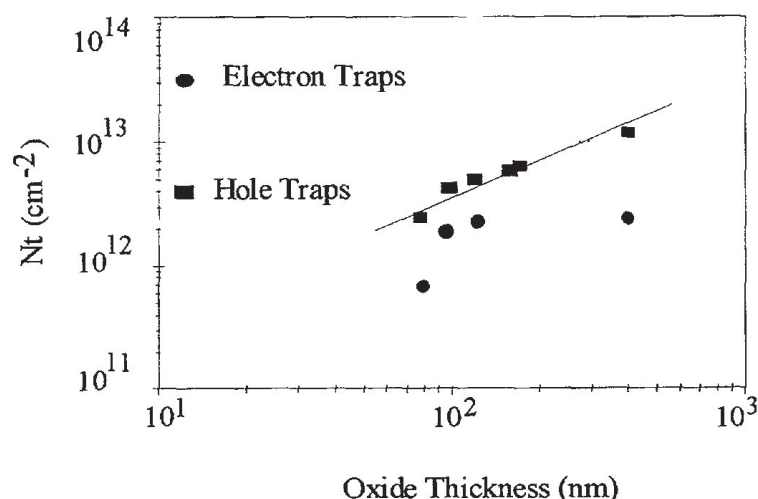


Fig. 14. — Correlation between the trap surface densities and the Buried Oxide thickness as obtained from electrical measurements.

ΔV_{ot} provide equivalent trap densities at the Si/SiO₂ interface, while the slopes of the curves provide trap capture cross sections.

Due to large discrepancies in capture cross sections of holes and electrons, hole trapping dominates at low dose (typically below 1 Mrad (SiO₂)), whereas electron trapping is predominant at high dose (above 1 Mrad (SiO₂)). Electron trapping is only evidenced in the case of an irradiation with a high negative applied bias, *i.e.* when the electrons, generated by the radiation and separated by the high electric field, are driven to the Si/SiO₂ interface. In this case, electrons trapped in the vicinity of the interface will induce a measurable image charge in the silicon substrate. When the irradiation is performed with a positive applied field, the electrons escaping initial recombination will be swept toward the gate. Even if they are trapped there, the electrostatic effect of this negative trapped charge may not be large enough to induce a measurable threshold voltage shift.

The correlation between the extracted trap densities and BOX thickness is shown in Figure 14. It suggests that the electron trap surface density does not depend on the oxide thickness, down to a thickness of 100 nm. Below this value, the electron trap surface density decreases noticeably. The simplest interpretation is to suppose that the electron traps are located in the interfacial areas (less than 100 nm from the silicon interfaces).

This result is in agreement with recent observations and model relating the origin of electron traps to the ultra high temperature treatment in SIMOX oxides [90]. High temperature anneal of an oxide film confined between two silicon layers is shown to result in degradation of the sandwiched oxide, in terms of oxygen-vacancy defects creation.

The physical mechanism producing the defects is related to the out-diffusion of oxygen from the oxide, caused by the oxygen solubility in the silicon layers at this temperature [90]. The O interstitial density in Si is far from its solubility limit at the anneal temperature, and represents the driving mechanism for this diffusion. This depletion should occur at each interface of the buried oxide. The authors calculate the distance from which oxygen is getterred from the oxide layer during the ultra-high temperature anneal, and found it to be 120 nm from the interface. This distance has to be compared to the lowering of the electron trap density observed around this oxide thickness, and leads us to propose that the interfacial locations of electron traps could likely be correlated to this interface oxygen depletion.

On one hand, the exact nature of the defect responsible for this negative charge trapping and its relation with the oxygen out diffusion still remains unclear, although we note that oxygen vacancy itself has been proposed as a possible candidate for electron trap [91]. On the other hand, the hole trap surface density is shown to be proportional to the oxide thickness, and thus confirms the existence of a uniform hole trap volume density. For standard SIMOX, this was confirmed by the study of V_{ot} using etch-back experiments concerning the oxide trapped charge as well as E' defects [92].

In all these SIMOX materials, the charge trapping properties are independent of the oxide thickness, in this sense that the volume hole trap density seems to be constant for the material, and electron traps are also present in each type of SIMOX.

Modifying the oxygen implantation conditions (oxygen fluence and energy), thus did not have a major effect on the trap properties of the material. It confirms that the most damaging factor of the process is the annealing step (temperature and gas ambient) performed on a confined oxide layer. It is the only common step of the different SIMOX processes, and it degrades any confined oxide structure (even a thermal oxide, see Ref. [89]) in a similar way, *i.e.* by out-diffusion of oxygen from the oxide, and generation of oxygen-vacancy related defects.

4.2. BESOI BURIED THERMAL OXIDES. — The radiation-induced behavior of BESOI buried oxides has also been investigated in the literature. Since these insulators originate from thermal oxides, one would expect them to exhibit exactly the same charge transport and trapping properties as the original layers. Results however show that it is not always the case. It is true that some properties of standard thermal oxide, such as charge transport properties, still remain in BESOI material. But the presence of the bonding interface in the oxide greatly modifies the radiation-induced charge trapping properties of the material. Moreover, the use of a high temperature bonding or post-bonding anneal step also contributes to the observed differences.

The presence of the internal bonding interface and its position in the oxide is the key parameter influencing the radiation-induced properties of the BESOI structure. This bonding interface usually is of relative poor quality, for example process-induced fixed negative charge has been found at this interface before irradiation [33, 93]. As a matter of fact, after irradiation this interface can efficiently trap both kinds of charge carriers [83, 94–96]. Depending on the position of this interface within the buried oxide, the electrostatic influence of its trapped charge can have different effects on the overlying transistor. These trap densities at the bonding interface are specific to the BESOI buried oxide, and superimpose on the “natural” trap densities located at each Si/SiO₂ interface (at the Si-film/oxide and oxide/bulk-Si interfaces). This material, made from thermal oxide, can thus exhibit deep trapping of both holes and electrons, while typical soft thermal oxides only show hole trapping. The presence of water from the hydrophilic bonding surfaces could be responsible for generating water-related deep electron traps in the BESOI buried oxide at the bonding interface [96]. These observations have been made on BESOI material with and without post-bonding anneal. The influence of a high temperature anneal on such Si/SiO₂/Si sandwich structures has been shown to induce a chemical reduction of the buried oxide [83, 89, 90]. This is of course the case in BESOI materials as well, and such annealed structures, while having less macroscopic defects (such as voids at the bonding interface), then show an enhanced quantity of oxygen vacancy related defects. Their radiation-induced behavior tends to look like that of SIMOX buried oxide [83, 89]. The same type of defect precursors (oxygen vacancies) are induced in the material, and the same defects are present independent of the method by which the oxide is initially formed.

5. Summary

In conclusion, the recent emergence of new varieties of buried oxides on silicon offers serious alternatives to the existing silicon technology as well as new technological solutions (only achievable with a SOI design) to design novel structures and circuits. SIMOX and BESOI materials have experienced the most important progresses and are now available and very competitive on the SOI market. The structural and electronic properties of these insulating layers have been drastically improved in the last decade and are now compatible with advanced microelectronics processes in the field of low power, high speed, high temperature and very rad-hard applications.

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