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CHAPTER 11

DEPOSITION

Microchip fabrication is a planar process involving many different film layers on the wafer surface. Deposition is a process that places the film layers on the wafer. Conductor and insulator films are essential to the successful fabrication of semiconductor devices on silicon substrate wafers. Film layering technology is used to manufacture the circuits and to connect the different IC devices, primarily with metal conducting layers sandwiched between insulating dielectric layers.

Many different types of films are deposited on wafers during the fabrication process. In some cases, these deposited films become an integral part of the device structure, while other sacrificial films are used for particular processing steps and then removed. Films deposited during microchip fabrication are often referred to as thin films because they are so thin that their electrical and mechanical properties differ from a thicker bulk film of the same material.

This chapter will discuss the processes and equipment used to deposit thin films, with a focus on dielectric films such as silicon dioxide and silicon nitride and the deposition of polysilicon. The deposition of metal and metal compound thin films is discussed in Chapter 12.

OBJECTIVES

After studying the material in this chapter, you will be able to:

1. Describe multilayer metallization. Discuss the acceptable characteristics of a thin film. State and explain the three stages of film growth.
2. Provide an overview of the different film deposition techniques.
3. List and describe the eight basic steps in a chemical vapor deposition (CVD) reaction, including the different types of chemical reactions.
4. Describe how CVD reactions are limited, and explain reaction dynamics and the effect of dopant addition to CVD films.
5. Describe the different types of CVD deposition systems, explain how the equipment functions, and discuss the benefits/limitations of a particular tool for film applications.
6. Explain the importance of dielectric materials for chip technology, giving examples of applications.
7. Discuss epitaxy and three different epilayer deposition methods.
8. Explain spin-on-dielectrics.

INTRODUCTION

The design and fabrication of early semiconductor wafers from the MSI and LSI eras was relatively straightforward. This process consisted of fabricating the semiconductor devices in silicon and interconnecting the devices to one metal conducting layer sandwiched between silicon dioxide as the dielectric material. Figure 11.1 on page 258 shows the deposited layers needed to make an early nMOS transistor. This technology was an extension of the first planar transistors made in the SSI era. The critical dimension was well over one micron. The wafer layers were not flat structures due

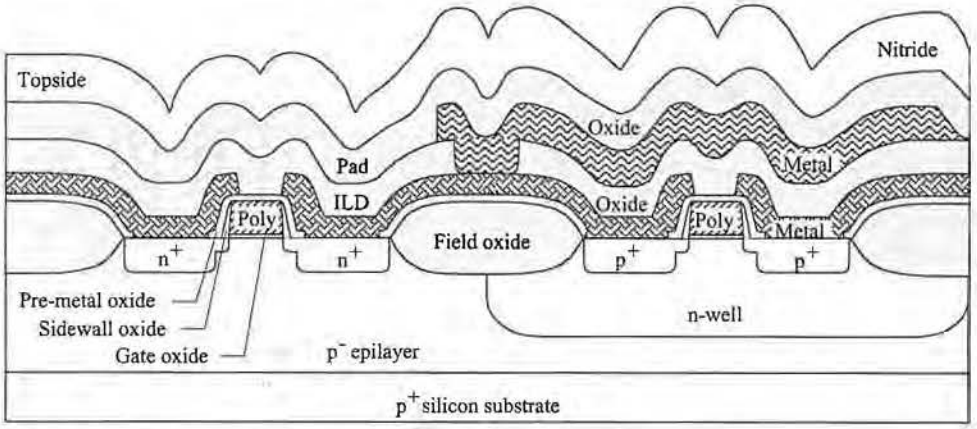


FIGURE 11.1 Film Layers for an MSI Era nMOS Transistor

to varying feature heights, which becomes a limiting factor for high-density chips with multiple metal layers needed in the ULSI era.

As wafers progress to higher density chips with shrinking geometries of 0.18 μm and below, the materials and processes used in wafer fabrication are undergoing dramatic changes. There is a concurrent scaling of all device features to maintain electrical performance. To make electrical connections in today's advanced microchips, six or more conducting metal layers are required. New metal conductor materials are needed to maintain electrical performance. Advanced dielectric materials are deposited between the metal films to provide adequate insulation protection. At the same time, each chip has literally tens of billions of electrical connections between the various metal layers and silicon devices. The ability to deposit reliable thin-film materials is a critical operation in a wafer fab. Thin films is a major process step in wafer fabrication, as shown in the process flow model in Figure 11.2.

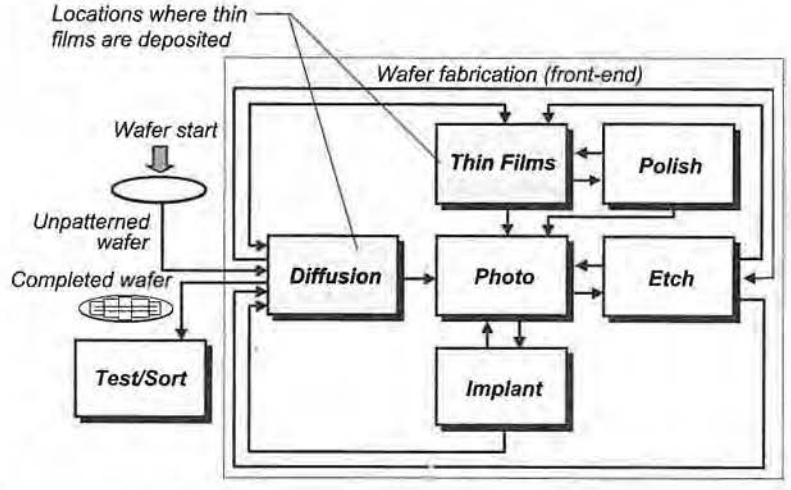


FIGURE 11.2 Process Flow in a Wafer Fab
(Used with permission of Advanced Micro Devices)

Film Layering Terminology

Multilevel metallization refers to the metal and dielectric layers needed to interconnect the densely packed devices on the wafer. An example of this process is shown in Figure 11.3. Without the dielectric insulating layers, electrical shorts would occur (similar to electrical wiring without its insulating cover). The metal layers are connected by openings in the dielectric filmreferred to as *vias*.

Adding metal levels is costly to manufacture. It is estimated that the addition of a single metal level in a CMOS process adds approximately 15% to the total wafer fabrication cost.[1] The

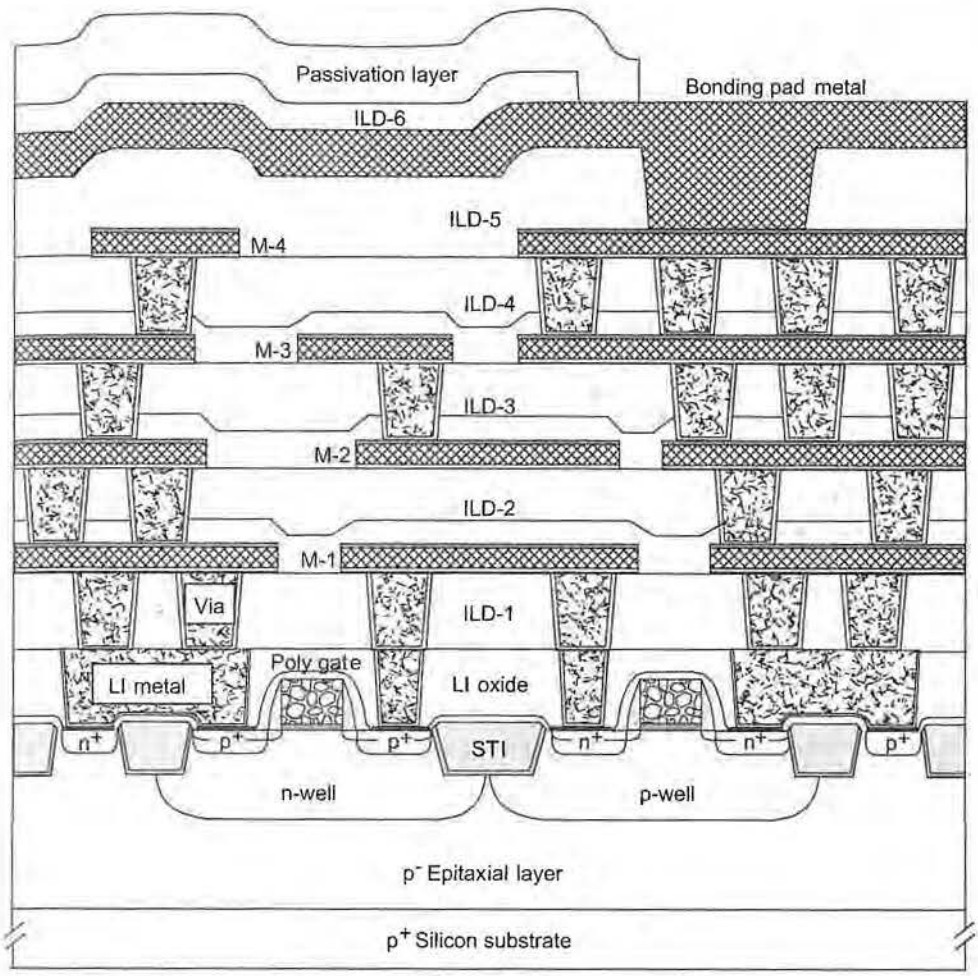
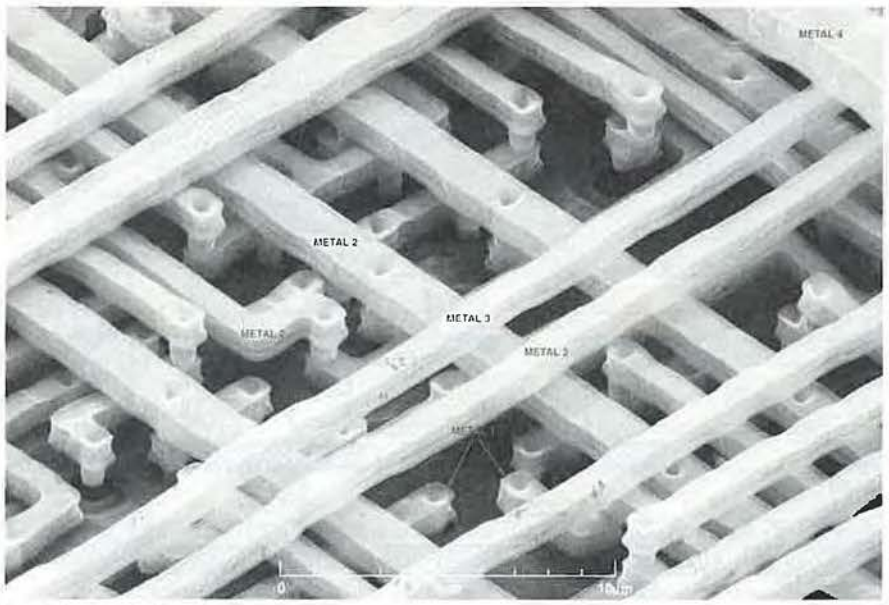


FIGURE 11.3 Multilevel Metallization on a ULSI Wafer

complexity added to wafer manufacturing by additional metal levels makes it important to reduce defects to ensure the chip yield is not impacted. The chip designer considers the tradeoffs among cost, complexity, and performance across the different wafer fab process areas for implementing additional metal levels.

Metal Layers ■ *Aluminum metallization* is the use of aluminum alloy for interconnect wiring. Aluminum alloy has been used since the beginning of semiconductor manufacturing. The Al metal is deposited on the entire surface of the wafer in a solid thin film and then etched to define the width and spacing of the interconnect lines. The industry is undergoing a transition to copper metallization to achieve increased chip speed with fewer process steps (copper metallization is reviewed in detail in Chapter 12). Each metal layer can be referred to as Metal-1, Metal-2, and so on. *Critical layers* are those metal layers with linewidths etched to the critical dimension of the device (e.g., CD of 0.15 μm). For ULSI, the CD typically occurs at the polysilicon features of the gate, the oxide structure, and the metal layers closest to the silicon surface. Critical layers are sensitive to particulate contamination (killer defects) and reliability issues such as electromigration are more pronounced in fine geometry linewidths. *Noncritical layers,* usually the upper metal levels, have much wider line widths, often 0.5 μm and larger, and are less sensitive to particulate contamination. However, factors such as long conductor lengths in the noncritical upper levels can affect chip speed and power consumption.[2]

Dielectric Layers ■ The dielectric layer between the active devices in silicon and the first metal layer is termed the *first interlayer dielectric (ILD-1)*. This layer is also called the *premetal dielectric (PMD)*. ILD-1 is typically a doped silicon dioxide, or glass (explained later in this chapter). The



Metal Layers in a Chip
(Micrograph courtesy of Integrated Circuit Engineering)

important function of the ILD-1 layer is to isolate transistor devices in two ways: electrically from the metal interconnect layers, and physically from contamination sources such as mobile ions. The ILD-1 has a restricted thermal budget in high-performance logic devices in order to avoid degrading transistor characteristics.[3]

The *interlayer dielectric* (*ILD*) is used between different metal layers in the device. The ILD serves as an insulating film between two conducting metals or adjacent metal lines. The ILD has traditionally been silicon dioxide (SiO_2) with a dielectric constant of around 3.9 to 4.0.[4] The dielectric constant is an important property of deposited insulating films because it directly affects circuit speed performance (see the following section).

FILM DEPOSITION

A *thin film* is a thin, solid layer of a material created on a substrate. If a solid material has three dimensions (thickness, width, and length), then a thin solid film has one of its dimensions (usually thickness) much smaller than the other two (see Figure 11.4). The thin film is bonded to a wafer substrate, which has a much thicker dimension than the film. The thin-film surface is so close to the substrate that it has a profound influence on the physical, mechanical, chemical, and electrical properties of the thin film material.[5] The most widely used unit to describe the thickness of a thin film in wafer fabrication is the angstrom (Å).

Thin film deposition in semiconductor fabrication is any process that physically deposits a film on the wafer substrate. The film can be either a conducting, insulating, or semiconducting material. Examples of deposited films are polysilicon, silicon dioxide (SiO_2), silicon nitride (Si_3N_4), polysilicon (silicon in a polycrystalline structure), and metals such as copper and refractory metals (e.g., tungsten).

Thin-Film Characteristics

For a thin film to be acceptable in wafer fabrication, it must have desirable film characteristics. General characteristics of an acceptable thin film for device performance are:[6]

- Good step coverage
- Ability to fill high aspect ratio gaps (conformality)
- Good thickness uniformity
- High purity and density

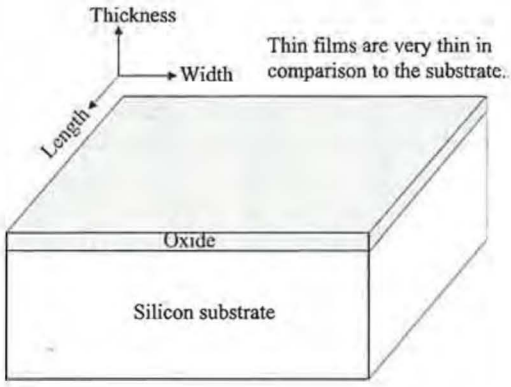


FIGURE 11.4 Solid Thin Film

- Controlled stoichiometries
- High degree of structural perfection with low film stress
- Good electrical properties
- Excellent adhesion to the substrate material and subsequent films

Film-Step Coverage ■ It is desirable for thin films to maintain a uniform thickness over surface features (see Figure 11.5). Steps on the wafer surface occur due to three-dimensional shapes from patterned features that create surface topography. If the film thins excessively at a step, this can cause high stress, electrical shorts, or undesirable induced charges in the device. Films with minimum stress are important, since stress can lead to substrate deformation in a convex or concave shape. All deposition techniques result in the formation of some stress in films.

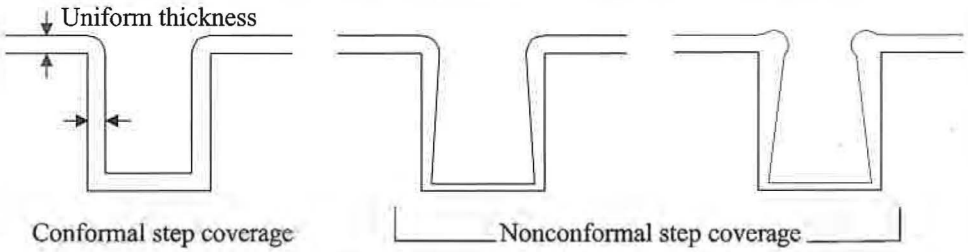


FIGURE 11.5 Film Coverage Over Steps

High Aspect Ratio Gaps ■ A small gap (trench or hole) is characterized by its *aspect ratio,* which is defined as the ratio of its depth to width (see Figure 11.6 on page 262). Aspect ratio is expressed as a ratio, such as 2:1, which in this case means the gap depth is two times the width. A gap can also be specified by its opening width, such as 0.25 μm, which may be different than the CD of other structures on the wafer. The ability to fill very small gaps and holes on the surface of the wafer has become one of the most important film characteristics for devices fabricated with sub-0.25 micron geometries. Examples of gaps that require effective gap-fill capability are vias passing through the interlayer dielectric (ILD) and trenches for shallow trench isolation (STI).[7] A high aspect ratio is typically above 3:1, with some applications having aspect ratios of 5:1 or larger. High aspect ratio gaps make it difficult to uniformly deposit the film, leading to pinch-off and voiding. Deposition processes that can produce uniform, void-free films in high aspect ratio openings are critical in the sub-0.25 μm era of high-density IC circuits with shrinking geometries.

Thickness Uniformity ■ Acceptable thin films are conformal with good thickness uniformity, which means the film follows the outline of the base material in all areas. The resistance of a material will change with varying thickness, which would be undesirable. Thinner layers of film also

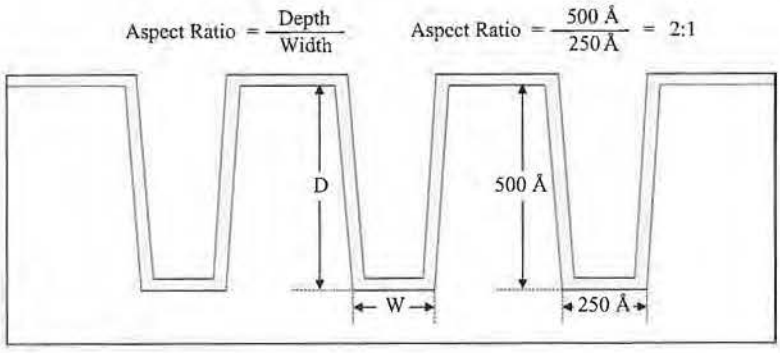
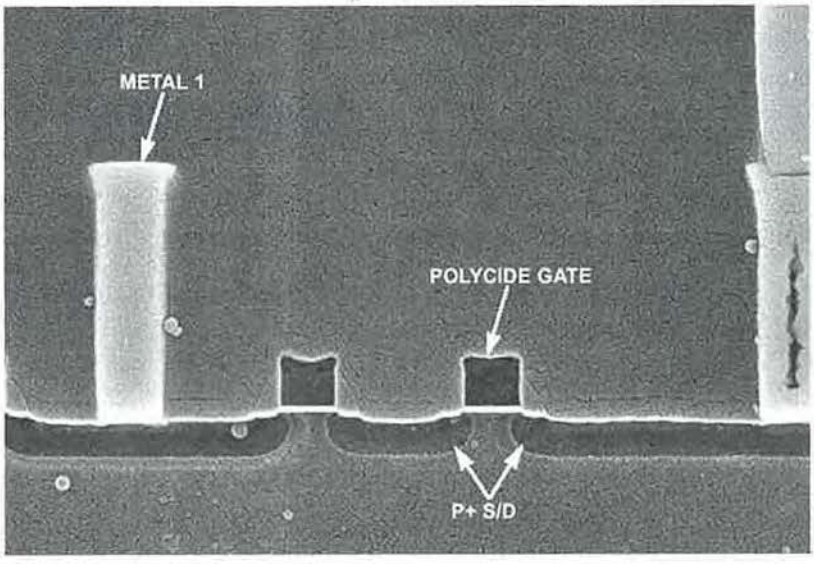


FIGURE 11.6 Aspect Ratio for Film Deposition



High Aspect Ratio Gap
(Micrograph Courtesy of Integrated Circuit Engineering)

tend to have more defects such as pinholes, which leads to less mechanical strength. It is desirable for thin films to have good surface flatness to minimize steps and cracking.

Film Purity and Density ■ High film purity means that the film does not have any unwanted chemical elements or molecules, which is important if the film is to function properly. This includes the avoidance of contaminants such as mobile ionic contaminants (MICs) and particulates. The occurrence of film contaminants such as hydrogen can degrade film properties. The density of the film is an important indicator of film quality because it means the film is free of pinholes and voids. A porous film has lower density and in some instances a lower refractive index than a nonporous film.

Stoichiometry ■ A desirable film will have uniform composition. As chemicals undergo change in a reaction, stoichiometry describes how the quantities of reactants and products are produced once the reaction ends or stabilizes. *Stoichiometry* is the ratio of one component amount to another component amount in a compound or molecule (e.g., the H_2O stoichiometric ratio is 2:1). If you know what is in a reaction, then stoichiometry tells you how much of the ingredients was needed. The chemical reactions that occur in deposition are complex and can lead to films that have a different composition than intended. A goal in deposition is to have the correct quantity of molecules in the reaction so that the deposited film approaches the ratio of the elements in the nominal chemical formula of the incoming gas.

Film Structure ■ The film structure is critical, especially related to the grain size. Materials tend to collect and grow as grains during the deposition process. If the grain size varies in a film, then it

will have varying electrical and mechanical properties that can affect the long-term reliability of the film, especially concerning electromigration (discussed in Chapter 12).[8] The growth of a film can cause undesirable stress in the film layer that deforms the wafer substrate, leading to film cracking, delamination or void formation. An example of this condition is hydrogen contamination in nitride film deposition, which leads to a compressive stress.[9] The objective during film deposition is always to minimize the amount of stress.

Film Adhesion ■ Film adhesion to the substrate material is important for thin films to avoid delamination and cracking. A cracked film can cause surface roughness and allows contamination to pass through the film. For insulating films, cracks can lead to electrical shorts or current-leakage paths. Adhesion of a film to a surface is determined by the cleanliness of the surface and also by the type of material to which the film can alloy. Metals such as chromium, titanium, and cobalt are often useful for their adhesion properties (see Chapter 12). Good adhesion of films in multilevel metallization is critical to maintaining the overall electrical and mechanical integrity of the structure. This is true in the as-deposited condition and after subsequent processing.

Film Growth

A deposited film grows in three distinct stages (see Figure 11.7).[10] The first stage is *nucleation* where clusters of stable nuclei are formed. This stage occurs when the first few atoms or molecules of the reactants combine to form isolated patches of film that attach to the wafer surface. Nucleation occurs directly on the wafer and is essential to further thin film growth. The second stage is the *nuclei coalescence* into clusters, also referred to as *island growth.* These randomly oriented island clusters grow based on surface mobility and the density of the cluster. The island clusters continue to grow and eventually develop into the third stage, a *continuous film* where they meet and form a solid sheet that spreads across the substrate surface.

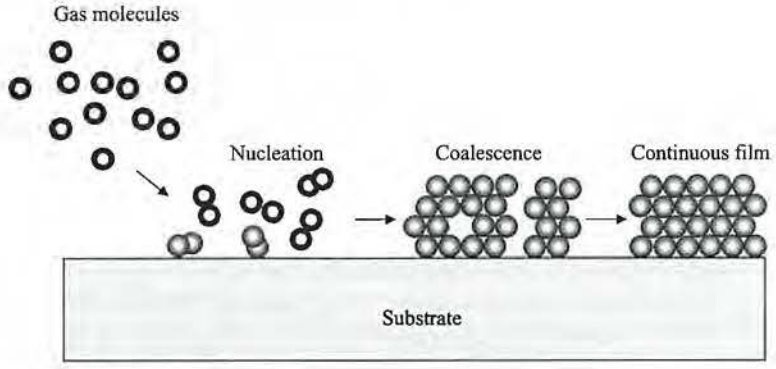


FIGURE 11.7 Stages of Film Growth

The size of the individual cluster, before meeting a neighboring cluster, is related to the surface mobility of the reacting species and the density of the nuclei. A high surface mobility and/or low nucleation rate promote the formation of relatively large clusters. This condition generally leads to polycrystalline films with short-range crystal order. On the other hand, low surface mobility combined with a high nucleation rate leads to amorphous film growth with no short-range order.[11] Low deposition temperatures usually favor amorphous films because the low thermal energy slows the surface mobility of the reacting materials.

Deposited films can be amorphous, polycrystalline or single crystalline.[12] Semiconductor films are used in all three forms. Insulator or metal films are usually amorphous or polycrystalline. Silicon deposited on an oxide layer is polycrystalline, as in the polysilicon used in the gate structure. Epitaxial single-crystal films are necessary for reliable semiconductor properties. To obtain a single-crystal deposited film, it is deposited on a single-crystal wafer substrate.

Film Deposition Techniques

Deposition of materials onto the wafer surface places a continuous thin film on the wafer. The film material derives from an external source, which may be a gas source that produces the material to be deposited through a chemical reaction or a solid target source that requires the physical removal of the material. With the increased complexity of semiconductor processing in the ULSI era, the number of deposited films on a wafer is high. As a result, the deposition of thin films is one of the most common processes in the semiconductor industry.

There are different techniques used in wafer fabrication to deposit films on a substrate. The major deposition methods shown in Table 11.1 are generally grouped into chemical or physical processes.

TABLE 11.1 Techniques of Film Deposition

Chemical Processes		**Physical Processes**		
Chemical Vapor Deposition (CVD)	**Plating**	**Physical Vapor Deposition (PVD or Sputtering)**	**Evaporation**	**Spin-On Methods**
Atmospheric Pressure CVD (APCVD) or Sub-Atmospheric CVD (SACVD)	Electrochemical deposition (ECD), commonly referred to as electroplating	DC Diode	Filament and Electron Beam	Spin-on-glass (SOG)
Low Pressure CVD (LPCVD)	Electroless Plating	Radio Frequency (RF)	Molecular Beam Epitaxy (MBE)	Spin-on dielectric (SOD)
Plasma Assisted CVD: • Plasma Enhanced CVD (PECVD) • High Density Plasma CVD (HDPCVD)		DC Magnetron		
Vapor Phase Epitaxy (VPE) and Metal-organic CVD (MOCVD)		Ionized metal plasma (IMP)		

Adapted from F. Barlow III, A. Elshabini-Riad, and R. Brown, "Film Deposition Techniques and Processes," *Thin Film Technology Handbook,* eds. A. Elshabini-Riad and F. Barlow III (New York: McGraw-Hill), pp. 1–2.

This chapter reviews the dielectric thin films deposited with chemical vapor deposition (CVD), epitaxy, and spin-on-dielectric (SOD) methods. All metallization is discussed in Chapter 12, including chemical vapor deposition (CVD) for metals, sputtering, electroplating, and evaporation.

CVD is commonly used for depositing dielectric and metal films. Spin-on-dielectric (SOD) is used for applying liquid dielectric films followed by a high-temperature curing process. Sputtering, or PVD, is the most common method in wafer fabrication for applying metals such as aluminum. Electroplating, widely used in thin film deposition for magnetic recording heads in disk drives, has not been used in silicon wafer fabrication. It has recently become the most promising process for depositing copper metallization. Evaporation is the traditional method for applying a metal layer, but its poor gap-fill property led to its demise at the start of the VLSI era, when it was replaced by sputtering.

CHEMICAL VAPOR DEPOSITION

Chemical vapor deposition (CVD) is the process of depositing a solid film on the wafer surface through a chemical reaction of a gas mixture. The wafer surface or its vicinity is heated in order to provide additional energy to the system to drive the reactions. The essential aspects of CVD are:

1. Chemical action is involved, either through chemical reaction or by thermal decomposition (referred to as *pyrolysis*).
2. All material for the thin film is supplied by an external source.
3. The reactants in a CVD process must start out in the vapor phase (as a gas).

CVD deposition by use of a chemical reaction occurs when chemical compounds are mixed and then reacted in a deposition chamber, referred to as a *reactor.* The atoms or molecules deposit on the wafer surface and form the film.



Chemical Vapor Deposition Tool
(Photo courtesy of Novellus Systems, Inc.)

CVD Chemical Processes

There are five basic chemical reactions that can be used in CVD:[13]

1. **Pyrolosis:** a compound dissociates (breaks bonds, or decomposes) with the application of heat, usually without oxygen.
2. **Photolysis:** a compound dissociates with the application of radiant energy that breaks bonds.
3. **Reduction:** a chemical reaction occurs by reacting a molecule with hydrogen.
4. **Oxidation:** a chemical reaction of an atom or molecule with oxygen.
5. **Reduction-oxidation (redox):** a combination of reactions 3 and 4 with the formation of two new compounds.

Among these five general types of reactions, there are many specific CVD reactions used to deposit films on a wafer substrate. The choice of a particular reaction is usually defined by parameters such as deposition temperature (which must be acceptable for the wafer materials), the film properties, and manufacturing issues. An example of a specific CVD reaction is the deposition of a silicon dioxide film by an oxidation reaction of silane with oxygen. This reaction produces silicon dioxide that is deposited on the heated wafer surface, with a by-product of hydrogen.

$$\underset{\textit{silane}}{SiH_4} + \underset{\textit{oxygen}}{O_2} \xrightarrow{\text{(heat)}} \underset{\textit{silicon dioxide}}{SiO_2} + \underset{\textit{hydrogen}}{2H_2}$$

CVD Reaction

The CVD chemical reaction that deposits the solid film takes place on (or very close to) the wafer surface. This is a *heterogeneous reaction* (also referred to as *surface catalyzed*). Some reactions also occur in the gas phase above the wafer surface, which is termed a *homogeneous reaction*. Homogeneous reactions are undesirable because they form gas-phase clusters of the depositing material, which results in poorly adhering, low-density films with higher defects.[14] In CVD chemical reactions, heterogeneous reactions at the wafer surface are favored for the production of high-quality films.

CVD Reaction Steps ■ The fundamental CVD reaction has eight major steps that explain the reaction mechanism. The steps are summarized in the following list and are shown in Figure 11.8:[15]

1. **Gas transport to deposition zone:** Mass transport of gas in the main gas flow region from the reactor inlet to the deposition zone of the wafer.
2. **Formation of film precursors:** Gas-phase reactions leading to the formation of the film precursors (initial atoms and molecules that will constitute the film) and by-products.
3. **Film precursors at wafer:** Mass transport of the film precursors to the wafer growth surface.
4. **Precursor adsorption:** Adsorption (binding) of film precursors to the surface.
5. **Precursor diffusion:** Surface diffusion of film precursors to the film growth sites.
6. **Surface reactions:** Surface chemical reactions leading to film deposition and by-products.
7. **By-product removal from surface:** Desorption (removal) of the by-products of the surface reactions.
8. **By-product removal from reactor:** Mass transport of the by-products in the bulk gas-flow region away from the deposition zone and towards the reactor exit.

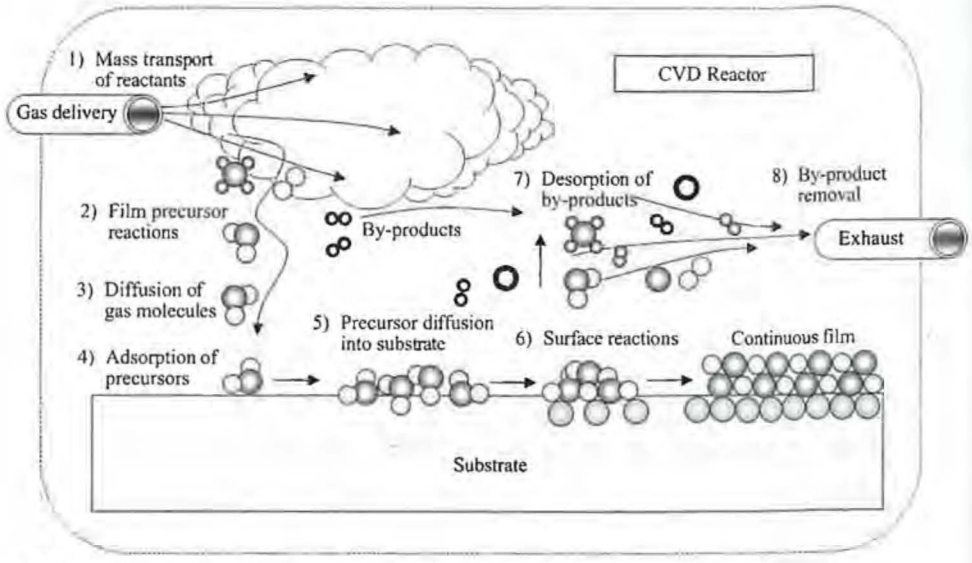


FIGURE 11.8 Schematic of CVD Transport and Reaction Steps

Adsorption is the chemical binding that occurs during deposition, causing the gaseous atoms and molecules to chemically attach to the solid wafer surface. *Desorption* is the removal or release of by-products from the wafer surface reactions. In chemical reactions, *species* describes a particular chemical substance that is an atom, ion, or molecule. In gas-phase reactions, there are often intermediate reactions called *precursors* that form a gas species that does not contain the original gas components. In CVD, gas precursors are transported to the wafer surface for adsorption and reaction. For example, for the following three reactions, the first gas-phase reaction shows that when

silane decomposes, a silicon hydride precursor is produced. This precursor then reacts with silane to form disilane. During the intermediate CVD reaction, the silicon hydride is adsorbed onto the wafer surface along with silane. Disilane then decomposes to form the final silicon solid-film product.

1)	SiH_4 (gas) *silane*	→	SiH_2 (gas) *silicon hydride*	+	H_2 (gas) *hydrogen*	(pyrolysis)
2)	SiH_4 (gas) *silane*	+	SiH_2 (gas) *silicon hydride*	→	Si_2H_6 (gas) *disilane*	(Reactive intermediate formation)
3)	Si_2H_6 (gas) *disilane*	→	2Si (solid) *solid film product*	+	$3H_2$ (gas) *by-product*	(Final product formation)

Rate Limiting Step ■ The length of time it takes for the CVD reaction to occur is important for productivity in manufacturing. The surface reaction rate increases with increasing temperature. Since CVD reaction steps are sequential, the slowest step defines the bottleneck in the process. In other words, the step that occurs at the slowest rate will determine the rate of deposition.[16]

The rate of a CVD reaction cannot proceed more rapidly than the mass-transport rate at which reactant gases are supplied from the main gas stream to the wafer substrate. This is true no matter how high the temperature is increased. This situation is referred to as a *mass-transport limited* deposition process. A mass-transport limited process is only weakly dependent on temperature.[17] This means that regardless of the temperature, there is insufficient reactant gas being supplied to the wafer surface to speed up the reaction. Because of this, a high-temperature, higher pressure CVD process that wants to proceed rapidly is usually mass-transport limited—it cannot supply enough reactant gas to the substrate because of diffusion or physical limitations.

At lower reaction temperatures and pressure, the surface reaction rate is reduced because there is less energy available to drive the surface reaction. Eventually the arrival rate of reactants will exceed the rate at which they are consumed by the chemical reaction process at the wafer surface. In this case, the deposition rate is *reaction-rate limited.*[18] This condition is similar to pouring too much liquid through a funnel—the liquid will not flow faster than the funnel permits. Even though more reactant gas is supplied, the reaction will not speed up because the low temperature provides insufficient energy. A reaction-rate limited CVD process is also referred to as *kinetically controlled,* meaning the diffusivity of the reactants is not as critical as the kinetic energy of the reactants at the surface. For reaction-rate limited processes, it is important to maintain a uniform temperature in order to achieve a uniform deposition rate across the wafer surface.

CVD Gas-Flow Dynamics ■ The gas-flow dynamics for CVD are important for uniform film deposition. Gas flow refers to the physical transport of reactant gases to the CVD sites on the wafer (see Figure 11.9 on page 268). At the molecular level, this requires having a sufficient number of molecules at the right place and the right time. This condition is necessary for a stoichiometric reaction to occur between the reactants and products.

The principal factors for CVD gas flow are the mass transport of the reactant gases from the main gas stream to the wafer surface and the chemical reaction rate at the surface. It is assumed that the dominant transfer mechanism from the gas phase to the surface is diffusion.[19] Considering the gas flow right at the wafer surface during a CVD reaction process, there is zero or near-zero gas flow. This condition creates a *boundary layer* of gas flow that increases from the zero gas-flow velocity at the wafer surface (due to frictional forces) to some typical gas flow farther from the surface.[20] These dynamics are shown in Figure 11.10 on page 268. The gas flow farther from the surface reaches some average gas-flow velocity that represents the average velocity of the main gas stream in the CVD reactor. If the boundary layer is narrow, then it can be treated as not moving at all near the wafer surface. In this case, it is referred to as a *stagnant layer.* The size of the stagnant layer will influence the design of the different types of CVD reactors considered later in this chapter.

Pressure in CVD ■ If a CVD reaction occurs at low pressure, then the diffusivity of the gas species increases significantly through the boundary layer to reach the surface. This diffusivity

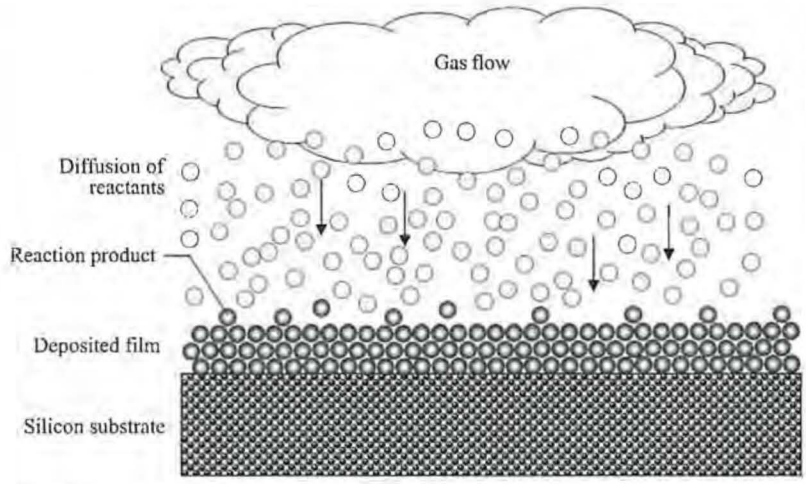


FIGURE 11.9 Gas Flow in CVD

increases the transport of the reactants to the substrate surface (and also increases the removal of by-products away from the substrate). The net effect of lower pressure in a CVD reactor is that the reactants reach the surface more quickly. In this case, the rate-limiting step becomes the surface reaction. At lower pressures, the CVD process is reaction-rate limited. This means that wafers can be stacked vertically and at very close spacing in the reactor since the transport of the reactants from the gas stream to the wafer is not limiting the process.

Doping During CVD ■ The introduction of dopants into SiO_2 during CVD deposition is desirable because it leads to important benefits for wafer fabrication. For instance, the introduction of phosphine (PH_3) to the gas stream during silicon dioxide deposition will lead to the formation of *phosphosilicate glass* (*PSG*). The chemical reaction is:

$$\underset{\textit{silane}}{SiH_4\,(\text{gas})} + \underset{\textit{phosphine}}{2PH_3\,(\text{gas})} + \underset{\textit{oxygen}}{O_2\,(\text{gas})} \rightarrow \underset{\textit{silicon dioxide}}{SiO_2\,(\text{solid})} + \underset{\textit{phosphorus}}{2P\,(\text{solid})} + \underset{\textit{hydrogen}}{5H_2\,(\text{gas})}$$

Within the glass, the phosphorous is in the form of a phosphorus pentoxide (P_2O_5), making the glass a dual compound as it codeposits with silicon dioxide. The P_2O_5 content in films is limited to about 4% by weight for films that are left permanently on the wafer because PSG becomes increasingly hygroscopic (water-absorbing).

PSG can be deposited at 600 to 650°C using high-density plasma CVD (HDPCVD) and has recently become popular for the first interlayer dielectric (ILD-1) layer because of its low deposition temperature, relatively planar surface, and excellent gap-fill characteristics. Incorporation of P_2O_5 into silicon dioxide films leads to a reduction in the film stress, which improves the film integrity. The dopant increases the moisture-barrier property of glass. Another benefit is that PSG layers are effective in serving as a getter to immobilize ionic contaminants. The ions become attached to the phosphorus and are thus restrained from diffusing through the film to the wafer surface.

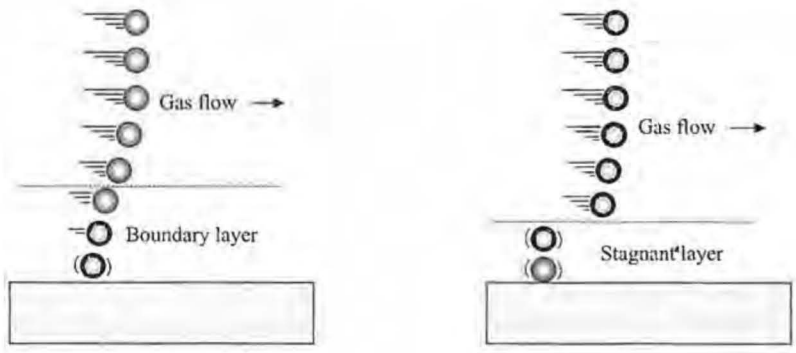


FIGURE 11.10 Gas-Flow Dynamics at the Wafer Surface

Borosilicate Glass. If diborane (B_2H_6) is used instead of phosphine (PH_3), then the result is *borosilicate glass* (*BSG*). BSG requires reflow at a high temperature (e.g., 1000°C) to smooth out sharp steps in the wafer surface and densify the film. However, a high-temperature reflow is undesirable for the wafer thermal budget. BSG also has the disadvantage of not being a good barrier to mobile ionic contaminants (MICs).[21]

Borophosphosilicate Glass. Another method for doping oxide is to incorporate about 2 to 6 % weight each of boric oxide (B_2O_3) and phosphorus pentoxide (P_2O_5) into the silicon dioxide deposition to form *borophosphosilicate glass* (*BPSG*). To achieve a dense oxide with good step coverage after deposition, the oxide is reflowed at a high temperature until it softens and flows. For BPSG, the reflow temperature is 800 to 1000°C for one hour. Reflow also improves its gettering characteristics to block mobile ionic contaminants (MICs). BPSG was commonly deposited on the wafer as the ILD-1 but has been recently replaced by PSG deposited by HDPCVD to reduce the thermal budget.[22]

High temperatures adversely affect the wafer thermal budget in sub-0.25 μm devices. For example, refractory metals (e.g., titaniun and cobalt) used to reduce contact resistance at junctions undergo material transformations at about 600°C that increase their contact resistance to unacceptable levels. In addition, the oxide planarity achieved by a high-temperature reflow is not sufficient for reduced depth of field requirements in ULSI photolithography. For this reason, reflow of doped oxide for planarity and gap fill has been largely replaced by high-density plasma CVD to achieve a stable film with good gap fill, followed by chemical mechanical planarization (CMP) to attain a flat surface (see Chapter 18).

Fluorosilicate Glass. *Fluorosilicate glass,* or *FSG,* is a fluorinated oxide that is being investigated as a first generation low-*k* dielectric for ILD deposition on 0.18 μm generation devices. By adding fluorine to silicon dioxide, there is a decrease in the dielectric constant of the material from about 3.9 for SiO_2 to about 3.5 for FSG.

To form an FSG film, silicon tetrafluoride (SiF_4) is added to the silane (SiH_4) and O_2 gases during the CVD reaction. A potential problem with using FSG is that the fluorine bonds are not always stable and can lead to corrosion, limiting the fluorine content to about 6%. If fluorine ions encounter moisture, hydrofluoric acid (HF), which etches oxide, is created. A method to avoid this problem is to remove weakly bonded fluorine atoms through the introduction of hydrogen during the deposition reaction.[23]

Oxide Versus Silicon Doping. Note that the doping of silicon dioxide is not the same as doping of silicon. When silicon is doped, there is a donation or acceptance of electrons between the dopant and silicon, within a single crystal lattice structure. Deposited oxide is an amorphous crystal structure and the dopants do not act as donors or acceptors of electrons. Doping is done to modify a physical characteristic of SiO_2, such as improving its ability to getter mobile ions.

CVD DEPOSITION SYSTEMS

There are different types of production systems for the deposition of dielectric and metal film layers. Some systems use large batch processing to perform CVD deposition on a large quantity of wafers at one time. However, the most advanced deposition systems currently in use for wafer manufacturing employ single-wafer processing in a cluster tool approach.

Table A.3 in Appendix A summarizes different gases used for CVD reactions. An example of a CVD gas is pure silane, which is used to deposit Si or SiO_2 in CVD systems. Silane reacts with air to form solid particles, causing particle contamination with the silane gas lines and leading to contaminated pipes or combustion. The gas line piping must be carefully installed to avoid any leaks. Many of the gases used in CVD film deposition are toxic. These gases are classified in Table A.3 based on four different safety hazards: pyrophoric (ignites spontaneously in air at or below 54.5°C), poisonous, corrosive, and dangerous combinations of gases, such as silane with hydrogen.

CVD Equipment Design

CVD has a range of equipment reactor designs, with each producing slightly different types of film quality. CVD reactors are broadly categorized based on the reaction chamber pressure regime used during operation: atmospheric-pressure CVD (APCVD) reactors and reduced-pressure reactors. The reduced-pressure CVD reactors have two general types. First, there are low-pressure CVD (LPCVD) reactors where the energy input is thermal. Second, there are plasma-assisted CVD reactors, either plasma-enhanced CVD (PECVD) or high-density plasma CVD (HDPCVD), where the energy is partially supplied by a plasma as well as thermally. Figure 11.11 depicts the different CVD reactor types.

CVD Reactor Types	Atmospheric	Low-pressure	Batch	Single-wafer
Hot-wall	✓	✓	✓	
Cold-wall	✓	✓	✓	✓
Continuous motion	✓		✓	
Epitaxial	✓		✓	
Plenum	✓		✓	
Nozzle	✓		✓	
Barrel	✓		✓	
Cold-wall planar		✓	✓	✓
Plasma-assisted		✓	✓	✓
Vertical-flow Isothermal		✓	✓	✓

FIGURE 11.11 CVD Reactor Types

CVD Reactor Heating ■ A major distinction in CVD reactors is whether they are hot-wall or cold-wall reactors. A *hot-wall reactor* employs a heating method that heats not only the wafer but also the wafer holder (referred to as a *susceptor*) and the walls of the reactor. Hot-wall reactors have film-forming reactions on both the reactor chamber walls and substrate, requiring frequent cleaning or in situ cleaning to minimize particle contamination. A resistance heater surrounding the reactor tube is an example of a hot-wall reactor. A *cold-wall reactor* heats only the wafers and susceptor, which is where film is deposited. The walls of the reactor are cold and therefore do not have sufficient energy to allow a deposition reaction to occur. RF induction heating or infrared lamps mounted in the reactor are examples of this type of reactor. Localized heating at the wafer minimizes particle formation in the reactor.

CVD Reactor Configuration ■ The geometry of the reactor design depends closely on the pressure attained during the deposition process. Atmospheric-pressure reactors operate in the mass-transport limited region, so they must be designed so that an equal amount of reactant gases are delivered to each wafer. To achieve this condition, wafers are usually laid flat on a horizontal surface. A drawback to this approach is that wafers are susceptible to contamination from falling particles.

Low-pressure reactors (LPCVD) are reaction-rate limited. This means that they can be vertically stacked at close spacing with a large number of wafers per run, since adequate reactant gas is always supplied to the wafer surface. Quartz wafer holders (boats) hold up to 200 wafers. At the same time, LPCVD reactors must have precise temperature control because of their limitation from the reaction rate.

CVD Reactor Summary ■ The different types of CVD processes and their principal characteristics are shown in Table 11.2.[24]

TABLE 11.2 Types of CVD Reactors and Principal Characteristics

Process	Advantages	Disadvantages	Applications
APCVD (Atmospheric Pressure CVD)	Simple reactor, fast deposition, and low temperature.	Poor step coverage, particle contamination, and low throughput.	Low-temperature oxides (both doped and undoped).
LPCVD (Low Pressure CVD)	Excellent purity and uniformity, conformal step coverage, and large wafer capacity.	High temperature, low deposition rate, more maintenance intensive, and requires vacuum system.	High-temperature oxides (both doped and undoped), silicon nitride, polysilicon, W, and WSi_2.
Plasma-Assisted CVD: • Plasma-Enhanced CVD (PECVD) • High-Density Plasma CVD (HDPCVD)	Low temperature, fast deposition, good step coverage, and good gap fill.	Requires RF system, higher cost, stress is much higher with a tensile component, and chemical (e.g., H_2) and particle contamination.	High aspect ratio gap fill, low-temperature oxides over metals, ILD-1, ILD, copper seed layer for dual damascene, and passivation (nitride).

APCVD (Atmospheric Pressure CVD)

The first type of chemical vapor deposition used in the semiconductor industry is *atmospheric pressure CVD (APCVD)*.[25] As previously discussed, APCVD generally operates in the mass-transport limited regime. At any given time, there may not be sufficient gas molecules present at the wafer surface for a reaction to occur. Therefore, the reactor must be designed to have optimum reactant gas flow to every wafer in the system. The basic system design should never permit the reaction to slow down because insufficient reactant gas is available. Since the reactor is at atmospheric pressure, the reactor design can be simple and allows for high deposition rates.

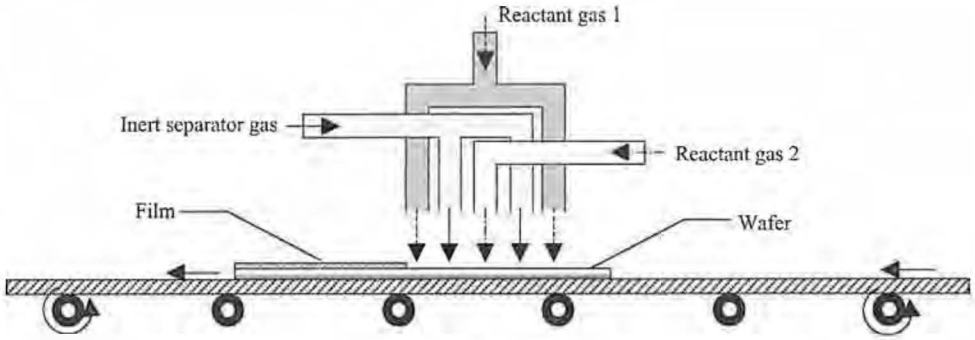
Two different types of continuous-processing APCVD systems are shown in Figure 11.12 on page 272. These equipment designs use a belt or conveyor to carry the wafer samples through the reactor gases, which flow through the center of the reactor.

Continuous-processing APCVD systems have high equipment throughput, good uniformity, and the capability to process large-diameter wafers. APCVD systems do have problems with high gas consumption and often need frequent reactor cleaning. Since film deposition also takes place on the conveyor as well as the wafer, the belt transport system must be cleaned (sometimes it is in cleaned in situ, or during use). APCVD deposited films often exhibit poor step coverage.

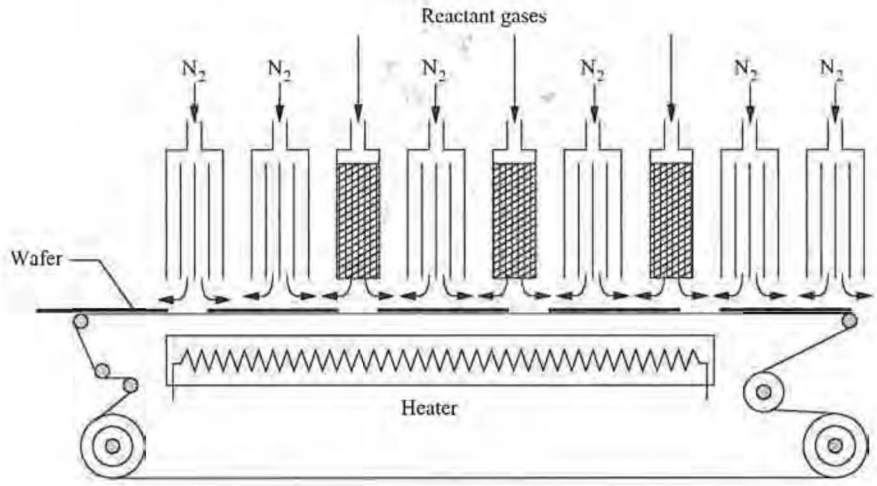
Silicon Dioxide ■ The most common use of APCVD is in the deposition of silicon dioxide (SiO_2) and doped oxides (e.g., PSG, BPSG, and FSG, as discussed earlier in this chapter). These films have been used traditionally as an interlayer dielectric (ILD), as a protective overcoat, or to planarize (smoothen) a nonuniform surface.

SiO_2 Deposition With Silane. SiO_2 is deposited by oxidizing *silane* (SiH_4) with oxygen. Pure silane is a highly pyrophoric, unstable gas that burns on exposure to air. For this reason, it is commonly supplied in a low dilution (typically 2 to 10% by volume) in argon or nitrogen in order to make it safer to handle. This reaction can be done at a low temperature of 450 to 500°C, which is an advantage for depositing SiO_2 on the aluminum metal lines as an ILD.[26] However, due to the small mean free path and poor surface migration through the boundary layer, this method has poor step coverage and poor gap-fill characteristics. This makes it unacceptable for critical ULSI applications.

SiO_2 Deposition With TEOS-Ozone. A common APCVD application is to deposit oxide by reacting *TEOS*, which is tetraethylorthosilicate ($Si(C_2H_5O)_4$) or tetraethoxysilane, with ozone (O_3). TEOS is an organic liquid precursor. It usually uses a carrier gas, typically nitrogen, bubbled through it for delivery of the TEOS gas mixture to the reactor. There are also flow controllers for delivering the TEOS source in liquid state to the reactor. Ozone is a triatomic oxygen molecule that is much more reactive than oxygen; therefore, the process can be done at low temperatures (e.g., 400°C) without plasma. Because the decomposition of TEOS is induced by O_3 without a plasma, the reaction takes place at atmospheric pressure (APCVD) of 760 torr or subatmospheric pressure (SACVD) at about 600 torr. There appears to be no significant difference between APCVD and



(a) Gas-injection type



(b) Plenum type

FIGURE 11.12 Continuous-Processing APCVD Reactors

SACVD.[27] The deposited oxide film has improved profiles over steps, is conformal, and has excellent electrical characteristics as a dielectric.[28] The reaction equation between TEOS and O_3 to obtain an oxide is:

$$\underset{\textit{TEOS}}{Si(C_2H_5O)_4} + \underset{\textit{ozone}}{8O_3} \rightarrow \underset{\textit{silicon dioxide}}{SiO_2} + \underset{\textit{water}}{10H_2O} + \underset{\textit{carbon dioxide}}{8\,CO_2}$$

An APCVD TEOS-O_3 as-deposited SiO_2 film is porous and often requires a reflow step to remove moisture as well as densify the film. This reflow adds a process step and reduces the thermal budget.[29] Doping uniformity is also a concern, as this can lead to problems for nonuniform removal rates during chemical mechanical planarization. The primary advantage of APCVD TEOS-O_3 is the improved step coverage for high-aspect ratio gaps for applications such as shallow trench isolation (see Figure 11.13). Another advantage to APCVD TEOS-O_3 is that it is just a basic thermal CVD process to deposit oxide, which could avoid wafer surface damage and wafer corner damage at steps. This type of damage is possible from high-density plasma CVD (discussed later in this chapter). An aspect of TEOS-O_3 films is that they are usually deposited in combination with other oxide film layers (e.g., PECVD oxide) for reasons such as reducing the TEOS-O_3 tensile stress on a thick film or to reduce sensitivity with the underlying material.[30]

Doped Oxides. APCVD oxides are usually doped with chemicals such as phosphorus and boron (discussed earlier in this chapter). If SiO_2 is undoped, it is referred to as *undoped silicate glass* (*USG*) or *undoped oxide* (*UDOX*). Phosphorus doped oxide is phosphosilicate glass (PSG). In the traditional deposition process, a high-temperature reflow (as high as 950°C for 15 to 30 minutes) heats and softens the doped oxide, causing it to planarize the surface (see Figure 11.14).

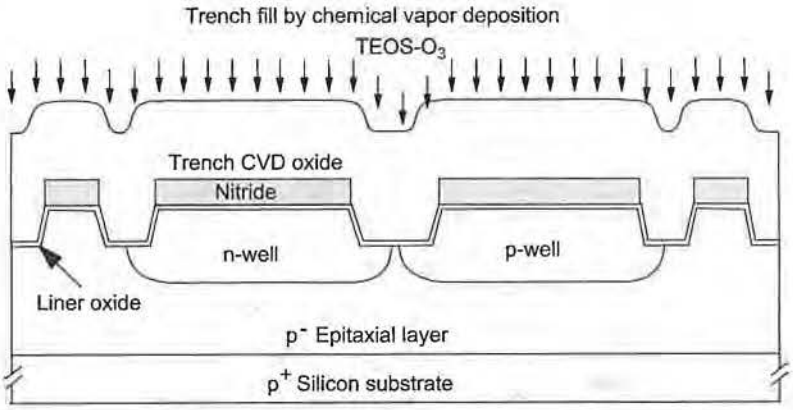


FIGURE 11.13 Improved Step Coverage of APCVD TEOS-O_3

Silane-based borophosphosilicate, or BPSG films, are deposited at low temperatures (400 to 450°C) and then immediately densified and stabilized at about 800°C for one hour. A smoother surface makes it easier to deposit and pattern the next film. Note that for the ULSI device technology, reflow has been replaced with chemical mechanical planarization (CMP) to planarize the surface. CMP is discussed in Chapter 18.

LPCVD (Low Pressure CVD)

Low pressure CVD (*LPCVD*) systems are more common now than APCVD because of their lower cost, higher production throughput, and superior film properties. LPCVD operates at a medium vacuum (about 0.1 to 5 torr), and employs temperatures between 300 and 900°C.[31] Conventional oxidation type furnaces (horizontal or vertical) and multichamber cluster tools can be used for LPCVD processing.

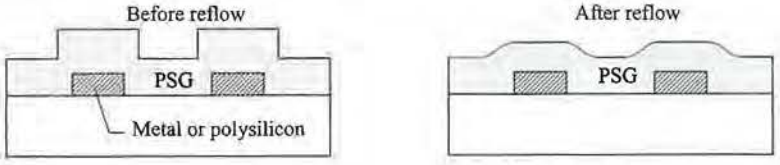


FIGURE 11.14 Planarized Surface after Reflow of PSG

LPCVD reactors typically operate in the reaction-rate limited regime. In this reduced-pressure regime, the diffusivity of the reactant gas molecules increases so that the mass-transfer of the gas to the wafer no longer limits the rate of the reaction. Because of this transfer state, the gas-flow conditions inside the reactor are not important, permitting the reactor design to be optimized for high wafer capacity (e.g., wafers can be closely spaced). Films are uniformly deposited on a large number of wafer surfaces as long as the temperature is tightly controlled.

The boundary layer in a LPCVD reactor is different from APCVD because it extends farther from the wafer surface due to the low-pressure condition (see Figure 11.15 on page 274). The boundary layer has a low molecular density, which permits incoming gas molecules to easily diffuse through this layer, exposing the wafer surface to more molecules than it can possibly consume. This condition explains why an LPCVD reactor operates in the reaction-rate limited regime. It is the reaction rate that is the limiting factor in the deposition rate, not the reactant supply. Furthermore, there are many collisions during LPCVD, so that material strikes the wafer in an undirected manner. This action is beneficial for conformal film coverage on high-aspect ratio steps and trenches. As a result, step coverage is usually good with LPCVD.[32]

The LPCVD reactor design favors the hot-wall reactor type so that uniform temperature control is achievable over a large operating length. A representative reaction chamber is shown in Figure 11.16 on page 274.

Since LPCVD reactors are often hot wall, particles deposit on the reactor wall. These deposits are minimized by reducing the partial pressure of the gas-phase reactants, which leads to fewer

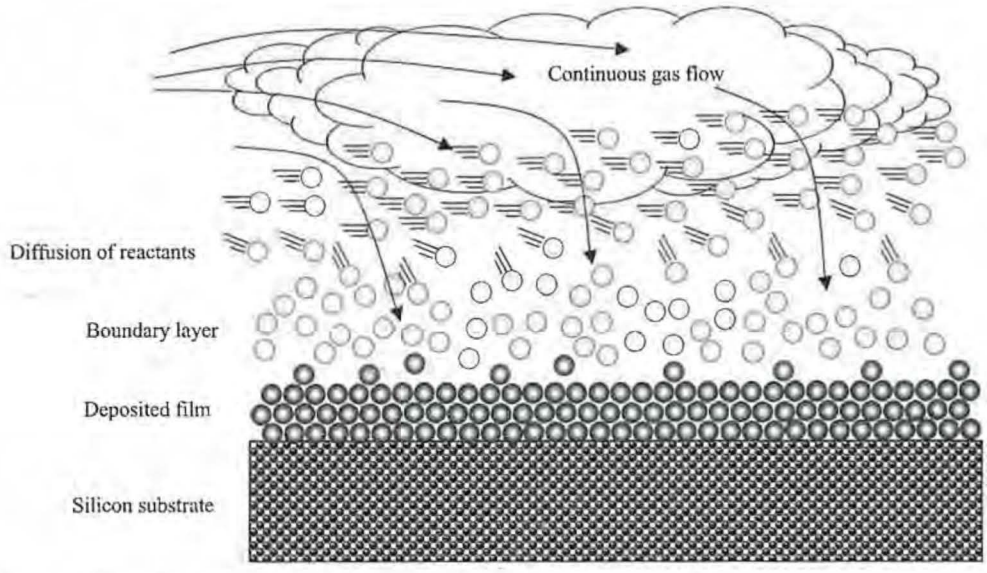


FIGURE 11.15 Boundary Layer at Wafer Surface

gas-phase reactions. For this reason, LPCVD reactors are usually operated at lower growth rates than APCVD systems.[33] Hot-wall reactors require periodic reaction chamber cleanup of particles by routine maintenance.

The traditional method of tube cleaning was to remove a dirty quartz tube, install a previously cleaned tube, and clean the dirty tube for future use. Cleaning involved manually rolling the tubes half-submerged in an acid bath such as aqueous HF. For production and safety reasons, an in situ clean is desirable. One in situ method is the use of plasma-generated fluorine gases that react with the solid residue in the reactor, forming volatile reaction products that are pumped from the system. Another in situ approach is to use chlorine trifluoride (ClF_3) with elevated temperature to activate a thermal clean. In situ tube cleaning for LPCVD reduces equipment downtime, lowers particle counts, and minimizes personnel exposure to chemicals.[34]

LPCVD reactors with a large number of wafers (e.g., 150 to 200 wafers) experience reactant depletion as gases are transported along the reaction chamber. This depletion leads to a reduction in growth rate. Adjusting the reactor temperature so that it increases slightly from inlet to outlet (typically by 25 to 50°C) compensates for this temperature nonuniformity.

Silicon Dioxide ■ There are numerous applications for LPCVD oxides (doped and undoped) in ULSI multilevel metallization. LPCVD oxides are used for interlayer dielectric (ILD), shallow trench isolation oxide fill, and sidewall spacers.

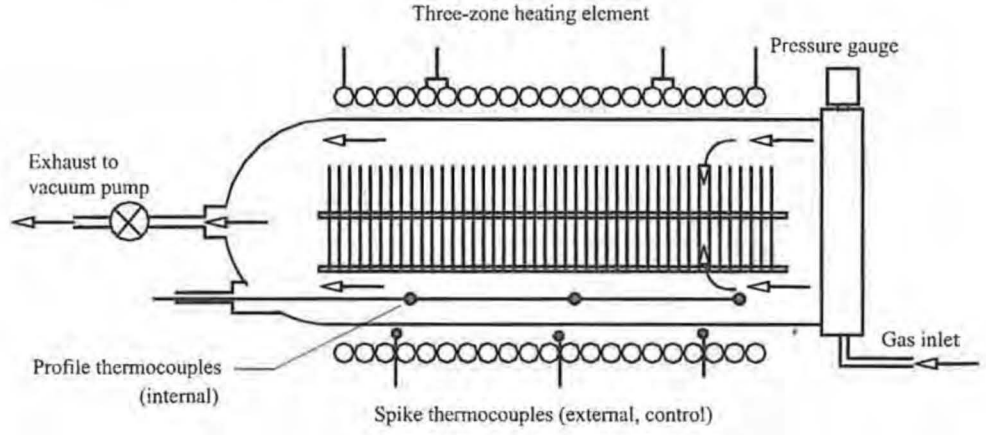


FIGURE 11.16 LPCVD Reaction Chamber

SiO_2 With TEOS. A common LPCVD method for depositing silicon dioxide is the pyrolosis (decomposition) of TEOS, with or without oxygen, at low pressure and at a temperature between 650 to 750°C. This method is sometimes referred to as LPTEOS, for low-pressure TEOS. LPTEOS yields very good oxide conformality due to rapid surface diffusion of gas molecules. A liquid TEOS source is used by bubbling a carrier gas through it (e.g., N_2, O_2, or He). The liquid source is heated by its own independent temperature source. The concentration of the liquid source vapor entering the reactor is controlled by the carrier gas-flow rate and liquid source temperature. A schematic of a typical TEOS deposition system is shown in Figure 11.17. The film growth rate for LPCVD oxides is significantly slower (100-150 Å/minute) than for APCVD films.[35]

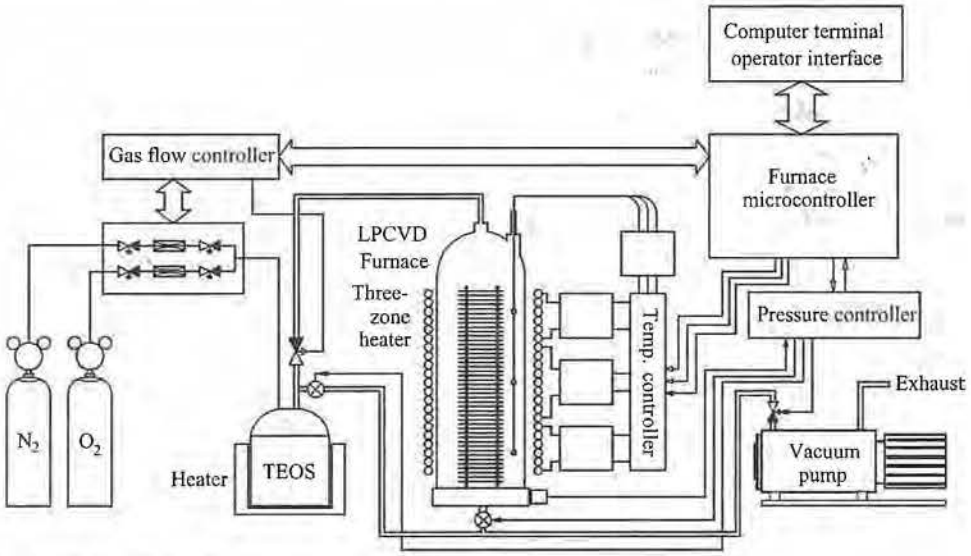


FIGURE 11.17 Oxide Deposition with TEOS LPCVD

SiO_2 With SiH_4. SiO_2 can also be deposited by LPCVD by oxidizing silane (SiH_4) at a relatively low temperature of about 450°C. Similar to APCVD oxide with SiH_4, this process has poor step coverage. A higher temperature deposition is done with dichlorosilane (SiH_2Cl_2 or DCS) and nitrous oxide (N_2O) at about 900°C to produce a good quality SiO_2 film. However, the high temperature is undesirable for the wafer thermal budget.

Silicon Nitride ■ *Silicon nitride (Si_3N_4)* is a film often used as the final wafer passivation layer because it provides good protection against the diffusion of impurities and moisture. It achieves excellent step coverage with high conformal coverage with LPCVD deposition. Silicon nitride is also used as a mask material (referred to as a hard mask), such as in the shallow trench isolation (STI) process. Silicon nitride has a high dielectric constant (i.e., a k value of 6.9, versus about 3.9 for CVD SiO_2), which makes it undesirable for the ILD dielectric due to the resultant high capacitance between conductor layers.

Reacting dichlorosilane ($SiCl_2H_2$) and ammonia (NH_3) in an LPCVD reactor produces silicon nitride at a reduced pressure and temperature between 700 and 800°C. The chemical reaction is:

$$\underset{\textit{dichlorosilane}}{3SiCl_2H_2\,(gas)} + \underset{\textit{ammonia}}{4NH_3(gas)} \rightarrow \underset{\textit{silicon nitride}}{Si_3N_4(solid)} + \underset{\textit{hydrogen chloride}}{6HCl\,(gas)} + \underset{\textit{hydrogen}}{6H_2(gas)}$$

The important variables that affect the properties of silicon nitride in an LPCVD process are total pressure, reactant concentrations, deposition temperature, and temperature gradients. For example, increasing the total pressure and partial pressure of dichlorosilane in the reaction chamber will increase the deposition rate.

Silicon nitride can also be produced in an APCVD process by reacting silane and ammonia, but better film uniformity and higher wafer throughput is achieved in the low-pressure process.[36] Deposited silicon nitride is an amorphous film that often contains large amounts of hydrogen. A high ammonia ratio and low deposition temperature will increase the hydrogen content.

Polysilicon ■ Polysilicon film (also referred to as *poly-si*, or *poly*) is commonly deposited using LPCVD. Recall that the term polysilicon means that the silicon is a polycrystal, with many small single-crystal regions separated by grain boundaries. The stress in thin polysilicon films is compressive.

Doped polysilicon serves as the gate electrode in MOS devices (see Figure 11.18). Key reasons for the use of doped polysilicon in the gate structure are:[37]

1. Ability to be doped to a specific resistivity.
2. Excellent interface characteristics with silicon dioxide.
3. Compatibility with subsequent high-temperature processing.
4. Higher reliability than possible metal electrodes (e.g., aluminum).
5. Ability to be deposited conformally over steep topography.
6. Allows for self-aligned gate process (see Chapter 12).

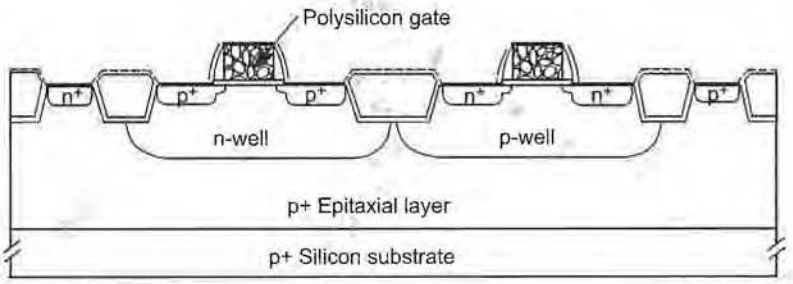


FIGURE 11.18 Doped Polysilicon as a Gate Electrode

Polysilicon is deposited in LPCVD by the pyrolysis (thermal decomposition) of silane at a temperature of 575 to 650°C. Low pressure reactors use either pure silane or 20 to 30% silane diluted with nitrogen, which is fed into the system at a pressure of 0.2 to 1.0 torr to fabricate polysilicon films. A practical deposition rate is about 100 to 200 Å/minute. The addition of diborane can enhance the polysilicon deposition rate because the diborane forms borane radicals, BH_3, which catalyze gas-phase reactions. The chemical reaction is:

$$\underset{\textit{silane}}{SiH_4\,(gas)} \rightarrow \underset{\textit{silicon}}{Si\,(solid)} + \underset{\textit{hydrogen}}{2H_2\,(gas)}$$

The polysilicon film is usually doped in situ during the deposition process by adding arsine (AH_3), phosphine (PH_3), or diborane (B_2H_6) to the gas mixture. An inert gas is often accompanied to improve film uniformity. Doping can be done after deposition by ion implantation (see Chapter 17). The resistivity of the polysilicon after doping is highly dependent on parameters such as deposition temperature, dopant concentration, and annealing temperature effects on grain size.

A refractory metal is deposited over the polysilicon gate to form a *polycide* or *silicide* structure (see Chapter 12). This action is taken to reduce electrical resistivity at the polysilicon interface with the other material (e.g., tungsten) that forms the electrical connection to other device components. Lightly doped polysilicon also serves as a resistor in memory cells, capacitors, and thin-film transistors.

Silicon Oxynitride ■ Silicon nitride films that contain oxygen are referred to as *silicon oxynitride* (SiO_xN_y) and combine the advantages of oxides and nitrides. Oxynitride films also have improved thermal stability, cracking resistance, and reduced film stress when compared to silicon nitride. In general, increased oxygen in oxynitride film also decreases the film's refractive index, which makes it less reflective and a useful antireflective layer in photolithography (see Chapter 14).[38] Another benefit of a silicon oxynitride film is the nitrogen in the film accumulates at the silicon interface to reduce the concentration of strained Si-O bonds, potentially reducing the creation of hot electrons (undesirable charge carriers) by as much as three orders of magnitude. An oxynitride layer at the Si/SiO_2 interface of thin gate oxides has been found to be beneficial for improving the device electrical performance.

Oxynitride films are formed by different techniques, including the oxidation of silicon nitride, the nitridation of SiO_2 with ammonia (NH_3), and the direct growth of SiO_xN_y using nitrous oxide as the oxidant species. One way of forming oxynitride films is by reacting silane (SiH_4) with nitrogen dioxide (N_2O) and NH_3. Nitride or oxynitride films are used frequently as an "etch stop" for selective etching of dielectric films.[39]

Plasma-Assisted CVD

The third major type of CVD equipment relies on plasma energy, in addition to thermal energy, to initiate and sustain the chemical reactions necessary for CVD. The advantages of using plasma during CVD are:

1. Lower processing temperature (250 to 450°C).
2. Excellent gap-fill for high aspect ratio gaps (with high-density plasma).
3. Good film adhesion to the wafer.
4. High deposition rates.
5. High film density due to low pinholes and voids.
6. Wide range of applications due to lower processing temperature.

Film Formation ■ The plasma-assisted CVD reaction necessary to form a film occurs when RF power is used to break up gas molecules in a vacuum. The frequency of the RF power depends on the application, with typical frequencies found at 40 kHz, 400 kHz, 13.56 MHz, and 2.45 GHz (microwave power). The molecular fragments (radicals) are chemically reactive species and readily bond to other atoms to form a film at the wafer surface (see Figure 11.19). Gaseous by-products are removed by the vacuum pumping system. The wafer is usually heated in order to assist the surface reactions and reduce the level of undesirable contaminants, such as hydrogen.

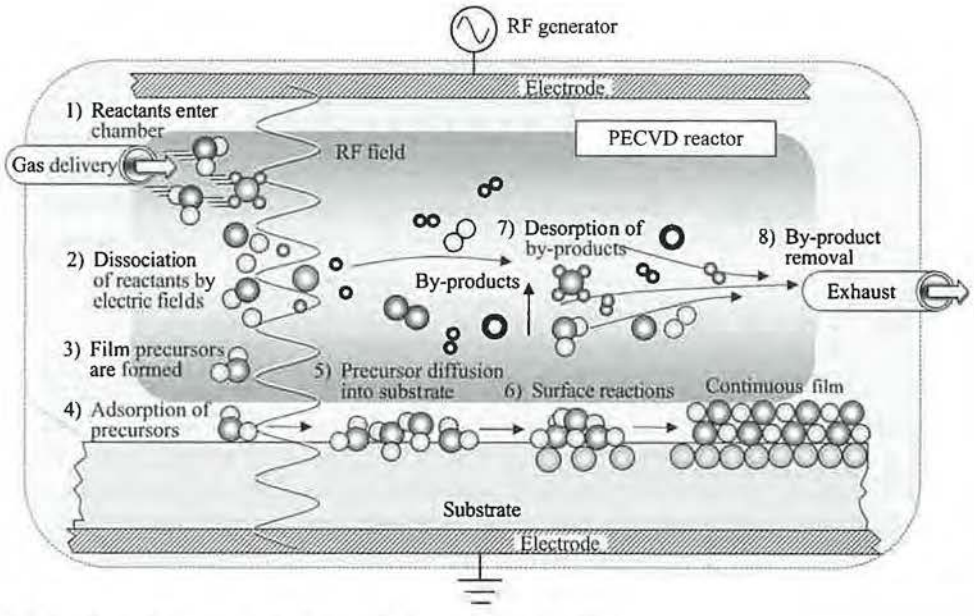


FIGURE 11.19 Film Formation During Plasma-Assisted CVD

The plasma-assisted CVD reactions at the wafer surface are very complex. The properties of plasma-deposited films depend on many variables, such as electrode configuration and separation, power level and frequency, gas composition, pressure and flow rate, and substrate temperature.[40] The essential aspect of these variables for production is embodied in the chamber design. The specific details of the intermediate reactions that occur in plasma glow discharge are not well understood. For these reasons, deposited films are often found to be not very stoichiometric. This means

that the deposited film will not necessarily have the same ratio of elements found in its nominal chemical formula.

There are two types of plasma processes used in CVD:

- Plasma-enhanced CVD (PECVD)
- High-density plasma CVD (HDPCVD)

Plasma-Enhanced CVD (PECVD) ■ The development of *plasma-enhanced CVD (PECVD)* uses plasma energy to create and sustain the CVD reaction. It is a natural follow-on to LPCVD since the system pressure for both types of CVD processes is comparable. The important difference is the much lower PECVD deposition temperature. For instance, silicon nitride (Si_3N_4) is deposited using LPCVD at 800 to 900°C, yet cannot be deposited over aluminum metallization because Al melts at 660°C. On the other hand, silicon nitride deposited with PECVD at a temperature of 350°C is suitable for this application.

PECVD is performed in a vacuum chamber between parallel conducting plates positioned several inches apart, typically with a variable gap for process optimization. A modern reactor is a multichamber cluster tool. The wafer (or wafers) is placed on the grounded bottom plate and RF power is applied to the top electrode. A plasma develops when the source gas is introduced through the gas manifold and the center of the electrodes. Exhaust gases are pumped out from the periphery of the bottom electrode. Sometimes the reactant gases are introduced at the periphery and pumped out at the center of the bottom electrode. A schematic of an overall PECVD system is shown in Figure 11.20.

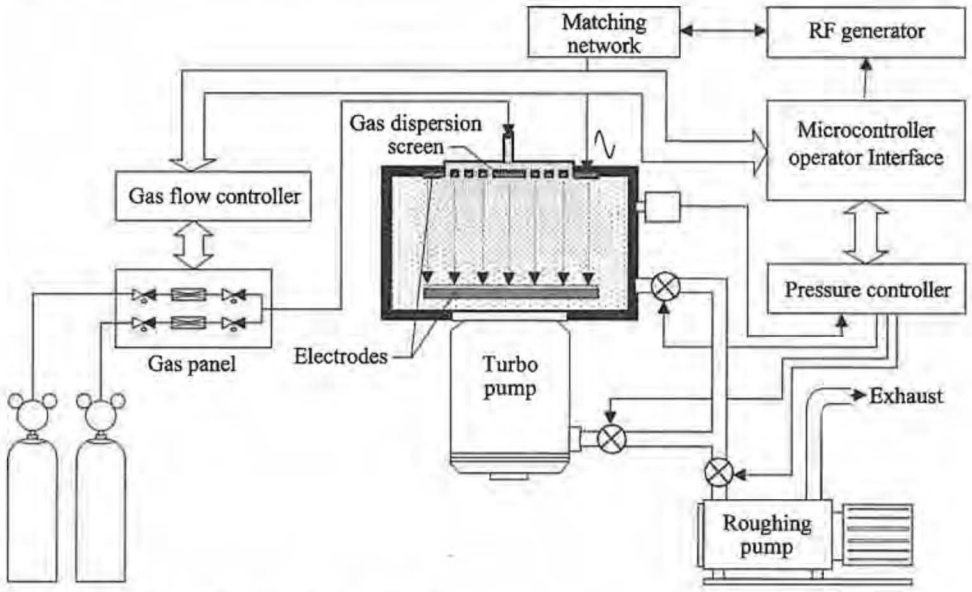


FIGURE 11.20 General Schematic of PECVD

A PECVD reactor is typically a cold-wall plasma reactor, with the wafer heated in its chuck while the remaining parts of the reactor are unheated. Deposition parameters must be controlled to ensure the temperature gradient does not affect the film thickness uniformity. Cold-wall reactors create fewer particles and require less downtime for cleaning. Deposition chambers often have in situ cleaning to reduce particles. With parallel-plate processing, there is the possibility that particles formed in the gas phase will fall on the wafer surface.

Silicon Dioxide PECVD. Oxide films with PECVD are usually formed by reacting silane (SiH_4) with either oxygen (O_2), nitrous oxide (N_2O), or carbon dioxide (CO_2) in a plasma. The processing temperature is about 350°C.[41] The oxide can be doped with boron or phosphorus to form BSG or PSG, respectively, or with both to deposit BPSG. PECVD PSG tends to be more crack resistant, conformal, and free of pinholes than APCVD PSG.

A plasma gas mixture of silane and oxygen is not normally used because oxygen reacts readily in the gas phase, which promotes particle generation and poor film quality (e.g., pinholes). The silane and nitrous oxide gas mixture produces more uniform films than through the use of an oxygen reactant. The reaction of silane with nitrous oxide to form silicon dioxide is:

$$\underset{\textit{silane}}{SiH_4\ (gas)} + \underset{\textit{nitrous oxide}}{2N_2O\ (gas)} \rightarrow \underset{\textit{silicon dioxide}}{SiO_2\ (solid)} + \underset{\textit{nitrogen}}{2N_2\ (gas)} + \underset{\textit{hydrogen}}{2H_2\ (gas)}$$

The silicon dioxide is nearly stoichiometric, although it does contain some hydrogen, with a small amount of nitrogen present in the film. Hydrogen can exist as a hydride (Si-H), silanol (Si-O-H), or as water (H-O-H). The presence of O-H groups is undesirable for MOS transistor electrical characteristics and must be minimized.[42]

Parallel-plate PECVD can also deposit SiO_2 using TEOS, and is referred to as *PETEOS*. However, PETEOS is not acceptable for filling narrow-spaced metal lines due to voids. PETEOS is combined with APCVD TEOS or high-density plasma CVD (HDPCVD) to attain conformal gap fill, followed by chemical mechanical planarization. PETEOS has a relatively high SiO_2 deposition rate, which makes it desirable for wafer throughput in integrated tools.

Silicon Nitride PECVD. *Silicon nitride PECVD* is a film used as a final passivation layer on the chip as scratch protection, and a moisture barrier and as a barrier to prevent sodium diffusion. It is also widely used as a mask material in shallow trench isolation (STI) and in self-aligned contact technology (see Chapter 12). The Si_3N_4 nitride film deposited by PECVD is not very stoichiometric, and is sometimes written as $Si_xN_yH_z$. This equation highlights its nonstoichiometric composition and identifies that the film contains hydrogen (usually 9 to 30%). Table 11.3 compares the properties of silicon nitride for LPCVD vs. PECVD.

TABLE 11.3 Properties of Silicon Nitride for LPCVD vs. PECVD

Property	LPCVD	PECVD
Deposition temperature (°C)	700 to 800	300 to 400
Composition	Si_3N_4	$Si_xN_yH_z$
Step coverage	Fair	Conformal
Stress at 23°C on silicon (dynes/cm^2)	$1.2 - 1.8 \times 10^{10}$ (tensile)	$1 - 8 \times 10^9$ (tensile or compressive)

PECVD nitride films are commonly produced from silane (SiH_4) and reacted with ammonia or nitrogen. The reaction equations are:

$$\underset{\textit{silane}}{SiH_4\ (gas)} + \underset{\textit{ammonia}}{NH_3\ (gas)} \rightarrow \underset{\textit{silicon nitride}}{Si_xN_yH_z\ (solid)} + \underset{\textit{hydrogen}}{H_2\ (gas)}$$

$$\underset{\textit{silane}}{SiH_4\ (gas)} + \underset{\textit{nitrogen}}{N_2\ (gas)} \rightarrow \underset{\textit{silicon nitride}}{Si_xN_yH_z\ (solid)} + \underset{\textit{hydrogen}}{H_2\ (gas)}$$

PECVD silicon nitride can have increased compressive film stress caused by ion bombardment during deposition that ruptures the Si-N or Si-H bonds. High compressive stress in a nitride layer can cause voids and cracks in the underlying aluminum metallization. There is usually substantial hydrogen content in the film. Hydrogen can reduce film stress, but it also degrades film properties.[43] When nitrogen is substituted for ammonia, the hydrogen content is reduced. However, ionization of nitrogen is difficult for plasma formation.

Silicon Oxynitride. Films of silicon oxynitride are deposited using PECVD by reacting Si_3N_4 with nitrous oxide (N_2O) at a temperature of 200 to 250°C.[44] Silicon oxynitride combines some properties from nitrides and oxides. It has good resistance to moisture and sodium penetration, with excellent mechanical, chemical, and electrical properties. These properties make silicon oxynitride suitable for topside passivation.

Gap Fill. A major limitation for PECVD in fine-geometry devices is gap fill. For gaps below 0.5 μm spacing (actual gap width), PECVD cannot fill the high aspect ratio gap without pinching off the top and leaving a void. A void in a dielectric material that is filling a gap is undesirable because of its effect on electrical performance and long-term reliability. For devices at the



High Density Plasma Deposition Chamber
(Photo courtesy of Applied Materials, Inc.)

0.25 μm technology node and below, HDPCVD has replaced PECVD because of its superior gap-fill properties.

It should be pointed out that other CVD methods can achieve fine-geometry gap-fill but have other limitations. For example, APCVD using TEOS oxide has good conformality and produces excellent gap fill. However, TEOS has different deposition characteristics depending on the underlying surface. One problem is that TEOS layers have dangling bonds that absorb moisture. To inhibit this condition, PECVD undercoat and overcoat layers are required. These layers add cost and also risk being removed during the subsequent chemical mechanical planarization (CMP).[45]

High-Density Plasma CVD (HDPCVD) ■ A recent development in plasma assisted CVD is *high-density plasma CVD* (*HDPCVD*). This deposition method became widely accepted in advanced wafer fabs in the mid-1990s. As its name implies, the plasma in HDPCVD is a high-density mixture of gases at low pressure that is directed toward the wafer surface in the reaction chamber. Its main benefit is that it can deposit films to fill high aspect ratio gaps with a deposition temperature range of 300 to 400°C. HDPCVD was initially developed for interlayer dielectric (ILD) applications, but is also being used for deposition in ILD-1, shallow trench isolation, etch-stop layers, and deposition of low-k dielectrics.[46]

The HDPCVD reaction involves a chemical reaction between two or more gas precursors. For the deposition of oxide ILD, oxygen (or ozone) is often used with a silicon containing gas such as silane or TEOS, along with argon. To form the high-density plasma, a source excites the gas mixture with RF or microwave power (2.45 GHz) and directs the plasma ions into a dense region above the wafer surface. There are different high-density plasma sources, such as electron cyclotron resonance (ECR), inductively coupled plasma (ICP), and Helicon. These plasma sources are explained in detail in Chapter 16.

Wafer Bias and Heat Load. An RF bias (often between 1,500 to 3,000 kW of RF power) is applied to the wafer, pulling energetic ions out of the plasma and directing them toward the wafer surface. Biasing the wafer gives directionality to the energetic ions of the plasma. The high-density plasma ion density is about 10^{11} to 10^{12} ions/cm^3 at low pressures (between 2 to 10 mtorr). This high plasma density, in conjunction with directionality from wafer biasing, is an important reason for HDPCVD's ability to deposit films into narrow gaps with high-aspect ratio geometries of 3:1 to 4:1 and higher.

Much of the challenge for the use of high-density plasma is related not only to the performance of the plasma source but also to the details of the chamber design so that the technology

works in high-volume wafer fabrication.[47] A particular problem is that the high-density plasma will increase the thermal load to the wafer, since 2000W of RF bias can result in power density application of approximately 6 watts/cm^2 on the wafer surface. This condition leads to high wafer temperatures. However, the ILD must have process temperatures below 400°C to avoid harming the aluminum metallization; in addition, high heat loads cause thermal stress to the wafer.[48] This temperature limit requires cooling the wafer by applying a backside blanket of helium gas to the wafer through access ports in the electrostatic chuck (ESC). This action creates a thermal conductivity path between the wafer and the ESC, thus cooling the wafer and the chuck.

Simultaneous Deposition and Etching. An HDPCVD process uses a simultaneous deposition and etching action that is the basis for its ability to fill high-aspect ratio gaps with dielectric material without voids (see Figure 11.21). This is referred to as the *dep:etch (D:E) ratio,* which typically has a value of approximately 3:1 for HDPCVD.[49] Interpret this ratio as meaning the deposition rate (i.e., the rate material is deposited) is occurring three times faster than the etch rate. Increasing the ratio will increase deposition and therefore wafer throughput, but if the ratio is too high, then voids occur because the gap is not completely filled.

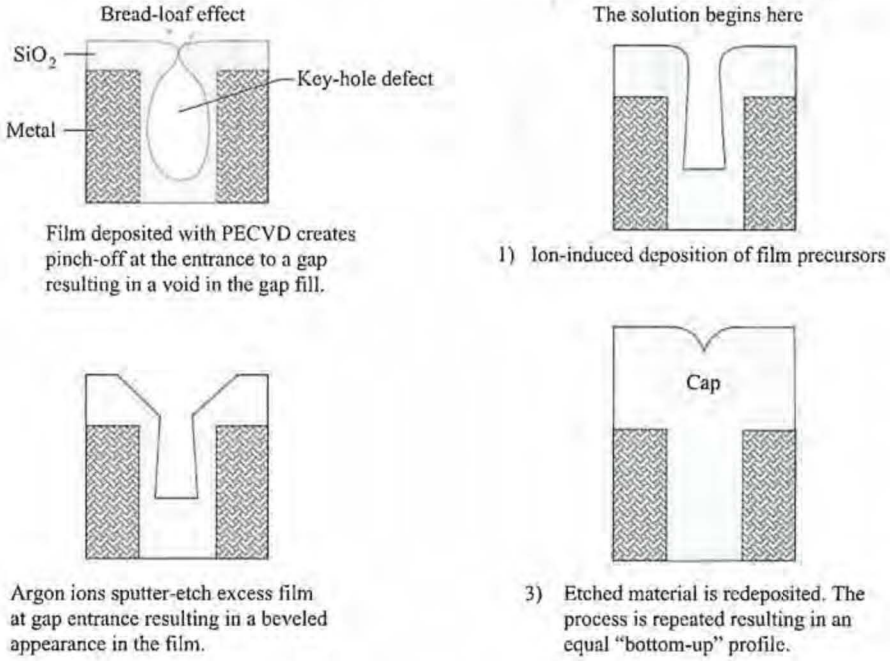


FIGURE 11.21 Dep-Etch-Dep Process

The surface reactions for the simultaneous deposition-etch include five steps, with the first three considered the dominant mechanisms:[50]

1. **Ion-induced deposition:** The ion is pulled from the plasma and deposited to produce the main gap-filling phenomena. It is driven by the kinetic energy of reactant ions breaking surface bonds to form reaction sites.
2. **Sputter etch:** Energetic argon and reactant ions attracted to the surface due to wafer bias will bombard the surface and etch (dislodge) atoms.
3. **Redeposition:** Atoms are dislodged from the bottom of the gap and usually redeposit on sidewalls. This is important for uniform thickness on sidewalls and the bottom of the gap.
4. **Hot-neutral CVD:** This is a minor contribution to the reaction where thermal energy drives some deposition.
5. **Reflection:** Another minor contribution of ions reflecting off sidewalls and then deposited.

Simultaneous deposition and etching is a beneficial by-product of the plasma directionality created in the oxygen and argon gas mixture in HDPCVD. For a silicon dioxide (SiO_2) deposition process, the oxygen reacts with silane (SiH_4) to form SiO_2, while argon acts to remove the deposited material away by sputtering (see Chapter 12 for an explanation of sputtering). Some factors that affect the dep:etch ratio are the ratio of the oxygen and argon gases, the chamber pressure, the ion energy, and the RF bias on the wafer.[51] Low pressure is important to reduce the mean free path, which reduces collisions and maintains good directionality of the plasma. For acceptable deposition rates and wafer throughput in HDPCVD, high gas-flow rates are required. As shown in Figure 11.22, the wafer often will sit directly on the throat of a high-speed turbo pump (e.g., 4,000 to 5,000 liters/sec pump speed for 300-mm diameter wafers).

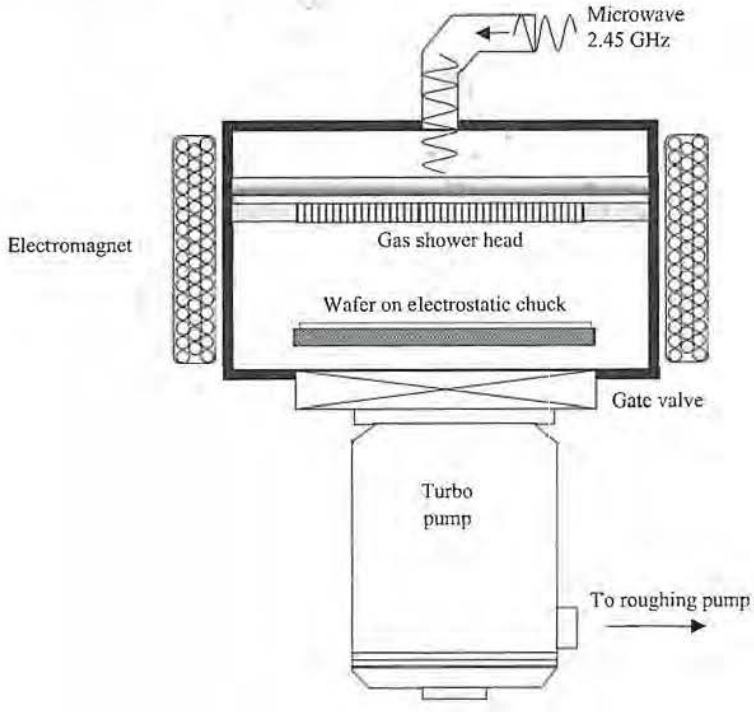


FIGURE 11.22 HDPCVD with Wafer at Throat of Turbo Pump

In practice, HDPCVD is sometimes used as the first step in a three-part process for dielectric gap fill.[52] High aspect ratio gaps (> 3:1) are filled with HDPCVD, followed by a regular density PECVD to deposit a cap film (see Figure 11.23). This capping film is then planarized by chemical mechanical planarization (see Chapter 18). Planarization maintains a smooth and constant oxide thickness on top of the metal conductor lines.

DIELECTRICS AND PERFORMANCE

The dielectric materials used in different film layers directly affect the performance of a microchip. Two important aspects of dielectrics are the dielectric constant and device isolation.

Dielectric Constant

The *dielectric constant* (k) of a nonconductive material represents its effectiveness at storing potential electrical energy under the influence of an electric field. In other words, this is the insulating material's ability to act like a capacitor. The lowest attainable k is 1.0 and represents air. A high k dielectric stores more electrical energy. The dielectric constant of thermal silicon dioxide (SiO_2) has a k value of about 3.9. The k value of a plasma-enhanced CVD (PECVD) oxide is about 4.1 to 4.3.



FIGURE 11.23 Three-Part Process for Dielectric Gap Fill

Doped SiO_2 has been traditionally the most common interlayer dielectric (ILD) material. Extensive research is underway to replace doped SiO_2 for the ILD with another dielectric material that has a lower dielectric constant (see Table 11.4).[53] Reducing the k value of the dielectric reduces capacitive losses between adjacent conductors because the dielectric stores less electric field and therefore takes less time to charge, allowing for an increase in speed performance of the metal conductors. A low-k dielectric material for the ILD becomes critical for smaller linewidths with less spacing between metal lines. As the metal linewidths decrease, the capacitive effects of the conductors and insulators increase, and using low-k materials compensates for this.

TABLE 11.4 Potential Low-k Materials for ILD of ULSI Interconnects

Potential Low-k Dielectric	Dielectric Constant (k)	Gap Fill (μm)	Cure Temp. (°C)	Remarks
FSG (silicon oxyfluoride, Si_xOF_y)	3.4 to 4.1	<0.35	No issue	FSG has almost the same k-value as SiO_2 and a reliability concern that fluorine will attack and corrode tantalum barrier metal.
HSQ (hydrogen silsesquioxane)	2.9	<0.10	350 to 450	Silicon-based resin polymer available in solution as FOx (Flowable Oxide) for spin-on coating application. May require surface passivation to reduce moisture absorption. Cure is done in nitrogen.
Nanoporous silica	1.3 to 2.5	<0.25	400	Inorganic material with tunable dielectric constant that relies on pore density. Increased porosity reduces mechanical integrity—porous material must withstand polishing, etching, and heat treatments without degradation.
Poly(arylene) ether (PAE)	2.6 to 2.8	<0.15	375 to 425	Spin-on aromatic polymer with excellent adhesion and ability to be polished with CMP.
a-CF (fluorinated amorphous carbon or FLAC)*	2.8	<0.18	250 to 350	Leading candidate for CVD deposition with high-density plasma CVD (HDPCVD) to produce film with good thermal stability and adhesion.
Parylene AF4 (aliphatic tetrafluorinated poly-p-xylylene)	2.5	<0.18	420 to 450	CVD film that meets adhesion and via resistance requirements with need to maintain gas delivery system at 200°C to control parylene precursor flow rate.

* P. Singer, "Technology News: Wafer Processing," *Semiconductor International* (October 1998): p. 44.

Chip Performance ■ An indicator of chip performance is the speed at which signals are transmitted. Continual die shrinks to achieve sub-0.25 μm technology nodes translate into reduced interconnect linewidths. This reduction leads to increased line resistance (R) for signals. Furthermore, reduced spacing between conductor lines creates more parasitic capacitance (C). The result is an increase in RC signal delay, which slows chip speed and lowers chip performance. This condition is a recent development due to sub-0.25 μm geometries and is often referred to as the *interconnect delay* (see Figure 11.24). In essence, reducing the interconnect dimensions results in more signal delay because of parasitic resistance and capacitance effects. This is the opposite of what occurs in transistors, where reducing gate length serves to reduce gate delay and increase transistor speed.[54]

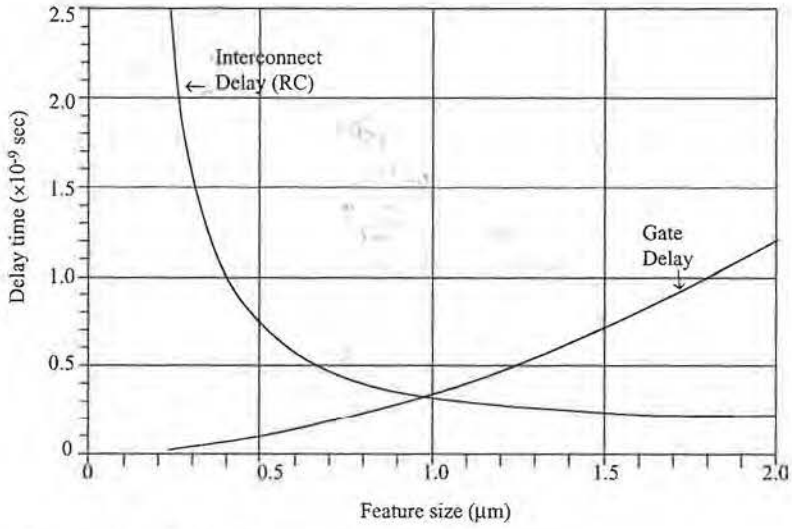


FIGURE 11.24 Interconnect Delay (RC) Versus Feature Size (μm)
(S. Murarka, "Low Dielectric Constant Materials for Interlayer Dielectric Applications, *Solid State Technology* (March 1996): p. 83.)

The line capacitance, C, is directly proportional to the *k*-value of the dielectric material. A low-*k* dielectric reduces the total interconnect capacitance of the chip (see Figure 11.25), reduces the RC signal delay, and improves chip performance. Lowering the total capacitance also decreases power consumption.[55] The use of a low-*k* dielectric material in conjunction with a low-resistance metal line provides the interconnect system with optimum performance for ULSI technology.

Low-*k* Dielectric Requirements ■ Table 11.5 outlines the typical requirements for a low-*k* dielectric constant film for introduction into wafer fabrication. It is anticipated in the semiconductor industry that the introduction of a low-*k* ILD material will follow the introduction of low-resistance metal lines made of copper (see Chapter 12 for a discussion of copper metallization). The investigation of alternative low-*k* dielectrics is being researched at this time.

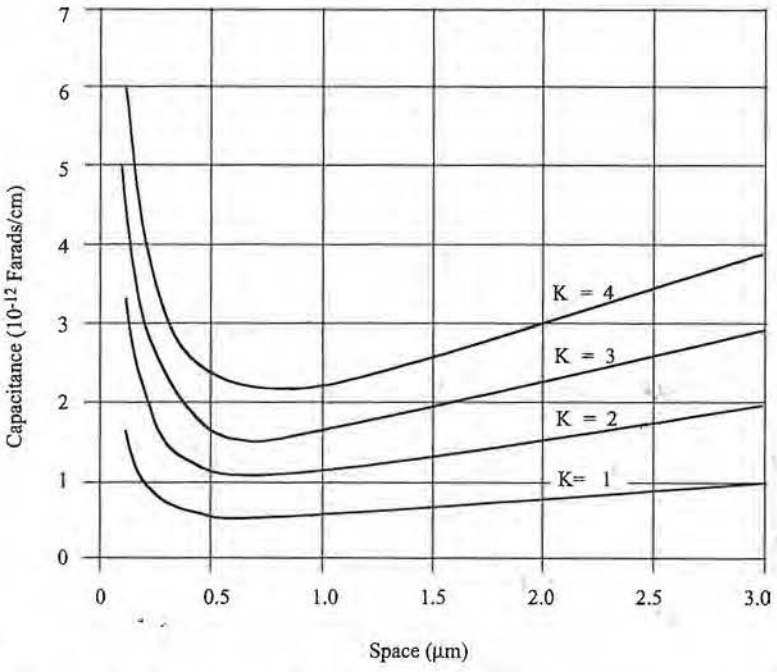


FIGURE 11.25 Total Interconnect Wiring Capacitance
(Used with permission from *Semiconductor International* (September 1998): p. 66.)

TABLE 11.5 Low-*k* Dielectric Film Requirements

Electrical	Mechanical	Thermal	Chemical	Processing	Metallization
Low dielectric constant	Good adhesion	Thermal stability	Resistant: acids and bases	Patternability	Low contact resistance
Low dielectric loss	Low shrinkage	Low coefficient of thermal expansion	Etch selectivity	Good gap fill	Low electromigration (corrosion)
Low leakage	Crack resistant	High conductivity	Low impurities	Planarization	Low stress voiding
High reliability	Low stress		No corrosion	Low pinhole	Hillock (smooth surface)
	Good hardness		Low moisture uptake	Low particulate	Compatible with barrier metals (Ta, TaN, TiN, and so on.)
			Acceptable storage life		

Adapted from P. Singer, "The Future of Dielectric CVD: High-Density Plasmas?" *Semiconductor International* (July 1997): p. 134.

High-*k* Dielectric Constant ■ There is ongoing investigation in the industry for new high-*k* dielectric materials, primarily for DRAM storage capacitors and as an eventual replacement for the extremely thin gate oxide (about 20 Å for 0.18 μm devices). DRAM technology has undergone a 4X increase in storage density every three years for the past 25 years due to processing and design improvements.[56] To attain the required charge storage with a SiO_2 and/or SiN_x dielectric, DRAM storage cell design has evolved into complex stacked capacitor structures (see Figure 11.26 on page 286). If the conventional SiO_2/SiN_x dielectric were replaced with a high-*k* dielectric, a simpler stack structure could be used for lower fabrication costs. A potential high-*k* material is tantalum pentoxide (Ta_2O_5), which has a value for *k* of 20 to 30 and can be easily integrated into the existing process. However, DRAM memory cells are sensitive to leakage and breakdown voltage of storage materials and interfaces. To compensate, the DRAM memory cell that requires a thicker Ta_2O_5

reduces its benefit. Another potential high-k material is barium strontium titanate ($(BaSr)TiO_3$, or BST), which gives a significant improvement in capacitance per unit area over conventional dielectrics.

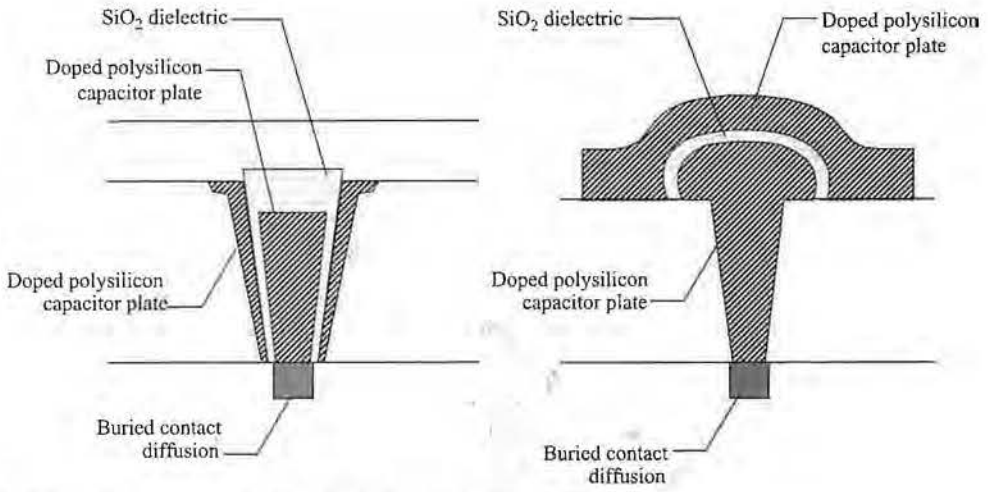


FIGURE 11.26 General Diagram of DRAM Stacked Capacitor

A new high-k gate dielectric is needed for the gate oxide because device scaling is forcing the existing SiO_2 to become extremely thin, with the future oxide thickness expected to be <10 Å for the 50 nm device generation. In a MOS transistor, the gate dielectric material must withstand a significant voltage difference between the gate electrode and the underlying silicon substrate. Thin gate oxides are affected by *tunneling currents*, which becomes a problem when the SiO_2 dielectric layer is below about 15 to 20 Å.[57] With the small gate dimensions in ULSI circuitry, electrons can tunnel through the gate material when the transistor is switched on and off. This leads to threshold voltage drift and eventual circuit failure because the device cannot switch states.

Device Isolation

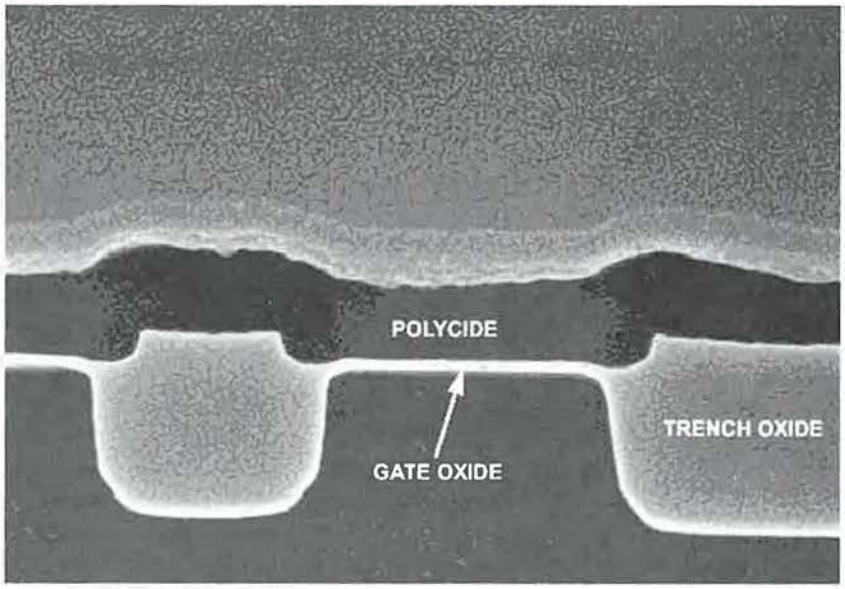
Device isolation in MOS wafer fabrication provides for electrical isolation between devices in the wafer. Isolation techniques serve to reduce or eliminate parasitic field transistors common in MOS planar fabrication (see Chapter 3). Isolation must accommodate scaling between the different device technologies (e.g., junction depth, gate oxide thickness, and so on.). This means that the space allocated for device isolation is being reduced for high-performance ICs. The two basic techniques for device isolation on MOS technologies are local field isolation through local oxidation of silicon (LOCOS), and shallow trench isolation (STI).[58]

Local Oxidation ■ The *local oxidation of silicon* (*LOCOS*) has been the traditional isolation technique for wafer fabrication of devices with critical dimensions of 0.35 μm and larger (see Chapter 10). This technique uses patterned islands of silicon nitride (Si_3N_4) to define the regions for oxidation growth. LOCOS isolation structures are too large for isolation in devices with deep submicron scaling.[59] The major factor limiting LOCOS for 0.25-μm geometries and below is the lateral growth of oxide during silicon oxidation, which imposes natural limits on the minimum area and topography achievable. LOCOS is not acceptable for high-density ULSI technology.

Shallow Trench Isolation ■ *Shallow trench isolation* (*STI*) is the preferred isolation process for wafers fabricated at the 0.25 μm and below technology nodes. The reasons why STI replaced the LOCOS process are:[60]

1. The need for more robust device isolation, especially in DRAM devices.
2. A significant reduction in the surface area for transistor isolation.
3. Superior latchup protection.
4. No channel encroachment.
5. Compatibility with chemical mechanical planarization (CMP).

In the basic STI process (see Chapter 10), trenches about 0.3 to 0.8 μm deep (up to several microns deep for DRAM trenches) are dry etched into the wafer substrate with nearly straight sidewalls and rounded corners (see Chapter 16 for an explanation of etching). The aspect ratio for STI trenches can vary from 2:1 to 5:1, with higher aspect ratios needed in DRAM devices due to their sensitivity to leakage. The trenches have a liner oxide grown on their surface, filled with CVD oxide and planarized using chemical mechanical planarization (CMP). STI technology is a more expensive process than LOCOS technology, primarily because it involves more complex process steps. Nevertheless, the benefits of STI outweigh its higher cost. The process steps for STI, including barrier layers and the liner oxide, are outlined in the CMOS process flow model in Chapter 9.



Shallow Trench Isolation
(Micrograph courtesy of Integrated Circuit Engineering)

SPIN-ON-DIELECTRICS

There are a wide range of low-*k* dielectrics that are designed to use wafer spin as an application method, referred to as spin-on-dielectric (SOD). The process for applying these materials is similar to a familiar process of spin-on-glass (SOG) used in low-cost IC fabrication, which we will review first.

Spin-On-Glass (SOG)

Spin-on-glass (*SOG*) was frequently used for gap fill and planarization of the ILD before the wide acceptance of chemical mechanical planarization (CMP) in the 1990s. SOG materials usually consist of two basic types: organic and inorganic.[61] The organic is based on siloxane, while the inorganic is based on a silicate. The organic siloxane SOG has significant water absorption after curing, is thermally unstable, and does not tolerate plasma exposure. After curing, the silicate SOG behaves like SiO_2, does not absorb excessive moisture, and is thermally stable. However, it shrinks significantly during curing, which leads to stress buildup and cracking if the layer is too thick. For these reasons, the siloxane SOG is usually used as a planarizing layer that undergoes an etchback process with a deposited oxide layer to render it smooth (see Chapter 18). The silicate SOG is used mainly for gap fill applications. There are many different commercial modifications of these two types.

Before applying the SOG, the wafer usually has a predeposited oxide layer, such as a PECVD oxide.[62] The SOG is a liquid and is applied by spinning the wafer at a predetermined speed in either a closed or open bowl. The spin speed and parameters such as ramp-up rate define the SOG thickness. The film is cured, typically at 400°C, and then etched back to planarize the surface. A capping oxide film is applied to seal and protect the SOG, which minimizes water absorption

(see Figure 11.27). Without the cap oxide, there is substantial risk of reliability problems from absorbed moisture, such as through poisoning where the via between the metal layers is corroded and has high resistance.

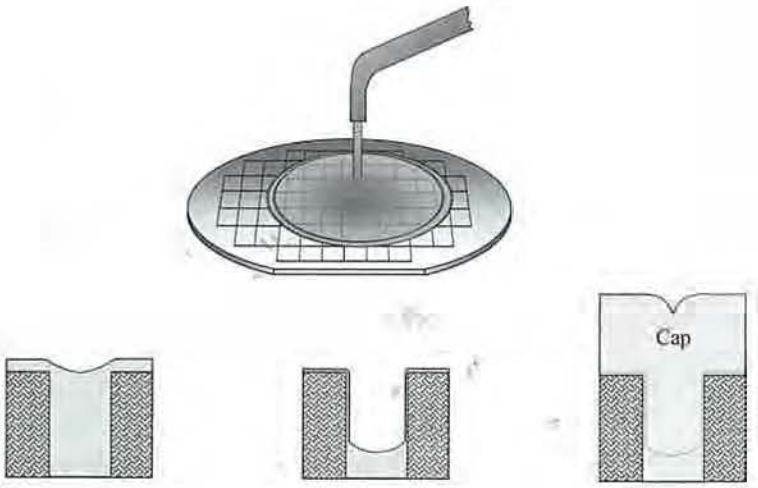


FIGURE 11.27 Gap-Fill with Spin-On-Glass (SOG)

Spin-On-Dielectric (SOD)

Low-*k* dielectric films are currently being investigated as *spin-on-dielectrics* (*SODs*). An example of an SOD low-*k* film is hydrogen silsesquioxane (HSQ), presented earlier in this chapter in Table 11.4 on page 283. The SOD technology is being considered as a cost-effective alternative to CVD processes for depositing low-*k* films. Most SOD applications have used standard spin coaters (used in photolithography which is discussed in Chapter 13) with batch curing in generic furnace tubes. There has been investigation into a single-wafer cluster tool approach to spin coat and cure the film, using a high-temperature hotplate at 350 to 475°C.[63] A proposed spin coat and cure process for HSQ is outlined in Table 11.6.

TABLE 11.6 Proposed HSQ Low-*k* Dielectric Processing Parameters

Major Operation	Process Step	Parameter
Spin Coating	Apply bowl speed	50 rpm
	Maximum bowl speed	800 to 1500 rpm
	Backside rinse	800 rpm, 5 sec
	Topside edge bead removal	1000 rpm, 10 sec
	Spin dry	1000 rpm, 5 sec
Cure	Initial soft-bake cure	200°C, 60 sec, N_2 purge
	In-line cure	475°C, 60 sec, N_2 ambient

In some cases, the nature of the SOD material is an extension of an existing SOG material. Other SOD materials are spin-on polymers that are substantially different than SOG materials. New low-*k* materials have less tendency to absorb moisture and have superior crack resistance. Because of these features, single layer deposition is usually acceptable with no need for a cap oxide layer. In some cases, however, an adhesion promoter is required.[64]

EPITAXY

Epitaxy is the deposition of a thin layer of single-crystal material upon the surface of a single-crystal substrate (see Figure 11.28). This epitaxial layer is often referred to as an epilayer. Epitaxy provides flexibility for the device designer to optimize performance by controlling epilayer doping thickness, concentration, and profile, independent of the wafer. This control is accomplished by the intentional addition of dopants during the epitaxial growth process. An epilayer also reduces the occurrence of latchup in CMOS devices (see Chapter 3). The most common epitaxial reactor in IC production is a high-temperature CVD system.[65]

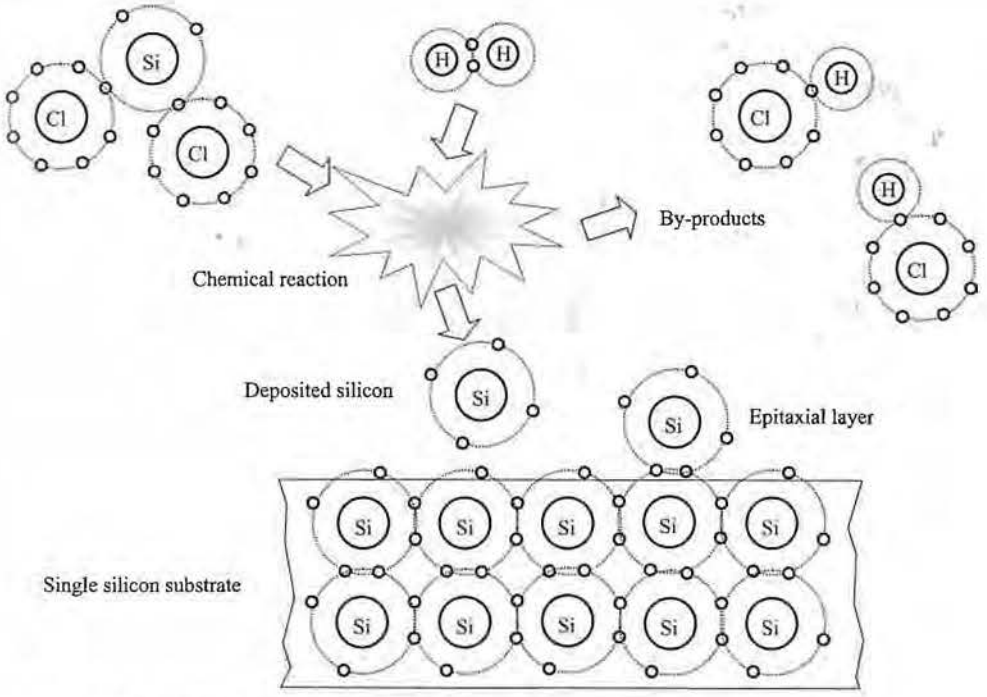


FIGURE 11.28 Silicon Epitaxial Growth on a Silicon Wafer

There are applications under investigation where epitaxy could contribute to advancing future IC performance. An example is *raised source/drain* (*S/D*) structures to achieve low contact resistance.[66] The raised S/Ds are formed by depositing epitaxial silicon on the source, drain, and gate areas of the device. This action effectively increases the surface areas of the S/Ds and therefore lowers the sheet resistance (similar to a larger diameter wire having lower resistance than the same wire with a smaller diameter). These deposits can decrease the contact resistance from 5 Ω/square on conventional devices to 1-2 Ω/square. The raised S/D structure is under investigation for possible implementation at the 0.15-μm technology node.

Undesirable conditions of nonuniform doping can occur during epitaxial deposition.[67] Since lightly doped epilayers are often grown on more heavily doped substrates, there is a condition of *autodoping* into the epitaxial layer. This condition occurs when dopant impurities evaporate from the wafer or are liberated due to chlorine etching of the wafer surface during deposition. These impurities move into the gas stream and cause unintentional doping of the epilayer. As the epilayer grows, less dopant is available from the wafer, and the impurities in the gas stream reach a constant level. Another form of irregular doping is the substrate acting as a source of dopant impurities that diffuse into the epilayer. This action is referred to as *out-diffusion*. Both autodoping and out-diffusion can affect the dopant transition between the substrate and epilayer, causing the transition to be less abrupt than desired.

If the film and substrate are of the same material (e.g., Si film on an Si substrate), then the film growth is *homoepitaxy*. A less common type of epitaxy is heteroepitaxy, which occurs when the film and substrate are of two different materials (e.g., Si on Al_2O_3).

Epitaxy Growth Methods

Epitaxial silicon is commonly deposited using CVD systems. Before epitaxy growth, the wafer must be cleaned of native oxide and any residual organic or metal impurities with a goal of achieving a perfect silicon surface (see Chapter 6). During the epitaxial deposition process, the atoms produced by the gas reaction strike the wafer surface and then move around until they find the correct location to bond to the surface atoms. This action forms the epitaxial layer with the same crystallographic arrangement as the substrate.

Possible gas sources for the epitaxy reaction are the hydrogen reduction of silicon tetrachloride ($SiCl_4$), silane (SiH_4), dichlorosilane (SiH_2Cl_2, or DCS) or trichlorosilane (TCS). Deposition temperatures are from 1050 to 1250°C. Nearly all silicon epitaxy for wafer fabrication is done by the reduction of chlorosilanes (SiH_xCl_{4-x}, where x = 0, 1, 2 or 3) that are diluted in hydrogen.[68] The temperature of the reaction can be lowered if there are fewer chlorine atoms in this precursor. Epitaxial silicon is not commonly grown with silane (SiH_4) because there is excessive particle formation when the silicon deposits on the warm surfaces of the reactor.

Different methods have been used to grow single-crystal layers on silicon wafers, including solid-phase, liquid-phase, vapor-phase, and molecular beam. Three methods used to grow epitaxial layers on silicon wafers for IC production are:

- Vapor-phase epitaxy (VPE)
- Metalorganic CVD (MOCVD)
- Molecular-beam epitaxy (MBE)

Vapor-Phase Epitaxy (VPE) ■ The most common method used for silicon epitaxial growth in wafer fabrication is *vapor phase epitaxy* (*VPE*), which is a subset of CVD.[69] Silicon VPE is achieved by passing gas compounds of the desired chemicals over single-crystal silicon wafers that are heated from 800 to 1150°C. The heat from the high temperature provides the energy necessary to drive the chemical reactions, which take place on the surface of the wafer. This process is shown in Figure 11.29.

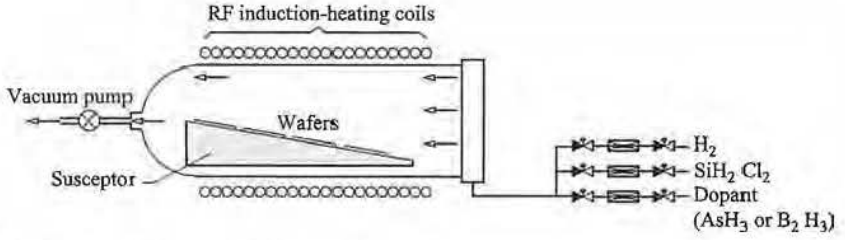


FIGURE 11.29 Illustration of Vapor-Phase Epitaxy

Before processing wafers in a VPE reactor, the system is purged with nitrogen or hydrogen, followed by a vapor HCl etching. The reactant gases, such as chlorosilane, along with dopant gases, are then introduced to the growth chamber where the wafer is heated to the desired temperature. Once the reactant and dopant gases are in the growth reactor, the chemical species undergo the necessary chemical and physical reactions to deposit the doped epilayer.

Typical equipment design for an epitaxial reactor consists of the gas distribution system, a reactor tube, a susceptor to hold and heat the wafer, a control system, and a gas exhaust system. Mass flow controllers and pneumatic valves are used in the gas distribution system to attain tight control over gas flows into the reactor chamber. The susceptor is typically made of graphite or a polysilicon that is coated with silicon carbide or silicon nitride. It must be strong and nonreactive to the reactants and their by-products.[70] Heating the susceptor is accomplished through inductive heating or by radiation from filament lamps. The horizontal and vertical reactors shown in Figure 11.30 are the most common. The susceptor in the horizontal reactor is tilted a few degrees to improve uniformity.

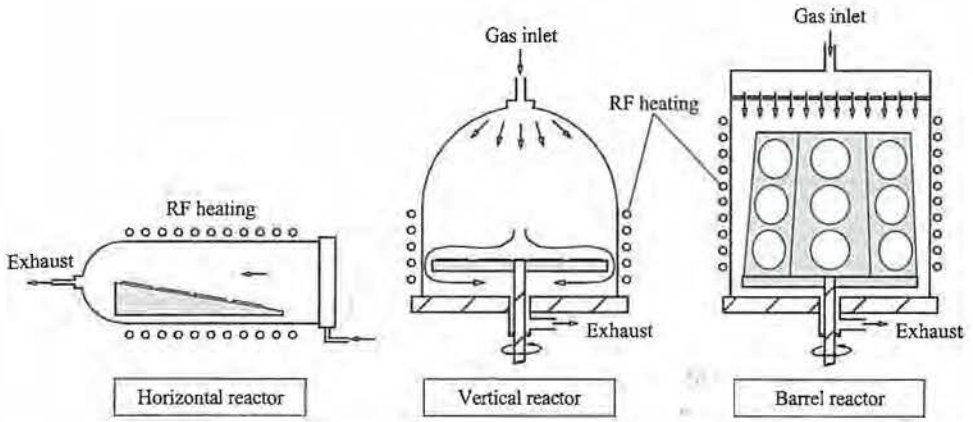


FIGURE 11.30 Silicon Vapor-Phase Epitaxy Reactors

Metalorganic CVD (MOCVD) ■ Another epilayer growth method is commonly referred to as *metalorganic CVD (MOCVD)*, but this is actually a broader term that is equally applicable to the deposition of polycrystalline and amorphous films of metals and oxides.[71] MOCVD is a form of VPE and is not typically used for silicon epitaxy because no suitable sources are readily available. It has been used to deposit compound semiconductor epitaxial layers, such as the III-V compound of gallium arsenide (GaAs) from organometallic sources at low temperature. As with the VPE process, compounds of the desired materials are transported to a heated substrate where the complex chemical reaction takes place on the wafer surface. MOCVD is important for the controlled deposition of ultra-thin, doped, or undoped semiconductor heterolayers (such as GaAs/Si), primarily used for lasers, light-emitting diodes (LED), and optoelectronic integrated circuits.[72] MOCVD is also used in development activity for depositing some organic low-k dielectrics for future IC fabrication.

Molecular-Beam Epitaxy (MBE) ■ *Molecular-beam epitaxy (MBE)* is one of the main methods used to deposit gallium arsenide (GaAs) heteroepitaxy with atomic resolution of thickness. It can also be used for depositing silicon onto a wafer substrate with very tight controls on epilayer thickness and doping uniformity. MBE takes place under conditions of high vacuum, usually at a base pressure of 10^{-10} to 10^{-11} torr or higher, typically with the use of a high vacuum cryopump. The reaction temperature range is between 500 to 900°C.

Most silicon MBE systems produce silicon atoms for the epitaxial reaction through the evaporation of silicon with an electromagnetically focused electron beam source. This process is similar to vacuum evaporation for deposition. The beam of silicon atoms leaving the silicon source travels through the evacuated chamber without collisions and deposits on the single-crystal wafer surface. Another more recent method is to deliver silicon atoms via a gas source at very low flow rates. The silicon growth rate of an MBE system is determined by measuring the number of atoms that leave the source and the fraction that actually strike the wafer surface and stick.

CVD QUALITY MEASURES

Important quality measures for CVD are listed in Table 11.7.

TABLE 11.7 Key Quality Measures for CVD

Quality Parameter	Types of Defects	Remarks
1. Voids during deposition of high-aspect ratio gap (>3:1) with PECVD SiO_2.	A. Keyhole voids are formed during deposition of high aspect ratio gaps. After chemical mechanical planarization (CMP) and removal of top surface, some voids become trenches (see Figure 11.31 on page 294). This trench can lead to an open circuit after metal deposition.	• Gap fill is critical as CDs are reduced and gaps have a high aspect ratio. • Voids are highly stressed regions and trap moisture or solvents that cause corrosion or outgas at high vacuum. • The root cause of this problem is trying to fill a high aspect ratio gap with a PECVD that is limited to deposition system. This application requires HDPCVD.
2. Film stress.	A. High film stress leads to cracking and delamination. B. Film stress can propagate silicon defects in the substrate. C. Stress may cause current leakage.	The presence of dopant in a glass film can reduce stress. Deposition parameters that affect film stress are: • RF power: adjust power to improve stress (e.g., reduce power by 10 watts to lower stress). • Pressure: adjust pressure to affect stress (e.g. increased pressure leads to higher film stress).
3. Film thickness.	A. Thickness of film exceeds requirements.	Deposition parameters that affect thickness are: • Time: reduce deposition time to reduce thickness (e.g., 1 sec reduction for each 100 Å of thickness). • Gas-flow rate: reduce gas flow to reduce thickness (e.g., reduce SiH_4 by 2 sccm for >5% thickness over nominal).
4. Refractive index (R/I).	A. R/I is a good monitor to assess quality of the film. B. R/I is highly dependent on the composition of the deposited film (stoichiometry).	R/I is an optical property of a material. Compared to thermal oxides, CVD oxides are inferior in quality and integrity. CVD oxides exhibit more particles and pinholes. The R/I of CVD SiO_2 can be compared to the R/I of SiO_2 (1.46) to assess relative quality: • High R/I means excessive Si in film. • Low R/I indicates a porous film, which tends to absorb moisture.

CVD TROUBLESHOOTING

Troubleshooting techniques for common CVD problems are described in Table 11.8. Plasma deposition systems have two areas of safety: chemical and electrical. Many plasmas use toxic gases (see Appendix A, Table A.3). There are high voltages and RF energy in the RF power supplies. Use caution when troubleshooting CVD systems.

TABLE 11.8 Common CVD Troubleshooting Problems

Problem	Probable Cause	Corrective Action
1. Particle contamination associated with film.	Source of particles is isolated by determining whether particles are found on top of film, in film, or below film: A. On film: particles formed after deposition. Check for particles on sidewalls of hot-wall reactors and belt-driven reactors. B. In film: Gas-phase nucleation particles from gas too rich in silane or silicon. Gas supply contamination causes particles. C. Under film: Particles from silicon carbide, quartz, or reactor walls fall on wafer before deposition.	• Particles on film: Particles on sidewalls indicate need for more frequent wet cleaning of quartzware and chamber surfaces for preventive maintenance. Inspect in situ dry cleaning process. Also verify the correct procedures for cleaning (manually or in situ). • Particles in film: Improper gas flows from MFC calibration or problem in process recipe of software program. Check for leaks in gas supply system or O-rings. Verify point-of-use filters are acceptable. • Particles under film: Check wafer cleaning process before deposition.
2. Film thickness.	Thickness is related to both equipment and process problems. Variables affecting thickness are: A. Incorrect temperature control. B. System pressure is too high or low. C. System power needs adjustment. D. Improper gas flow.	• Temperature controller may require calibration. A common problem is a defective thermocouple. • System pressure is controlled by process recipe. Check vacuum system for leaks. • Adjust RF power to optimize film thickness. • Check calibration of MFC to ensure proper gas flow. • If checking thickness with test wafer, verify the test wafer is clean and does not have a thickness variation before the test.
3. Cracking of dielectric material on top of electrostatic chuck (ESC).	High thermal load at the ESC causes the dielectric material to erode or crack. This condition leads to plasma arcing or wafer chucking/dechucking problems.	• Investigate the ESC backside cooling system to ensure it is functioning properly. • Inspect ESC materials to verify there is no breakdown due to high power exposure, temperature, or plasma clean conditions.

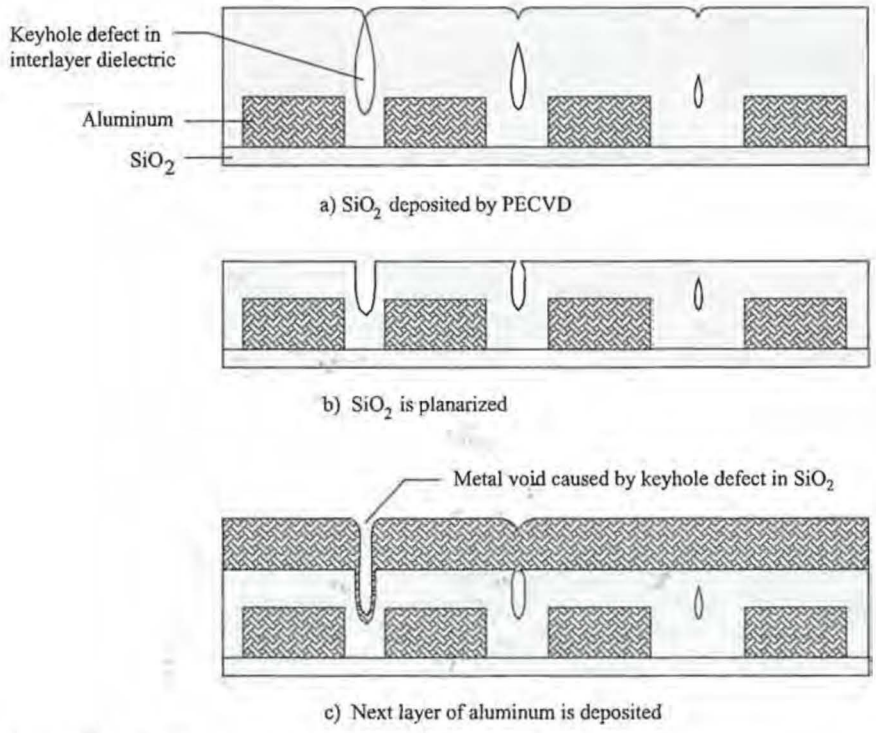


FIGURE 11.31 Effects of Keyholes in ILD on Metal Step Coverage

SUMMARY

Multilevel metallization with dielectric and metal layers is necessary for advanced ICs. Thin films have special characteristics to meet the requirements for wafer fabrication, including high aspect ratio gap fill. A film grows in stages from a cluster of nuclei to a continuous film. There is a wide range of tools for depositing film layers, with the focus on dielectric chemical vapor deposition (CVD). CVD deposits a thin film on the wafer surface through a chemical reaction that is assisted by thermal or plasma energy. CVD surface reactions include pyrolosis, oxidation, and reduction. The CVD chemical reaction follows defined steps and can be limited by the supply of chemicals or by the nature of the surface reaction. The thin film is sometimes doped to obtain improved performance. Reactors for CVD are categorized by atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD), or plasma-assisted CVD. APCVD is simple in design and is primarily used to deposit conformal oxide with a TEOS-O_3 process. LPCVD deposits various films, including oxide, silicon nitride, and polysilicon. The LPCVD process is reaction-rate limited (gas flow is not critical) and often occurs at lower temperatures. Plasma-assisted CVD is divided into plasma-enhanced CVD (PECVD) and high-density plasma CVD (HDPCVD). PECVD was the first plasma-assisted CVD but had limited use for filling gaps less than 0.5 μm. HDPCVD is used for advanced ICs because of its excellent gap-fill capability for high-aspect ratios at relatively low temperatures. The deposited dielectric material increases chip performance by reducing the RC interconnect delay with a low-*k* dielectric. Dielectric material is also important for isolation technologies. Dielectric materials have been applied in liquid form by spinning, which may be an application method for future low-*k* dielectrics. Epitaxy is grown primarily by CVD methods, including vapor-phase epitaxy (VPE), metalorganic CVD (MOCVD), and molecular-beam epitaxy.

KEY TERMS

multilevel metallization
aluminum metallization
critical layers
noncritical layers
first interlayer dielectric (ILD-1)
premetal dielectric (PMD)
interlayer dielectric (ILD)
thin film
stoichiometry
aspect ratio
nucleation
nuclei coalescence
continuous film
chemical vapor deposition (CVD)
reactor
heterogeneous reaction (also surface catalyzed)
homogeneous reaction
adsorption
desorption
species
precursors
mass-transport limited
reaction-rate limited
kinetically controlled
boundary layer
stagnant layer
phosphosilicate glass (PSG)
borosilicate glass (BSG)
borophosphosilicate glass (BPSG)
fluorosilicate glass (FSG)
cluster tools
hot-wall reactor
cold-wall reactor
atmospheric pressure CVD (APCVD)
silane
TEOS oxide
low pressure CVD (LPCVD)
silicon nitride (Si_3N_4)
silicon oxynitride (SiO_xN_y)
plasma-enhanced CVD (PECVD)
PETEOS
silicon nitride PECVD
high-density plasma CVD (HDPCVD)
dep:etch ratio
dielectric constant (k)
device isolation
local oxidation of silicon (LOCOS)
shallow trench isolation (STI)
spin-on-glass (SOG)
spin-on-dielectric (SOD)
epitaxial growth
raised source/drain structures
autodoping
out-diffusion
homoepitaxy
heteroepitaxy
vapor-phase epitaxy (VPE)
metalorganic CVD (MOCVD)
molecular-beam epitaxy

REVIEW QUESTIONS

1. What is multilevel metallization? Why is it necessary for chip fabrication?
2. What is aluminum metallization? Describe a chip critical layer and a noncritical layer.
3. Explain the purpose of an ILD layer. Where is the ILD-1 layer located on a chip?
4. What is a thin film? List and describe eight characteristics of an acceptable thin film.
5. Define the aspect ratio. Why is a high-aspect ratio important for ULSI devices?
6. List and describe the three stages of thin film growth.
7. List the five major techniques for deposition.
8. Define chemical vapor deposition (CVD).
9. What are the five basic CVD chemical reactions? Give a short description of each reaction.
10. In a CVD reaction, is a heterogeneous or homogeneous reaction preferred? Why?
11. Identify and describe the eight steps in a CVD reaction.
12. Explain the difference between a mass-transport limited and a reaction-rate limited CVD process. Which process is temperature dependent?
13. What is a boundary layer in CVD? Under what conditions does it become a stagnant layer?
14. What is the beneficial effect of low pressure in a CVD reaction?
15. What do the abbreviations PSG, BPSG, and FSG stand for? What are three benefits of adding dopants to oxide?

16. Describe the different types of CVD reactors and their principal advantages.
17. Explain the difference between a hot-wall reactor and cold-wall reactor for CVD.
18. Explain APCVD. What is the principal disadvantage with APCVD SiO_2, using silane as a source?
19. What is TEOS? Discuss the primary advantages to using APCVD TEOS-O_3.
20. Why is LPCVD more common than APCVD? Describe LPCVD processing.
21. Why does LPCVD operate in the reaction-rate regime?
22. State what film is deposited using LPCVD TEOS, and explain the advantage of this film.
23. Why is silicon nitride often used as a passivation layer?
24. What CVD tool is used to deposit the polysilicon gate material? List six reasons why polysilicon is used as a gate electrode.
25. What are the benefits to using a silicon oxynitride film?
26. State six advantages to using plasma during CVD.
27. What is PECVD? What is the main difference between PECVD and LPCVD?
28. Describe the main differences between silicon nitride PECVD and LPCVD.
29. Discuss a major limitation for using PECVD in ULSI microchips.
30. Explain what HDPCVD is. What are its main benefits in advanced ICs?
31. Describe the effect wafer biasing has on HDPCVD directionality.
32. Explain simultaneous deposition and etching for HDPCVD. What is the value for the typical dep-etch ratio?
33. List and describe the five steps used for simultaneous deposition-etching in CVD.
34. Discuss the importance of the dielectric constant of the ILD.
35. Explain the interconnect delay and why it is beneficial to lower the ILD constant dielectric.
36. What is an application for a high-k dielectric material and why is it needed?
37. What are LOCOS and STI? Why has STI replaced LOCOS for advanced ICs?
38. List the processing steps for STI.
39. What is spin-on-glass? Explain spin-on-dielectric and what it could be used for in future applications.
40. Describe what epitaxy is. Define the terms *autodoping* and *out-diffusion*.
41. List and discuss three methods for epitaxial growth.

DEPOSITION EQUIPMENT SUPPLIERS' WEBSITES

Amtech Systems Inc.	http://www.amtechsystems.com/
Applied Materials	http://www.appliedmaterials.com/products/
ASM	http://www.asm.com/
CVC Incorporated	http://www.cvc.com/
CVD Equipment Corporation	http://www.cvdequipment.com/
Genus Incorporated	http://www.genus.com/
Kokusai Semiconductor Equipment	http://www.ksec.com/
Novellus Systems Inc.	http://www.novellus.com/index.htm
TEL, Tokyo Electron Ltd.	http://www.teainet.com
Tystar Corporation	http://www.tystar.com/

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CHAPTER 12

METALLIZATION

Metallization in wafer fabrication is the process of depositing metal film over a dielectric film and later patterning it to form the interconnecting metal lines and plugs of integrated circuits. This is similar to using insulated copper wire in an automobile to interconnect all the electrical components to make a fully-functional electrical system. The metal lines are sandwiched between dielectric layers for electrical integrity. High-performance microprocessors use metal lines to interconnect tens of millions of devices on one chip. Transistor densities are projected to reach 1 billion transistors per chip by the year 2010, with a corresponding increase in interconnect complexity.

Microchip interconnect technology has become a critical challenge for future IC performance due to the need to decrease signal propagation delay. Because the density of ULSI circuit elements is increasing, interconnect resistance and parasitic capacitance increase, thereby slowing the signal propagation.

A significant change currently underway in wafer fabrication technology is the reduction in interconnect metal resistivity, ρ. This reduction is achieved by the replacement of aluminum alloy with copper as the primary conducting metal. With deep submicron linewidths, there is also a need for a low-k interlayer dielectric (ILD). Lowering the dielectric constant will reduce parasitic capacitance, which contributes to signal delay.

Traditionally, the methods used to deposit metals on a wafer have been physical processes. On the other hand, processes used to deposit insulating and semiconducting layers usually involved the CVD chemical reactions studied in Chapter 11. This separation into physical and chemical processes is less defined with the introduction of new IC metallization technology.

OBJECTIVES

After studying the material in this chapter, you will be able to:

1. Explain the terminology for metallization.
2. List and describe the six categories of metals used in wafer fabrication. Discuss the performance requirements and give applications for each metal category.
3. Explain the benefits for using copper metallization in wafer fabrication. Describe the challenges for implementing copper.
4. State the advantages and disadvantages to sputtering.
5. Describe the physics of sputtering and discuss different sputtering tools and applications.
6. Describe the benefits and applications for metal CVD.
7. Explain the fundamentals of copper electroplating.
8. Describe a process flow for dual-damascene processing.

INTRODUCTION

Wafer metallization is the deposition of a thin film of conductive metal onto a wafer by use of a chemical or physical process. This process is closely linked to dielectric deposition. Metal lines conduct the signal through the IC circuit while the dielectric layers ensure signals are not influenced by adjacent lines. Both metal and dielectrics are thin film processes. In some cases, metal and dielectrics are deposited by the same type of equipment.

Metallization has unique terminology for the different metal connections. The term *interconnect* describes the conductor materials, such as aluminum, polysilicon, or copper, that create the metal wiring that carries electrical signals to different parts of the chip. Interconnect is also used as a general term for the wiring between devices on a die and the overall package. A *contact* is the electrical connection at the silicon surface between the devices in the silicon wafer and the first metal layer. *Vias* are openings that pass through the various dielectric layers to form an electrical pathway from one metal layer to the adjacent metal layer. A metal *plug* fills the vias to form the electrical connection (interconnect) between the two metal layers. These connections are illustrated in Figure 12.1.

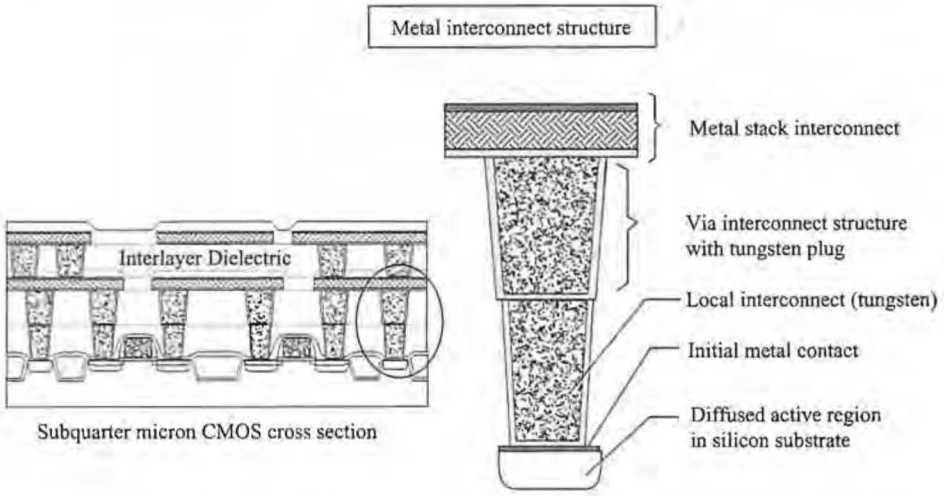


FIGURE 12.1 Multilevel Metallization

The interlayer dielectric (ILD) is an insulating material that electrically separates the metal levels. Once deposited, the ILD is patterned and etched to form via pathways for the various metal layers and the silicon. The vias are filled with a metal, traditionally tungsten (W), to form the via plug. Appreciate that there are many vias on a wafer, up to 10^{11} vias on each individual layer of a 300-mm product wafer.[1] This process of creating vias in the ILD is repeated for every ILD layer on the die. In traditional metallization, a blanket layer of aluminum alloy metal is deposited on the dielectric layer and then patterned and etched to form metal lines. Metal etch is an important technology for traditional metallization.

Metallization is in a transition period and is undergoing rapid change with the introduction of copper metallurgy to replace aluminum alloy. This change is due to the difficulty of etching copper. To overcome this problem, copper metallurgy uses the dual damascene process to form vias and copper interconnects (explained later in this chapter). This metallization process is literally the opposite approach of traditional metallization (see Figure 12.2). Damascene starts with deposition of a blanket dielectric, planarizes the dielectric, patterns and etches holes or trenches in the dielectric for vias and connecting metal lines, deposits blanket metal into the trenches, and then planarizes the metal down to the dielectric to define the metal interconnects.

Metallization technology is critical for increasing performance in advanced ICs, as explained in Chapter 11. Reducing chip performance signal delay caused by interconnect lines was not a significant concern for older IC technologies. The dominant signal delay has traditionally been caused by the device. However, for newer ULSI products manufactured with denser wiring, signal delay

due to interconnect has become a larger portion of the clock cycle time and has more effect on limiting the IC performance.[2]

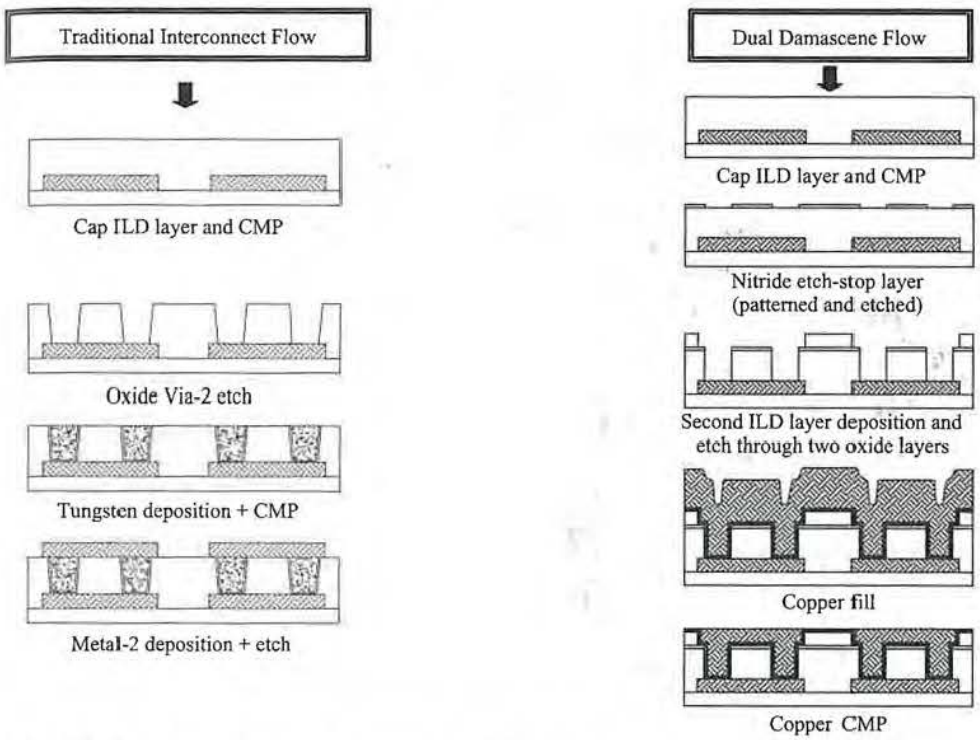
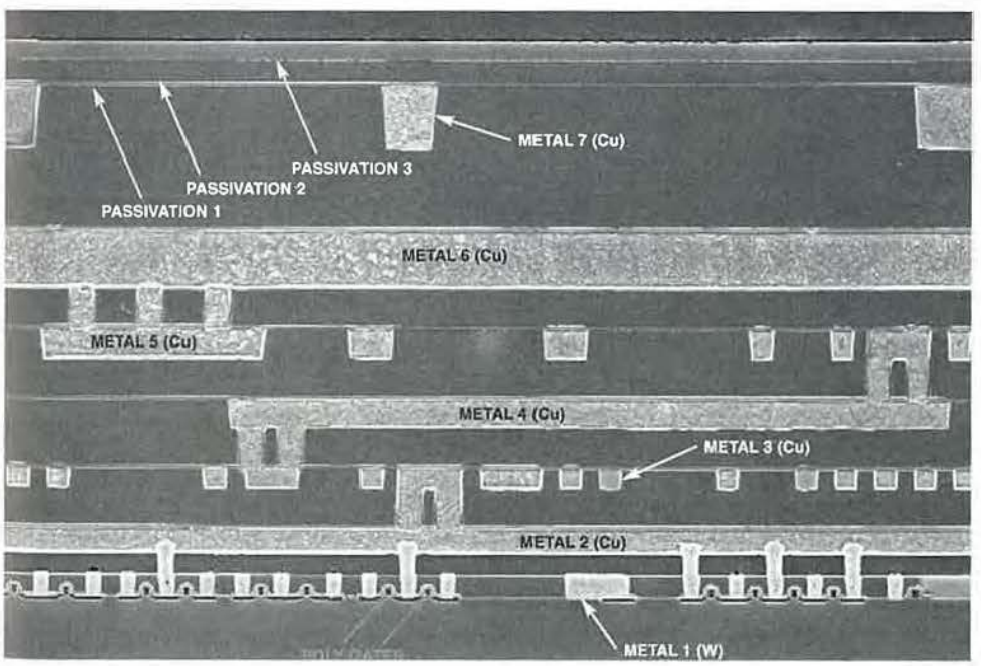


FIGURE 12.2 Traditional Versus Damascene Metallization



Copper Metallization
(Micrograph courtesy of Integrated Circuit Engineering)

TYPES OF METALS

The types of metals and metal alloys used for chip interconnects are evolving based on the performance requirements. Requirements for a successful metal material are:[3, 4]

1. **Conductivity:** Must be highly conductive and capable of handling high current densities while maintaining electrical integrity.
2. **Adhesion:** Ability to adhere to the underlying substrate and easily connect to external connections. Low contact resistance to semiconductor and metal interfaces.
3. **Deposition:** Readily deposited with a uniform structure and composition (for alloys) by a relatively low-temperature process. Deposition into high-aspect ratio gaps for damascene metallization technique.
4. **Patterning/Planarization:** High-resolution patterning for traditional Al-based metallization without etching the underlying dielectric. Ease of planarization for damascene metallization.
5. **Reliability:** The metal is relatively soft and ductile in order to withstand cyclic temperature variations during processing and service.
6. **Corrosion:** High resistance to corrosion with minimal chemical interactions with the adjacent layers and underlying device regions.
7. **Stress:** Resistance to mechanical stress to reduce wafer distortion and material failures for reasons such as cracking, void formation, and stressed-induced corrosion.

The melting temperature and resistivities of different metals found in wafer fabrication and silicon are shown in Table 12.1.[5]

TABLE 12.1 Silicon and Select Wafer Fab Metals (at 20°C)

Material	Melting Temperature (°C)	Resistivity (μΩ-cm)
Silicon (Si)	1412	$\approx 10^9$
Doped Polysilicon (Doped Poly)	1412	≈ 500 to 525
Aluminum (Al)	660	2.65
Copper (Cu)	1083	1.678
Tungsten (W)	3417	8
Titanium (Ti)	1670	60
Tantalum (Ta)	2996	13 to 16
Molybdenum (Mo)	2620	5
Platinum (Pt)	1772	10

The various metals and metal alloys used in wafer fabrication can be grouped into the following categories:

- Aluminum
- Aluminum-copper alloys
- Copper
- Barrier metals
- Silicides
- Metal plugs

Aluminum

The earliest interconnect metal in semiconductor fabrication was aluminum, and it is still the most common interconnect metal in wafer fabrication. Aluminum is projected to continue as the dominant fab interconnect metal for several more years.[6] Copper interconnect metal is expected to replace aluminum for high-performance IC fabrication during the early 2000s. Nevertheless, it is beneficial to review the background into the selection of aluminum for metallization because many of the same basic technical challenges exist today.

Selection of Aluminum ■ Aluminum has been one of the major materials used in wafer fabrication, along with silicon and silicon dioxide. It is used during wafer fabrication in thin film form to interconnect the different devices in the silicon wafer (see Figure 12.3). At the same time, aluminum is one of the thickest films deposited on the wafer, with the first metal layer deposition about 5,000 Å thick. The upper noncritical layers on a wafer (e.g., metal layer with bonding pads) can range up to 20,000 Å thick.

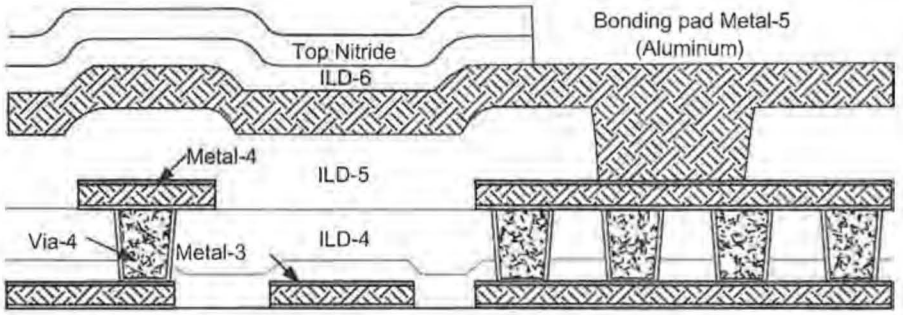


FIGURE 12.3 Aluminum Interconnect

Aluminum's low resistivity of 2.65 μΩ-cm at 20°C has similar but slightly higher resistivity than copper, gold, and silver. However, silver and copper are both prone to corrosion and have high diffusivity in Si and SiO_2, a fact that keeps them from being used for semiconductor fabrication. Gold and silver are much more expensive than aluminum and do not adhere well to oxide films. Gold was sparingly used in the beginning of wafer fabrication, but its high contact resistance with silicon required a platinum barrier metal. On the other hand, aluminum reacts readily with silicon dioxide (SiO_2) when heated to form a thin layer of aluminum oxide (Al_2O_3), which promotes adhesion between the silicon dioxide and aluminum. Aluminum is easily deposited on the wafer and etches in solutions that do not attack underlying films. For these reasons, aluminum was selected as the preferred metal for metallization.

Overall, aluminum is compatible with the major processes in silicon IC fabrication and is relatively inexpensive, making it the choice for metallization since the early days of IC fabrication. However, because of increased circuit density, increased number of metal layers on a wafer, and the reduction in linewidth due to scaling, the metallization technology has evolved from the simple one-level metal layer to a scheme of multiple metal layers. With its lower resistivity, copper is desirable to replace aluminum as the primary interconnect material.

Ohmic Contact ■ Before VLSI circuitry, pure aluminum was used for metallization. Silicon melts at a temperature of 1412°C and pure aluminum melts at 660°C. However, aluminum and silicon alloyed together actually have a lower melting temperature depending on their composition. For an alloy of 88.7% aluminum and 11.3% silicon, the alloy melts at 577°C, which is referred to as the *eutectic temperature.*[7] The eutectic temperature is the lowest temperature that an alloy melts at a particular eutectic composition.

To form a contact between aluminum and silicon, it is necessary to heat the interface, usually in an inert or reducing H_2 atmosphere at a temperature of 450 to 500°C. This thermal bake is also referred to as a low temperature *anneal* or *sinter.* Baking the aluminum on silicon forms a desirable electrical interface referred to as an *ohmic contact.* An ohmic contact has very low resistance (the voltage-current characteristics of the contact interface behave according to Ohm's law). However, there is a small resistance associated with the ohmic contact and it is inversely proportional to the area of the contact. That is, smaller contacts have higher resistance. In modern chip design, ohmic contacts use a special refractory metal (e.g., titanium in the form of a silicide) as a contact at the silicon interface to reduce electrical resistance and improve adhesion (see Figure 12.4 on page 304). Ohmic contacts are fabricated with a salicide (self-aligned silicide) process to achieve optimal positioning above the source/drain and in close proximity to the gate structure. The salicide process is discussed later in this chapter.

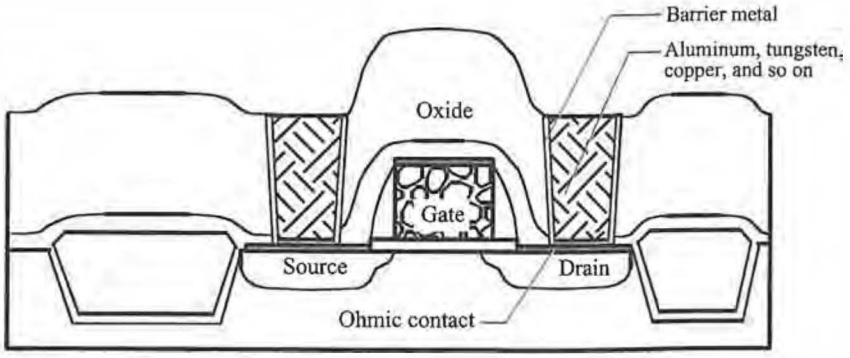


FIGURE 12.4 Ohmic Contact Structure

Given the hundreds of millions of contacts that can exist on a particular die, a reliable contact interface with low resistance and excellent adhesion is extremely important for optimum electrical performance. A failure in any individual contact can cause the entire chip to fail during test or use.

A problem encountered during the earliest work to develop ohmic contacts was undesirable interaction between the aluminum and silicon during the thermal step. This condition led to the microalloying of the contact metal to the silicon, and was referred to as *junction spiking*. Spiking occurs when the interface of pure aluminum and silicon is heated (see Figure 12.5), causing the diffusion of silicon into the aluminum. The amount of silicon dissolved into the aluminum is not uniform and will depend on the time and temperature involved in the heating process. If pure aluminum is heated to 450°C and a source of silicon is present, silicon will begin to dissolve in the aluminum until it reaches a concentration of about 0.5%.[8] The problem is that the source of this silicon is the wafer. As the silicon is dissolved in the aluminum, it leaves behind voids in the wafer, permitting spikes of aluminum to form and penetrate into the silicon contact region. If the aluminum forms an ohmic contact to a shallow junction, the spike may cause a junction short.

The problem of junction spiking was addressed by two methods: the addition of silicon to the aluminum and barrier metallization. The first approach was to use an alloy of aluminum and silicon instead of pure aluminum. If there is already silicon in the aluminum, this will slow down the dissolution of additional silicon from the substrate. However, silicon alloying in aluminum is limited and can lead to silicon nodule formation (small regions of high silicon concentration) in the aluminum due to silicon condensation. Nodule formation can significantly increase the contact resistance and pose a serious reliability concern from local heating at the nodules. The main method to resolve junction spiking was the introduction of barrier metallization to inhibit diffusion (see the following section).

It is important that the oxide at the contact interface be as thin as possible. Wafers with exposed contact regions are often dipped in a dilute hydrofluoric (HF) acid solution immediately before placing the wafers in the deposition chamber. This serves to remove the native oxide layer prior to contact formation.

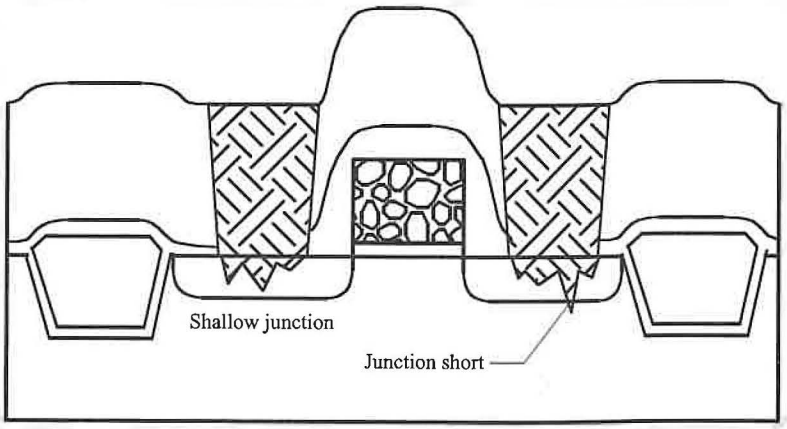


FIGURE 12.5 Junction Spiking

Aluminum-Copper Alloys

Aluminum metal was selected as the primary interconnect material for ICs because of its low resistivity and its compatibility with silicon and the wafer fabrication process. However, aluminum suffers from a reliability problem known as *electromigration*. This is the movement of aluminum atoms in the conductor due to momentum transfer from the electrons carrying the current.[9] Under high current-density conditions, electrons collide with aluminum atoms, causing the atoms to gradually move. This movement of atoms leads to a depletion of atoms at the negative end of the conductor. In conductor regions where depletion occurs, this action leads to voids, thinning of lines, and a potential open circuit. In other regions of the conductor that have an accumulation of metal atoms, metal atoms pile up and form hillocks (see Figure 12.6).[10] *Hillocks* are protrusions on the surface of metal films due to electromigration. If excessive or large hillocks form, adjacent lines or lines on two levels can short together. With advanced circuitry designs in ULSI technology, there is increased current density and chip temperature, both of which make the aluminum chip metallization more prone to electromigration.

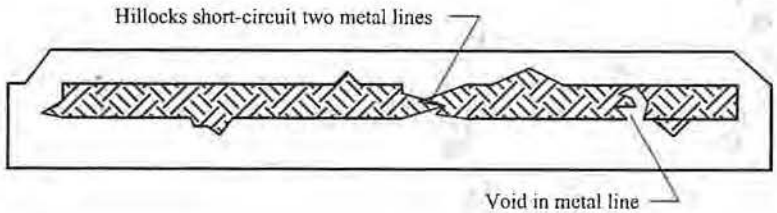


FIGURE 12.6 Hillock on a Metal Line

Electromigration in interconnects is controlled by alloying the aluminum with between 0.5 to 4% copper. This alloying essentially increases the conductor's current-carrying capacity by reducing the grain boundary diffusion effects in the aluminum. At the same time, it has been shown that values of copper in aluminum greater than 8% will actually increase electromigration.[11] The exact reason why the addition of copper reduces the chance of electromigration failure in Al-Cu alloys is not well understood.[12] If copper is alloyed with aluminum, more care must be given to plasma etching this alloyed aluminum (etching is discussed in Chapter 16). Copper is difficult to etch, and any residual copper remaining after etching the aluminum alloy interconnect can promote corrosion.[13] It is also possible to have electromigration in contacts and vias. Electromigration failure in contacts is resolved by the use of barrier metallization.

Electromigration is probably one of the most widely studied failure mechanisms of integrated circuits. Studies of this failure began in the 1950s with the development of the semiconductor and intensified in the late 1960s with the discovery of crack formation in the aluminum conductor leading to failures.[14] The significance of electromigration is that it usually occurs after the chip has been in service for an amount of time, which means that failure occurs catastrophically during customer usage.

Copper

A major transformation is underway in IC design and fabrication by means of the introduction of *copper interconnect* technology. Copper interconnects will replace aluminum metallization with copper to achieve significant benefits in chip performance. A legitimate question that someone may pose is why introduce copper if aluminum has performed so admirably over the years.

Need for Copper ■ The benefits for introducing copper for IC interconnect metallization are:[15]

1. **Reduction in resistivity.** The interconnect wiring resistivity reduces from 2.65 $\mu\Omega$-cm for aluminum to 1.678 $\mu\Omega$-cm at 20°C for copper, reducing RC signal delay and increasing chip speed.
2. **Reduction in power consumption.** Narrower lines consume less power.

3. **Tighter packing density.** Narrower lines permit tighter circuitry packing, which means that fewer levels of metal are needed.
4. **Superior resistance to electromigration.** Copper does not have a concern for electromigration.
5. **Fewer process steps.** Potential for 20 to 30% fewer processing steps with damascene processing of copper.

As wafer fabrication design rules reduce to 0.15-μm linewidths and below, the increased packing density of devices on the chip permits more electrical signal speed from device to device (the transistors are closer; therefore, the signal has less distance to travel). This density leads to improved chip performance. However, this improved chip performance is only possible if the interconnect system between the devices is optimized. Narrower linewidths lead to increased line resistance. Tightly spaced conductor lines with a dielectric material between them act as capacitors, leading to a degradation in performance from an increase in resistance (R) and capacitance (C). This condition is the signal delay or interconnect delay discussed in Chapter 11. If either or both of these two parameters are reduced, then the signal delay reduces, leading to increased chip performance.

One possible method reducing interconnect resistance is to increase the conductor cross section. However, this contradicts the goal of increased packing density since wider conductors will take substantially more space. Smaller IC feature sizes are not achievable with larger linewidths. This is why the semiconductor industry is placing emphasis on copper—to lower the interconnect resistance, which lowers R and therefore the overall signal delay. The optimum improvement to RC signal delay is gained when resistance (R) is reduced and the capacitance (C) is lowered by using a low-*k* dielectric along with thinner barrier metals (see Table 12.2).[16]

TABLE 12.2 Change in Interconnect Delay Compared to 0.25-μm Device Generation

Technology	0.25 μm	0.18 μm	0.13 μm
Conventional Interconnect Technology: • Al/Cu interconnect alloy and TiN barrier metal	0	+21%	+93%
New Technology Introduced by Generation: • Reduced barrier thickness • Low-*k* (3.0) dielectric • Dual damascene Cu interconnect and plugs	−10%	−27%	−16%

Another benefit from the implementation of copper is that smaller linewidths can carry the same amount of current, permitting a tighter packing density on each metal level. This condition produces fewer overall levels of metal on a chip, leading to significantly reduced manufacturing costs.[17]

Copper is a relatively soft metal. It has superior resistance to electromigration, a common reliability problem with aluminum.[18] This means that chips fabricated with copper can handle higher electrical power densities, which permits the development of new product applications. Table 12.3 compares Cu and Al for different properties and processes common in wafer fabrication.[19]

TABLE 12.3 Comparison of Properties/Processes Between Al and Cu

Property/Process	Al	Cu
Resistivity (μΩ-cm)	2.65 (3.2 for Al—0.5% Cu)	1.678
Electromigration resistance	Low	High
Corrosion resistance (in air)	High	Low
Etch processing	Yes	No
CMP (chemical mechanical planarization) processing	Yes	Yes

Copper Challenges ■ There are three major challenges involved with using copper as semiconductor interconnects that distinguish it from traditional aluminum interconnects. These three challenges differ significantly from aluminum technology and must be resolved before the implementation of copper for IC interconnects:[20]

1. Copper diffuses quickly into oxides and silicon. This is a concern if copper diffuses into the active region of the silicon (i.e., source/drain/gate region of the transistor) because it will damage the device by creating junction or oxide leakage.
2. Copper cannot be easily patterned using regular plasma etching techniques (see Chapter 16 for a discussion of etching). Copper dry etching does not produce a volatile by-product during the chemical reaction that is necessary for economical dry etching.
3. Copper oxidizes quickly in air at low temperatures (<200°C) and does not form a protective layer to stop further oxidation.

These challenges are addressed by converting to dual damascene processing with special barrier metals optimized for copper. Damascene processing eliminates the need to etch copper. Furthermore, tungsten plugs are expected to be used as the first level of metal to contact the source, drain, and gate regions.[21] This use of tungsten overcomes the concern of copper contaminating the silicon (referred to as copper poisoning). The tungsten may even be patterned for wiring of the local interconnect (LI). All other metal lines and vias for the multiple metal layers are expected to be copper.

Another major hindrance to converting to copper in semiconductor manufacturing is the natural reluctance to introducing new materials into production. New materials means there are new sources of contamination, new equipment and procedures, unpredictable results, and so on. Change always brings unforeseen problems that pose increased risks to the semiconductor manufacturer. However, these risks are balanced by the benefits from changing the interconnect material in order to improve IC performance.

Barrier Metals

A more effective way to make reliable ohmic contacts to shallow junctions without material diffusion or problems such as junction spiking is to use barrier metallization. A *barrier metal* is a thin layer of deposited metal or metals that is designed to prevent intermixing of the materials above and below the barrier (see Figure 12.7). The thickness of barrier metals has typically been around 100 nm for features sizes in the 0.25-μm generation, which is substantially thinner than the 400 to 600 nm thickness required for 0.35-μm generation of devices. Thickness of barrier metals is projected to decrease to 23 nm or less for the 0.18-μm technology node and beyond.[22]

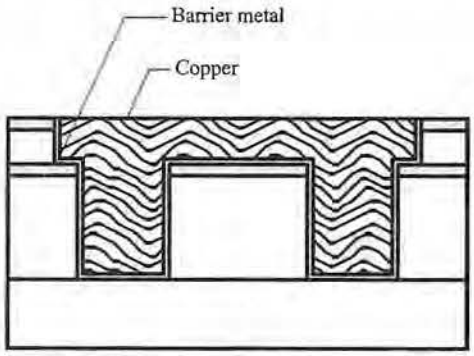


FIGURE 12.7 Barrier Layer for Copper Interconnect Structure

Barrier metals are widely used in semiconductor manufacturing. For contacts between the tungsten (W) plug that connects the aluminum interconnect wiring and the silicon source/drains, the barrier metal prevents the silicon and W from coming into contact with each other. This barrier prevents diffusion between the W and silicon and any junction spiking.

The essential properties of an acceptable barrier layer metal are:

1. Good diffusion barrier properties so that the diffusivity of the two interface materials (e.g., tungsten and silicon) is low at the sintering temperature (*sintering* refers to joining the materials by thermal means).
2. High electrical conductivity with low ohmic contact resistance.
3. Good adhesion between the semiconductor and the metal.

4. Resistance to electromigration.
5. Stability when thin and at high temperature.
6. Resistance to corrosion and oxidation.

Metals commonly used for barrier metals are a class of high melting point metals known as *refractory metals.* Common refractory metals used in multilevel metallization for wafer fabrication are titanium (Ti), tungsten (W), tantalum (Ta), molybdenum (Mo), cobalt (Co), and platinum (Pt). Refractory metals have been used in wafer fabrication since the 1960s, such as in the formation of Schottky barrier diodes in bipolar processes. The benefits of using titanium as a barrier metal for aluminum alloy wiring are improved adhesion, reduced contact resistance, reduced stress, and controlled electromigration. To achieve good barrier properties, wafers undergo a clean step (referred to as *sputter etch* and explained in a later section) before deposition in the processing chamber to remove native oxides and oxide residues on the wafer.

Titanium tungsten (TiW) and titanium nitride (TiN) are two common barrier metal layers that inhibit diffusion between the silicon substrate and aluminum. TiN is widely used in ULSI manufacturing for its superior barrier performance in aluminum alloy interconnect processing. TiN functions as a barrier metal for both tungsten and aluminum. TiN is also widely used as an antireflective coating on aluminum to improve the photolithography patterning process (see Chapter 14). However, TiN does not produce good contact resistance to silicon. To resolve this problem, a thin layer of titanium (e.g., several hundred angstroms or less) is typically deposited before the TiN so that it can react with the underlying material as a silicide (see the following section for an explanation of silicide) and lower the contact resistance. The Ti and TiN are typically deposited in a cluster tool to keep oxides from forming between the two layers.

Copper Barrier Metals ■ Barrier metals are critical for copper metallurgy. Cu has high diffusivity in silicon and silicon dioxide, which will destroy device performance. Traditional barrier metals are not sufficient barriers for copper. Cu requires complete encapsulation by a thin-film barrier layer that functions as an adhesion promoter and effective diffusion barrier.[23] There is a trade-off between these two requirements since good adhesion requires some reaction with Cu, whereas a good barrier metal should not react with Cu. The special barrier metal requirements for copper are:[24]

1. Prevent copper diffusion.
2. Low film resistivity.
3. Good adhesion to both dielectric material and copper.
4. Compatible with chemical mechanical planarization (CMP).
5. Metal layer is continuous and conformal with good step coverage and deposition in high aspect ratio gaps.
6. Minimal thickness to allow the copper to occupy the maximum cross-sectional area.

For Cu interconnect metallurgy, tantalum (Ta), tantalum nitride (TaN), and tantalum silicon nitride (TaSiN) are candidate materials for barrier metals (see Figure 12.8). The diffusion barrier must remain thin (about 75 Å) so that it does not affect the resistivity of the high-aspect ratio plug while still acting as a barrier metal. This condition is difficult to maintain as geometries continue to shrink and metals are deposited into high-aspect ratio vias. Research has shown Ta has good barrier and adhesion properties for copper, whereas TiN, a traditional barrier metal for Al/SiO_2 interconnects, has good barrier properties but poorer adhesion.[25] If TaN is used, it is obtained by small amounts of nitrogen doping or by deposition with a tantalum nitride compound. Investigations have also shown tungsten nitride (WN) functions as an effective barrier for Cu metal.[26] There is ongoing research in the development of barrier metals for Cu metallurgy.

Copper barrier layers can be deposited by using high-density plasma CVD (HDPCVD) or ionized metal plasma physical vapor deposition. Ionized metal plasma PVD for tantalum achieves good step coverage. For deposition with high aspect ratio gaps, then HDPCVD barrier deposition is often the choice.[27]

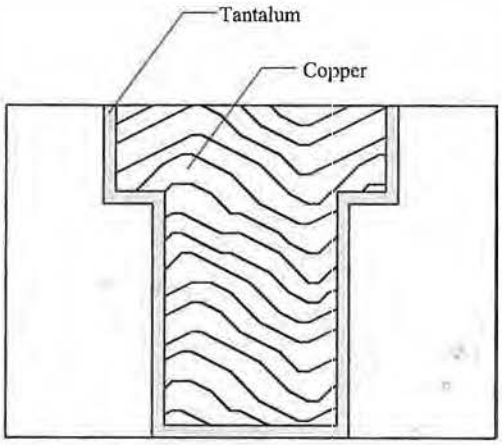


FIGURE 12.8 Ta for Copper Barrier Metal

Silicides

Refractory metals react with silicon when alloyed together to form a silicide. A *silicide* is a metal compound that is thermally stable and provides for low electrical resistivity at the silicon/refractory metal interface (see Figure 12.9). Refractory metal silicides are important in wafer fabrication because of the need to reduce the electrical resistance of the many silicon contacts in the source/drain and gate regions for chip performance. Titanium and cobalt are common refractory metal used for contacts in aluminum interconnect technology.

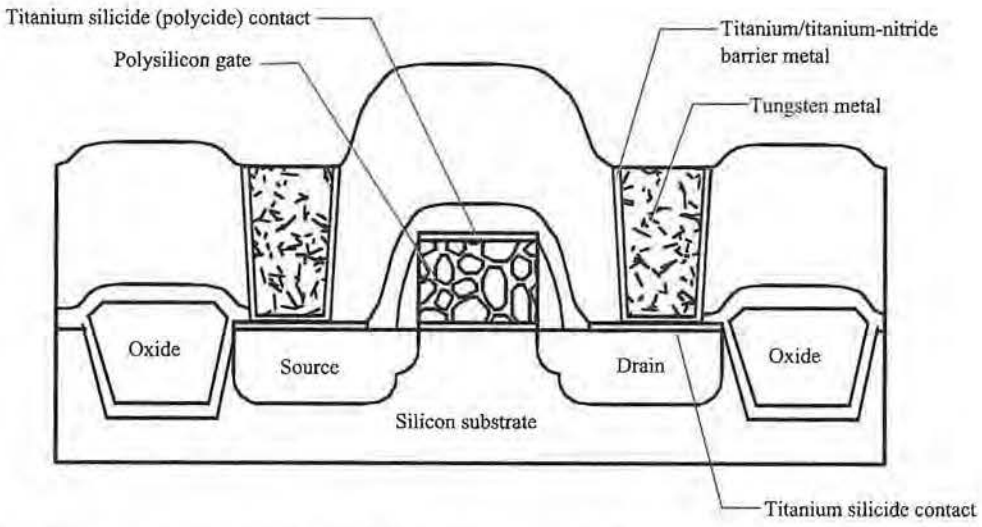


FIGURE 12.9 Refractory Metal Silicide at a Silicon Contact

If the refractory metal is reacted with polysilicon, it is called a *polycide* (see Figure 12.10 on page 310). Doped polysilicon is used as the gate electrode and has a relatively high resistivity (about 500 $\mu\Omega$-cm), which leads to an undesirable RC signal delay. A polycide is beneficial for reducing the series resistance of an interconnection to polysilicon. At the same time, it maintains polysilicon's good interfacial characteristics to oxides.

Silicides improve contact resistance by reducing residual oxides on the silicon surface during silicide formation. Silicides form extremely good metallurgic contact to the silicon, serving as a critical adhesion layer between the contact metal and the silicon junction regions. Many silicides are stable at temperatures exceeding 1000°C with a relatively high eutectic temperature. Table 12.4 on page 310 lists some properties of common silicides used in wafer fabrication.[28] Recall that the eutectic temperature is the lowest temperature where the alloy melts. It is undesirable for the silicide to melt because the liquid alloy can extend into the substrate material and cause junction spiking.

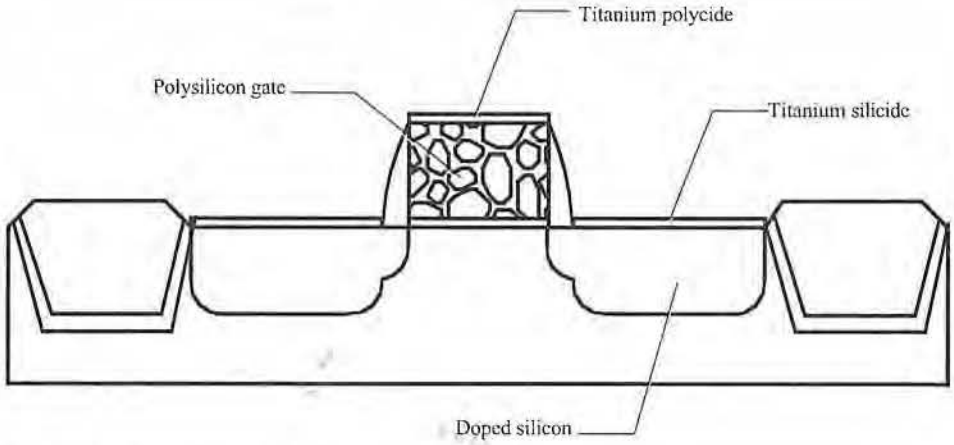


FIGURE 12.10 Polycide on Polysilicon

TABLE 12.4 Some Properties of Select Silicides

Silicide	Lowest Eutectic Temperature (°C)	Typical Forming Temperature* (°C)	Resistivity (μΩ-cm)
Cobalt/silicon ($CoSi_2$)	900	550–700	13–19
Molybdenum/silicon ($MoSi_2$)	1410	900–1100	40–70
Platinum/silicon (PtSi)	830	700–800	28–35
Tantalum/silicon ($TaSi_2$)	1385	900–1100	35–55
Titanium/silicon ($TiSi_2$)	1330	600–800	13–17
Tungsten/silicon (WSi_2)	1440	900–1100	31

* B. El-Kareh, *Fundamentals of Semiconductor Processing Technologies.* (Boston: Kluwer Academic Publishing 1995), p. 537.

Silicide formation typically requires the refractory metal be deposited on the silicon wafer, followed by a high temperature thermal anneal process to produce the silicide material. In areas where there is silicon, the metal reacts to form a silicide. In other areas on the wafer surface, such as where there is SiO_2, there is little or no silicide formation. Often this thermal anneal step uses a rapid thermal anneal (RTA) process in a multichamber cluster tool.

$TiSi_2$ has traditionally been the most common contact silicide for wafer fabrication, serving as the contact between the transistor active regions of silicon and the tungsten plug. It is often referred to as the glue that holds the tungsten to the silicon. Its beneficial properties are high temperature stability, compatibility with self-aligned contact processing (discussed in the following section), low resistivity when compared to other silicides, and its compatibility with TiN barrier metals.[29] $TiSi_2$ forms two different grain phases (a phase is a physically homogeneous material state) as it is annealed, a low-temperature C49 phase and a high-temperature C54 phase (see Figure 12.11). Both of these phases are $TiSi_2$.

The C49 phase of $TiSi_2$ forms at an anneal temperature of 625 to 675°C with a resistivity of 60 to 65 μΩ-cm. The C54 phase is formed in a second anneal following the C49 phase formation and requires a temperature of 800°C or more. It has a much lower resistivity of only 10 to 15 μΩ-cm, which is desirable to lower the overall contact resistance.[30]

However, at the time of this writing, $TiSi_2$ appears limited in its future use as a contact silicide in sub-0.25 μm technologies. Contacts for ultrashallow source/drain junctions are becoming thin. $TiSi_2$ is undesirable for thin contacts because the silicide resistivity increases.[31] It is also difficult to form this contact during the second anneal because of critical time at temperature requirements.

The silicide that appears promising for the 0.18 μm and below technology nodes is cobalt silicide ($CoSi_2$). This silicide maintains a reduced contact resistance of 13 to 19 μΩ-cm after its

	Sintering Temperature	Resistivity
$TiSi_2$ – C49	625 – 675°C	60 – 65 μΩ-cm
$TiSi_2$ – C54	800°C	10 – 15 μΩ-cm

FIGURE 12.11 Anneal Phases of $TiSi_2$

anneal operation, even with deep submicron geometries of 0.18 μm and less. This reduced resistivity occurs because the grain size of $CoSi_2$ is about ten times smaller than the grain size of $TiSi_2$. Therefore, the low resistance phase is completely nucleated and grown during the thermal anneal operation. A $CoSi_2$ contact is also easier to form because of the smaller grain size.

Note that a silicide is not a barrier metal. In some silicides it is found that silicon diffuses rapidly through them. This diffusion occurs during heat treatment of the metal-silicide-silicon system where silicon diffuses through the silicide to the metal, which then reduces the integrity of the system. The solution to this problem is to place a metal barrier layer between the silicide and the metallization layer (discussed in the preceding section). A common silicide barrier film is titanium nitride (TiN), which is effective for both tungsten and aluminum. A tantalum-based barrier layer is anticipated for copper metallurgy.

Salicide ■ Because of the need to scale device sizes in VLSI and ULSI to optimize performance, the cross-sectional area of the source/drain (S/D) contact between the silicon and the first metal layer is small. This small size leads to increased resistance. A technique to decrease contact resistance at the source and drain areas by providing stable contact structures is referred to as a salicide. A *salicide* approach (taken from the expression *self-aligned silicide*) is used to create silicides that are properly aligned with the exposed silicon of the source, drain, and polysilicon gate. There are numerous chip performance issues that depend on salicide formation (see Figure 12.12).

The basic salicide steps are shown in Figure 12.13 on page 312. This process flow corresponds to Step 6 of the CMOS process flow described in Chapter 9. To form a salicide, oxide has been previously deposited and etched back with a dry plasma etch to leave oxide sidewall spacers

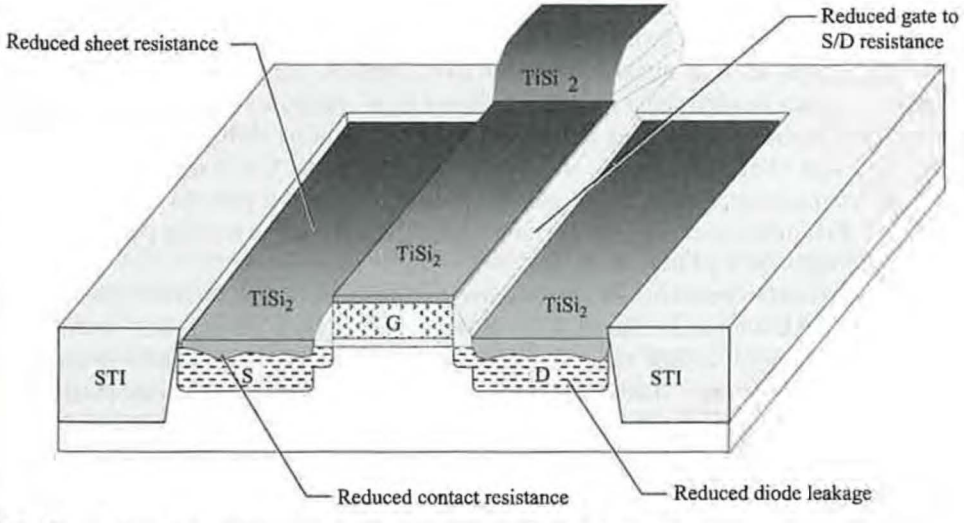


FIGURE 12.12 Chip Performance Issues Related to a Salicide Structure

on the side of the polysilicon gate (Step 5 of the CMOS process flow described in Chapter 9). With the sidewall spacers, only the top poly surface of the gate is exposed. After an HF-dip clean step to remove native oxides, a 250 to 350 Å thin layer of titanium metal is deposited on the wafer. The refractory metal undergoes an RTP rapid anneal at 600 to 800°C to create the high-resistivity C49 titanium silicide phase wherever the refractory metal contacts silicon. The sidewall spacer keeps the S/D $TiSi_2$ from shorting out to the sides of the gate poly, while the oxide of the shallow trench isolation separates the devices. After the first RTP anneal, all unreacted titanium is removed by a wet chemical etch in ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2). $TiSi_2$ remains and covers the S/D areas and top surface of the poly gate. A second RTP silicide anneal at 800 to 900°C creates the low-resistivity C54 metallic silicide. A major benefit of the salicide process is the avoidance of alignment tolerances that would occur if patterning were required to align the refractory metal on the silicon contact. Care must be taken during the anneal steps to avoid oxygen contamination in the furnace tube. Titanium reacts easily with oxygen to form undesirable titanium oxides. This oxide contamination can promote silicide formation on top of the oxide spacer regions, leading to a short between the polysilicon gate and source or drain.

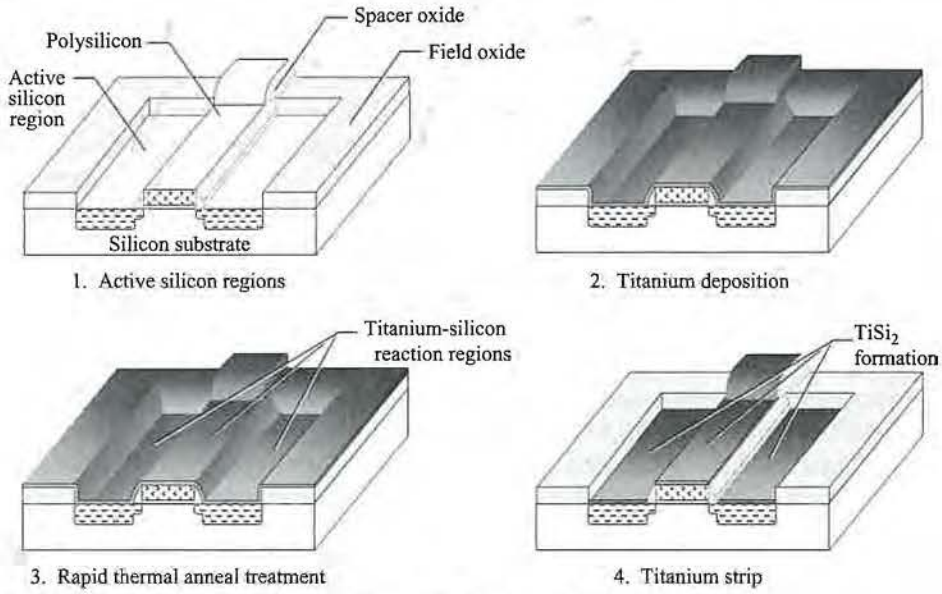


FIGURE 12.13 Formation of Self-Aligned Metal Silicide (Salicide)

Metal Plugs

Multilevel metallization creates the need for billions of vias filled with metal plugs to form electrical pathways between two metal layers. A contact plug is also used to connect the silicon devices in the wafer to the first level of metallization. The most common metal currently used for plugs is tungsten (W), which is why plugs are often referred to as *tungsten plugs* (see Figure 12.14). Tungsten has been traditionally used as a plug material because of its ability to uniformly fill the high-aspect ratio vias when deposited by chemical vapor deposition (CVD) methods. Tungsten is resistant to electromigration failure. It also serves as a barrier to inhibit diffusion and reaction between Si and the first metal layer. Tungsten is a refractory material with a melting point of 3,417°C and a bulk resistivity of 52.8 μΩ-cm at 20°C.

Aluminum would be desirable as a plug material because of its lower resistivity (2.65 μΩ-cm at 20°C), but sputtered aluminum cannot fill high-aspect ratio vias (see the next section for a description of sputtering). For this reason aluminum is used as the interconnect material and tungsten is limited to the plug. There has been recent interest in reflow aluminum plugs, where aluminum is sputter deposited into the via and then reflowed by a high-temperature anneal with a rapid thermal processor (RTP).[32]

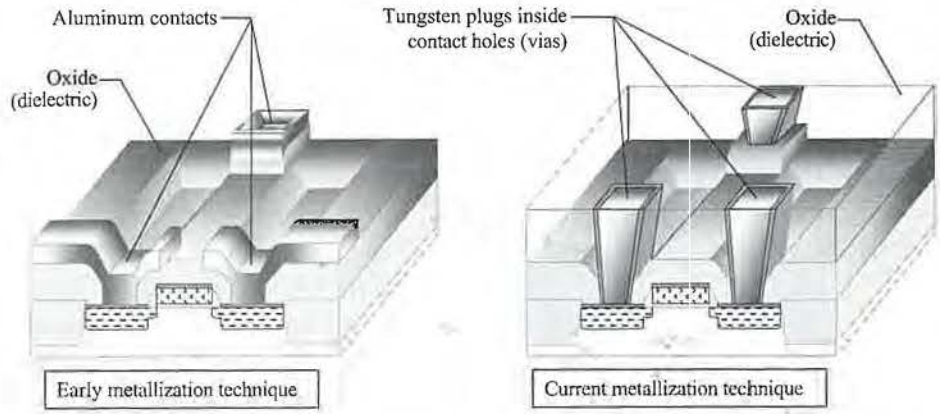


FIGURE 12.14 Tungsten Plug for Multilevel Metal Layers

METAL DEPOSITION SYSTEMS

The traditional metallization techniques used in semiconductor manufacturing fall under a category called *physical vapor deposition* (*PVD*). PVD has been done with filament evaporation, followed by electron beam evaporation and, most recently, sputtering. Chemical vapor deposition (CVD) has recently become a frequently used technique to deposit metal films. Each change in the deposition system has brought improved control of thin film properties and quality.

During the SSI and MSI eras of semiconductor manufacturing, evaporation was the method for metallization. It was replaced by sputtering primarily because evaporation has poor step coverage. Evaporation is still used in research applications and for semiconductors using III–V technologies. It is also used in some specialized areas, such as for C4 bump deposition during packaging (see Chapter 20).

Electroplating technology has been employed in various applications. In recent years it has been used for thin film head metallization in the disk drive industry. However, electroplating is just now being introduced for semiconductor manufacturing as a copper deposition method. It is the early deposition method of choice for creating copper interconnects.

The different metal deposition systems used in traditional and dual damascene metallization are:

- Evaporation
- Sputtering
- Metal CVD
- Copper electroplate

Evaporation

In the early days of semiconductor manufacturing, all metal layers were deposited by the PVD method of *evaporation*. Since the late 1970s, sputtering has replaced evaporation in most silicon wafer technologies in order to gain improved step coverage, gap fill, and yield. It is beneficial to review evaporation to understand how it functions and why the silicon industry changed to sputtering.

The process of evaporation consists of placing the material to be deposited in a crucible and heating it inside a vacuum chamber until it vaporizes (see Figure 12.15 on page 314). The most typical method of heating was the use of an electron beam to heat the metal placed in a crucible. By maintaining a high vacuum in the evaporator, the mean free path of the vapor molecules is increased, and the vapor travels in a straight line in the chamber until it strikes a surface and condenses to form a film.

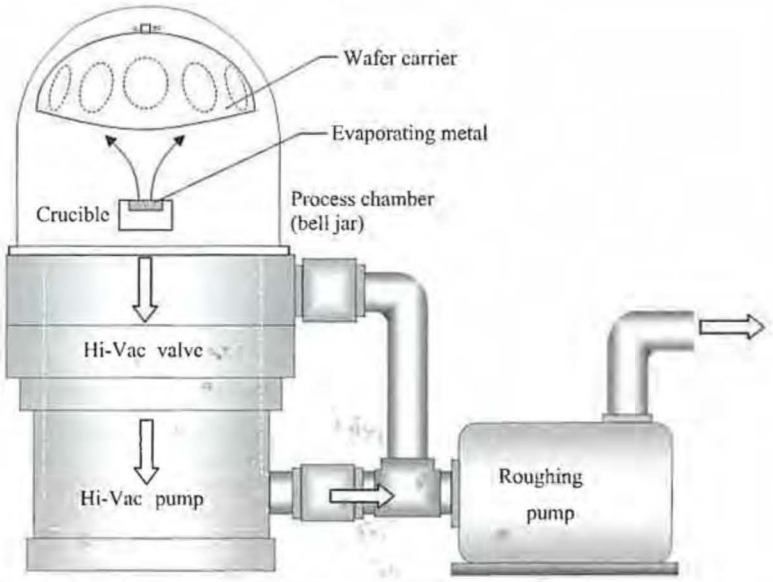


FIGURE 12.15 Simple Evaporator

The biggest drawback to evaporation was the inability to produce uniform step coverage. As the industry progressed to VLSI and ULSI technology, metallization needed to be capable of filling higher aspect ratio holes and producing conformal step coverage. Evaporators made some progress for step coverage by heating the wafers and rotating the wafers in the chamber with a hemispherical cage. However, evaporator technology is not able to form a continuous film over features with an aspect ratio greater than 1.0:1, and is marginal for an aspect ratio of 0.5:1 to 1.0:1. This drawback to evaporation led to its demise in IC production.

Another serious drawback of evaporation is its limitation for depositing alloys. The evaporator requires multiple crucibles for the different materials, which is a problem because of the different vapor pressures of the materials. This limitation makes it difficult to control the ultimate composition of the deposited alloy with any degree of accuracy.

Ultimately, the wafer fabrication industry quickly replaced evaporators with sputtering systems due to their improved step coverage capability. The evaporator is still used in research applications and for some compound semiconductor technologies that can actually use the poor step coverage of evaporators to their advantage during specialized processing. In addition, evaporators are still sometimes used in the chip packaging process to deposit solder bumps on the chip surface (see Chapter 20).

Sputtering

Sputtering, a form of physical vapor deposition (PVD), was discovered in 1852 by Sir William Robert Grove and developed as a thin film deposition technique in the 1920s by Langmuir.[33] As its name implies, sputtering is mainly a physical, rather than chemical, process. In the sputtering process, high-energy particles strike a solid slab of high-purity target material and physically dislodge atoms. These sputtered atoms migrate through a vacuum and eventually deposit on a wafer.

The advantages of sputtering are:[34]

1. Ability to deposit and maintain complex alloys.
2. Capability to deposit high-temperature and refractory metals.
3. Ability to deposit controlled, uniform films on large wafers (200 mm and larger).
4. Capability of multichamber cluster tools to clean the wafer surface for contamination and native oxides before depositing metal (referred to as *in situ sputter etch*).

While sputtering was a big improvement in gap fill over the earlier metallization method of evaporation, its limited capability for step coverage and filling high-aspect ratio gaps makes it insufficient for ULSI applications.[35] Over the years, improvements have been made to the sputtering

process to obtain better step coverage, including recent advances with ionized metal plasma PVD. For critical applications, such as the step coverage in tungsten plugs, deposition will usually be done with a CVD metal process. Sputtering continues to be used for depositing critical barrier and seed layers, such as tantalum/tantalum nitride used in copper metallization (when the aspect ratio is reasonable).

Basic Sputtering Steps ■ There are six basic steps to sputtering:[36]

1. Positive argon ions are generated in a plasma in a high vacuum chamber and accelerated toward a target material at a negative potential.
2. During acceleration, the ions gain momentum and strike the target.
3. The ions physically dislodge (sputter) atoms from the target, which has the desired material composition.
4. The dislodged (sputtered) atoms migrate to the wafer surface.
5. The sputtered atoms condense and form a thin film on the wafer surface with essentially the same material composition as the target, following the stages for thin film growth outlined in Chapter 11.
6. Excess material is removed from the chamber by vacuum pump.

To illustrate sputtering, Figure 12.16 shows the basic configuration of a simple, DC diode sputter deposition chamber with parallel plates. It consists of the solid *target* material, a substrate (wafer), and a vacuum enclosure. The target is electrically grounded and referred to as the *cathode,* while the substrate has a positive potential and is termed the *anode.* The anode and cathode are both called *electrodes.* The sputtering target is composed of the necessary material for deposition. Targets are manufactured to achieve a homogeneous composition, fine grain size, and specific crystallographic orientation, all of which contribute to achieving a uniform film deposition rate across the wafer.[37] Target purity levels of 99.999% (5 nines) or better are required for achieving acceptable film purity for sub-0.25 μm geometries.

A high density of positive ions from an argon gas glow discharge is strongly attracted to the negative target material, striking it at high velocity and dislodging the atoms to be deposited. The atoms are sputtered (knocked off) from the target material and scatter in the chamber; eventually some come to rest on the wafer or the chamber walls. This action necessitates cleaning of the chamber in some systems. The atoms on the wafer nucleate and grow a thin film. An important aspect of sputtering is that this process can be used to sputter-deposit alloys, in particular aluminum-silicon

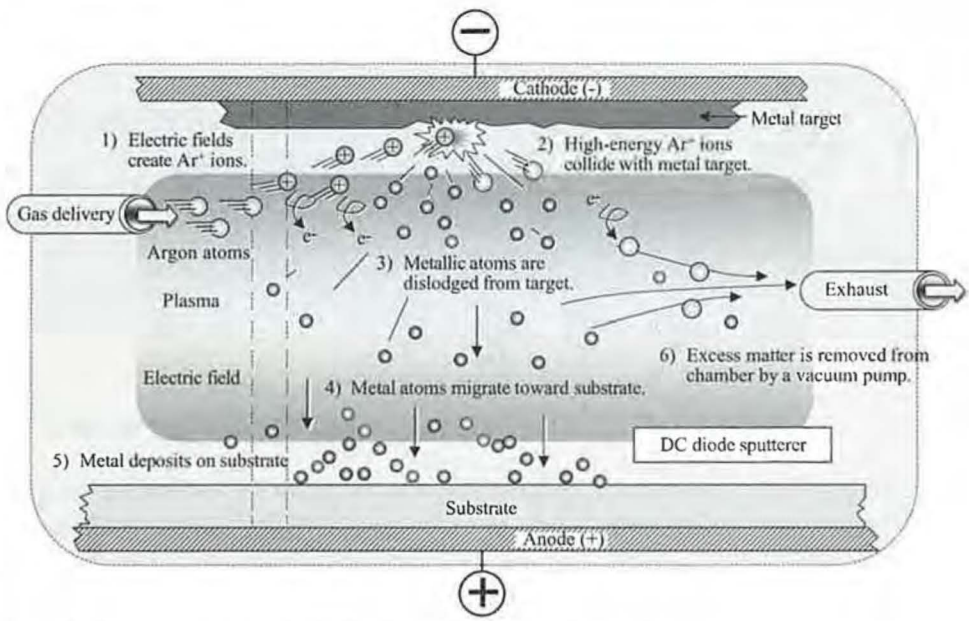


FIGURE 12.16 Simple Parallel Plate DC Diode Sputtering System

and aluminum-copper alloys. For instance, if the target material is aluminum with 1% copper, then the deposited film will be aluminum with 1% copper (at steady-state conditions).

The latest technology of sputtering equipment systems are multichamber cluster tools. The system has a loadlock that moves single wafers from the wafer cassette to its ultimate base vacuum pressure. The loadlock may consist of dual loadlocks to move the wafer through a staged vacuum sequence from ambient atmosphere to base vacuum pressure. A robot transfer system designed specifically for the cluster tool environment moves wafers from the various process chambers and a buffer chamber. It is important that the robot operate without generating particles and be extremely reliable. Cluster tool robots are often magnetically coupled, which permits the robot drive motor to remain on the outside of the process chambers to reduce particles.

Vacuum conditions are important in the sputtering chamber to create the plasma and maintain purity of the deposited films, with base vacuum typically at 10^{-7} torr during initial pump down. The rate that argon gas enters the process chamber is critical because it causes the pressure to rise in the chamber. With the argon and sputtered material in the chamber, the pressure rises to about 10^{-3} torr. The hot, high-vacuum environment of the process chamber promotes the formation of the sputtered atoms into thin films on the wafer surface.

Physics of Sputtering ■ An essential aspect of sputtering is the formation of the ionized argon gas into a plasma (see Chapter 8). Argon is used as the sputtering ion species because it is relatively heavy and is a chemically inert gas, which keeps it from reacting with the growing film or the target. If a high-energy electron strikes the neutral argon, the collision knocks off outer electrons and creates a positively charged argon ion. This energetic particle is used to strike the negatively charged target material to be sputtered.

Sputtering Mechanism. Positively charged argon ions in the plasma are strongly attracted to the negative potential of the cathode target. The charged ions accelerate and acquire kinetic energy (or energy of motion) as they pass through the voltage drop of the glow-discharge dark space (see Chapter 8 for a description of glow discharge). When the Ar ions strike the target surface, the momentum of the Ar ion transfers to the target material to dislodge one or more atoms. This action is referred to as *momentum transfer.* The ejected neutral atom or atoms move through the plasma (with a small chance of being ionized) and land on the wafer. The incident ion energy must be large enough to dislodge target atoms but not so large that the ion penetrates into the target material. Typical sputtering ion energies range from 500 to 5,000 eV.

An analogy for dislodging metal atoms from the surface of the target material during sputtering is hitting billiard balls in a pool game. Even though the cue ball in pool is travelling in one direction, the billiard balls can be knocked in some other direction. This same effect occurs in sputtering, where the argon ion impacts the target and dislodges one or more atoms from the surface of the target (see Figure 12.17).

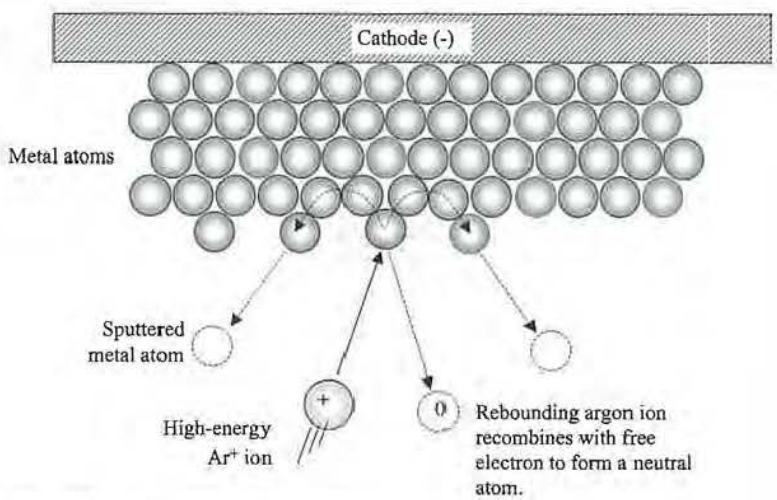


FIGURE 12.17 Dislodging Metal Atoms from Surface of Sputtering Target

The *sputtering yield* is defined as the number of atoms ejected by the target (cathode) per incident ion that strikes it. The yield largely determines the rate of sputter deposition. It varies from about 0.5 to 1.5. A sputter yield of 0.5 means that, on the average, two ions must strike the target for one atom to be ejected. The sputter yield depends on the following conditions:[38]

1. Incident angle of the bombarding ions.
2. Composition and geometry of the target material.
3. Mass of bombarding ions.
4. Energy of the bombarding ions.

A method of increasing the sputtering deposition rate is to confine the plasma to the region between the target and wafers. Due to the ionization process, there are dark spaces just to the front and the sides of the target. Dark space shields are placed on the sides of the target to prevent target material from being sputtered on the sides, since this material will never deposit on the wafers. Shields require periodic changing because sputtered target material builds up on the surface and causes particulate contamination.

Targets undergo erosion from the ion bombardment and are replaced when about 50% or more of the target material is removed.[39] Much of the energy consumed during the sputtering process is dissipated as heat in the target, or by emission of secondary electrons and photons by the target. For this reason, cooling of the target material is done to maintain a low target temperature.

In addition to being struck by the sputtered atoms, the substrate has other species landing on it (see Figure 12.18). These species cause heating of the substrate (up to 350°C) which leads to uneven film deposition. The high temperature can also create an undesirable aluminum oxide during aluminum deposition, which interferes with the sputtering process. The many species impinging on the wafer surface during diode sputtering also increase the possibility of damage due to radiation to sensitive devices.

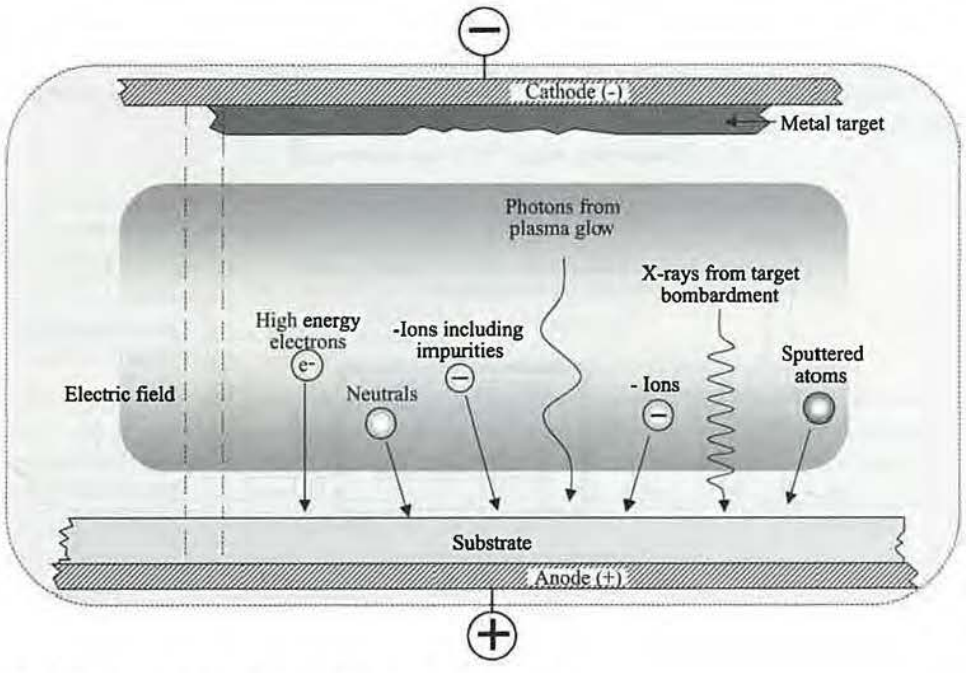


FIGURE 12.18 Different Species Landing on Substrate

Note the presence of the impurity gas atoms during diode sputtering. This is a problem if the impurity atoms are incorporated into the growing film on the substrate. The sources of contaminants are: (1) impure sputtering gas, (2) outgassing from the wafer holder, (3) outgassing from chamber walls, and (4) vacuum leaks.[40] It is necessary to use ultrahigh purity (UHP) sputter gases and to verify there are no chamber leaks.

The spacing between the cathode and anode must be optimized for each sputtering system. The goal is to have as many sputtered atoms as possible be deposited on the wafers and form the desired film.

The sputtering system described thus far is a simple DC diode system that has a DC voltage applied between two electrodes (cathode and anode). The DC diode sputtering system has serious drawbacks that limit its use in manufacturing. A DC diode type sputtering system cannot be used to sputter dielectrics because the electrodes become coated with the dielectric and the glow discharge cannot be sustained. The target rapidly builds up a positive charge, which repels incoming positive ions. DC diode type sputtering is also not capable of performing a sputter etch. *Sputter etch* (or *reverse sputter*) is a preclean step where the sputter process is reversed and argon atoms are used to remove thin native-oxide layers and remaining etch residues that contaminate contacts and vias. In other words, the wafer is sputtered instead of the target. This sputter etch preclean is important in multichamber cluster tools because of the benefit of cleaning followed by deposition without removing the wafer from the vacuum environment.

Three types of sputtering systems are covered in the following pages:

- RF (radio frequency)
- Magnetron
- IMP (ionized metal plasma)

The simple RF sputter system is not used in wafer fabrication because of its inherent inefficiency. The magnetron has traditionally been the most widely used sputter system, and ionized metal plasma (IMP) is becoming more common for sub-0.25 micron technology.

RF Sputtering ■ In an *RF sputtering* system, an RF field is used to create the plasma instead of the DC field described above. The RF frequency has commonly been 13.56 MHz. It is applied to the back surface of the target electrode and capacitively coupled to its front surface (see Figure 12.19). Both the electrons and ions in the plasma are exposed to the RF field, but due to the high frequency, the electrons respond most strongly. The chamber and electrode behave like a diode, creating a high amount of electron flow and resulting in a negative charge on the target electrode. This negative charge (produced by a self-bias) attracts positive argon ions, which sputter material from the insulator or non-insulator target.[41]

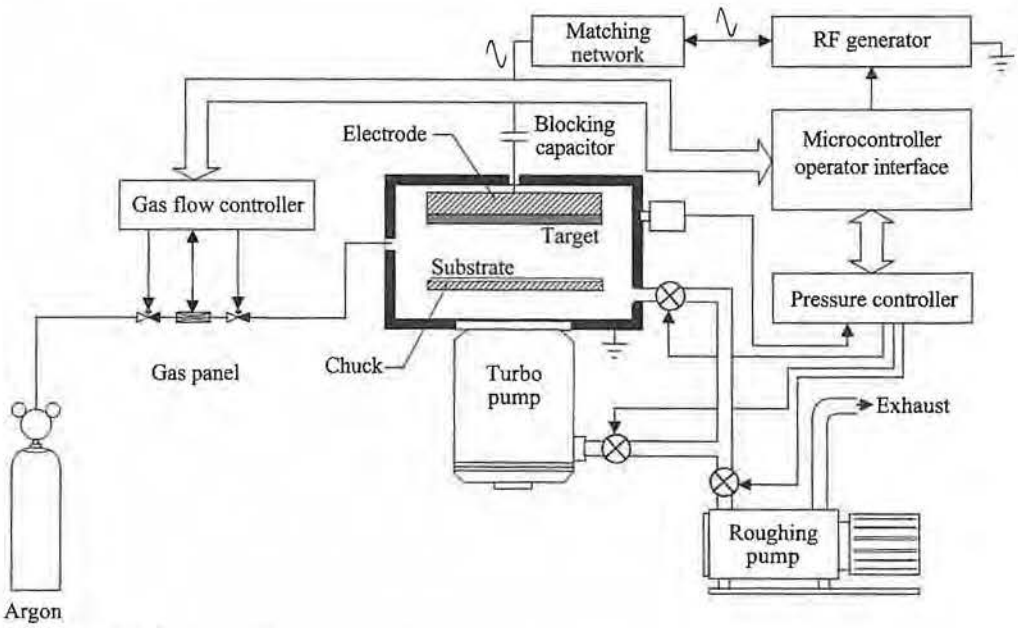


FIGURE 12.19 RF Sputtering System

The wafer can be electrically biased to put it at a different field potential than the argon. The bias applied to the wafer causes the argon atoms to strike the wafer directly. This RF biasing permits the exposed wafer surface to be sputter etched and cleaned.

In practice, an RF sputtering system is limited because it does not have a high sputtering yield, leading to a low deposition rate. Many of the secondary electrons emitted by the target pass through the discharge region without contributing to the creation of plasma. The sputtering rate of the target would be much higher if these secondary electrons were involved in ion collisions, leading to the creation of more ions to bombard the target. To overcome this inefficiency and to achieve high metal deposition rates necessary for wafer fabrication, the concept of magnetron sputtering was developed.

Magnetron Sputtering ■ *Magnetron sputtering* employs magnets configured around and behind the target to capture and restrict the electrons in front of the target (see Figure 12.20). This setup increases the ion bombardment rate on the target in order to produce more secondary electrons, which then increases the ionization rate in the plasma. The end result is that more ions cause more sputtering of the target, which increases the deposition rate of the system. The invention of magnetron sputtering to improve the deposition rate is one of the main reasons why sputtering has become the leading process for single-wafer deposition systems for aluminum and contact alloys used in metallization.

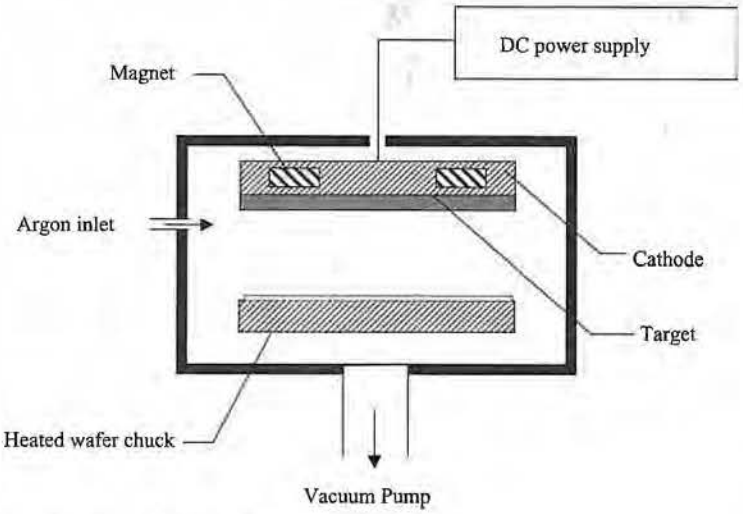


FIGURE 12.20 Magnetron Sputtering

The magnetron sputtering design requires a substantial amount of power supplied to the argon plasma to maximize the sputtering rate (about 3kW to 20 kW of power). Because the sputtering target absorbs most of this power and is in contact with the cathode, cooling of the cathode is required. An important challenge is uniformity of the sputtered deposit on large wafers. To achieve high deposition rates and film uniformity in single-wafer cluster tools, new cathodes have been developed with rotating, rare earth, high-strength permanent magnets.[42]

Step Coverage. Sputtering requires a vacuum environment with high-purity argon to avoid contamination from residual gas. The vacuum during the sputtering process is around 1 mtorr, with a mean free path of several centimeters. This is approximately the distance between the target and wafer. Because of this distance, atoms dislodged from the target essentially pass on to the wafer by following a line-of-sight path.

This line-of-sight path for the ejected atoms exiting at many different angles from the target causes poor coverage on steps and sidewalls in contacts and vias. Due to their geometry, the sidewalls and bottoms of high-aspect ratio contact windows and vias will receive only 10% or less of the metal deposited on the top surface.[43] For this reason PVD is not usually chosen when depositing a material on high aspect ratio steps and trenches.

Collimated Sputtering. To achieve increased coverage on the bottom and side of a contact or via, directional enhancement can be achieved by the use of *collimated sputtering* (see Figure 12.21). The collimator is configured so that it appears as the electrical ground for the plasma. In this manner, any neutral species sputtered from the target at a high angle is intercepted and deposited on the collimator. Other atoms that are ejected straight back from the target will pass by the collimator and deposit on the bottom of the contact hole. At the same time, a collimator reduces sidewall coverage in the contact or via.

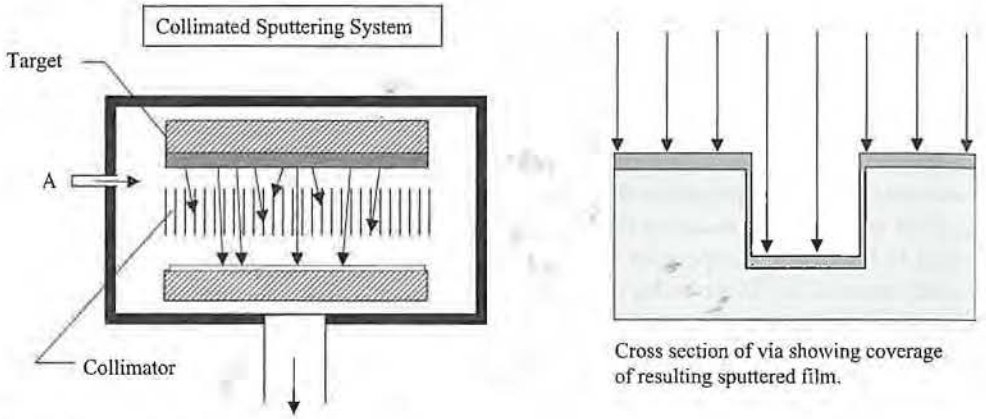


FIGURE 12.21 Collimated Sputtering

The use of a collimator means that a large portion of the sputtered material will not reach the wafer, since most of the sputtered material ends up on the collimator. This result lowers the sputter yield and increases the cost of deposition, since fewer sputtered atoms reach the wafer. At the same time, maintenance costs increase because the target is less efficient. Given these problems, it is more efficient to use ionized metal plasma (IMP) or CVD deposition over magnetron sputtering if step coverage is a critical factor.

Ionized Metal Plasma (IMP) ■ A problem for sputtering technology in wafer fabrication for high performance ICs is that as feature sizes shrink, the capability to sputter into high aspect ratio vias and narrow trenches becomes limited. A recent development in PVD to overcome this problem is *ionized metal plasma PVD (IMP* or *ionized PVD),* which was introduced in the mid-1990s. In this approach, the sputtered metal is ionized in an RF plasma at a pressure of 20 to 40 mtorr (see Figure 12.22). The positive metal ions then travel in a highly directional, vertical path toward a wafer configured with a negative voltage bias. This voltage bias can also be used to control the energy of the incoming metal ions, which helps reduce damage to the surface of the wafer.[44] Biasing the wafer enables a higher degree of film conformality in the bottom and corners of high aspect ratio gaps.

Ionized PVD achieves good hole-fill for Ti and TiN on structures with 0.25-micron contacts and vias and 6:1 aspect ratios, with 70% bottom coverage, 10% sidewall coverage, and excellent sidewall integrity. This coverage is critical in the bottom, bottom corner, and lower sidewall areas of holes with a typical 85° sidewall angle.

Ionized PVD is used in production to deposit titanium and titanium nitride barrier films for devices at the 0.25 μm and below generations with high-aspect ratio contact and via structures.[45] It is also capable of depositing tantalum, tantalum nitride, and copper, which are important metals for copper metallization. The development of ionized PVD has further improved sputtering to extend its usefulness in high-aspect ratio gap fill.

Metal CVD

The use of chemical vapor deposition (CVD) for metal deposition is increasing because of its superior conformal step coverage and void-free filling of high-aspect ratio contacts and vias. These factors are critical for wafer fabrication as feature sizes decrease to the 0.15-μm generation and

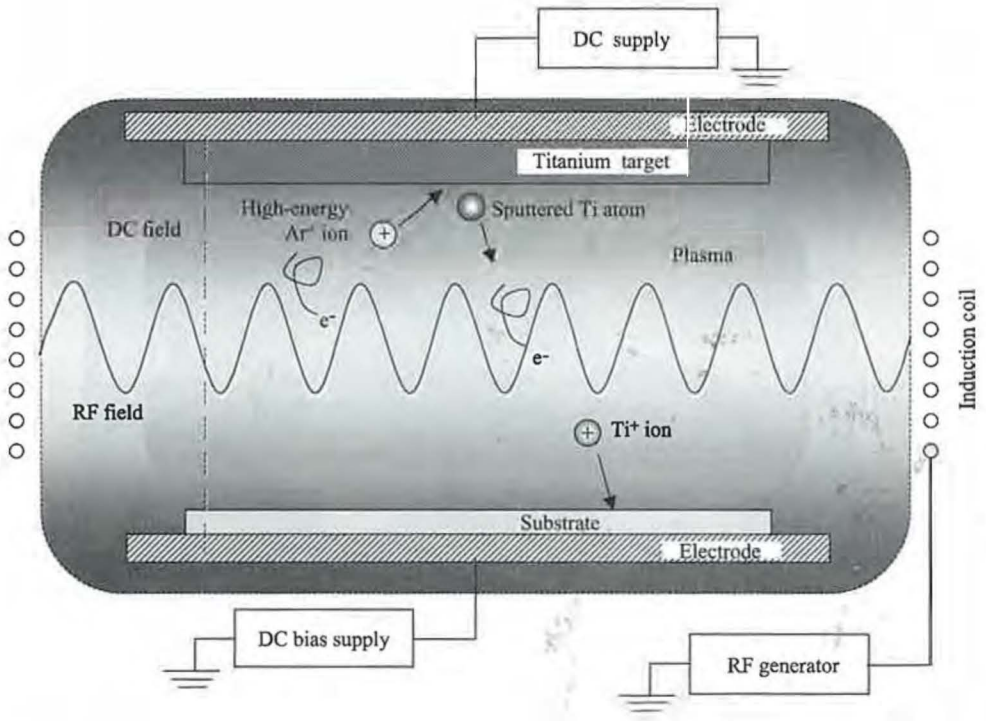


FIGURE 12.22 Concept of Ionized Metal Plasma PVD

beyond. The projected aspect ratio for vias in DRAM memory is projected to be 7:1 for the 0.15-μm generation, and 2.4:1 for logic.[46]

Tungsten CVD ■ *Tungsten (W) CVD* is used in multilevel interconnection technology as the process to deposit the via plug and to act as the contact plug between the first metal layer and the silicide contact. Tungsten CVD is also used as the local interconnect (LI) because of its low resistivity. Tungsten has performed reliably, with billions of W CVD plugs used on one microchip. However, its usefulness as a vertical interconnect may be limited with the introduction of the new damascene copper metallization scheme.

Tungsten CVD is common as a plug material due to:

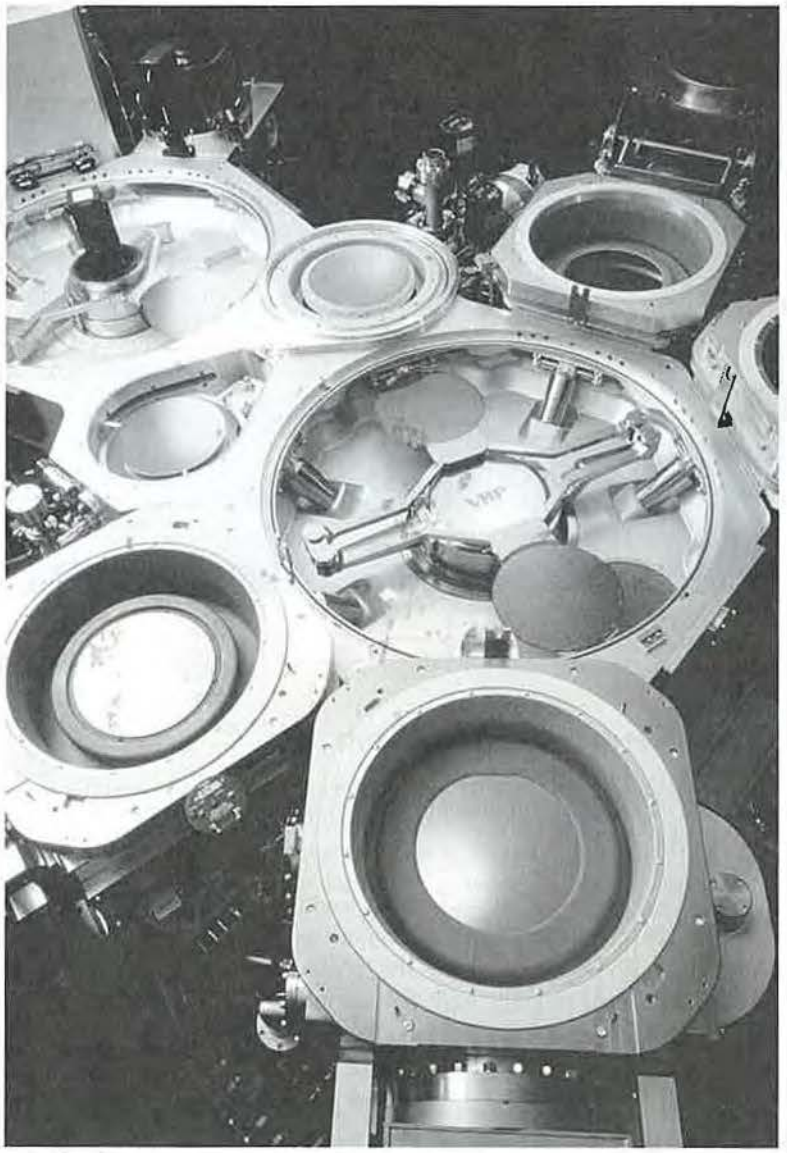
1. Excellent step coverage and gap-fill, particularly in high-aspect ratio vias.
2. High electromigration resistance.

Low-pressure CVD (LPCVD) is the usual method for depositing W plugs, along with plasma-enhanced CVD (PECVD). Reactors are both hot- and cold-wall and configured as batch or multichamber cluster tools. The most common source gas for W is WF_6.[47] Sputtering costs less to operate than CVD for W deposition but has traditionally poorer directional control. This coverage produces nonuniform tungsten deposition quality in vias, which is why CVD has been the preferred method. This may change with the recent development of ionized PVD.

Tungsten CVD is typically deposited in blanket films. Blanket deposition deposits tungsten nonselectively on the entire wafer surface, including the via pathways, and is the most common approach.

Blanket Tungsten CVD Deposition. Blanket tungsten deposition followed by chemical mechanical planarization (CMP) is the common method used to fill vias to connect between metal layers. As always in CVD, the properties of the film deposited with CVD depend on the chemical reactions that occur at the wafer's surface. For blanket tungsten CVD, the most frequently used reaction is the reduction of tungsten hexafluoride (WF_6) by hydrogen to produce tungsten and hydrogen fluoride:

$$\underset{\textit{tungsten hexafluoride}}{WF_6\ (\text{gas})} + \underset{\textit{hydrogen}}{3H_2\ (\text{gas})} \rightarrow \underset{\textit{tungsten}}{W\ (\text{solid})} + \underset{\textit{hydrogen fluoride}}{6HF\ (\text{gas})}$$



PVD Cluster Tool
(Photo courtesy of Applied Materials, Inc.)

Typically the first step in blanket tungsten CVD is to deposit a titanium/titanium nitride (Ti/TiN) barrier layer (see Figure 12.23). The Ti is deposited before TiN to react with the underlying material and lower the contact resistance. If this is a contact in the first interlayer dielectric (ILD-1), then Ti reacts with silicon to form $TiSi_2$ silicide. The TiN functions as a barrier metal and adhesion promoter (glue layer) for tungsten. It needs a minimum bottom thickness of about 50 Å with continuous sidewall coverage to be an effective barrier metal and keep the tungsten from attacking underlying layers.[48] The Ti/TiN barrier layer may be deposited by IMP PVD. The TiN barrier metal may also be deposited either by CVD using ammonia and one of a number of precursor molecules, including the tetrakis dimethylamino titanium (TDMAT) or tetrakis diethylamino titanium (TDEAT). CVD has usually been preferred for TiN because of improved step coverage.

It is necessary to remove the excess blanket tungsten above the dielectric layer. This was previously done by a tungsten etchback process to remove the excess tungsten and leave a planarized plug. In 0.25-μm device generations and below, planarization of tungsten by chemical mechanical planarization (CMP) is the preferred process (CMP and etchback are addressed in Chapter 18).[49] Barrier metals such as TiN and Ti are used to prevent diffusion between the tungsten and the silicon.

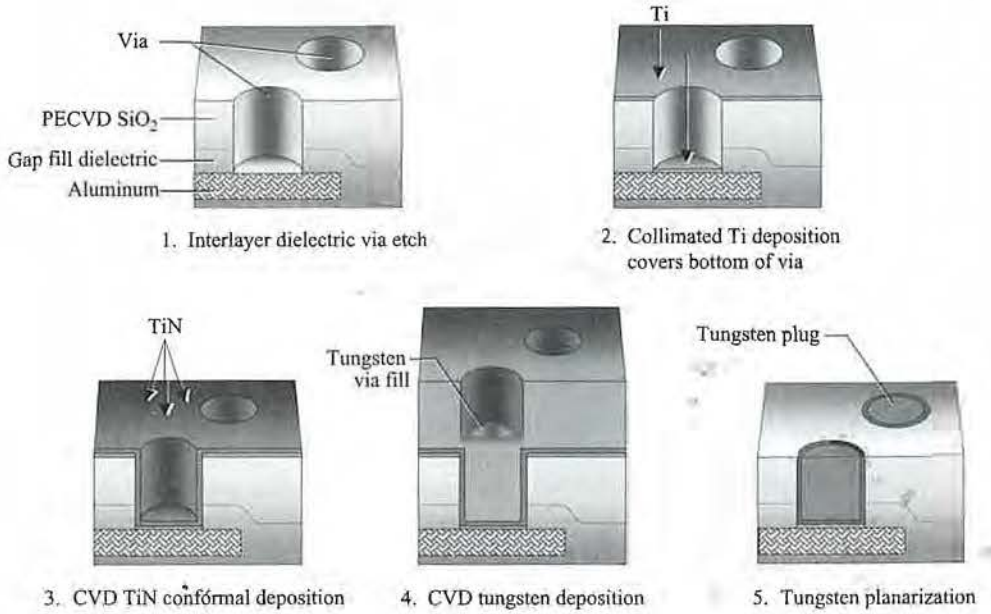


FIGURE 12.23 Blanket Tungsten CVD with Ti/TiN Barrier Metal

Copper CVD ■ *Copper (Cu) CVD* is a potential process for depositing a thin copper seed layer necessary for copper electroplating. The seed layer, or strike layer, is thin (about 500 to 1000 Å) and deposited on top of a diffusion barrier (most likely a Ta-based barrier metal). For successful electroplating, it is critical that this seed layer be continuous and free of pinholes and voids along the feature sidewalls and bottom. If a seed layer is not continuous, this can create a void in the electroplated copper. The excellent conformality of CVD is why this process has been investigated for the seed layer.

Cu Precursors. There are two precursors for CVD Cu, Cu(I), and Cu(II). Note that Cu(I) indicates a copper ion with a +1 positive charge and Cu(II) indicates a +2 positive charge. The most widely used Cu(I) precursor is Cu(hfac)(TMVS), chemical name trimethylvinylsilylhexafluoroacetylacetonate copper (I), chemical formula $C_{10}H_{13}CuF_6O_2Si$, and referred to by its trade name of CurpraSelect.[50] This molecule combines copper in a +1 oxidation state with TMVS and hfac ligands to make a clear yellow, liquid precursor (a ligand is a molecule or ion surrounding a central metal cation). TMVS is flammable, but the compound Cu(hfac)(TMVS) does not ignite easily. Cu(hfac)(TMVS) is compatible with industrial stainless steel delivery vessels. The CVD deposition proceeds by reducing a copper atom to metal while oxidizing another atom to $Cu(hfac)_2$ and releasing free TMVS as by-products. The chemical reaction is:

$$2Cu^{+1}(hfac)TMVS\ (gas) \rightarrow Cu^{0}\ (solid) + Cu^{+2}(hfac)_2\ (gas) + 2TMVS\ (gas)$$

The most common Cu(II) precursor is $Cu(hfac)_2$. For example, the Cu(II) reaction can proceed by reduction in H_2:

$$Cu(hfac)_2\ (gas) + H_2\ (gas) \rightarrow Cu^{0}\ (solid) + 2H(hfac)\ (gas)$$

Copper Electroplate

The transformation of IC fabrication to copper metallization is underway for all chip manufacturers. Initially, high-performance microprocessors and fast, static RAMs are being converted to copper technology. *Copper electroplate,* also known as *electroplating, electrochemical deposition (ECD),* or *electrofill,* is the first-generation deposition method to be used for copper metallization. Cost and performance will be important issues that affect when copper will replace aluminum as the mainstream interconnect metallization. Electroplating has not traditionally been used in semiconductor manufacturing. However, it has been an important metallization process in other areas of electronic manufacturing, such as thin film heads used in disk storage devices and copper wiring for printed circuit boards. Therefore, its process and equipment requirements are well understood.



Copper Electroplating Tool
(Photo courtesy of Novellus)

Electroplating Fundamentals ■ The basic principle of electroplating copper metal is to immerse a wafer with a conductive surface into a solution of copper sulfate ($Cu(SO_4)$) which contains copper ions to be deposited (see Figure 12.24). The wafer and its seed layer are connected electrically to an external power supply as a negatively charged plate, or cathode. A solid piece of copper is immersed in the solution and configured as the positively charged anode. Electrical current passes through the wafer, into the solution, and through the copper anode.[51] When current flows, the following reduction reaction occurs at the wafer surface to deposit copper metal:

$$Cu^{2+} + 2e^{-} \rightarrow Cu^{0}$$

Copper ions *Electrons* *Copper metal*

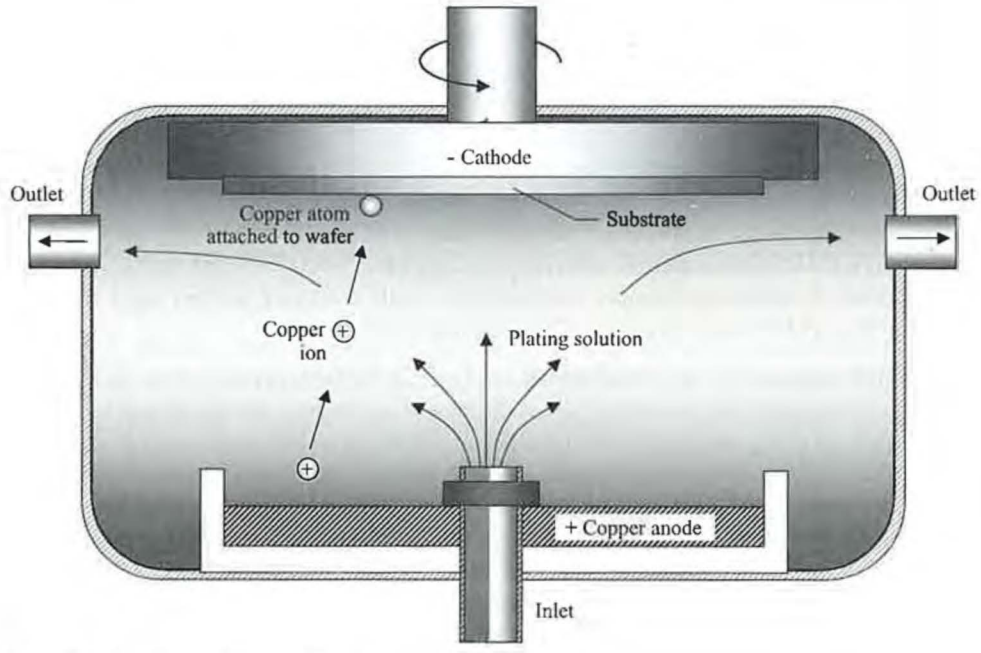


FIGURE 12.24 Copper Electroplating

Metal copper ions on the cathode wafer surface are reduced to metal copper atoms during electroplating. At the same time, an oxidation reaction occurs at the copper anode that balances the current flow in the cathode. This reaction maintains electrical neutrality in the solution.

The quantity of copper deposited is directly proportional to the current delivered to the conductive wafer surface (Faraday's law of electrolysis).[52] With this relationship, the basic parameters to control in electroplating are current and time. With no current flow, there is an equilibrium potential among the anode, cathode, and solution. When an external power source applies a voltage, a current flows between the anode and cathode and metal is deposited on the cathode proportional to the amount of current.

In practice, electroplating is complicated to control, especially the electroplating solution and how the current is applied. Given the high-aspect ratio holes and trenches that must be filled on high-performance ICs, electroplating is challenged to maintain a uniform current density in the holes. This condition is important because the plating rate is a direct function of current density. If there is a high current density at the top of the hole and a lower current density at the bottom of the hole, then copper will plate faster at the top.

Different types of voltage waveforms applied to the cathode/anode system can assist in plating high-aspect ratio holes. For instance, by applying an oscillating electric field and controlling the amplitude of the waveform, a deposit/etch (referred to as dep/etch) sequence is obtained. In this manner, the copper can be slightly removed (etched) in the high-density current regions to balance the copper gap-fill capability.

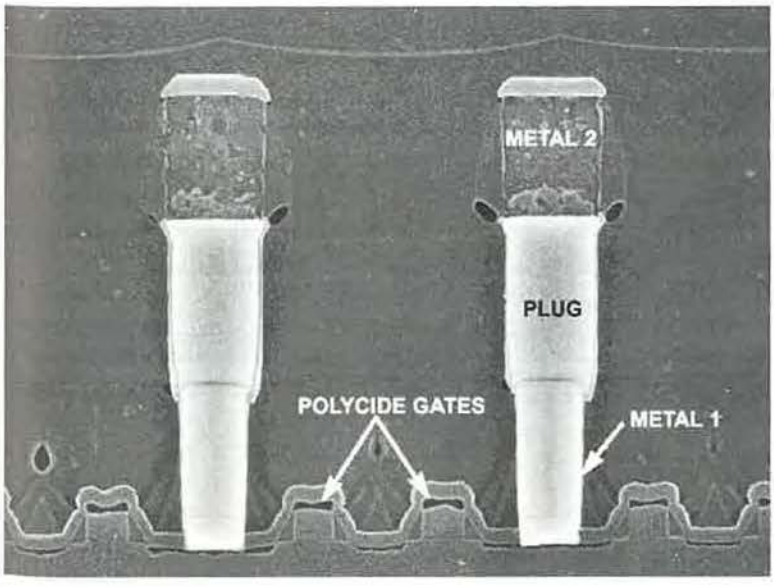
Because the copper electroplating metallization is a new process for semiconductor manufacturing, there are a host of other issues to address. For instance, it is important that no copper plate on the backside of the wafer. Electroplating also poses concerns for chemical control and disposal. It does simplify the metallization process somewhat by avoiding a high vacuum or complex heating of the wafer.

METALLIZATION SCHEMES

The strategy for metal interconnects for IC fabrication is undergoing dramatic change. After many years of development activities, copper is being implemented as the main chip interconnect conductor for a wide range of ICs.[53] Either aluminum or copper metallization is expected to be used for chip applications during a transition period until copper is fully implemented. The type of metallization scheme used depends on how the chip design is optimized for performance and price.

Traditional Aluminum Structure

The traditional interconnect metal has been an aluminum-copper alloy with an interlayer dielectric of SiO_2 to insulate between the metal layers. The process steps for the traditional aluminum



Blanket Aluminum Etch (Micrograph courtesy of Integrated Circuit Engineering)

interconnect technology for an ILD-2 and metal-2 (one complete level) are described in Steps 11 and 12 of the process flow described in Chapter 9. This traditional process can be viewed as an *aluminum subtractive process* because the aluminum is deposited as a blanket film and then etched away (subtracted) to form the circuitry. The critical step that defines the width and spacing of the aluminum interconnect lines is metal etch, while SiO_2 is deposited into the narrow gaps between the lines.

New materials and processes are being rapidly introduced into advanced wafer fabs to support the 0.18-μm technology node with traditional aluminum alloy metallization. This is a transitional period until copper metallization is eventually implemented. As a rule, most fabs will change only one major microchip material at a time (e.g., metal or insulator) to minimize the inherent risk to production. With these new fabrication materials and their stringent processing requirements, the general trend is for increased use of high-density plasma CVD (HDPCVD) for dielectrics, a shift from sputtered metals to metal CVD, and increased use of chemical mechanical planarization (CMP). The goals are to increase product performance and manufacturing productivity.

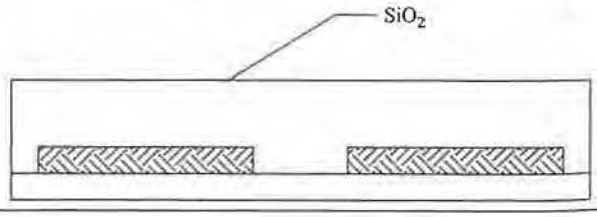
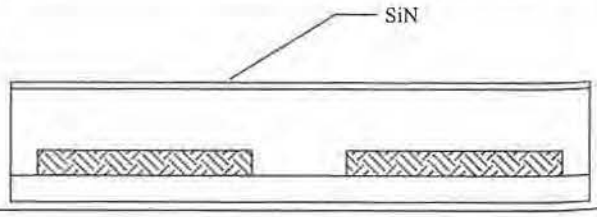
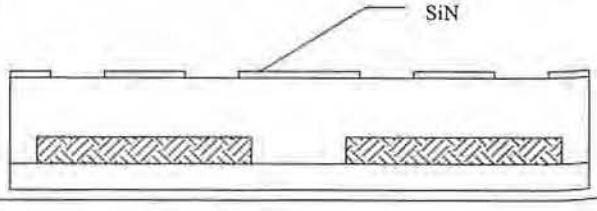
Copper Damascene Structure

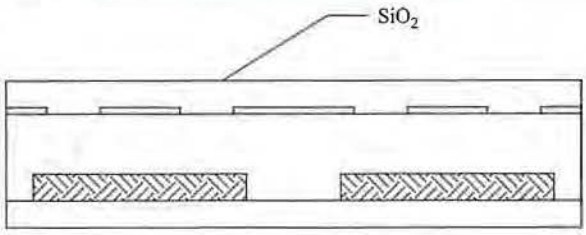
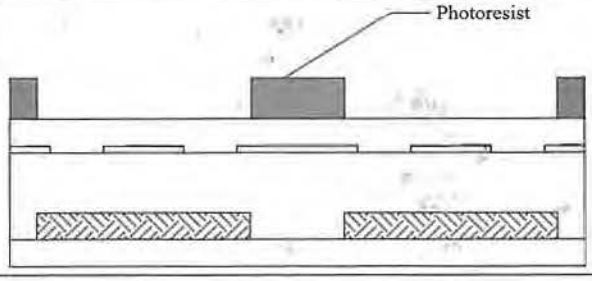
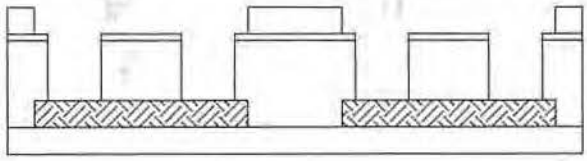
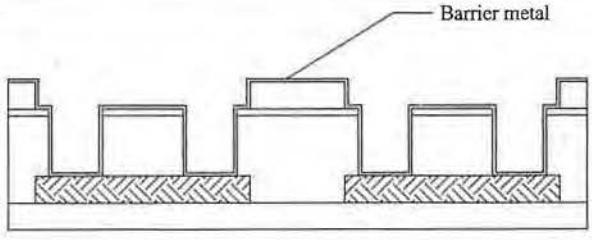
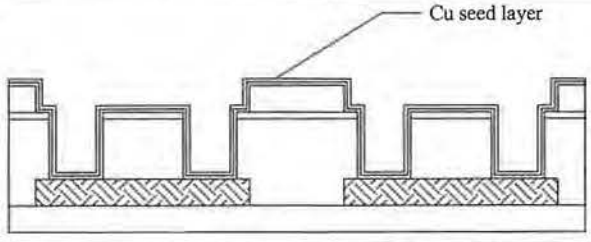
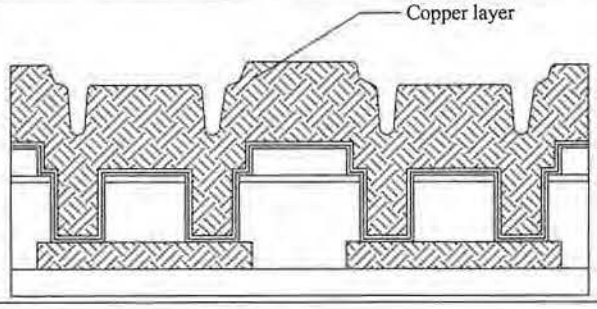
The semiconductor industry is implementing copper as the interconnect material for microchip fabrication. The traditional process flow will not be used for copper metallurgy because copper is not suitable for dry-etching. Copper also has special requirements to minimize its diffusion into silicon. To form copper interconnect wiring, a dual-damascene process is used to avoid copper etching. In the damascene process, it is no longer metal etch that defines the critical line width and spacing, but rather dielectric etch.

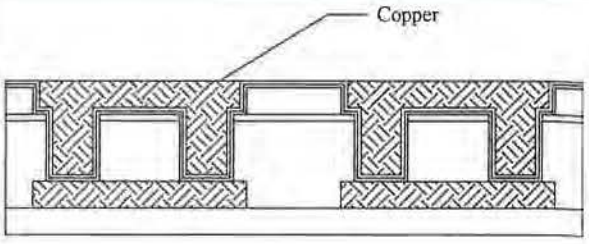
Dual Damascene Process ■ Since copper is difficult to etch, early developers of copper technology were forced to consider alternative approaches to creating metal lines. The *dual-damascene process* became the consensus process for copper metallurgy. It creates both the vias and lines for each metal layer by etching holes and trenches in the ILD, depositing copper in the etched features and using chemical mechanical planarization to remove the excess copper (referred to as *copper overburden*).

There are many possible scenarios for a dual-damascene process flow. Table 12.5 explains a basic process flow with the essential technologies that may or may not include all the steps performed by a particular manufacturer.

TABLE 12.5* Copper Metallization using Dual Damascene

Process Step	Description	Structure
1. SiO_2 deposition	ILD oxide deposition with PECVD to desired thickness for via. There is no critical gap fill; therefore, PECVD is acceptable.	
2. SiN etch stop deposition	Thin (250 Å) SiN etch stop is deposited on ILD oxide. The SiN needs to be dense and pinhole-free; therefore, HDPCVD is used.	
3. Via patterning and etch	Photolithography to pattern and dry etch via openings into SiN. Strip photoresist after completion of etch.	

Process Step	Description	Structure
4. Deposit remaining SiO_2	PECVD oxide deposition for remaining ILD oxide.	
5. Interconnect patterning	Photolithography to pattern SiO_2 trench with resist. Previously patterned via openings are located in trench.	
6. Etch trench for interconnect and hole for via	Dry etch trench in ILD oxide, stopping on the SiN layer. Etch continues to form via opening by passing through opening in SiN.	
7. Deposit barrier metal	Deposit Ta or TaN diffusion layer with ionized PVD on bottom and sidewalls of trench and via.	
8. Deposit Cu seed layer	Deposit continuous Cu seed layer with CVD. The layer must be uniform and free of pinholes.	
9. Deposit Cu fill	Deposit Cu fill with electrochemical deposition (ECD). Fill both via opening and trench.	

Process Step	Description	Structure
10. Remove excess Cu with CMP	Remove excess Cu using chemical mechanical planarization (CMP). This planarizes the surface and prepares for the next level. The resulting surface is a planar structure with metal inlays in the dielectric to form the circuitry.	

[54] P. Singer, "Making the Move to Dual Damascene Processing," *Semiconductor International* (August 1997): p. 79.

For dual-damascene processing, a two-tiered metal inlay is created that includes a series of holes (for contacts or vias) in addition to the interconnect trench for metal lines. The vias and metal line levels undergo copper fill concurrently, which saves a process step and eliminates the interface between the via and metal line.

There are different approaches to performing dual-damascene processing, each with their own set of challenges. Most of the manufacturing methods integrate the use of etch-stop materials to control how deep etching occurs for the via and trench. Etch stop is typically done by using a barrier metal such as silicon nitride (Si_3N_4 or Si_xN_y) as a hard mask at the bottom of the via or trench. Si_3N_4 etches at a much slower rate than the dielectric material, thus effectively stopping the etch process. Some approaches may even have two separate Si_3N_4 layers, which adds process complexity. In addition, Si_3N_4 has a high-k and increases the interlayer capacitance of the interconnect stack, which is why the Si_3N_4 layer needs to be thin.

The dual-damascene flow shown above has the via etch done in the same etch step as the trench, with the SiN etch stop to define the bottom of the trench. In other variations of dual-damascene, the via is etched first, then the trench is patterned and then etched. Trench structures created over topography from a previous via etch pose a significant challenge for photolithography.

The most important reason for using a damascene approach to copper metallization is to avoid metal etch. A second advantage to damascene processing is that there is no further need for dielectric gap fill between etched metal lines, since the dielectric is applied as a blanket and then etched.

The dual-damascene process in wafer fabrication potentially uses 20 to 30% fewer steps than traditional aluminum metal interconnect. Not only are there fewer manufacturing steps, but dual damascene also eliminates or reduces some of the most difficult steps of traditional aluminum metallization, including aluminum etch and many of the tungsten and dielectric chemical-mechanical polish steps.[54] Reducing process steps in wafer fabrication is important for improving the yield of the process, since fewer process steps translate to fewer sources of error that reduce assembly yield.

METALLIZATION QUALITY MEASURES

Wafer fabrication quality measures for metallization are provided in Table 12.6.

TABLE 12.6 Quality Measures for Metallization

Quality Parameter	Types of Defects	Remarks
1. Sputtered metal adhesion.	A. Metal layer does not adhere to substrate.	Parameters affecting film adhesion are: • Wafer contamination • Stress • Types of materials • Temperature of substrate • Argon pressure
2. Sputtered film stress.	A. Excessive stress leads to: • Cracks in the film surface. • Loss of film adhesion. • Increased resistivity in some materials.	Film stress can be caused by excessive temperature of the wafer substrate. Ways to reduce wafer temperature are: • Lower deposition rate • Increased backside cooling Cracks can cause: • Peeling of the film layer • Contaminant migration • Electrical opens or short. Measure film stress (bow of wafer surface) before and after deposition. Units for stress are dynes.
3. Sputtered film thickness.	A. Metal layer does not meet film thickness specifications (e.g., sheet resistance out of specification).	Parameters that affect film thickners are: • Incorrect recipe • Improper flow rates • Improper substrate temperature • Improper chamber pressure • Improper power supply energy • Wrong time setting
4. Uniformity of electroplated (electrochemical deposition, or ECD) metal film.	A. Nonuniform film thickness indicated by: • Inadequate gap fill and step coverage for high aspect ratio openings (nonuniform metal thickness at top and bottom of high aspect ratio holes). • Nonuniform deposition thickness across the wafer and from wafer to wafer. • Voids in film.	Critical parameters for electroplating film uniformity are: • Depositing a uniform CVD seed layer without voids. • Maintaining proper electroplating bath chemistry (composition and concentration) for organic additives, primarily brighteners and suppressors, to attain void-free deposition that fills bottom and sidewalls of gaps.

METALLIZATION TROUBLESHOOTING

Common troubleshooting problems for metallization are provided in Table 12.7.

TABLE 12.7 Common Metallization Troubleshooting Problems

Problem	Probable Cause	Corrective Actions
1. Degradation in step coverage of metal film.	A. Decrease in substrate temperature. For Al alloy sputter deposition, step coverage is dependent on the wafer temperature during deposition.	Heating the substrate to improve step coverage because surface mobility of deposited metal atoms improves.
	B. Increase in deposition rate.	Decrease deposition rate. Increase in sputter deposition rate may degrade step coverage due to reduced surface mobility because of arrival of more atoms at surface.
2. Vacuum chamber integrity.	A. Chamber cleanliness or moisture in chamber.	• Check for vacuum leaks or chamber outgassing. Residual gas in chamber that can change film reflectivity. • Check for O_2 or N_2 in metal films that can change resistivity and film stress. • Clean chamber and do H_2O bake-out.
	B. Outgassing or system leaks.	• Use helium leak detection to inspect for system leaks. • Assess the chamber conditions before deposition with residual gas analyzer.
3. Contamination of metal film.	A. Particles on surface of film.	Check the following common particle sources: • Dirty input wafers. • Problems in hand-off between robot and chamber mechanism. • Incomplete chamber cleaning between runs. • Dirty cassettes. • Contaminated nitrogen backfill.
4. Voids in copper trench fill after dual-damascene electroplating.	A. Excessive seed layer thickness on the wafer surface (field) that pinches off the via or trench, creating a center void in the film.*	Optimize the CVD Cu seed layer deposition by evaluating the electroplating current from the field to the bottom of vias and trenches. The goal is to deposit adequate seed layer at the bottom of a high-aspect ratio feature without increasing field thickness.
5. Excessive copper dishing after dual-damascene CMP.	A. Cu dishing for Cu CMP is often caused by tantalum diffusion barrier, which must be polished back in the presence of Cu.**	After Cu is polished, the Ta layer must be removed from the level. The Cu pad/slurry field does not effectively remove Ta. Options are: • Optimize the pad/slurry for Ta. • Minimize the Ta field level thickness.

* R. Jackson et al., "Processing and Integration of Copper Interconnects," *Solid State Technology* (March 1998): p. 56.
** Ibid.

SUMMARY

Metallization deposits a thin metal film to form the interconnect wiring and contact or via connections on the chip. There are six metal categories used in wafer fabrication, with specific requirements for optimum performance. Aluminum has been the traditional metal for interconnect lines. An ohmic contact is the low-resistance contact between silicon and the interconnect metal. Aluminum is sometimes alloyed with silicon to reduce junction spiking at the ohmic contact. Aluminum is often alloyed at 0.5 to 4% copper to minimize electromigration reliability problems. New interconnect metallization is based on copper metallurgy to decrease the metal resistivity. Copper combined with low-k dielectric will decrease the chip interconnect delay, but copper does require a new processing approach since it does not etch well. Barrier metals are used when joining metals. Different barrier metals have optimum properties depending on the application. A silicide is a refractory metal alloyed with silicon to improve contact resistance and adhesion. A salicide is a particular silicide that is aligned to the source, drain, and gate structure. Metal layers are connected with vias filled with tungsten plugs. The most widely used metal deposition system is sputtering. Sputtering physically bombards a target to dislodge atoms and deposit the atoms as a thin film on the wafer surface. The three most common types of sputtering are RF, magnetron, and ionized metal plasma. RF sputtering is inefficient, while magnetron has a higher deposition rate but limited gap-fill capability. Ionized metal plasma has improved directionality for high-aspect ratio deposition. CVD metal has the best conformality and is used for tungsten plug fill and copper seed layer. Copper electroplate is the process chosen by major semiconductor manufacturers for copper wiring deposition. Traditional aluminum metallization deposits a blanket aluminum film and then etches line patterns to form interconnect wiring. Copper metallurgy will use a dual-damascene process that etches vias and trenches in dielectric, deposits copper fill, and then removes excess copper through chemical mechanical planarization.

KEY TERMS

interconnect
wiring
contact
vias
plug
eutectic temperature
anneal or sinter
ohmic contact
junction spiking
electromigration
hillocks
copper interconnect
barrier metal
refractory metals
silicide
polycide
salicide
tungsten plugs
evaporation
physical vapor deposition (PVD)
target
momentum transfer
sputtering yield
sputter etch (reverse sputter)
RF sputtering
magnetron sputtering
collimated sputtering
sputtered aluminum
ionized metal plasma PVD (IMP or ionized PVD)
tungsten (W) CVD
copper CVD
electroplate (electroplating, electrochemical deposition (ECD), or electrofill)
evaporation
aluminum subtractive process
dual-damascene process

REVIEW QUESTIONS

1. Define the following terms: interconnect, contact, via, and plug.
2. What metal has traditionally been used for interconnect wiring, and what is its replacement?
3. List and describe the seven performance requirements for metals used in wafer fabrication.
4. List the categories of metals and metal alloys used in semiconductor manufacturing.
5. Explain why aluminum has been the interconnect metal of choice for microchips.
6. What is an ohmic contact and what is its advantage?
7. Describe junction spiking and list the two primary ways it was resolved.
8. Discuss electromigration and how it affects reliability. How is electromigration controlled in aluminum wiring?
9. List and discuss the five benefits for introducing copper metallization.
10. What are the three major challenges for converting to copper for interconnects?
11. Explain what a barrier metal is and the essential properties of a barrier material. What metals are commonly used as a barrier metal?
12. List the special requirements for a copper barrier metal.
13. Define silicide and explain why refractory metal silicides are important in wafer fabrication.
14. What are the benefits of titanium silicide? Explain the C49 and C54 phase structures.
15. What silicide is promising for future wafer technology? Why?
16. What is the salicide process?
17. Describe a tungsten plug, and discuss how it is used in multilayer metallization.
18. Why was evaporation replaced as a metal deposition system?
19. Provide a short explanation about sputtering and how it works.
20. Is sputtering suitable for alloy deposition?
21. What are the advantages to sputter deposition?
22. List and explain the six steps to sputtering.
23. Explain the physics of sputtering.
24. Describe sputter yield.
25. What is the purpose of sputter etch?
26. Describe an RF sputter system. What is its major limitation?
27. Discuss how a magnetron sputtering system improves the deposition rate.
28. Explain why sputtering has poor step coverage. How does collimated sputtering improve step coverage?
29. Describe ionized metal plasma. How does this process improve high-aspect ratio gap fill?
30. What is the typical method for creating a tungsten plug in advanced ICs?
31. Why could CVD be used for the copper seed layer?
32. Explain the fundamental process of copper electroplate.
33. Why is traditional aluminum metallization a subtractive process?
34. What is the primary reason for implementing the dual-damascene process for copper?
35. List ten steps for a dual-damascene metallization process.

METALLIZATION EQUIPMENT AND MATERIALS SUPPLIERS' WEB SITES

Angstrom Sciences Inc.	http://www.angstromsciences.com/
Applied Materials	http://www.appliedmaterials.com/products/
Genus Incorporated	http://www.genus.com/
Materials Research Corporation	http://www.materialsresearch.com/
Nordiko USA Inc.	http://www.nordiko.com/
Novellus Systems Inc.	http://www.novellus.com/index.htm
Process Materials Inc	http://www.processmaterials.com/
TEL, Tokyo Electron Ltd.	http://www.teainet.com/
Veeco-CVC	http://www.veeco.com

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