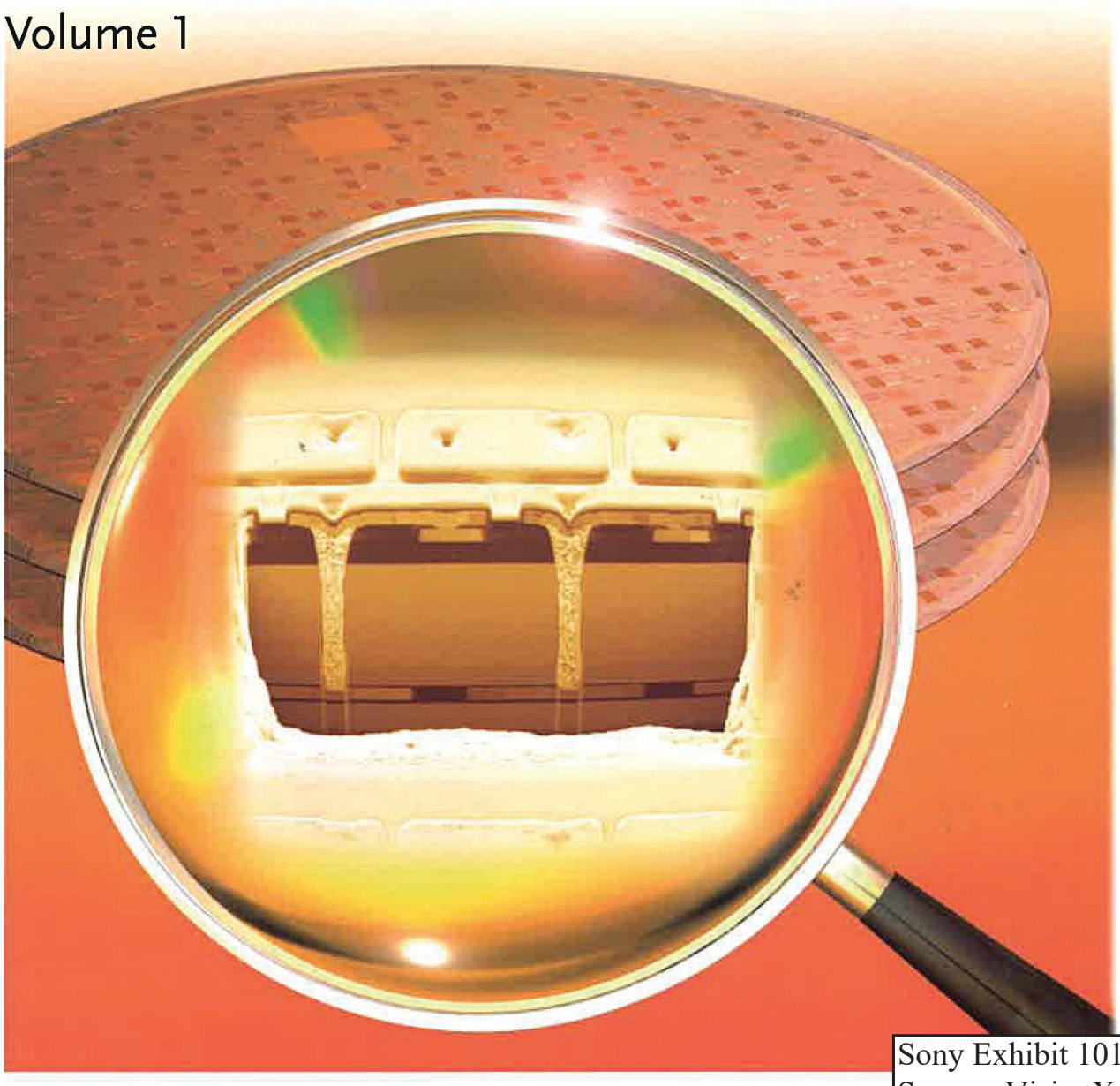
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Handbook of 3D Integration

Technology and Applications of 3D Integrated Circuits

Volume 1



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Edited by
Philip Garrou, Christopher Bower and Peter Ramm



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Cover Description:
The artistic illustration explains the principle of 3D integration: Stacking and vertical interconnecting of device layers. The magnified portion depicts a cross section of a 3D integrated test chip which was fabricated at Fraunhofer Munich. The wafer-level 3D integration technology is based on bonding of thinned device substrates and a metallization process providing a high vertical wiring density. This technology presents a solution to performance and reliability limitations due to the wiring of microelectronic devices and enables completely new ultra-miniaturized products.

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Phil Garrou, Christopher Bower, and Peter Ramm

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9
Metallization by Chemical Vapor Deposition of W and Cu

Armin Klumpp, Robert Wieland, Ramona Ecke, and Stefan E. Schulz

9.1
Introduction

To build vertical electrical interconnects between thinned chip stacks or wafer stacks, TSVs with high aspect ratios are used in several currently presented 3D process flows [1–4]. For this purpose, the required metallization needs to be deposited after the electrical isolation of Through Silicon Vias (TSV; see Chapter 6, Dielectrics) in such a way, that reliable electrical interconnects are formed. Mostly, the TSV metallization consists of a bi- or multilayer stack of a thin diffusion barrier, adhesion layer and/or seed layer and the conductor material like tungsten (W) or copper (Cu). In general, different deposition techniques are available to realize metal deposition: electrochemical deposition (ECD, electroplating), chemical vapor deposition (CVD), electroless plating and physical vapor deposition (PVD: Sputtering). Apart from PVD all processes have the potential to fill high aspect ratio (HAR) patterns. Figure 9.1 shows the applicability of different deposition processes and filling concepts depending on the TSV diameter. The pure metal CVD approach is suited for complete TSV fill with lateral width of up to ~3 μm at high aspect ratios. It is currently unclear as to what extent the electroplating technology is able to substitute MOCVD (metal-organic chemical vapor deposition) processes for HAR TSV metallization [5, 6]. However, if aspect ratios of larger than 7 : 1 are to be filled with a conducting material, CVD is the process with the highest currently available conformality. To date, CVD of poly-Si, tungsten or copper has been used to completely fill TSVs. In the region above 3 μm lateral size, several factors limit the application of metal CVD, like high film stress for W CVD and process limitations for Cu CVD. In this case, filling can be performed by electroplating. CVD can be used to deposit a so-called seed layer only, which then acts as a base layer to grow metals by subsequent electroplating techniques. This is especially of great interest since even most advanced PVD tools are hardly able to cover vias with aspect ratios larger than 7 : 1 [7, 8]. Depending on the chosen

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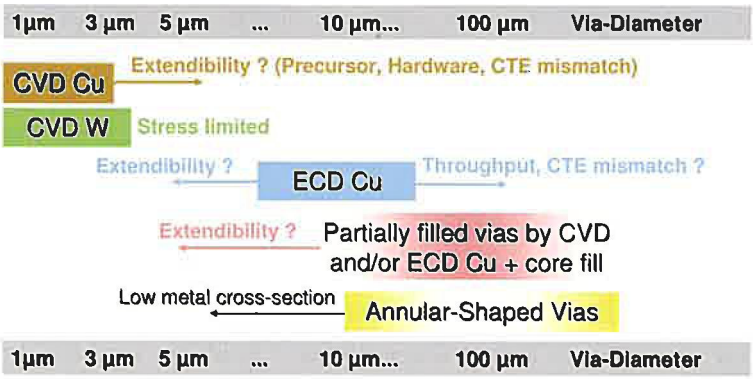


Figure 9.1 Overview of deposition processes and concepts for metallization of TSVs.

metallization scheme, a thin conducting CVD layer such as W or barrier/Cu can be used as a seed layer for the subsequent electroplating process.

TSV dimensions vary over a wide range, from ~2 up to 100 µm and beyond. An increasing demand for TSVs with HAR will probably require an increasing amount of metal CVD applications now and in the future, because the use of metal-PVD for a seed layer is strongly limited by the desired AR. For completely filled Cu TSVs with large diameters the mismatch in the coefficient of thermal expansion (CTE) of copper and silicon should be considered. This leads to vertical movement of the Cu plug in the TSV during repeated thermal cycling in further BEOL processes [9]. With the hybrid method, where the TSVs are only covered by Cu at the sidewalls and are backfilled by a composite material, the damage of dielectric layers due to thermal mismatch is prevented [9]. At the same time this has the potential to provide a low cost process that avoids the complexity of the void-free complete fill by ECD. The annular shaped TSV in contrast to cylindrical TSV is a further approach to reduce the impact of the thermal mismatch due to the reduction of metal volume in the TSV and to produce low resistance vias at the same time [9].

In this chapter we focus on the CVD of metals, that is, W and Cu, and metal nitrides (TiN). Metal-CVD or metal-organic. CVD (MOCVD) is typically carried out in a conventional CVD single wafer chamber (cold wall reactor). The deposition process is a strictly chemically based, temperature driven reaction of the decomposed precursor material on the wafer surface. Since moisture causes metal oxides, a load lock based system is required to accomplish repeatable and stable process conditions.

9.2 Commercial Precursors

The availability and choice of a precursor is one of the most delicate issues of metal deposition by CVD. The precursor choice determines the quality of the deposited films (impurities, adhesion), deposition parameters (temperature, pressure, reactants) and therefore influences the reliability of the 3D integrated TSVs. Most

commonly used metals for 3D integration are, currently, tungsten and copper for TSV filling and often TiN and also TaN as barrier/seed layer films. The former three materials will be discussed in more detail.

9.2.1 TiN Precursors

Commercially available precursors for CVD of TiN are $TiCl_4$ with NH_3 addition [11, 12], TDMAT [tetrakis(dimethylamino)titanium] [13, 14] and TDEAT [tetrakis(diethylamino)titanium) [15]. With $TiCl_4$, the chemical reduction of $TiCl_4$ with NH_3 to TiN and HCl occurs instantly and requires sophisticated management of the gas/precursor flows into the reaction chamber to avoid unwanted gas phase reactions above the wafer surface, thus creating particles and TiN deposition behind the gas distribution plate. Additionally, an acceptable Cl-content in the TiN-film would require temperature treatments in the 600 °C range [16], which is far too high for backend processes like 3D integration.

Therefore, metal-organic precursors like TDMAT or TDEAT are often applied in commercially available metal-CVD reactors, for example from Applied Materials or from Novellus Systems. With TDMAT, the TiN film is thermally deposited on a heated substrate from TDMAT that is delivered from a bubbler by using a helium carrier gas. The underlying deposition reaction can be described by the following equation:

$$Ti[N(CH_3)_2]_4 \rightarrow TiN(C,N) + HN(CH_3)_2 + \text{other hydrocarbons}$$

The deposition is carried out under surface reaction limited conditions for films with high step coverage [17]. To remove impurities and to achieve a stable film, a plasma densification step is needed after the thermal decomposition of TDMAT (see Section 9.3.1).

9.2.2 Copper Precursors

There are inorganic and metalorganic precursors for the CVD of Cu. The copper halides have the disadvantage that they are solids, which causes problems of the precursor delivery. Turning to liquid sources, which are more convenient than solid ones, metalorganic precursors are attractive because of the lower precursor processing temperature. Metalorganic precursors are classified with respect to the oxidation state of the copper as Cu(II) and Cu(I) compounds. Most compounds in use are β-diketonate complexes. In a Cu(II) compound the central Cu^{2+} ion is bonded to two singly-charged β-diketonate ligands. In contrast, Cu(I) compounds contain one singly charged β-diketonate ligand that is strongly bonded to the central Cu^{+} ion and a second neutral ligand that is more weakly bonded to the Cu. The difference in the Cu–ligand bond strengths is reflected in the minor stability, lower deposition temperatures and higher growth rates typical of the Cu(I) compounds. An important characteristic of both kinds of precursors is the use of heavily fluorinated ligands

such as hexafluoroacetylacetonate (hfac). Substitution of hydrogen with fluorine induces a significant increase in volatility of the complexes, but also affects negatively the adhesion of the deposited films. [18]

Major efforts have gone into the design and development of new precursors, for both Cu(II) and Cu(I) compounds. Some authors focus on the thin film deposition as conformal seed layer for the Cu electroplating [19–21].

The most widely used precursor for Cu CVD is (hfac)Cu(TMVS) (copper hexafluoroacetylacetonate trimethylvinylsilane), named CupraSelect, which is commercially available from Schumacher (Air Products). Beneficial for the industrial employment of CupraSelect is its availability in large quantities and good purity. Its vapor pressure at room temperature is 8 Pa and increases to 260 Pa at 65 °C. Nevertheless, it has insufficient thermal stability at elevated temperatures, so that a bubbling system should not be used for precursor delivery [22].

Another commercially available precursor is GigaCopper [(hfac)Cu(MHY)] (MHY = 2-methyl-1-hexene-3-yne) from BASF (formerly Merck). Joulaud *et al.* [23, 24] compared both CupraSelect and GigaCopper in regard to the deposition rate and film properties.

Both precursors decompose in the same way:

$$2Cu^{I}(hfac)L_{(g)} \rightarrow Cu^{0} + Cu^{II}(hfac)_{2(g)} + 2L \quad (L = TMVS,\ MHY)$$

The Cu deposition with GigaCopper shows no essential improvement concerning deposition rate and adhesion behavior. For both precursors only half of the Cu contained in the precursor contributes to film formation. Moreover, one reaction product in both cases is $Cu^{II}(hfac)_2$, which has a low vapor pressure as it is a solid under normal conditions. This results in extensive pump down steps between single deposition processes.

9.2.3 Tungsten Precursor

WF_6 (tungsten hexafluoride) is a well established precursor and has been used successfully for contact and via metallization in VLSI fabrication since the mid-1980s [25]. As an inorganic vapor, WF_6 is comparably easy to handle. It is highly corrosive, forming HF (hydrofluoric acid) if exposed to a humid atmosphere.

The main reaction to deposit a tungsten film is the hydrogen reduction of WF_6 (bulk deposition):

$$WF_6(vapor) + 3H_2(gas) \rightarrow W(solid) + 6HF(gas)$$

As is typical for CVD-processes, depending on the amount of WF_6-flow, there is a mass-transport-limited deposition regime, with deposition rate = f(WF_6-flow) and also a surface-reaction-rate-limited regime, with deposition rate = f(temperature, H_2-flow). For HAR trench filling, the latter regime is used for W-filling [10].

9.3
Deposition Process Flow

No matter if W or Cu is chosen as the main filling material in HAR TSVs, a conformal deposition of a barrier seed layer is always the first step in the filling of the TSVs. With W, the growth on and the adhesion to silicon oxide is poor. Therefore, a thin nucleation/adhesion layer, also called "liner", has to be deposited, for example, a TiN, TiW or a tungsten silicide (WSi_x) film. For copper metallization, a diffusion barrier is required to prevent the diffusion of copper towards the bulk silicon. Copper in dielectrics can lead to increased leakage current up to dielectric breakdown. In silicon, copper has a high diffusion coefficient and a high solubility at elevated temperatures. It forms Cu-Si compounds at relatively low temperatures and introduces deep level traps in Si. This causes electronic device failures. Barrier layers should prevent copper diffusion and reaction with adjacent materials. The nitrides of refractory metals (e.g., Ti, Ta, W) are promising candidates for barrier layers based on their properties. For Cu CVD, an additional adhesion layer may be necessary between the diffusion barrier and the Cu film.

Depending on the aspect ratio of the TSVs, the above-mentioned adhesion layers can be deposited by either PVD or MOCVD. In general, chemical vapor deposition is superior to physical vapor deposition concerning conformality. With increasing aspect ratio of the TSVs to larger than 7 : 1, MOCVD of TiN is a commonly used process. Once the barrier/adhesion layer has been deposited, the actual metal CVD process can be started. It is in any case preferable to use a multi-chamber system, where the TSV metallization flow can be performed without exposing the wafer to atmosphere until all metal is deposited, thus avoiding unwanted oxidation on the barrier layer surface (Figure 9.2). To finish the metallization sequence, an etch back

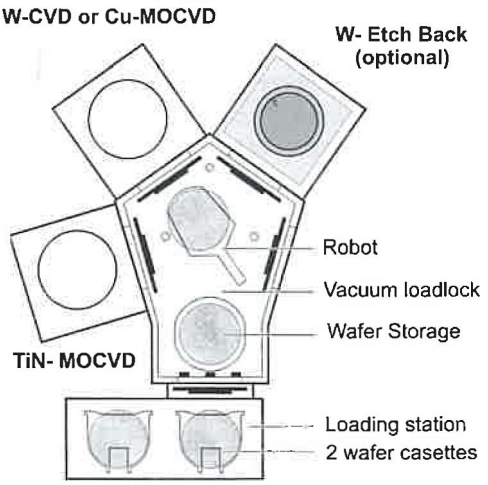


Figure 9.2 Schematic top view of a multi-chamber system with central load lock and robotic handling system for CVD of metal.

process, CMP of metal or a combination of both techniques, is required to remove the laterally deposited metal film until the TSV is electrically isolated.

9.3.1 Barrier Deposition

Presently, TiN is the most promising barrier material for application in 3D integration concerning precursor availability, deposition temperature (400 °C), good conformality and barrier properties.

For tungsten CVD, a TiN layer is used to provide an adequate nucleation and adhesion layer. For Cu filling it acts as barrier against Cu diffusion. Both metallization schemes use the same precursor and deposition process.

TiN depositions can be performed in commercially available CVD reactors with plasma capability. The precursor, TDMAT, is delivered by a bubbler system. The as-deposited film by pyrolysis of TDMAT contains substantial amounts of impurities (C,H) and is not stable to air. Therefore, a plasma densification treatment is needed after the deposition step. For CVD-W this step is also essential to promote the required adhesion for the highly stressed W films. The TiN barrier layers are produced by a multistep process consisting of alternating pyrolysis steps and plasma treatment steps. The TiN layer is plasma-densified after depositing ~5 nm TiN, resulting in a final thickness of ~2.5 to 3 nm after plasma treatment, depending on treatment time. The number of cycles determines the thickness of the entire barrier, for example, eight cycles for ~20 nm thickness. The deposition process and the TiN layer properties are described in detail in References [26, 27].

The step coverage in high aspect ratio TSVs depends on their geometry and diameter size as well as their depth. Vias with a width of 20 µm diameter and greater are uncritical with respect to the step coverage. Conversely, in slot holes 20 µm long, 1–5 µm wide, and 30 µm deep TiN films show a step coverage of 30–70% at the bottom of the via, depending on the width of the slot hole. In vias with circular cross-section the same dependence was found (Table 9.1). Higher step coverage is observed on sidewalls, particularly in the upper via range (over 100%, see Figure 9.3). Since the plasma treatment is quite directional, the densification is not very effective at surfaces parallel to the incident direction of the ions.

Table 9.1 Step coverage in TSVs with circular cross section and different sizes.

TSV size	1 µm	1.7 µm
depth	15 µm	15 µm
AR	15	8
Top	82 nm = 100%	82 nm = 100%
Upper side wall	110 nm = 163%	10 nm = 163%
Lower side wall	59 nm = 73%	63 nm = 78%
Bottom	27 nm = 33%	46 nm = 57%

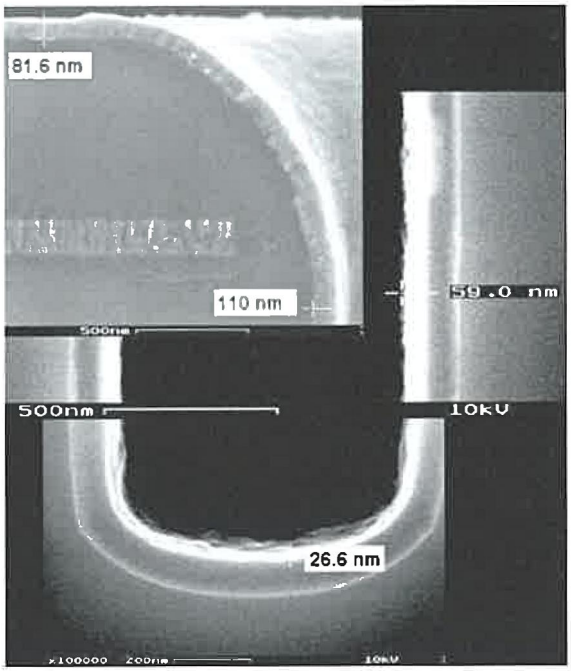


Figure 9.3 Step coverage of TiN in a TSV with AR = 15 and a width of 1 µm.

9.3.2 Adhesion Layer

Copper deposited by CVD often has insufficient adhesion to the barrier layer, especially when fluorine-containing precursors are used. Copper is a relatively precious metal, thus it is not possible to achieve good adhesion with oxide bonds. These oxide bonds, however, are the reason for the excellent adhesion of CVD TiN to SiO_2. Copper adhesion is influenced by the deposition process. For a PVD process the adhesion of copper on different layers is always sufficient. The kinetic energy of the particles forming the layer is greater than for CVD and ECD (electrochemical deposition) processes. During sputtering, adsorbates are removed and there is a forced intermixing in the monolayer range. Another reason for the insufficient adhesion of CVD copper is the chemistry used. Although very pure copper layers are available with the CupraSelect precursor, impurities are enriched at the interface. They form an amorphous interlayer 3 nm thick, consisting of fluorine, oxygen, and carbon (Figure 9.4a) [28]. This interlayer was also found by other authors [29].

Furthermore, there is a contradiction between the barrier properties and the adhesion to the copper. On the one hand, no reactions and mixing with copper are allowed to prevent the diffusion. On the other hand, a very thin layer between TiN and CVD copper can promote the adhesion. However, this layer must not negatively influence the properties of the barrier and the conductor. Such an adhesion layer is a

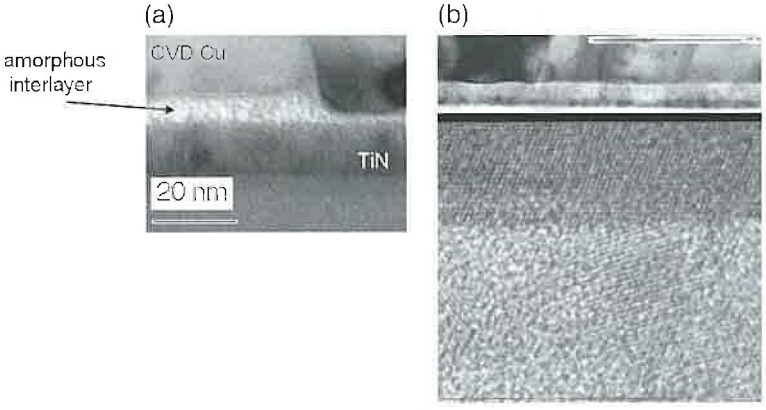


Figure 9.4 (a) XTEM of 20 nm TiN/CVD-Cu with amorphous interlayer. (b) XTEM of 5 nm TiN/10 nm PE-TiN/Cu HRTEM of the interface PE-TiN/Cu showing no interlayer.

very thin film with strong adhesion to the upper and lower layers, but in the case of Cu it is not suitable as a barrier layer. Therefore, a process leading to a Ti-rich TiN layer was developed. The free Ti can react with Cu, which strongly promotes the adhesion.

The adhesion layer is grown by PECVD with the same precursor, TDMAT. The deposition process and the layer properties are described in detail in Reference [27]. The electrical resistivity of the adhesion layer (~3–4 nm) was investigated together with a 5 nm thick standard TiN layer. The layer stack had a resistivity of 320 μΩ cm, slightly higher than 5 nm TiN (290 μΩ cm). This increase results from the higher impurity content of the PE-TiN, but it is acceptable.

The Ti-rich TiN layer shows only excellent adhesion to the copper if adhesion layer deposition and Cu CVD are carried out *in situ* with a subsequent heat treatment. The PECVD-TiN is not stable in air for long so that a vacuum break should be avoided. The complete stack, TiN barrier/TiN adhesion/CVD-Cu, shows no interlayer (Figure 9.4b) and successfully passed the subsequent step of CMP.

Normally ~ 2 nm of this adhesion layer are sufficient to obtain good adhesion of CVD-Cu. Since step coverage is reduced for plasma-enhanced CVD processes the deposition process had to be optimized and extended. By varying the spacing (distance from shower head to wafer), step coverage of 20–30% at side walls and 15–40% on the bottom can be achieved, depending on TSV size and depth ($d = 1$–5 μm, depth 30 μm). For larger sizes step coverage increases. For a reliable TSV formation, especially to achieve a good bottom contact, the adhesion layer is also essential in the structures and not only on top. Adhesion of Cu on the inner surfaces of the TSVs must be ensured during further temperature steps in processing. If the TSVs are not completely filled with Cu because of overhang at the entrance of the TSVs, or when only a Cu seed layer is used for further Cu plating to fill the via, the Cu film can be extracted. In this case, no electrical contact can be realized by this TSV (Figure 9.5).

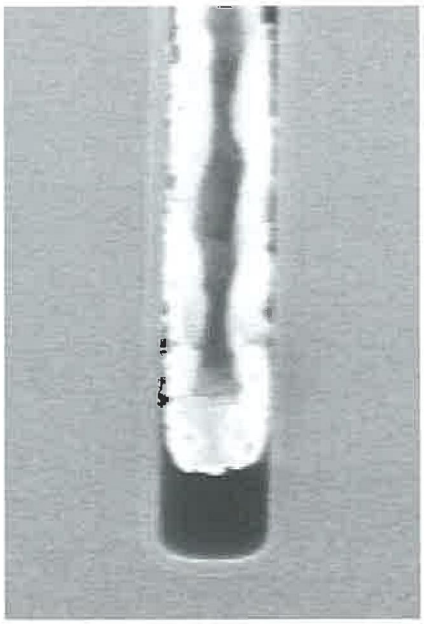


Figure 9.5 Cu extraction in the case of insufficient adhesion in TSV.

9.3.3
Copper Deposition

9.3.3.1 Deposition Equipment and Liquid Precursor Delivery Systems

The deposition equipment used was a P5000 with a lamp-heated Blanket Tungsten Chamber, but we recommend a resistively heated deposition chamber to minimize undesired Cu depositions, for example, at the heater window. A shadow ring is suggested, to prevent Cu deposition at the wafer backside and on the susceptor in either case. The results described in this chapter were obtained with the precursor (hfac)Cu(TMVS), which was evaporated using a liquid delivery system (LDS). This system is composed of a liquid flow meter for the precursor, a mass-flow controller for the carrier gas and a controlled evaporator unit from Bronkhorst. Within the system the precursor is dosed as a liquid with high accuracy and is vaporized just before the deposition. The heated stainless-steel gas line between the vaporizer and the deposition chamber should be as short as possible to avoid precursor loss due to Cu deposition on the inner surface of the line. In the worst case, precursor condensation can occur for very high precursor flow rates and long deposition times. Direct liquid injection systems (DLI) are an alternative means of precursor delivery.

9.3.3.2 Cu CVD Process Characteristics and Blanket Film Properties

The deposition rate of Cu with CupraSelect onto blanket wafers is relatively high and can reach up to 200 nm min^{-1} depending on the wafer size. This rate can be achieved

with high temperature (≥190 °C), high total pressure (≥2 kPa) and high precursor flow. A long incubation time compared to other CVD processes is observed for film formation, which depends on deposition temperature and pressure in the chamber. With increasing temperature, as well as for lower pressure, the incubation time is shortened. The pressure influences the free adsorption sites. Their density is reduced with higher pressure. In the same manner, the barrier material and potential pretreatments of the surface, such as H_2 plasma, impact the nucleation. The addition of water vapor during the nucleation stage leads to higher nuclei density and uniform distribution [22, 30].

The properties of the deposited Cu layers are influenced by the deposition parameters. The specific resistivity of the films depends on film thickness and grain size and is in the range 2.2–3 μΩ cm for unpolished films. The root mean square (RMS) roughness ranges from 15 to 20% of the Cu thickness. Hence, the determined layer thickness is usually too high, which in turn affects the calculation of the electrical resistivity. After polishing, the Cu layers exhibit electrical resistivity, <2 μΩ cm. The film density represents 90–96% of the bulk value. For a 350 nm thick Cu layer deposited at 200 °C the average grain size is 110 nm. The grains show a columnar structure. Impurity concentrations in the films resulting from the metal-organic precursor (Si, F, C and O) are below the detection limit of Auger electron spectroscopy (AES). However, there is an enrichment of impurities at the interface to the diffusion barrier, which heavily impacts the adhesion.

With the equipment described above, a deposition rate of 165 nm min^{-1} on 150 mm wafers at 200 °C and 2.7 kPa were achieved. However, the high deposition rate process is inapplicable for filling TSV structures because of the reduced step coverage of 65%.

9.3.3.3 MOCVD Cu Application to TSV Fill

Presently, complete filling of TSVs by Cu CVD using the described processes is only applicable for TSV sizes ≤ 2 μm after oxide passivation (Figure 9.6).

One way to achieve higher step coverage is to lower the deposition temperature. The parameters for the high-rate process are close to the transport-controlled regime. With lower temperatures (<170 °C wafer temperature) deposition takes place in the reaction-limited region. However, also with decreased temperature the deposition rate decreases drastically, to about 70 nm min^{-1}. Furthermore, the deposition surface enlargement with increasing TSV depth and TSV structure density becomes important for the deposition rate and step coverage. Therefore, the deposition parameters should be modified for each TSV layout to achieve the desired Cu thickness and step coverage. It is advised to use only one TSV size per layout. For moderate via diameters, that is, below 2.5 μm, and aspect ratios of lower or around 20 a complete TSV fill can be achieved using low deposition temperature (see Figure 9.6 for filling of 1.2 μm wide TSV with an aspect ratio of 12.5). For larger TSV diameters the filling process becomes more critical and the throughput will decrease further.

Moreover, the etch profile at the entrance of via is also important for the filling capability of the Cu CVD. A V-shaped via entrance is effective against the formation of

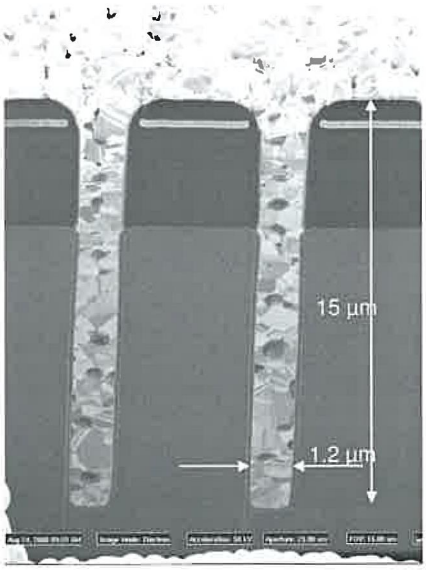


Figure 9.6 Cu-filled via holes with AR 12.5 : 1 after Cu CVD at 170 °C and anneal (focused ion beam, FIB).

overhangs due to the reduced step coverage of the deposition processes (passivation, barrier, metal). A completely V-shaped via further improves the filling capability.

9.3.3.4 MOCVD Cu Application to Cu Seed Layer

Depending on the application of the devices and stacks, the TSVs can have different sizes and depth. TSV sizes $\geq$2.5 µm can not be filled completely by Cu CVD in an economic manner. In this case the TSVs can be filled by electrochemical deposition. Therefore, this deposition technique requires a seed layer that should have a homogenous thickness in all structures. A thin Cu layer deposited by PVD is used as seed layer in Cu damascene applications. However, in vias with high aspect ratios the deposited Cu layer will become thinner with increasing depth and can be discontinuous at the bottom of TSV. Here, a complete fill by electrochemical deposition is impossible. Therefore, a conformal seed layer deposited by Cu CVD can be applied in HAR patterns.

The requirement of a homogenously thick Cu layer also demands modifications in the CVD process for high conformality. Reduction of the deposition temperature leads to high step coverage of Cu films in TSVs. In addition, the deposition pressure can be reduced to further improve step coverage achieved for very aggressive aspect ratios of 20 and more. This influences the deposition rate only marginally. The lower total pressure enables a longer mean free path of the reactants so that the precursor molecules can reach the bottom of the vias. The desorption of $Cu(hfac)_2$ from the surface is enhanced as well as the diffusivity in the gas phase. This is also noticed in the pump down steps after the deposition. The initial pressure before deposition can be reached in shorter time due to the lower residence time of the by-products in the

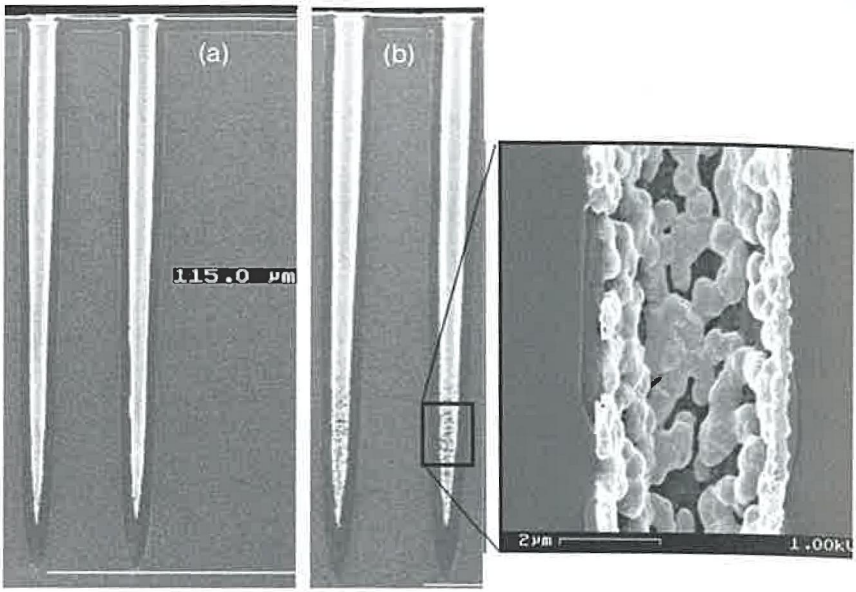


Figure 9.7 Step coverage of a Cu CVD seed layer in aggressive aspect ratios >20 : 1: (a) deposited at lower total pressure, giving a continuous film, and (b) deposited at higher total pressure – agglomeration of Cu grains due to the adhesion anneal and too low thickness achieved in the lower via region.

reactor. The application as seed layer for Cu ECD requires a homogenous Cu layer thickness. The lowest CVD Cu seed layer thickness for plating processes should be at least 120 nm to avoid agglomeration of Cu grains during the adhesion temperature anneal. As shown in Figure 9.7, the reduced step coverage leads to thinner films that agglomerate during subsequent temperature steps. Discontinuous films are unsuitable for the electroplating process to further fill the TSVs. The process with lowered total process pressure yields conformal and continuous Cu films suitable as seed layers for Cu ECD.

9.3.4 Tungsten CVD Application to TSV Fill

Conformal W-CVD processes require an appropriate barrier/seed layer film to be deposited on SiO_2-surfaces without peeling. A thin TiN barrier layer, approx. 20–30 nm thick, is sufficient for this purpose (Section 9.3.1). The chosen thickness of the TiN layer depends on the lateral size, the taper angle and the aspect ratio of the TSV to be metallized. Once the barrier film is deposited, the wafer is transported directly to the W-deposition chamber under vacuum. The TSV W-fill process is carried out in four steps:

Step 1: Heat to 430 °C, H_2-purge and W-nucleation layer deposition. Nucleation on adhesion layers like TiN is carried out by silane reduction of the WF_6 to form a thin,

uniform W-layer, thus improving the film quality of the subsequent via-fill process [31].

$$3SiH_4 + 2WF_6 \rightarrow 2W + 3SiF_4 + 6H_2$$

Step 2: W-via fill process (bulk deposition) of conformal W up to ~1100 nm, which is a surface-reaction-rate-limited process [32]. The final thickness is determined by the maximum lateral TSV size to be filled. The bulk deposition step uses hydrogen reduction of the WF_6. The deposition rate mainly depends on the wafer temperature and the WF_6-flow.
Deposition rate for a typical W-Via-fill process at 430 °C is ~300 nm min^{-1}. The sheet resistance of a 1100 nm thick W-film is in the range of 95–100 mΩ cm^{-2}; the extrinsic film stress (tensile) is ~0.95 GPa. Surface roughness is ~17 nm (R_a), measured by AFM after deposition of 1100 nm W and plasma etch back to ~400 nm remaining thickness. The maximum achievable W-film thickness is mainly limited by the comparably high film stress, which reaches the GPa range once 1 µm film thickness is exceeded. Si wafers with the above-mentioned film thickness and stress can reach wafer bow levels of 300 µm and higher, which in turn can cause handling problems with some robot types. Besides this, peeling of the W-film has also been observed, depending on the subsequent dielectric layers and the adhesion of the TiN to the underlying SiO_2.

Step 3: W-interconnect process to eventually close any gaps on top of the TSV-hole; this is a transport-limited process with reduced WF_6 flow and a 20% slower deposition rate and lower step coverage. The need for an additional W-interconnect deposition step depends strongly on the shape and size of the TSVs to be filled. Tapered TSVs result in almost void-free filling; thus the main W-via fill process is sufficient. If voids are expected due to rather vertical sidewall angles of the TSVs, an additional W-interconnect step is helpful to reduce the attack of the top W-layer during W-etch back.

Step 4: Plasma chamber clean with an F-containing etching gas after every wafer. For example, NF_3 is a commonly used gas for a W cleaning process.

9.4
Complete TSV Metallization Including Filling and Etchback/CMP

9.4.1
W-CVD Metallization

After the TSVs are isolated by a dielectric layer, for example by a conformal deposition of a SACVD based ozone-TEOS film (Chapter 6), the W-CVD metallization and subsequent W etch back can be performed. Since CVD of W requires processing temperatures in the 400 °C range, the dielectric isolation film inside the TSVs must sustain the same temperature level. The complete process sequence is carried out as follows:

After the isolation of the TSVs is completed, a full *in situ* process sequence under vacuum is performed, consisting of an Ar pre-sputtering step in the W etch back chamber (RIE), multiple deposition/etch steps to achieve a 20 to 30 nm thick, plasma densified TiN seed layer in the TiN-MOCVD chamber, followed by ~1100 nm W CVD, cool down under vacuum and partial etching of the W in the W etch back chamber.

Since relatively thick W-layers are required to fill the TSV-holes, a partial blanket W etch back to a remaining film thickness <500 nm is carried out, thus avoiding any peeling or delamination of the W-layer. A conventional RIE plasma chamber with an SF_6-based etch chemistry can be used for the partial blanket W-etch step as well as for the following structured W-etch step described below. The partial etch back also helps decrease the wafer bow to a moderate level, so wafers can be handled normally into a lithography tool, that is, a wafer stepper. By use of a photoresist mask, a PR-structured W etch is done afterwards to remove the remaining W after *in situ* partial W etch back. The remaining W film is structured in such a way that the area of the original TSV plus some overlap is fully covered with photoresist (light field mask). Therefore, excessive etch attack on the W inside the TSV is avoided during W-etch. The first stop layer is the thin TiN-layer, preventing the underlying oxide being etched excessively during the W over-etching step. Finally, the remaining TiN layer is etched with chlorine chemistry, so that the TSVs are electrically isolated from each other and can be further integrated.

Figure 9.8 shows a typical W-filled TSV (20 µm depth) after the completed W-structuring sequence as a cross-section (left) and from the top (right). The achievable conformality of the W-CVD step depends mainly on the taper angle and the aspect ratio of the TSV and is >80% for a TSV with a 10 : 1 AR at 3 µm lateral size (trench width). The left W-filled TSV shows part of the formerly produced dielectric

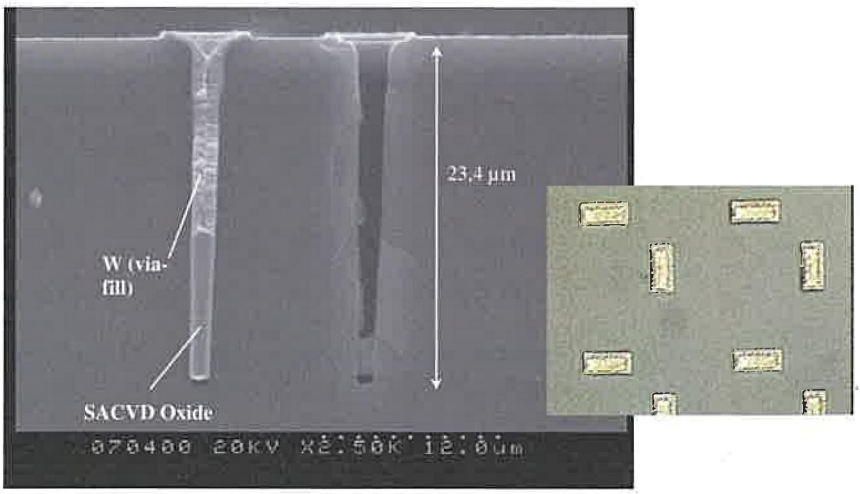


Figure 9.8 SEM-image (left) and top-view micrograph image (right) of a W-filled TSV, AR > 10 : 1, taper angle 88° (HBr-chemistry) after a structured W-etch step.

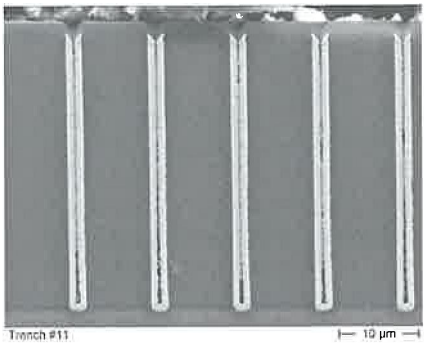


Figure 9.9 SEM-image of a W-filled TSV, AR > 15 : 1, taper angle 89.5° (SF_6/C_4F_8-chemistry), after blanket W etch back.

isolation layer (ozone-TEOS based SACVD film) and also the W-film inside of it at the upper part of the TSV. (Owing to its stiffness and hardness the W-film in the right tungsten filled plug was completely removed while cleaving the sample).

A void free W-fill result is difficult to achieve for HAR TSVs; the taper angle of the formerly fabricated TSV is the main parameter for the size of the void. Figure 9.9 shows an SEM image of a W-filled TSV with an aspect ratio >15 : 1 and a taper angle of 89.5°, resulting in a noticeable void.

Besides the above-mentioned possibility of an W etch back process, CMP of W could also be applied to polish the remaining bulk tungsten until the underlying dielectric layer is reached, thus resulting in electrically isolated TSV with negligible topography.

9.4.2 Cu CVD Metallization

In case of copper metallization for TSV fill the process sequence has been set up as follows.

After TSV isolation, TiN barrier deposition is carried out. To meet the demands of a diffusion barrier the TiN barrier should be ~ 20 nm thick in the lower region of TSV. With smaller sizes and higher aspect ratios the step coverage decreases. Therefore, the deposited barrier thickness should be chosen with respect to the TSV geometry. We apply TiN barrier thickness in the range 30 nm on top for larger TSV and up to 90 nm for smaller diameters for depths between 20 and 50 µm. Deposition of the adhesion layer TiN takes place in the same deposition chamber as for the barrier, but at lower temperatures. In contrast to the TiN barrier deposition this is a pure plasma enhanced process. The Cu deposition process is accomplished in situ, without vacuum break. After the complete TSV fill a thermal treatment is necessary to obtain sufficient adhesion between the adhesion layer and the Cu. This thermal treatment is carried out in one of the CVD chambers of the P5000 cluster tool. The wafer is treated in vacuum at a susceptor temperature range of 380–420 °C for 3–5 min. Without this temperature anneal the layer stack does not pass the following

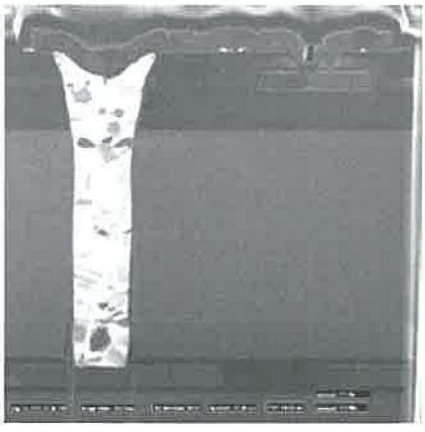


Figure 9.10 Complete CVD-Cu filled TSV after thinning and top and bottom metallization (tilted FIB cross-section).

CMP process. Chemical Mechanical Polishing removes the surplus copper as well as the TiN barrier/adhesion layer from the top of the wafer. Usually, this requires two steps. In a first step the protruding Cu is removed, while the second step removes the TiN layer. Different slurries with defined selectivity are used for these processes to achieve well-insulated, in-plane TSVs and to avoid issues like dishing and copper corrosion.

Subsequent to the CMP, insulator depositions and interconnect processing using Al or Cu damascene metallization is carried out for assembling the interconnection between the TSVs and/or the stacked chips. Figure 9.10 shows an example of a TSV completely filled by CVD-Cu after thinning and top and bottom metallization.

9.5 Conclusions

Both W CVD and Cu CVD can be used for the metallization of TSVs. Depending on the lateral TSV size, either a complete CVD-based TSV fill or the use of CVD as a seed layer with a subsequent electroplating process to complete the fill is employed. A complete fill by CVD is generally applicable for small TSV diameters in the range of up to ~3 µm, especially at high aspect ratios. This limitation to comparably small TSV sizes is due to the metal properties and also to the deposition process itself. The W fill process is stress limited. The Cu fill process is determined by efficiency factors, such as precursor costs and the relatively long processing times. New precursor developments could make the present Cu CVD process more efficient.

Both processes are highly qualified for making seed layers. The high conformality of the CVD allows for a film deposition with homogenous thickness on top and in the TSV structures. Homogenous film thickness is a major condition for equal current density distribution in electroplating processes, thus enabling void-free filling.

References

1 Temple, D., Bower, C.A. *et al.* (2007) in 2006 MRS Symposium Proceedings, volume 970, 0970-Y03-04, p. 115–117.

2 Wieland, R. *et al.* (2007) in Smart Systems Integration 2007, 649, Verlag GmbH, 978-3-8007-3009-4.

3 Ramm, R. *et al.* in AMC 2001 Proceedings, 159, 1-55899-670-2.

4 Sakuma, K. *et al.* ECTC 2007 Proceedings, 627, IEEE 1-4244-0985-3/07/

5 Kim, B. (2007) 2006 MRS Symposium Proceedings, 970, 253 0970-Y06-02, p. 259–260.

6 Burkett, S., Schaper, L. *et al.* (2007) in 2006 MRS Symposium Proceedings, 970, 0970-Y06-01, p. 261–273.

7 Wang, S.-Q. *et al.* (1996) *Journal of Vacuum Science & Technology*, **14** (3), 1846.

8 Rossnagel, S.M. and Kim, H. (2001) 2001 Proceedings IITC, pp. 3–5.

9 Tsang, C.K. *et al.* (2007) *Materials Research Society Symposium Proceedings*, **970**, p. 261–273.

10 Körner, H. and Seidel, U. (1994) in 1993 Advanced Metallization for ULSI Appl. VII, MRS, p. 513.

11 Ohshita, Y. *et al.* (1995) *Journal of Crystal Growth*, **146**, 188–192.

12 Hillmann, J. *et al.* (July 1995) *Solid State Technology*, **38**, p. 147.

13 Chang, Y.H. *et al.* (1996) *Applied Physics Letters*, **68** (18), 2580.

14 Weber, A., Gross, M.E. *et al.* (1995) *Journal of the Electrochemical Society*, **142** (6), L79.

15 Tsau, L. *et al.* (1996) in 1996 VIMC Conference, Vol. 106, p. 596–598.

16 Leutenecker, R. *et al.* (1995) *Thin Solid Films*, **270**, 621–626.

17 Paranjpe, A. and Islam Raja, M. (September/October 1995) *Journal of Vacuum Science & Technology B*, **13**, p. 2105–2114.

18 Kodas, T. and Hampden-Smith, M. (1994) *The Chemistry of Metal CVD*, VCH, Weinheim, 3-527-29071-0.

19 Kim, C.K. *et al.* (2003) Chemical Vapour Deposition XVI and EUROCVD 14. Electrochemical Society Proceedings, PV, 2003-08 (2), p. 1284.

20 Kim, K. and Yong, K. (2003) Chemical Vapour Deposition XVI and EUROCVD 14. Electrochemical Society Proceedings, PV, 2003-08 (2), 1290, 1-56677-378-4.

21 Das, M. and Shivashankar, S.A. (2007) *Applied Organometallic Chemistry*, **21**, 15–25.

22 Röber, J., Kaufmann, C. and Gessner, T. (1995) *Applied Surface Science*, **91**, 134–138.

23 Joulaud, M., Angekort, C., Doppelt, P. *et al.* (2002) *Microelectronic Engineering*, **64**, 107.

24 Joulaud, M. *et al.* (2003) Chemical Vapour Deposition XVI and EUROCVD 14. Electrochemical Society Proceedings, PV, 2003-08 (2) p. 1268. 1-56677-378-4.

25 Blewer, R.S. (1988) Tungsten and Other Refractory Metals for VLSI Applications. Proceedings of the 1988 Workshop Held October 4–6, Albuquerque, USA Materials Research Society Conference Proceedings, (ed. Carol M. Conica), p. 65–76.

26 Riedel, S., Schulz, S.E. and Gessner, T. (2000) *Microelectronic Engineering*, **50**, 533.

27 Ecke, R. *et al.* (2003) Chemical Vapour Deposition XVI and EUROCVD 14 (eds Allendorf, M., Maury, F and Teyssandier, F), Electrochemical Society Proceedings, PV, 2003-08 (2), p. 1284.

28 Riedel, S., Weiss, K., Schulz, S.E. and Gessner, T. (2000) AMC 1999 Proceedings, p. 195, 1-55899-539-0.

29 Gandikota, S. *et al.* (2000) *Microelectronic Engineering*, **50**, 547.

30 Yang, D., Hong, J., Richards, D.F. and Cale, T.S. (2002) *Journal of Vacuum Science & Technology B*, **20** (2), 495–506.

31 Körner, H. and Seidel, U. (1994) *Advanced Metallization for USLI Applications 1993* (ed. Fareau *et al.*), MRS, Pittsburgh, PA, p. 513.

32 Körner, H. *et al.* (1991) *Tungsten and other Refractory Metals for ULSI VII* (eds R. Blumenthal and G. Smith), MRS, Pittsburgh, PA, p. 369