

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SONY GROUP CORPORATION,  
Petitioner,

v.

VISIONX TECHNOLOGIES, LLC,  
Patent Owner.

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Case No. TBD  
Patent No. 8,035,143

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**DECLARATION OF MICHAEL GUIDASH**

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| Sony Exhibit 1003<br>Sony v. VisionX |
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## **I. INTRODUCTION**

I, Michael Guidash, declare:

1. I, R. Michael Guidash, have been retained by counsel to render certain opinions as an expert witness, for the above-referenced *inter partes* review (“IPR”) proceeding regarding U.S. Patent No. 8,035,143 (“the ’143 patent,” Ex. 1001). In connection with my analysis, I have reviewed the ’143 patent, the respective file history, and the documents listed in Section IV (which starts on page 8). I have been asked to provide a declaration regarding my opinions on the validity of claims 1-4 (the “Challenged Claims”) of the ’143 patent.

2. This declaration sets forth the opinions I have formed in this IPR and provides the bases and reasons for those opinions. I have summarized my educational background, professional experience, and publications herein and have attached my complete curriculum vitae, labeled as Exhibit 1004.

3. This report is based on information currently available to me. I declare that I have personal knowledge of the facts set forth in this declaration and, if called to testify as a witness, could and would do so competently.

4. I am being compensated at my usual consulting rate of \$600.00 per hour, plus actual expenses, for my work on this matter. My compensation is in no way dependent upon my opinions or testimony or the outcome of this proceeding.

## II. SUMMARY OF OPINIONS

5. For reasons that I will address in more detail below, it is my firm belief and opinion that, at the time of the purported invention claimed by the '143 patent, the Challenged Claims would have been anticipated or obvious to a person having ordinary skill in the art ("POSA").

6. **Petition Ground 1:** Claims 1-3 would have been obvious over Sumi because Sumi discloses an image sensor comprising a semiconductor substrate, an interconnecting layer, a connection via having a projection part, an insulating layer, a pad, and the insulating part having a thickness thinner than the projection height of the projection part of the connection via. Although Sumi does not specifically state the interconnection layer, connection via, and pad are metal, fabricating these interconnections using metal would have been a standard way for POSAs to implement Sumi's disclosed sensor and would have offered well-known benefits. POSAs would have known how to implement these structures using metal and the use of metal would have yielded predictable results. POSAs also would have known it would be advantageous to use tetraethyl orthosilicate ("TEOS") in the oxide insulating layer disclosed in Sumi.

7. **Petition Ground 2:** Claims 2 and 4 would have been obvious over Sumi in view of Yanagida-2 because Yanagida-2 discloses TEOS as an insulating layer and a protective layer formed on the insulating layer, both of which POSAs

would have recognized as desirable to incorporate into Sumi's sensor when implemented in accord with Ground 1.

8. **Petition Ground 3:** Claims 1-3 would have been obvious over Shiraiwa in view of Sumi. Shiraiwa's sensor meets every element of claims 1-3, except a connection via having a projection part and a metal pad covering the projection part. However, it would have been obvious to implement Shiraiwa's sensor with a connection via metal and metal pad as disclosed in Sumi to electrically connect the on-chip lens to the interconnection layer. It would also have been obvious for the connection via metal to have a projection part projecting from the second surface, as disclosed in Sumi, to improve the structure and function of the device.

9. **Petition Ground 4:** Claims 2 and 4 would have been obvious over Shiraiwa in view of Sumi and Yanagida-2 because Yanagida-2 discloses TEOS as an insulating layer and a protective layer formed on the insulating layer, both of which POSAs would have recognized as desirable to incorporate into Shiraiwa's sensor when implemented in accord with Ground 3.

10. **Petition Ground 5:** Claims 1-3 would have been obvious over Yanagida-1 because Yanagida-1 discloses an image sensor comprising a semiconductor substrate, an interconnecting layer, a connection via having a projection part, an insulating layer, a pad, and the insulating part having a

thickness thinner than the projection height of the projection part of the connection via. Although Yanagida-1 does not specifically state the interconnection layer and pad are metal, fabricating these interconnections using metal would have been a standard way for POSAs to implement Yanagida-1's disclosed sensor and would have offered well-known benefits, as previously noted in connection with Grounds 1 and 3.

11. **Petition Ground 6:** Claims 2 and 4 would have been obvious over Yanagida-1 in view of Yanagida-2 because Yanagida-2 discloses TEOS as an insulating layer and a protective layer formed on the insulating layer, both of which POSAs would have recognized as desirable to incorporate into Yanagida-1's sensor when implemented in accord with Ground 5.

### **III. PERSONAL AND PROFESSIONAL BACKGROUND**

12. A description of my professional background and qualifications is provided below. An additional account of my work experience and qualifications is included in my curriculum vitae, which is labeled as Exhibit 1004.

13. I started my career with Eastman Kodak as a product engineer for Photometer ASICs for Kodak film cameras after graduating with a Bachelor of Science in Electrical Engineering from the University of Delaware in 1981. In 1986, I transferred to the Kodak Research Laboratories and CCD wafer fabrication facility. During my time with the Kodak Research Laboratories and CCD wafer

fabrication facility, I developed 2 micrometer ( $\mu\text{m}$ ) and 1 $\mu\text{m}$  CMOS processes, and a 30V 4 $\mu\text{m}$  BiCMOS process. These processes were used for gate arrays for many Kodak products and output driver ASICs for all of Kodak's copiers. During this time, I was also awarded entrance into the Special Opportunity Graduate Program allowing me to obtain a Master's of Science in Electrical Engineering from the Rochester Institute of Technology.

14. In 1989, I transferred to the Smart Sensor Group, which developed BiCMOS-CCD processes to provide fully integrated CCD systems on a chip. I also served as a product engineer and yield-enhancement engineer for Kodak's CCDs. During this time, I led product delivery and technology development of all ASIC and smart-sensor products. I developed a number of products during this time to include (1) an interline CCD integrated with 2 $\mu\text{m}$  CMOS on the same chip, (2) the world's first pinned-photodiode Active Pixel CMOS Sensor product, and (3) linear CCD image sensors with on-chip timing and control. I also led and directed the CCD dark current and point-defect reduction team.

15. In 1996, I formally started the CMOS Image Sensor group at Kodak. From 1996 to 2009, I managed the research and development and product development of CMOS Image Sensor (CIS) programs. As further shown in my curriculum vitae, I was the inventor or co-inventor of many key patents in the field of CMOS image sensors. The inventions of these patents include Pinned

Photodiode Pixels, Camera-on-a-Chip architecture, and shared amplifier pixel architectures. During this time, I also led development of the world's first pinned-photodiode CIS product, a Megapixel CIS device, and a shared amplifier CIS pixel product. Further, I led development of the world's first half-inch optical format 1.3 megapixel CMOS image sensor for mass production, which was successfully implemented into several compact digital camera products. I also led the development of an early 3D hybrid stacked BSI CIS architecture. This led to demonstration of very high performance, low-dark current BSI prototype sensors with pixel sizes ranging from 0.9 $\mu\text{m}$  to 5.0 $\mu\text{m}$ .

16. Much of my experience in CIS development was directed to working with various wafer foundry partners to modify their baseline CMOS process flows for use in manufacturing high quality CIS devices for Kodak. Wafer foundry partners included Motorola, Intel, Tower Semiconductor, IBM and TSMC. The process modifications included incorporation of additional process steps for formation of the photodetector structure, as well as modification of the metal interconnect processes to optimize optical performance.

17. One such project related to optical performance done with IBM from 2003-2005, was implementation of a thin copper (Cu) metallization. This project was directed to reducing the optical stack height of the CIS device so that the microlens in each pixel could be more effective at focusing light from a wide set of

incident angles on the photodetector in the pixel. This was a key performance metric required for low-cost CIS devices used in cell phone cameras. The replacement of the standard aluminum-based metallization with Cu metallization enabled making the optical stack shorter without affecting the electrical and clock skew performance of the pixel array readout, due to the low resistivity of Cu. This project also included modification of the Cu barrier layer, (from silicon nitride to a cobalt tungsten phosphorous alloy (CoWP)), to reduce reflections in the dielectric stack above the photodiode in order to increase the amount of light transmitted to the photodiode.

18. In late 2009, when Eastman Kodak closed its CMOS Image Sensor Business, I transitioned into a role as an intellectual-property technologist and coordinator. This role included managing the remaining image sensor patent applications and respective office actions, managing broad electronic components patent applications and respective office actions, and providing technical support for intellectual property sales and licensing teams.

19. In early 2012, I left Eastman Kodak and transitioned into a role of providing technical consulting services relating to CMOS image sensors. In this role I provide consulting services for process, pixels, circuits, sensor architectures, systems, and intellectual property to companies and clients.

#### IV. MATERIALS REVIEWED AND CONSIDERED

20. My findings, as explained below, are based on my years of education, research, experience, and background in the field of CMOS image sensors and BSI image sensors, as well as my investigation and study of relevant materials for this declaration. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth in Section VI below. In forming my opinions, I have studied and considered the materials identified in the list below.

| Exhibit | Description                                                                                                                                                                                                                                                                                                                           |
|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1001    | U.S. Patent No. 8,035,143 (“the ’143 patent”)                                                                                                                                                                                                                                                                                         |
| 1002    | Prosecution History of U.S. Patent No. 8,035,143                                                                                                                                                                                                                                                                                      |
| 1005    | U.S. Patent Publication No. US 2006/0094151 A1 (“Sumi”)                                                                                                                                                                                                                                                                               |
| 1006    | Certified English Translation of Japanese Publication No. JP 2006-032497 A (“Yanagida-1”)                                                                                                                                                                                                                                             |
| 1007    | Certified English Translation of Japanese Publication No. JP 2006-339566 A (“Yanagida-2”)                                                                                                                                                                                                                                             |
| 1008    | Certified English Translation of Japanese Patent Publication No. JP 2005-353996 A (“Shiraiwa”)                                                                                                                                                                                                                                        |
| 1009    | U.S. Patent No. 7,875,948 (“Hynecek”)                                                                                                                                                                                                                                                                                                 |
| 1010    | “Sony develops back-illuminated CMOS image sensor, realizing high picture quality, nearly twofold sensitivity(*1) and low noise”, Sony Group Portal - Sony Global Headquarters (June 11, 2008), <a href="https://www.sony.com/en/SonyInfo/News/Press/200806/08-069E/">https://www.sony.com/en/SonyInfo/News/Press/200806/08-069E/</a> |
| 1011    | U.S. Patent Publication No. US 2006/0076590 A1 (“Pain-1”)                                                                                                                                                                                                                                                                             |
| 1012    | U.S. Patent Publication No. US 2007/0117254 A1 (“Pain-2”)                                                                                                                                                                                                                                                                             |
| 1013    | Jean-Luc Leray et al., An Overview of Buried Oxides on Silicon: New Processes and Radiation Effects. Journal de Physique III, EDP Sciences, 1996, 6 (12), 1625-1646 (“Leray”)                                                                                                                                                         |
| 1014    | Michael Quirk and Julian Serda, Semiconductor Manufacturing Technology, 257-333 (2001) (“Quirk”)                                                                                                                                                                                                                                      |
| 1015    | Metallization by Chemical Vapor Deposition of W and Cu, 1 in Handbook of 3D integration: Technology and applications of 3D                                                                                                                                                                                                            |

|      |                                                                                                                                                                            |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | Integrated Circuits (Philip Garrou, Christopher Bower & Peter Ramm, eds., 2008) (“Garrou”)                                                                                 |
| 1016 | British Library Public Availability Date Authentication Letter                                                                                                             |
| 1017 | Garrou Vol. 1 Public Availability Date Authentication                                                                                                                      |
| 1018 | Declaration of Mary Bolin                                                                                                                                                  |
| 1019 | H. C.M Knoops et al., “Deposition of TiN and TaN by Remote Plasma ALD for Cu and Li Diffusion Barrier Applications” Journal of The Electrochemical Society (Oct. 10, 2008) |
| 1020 | Japanese-language Publication of Japanese Publication No. JP 2006-032497 A                                                                                                 |
| 1021 | Japanese-language Publication of Japanese Publication No. JP 2006-339566 A                                                                                                 |
| 1022 | Japanese-language Publication of Japanese Publication No. JP 2005-353996 A                                                                                                 |
| 1023 | U.S. Patent Publication No. US 2005/0179053 A1 (“Ezaki”)                                                                                                                   |
| 1024 | McGraw-Hill, McGraw-Hill Dictionary of Scientific and Technical Terms (6th ed. 2003) (“McGraw-Hill”)                                                                       |
| 1025 | Electrical Engineering Dictionary (Phillip A. Laplante et al. eds., 2000) (“Laplante”)                                                                                     |
| 1026 | Robert S. Patti, “Three-Dimensional Integrated Circuits and the Future of the System-on-Chip Designs,” Proceedings of the IEEE, vol. 94, no. 6, 1214-1224, 2006 (“Patti”)  |

## **V. UNDERSTANDING OF APPLICABLE LEGAL STANDARDS**

21. Although I am not an attorney, I have a general understanding of the applicable legal standards pertaining to the patentability issues presented in this proceeding based on my work experience both at Kodak and in my time as a consultant.

### **A. Burden of Proof**

22. I understand that, in this IPR, Petitioner has the burden of proving that each challenged claim is unpatentable by a preponderance of the evidence. I understand that “preponderance of the evidence” means that a fact or conclusion is more likely true than not true.

### **B. Anticipation**

23. I understand that one way a patent claim may be invalid is if it is “anticipated” by the prior art. I understand that, for a patent claim to be “anticipated” by the prior art, each and every limitation of the claim must be found, expressly, implicitly or inherently, in a single embodiment found in a prior art reference.

24. I understand that a claim limitation is implicit in a prior art reference if POSA understood the reference to disclose the limitation based on inferences that a POSA would reasonably be expected to draw from the express teachings in the reference when read in light of the POSA’s knowledge and experience.

25. I understand that a claim limitation is inherent in a prior art reference if that limitation is necessarily present when practicing the teachings of the reference, regardless of whether a POSA recognized the presence of that limitation in the prior art.

**C. Obviousness**

26. I understand that a patent claim is unpatentable if, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of the prior art to yield the patent claim. I also understand that it is not required (although it is acceptable) that each element of a patent claim be found in a single reference in order to find a patent claim obvious. For a patent claim to be found obvious, all the elements of the patent claim may be found in a combination of references at which a POSA would have been reasonably expected to arrive. I understand that a proper analysis of whether an invention is unpatentable for obviousness includes a review of the scope and content of the prior art, the differences between the patent claims at issue and the prior art, the level of ordinary skill in the field of the invention at the time of the invention, and other objective considerations identified below.

27. I understand that a showing of obviousness requires some articulated reasoning with a rational underpinning to support the combination of the references. I understand that in consideration of the issue of obviousness it is

important to identify whether a reason existed at the time of the invention that would have led a POSA to combine elements of the references in a way that yields the claimed invention.

28. I understand that a claim may be considered unpatentable for obviousness for various reasons. I have been informed that the following exemplary rationales may support a finding of obviousness:

- A. combining prior art elements according to known methods to yield predictable results;
- B. simply substituting one known element for another to obtain predictable results;
- C. use of a known technique to improve similar devices in the same way;
- D. applying a known technique to a known device ready for improvement to yield predictable results;
- E. choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- F. known work in a field that prompts variations in the work in the same or a different field that leads to predictable results; and
- G. some teaching, suggestion, or motivation in the prior art that would have led a POSA to modify a prior art reference or combine

multiple prior art references or teachings to arrive at the claimed invention.

29. I understand that various objective or “real world” factors may be indicative of non-obviousness. I understand that such factors include:

- A. the commercial success of the claimed invention;
- B. the existence of a long-felt, unresolved need for a solution to the problem solved by the claimed invention;
- C. failed attempts to solve the problem solved by the claimed invention;
- D. copying of the claimed invention;
- E. unexpected results of the claimed invention;
- F. praise for the claimed invention by others in the relevant field; and
- G. willingness of others to accept a license under the patent because of the merits of the claimed invention.

## **VI. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)**

30. I have been informed and understand that for purposes of assessing whether prior-art references disclose every element of a patent claim (thus “anticipating” the claim) and/or would have rendered the claim obvious, the patent and the prior-art references must be assessed from the perspective of a POSA to which the patent is related, based on the understanding of that person at the time of

the patent claim's priority date. I have been informed and understand that a POSA is presumed to be aware of all pertinent prior art and the conventional wisdom in the art, and is a person of ordinary creativity. I have applied this standard throughout my declaration.

31. The '143 patent involves technology in the field of backside illuminated image sensors. I have been asked to provide my opinions as to the state of the art in this field prior to November 5, 2008. I use this timeframe because the face of the '143 patent indicates an earliest claimed priority date of November 5, 2008. Whenever I offer an opinion in this declaration about the knowledge of a POSA, the manner in which a POSA would have understood the claims of the '143 patent or its description, the manner in which a POSA would have understood the prior art, or what a POSA would have been led to do based on the prior art, I am referencing the November 5, 2008 timeframe, even if I do not say so specifically in each case.

32. In my opinion, a POSA prior to November 5, 2008 would have had a Bachelor's degree in electrical engineering, physics, microelectronics, or material science, and at least 3-5 years of industrial experience or equivalent research or teaching experience, or a Master's degree in the same fields and 1-3 years of industrial experience or equivalent research or teaching experience in the field of semiconductor image sensor design and fabrication. More education could

substitute for experience, and vice versa. This person would have been capable of understanding and applying the teachings of the '143 patent and the prior-art references discussed in this declaration.

33. By 2008, I held a Bachelor's of Science and a Master's of Science in Electrical Engineering, and I had over 20 years of experience with imaging devices and sensors. Therefore, I was a person of more than ordinary skill in the art during the relevant timeframe. However, I worked with many people who fit the characteristics of the POSA, and I am familiar with their level of skill. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth above.

## **VII. CLAIM CONSTRUCTION**

34. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a POSA in the context of the entire patent and the prosecution history pertaining to the patent. I understand that when construing claim terms that are terms of art, that the claim term should be construed in a manner consistent with the scientific and technical context in which it is used in the patent. But, if the specification provides a special definition for a claim term that differs from the meaning the term would otherwise possess, the specification's special definition controls.

35. I have applied these standards in preparing the opinions in this declaration.

### **VIII. THE '143 PATENT**

36. The '143 patent was filed on November 2, 2009 and claims the benefit of Korean Application No. KR 10-2008-0109560 A filed on November 5, 2008. I have been asked to assume, for purposes of this declaration, that the '143 patent is entitled to a priority date of November 5, 2008.

37. The '143 Patent and Challenged Claims concern backside-illuminated (“BSI”) image sensors for converting light<sup>1</sup> into electrical signals, including those incorporating complementary metal-oxide semiconductor (“CMOS”) technology.

38. By 2008, BSI CMOS image sensors had been disclosed as an alternative to traditional frontside-illuminated (“FSI”) sensors. Pain-1 (Ex. 1011), [0003]-[0004]. As illustrated in the figure below ¶39, the metal wiring in FSI sensors is provided between the lenses and the photodiodes formed in the substrate prevents some portion of the light from reaching the photodiode. That arrangement can reduce light collection efficiency and sensitivity because the metal layers must be positioned in the pixels to connect the in-pixel transistors for operation and readout of the pixel. Sumi (Ex. 1005), [0004]. The metal layers are not placed over

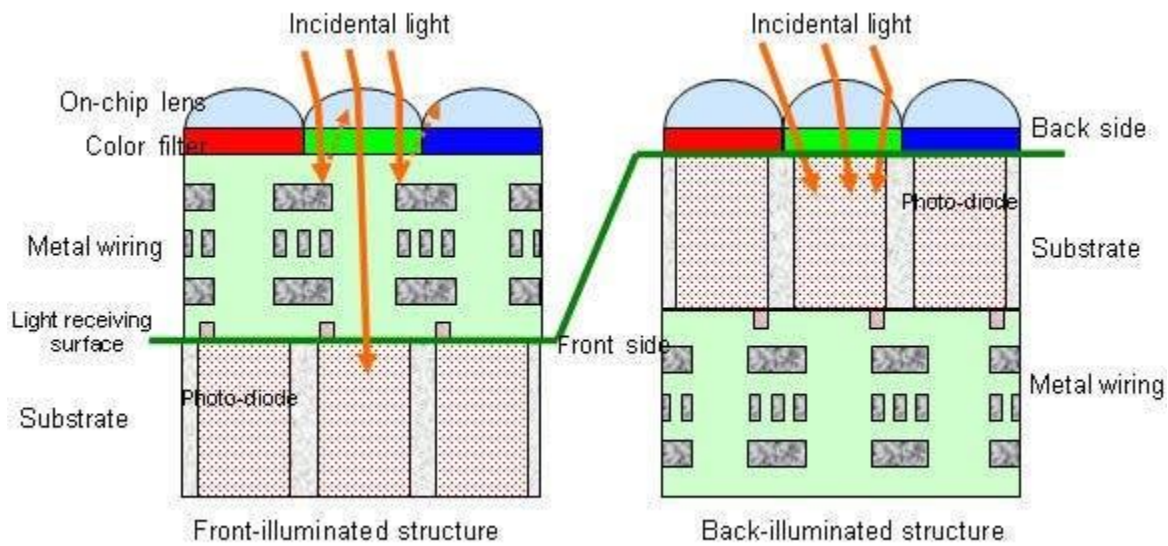
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<sup>1</sup> Light is a type of electromagnetic radiation. In particular, “light” often refers to radiation that has a wavelength within the visible spectrum of about 380 nm to about 750 nm.

the photodiodes so incident light can reach the photodiodes. Instead, the metal layers create an aperture or window of metal lines surrounding the photodiode. Having multiple layers of metal interconnections (typically three, as shown below) can create a tall and narrow aperture over the photodiode that makes it difficult to efficiently focus light on the photodiode. This is especially difficult as pixel sizes shrink to provide higher resolution image sensors. Additionally, for very small pixels, (less than 2 microns), the aperture will become smaller than the wavelength of visible light which then produces diffraction of the incident light. As a result of the above effects, only a fraction of the light incident on the on-chip lenses is converted to charge and collected by the corresponding photodiodes, thereby reducing the image quality of the sensor.

39. Apart from issues with poor collection efficiency, low sensitivity, FSI sensors also suffer from low quantum efficiency (QE), increased cross-talk, and

poor angular response. Pain-1, [0007]; Ex. 1010.



40. Unlike traditional FSI sensors, BSI sensors position the sensor circuitry behind a photosensitive layer to minimize the amount of light that is blocked from reaching the photodiode for detection as seen above.

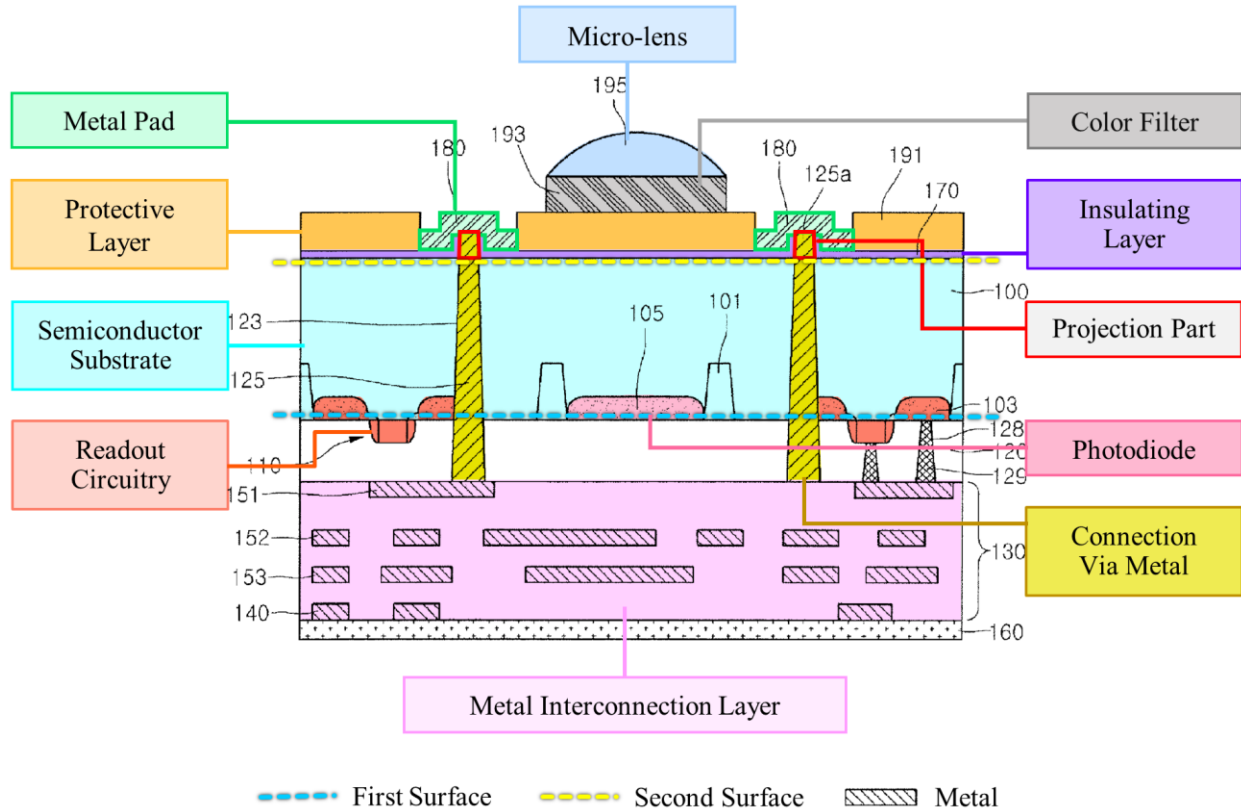
41. BSI CMOS-based image sensors had been described at least as early as 2004. Sumi, [0001]; Pain-1, [0001]. BSI sensors are formed by taking a conventional CMOS sensor wafer and bonding another substrate to the front side of the CMOS sensor wafer (the front side being the side where the transistors are formed and connected together with metal interconnections). Next, the CMOS sensor wafer undergoes a backside thinning process where a specified amount of silicon is removed from the backside surface (the surface opposite to the front side surface). The backside thinning process creates a thin layer of silicon left where the resulting new backside surface is very close to the photodiodes formed near the

front side surface. This allows the photodiodes to receive incident light from the backside of the device. Color filters and on-chip lenses are now placed on the backside surface rather than the front side surface.

42. The backside layers on BSI sensors are fabricated using low-temperature manufacturing processes to avoid impacting previously deposited components. *See* Pain-1, [0051]. The process begins with a wafer similar to those used in other CMOS manufacturing processes. *Id.*, [0069]. As described above, a CMOS sensor wafer is fabricated in the same manner as FSI sensor wafers, but the layout of the metal lines on the front side is modified since light will not be incident on the front side. The metal layers can be placed anywhere in the pixel which improves the electrical performance of the pixel. After completion of the standard CMOS wafer processing flow, the wafer is bonded to a carrier wafer or “handle,” then turned over. Sumi, [0014]; Pain-1, [0072]; Pain-2 (Ex. 1012), [0037]-[0038]. The rear side is then ground and etched away until the photoactive layer is exposed—allowing light to strike the photodiode. Sumi, [0015]; Pain-1, [0006]. Subsequent layers are then applied to the rear side. Pain-1, [0077].

#### **A. Described Embodiments**

43. The '143 patent discloses a BSI CMOS image sensor as seen below. An annotated cross-sectional view is shown below. *See* '143 patent (Ex. 1001), Fig. 9.



44. As seen in the figure, the claimed image sensor comprises a substrate 100 comprising transistors 110 (referred to as part of a readout circuitry) and photodiode area 105. '143 patent, 5:47-54; *see also id.*, 3:18-19, 3:26-31. The BSI sensor further comprises metal interconnection layer 130 formed on substrate 100 (*id.*, 3:36-37, 4:26-31), connection via metal 125 having a projection part 125a (*id.*, 4:57-60), an insulating layer 170 (*id.*, 5:4-9), and a metal pad 180 (*id.*, 5:43-49). In this embodiment, the liner oxide layer 170, namely an insulating layer, has a thickness thinner than the height of the projection part 125a along the vertical direction. The claimed image sensor further comprises a metal pad formed on the insulating layer such that the metal pad covers the projection part. In the

embodiment shown above, metal pad 180 is formed on insulating layer 170 and covers the projection part 125a.

**B. Prosecution History of the '143 Patent**

45. The application for the '143 patent was filed on November 2, 2009. '143 patent Prosecution History (Ex. 1002), 1. The Applicant subsequently filed an Information Disclosure Statement ("IDS") listing Yanagida-1 (Ex. 1006) and Japanese Patent Application No. JP 2005-150463 A ("Yamamoto"). Aside from the Japanese-language originals, Applicant submitted English-language abstracts of Yanagida-1 and Yamamoto. *Id.*, 71-119. The abstract submitted for Yanagida-1 did not disclose (1) the connection via metal with a projection part, (2) the oxide film in the antireflective layer discussed below, (3) a metal pad, and (4) the thickness of the insulation layer being less than the height of the projection part. *Id.*, 102.

46. The Examiner never cited these Japanese applications or the incomplete English-language abstracts. Instead, on February 25, 2011, the Examiner rejected the original independent claims and most of the dependent claims over English-language patent publications including US 2003/0081069 A1 (Kim et al.), US 2005/0029643 A1 (Koyanagi), US 2008/0111169 A1 (Liu et al.), and US 2008/0308893 A1 (Kirby et al.). Ex. 1002, 133-140. Neither the

Examiner's rejection nor the Applicant's IDS identified Sumi, Shiraiwa (Ex. 1008), or Yanagida-2 (Ex. 1007) as prior art.

47. In the Non-final Rejection, the Examiner found that Koyanagi taught a (1) semiconductor substrate comprising readout circuitry and a photodiode area, (2) a metal interconnection layer formed on a first surface of the substrate, (3) a connection via extending from the first surface to a second surface of the substrate, (4) an insulating layer formed on the second surface of the substrate, and (5) a pad formed on the insulating layer. Ex. 1002, 135-136. The Examiner stated that Kirby discloses the via is a via metal and the pad is a metal pad. *Id.*, 136. The Examiner also found that Kim discloses an insulating layer comprising a TEOS layer. *Id.*, 137-138. Further, Koyanagi discloses an insulating layer formed on a portion of the projection part extending from the second surface (claim 3) as well as a protective layer formed over the insulating layer and a micro-lens formed on the protective layer in a region corresponding to the photodiode area (claim 4). *Id.*, 136-137. The Patent Owner did not contest the Examiner's findings on these rejections. *Id.*, 148-154.

48. The Examiner found that originally-filed claim 2 recited allowable subject matter because the "cited art" did not "teach or render obvious an image sensor" in which "the insulating layer has a thickness thinner than a projection height of the projection part." *Id.*, 138-139. The Applicant subsequently

incorporated this limitation into independent claim 1, and the Examiner allowed the claims without further rejection over any prior art. *Id.*, 148-154, 157-162. However, Sumi (which was not of record during prosecution), Shiraiwa (which was not of record in during prosecution), and Yanagida-1 (which was of record, but never cited by the Examiner) teach this feature (*i.e.*, an insulating layer with a thickness thinner than a projection height of the projection part) despite the Examiner’s misunderstanding—based on an incomplete record—that these dimensions created a point of novelty.

### **C. The Challenged Claims**

49. I provide in Appendix A, attached hereto, a listing of claims 1-4 of the ’143 patent. I will refer throughout this declaration to the elements of the claims with reference to the number and letter designations that have been added in the left column (e.g., “[Preamble],” “[1A],” “[1B],” etc.).

## **IX. PRIOR-ART REFERENCES**

50. I briefly introduce in this Section below various prior-art references discussed in this declaration.

### **A. Sumi (Ex. 1005)**

51. Sumi published as a U.S. Patent Publication No. US 2006/0094151 A1 on May 4, 2006. Sumi, 1. I understand that Sumi is therefore indisputable prior art under pre-AIA 35 U.S.C. § 102(b).

52. Sumi discloses each limitation of claim 1 and 3 except that Sumi does not specify what material was used for the sensor's electrical interconnects—*i.e.*, the disclosed wiring layers, vertical vias and electrode pads. It would have been obvious to make Sumi's image sensor using industry-standard metal interconnections—thereby yielding a sensor falling within the scope of claims 1 and 3 of the '143 patent. Thus, the common and routine use of metal interconnects in Sumi's sensors render obvious claims 1 and 3.

53. Claim 2 requires that the sensor's insulating layer of the image sensor include a TEOS layer. It would have been obvious when manufacturing Sumi's sensor to incorporate a low temperature oxide layer such as TEOS (which was well known by 2008) to insulate the substrate on a CMOS sensor. The use of TEOS in Sumi's sensor renders obvious claim 2.

**B. Shiraiwa (Ex. 1008)**

54. Shiraiwa published as a Japanese Patent Publication No. JP 2005-353996 A on December 22, 2005. Shiraiwa, 2. I understand that Shiraiwa is therefore indisputable prior art under pre-AIA 35 U.S.C. § 102(b). Shiraiwa was published in Japanese (Ex. 1022) and a certified English translation is provided (Shiraiwa, 2-13).

55. Shiraiwa discloses each limitation of claim 1 except a connection via metal with a projection part and a metal pad covering the projection part. The use

of vertical via comprising a projection part and a metal pad covering the projection part to electrically connect the on-chip lens to the interconnection layer was well-known in the art. It would have been obvious to a POSA to implement a connection via metal to have a projection part projecting from the second surface.

56. Further, similar to Sumi, Shiraiwa does not specify what material was used for the sensor's electrical interconnects. As previously discussed, it would have been obvious to make Shiraiwa's image sensor using industry-standard metal interconnections, thus rendering claims 1 and 3 of the '143 patent obvious.

57. Like Sumi, Shiraiwa discloses an oxide insulting layer, and it would have been obvious to a POSA to implement this layer using TEOS—rendering claim 2 obvious.

**C. Yanagida-1 (Ex. 1006)**

58. Yanagida-1 published as Japanese Publication No. JP 2006-032497 A on February 2, 2006. Yanagida-1, 1. I understand that Yanagida-1 is therefore indisputable prior art under pre-AIA § 102(b). Yanagida-1 was published in Japanese (Ex. 1020) and a certified English translation is provided (Yanagida-1, 1-17).

59. Yanagida-1 discloses all limitations of claims 1 and 3 aside from expressly requiring that the connection via, pad and interconnection layer be made of metal. As with Sumi, it would have been obvious to implement Yanagida-1's

sensor using industry-standard metal connection vias—thereby yielding a sensor falling within the scope of claims 1 and 3. Further, Yanagida-1, like Sumi and Shiraiwa, discloses an oxide insulting layer, and it would have been obvious to a POSA to implement this layer using TEOS—yielding a sensor falling within the scope of claim 2.

**D. Yanagida-2 (Ex. 1007)**

60. Yanagida-2 published as Japanese Publication No. JP 2006-339566 A on December 14, 2006. Yanagida-2, 1. I understand that Yanagida-2 is therefore indisputable prior art under pre-AIA § 102(b). Yanagida-2 was published in Japanese (Ex. 1021) and a certified English translation is provided (Yanagida-2, 2-16).

61. Yanagida-2 discloses all limitations of claims 2 and 4. The additional limitations of claims 2 and 4 were industry standards for CMOS image sensors. Claim 2 requires that the sensor's insulating layer include a TEOS layer, which is disclosed in Yanagida-2.

62. Claim 4 recites a protective layer formed over the insulating layer and a micro-lens formed over the protective layer. Yanagida-2 incorporates a protective layer between the insulating layer and the micro-lens to reduce the reflection of incident light and improve photodiode light collection efficiency.

**X. THE CHALLENGED CLAIMS ARE UNPATENTABLE IN LIGHT OF THE PRIOR ART IDENTIFIED IN THE PETITION**

63. I have been asked to provide my opinion concerning whether claims 1-4 of the '143 patent are anticipated or would have been obvious to a POSA in light of the prior-art references identified in the Petition. For the reasons explained below, it is my opinion that each of claims 1-4 would have been obvious to a POSA.

**A. GROUND 1: CLAIMS 1-3 WOULD HAVE BEEN OBVIOUS OVER SUMI'S RELATED-ART EMBODIMENT**

64. Claims 1-3 would have been obvious in view of Sumi's Related-Art sensor. Sumi describes a solid-state image sensor comprising a semiconductor substrate. Sumi, [0010]-[0019]. In particular, Sumi describes the advantages of BSI CMOS image sensors over the problems associated with front-side-illuminated sensors, such as reduced efficiency and lower sensitivity. *Id.* Specifically, in front-illuminated sensors, "light is illuminated from the front surface side where a wiring layer of a semiconductor substrate is formed and the light is detected by a photodiode formed on the semiconductor substrate is typical." *Id.*, [0004]. For example, "efficiency in using light is reduced and sensitivity is lowered, because multi-layered wirings exist on the route of light illuminated, particularly, on the optical path of oblique light in the vicinity of the effective pixel area and the light is scattered by the multi-layered wirings." *Id.* Given these problems, Sumi

describes “back-illuminated” CMOS image sensors as a “promising” alternative.

*Id.* Sumi describes BSI sensors in which optical components are formed on an opposing side of the semiconductor substrate from the wiring layers to avoid light being blocked by the wiring layers. *Id.*

65. Sumi discloses two BSI sensor manufacturing approaches, which differ by the choice of substrate. First, in the “Description of the Related Art” (“Related-Art Embodiment”), Sumi discloses a BSI image sensor comprising a Silicon-On-Insulator (“SOI”) substrate, multi-layer wiring, an opening, a conductive layer, and a metal pad. *Id.*, [0009]-[0013]. Specifically, the SOI substrate comprises a base silicon substrate (e.g., a silicon wafer) with an insulating layer separating the silicon at the bottom of the substrate with a thin top layer of silicon on which the read-out transistors and wiring layers are formed. *Id.*

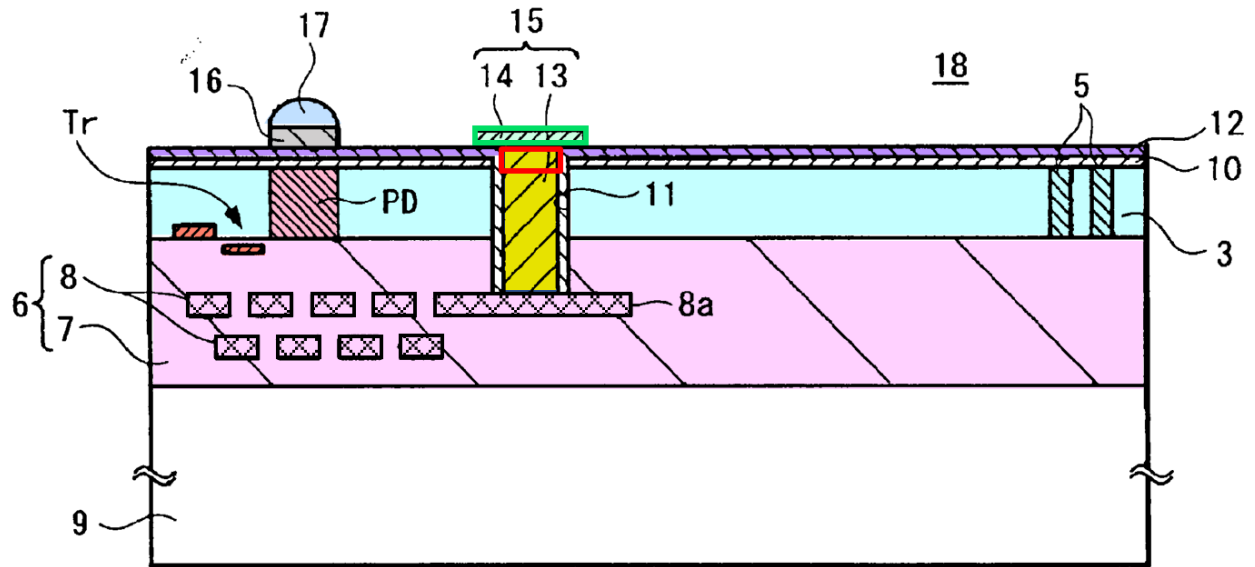
66. Second, in the “Detailed Description” section, Sumi discloses using a silicon wafer as the substrate on which the read-out transistors and corresponding wiring layers are formed. *See id.*, [0063]-[0070].

67. Both known approaches had respective advantages and disadvantages. SOI substrates were advantageous because SOI’s insulating layer provided an etch-stop preventing uneven etch-back of the substrate’s rear surface. *Id.*, [0009], [0015]-[0017]; *see also* Shiraiwa, [0006]-[0008].

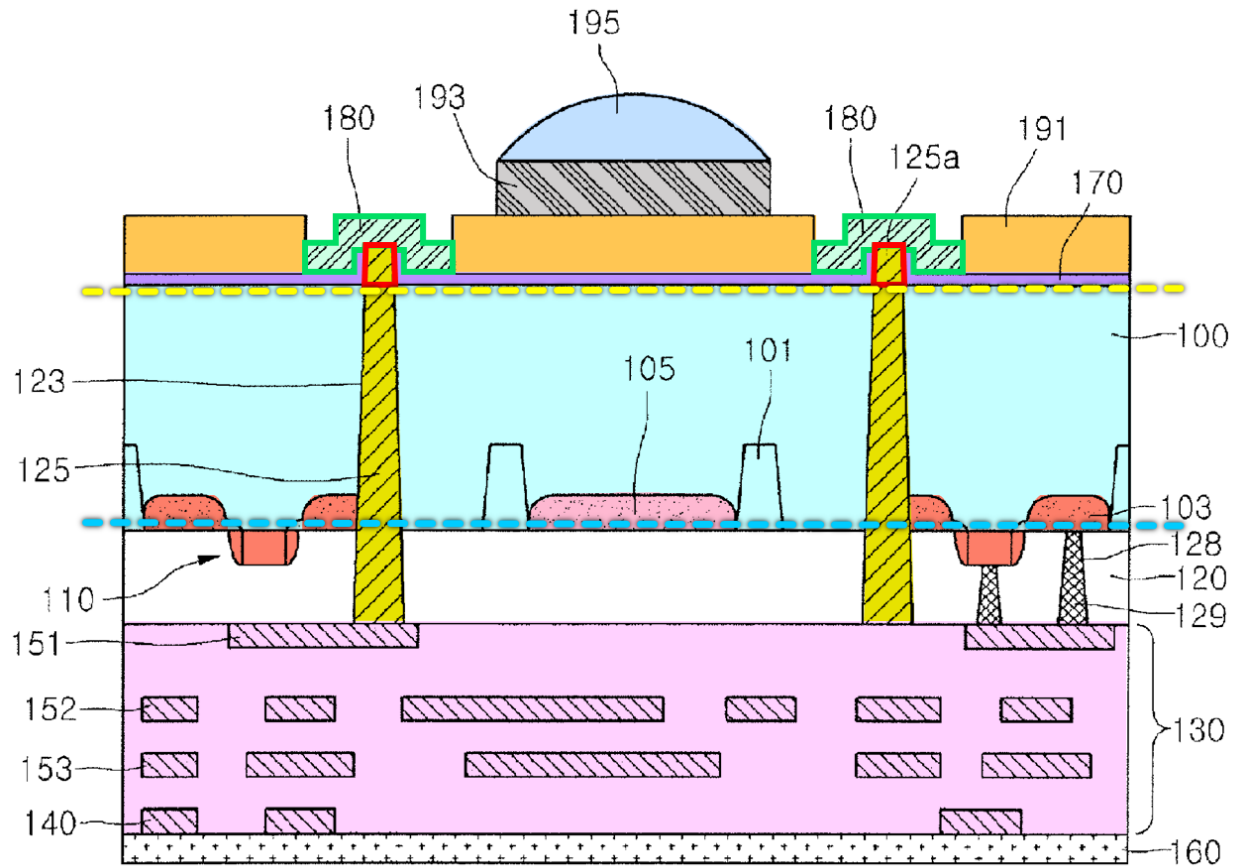
68. However, producing SOI substrates requires processing steps on the silicon wafer (or wafers) to interpose the insulating layer with the substrate, increasing manufacturing costs relative to using a silicon wafer as the substrate as in the second approach. Sumi, [0018], [0064]. Further, because the silicon wafer lacks the SOI substrate's insulating layer, etch stop layer(s) must be formed in the silicon substrate so that rear-side etch-back process thins the silicon substrate to the appropriate (and even) thickness prior to the rear-surface fabrication of the sensor's optical components. *See, e.g.*, Sumi, [0064], [0069].

### **1. The Related-Art Embodiment**

69. The BSI sensor disclosed in Sumi's Related-Art Embodiment comprises a "silicon layer 3" on which "MOS transistors [Tr]", corresponding "photodiodes PD" and "multi-layered wiring layer 6" are formed on a "front surface side" of the silicon layer and "color filter 16" and "on-chip lens 17" are formed on a "rear surface" of silicon layer 3 to produce "back-illuminated type [sensor] 18," as illustrated in Figure 3B of Sumi reproduced below with color annotation for elements recited in claim 1. *Id.*, [0011]-[0017].



70. A “rear surface electrode 15” is provided by depositing “conductive layer 13” inside “opening 11” to connect “wiring layer 8a” on the front surface to forming “electrode pad 14” on the rear surface. *Id.*, [0016]. The region of conductive layer 13 boxed in red shows that a portion of conductive layer 13 projects beyond the rear surface of silicon layer 3 by an amount greater than the thickness of “insulation film 12.” Comparison with Figure 9 of the ’143 patent reproduced below with the same color coding for the elements of claim 1, shows that Sumi’s sensor 18 includes all of the claimed structural elements illustrated in Figure 9.



71. Sumi's Related-Art Embodiment discloses all limitations of claim 1, except that Sumi does not explicitly state that metal was used for sensor 18's electrical interconnects—i.e., “multi-layered wiring layer 6,” “conductive layer 13,” and “electrode pad 14.” However, metal was widely used to implement electrical connections, and metal's benefits were well-known. Quirk (Ex. 1014), 302; Patti (Ex. 1026), 1217. The obvious use of metal in Sumi's Related-Art Embodiment renders claims 1 and 3 obvious. Similarly, the obvious use of TEOS in Sumi's Related-Art Embodiment renders claim 2 obvious.

## **2. Implementing Sumi's Related-Art Embodiment With Metal Components**

72. Claim 1 recites a “*metal* interconnection layer,” a “connection via *metal*,” and a “*metal* pad.” Sumi's Related-Art Embodiment discloses each of these same electrical connections (*i.e.*, “multi-layered wiring layer 6,” “conductive layer 13,” and “electrode pad 14,” respectively), but does not specify any particular material to be used for these conductors. Sumi, [0013]-[0016].

73. However, metal (*e.g.*, copper, aluminum, tungsten, etc.) was the industry-standard choice for fabricating each of these interconnect types. Quirk, 299-308. Indeed, absent explicit disclosure of a non-metal alternative, POSAs would have understood that Sumi's Related-Art Embodiment incorporated metal to provide the disclosed electrical connections. POSAs implementing Sumi's related art embodiment design would have been motivated to use a metal to fabricate the interconnection layer, connection via, and pad using metal.

## **3. The Use of Metal Was Well-Known**

74. To the extent any of Sumi's electrical connections theoretically could have been implemented with non-metal materials, metal would at minimum have been an obvious choice for implementing Sumi's connections. For example, Pain-1 discloses a BSI sensor using metal for each of the interconnection layers, vertical connection vias, and pads connected to the wiring layers through the vias. *See, e.g.*, Pain-1, [0036] (“metal layers 150 for interconnection of circuits and photo-

detectors”), [0048] (“metal pads 525 resid[ing] on the same side of light entrance”), [0077] (“Metal pads 700 [] connected with ILD 610 [metal wiring] by means of interconnect metal 710 [vertical connection via]”), Fig. 10; Hynecek (Ex. 1009), 8:53-57 (“The first to fourth interconnection layers 113, 116, 119 and 122 are formed of a conductive material, for example, a metal, or an alloy containing at least two metals. Preferably, the first to fourth interconnection layers 113, 116, 119 and 122 are formed of aluminum (Al).”).

75. POSAs implementing the Sumi’s related Related-Art Embodiment in Sumi would have had reason to use a metal to fill vias. Quirk, 320-323; Garrou (Ex. 1015), 157-173. A low resistivity conductor within the described connection via in the related art embodiment would electrically and thermally connect the layers. Quirk, 320-323; Garrou, 157-173. Incorporating metal conductors in image sensors was standard practice by 2008; aside from being less expensive than alternatives, metal provided higher conductivity and better durability. Quirk, 320-323; Garrou, 157-173. Further, POSAs would have known that a metal could be easily deposited in BSI sensors using chemical vapor deposition (“CVD”). Quirk, 320-323; Garrou, 157-173. POSAs therefore would have had reason to incorporate metal in the Related -Art Embodiment’s connection via in the ordinary course of implementing the Related-Art Embodiment.

76. Similarly, POSAs would have had reason to fabricate Sumi's Related-Art Embodiment's interconnection and pad using metal. Since the interconnection and pad is electrically connected to the opening, it would have been obvious to a POSA to use a conductive material to electrically couple the two elements. Quirk, 320-323; Garrou, 157-173. As with the connection via, metal would have been an obvious material to use for the pad given its high conductivity and low cost.

77. It would have been obvious for POSAs to use metal for each of Sumi's electrical connections discussed above as it is a known material used for electrical conductors.

#### **4. Reasons For Using Metal**

78. The high conductivity, durability and relatively low cost of using metal to implement electrical connections in semiconductor devices, including image sensors, would have made using metal conductors an obvious and desirable choice for implementing all of the disclosed electrical connections of Sumi's sensor 18 (*i.e.*, wiring layers 8 of multi-layered wiring layer 6, conductive layer 13 and electrode pad 14). Quirk, 300-306, 320-323; Garrou, 157-173.

79. Furthermore, the backside fabrication process for CMOS devices was well-known by at least 2004. This included the need for using a material that could be fabricated at low temperature without requiring doping. Specifically, the processes for metal deposition were well-established and understood, for example,

CVD suitable for low temperature fabrication and for metallizing deep high aspect ratio structures such as vertical vias. Pain-1, [0060]; Quirk, 305-306, 320-323; Garrou, 157-173. POSAs therefore would have had multiple reasons to use metal as the conductive material for multi-layered wiring layer 6, conductive layer 13 and electrode pad 14 of Sumi's Related-Art Embodiment.

## **5. Reasonable Expectation of Success**

80. POSAs would have had a reasonable expectation success in using metal for any of the electrical connections in Sumi's Related-Art Embodiment. As discussed above, providing metal conductors for electrical connections in semiconductor devices, including BSI sensors, was well-established and well-understood; POSAs would have had a reasonable expectation in succeeding in implementing the Sumi's Metal-Related-Art Sensor. Pain-1 disclosed a BSI sensor in which the equivalent structures were all made of metal—including the metal wiring on a first surface of the semiconductor substrate, the pad formed on a second surface of the substrate, and the vertical via electrically connecting the pad and the wiring. Pain-1, [0036], [0048], [0077], Fig. 10.

81. Additionally, POSAs understood that metal was compatible with BSI sensor fabrication processes and thus suitable for use in each of the conductors in Sumi's Related-Art Embodiment given the ability to deposit metal at low temperatures and at high aspect ratios (*e.g.*, within deep holes or trenches). Quirk

271-272. Metal was the commonly and routinely used material for fabricating each of the disclosed interconnect types, and POSAs would have expected success in implementing metal connections in Sumi's sensor 18.

## **6. Resultant Metal-Related-Art Sensor**

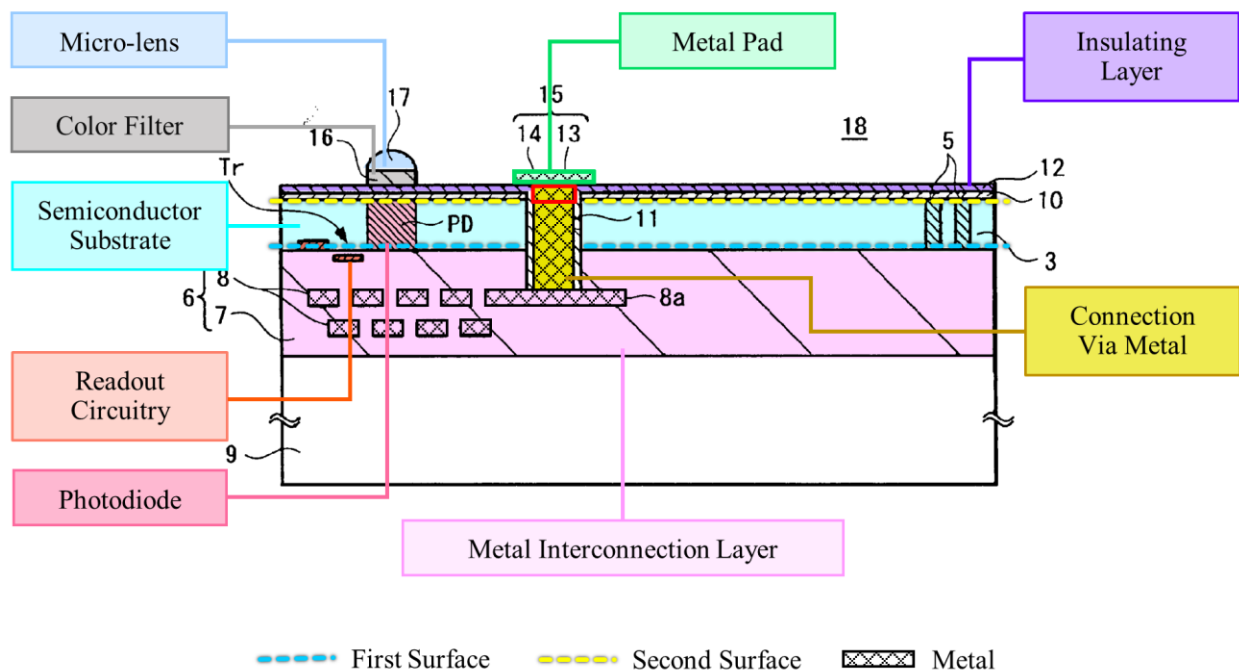
82. The figure below illustrates the image sensor resulting from implementing design of the Sumi's Related-Art Embodiment to using metal to fabricate in the interconnection layer, connection via and pad ("Metal-Related-Art Sensor").

83. The cross-hatching added to Figure 3B of Sumi below ¶86 illustrates Sumi's sensor 18 implemented using metal to fabricate multi-layer wiring 8, conductive layer 13 and electrode pad 14. This Metal-Related-Art Sensor has the same structure as Sumi's sensor 18 and, as shown by annotations and as demonstrated in the limitation-by-limitation analysis below, meets each of the limitations recited in claims 1 and 3.

84. The conductive layer 13 in opening 11, which is the connection via, is etched from the rear side of the sensor. As such, the fabrication of the connection via would occur after all front side layers have been formed and the wafer is complete. Low-temperature CVD would fill the connection via with a conductive material—in this case metal—for the reasons detailed in the preceding section, while leaving the completed front side layers intact.

85. As with the connection via, the multi-layer wiring 8 in multi-layered wiring layer 6 and electrode pad 14 would be fabricated using metal with no changes to the physical structure of the component. Both would be formed using a low-temperature process compatible with rear-side fabrication.

86. Further, the metal pad in the Sumi Related-Art Embodiment may be patterned and routed to other elements to conduct electrical signals in the same manner as the electrode pad disclosed in Sumi's Related-Art Embodiment, which does not expressly disclose the material for the pad in the device design.



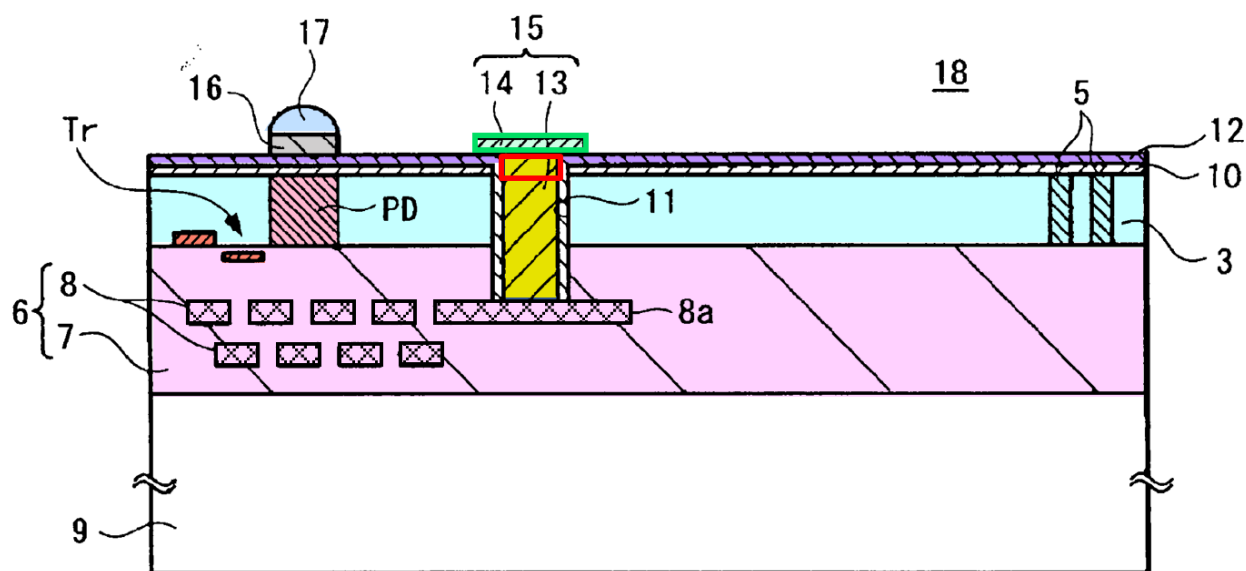
## 7. Claim-by-Claim Analysis

87. The analysis below demonstrates that the Metal-Related-Art Sensor meets each and every element of claims 1 and 3 of the '143 patent.

a. **Claim 1**

i. **Preamble – “An image sensor comprising:”**

88. Sumi’s Related-Art Embodiment discloses “a CMOS solid-state *image sensor* of a back-illuminated type”<sup>2</sup> (Sumi, [0004]-[0005])—satisfying the preamble’s “image sensor” requirement.



ii. **[1A] “a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;”**

89. Sumi’s Related-Art Embodiment describes a semiconductor substrate, and the Metal-Related-Art Sensor would likewise satisfy this requirement. Sumi discloses “an SOI substrate 4 in which a thin-film silicon layer 3 is formed on a silicon substrate 1 with a silicon oxide film (SiO<sub>2</sub> film) 2 in between is prepared.”

<sup>2</sup> Emphasis added unless otherwise noted.

Sumi, [0011]. POSAs would have understood the silicon layer 3 is a semiconductor substrate. See Yanagida-1, [0025]; Ezaki (Ex. 1023), [0047].

90. First, silicon is a well-known semiconductor.

91. Second, it is well known to POSAs to fabricate a semiconductor substrate by starting with an SOI wafer, thinning the back of the SOI wafer to remove the handle layer entirely to stop at the oxide film to form a semiconductor substrate with only the top silicon layer. Sometimes the oxide film is also removed as described in [0015] of Sumi to provide a uniform and flat surface. For example, Pain-1 discloses methods to manufacture a BSI sensor using an upper silicon layer of an SOI substrate as a semiconductor substrate. Pain-1, [0069]-[0071].

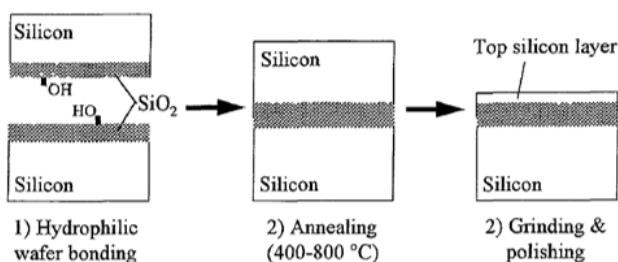
92. As another example, Yanagida-1 discloses a BSI image sensor wherein “MOS type transistors Tr1” and corresponding “photoelectric conversion elements 7” are formed on a first side of the top “silicon layer 4” of a “SOI substrate 30,” and wherein “color filter[s] 11” and “chip lenses 12” are formed on a second side of silicon layer 4 after removing the bottom two layers of SOI substrate 30. Yanagida-1, [0025]-[0026], [0054]-[0057], [0060]-[0061], [0066]. Yanagida-1 describes this silicon layer 4 (*i.e.*, the same top silicon layer of a SOI substrate as Sumi’s silicon layer 3) as a “**semiconductor substrate.**” *Id.*, [0005], [0007], [0013]-[0019], [0025] (“[P]hotoelectric conversion elements 7...[are] formed in the semiconductor substrate (e.g., single crystal silicon layer) 4.”).

93. Ezaki also describes the top “silicon layer 1” of “SOI substrate 23” as a “**semiconductor substrate** 1” on which “readout circuits” and “photoelectric conversion elements are respectively formed on one surface of the single-crystal silicon layer 1” and “on-chip lenses...are formed on the other surface of the silicon layer 1.” Ezaki, [0047], [0085]-[0088], [0098], [0106]; *see also* Yanagida-2, [0029], [0047].

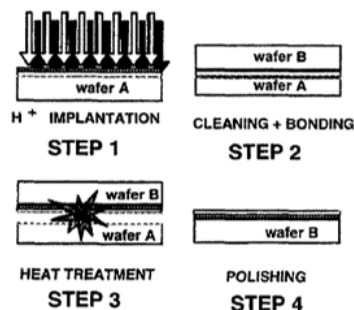
94. This usage in the art (*i.e.*, describing as a “semiconductive substrate” the top layer of a SOI substrate in which the bottom two layers are removed) is consistent with a POSAs understanding. As such, a POSA would have understood silicon layer 3 in Sumi’s Related-Art Embodiment as a “semiconductor substrate” as claimed.

95. Additionally, the ’143 patent states that a “semiconductor substrate may include a wafer having a single crystalline structure, or a silicon substrate in which an epitaxial layer is formed on a wafer.” ’143 patent, 3:13-15. Depending on the technique used to manufacture the SOI substrate, the top silicon layer is either a single-crystalline silicon wafer, or a thin silicon layer deposited on such a wafer. Specifically, SOI substrates were manufactured in one of two ways: 1) a bond and etch-back SOI (“BESOI”) process; and 2) separation by implantation of oxygen (“SIMOX”). Leray (Ex. 1013), 1631-1637.

96. The BESOI process involves bonding together two silicon wafers, one or both of which have an oxide layer formed thereon, and etching-back one of the wafers to a desired thickness for the top silicon layer, as illustrated in Figures 11 (left) and 12 (right) of Leray reproduced below. *Id.*, 1635-1637.

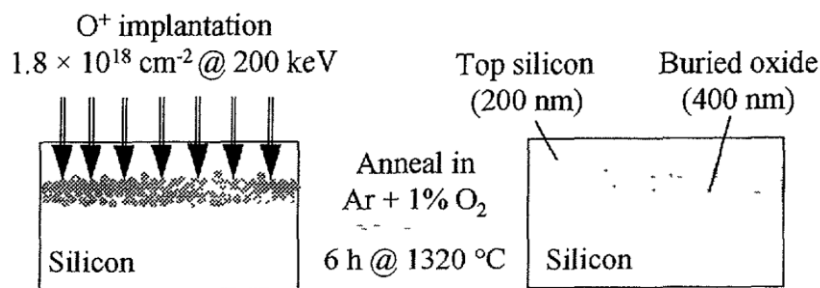


Ex. 1030, Fig. 11



Ex. 1030, Fig. 12

97. SIMOX involves implanting oxygen ions in a silicon wafer at a desired depth, then annealing to form a buried oxide (“BOX”) layer having a thin layer of the silicon wafer above the BOX layer and a thicker base below it. See Figure 6 of Leray reproduced below.



98. In both processes, the top silicon layer of a SOI substrate is formed by a silicon wafer, which the '143 patent describes as a semiconductor substrate. Depending on the desired application for the SOI substrate, a thin silicon film may



providing the substrate on which a “plurality of MOS transistors [Tr]” and “photodiodes PD” are formed on silicon layer 3’s “front surface side.” Sumi, [0012].

100. After multi-layered wiring layer 6 is formed thereon, the bottom two layers of SOI substrate 4 are removed, exposing silicon layer 3’s “rear surface” on which further sensor components (*e.g.*, color filter 16 and lens 17) are formed (*see* Sumi, Figs. 3A, 3B). *Id.*, [0015]-[0017]. POSAs would have understood that silicon layer 3 of the SOI substrate, both surfaces of which provide the substrate on which components of the sensor are fabricated, constitutes the claimed “semiconductor substrate.”

101. Sumi’s Related-Art Embodiment further discloses readout circuitry and a photodiode area. A POSA would have understood that the “**plurality of MOS transistors [Tr]** of a HAD (Hole Accumulation Diode) structure which **constitute a pixel** with the photodiodes PD” meets the claimed “readout circuitry.” Sumi, [0012], Figs. 1-3 (illustrating MOS transistors with label Tr). That is, these transistors “constitute a pixel with the photodiodes” because the transistors read out the charge accumulated in the corresponding photodiode.

102. Sumi’s Related-Art Embodiment does not detail the operation of these MOS transistors Tr, but it was well-known that such transistors provided readout circuitry for the sensor. In a separate embodiment, Sumi itself discloses that the

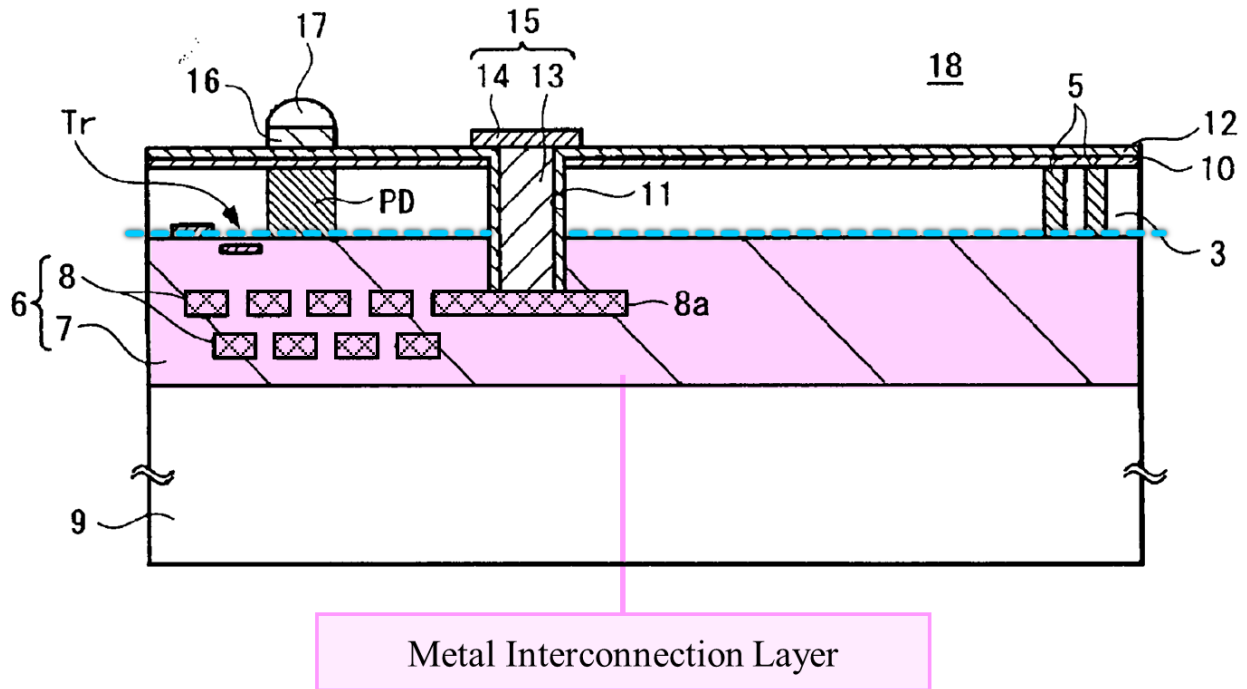
“plurality of MOS transistors Tr that read out signal electric-charge from a photodiode” and comprise “an electric-charge readout transistor, a reset transistor, an amplifier transistor and a vertical selection transistor.” *Id.*, [0065]-[0066].

103. Thus, a POSA would have understood that the plurality of MOS transistors in the Related-Art Embodiment provide “readout circuitry” for the corresponding photodiode (which has a “photodiode area” where the photodiode is formed), which is the very purpose of these transistors in CMOS imaging sensors. *Id.*; Ezaki, [0047]-[0050].

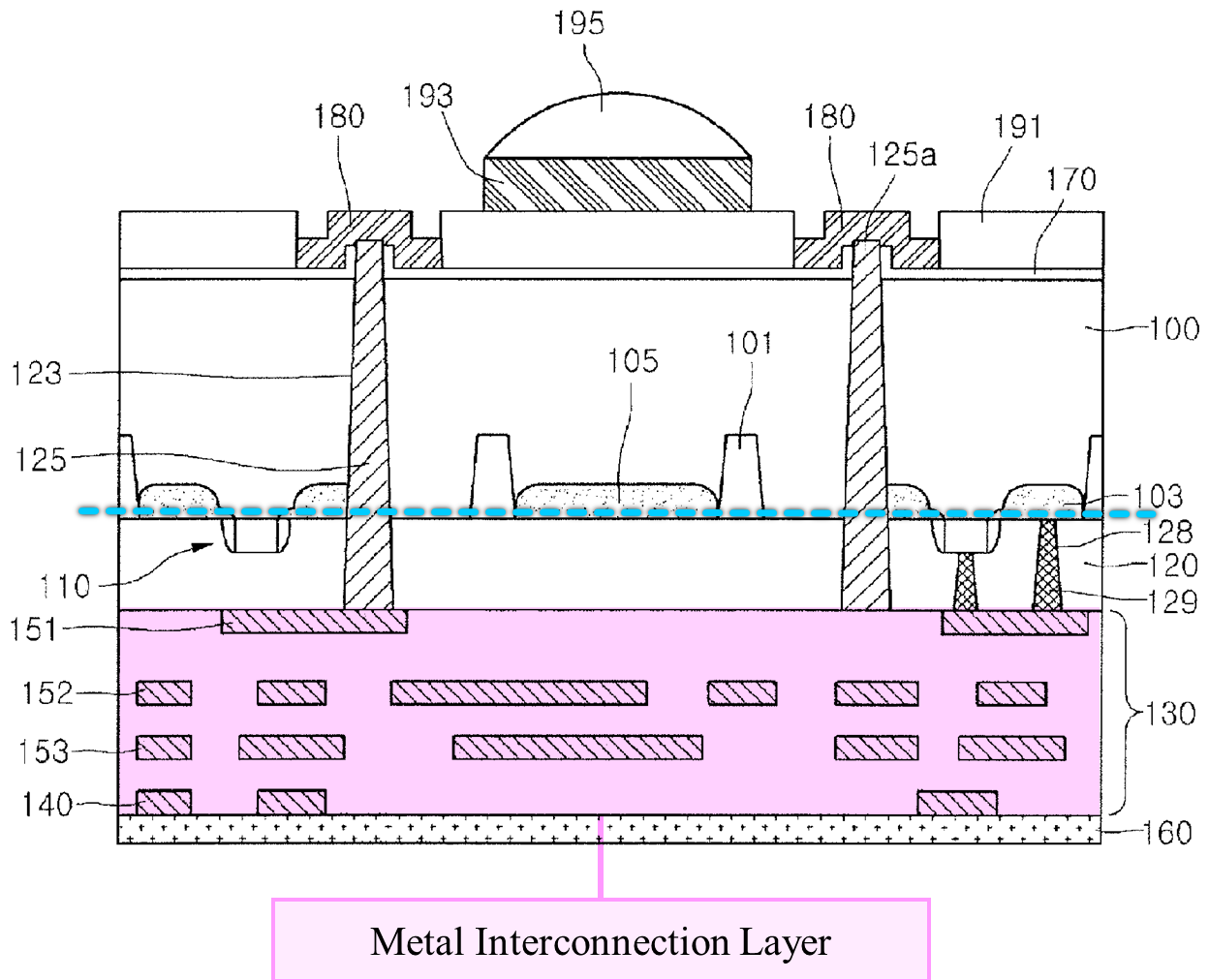
104. As discussed above, the Metal-Related-Art Sensor does not alter the structure of the Related-Art Embodiment and, therefore, Sumi’s silicon layer 3 (“semiconductor substrate”) having a plurality of MOS transistors Tr (“readout circuitry”) and corresponding photodiodes PD (formed in a “photodiode area”) on a front surface side (“first surface”) of silicon layer 3 in the Metal-Related-Art Sensor meets [1A].

**iii. [1B] “a metal interconnection layer formed on the first surface;”**

105. Using metal for “multi-layer wiring 8” of “multi-layered wiring layer 6” in the Metal-Related-Art Sensor meets [1B]. As illustrated in annotated Figure 3B reproduced below, a “multi-layered wiring layer 6” comprising “multi-layer wiring 8” with an “interlayer insulation layer 7” therebetween formed on the front surface side (*i.e.*, the claimed “first surface”) of silicon layer 3. Sumi, [0013].



106. The '143 patent describes and illustrates this same multilayer structure as a “metal interconnection layer,” as illustrated in Figure 9 reproduced below. The '143 patent states that “metal interconnection layer 130 can include a stacked structure of second and third metal interconnections 152 and 153 and a plurality of interlayer dielectric layers.” '143 patent, 4:28-31.



107. Sumi's multi-layered wiring layer 6 comprising multiple stacked wiring layers 8 with insulation layer 7 in between is a "interconnection layer" as recited in [1B] for the same reason. As discussed previously, Sumi does not explicitly state that wiring 8 is made of metal, but implementing multi-layer wiring 8 using metal would have been obvious and desirable given metal's high conductivity, durability, low cost, and ease of deposition. Metal additionally provides good adherence to silicon and silicon dioxide providing additional reason

to implement wiring 8 using metal. Thus, wiring 8 made of metal in the Metal-Related-Art Sensor meets the claimed “metal interconnection layer.”

108. Sumi discloses that the multi-layered wiring layer 6 is “laminated thereon”—*i.e.*, formed on the “front surface side” of silicon layer 3. Sumi, [0012]-[0013]. To the extent there are any intervening layers between multi-layered wiring layer 6 and silicon layer 3, multi-layered wiring layer 6 is still “formed on” the front surface side (*i.e.*, the claimed “first surface”) of silicon layer 3 because the ’143 patent states that when a layer is formed “on” another layer “intervening layers may also be present.” ’143 patent, 3:1-4.

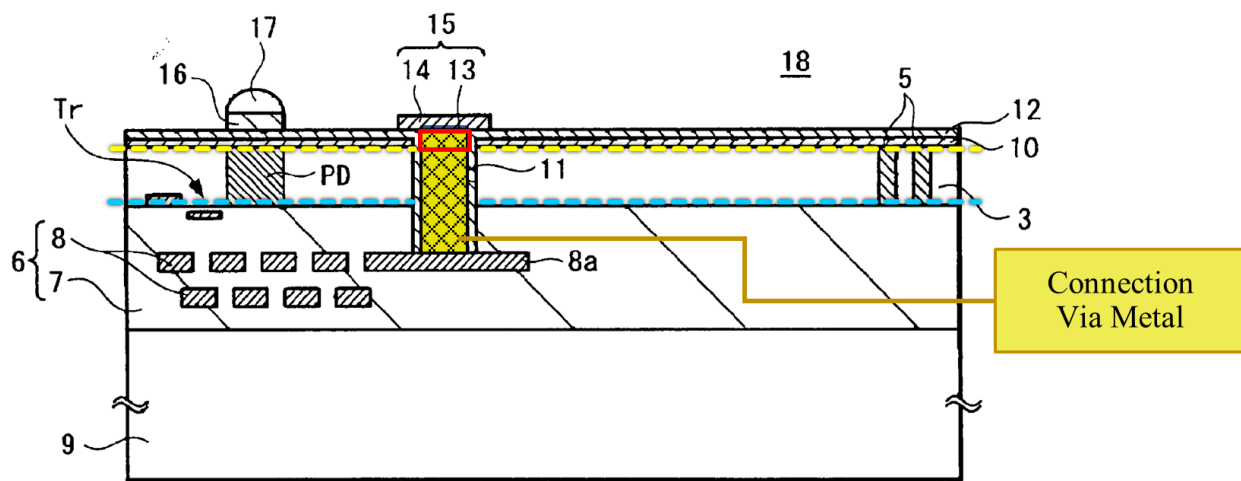
109. Thus, multi-layered wiring layer 6 of the Metal-Related-Art Sensor meets [1B].

**iv. [1C] “a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface;”**

110. Sumi’s Related-Art Embodiment describes Sumi teaches a connection via extending from the first surface to a second surface of the semiconductor substrate. Connection vias are holes filled with a metal plug that form an electrical pathway from one metal layer to another. Quirk, 300. The ’143 patent depicts “connection vias” consistently with this ordinary meaning. For example, claim 1 recites the “connection via metal [extends] from the first surface to a second

surface of the semiconductor substrate.” Figure 9 above shows connection via 123 filled with the connection via metal 125 in the ’143 patent. ’143 patent, 3:41-55.

111. Sumi teaches “[a] **conductive layer 13** that connects to the wiring layer 8a inside the **opening 11** is formed and an electrode pad 14 that connects to the conductive layer 13 and faces to the rear surface is formed, and what is called a rear surface electrode 15 is formed.” Sumi, [0016]. The “conductive layer 13” of the Metal-Related-Art Sensor meets [1C]. Sumi states that “an opening 11 that reaches a wiring layer 8a is formed” and a “conductive layer 13 that connects to the wiring layer 8a inside the opening 11 is formed and an electrode pad 14 that connects to the conductive layer 13 and faces to the rear surface is formed,” as illustrated in Figure 3B of Sumi reproduced below with annotations. Sumi, [0016].



112. Sumi describes the structure comprising electrode pad 14 connected to wiring layer 8a via conductive layer 13 as a “rear surface electrode 15.” *Id.* Conductive layer 13 is a “connection via” because it forms an electrical pathway

from one metal layer to another by way of an opening (“opening 11”) formed through one or more intervening layers, just like connection via metal 125 through connection via 123 of the ’143 patent. *Compare* Sumi, [0016] *with* ’143 patent, 3:41-55; Quirk, 300.

113. Sumi’s “rear surface electrode 15” forms the same structure as pad 180, connection metal via 125 and metal interconnection 151 in the ’143 patent (*see, e.g.*, ’143 patent, Fig. 8) and performs the same function—*i.e.*, connecting the pad on the second surface of the semiconductor substrate with the wiring layers on the first surface. Sumi, [0016]; ’143 patent, 3:41-55, 5:39-42.

114. As discussed above, Sumi’s Metal-Related-Art Sensor uses metal for conductive layer 13 as was commonplace when forming connection vias—including through-silicon vias connecting the front and backside electrical circuitry in imaging sensors. Pain-1, [0077], Fig. 10.

115. Thus, as shown in Figure 3B above, conductive layer 13 provided in opening 11 extends from wiring layer 8a formed on the first surface (*i.e.*, “front surface side” of silicon layer 3) to a second surface (*i.e.*, “rear surface of silicon layer 3”), and therefore metal conductive layer 13 of the Metal-Related-Art Sensor meets “a connection via metal extending from the first surface to a second surface of the semiconductor substrate,” as recited in [1C]. Sumi, [0012]-[0016].

116. As illustrated by annotation in Figure 3B above, conductive layer 13 (yellow) includes a portion (boxed in red) projecting from the second surface. Specifically, silicon nitride film 10 is provided on silicon layer 3's rear surface, and opening 11 is formed through the silicon nitride film 10 and silicon layer 3. Sumi, [0016]. Subsequently, insulation film 12 is formed, covering nitride film 10 and the inside wall of opening 11. *Id.* Thus, when conductive layer 13 is thereafter deposited, the portion of conductive layer 13 boxed in red above extends above silicon layer 3 to form "a projection part projecting from the second surface" as claimed. *Id.*

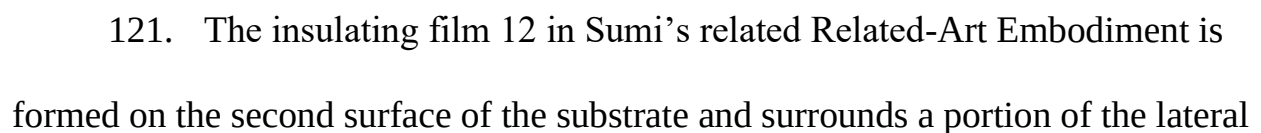
117. Thus, the metal conductive layer 13 of the Metal-Related-Art Sensor meets [1C].

**v. [1D] "an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and"**

118. Sumi's Related-Art Embodiment discloses an insulating layer formed on the second surface of the semiconductor substrate of the related art embodiment to expose the projection part while surrounding a portion of a lateral side of the projection part.

119. "Insulation film 12" in Sumi's Related-Art Embodiment meets [1D]. Sumi discloses that "insulation film 12...is formed from the inside wall of the opening 11 to cover the surface of the silicon nitride film 10," which film 10 is

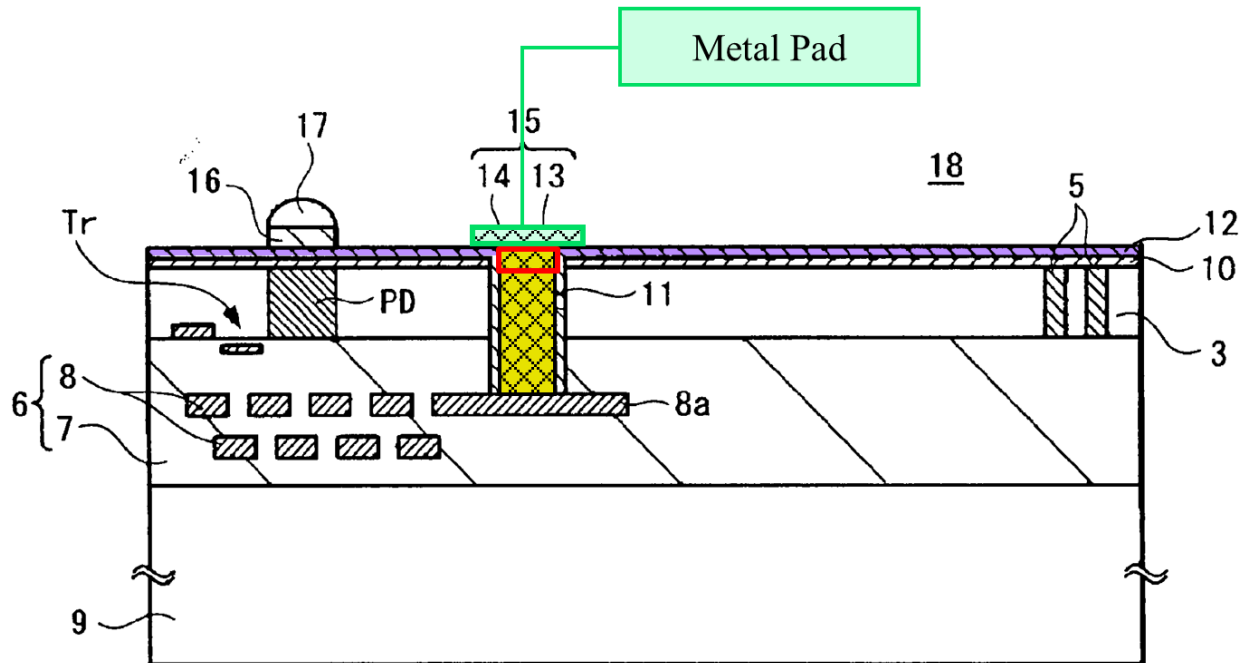
120. Conductive layer 13 is then formed inside opening 11 on insulation film 12 to expose the top surface of conductive layer 13, while the lateral sides of conductive layer 13 extending beyond silicon layer 3—*i.e.*, the “projection part”—are surrounded by insulation film 12, as illustrated in Figure 3B below. Sumi, [0016]. Thus, insulation film 12 (purple) surrounding the lateral sides of the projection part (red) of conductive layer 13 and leaving exposed the top of the portion of the projection part meets [1D].



sides of the projection part (red) of the connection via 13. This structure shown in Figure 3B is the same structure described in the '143 patent in which the top surface of projection part 125a is exposed (and subsequently covered by pad 180) while the lateral sides of the projection part are surrounded by oxide layer 170. '143 patent, 5:30-38 ("liner oxide layer 170 is formed on the entire surface of the backside except for a top of the projection part 125a"). Thus, Sumi's insulation film 12 meets [1D] for the same reasons the '143 patent's oxide layer 170 does. The Metal-Related-Art Sensor does not alter this structure and so also meets [1D].

**vi. [1E] "a metal pad formed on the insulating layer such that the metal pad covers the projection part,"**

122. Sumi's "electrode pad 14" implemented with metal in the Metal-Related-Art Sensor meets [1E]. As discussed above, Sumi discloses forming a "rear surface electrode 15" to electrically connect to the wiring layers on the front surface of silicon layer 3 by forming an electrode pad 14 on insulation film 12 over the exposed portion of conductive layer 13 such that electrode pad 14 "connects to the conductive layer 13" to provide the electrical connection to wiring layer 8a, as illustrated in Figure 3B of Sumi reproduced below with annotation.



123. As discussed above, the Metal-Related-Art Sensor uses metal to form electrode pad 14 as was commonly done to provide a highly conductive, durable pad formed using well-established processes (*e.g.*, CVD) compatible with BSI fabrication. Thus, Metal-Related-Art Sensor's metal electrode pad 14 formed on insulating film 12 and covering the exposed portion of conductive layer 13 extending above silicon layer 3 meets [1E].

**vii. [1F] “wherein the insulating layer has a thickness thinner than a projection height of the projection part.”**

124. Sumi's insulation film 12 meets [1F] because this layer is thinner than the projection part of conductive layer 13, as illustrated in the enlarged portion of Sumi's Figure 3B reproduced below with annotation.



including BSI sensors. Pain-2, [0074]; Quirk, 271-272; Hyneczek, 6:33-46; Yanagida-2, [0037], [0040], [0042]-[0043], [0047], [0054], [0061].

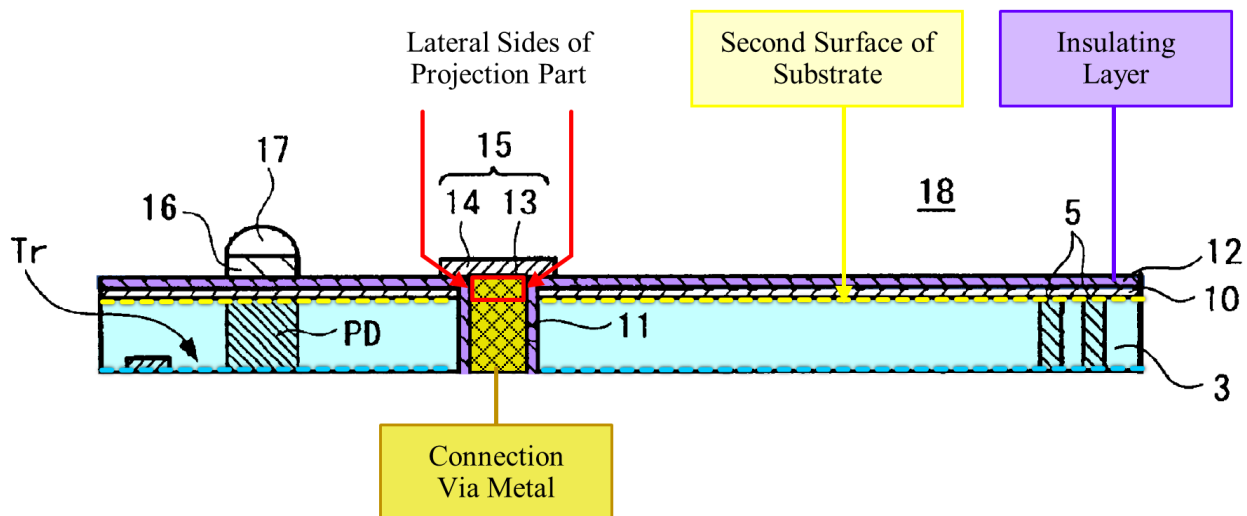
127. POSAs would have known that the primary advantage of using TEOS in a CVD process is “the improved step coverage for high-aspect ratio gaps for applications such as shallow trench isolation.” Quirk, 272. Further, the TEOS deposition process may avoid wafer surface damage and wafer corner damage at steps. *Id.*

128. Accordingly, it would have been obvious to implement insulation film 12 as a TEOS layer at least because doing so is merely the use of a known material (TEOS) for its intended function (insulating) to yield the predictable result of providing the insulation film 12 in Sumi’s sensor 18. Furthermore, TEOS was known to facilitate low-temperature fabrication, and POSAs would have been motivated to use TEOS for insulation film 12 to avoid high temperature deposition that might disrupt previous deposited layers in Sumi’s sensor 18. Quirk 271-272.

129. Pain-2 discloses a BSI sensor incorporating TEOS for a variety of layers, including sidewall insulation films on the inner walls of through-holes. Pain-2, [0074]. Similarly, Yanagida-2 discloses a BSI sensor incorporating TEOS for an insulation (Yanagida-2, [0051]-[0054]) and in conjunction with a nitride film underneath the sensor lenses to provide an anti-reflective layer (*id.*, [0043] (demonstrating the suitability of TEOS for Sumi’s insulation film 12)).

c. **Claim 3 – “The image sensor of claim 1, wherein the insulating layer is formed on a portion of the projection part extending from the second surface.”**

130. Sumi’s Related-Art Embodiment discloses an insulating layer formed on a portion of the projection part extending from the second surface. In particular, annotated figure below shows the insulation film 12 is formed on the lateral sides of the portion of the projection part (red) of opening 11 that extends from the second surface of the silicon layer 3. This arrangement would remain the same in the Metal-Related-Art Sensor.



131. Using a metal to fill opening 11 would not impact the deposition of the insulation film on the projection part. Sumi’s insulating film 12 comprises a silicon oxide film commonly fabricated on metal connection vias. Sumi, [0016]. Accordingly, Sumi’s Related-Art Embodiment renders claim 3 obvious for the same reasons it renders claim 1 obvious.

**B. GROUND 2: CLAIMS 2 AND 4 WOULD HAVE BEEN OBVIOUS OVER SUMI'S RELATED-ART EMBODIMENT IN VIEW OF YANAGIDA-2**

132. The additional limitations of claims 2 and 4 recite well-known BSI CMOS image sensor features expressly disclosed in Yanagida-2. POSAs would have had reason to incorporate these features when implementing Sumi's above-noted Metal-Related-Art Sensor—thereby rendering claims 2 and 4 obvious.

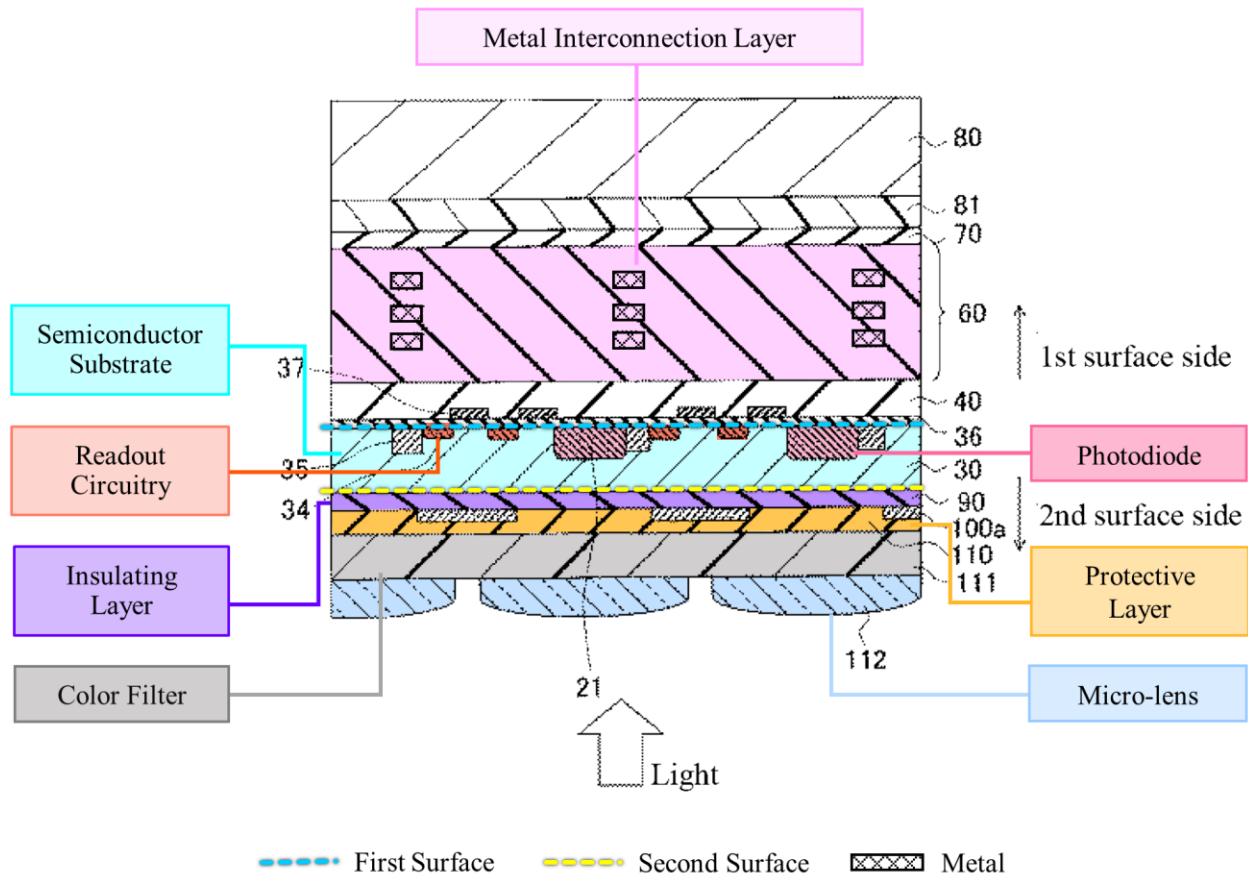
133. Early BSI sensors suffered from image degradation problems because light incident on the active regions of transistors formed in the substrate (read out transistors in particular) could react with the active regions—causing the transistors to produce a read-out signal (*e.g.*, a voltage or current) having a component not corresponding to the charge accumulation measured in the corresponding photodiode. In addition, light that was incident on the border regions of a pixel with a color filter of one color produced charge that could be collected by adjacent pixels having color filters of different colors. This effect caused color mixing and degraded the color accuracy and signal to noise ratio of the captured images.

134. A known solution to this problem was to form and pattern a light-shielding layer to block light from penetrating into the substrate in areas other than the intended photoactive regions.

135. A light-shielding layer also prevented light from adjacent pixel regions from reaching the photodiode and allowed reference transistors to be provided to measure “dark current” in the substrate that could be subtracted from the read-out signals to remove this additional source of noise. Yanagida-1, [0024].

### **1. Overview of Yanagida-2**

136. Like Sumi’s Related-Art Embodiment, Yanagida-2 describes a backside-illuminated solid-state CMOS image sensor. Yanagida-2, Abstract, [0003]-[0004]. Yanagida-2’s sensor includes substrate 30 and a wiring layer 60 formed on a first surface of the substrate. *Id.*, Abstract. As seen in the figure below, Yanagida-2 further comprises an insulating layer formed on the second surface of the substrate. *See id.*, [0034]. The insulating layer comprises an oxide layer “for example, a TEOS film.” *Id.*, [0043]. A protective film 110 is formed on the insulating oxide layer. *Id.*, [0034]



137. “On the protective film 110, a color filter 111 is formed to pass only light in a desired wavelength region. In addition, on the color filter 111, an on-chip lens 112 is formed to focus the incident light onto the photodiode 21.” *Id.*, [0035].

## 2. Combination of Sumi’s Related Art Embodiment and Yanagida-2

138. POSAs would have understood that without light shielding, light would interact with the transistors—thereby corrupting read-out signals (*i.e.*, by introducing components not corresponding to light detected by the photodiode) and produce color mixing, thus degrading color accuracy and signal-to-noise ratios of captured images.

139. It would have been obvious and desirable to include Yanagida-2's light shielding layer and protective covering over the light shielding layer (*i.e.*, "protective film 110 [] formed to cover the light shielding film 100a," Yanagida-2, [0034]) to shield the underlying transistors to prevent signal contribution from sources other than charge accumulation in the photodiode resulting from incident light passing through the corresponding lens.

140. Additionally, Sumi discloses a silicon oxide film 12 that covers a silicon nitride film 10, a dual-film layer known to provide passivation and anti-reflection for the sensor. Sumi, [0016]; *see also* Shiraiwa, [0027] (disclosing "a passivation film (also serving as an anti-reflection film) 38 composed of a silicon nitride film 36 and a silicon oxide film 37"), [0039]; Yanagida-2, [0043].

Yanagida-2 discloses that the silicon oxide film of anti-reflective layer 90 of this same dual-film structure is a TEOS layer, a well-known silicon oxide that Yanagida-2 uses for various insulating layers, including to cover the sidewalls of through-holes. Yanagida-2, [0050]-[0051].

141. Thus, it would have been obvious to use a TEOS layer for Sumi's silicon oxide film 12 at least because, as Yanagida-2 confirms, TEOS was a known silicon oxide material suitable for both ways in which Sumi uses silicon oxide film 12 (*i.e.*, as an insulating film for the sidewalls of through-holes and as part of a dual-film stack with a silicon nitride film). Sumi, [0016]. In addition, POSAs

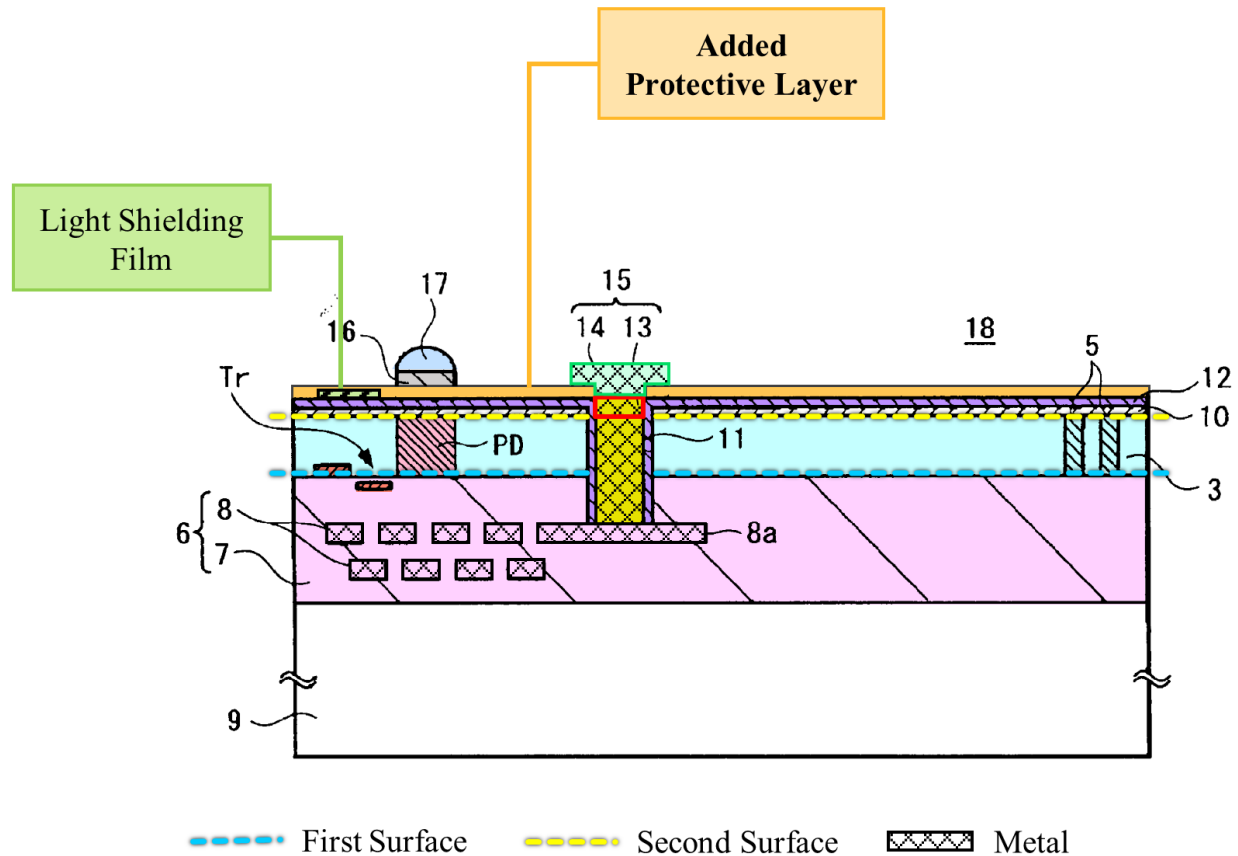
would have recognized the desirability of implementing silicon oxide film 12 as a TEOS layer given that TEOS can be applied at low temperatures, avoiding high-temperature deposition and the associated risks for previously formed BSI structures. Quirk, 271-272.

142. POSAs would have recognized multiple ways to provide Sumi's electrode pad 14 when using Yanagida-2's light shielding layer and corresponding protective layer to cover it. One obvious implementation would have been to form Yanagida-2's light shielding film 100a on Sumi's insulating film 12 (implemented as a TEOS layer on silicon nitride film 10), pattern the light shielding film 100a to provide openings for corresponding diodes, and deposit protective film 110 "to cover the light shielding film 100a"—*i.e.*, the same order disclosed in Yanagida-2 ([0034]).

143. To form electrode pad 14, protective film 110 can be selectively etched over conductive layer 13 and electrode pad 14 formed thereon to connect to conductive layer 13 to form rear surface electrode 15. For example, protective film 110 could be selectively etched using a photoresist layer on top of protective layer that is then removed after electrode pad 14 is formed. Color filter 16 and on-chip lens would then be formed on protective film 110.

144. POSAs would have also understood that there were multiple other ways to implement Yanagida-2's light shielding layer and protective covering in

Sumi's sensor. Regardless of the exact method, the end result would be the sensor ("Metal-Sumi-Yanagida-2 Sensor") illustrated in the figure below.



145. This design blocks light from interacting with Sumi's read out transistors—improving image quality by preventing corruption of the read-out signals measuring the light detected by the photodiodes. In addition, the light shielding layer would allow reference transistors to be formed in the substrate to measure “dark current” in the substrate so that this additional noise can be subtracted from the read-out signals. Yanagida-1, [0024]. POSAs would understand that the Sumi's Metal-Related-Art Sensor provides a small level difference at the backside surface of only the thickness of the pad 14, which

according to Yanagida-2 can prevent uneven application of color filter and lens materials. Yanagida-2, [0067]-[0068].

146. POSAs would have had reasonable expectation of success in fabricating the Metal-Sumi-Yanagida-2 Sensor because the same steps used to form Yanagida-2's light shielding layer and protective film on Yanagida's anti-reflective 90 (*i.e.*, a dual-film nitride-oxide layer) could have been used to form these same layers on Sumi's dual film nitride-oxide layer (*i.e.*, silicon nitride film 10 and silicon oxide film 12). Additionally, forming metal electrode pad 14 (*e.g.*, by selectively etching protective film 110 or otherwise) could be achieved using any number of well-known and well-established semiconductor fabrication techniques.

**a. Reasons for Incorporating Yanagida-2's Teachings**

147. Sumi's Related-Art Embodiment and Yanagida-2 are both directed to backside-illuminated image sensors, and describe the same sensor elements in the same order. Both teach insulation elements formed on the light incident side of the substrate. Sumi, [0016]; Yanagida-2, [0034]. Sumi's Related-Art Embodiment teaches "insulation film 12 such as a silicon oxide film is formed from the inside wall of the opening 11 to cover the surface of the silicon nitride film 10" (Sumi, [0016]) while Yanagida-2 teaches "[t]he anti-reflection film 90 comprises two layers, for example, a TEOS film and a silicon nitride film" Yanagida-2, [0043].

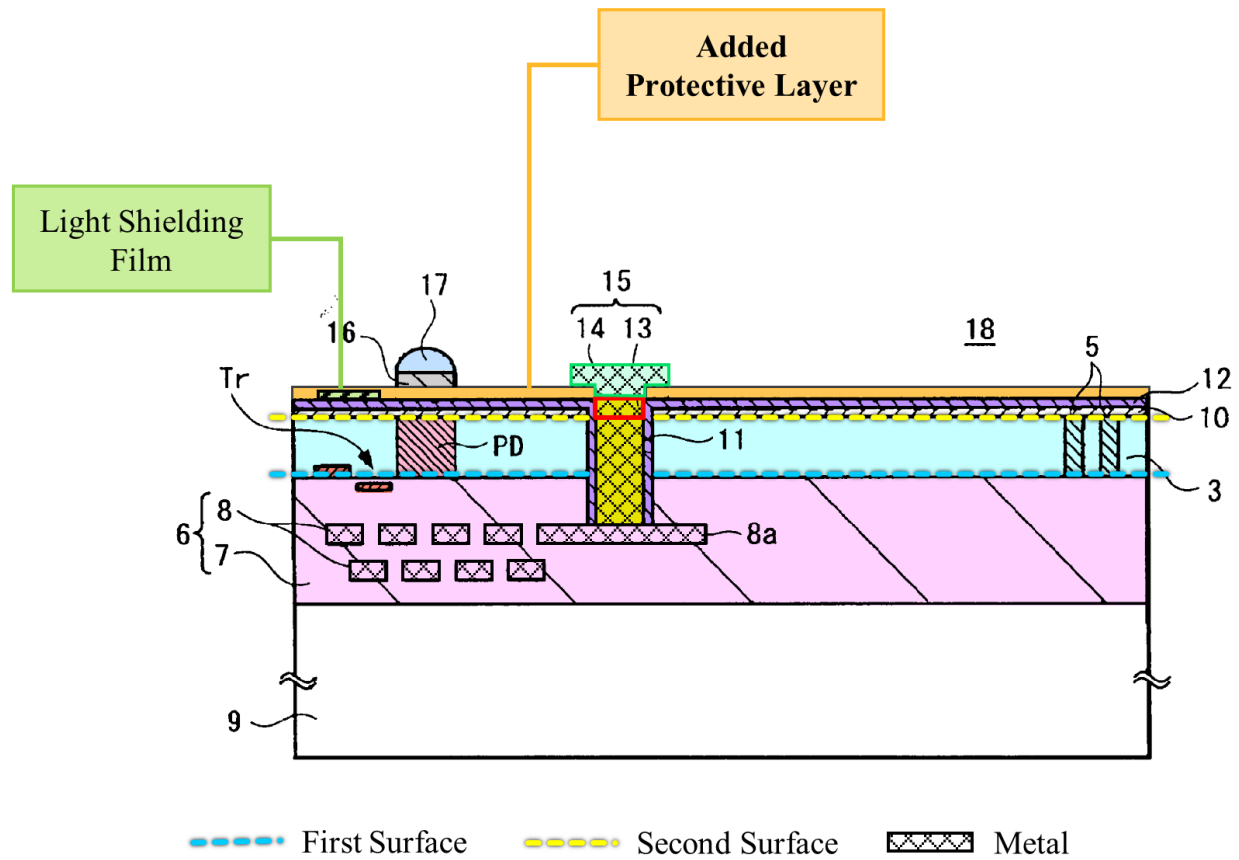
POSAs would have been motivated to improve the insulation film in Sumi's Related-Art Embodiment with a TEOS layer because a low-temperature oxide formed on the backside is highly desirable to prevent the disruption of components already formed on the device and TEOS is common low-temperature oxide, as taught in Yanagida-2. Further, POSAs would know that TEOS is commonly used as an interlayer dielectric, and, as such, could be combined with Sumi's Metal-Related-Art Sensor. Quirk, 271-272.

148. Further, POSAs would have recognized that the Sumi's Metal-Related-Art Sensor could be improved by incorporating a protective layer, sometimes referred to as a passivation layer, to protect the image sensor from corrosion. Passivation enhances the performance of the BSI image sensor by avoiding deterioration caused by moisture or undesirable mobile ions. Passivating the image sensor with a protective layer on the insulating film will better protect the sensor and prevent it from losing sensitivity. Pain-2, [0052]-[0053], Fig. 13. POSAs would understand that Yanagida-2, also directed to a BSI sensor, teaches a protective layer on the insulation layer to passivate the sensor and guard against degradation. POSAs would have applied the protective layer to Sumi's Metal-Related-Art Sensor to achieve the same result of passivating the image sensor. The modification would have been routine, such as by deposition of a TEOS material as taught in Yanagida-2 and would have provided expected results.

**b. Resultant Metal-Sumi-Yanagida-2 Sensor**

149. Incorporating a TEOS layer in Sumi's Metal-Related-Art Sensor design would not impact the physical structure of the device. The TEOS material would simply be used in the insulating film 12. As taught in Sumi's Related-Art Embodiment, the insulating film comprises a silicon oxide. Sumi, [0016]. As discussed above, TEOS is a common oxide material. Pain-2, [0074]. As such, incorporating TEOS in the Metal-Sumi-Yanagida-2 Sensor would not impact the design or fabrication of the image sensor.

150. The sensor resulting from modifying Sumi's Metal-Related-Art Sensor design to include a protective layer formed on the insulating layer (*i.e.*, the Metal-Sumi-Yanagida-2 Sensor) is shown below.



151. As seen above, the protective layer will form a layer above the insulating film in Sumi's Related-Art Embodiment. The protective layer will prevent the adverse effects described above in ¶148. Further, when formed on the insulating film, the protective layer will be patterned and etched to expose the electrode pad in Sumi. As confirmed in Yanagida-2, the color filter and on-chip lens can be formed on the protective layer. Yanagida-2, [0035]. As such, the color filter and on-chip lens in Sumi can be formed on the protective layer with no further changes to the physical design.

**c. Reasonable Expectation of Success**

152. POSAs would have had a reasonable expectation of success in using TEOS as the insulating film in the Sumi's Metal-Related-Art Sensor POSAs would also have had a reasonable expectation of success in modifying the Metal-Related-Art Sensor by forming a protective layer on the insulating film. Both procedures were known in the art and would require no significant modification to the physical design of Sumi's Related-Art Embodiment. Pain-2, [0072]-[0074].

**3. Claim-by-Claim Analysis**

**a. Claims 1 and 3**

153. The combination of Sumi and Yanagida-2 (and in particular the Metal-Sumi-Yanagida-2 Sensor) meets claims 1 and 3 for the same reasons as Sumi's Related-Art Embodiment alone discussed above, which are unchanged in the combination. Nothing about Yanagida-2's teachings is in any way inconsistent with Sumi's Related-Art Embodiment and/or would otherwise detract from the selection of a metal material for the opening 11 or the electrode pad 14. Yanagida-2 already teaches a connection via metal (contact C1), a metal interconnection layer (wiring M), and a metal pad. Yanagida-2, [0038], [0040], [0044], [0055].

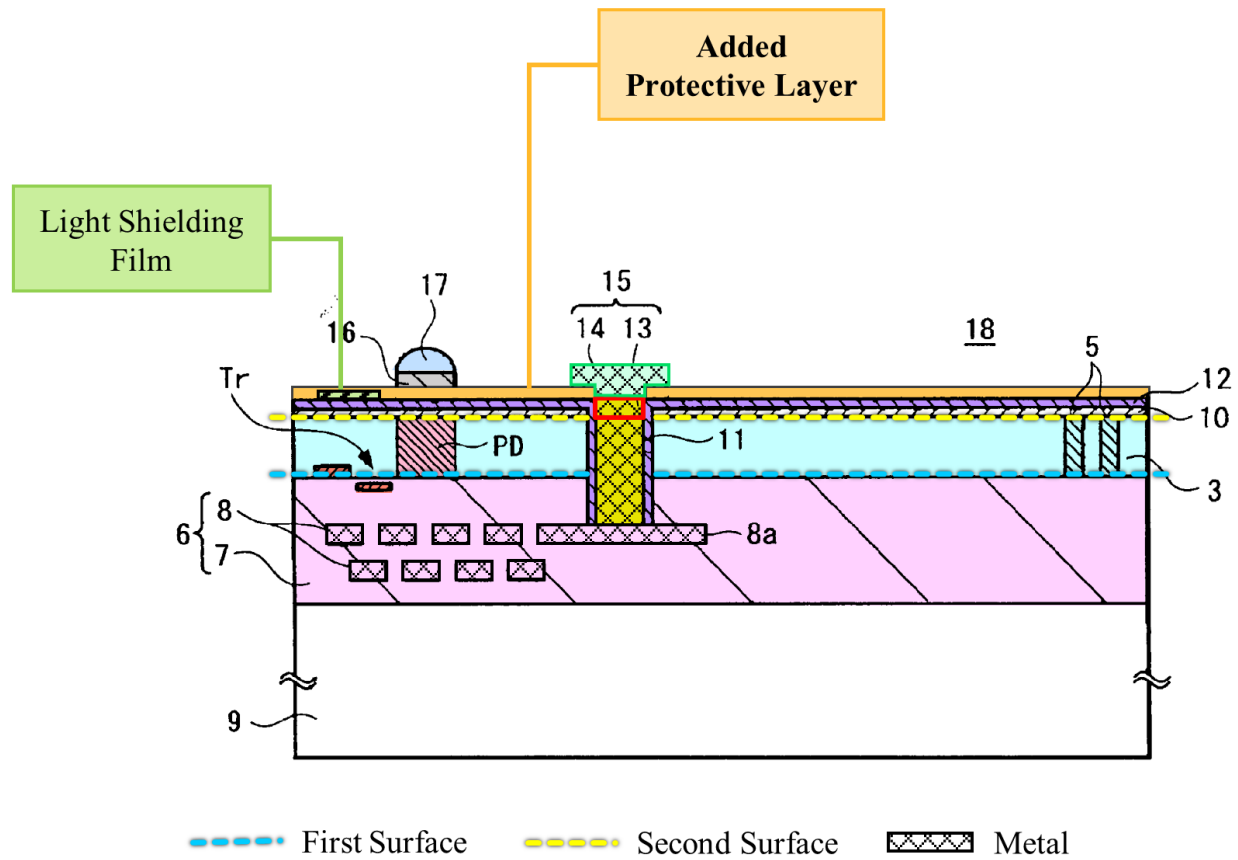
**b. Claim 2 - "The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer."**

154. As discussed above, it would have been obvious to fabricate Sumi's Metal-Related-Art Sensor using TEOS for insulating film 12 as disclosed in

Yanagida-2. In addition to TEOS being a common selection for oxide layers, TEOS would have been particularly desirable given good step coverage for deposition on the sidewalls of opening 11 and low-temperature deposition for rear surface fabrication of a BSI sensor. Quirk, 271-272. Accordingly, insulating film 12 implemented as a TEOS layer in the Metal-Sumi-Yanagida-2 Sensor meets the limitations of claim 2.

**c. Claim [4A] – “The image sensor of claim 1, further comprising: a protective layer formed over the insulating layer; and”**

155. As discussed previously, the Metal-Sumi-Yanagida-2 Sensor implements Yanagida-2’s light shielding film 100a and protective film 110 by forming these layers on Sumi’s insulation film 12 (implemented as a TEOS layer as disclosed in Yanagida-2) and forming Sumi’s color filter 16 and on-chip lens 17 thereon. As illustrated below, the Metal-Sumi-Yanagida-2 Sensor meets each limitation in claim 4.



156. Specifically, Yanagida-2's light shielding film 100a and protective film 110 are formed on Sumi's insulation film 12 in the same manner Yanagida-2 discloses forming these layers "on the anti-reflection film 90" (Yanagida-2, [0034]) composed of a dual nitride-oxide layer similar to Sumi's. As in Yanagida-2 (which discloses the protective layer as being "[o]n the anti-reflection film 90...to cover the light shielding film 100a"), the protective film 110 in the Metal-Sumi-Yanagida-2 sensor is at some locations directly on insulation film 12 and in some locations light shielding film 100a intervenes and is therefore "formed over the insulating layer," as recited in [4A]. '143 patent, 3:1-4 (defining "over" another layer to mean directly over or with intervening layers).

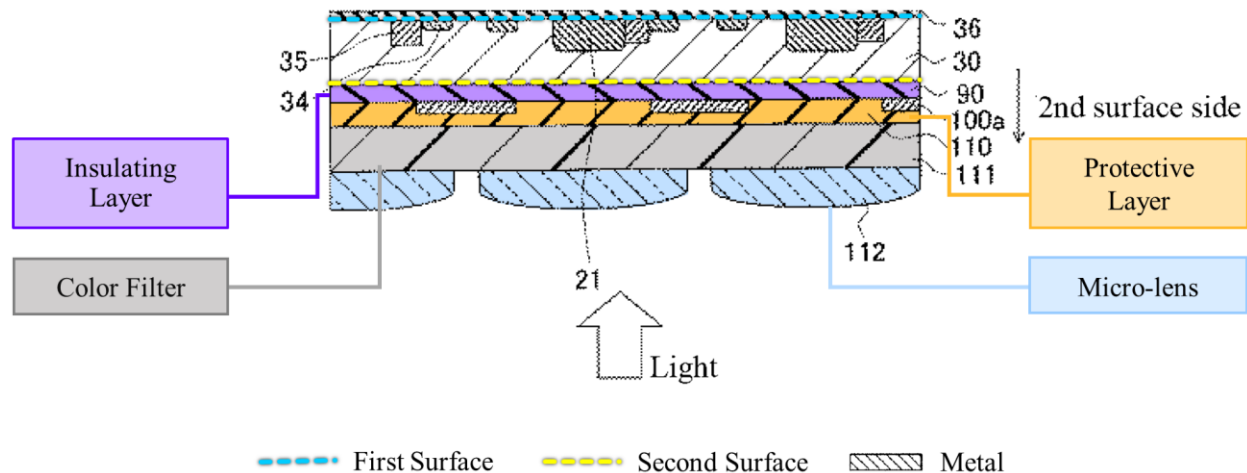
157. Likewise, with the introduction of the light shielding layer and the protective film to cover it, Sumi's on-chip lens 17 is positioned on the protective film 110 with intervening color filter 16 in a region corresponding to the photodiode area—*i.e.*, over the region of the substrate in which photodiode PD is formed—in the Metal-Sumi-Yanagida-2 Sensor, thereby meets [4B].

**d. Claim [4B] – “a micro-lens formed on the protective layer in a region corresponding to the photodiode area.”**

158. Sumi's Related-Art Embodiment teaches “a color filter 16 and an on-chip lens 17 are formed on the rear surface at a position corresponding to the photodiode PD of each pixel, and a CMOS solid-state image sensor of the back-illuminated type 18 is obtained.” Sumi, [0017]. As seen on the figure under ¶155, the color filter 16 and on-chip lens 17 are formed on the insulation film 12 of Sumi's Related-Art Embodiment.

159. As discussed above, Yanagida-2 teaches a protective film 110 formed over the anti-reflection film 90. Yanagida-2 further teaches a micro-lens formed over the protective layer. Specifically, Yanagida-2 states that “[o]n the protective film 110, a color filter 111 is formed to pass only light in a desired wavelength region. In addition, on the color filter 111, an on-chip lens 112 is formed to focus the incident light onto the photodiode 21.” Yanagida-2, [0035].





161. POSAs would understand that increasing the light reaching the photodiode is an important consideration for all image sensors. Forming the micro-lens over a protective layer passivates the second surface of the substrate so that dark current via chemical and field effect passivation may be reduced. In sum, this element is rendered obvious over Sumi's Related-Art Embodiment in view of Yanagida-2.

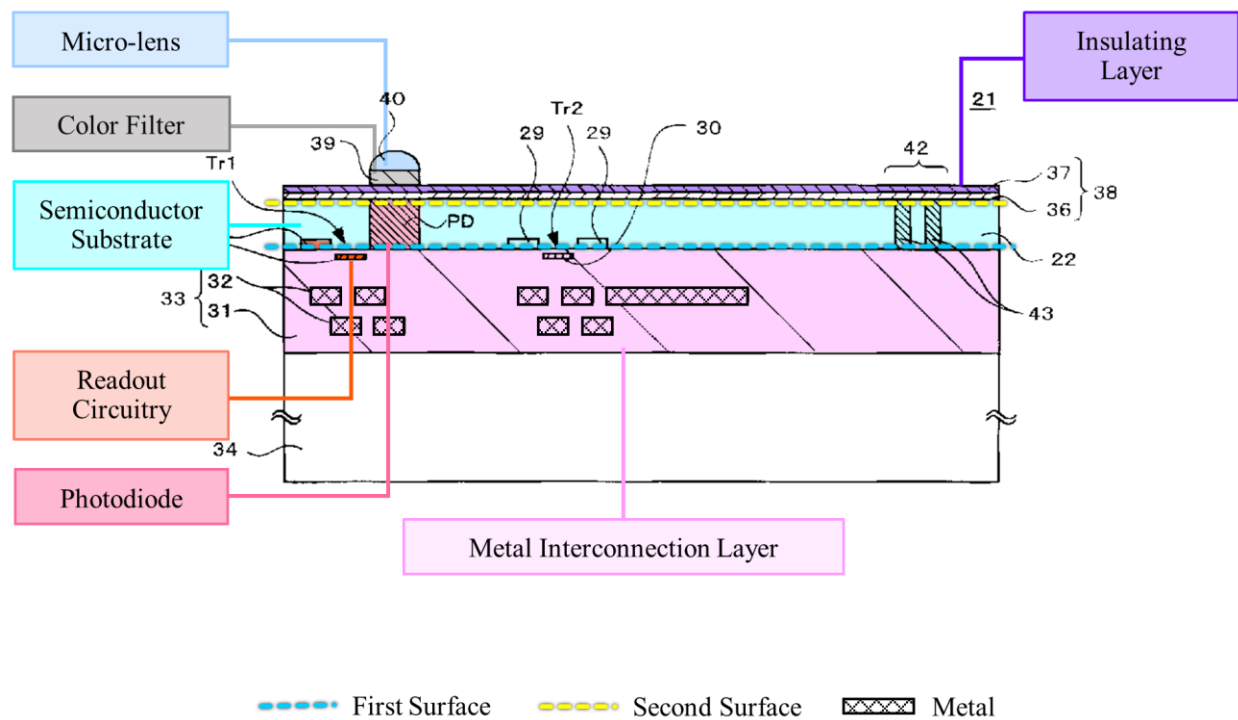
**C. GROUND 3: CLAIMS 1-3 WOULD HAVE BEEN OBVIOUS OVER SHIRAIWA IN VIEW OF SUMI'S RELATED-ART EMBODIMENT**

**1. Shiraiwa**

Shiraiwa published as Japanese Publication No. JP 2005-353996 A on December 22, 2005 and is therefore pre-AIA §102(b) prior art. Shiraiwa, 2. Shiraiwa was published in Japanese (Ex. 1022) and a certified English translation is provided herein (Shiraiwa, 2-13).

## 2. Overview of Shiraiwa

162. Like Sumi, Shiraiwa discloses sensors manufactured from either a SOI substrate (Shiraiwa, [0007]-[0012]) or a silicon wafer (“a normal silicon substrate”) (*id.*, [0012], [0026]-[0044]). Concerning the latter, Shiraiwa discloses a BSI sensor in which read-out transistors Tr1 for “reading signal charges of the photodiode PD” and a multilayer wiring layer 33 are formed on a “front surface side” of a thinned semiconductor substrate 22, as illustrated in Shiraiwa’s Figure 1 reproduced below with annotations. Shiraiwa, [0026]-[0027].



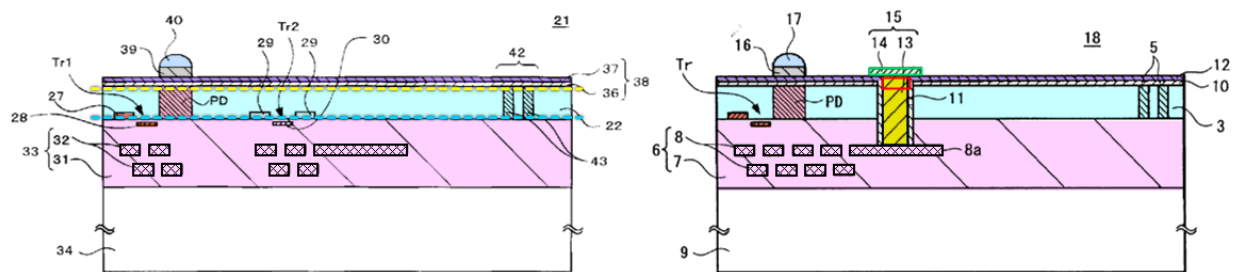
163. On substrate 22’s “back surface side,” a color filter 39 and an on-chip lens 40 corresponding to each pixel 25 is formed on a passivation film 38 composed of a silicon nitride film 36 and a silicon oxide film 37. Shiraiwa, [0026],

[0032], [0039]. Shiraiwa discloses (but does not illustrate) that a pad is formed on the rear surface side to connect to the wiring 32 prior to forming color filter 39 and on-chip lens 40. Shiraiwa, [0040]-[0041]; *see also* Shiraiwa, [0040] (disclosing same pad connecting to wiring on front-surface side of SOI-based sensor).

164. Shiraiwa discloses a rear-surface pad connected to the front-surface wiring layer, but does not describe the details of its manufacture or illustrate this connection component in the drawings.

### 3. Shiraiwa-Sumi Combination

165. As discussed above, Sumi discloses a rear surface electrode 15 providing the vertical connection for accessing the wiring on the substrate's front-side surface. Sumi, [0016]. Sumi's rear surface electrode 15 is implemented in virtually the identical BSI sensor disclosed in Shiraiwa, as illustrated by the side-by-side comparison of Shiraiwa's Figure 1 (left) and Sumi's Figure 3B (right) below.



166. Thus, it would have been obvious to POSAs to use Sumi's rear surface electrode 15 as a known way to implement Shiraiwa's disclosed (but not illustrated) electrical connection between a rear-surface "pad" and "wiring 32" of

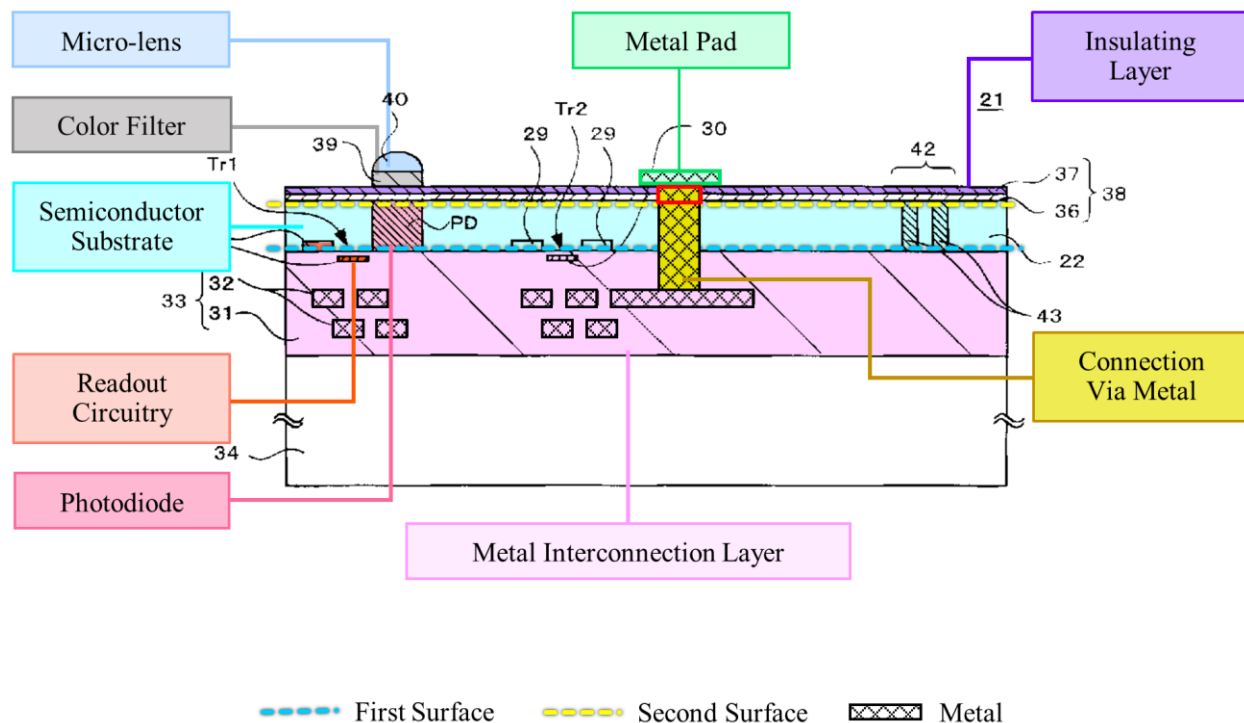
Shiraiwa's sensor 21. Shiraiwa, [0040]. Moreover, POSAs would have been motivated to adopt Sumi's rear surface electrode 15 as doing so would not require changing the structure of Shiraiwa's sensor or significantly altering the fabrication process.

167. In particular, Shiraiwa and Sumi both disclose forming layered silicon nitride and oxide insulating films on the rear-surface side of the semiconductor substrate (Shiraiwa, [0027], [0039]; Sumi, [0016]) and, prior to forming a color filter and on-chip lens on top of the oxide insulating film (Shiraiwa, [0027], [0041]; Sumi, [0016]), providing electrical connection between a pad on the rear surface and the wiring on the front surface (Shiraiwa, [0040]; Sumi, [0016]). Thus, POSAs would have recognized the desirability of implementing Sumi's rear surface electrode 15 in Shiraiwa's sensor given the simplicity of this straightforward implementation.

168. Specifically, implementing Sumi's rear surface electrode 15 in Shiraiwa's sensor could have been integrated into the same rear-surface fabrication steps disclosed in Shiraiwa. After depositing Shiraiwa's silicon nitride film 36 on semiconductor 22's rear surface (Shiraiwa, [0039], Fig. 5F), Sumi's opening 11 would be formed through nitride film 36 and semiconductor substrate 22 to reach wiring 32, as disclosed in Sumi (Sumi, [0016]).

169. Next, Shiraiwa's silicon oxide film 37 would be formed over nitride film 36 (Shiraiwa, [0039]), which would also therefore cover the inside wall of the opening (Sumi, [0016]). Sumi's conductive layer 13 would then be formed inside the opening to electrically connect to Shiraiwa's wiring 32 (*id.*), followed by Sumi's electrode pad 14 that connects to conductive layer 13 to provide rear surface electrode 15 (*id.*). Thereafter, the optical components are formed on silicon oxide film 37 (Shiraiwa, [0041]).

170. Thus, formation of Sumi's rear surface electrode 15 can be integrated in Shiraiwa's disclosed BSI fabrication process. An example of the resulting Shiraiwa-Sumi sensor ("Metal-Shiraiwa-Sumi Sensor") is illustrated below by incorporating Sumi's rear surface electrode 15 into Shiraiwa's sensor 21 illustrated in Figure 1 below.



171. Sumi’s rear surface electrode was positioned as shown above for clarity to illustrate how this structure would have been implemented to connect a rear facing electrode pad to the wiring on the front-side surface of the substrate without obscuring the structure illustrated in Shiraiwa’s Figure 1. However, POSAs understood that Sumi’s rear surface electrode would have been implemented at locations where electrical connections to the wiring were needed—*i.e.*, at a “required position” in the BSI sensor, as disclosed in Shiraiwa (*id.*, [0011], [0040]).

172. POSAs would have had a reasonable expectation of success at least because the same fabrication processes performed on the same material layers used

to provide Sumi's rear surface electrode 15 can be applied to implement this structure in Shiraiwa's sensor.

#### **4. The Metal-Shiraiwa-Sumi Sensor**

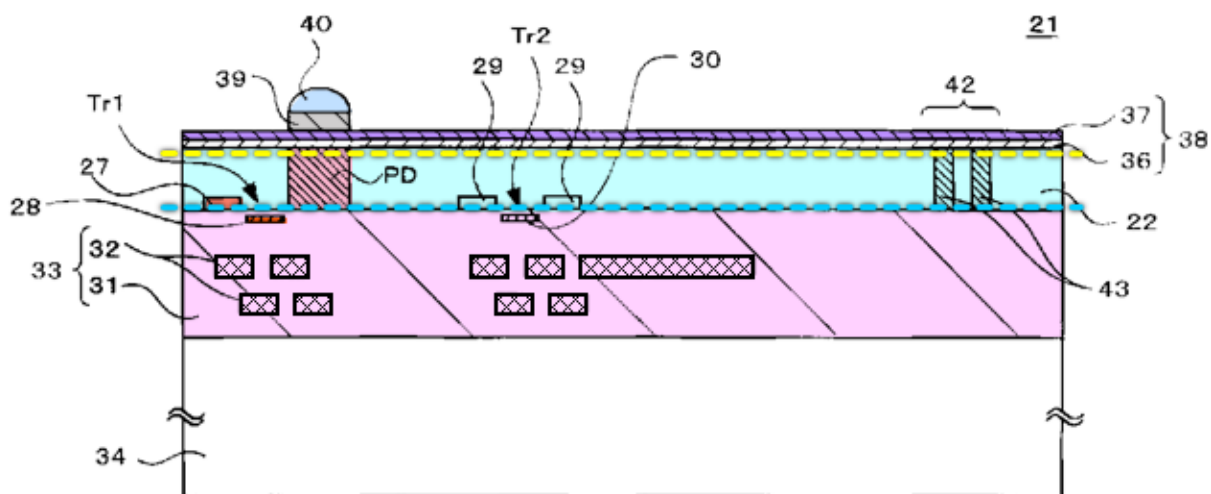
173. Like Sumi, Shiraiwa does not specify the material used for the wiring 32 or the pad (disclosed by not illustrated), but it would have been obvious and desirable to use metal for all electrical connections in the Shiraiwa-Sumi sensor, including "multilayer wiring 32" and Sumi's rear surface electrode 15 (*i.e.*, conductive layer 13 and electrode pad 14). This Metal-Shiraiwa-Sumi Sensor renders obvious claims 1-3.

#### **5. Claim-by-Claim Analysis**

##### **a. Claim 1**

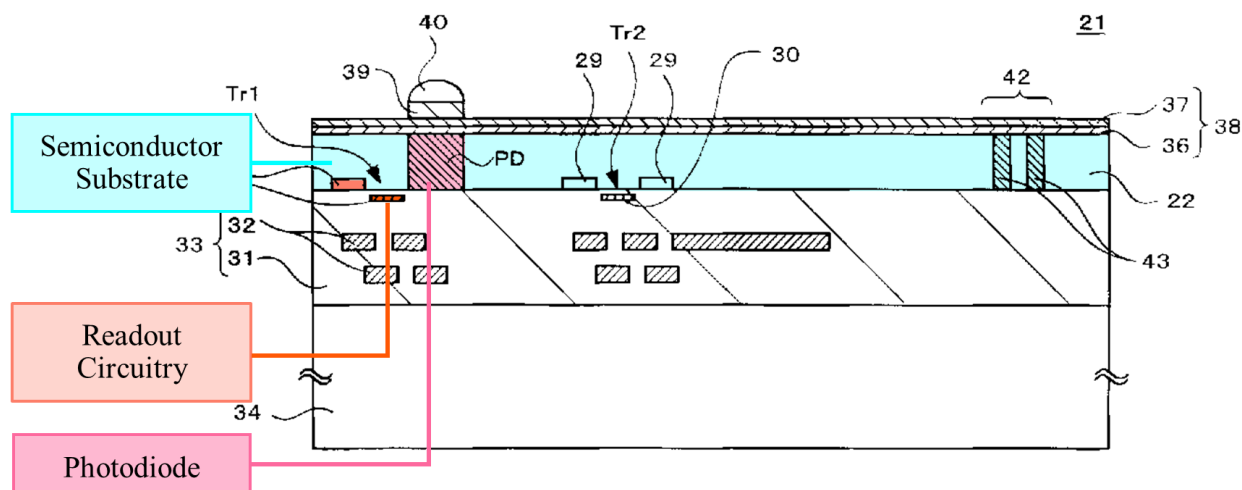
##### **i. Preamble – "An image sensor comprising:"**

174. Shiraiwa discloses "a back-lit CMOS solid-state imaging element" comprising "light-receiving" photodiodes and read-out transistors (Shiraiwa, [0026]), which imaging element POSAs understood is an "image sensor," as recited in the preamble.



ii. [1A] – “a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;”

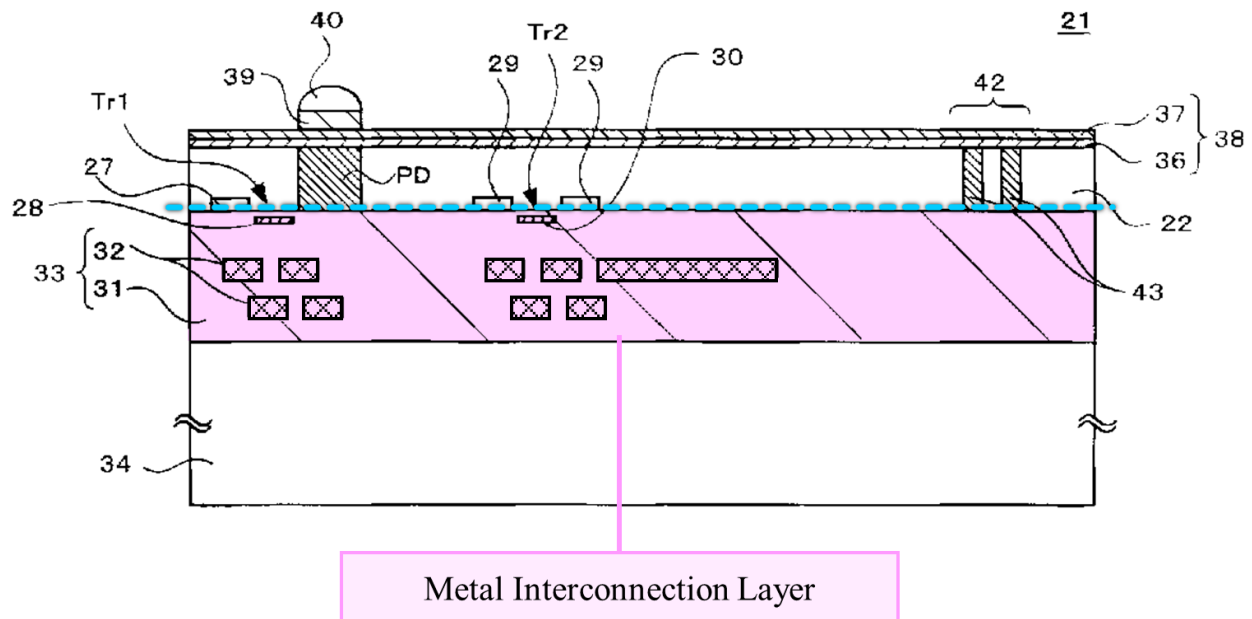
175. Shiraiwa discloses “a plurality of unit pixels 25,” each configured from a “*photodiode* PD” and “a plurality of MOS transistors Tr1 serving as means for *reading signal charges* of the photodiode PD,” formed on the “front surface side” of “silicon *semiconductor substrate* 22,” as illustrated in Shiraiwa’s Figure 1 reproduced below with annotations. Shiraiwa, [0026]-[0027], [0035].



176. The Metal-Shiraiwa-Sumi Sensor implements these same elements. Accordingly, semiconductor substrate 22 of the Metal-Shiraiwa-Sumi Sensor having a photodiode area in which photodiode PD and corresponding readout transistors Tr1 are formed on the front surface side of the semiconductor substrate meets [1A].

**iii. [1B] – “a metal interconnection layer formed on the first surface;”**

177. Using metal for “multilayer wiring 32” in “multilayer wiring layer 33” of the Metal-Shiraiwa-Sumi Sensor meets [1B]. Figure 1 of Shiraiwa reproduced below with annotations illustrates multi-layered wiring layer 33 comprising wiring 32 and interlayer insulating film 31. Shiraiwa, [0027], [0035].



178. The '143 patent discloses this same multi-layer wiring structure, which it describes as a metal interconnection layer. '143 patent, 4:28-31 (“metal

interconnection layer 130 can include a stacked structure of second and third metal interconnections 152 and 153 and a plurality of interlayer dielectric layers”).

Shiraiwa’s multi-layered wiring layer 33 comprising multiple stacked wiring layers 32 with insulation layers 31 in between is an “interconnection layer” as recited in [1B] for the same reason.

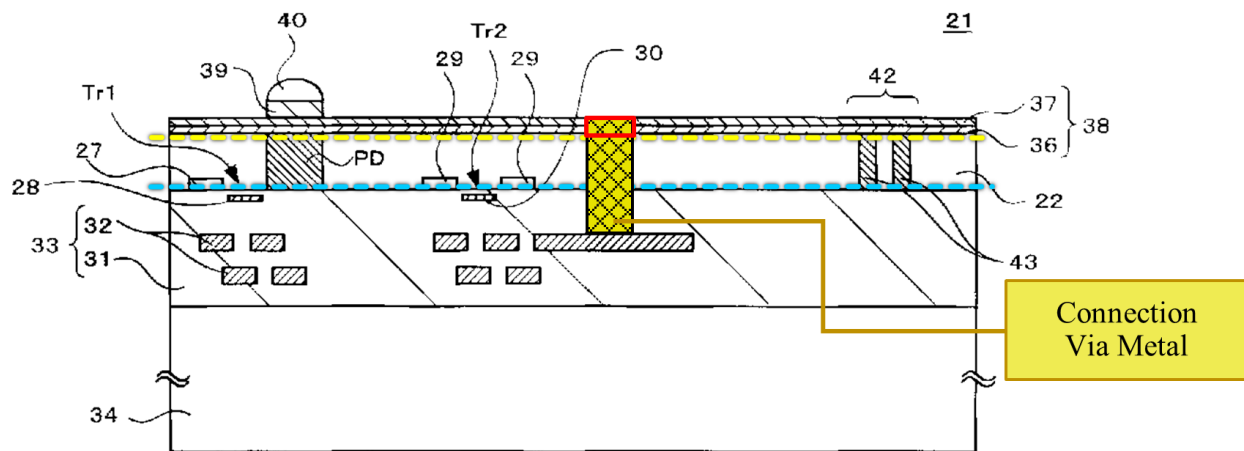
179. The Metal-Shiraiwa-Sumi Sensor uses metal for multi-layer wiring 32, and therefore multi-layered wiring layer 33 of this sensor meets the claimed “metal interconnection layer.” As illustrated in Figure 1 of Shiraiwa above, multi-layered wiring layer 33 is formed on the front side surface—*i.e.*, the claimed “first surface”—of semiconductor substrate 22 even if intervening layers were present. ’143 patent, 3:1-4. When multi-layered wiring layer 33 is formed, the “front surface side” of semiconductor substrate is facing up, as illustrated in Shiraiwa’s Figure 4C. Shiraiwa, [0035].

180. Thus, multi-layered wiring layer 33 of the Metal-Shiraiwa-Sumi Sensor meets [1B].

**iv. [1C] – “a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface;”**

181. As discussed above, the Metal-Shiraiwa-Sumi Sensor uses the rear surface electrode 15 of the Metal-Related-Art Sensor (*i.e.*, by using metal for conductive layer 13 and electrode pad 14 of Sumi’s rear surface electrode 15) to

provide the electrical connection to multi-layered wiring layer 33 on the opposing side (*i.e.*, the claimed “first surface”) of semiconductor substrate 22, as illustrated in Figure 1 modified to include the metal-based conductive layer 13 (the claimed “connection via metal”), which will be connected to metal pad 14 forming a rear surface electrode 15.

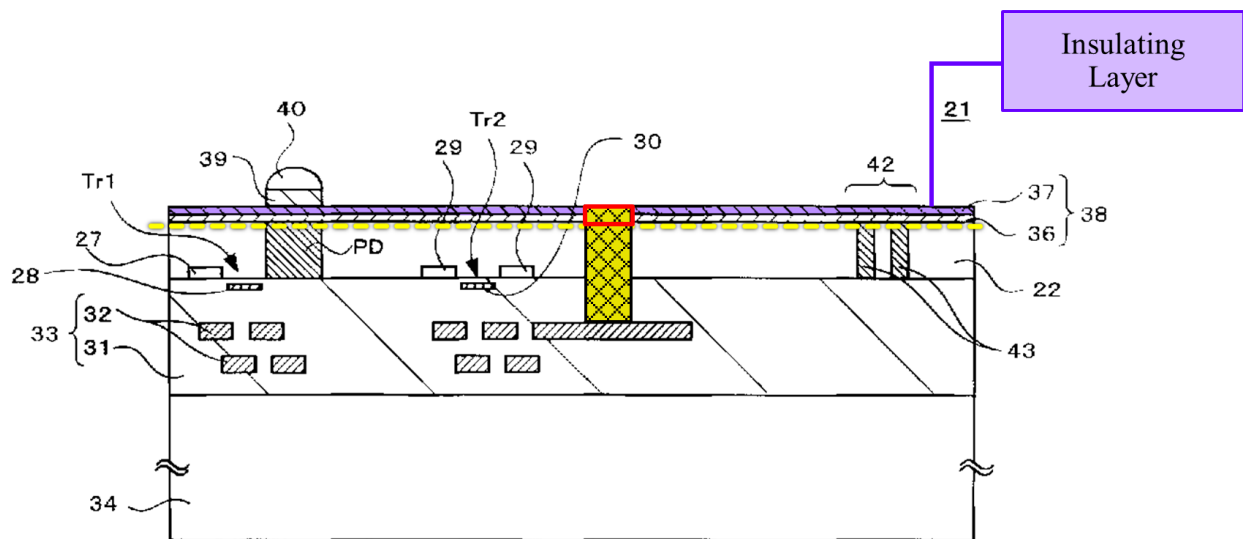


182. Thus, metal conductive layer 13 (highlighted above) formed through semiconductor substrate 22 of the Metal-Shiraiwa-Sumi Sensor meets [1C] for the same reasons discussed previously.

- v. **[1D] – “an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and”**

183. Silicon oxide film 37 of the Metal-Shiraiwa-Sumi Sensor meets [1D] for the same reasons discussed above that Sumi’s insulation film 12 meets [1D] because Sumi’s rear surface electrode 15 is formed in Shiraiwa’s sensor in the

manner described in Sumi, as discussed above and illustrated in the Metal-Shiraiwa-Sumi Sensor below.

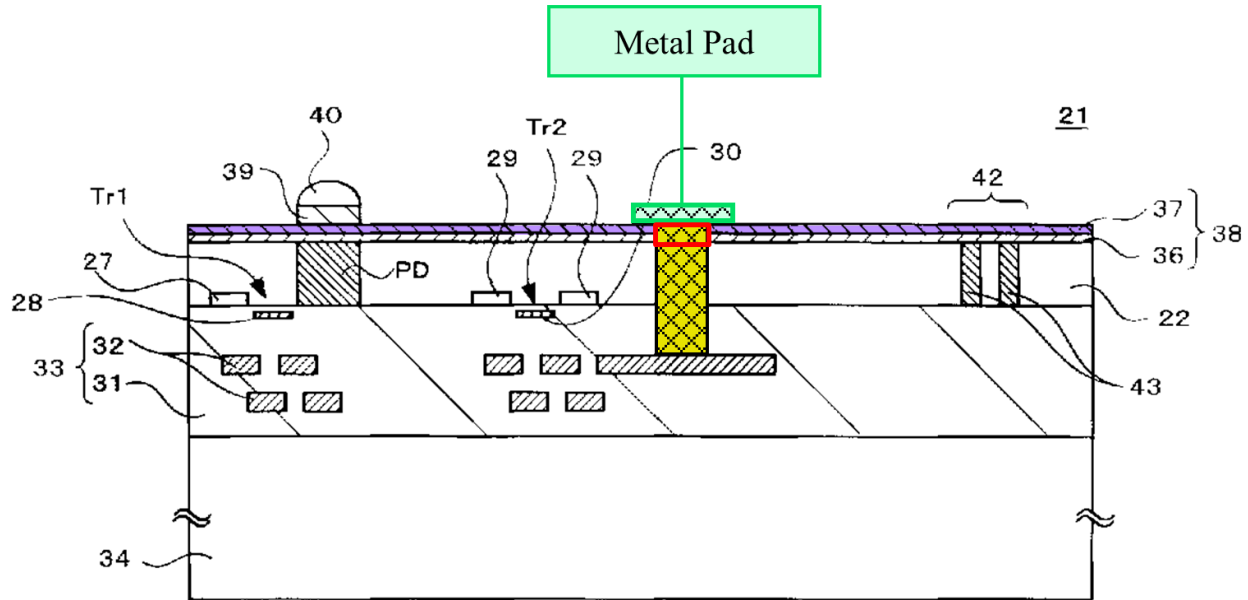


184. That is, after silicon nitride film 36 is formed on semiconductor substrate 22, Sumi's opening 11 is formed to reach wiring 32 and silicon oxide film 37 is formed on the inside wall of opening 11 and covering silicon nitride film 36. Thus, when conductive layer 13 is formed in the opening, the top surface of conductive layer 13 is exposed, while the lateral sides of the projection part (red)—*i.e.*, the portion of conductive layer 13 extending beyond semiconductor substrate 22—are surrounded by silicon oxide film 37 (purple).

**vi. [1E] – “a metal pad formed on the insulating layer such that the metal pad covers the projection part,”**

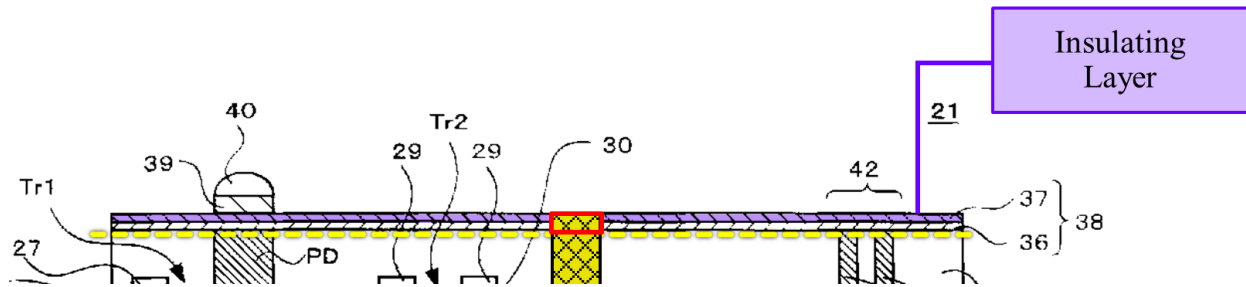
185. As discussed previously, the Metal-Shiraiwa-Sumi Sensor uses the Sumi's Metal-Related-Art Sensor's rear surface electrode 15 and, therefore, the metal electrode pad 14 highlighted in the Metal-Shiraiwa-Sumi Sensor illustrated

below meets [1E] for the same reasons discussed that Sumi's metal pad meets claim [1E].



**vii. [1F] “wherein the insulating layer has a thickness thinner than a projection height of the projection part.”**

186. As discussed above, because Sumi's rear surface electrode 15 is formed in Shiraiwa's sensor in the same manner disclosed in Sumi, the height of the portion of the conductive layer 13 extending beyond semiconductor substrate 22 in the Metal-Shiraiwa-Sumi Sensor (illustrated below) is at least equal to the sum of the thicknesses of nitride film 36 and oxide film 37. Thus, oxide film 37 (*i.e.*, the insulating layer) is “thinner than a projection height of the projection part,” as recited in [1F] by at least the thickness of film 36.

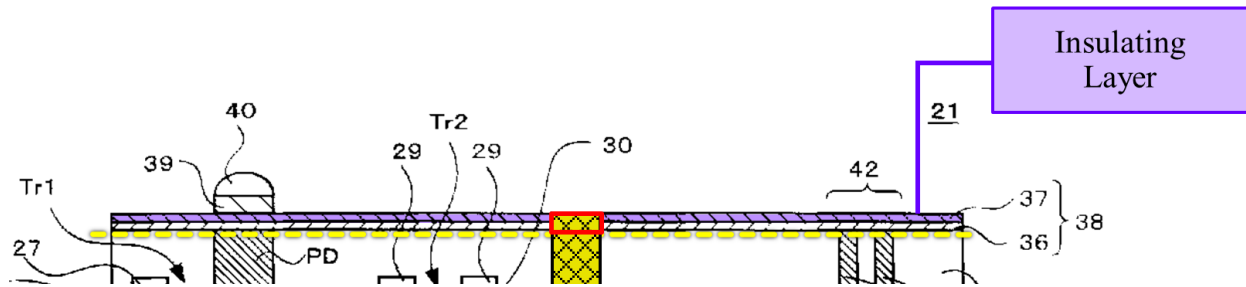


**b. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”**

187. Like Sumi’s description of “insulation film 12,” Shiraiwa describes the insulating film 37 as “silicon oxide,” but does not expressly describe it as a TEOS layer. Shiraiwa, [0008]. However, it would have been obvious to implement film 37 as a TEOS layer for the same reasons described above concerning Sumi’s film 12.

**c. Claim 3 – “The image sensor of claim 1, wherein the insulating layer is formed on a portion of the projection part extending from the second surface.”**

188. The Metal-Shiraiwa-Sumi Sensor discloses a stacked dual-layer insulating layer formed on the substrate’s second surface. The figure below shows the insulating layer in the stacked dual-layer insulation film formed on the lateral sides of the portion of the projection part of the connection via extending from the second surface of semiconductor substrate 22.

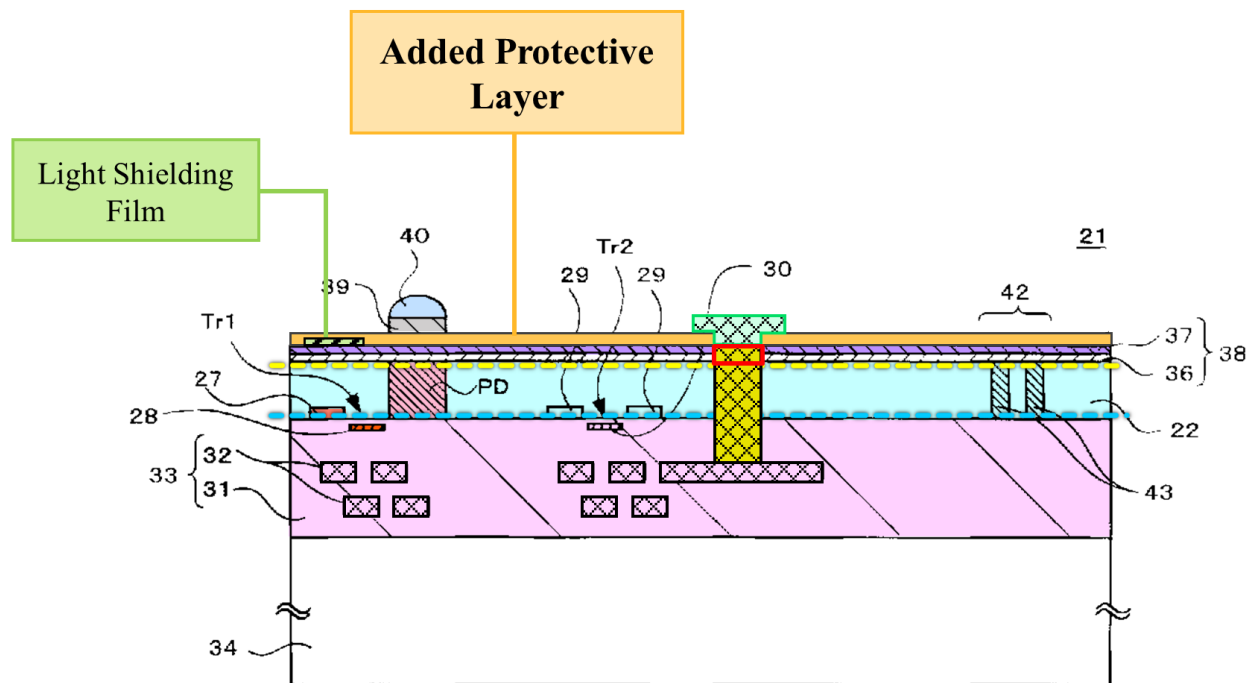


189. Using a metal to form the connection via would not impact the deposition of the insulating layer on the projection part. The insulating layer in the stacked dual-layer insulation in Metal-Shiraiwa-Sumi Sensor comprises a silicon oxide film commonly fabricated on metal connection vias. Sumi, [0064]; *see also* Pain-1, [0077]. Accordingly, the Metal-Shiraiwa-Sumi Sensor renders claim 3 obvious.

**D. GROUND 4: CLAIMS 2 AND 4 WOULD HAVE BEEN OBVIOUS OVER SHIRAIWA IN VIEW OF SUMI'S RELATED-ART EMBODIMENT AND YANAGIDA-2**

190. Yanagida-2 discloses a light-shielding layer that POSAs would have recognized as desirable to incorporate into the Metal-Shiraiwa-Sumi Sensor. The light-shielding layer (as disclosed in Yanagida-2) blocks light from penetrating into the substrate in areas other than the photoactive regions, and prevents light from adjacent pixel regions from reaching the photodiode. It would have been obvious to a POSA to incorporate Yanagida-2's protective layer and light shielding film into the Metal-Shiraiwa-Sumi Sensor. As with Sumi's Metal-Related-Art Sensor, POSAs would understand that the Metal-Shiraiwa-Sumi Sensor provides a

small level difference at the backside surface of only the thickness of the pad 14, preventing the uneven application of color filter and lens materials. Yanagida-2, [0067]-[0068].



191. Further, Shiraiwa, like Sumi, discloses forming layers of silicon nitride and silicon oxide films on the rear-surface side of the semiconductor substrate and then forming a color filter and on-chip lens on top of the insulating film. It would have been obvious when implementing the Metal-Shiraiwa-Sumi Sensor to incorporate TEOS as the silicon oxide (as taught in Yanagida-2).

192. The resulting combination would render claims 2 and 4 obvious over Shiraiwa in view of Sumi and Yanagida-2 for the same reasons detailed previously concerning why claims 2 and 4 are unpatentable as obvious over Sumi in view of Yanagida-2.

**E. GROUND 5: CLAIMS 1-3 WOULD HAVE BEEN OBVIOUS OVER YANAGIDA-1**

193. Yanagida-1 published as Japanese Publication No. JP 2006-032497A on February 2, 2006. Yanagida-1, 1. Yanagida-1 is therefore indisputable prior art under pre-AIA § 102(b). Yanagida-1 was published in Japanese (Ex. 1020) and a certified English translation is provided herein (Yanagida-1, 1-17).

194. Yanagida-1 describes BSI CMOS image sensors and notes the advantages of such sensors over front-side-illuminated sensors. “Conventional solid-state image sensors are constructed with photoelectric conversion elements, an electrode layer, such as a readout electrode, and a color filter or on-chip lens which are formed on the front face side of the semiconductor substrate to capture images by allowing light to enter from the front face side.” *Id.*, [0002]. However, as previously stated, frontside-side-illuminated sensors have “reduced photoelectric conversion efficiency and reduced sensitivity with respect to incident light.” *Id.*, [0004]. As such, Yanagida-1, like Sumi, describes a BSI solid-state image sensor. *Id.*, [0005]. Yanagida-1 in turn explains that problems may arise with BSI image sensors if the “semiconductor well region formed at the periphery of the photoelectric conversion elements were grounded via the wiring disposed from the front face side of the single crystal silicon layer.” *Id.*, [0008]. Such a configuration may cause a high resistance in the semiconductor well region and inhibit extraction of minority carrier (holes) from the photoelectric elements. *Id.*,

[0008]-[0010]. Yanagida-1 addresses these issues by providing a “solid-state image sensor, a solid-state image pickup device, and a process for producing the solid-state image sensor capable of allowing the minority carriers generated in the photoelectric conversion elements to be easily extracted.” *Id.*, [0011].

195. Yanagida-1’s image sensor comprises a solid-state substrate, interconnection layers, a through silicon via, a passivation layer, a bonding pad, and a microlens. *See id.*, [0012].

**1. Obviousness of Implementing Yanagida-1 Using Metal-Based Film**

196. Yanagida-1 does not disclose particular materials for the interconnection layer (wiring 26) and pad (light shielding film). POSAs would have been motivated to use metal for these structures.

**a. Reasons for Using Metal**

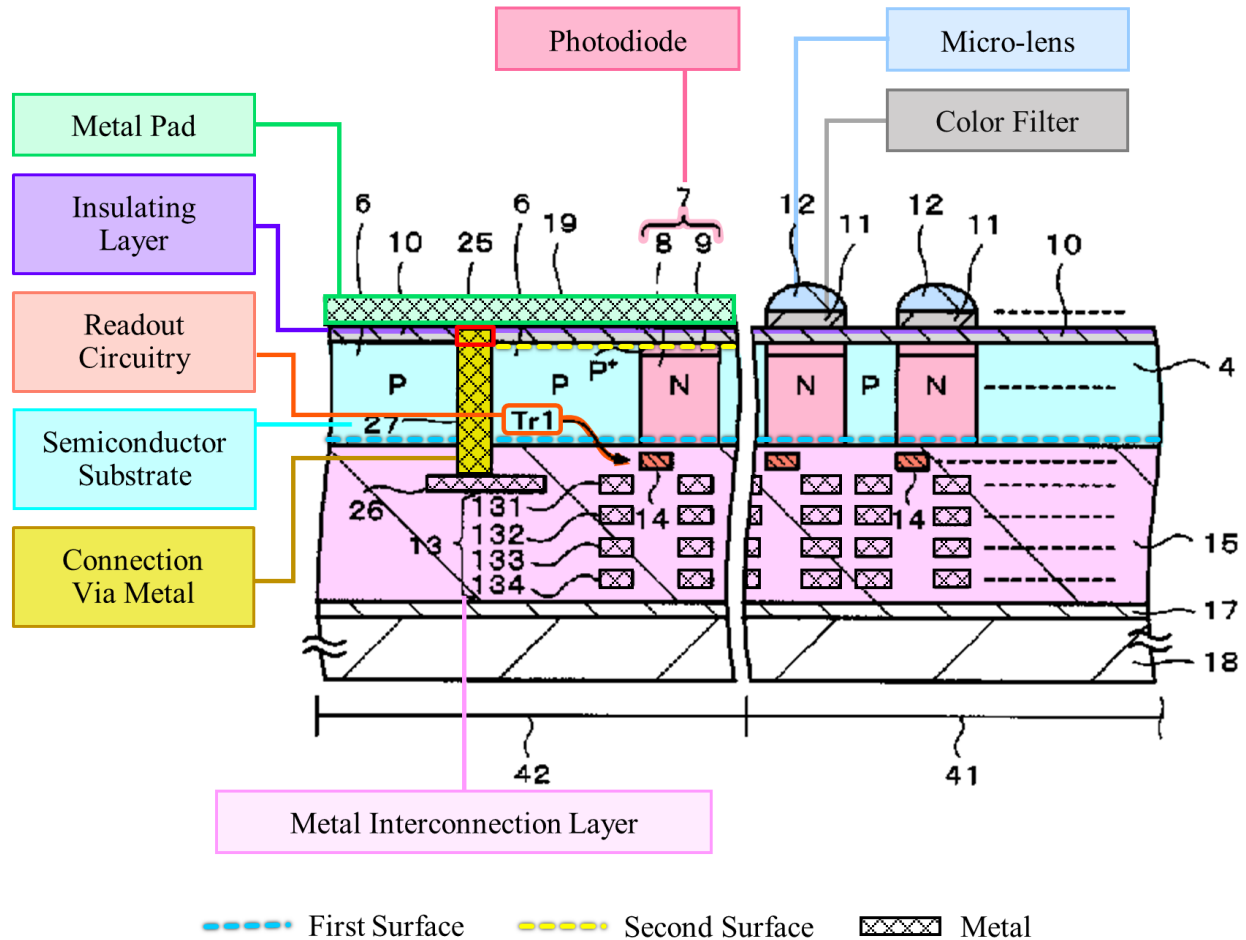
197. POSAs implementing Yanagida-1 would have had reason to incorporate a metal-based interconnection layer. Pain-1, [0036]. Fabricating wiring 26 using a low-resistivity metal such as copper would ensure that the wiring serves its disclosed function, including electrically connecting to the conductive material in the connection via. Garrou, 157-173; Quirk 305-306. Yanagida-1 teaches applying a voltage to the “conductive material layer 25...by using the wiring 26 formed within the insulating layer 15 on the front face side of the single crystal silicon layer 4, and the electrode layer 20 of the pad region 43 [is] connected to the

wiring 26. It is adapted to apply a voltage to the conductive material layer 25 via the electrode layer 20. The wiring 26 and the electrode layer 20 are connected....” Yanagida-1, [0039]. Further, Yanagida-1 states, “a conductive material layer 25 is formed in an element separation region 5 of the optical black region 42, a voltage application means is constructed to apply a voltage to the conductive material layer 25 from the front face side of the single crystal silicon layer 4.” *Id.*, [0075]. Metal conductors, especially copper, were commonly used in image sensors by 2008 to provide high conductivity. Garrou, 157-173. POSAs therefore would have used metal in Yanagida-1’s wiring in the ordinary course of implementing Yanagida-1’s design.

198. Similarly, POSAs would have had reason to fabricate Yanagida-1’s light shielding film using metal to fulfill the film’s disclosed function of electrically connecting to the conductive material in the hole. Yanagida-1, [0064]. As with the conductive material, metal would have been an obvious choice to ensure the electrical connection.

#### **b. Resultant Metal-Yanagida-1 Sensor**

199. The image sensor resulting from implementing Yanagida-1’s design using metal in the interconnection layer and pad (“Metal-Yanagida-1 Sensor”) is shown below.



200. As the figure illustrates, Yanagida-1's device is not impacted by the above-discussed selection of metal for wiring 26 and light shielding film 19.

201. Wiring 26 (*i.e.*, the metal interconnection layer) is formed on the front side of the sensor and connected to the conductive material in connection via (hole 27). The wiring layer is etched from the BSI sensor's rear side—requiring a material that can be processed at low temperatures. Metals such as copper can be deposited at low temperatures—confirming the above-noted reasons for using metal.

202. As with the interconnection layer, the pad (light shielding film 19) can be implemented using metal without impacting the sensor's structure. The metal pad would be formed over the projection part of the connection via using a low-temperature process compatible with rear-side fabrication. The resultant metal pad in Yanagida-1 may be patterned and routed to other elements to conduct electrical signals in the same manner as the electrode pad currently does in the device design. Yanagida-1, [0075].

**c. Reasonable Expectation of Success**

203. POSAs would have had a reasonable expectation success in implementing a metal interconnection layer in Yanagida-1's sensor. Quirk, 320-323; Garrou 157-173. Yanagida-1 itself does not disclose specify a particular material for its wiring 26 and light shielding film 19. POSAs would have had a reasonable expectation of success when using any suitable material consistent with the physical design and fabrication requirements of the Yanagida-1 device. Metal would have been desirable due to its high conductivity, low resistivity, and compatibility with the low-temperature methods required for the backside fabrication process.

204. Second, the backside fabrication process is a low temperature process well-known to POSAs. Pain-1, [0053], [0060]; Quirk 271-272. The rear-side fabrication requires the use of materials compatible with the low temperature

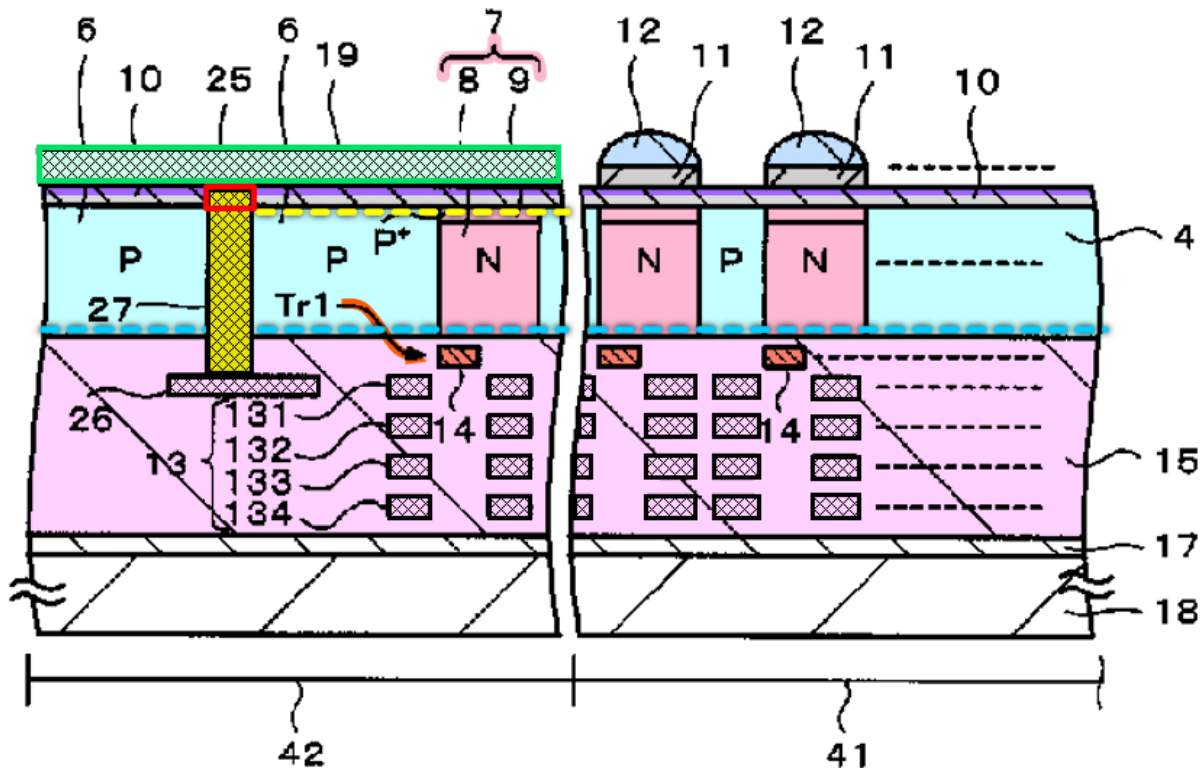
process. Pain-1, [0060]-[0061]. POSAs would thus have had a reasonable expectation of implementing metal wiring and pads using such a well-known process.

## 2. Claim-by-Claim Analysis

### a. Claim 1

#### i. Preamble – “An image sensor comprising:”

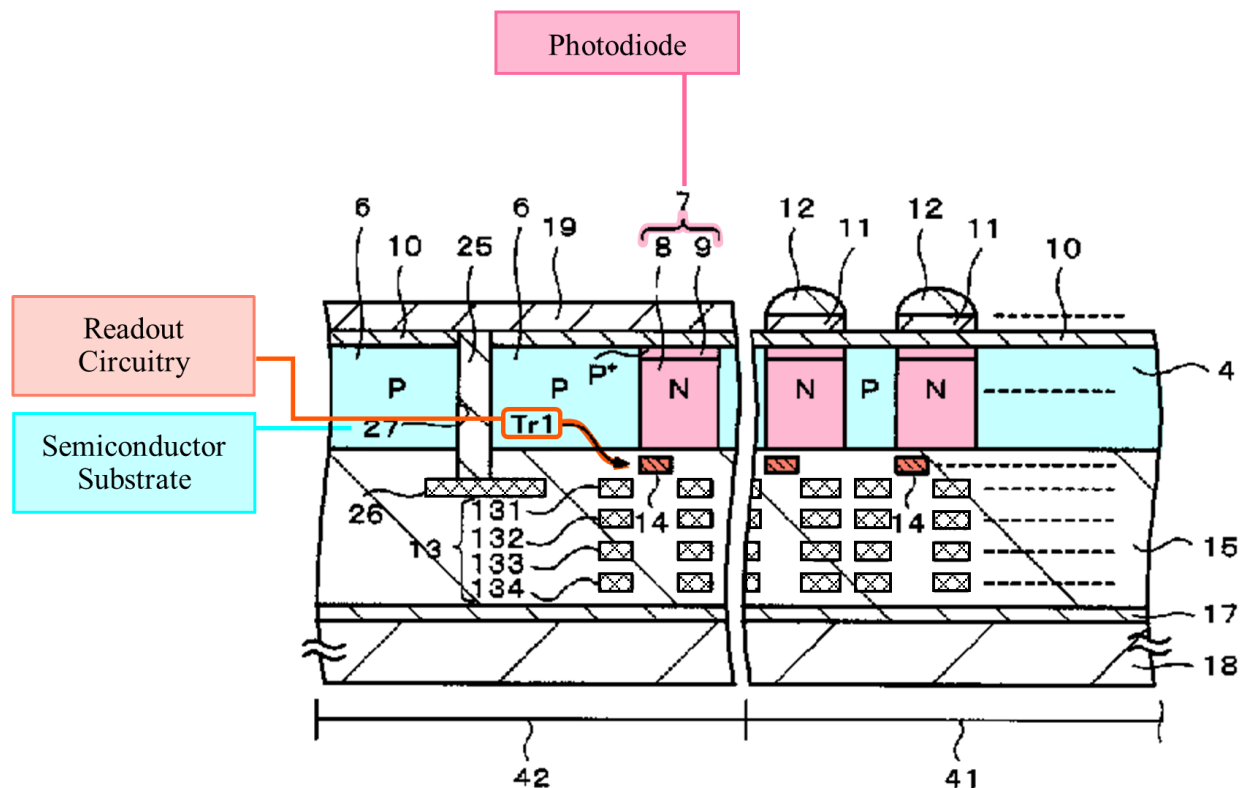
205. Yanagida-1 discloses a “solid-state image sensor,” which constitutes an “image sensor” per the preamble. Yanagida-1, [0012].



#### ii. Claim [1A] – “a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;”

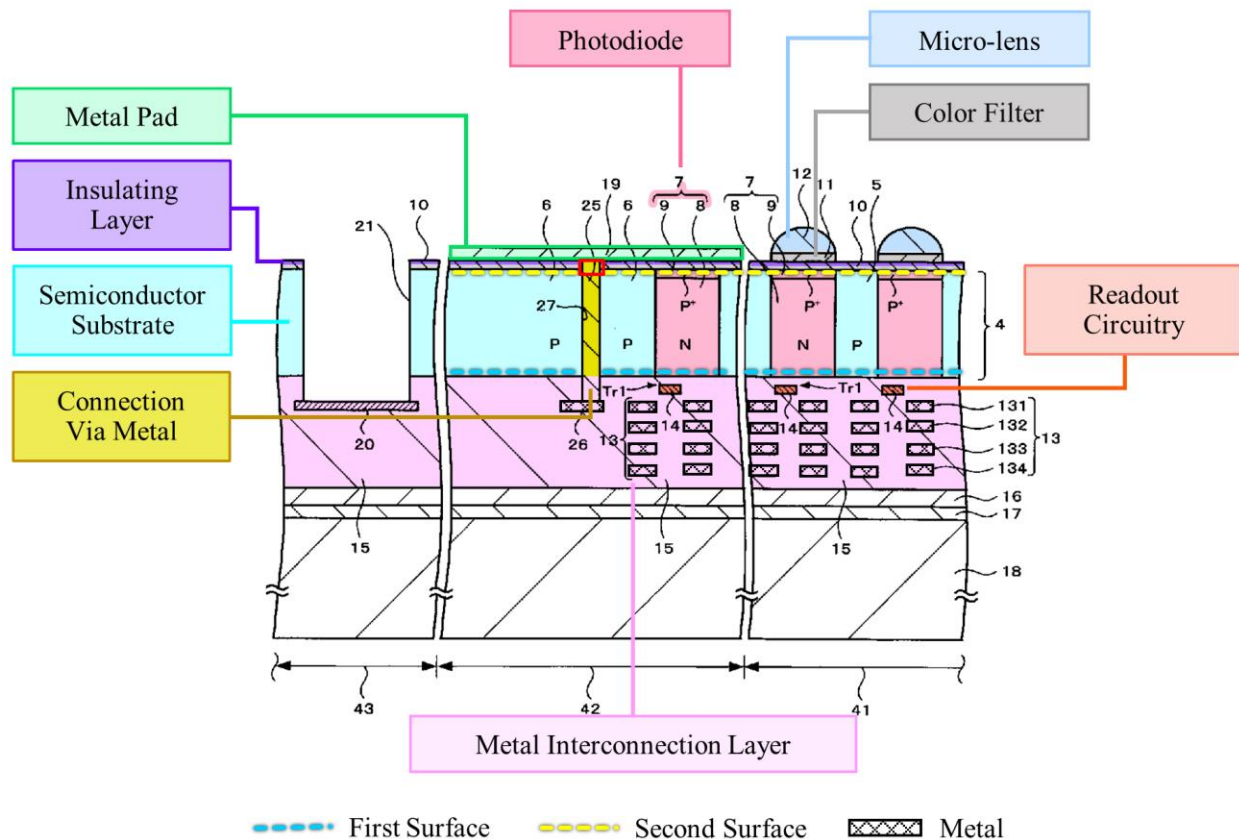
206. Yanagida-1’s image sensor includes a semiconductor substrate formed on a first surface with readout circuitry and a photodiode area. Yanagida-1

discloses a sensor in which lights is “irradiated against the photoelectric conversion elements from the back face side of the semiconductor substrate, wherein the solid-state image sensor is constructed with a semiconductor region formed in the semiconductor substrate at the periphery of the photoelectric conversion elements...” Yanagida-1, [0012].



207. Regarding the photodiode, Yanagida-1 states “[i]n the image pickup region 41, as shown in Fig. 2, photoelectric conversion elements 7 comprising N-type semiconductor regions are formed in unit pixel regions divided by the element separation regions 5 formed in the semiconductor substrate (e.g., single crystal silicon layer) 4. The photoelectric conversion elements 7 is each formed with a

charge accumulation region 8 comprising an N-type semiconductor region, and a positive charge accumulation region 9 comprising a high concentration P-type semiconductor region.” *Id.*, [0025]. POSAs would understand the photoelectric conversion elements as photodiodes, as illustrated below.

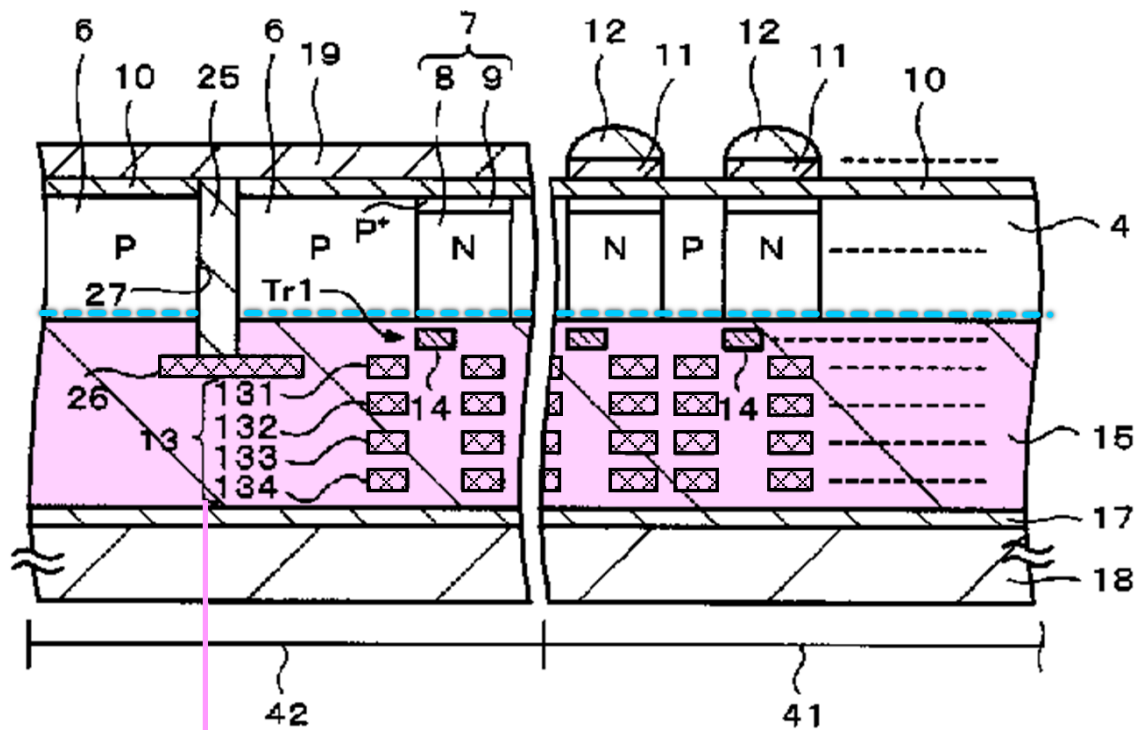


208. Further, readout circuitry is formed with the photo conversion elements. Specifically, “[o]n the other principal face side of the single crystal silicon layer 4, i.e., the front face side (lower side in the figure), MOS type transistors Tr1, for example, are formed in correspondence to the photoelectric conversion elements 7, and multilayer wiring layers 13 are formed on the

transistors Tr1.” *Id.*, [0026]. POSAs would understand the transistors as readout circuitry.

iii. **Claim [1B] – “a metal interconnection layer formed on the first surface;”**

209. Yanagida-1 discloses **wiring layers 13** on the front face side of the semiconductor well region 6. Yanagida-1, [0036]. POSAs would therefore understand Yanagida-1’s wiring layers 13 as an interconnection layer.

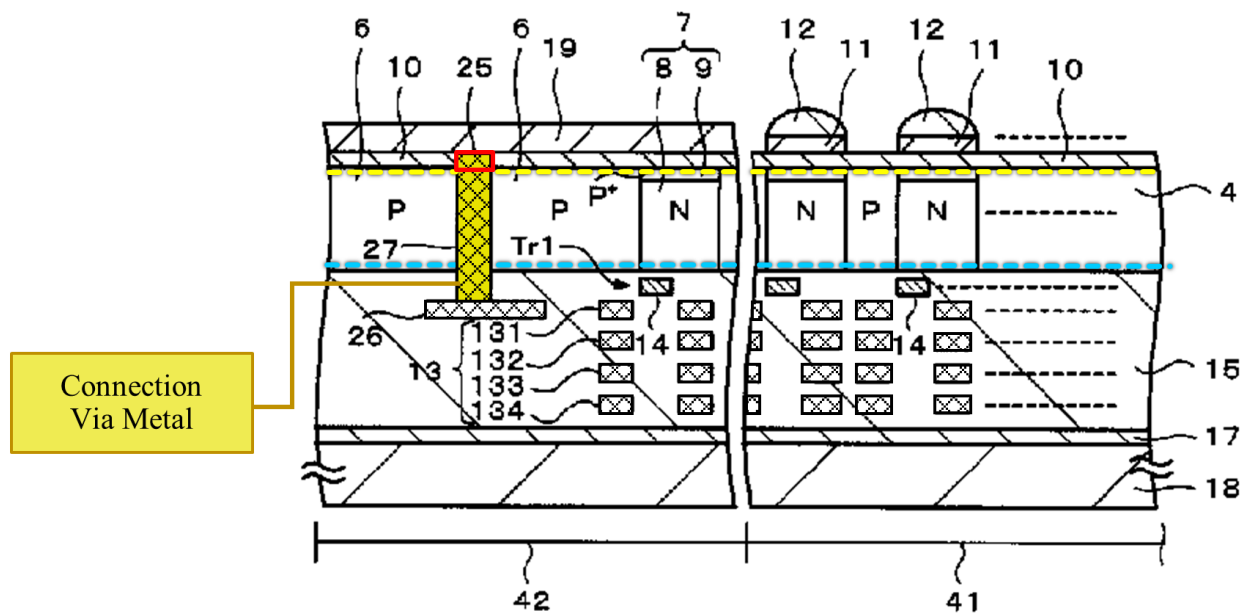


210. As discussed above, it would have been obvious when implementing Yanagida-1 to incorporate metal-based wiring, therefore forming a metal interconnection layer.

211. As shown above, metal interconnection layer 13 is formed on a first surface of the substrate.

- iv. **Claim [1C] – “a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface;”**

212. As seen in the figure below, Yanagida-1 discloses a connection via (hole 27) extending from the substrate’s first surface to the second surface. The figure below illustrates the projection part (red box) of the connection via of the hole projecting from the second surface of the substrate.



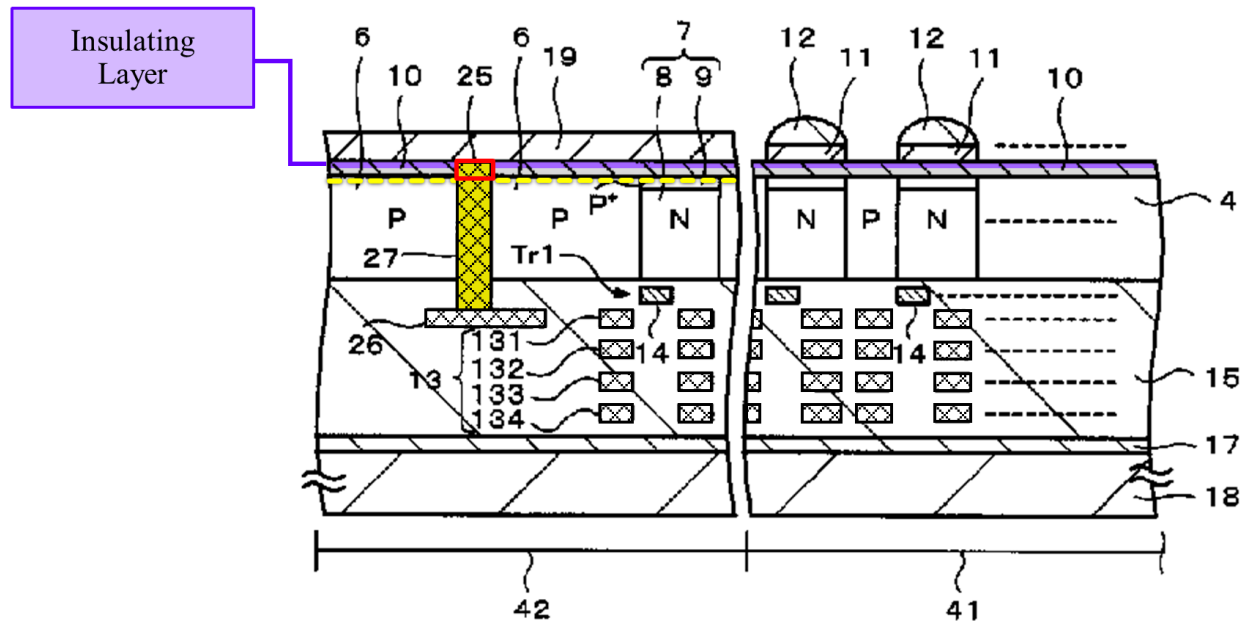
213. Further, Yanagida-1 teaches the connection via 27 comprises a metal material film. Yanagida-1, [0036] (“conductive material layer 25 is formed by being embedded in the **hole 27.**”). Yanagida-1 states, “[f]or the conductive material layer 25, a conductive material, for example, **metal materials, such as**

**AlCu, Al, AlSi, or W can be used.** When such a metal material is used, the resistance of the conductive material layer 25 will be lower than that within the semiconductor well region 6.” *Id.*, [0037].

- v. **Claim [1D] – “an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and”**

214. Yanagida-1 discloses an antireflective film 10 comprising oxide and nitride layers. Yanagida-1, [0026]. POSAs would recognize the oxide layer itself as an insulating layer. As discussed previously, POSAs would have known that the oxide insulating layer in the antireflective film 10 would have been etched to expose the projection part of the connection via while surrounding a portion of the lateral side of the projection part.

215. The antireflective film comprising the oxide film is formed on the second surface of the substrate. “More specifically, in the state where the single crystal silicon layer 4 of the SOI substrate 30 is exposed [], an antireflective film is formed on the single crystal silicon layer 4, then a photoresist film is formed on the antireflective film, and then the resist mask having the pattern for forming the opening and the hole is formed by a known lithography process.” *Id.*, [0063].



216. As seen in the figure above, the antireflective film 10 (purple) comprising the oxide film exposes the projection part (red box) and surrounds the lateral sides of the projection part.

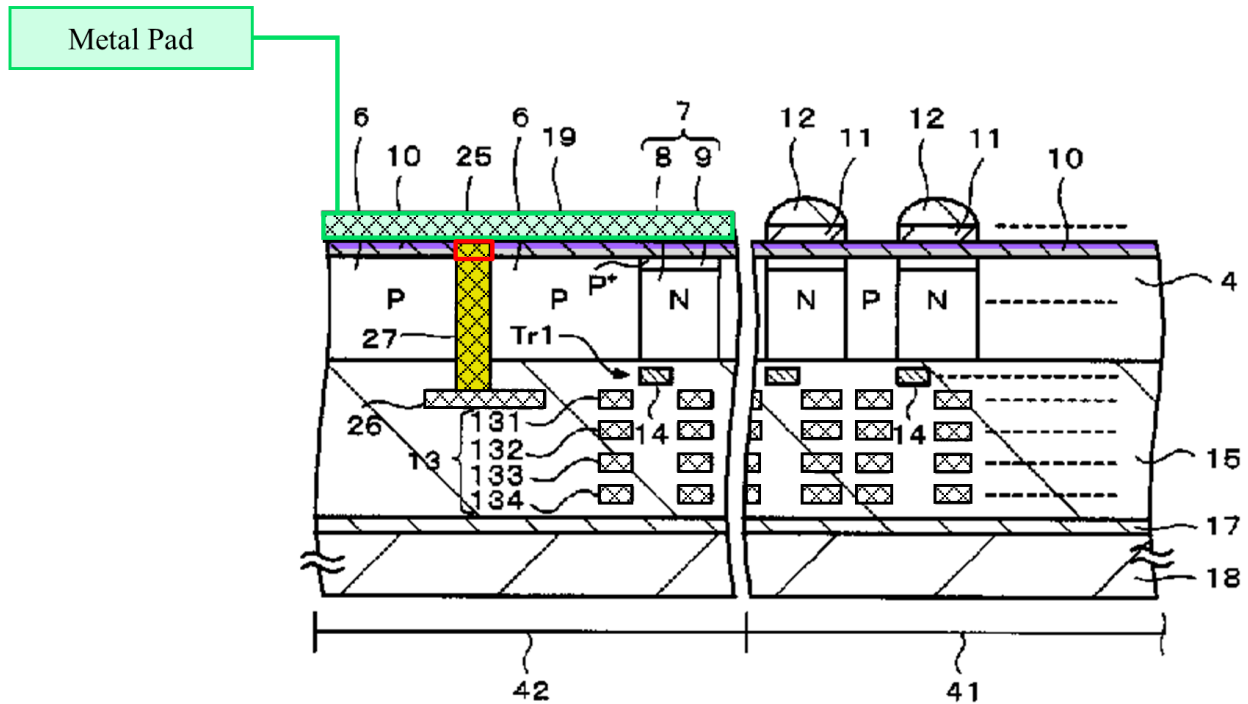
**vi. Claim [1E] – “a metal pad formed on the insulating layer such that the metal pad covers the projection part,”**

217. Yanagida-1’s light shielding film is a pad. A bonding pad is “a metallized area on the surface of a semiconductor device, to which connections can be made.” McGraw-Hill (Ex. 1024), 266; *see also* Laplante (Ex. 1025), 6. Although Yangida-1 does not specifically state the light shielding film is metal, the use of metal was well-known. POSAs would have known how to implement these structures using metal and the use of metal would have yielded predictable results.

218. Yanagida-1 states, “[i]n the optical black region 42, a light shielding film 19 is formed on the back face side of the single crystal silicon layer 4 via the

antireflective film 10.” Yanagida-1, [0031]. “The light shielding film 19 is formed so as to cover all the photoelectric conversion elements formed in the optical black region 42.” *Id.* Further, “voltage can be applied to the conductive material layer 25 via the light shielding film 19.” *Id.*, [0075]. POSAs would have recognized that Yanagida-1’s light shielding film 19 is a pad; the design and layout is identical to structures commonly used as bond pad or bump landing pad. McGraw-Hill, 266; *see also* Laplante, 6. Similar to the metal pad described in the ’143 patent, Yanagida-1’s light shielding film 19 connects to a super via.

219. Further, a metal pad serves to provide electrical interconnection from outside the chip. Yanagida-1 teaches “a wire is connected to the light shielding film 19 of the optical black region 42 so that a voltage can be applied to the conductive material layer 25 via the light shielding film 19.” Yanagida-1, [0075]. POSAs would understand the light shielding film 19 is the only structure in Yanagida-1 that provides an external connection. As such, the light shielding film 19 renders obvious the “metal pad” recited in claim 1. The connection of the structure to the via is consistent with a metal pad.

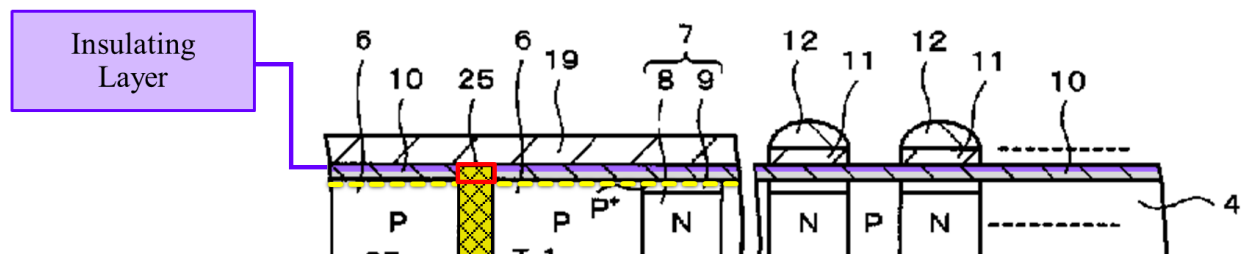


220. Yanagida-1 does not describe the material composition of light shielding film 19; however, it would have been obvious when implementing Yanagida-1 to select a metal-based film for the reasons discussed above.

**vii. Claim [1F] – “wherein the insulating layer has a thickness thinner than a projection height of the projection part.”**

221. As seen in the figure below, the projection part extends past the substrate through Yanagida-1’s antireflective film 10 and has a thickness that is at least equal the film’s height. The antireflective film comprises both an oxide film and nitride film. Yanagida-1, [0026]. The ’143 patent does not explicitly identify an “insulating layer” formed on a second surface of the substrate. Rather, the ’143 patent discloses a liner oxide layer 170 such that the “liner oxide layer 170” itself constitutes the “insulating layer.” See ’143 patent, 5:4-38. As discussed previously,

the disclosure in the '143 patent, the insulation layer comprises only an oxide layer. As such, the oxide insulating layer alone in Yanagida-1's antireflective film 10 corresponds to the insulating layer recited in the '143 patent. The thickness of the projection part is the sum of the thicknesses of the oxide insulating layer and nitride film in Yanagida-1. In sum, the thickness of the projection part in Yanagida-1 exceeds the thickness of the insulating oxide film.

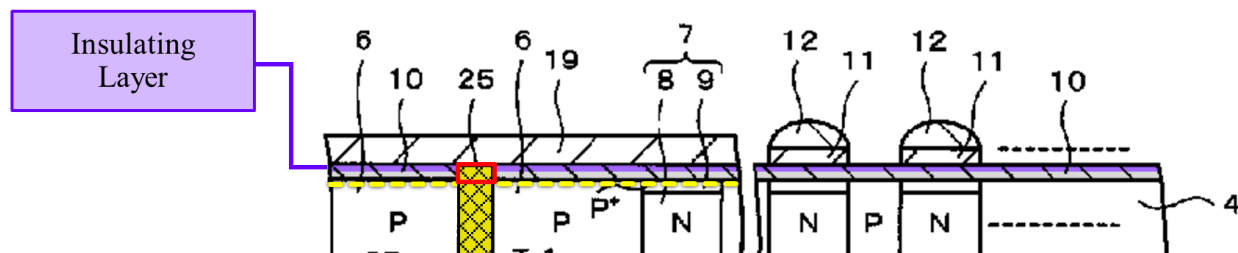


**b. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”**

222. While Yanagida-1 does not disclose the exact composition of the oxide film (*i.e.*, the insulating layer as discussed above), POSAs would have had reason to select TEOS for the same reasons discussed previously. Incorporating a TEOS layer would have constituted the use of a known material (TEOS) for its intended function (insulating) to yield the predictable result of providing the oxide film in Yanagida-1's sensor.

- c. **Claim 3 – “The image sensor of claim 1, wherein the insulating layer is formed on a portion of the projection part extending from the second surface.”**

223. Yanagida-1’s oxide film (*i.e.*, the insulting layer as discussed above) is formed on a portion of the projection part extending from the second surface. The figure below shows the oxide insulating layer in antireflective film 10 is formed on the lateral sides of the projection part of hole 27.



**F. GROUND 6: CLAIMS 2 AND 4 WOULD HAVE BEEN OBVIOUS OVER YANAGIDA-1 IN VIEW OF YANAGIDA-2**

**1. Combination of Yanagida-1 and Yanagida-2**

224. POSAs would have recognized that TEOS was a particularly desirable type of oxide to use in Yanagida-1’s oxide layer.

**a. Reasons for Incorporating Yanagida-2’s Teachings**

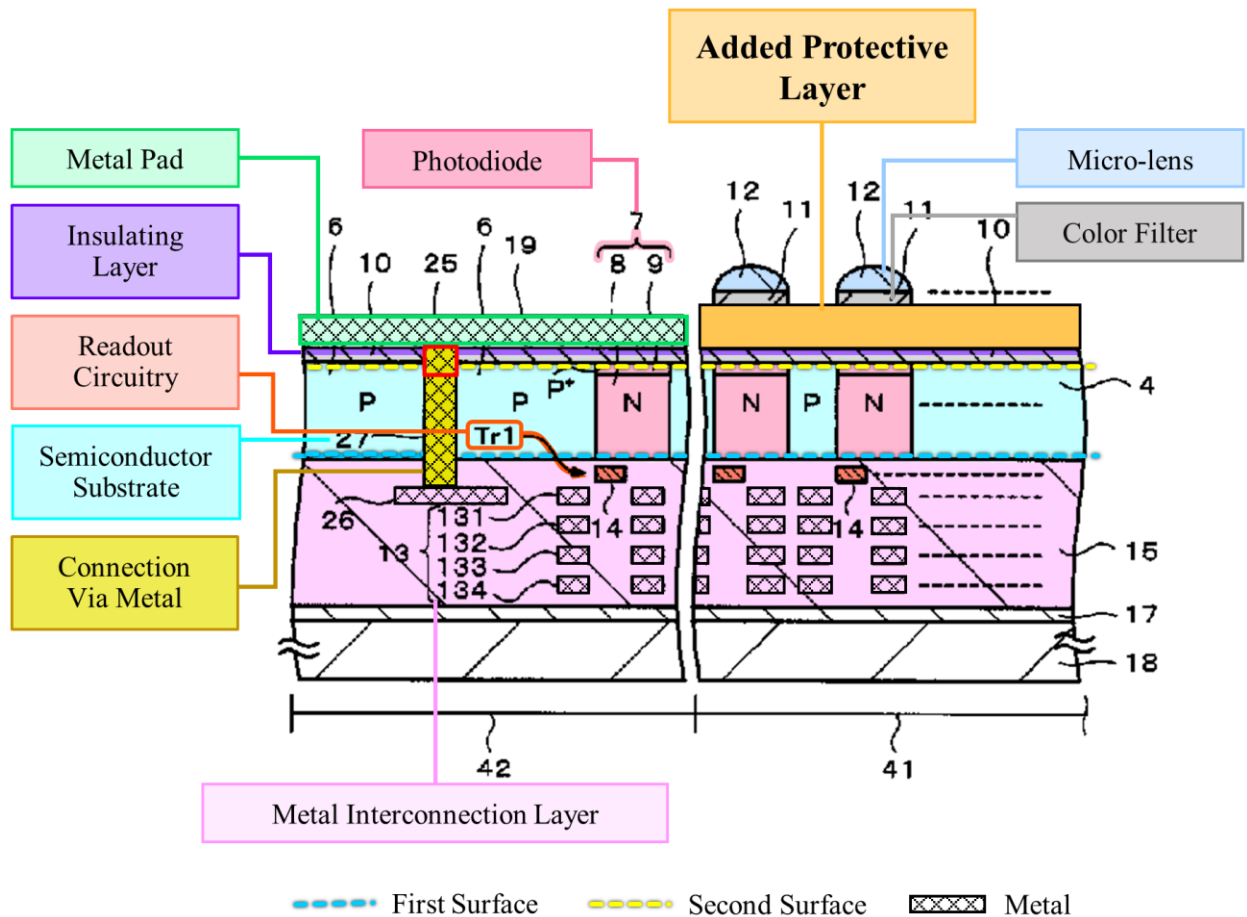
225. Yanagida-1 and Yanagida-2 both describe backside-illuminated image sensors and address the same problem of light inefficiency and sensitivity caused by frontside-illuminated sensors. Yanagida-1 and Yanagida-2 teach insulation elements, comprising at least an oxide layer, formed on the light incident side of the substrate. Yanagida-1, [0026]; Yanagida-2, [0034]. They also both describe the

oxide layer as paired with a nitride film. Yanagida-1, [0026] (components of Yanagida-1's "antireflective film 10"); Yanagida-2, [0043] (components of Yanagida-2's "anti-reflection film 90"). Yanagida-2 specifically discloses TEOS as the oxide layer in the antireflection film (Yanagida-2, [0043]), and POSAs likewise would have recognized TEOS as a very common and particularly desirable type of oxide for Yanagida-1's film. Using a TEOS layer as a low-temperature insulator formed on the backside and using a protective layer above the oxide insulating layer would better passivate the device, as Yanagida-2 disclosed.

**b. Resultant Metal-Yanagida-1-Yanagida-2 Sensor**

226. The sensor resulting from implementing the Metal-Yanagida-1 Sensor design using a TEOS layer would not change the device's physical structure or methods for fabrication. The TEOS material would be used in the oxide insulating layer in the antireflective film 10. As taught in Yanagida-1, the insulation layer comprises an oxide film. As discussed above, TEOS is a common oxide material. Pain-2, [0074].

227. The sensor resulting from modifying the Metal-Yanagida-1 Sensor to include a protective layer on the insulating layer ("Metal-Yanagida-1-Yanagida-2 Sensor") is shown below.



228. As seen above, the protective layer will form a layer above the oxide insulating layer—preventing the adverse effects described above in ¶148. Further, when formed on the insulating film, the protective layer will be patterned and etched to expose Yanagida-1’s metal pad. This is consistent with Yanagida-1’s color filter and microlenses; Yanagida-2 discloses that both can be formed on the protective layer. Yanagida-2, [0035].

### c. Reasonable Expectation of Success

229. POSAs would have had a reasonable expectation of success in using a TEOS layer as the Metal-Yanagida-1 Sensor’s oxide film and also forming a

protective layer on the film. Both procedures are known in the art and would require no modification to Yanagida-1's physical design. Pain-2, [0074]; Quirk 271-272.

## **2. Claim-by-Claim Analysis**

### **a. Claims 1 and 3**

230. The combination of Yanagida-1 and Yanagida-2 meets claims 1 and 3 for the same reasons as Yanagida-1 alone discussed above, which are unchanged in the combination.

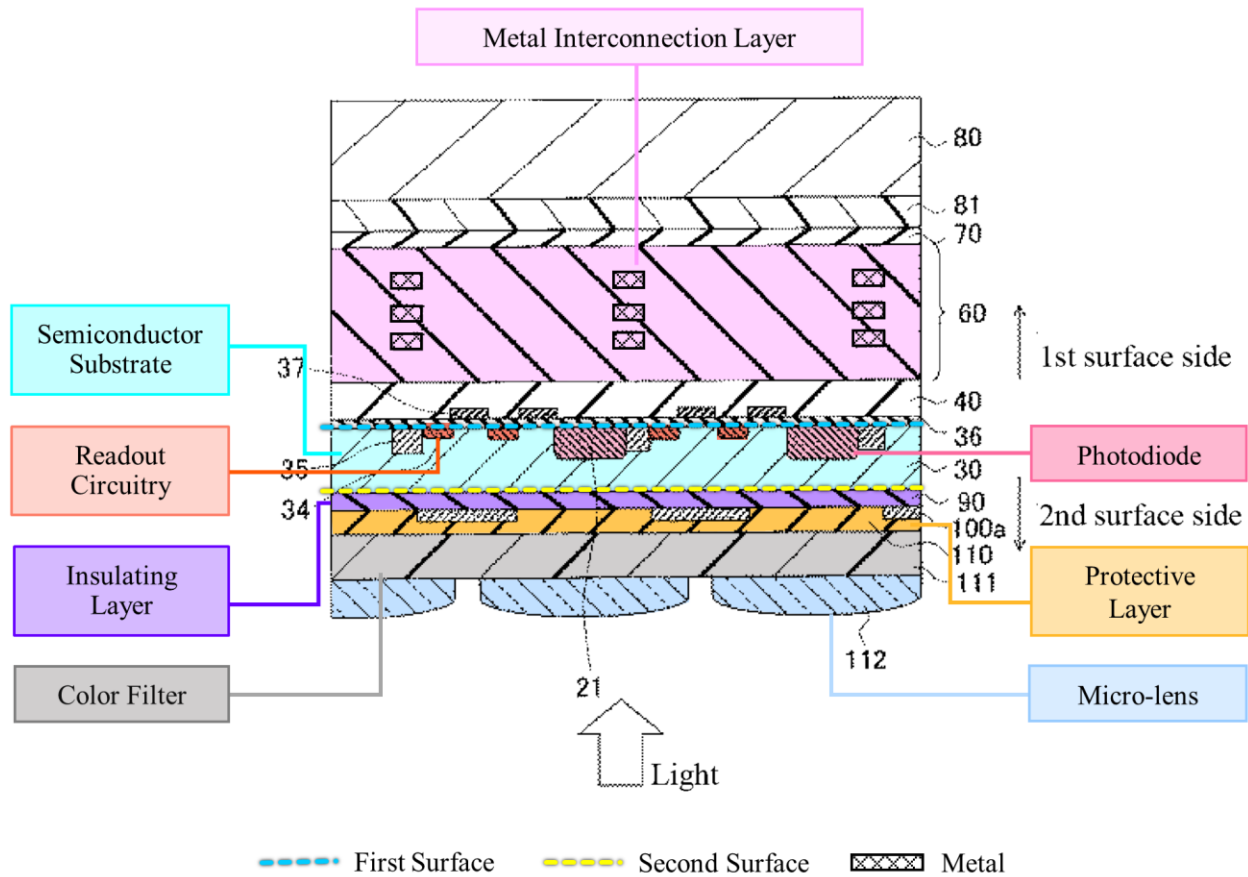
### **b. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”**

231. As discussed previously, TEOS was a commonly known material for oxide layers and facilitates the low-temperature fabrication required for BSI sensors such as Yanagida-1. POSAs accordingly would have been motivated to use a TEOS layer as described in Yanagida-2 as an insulating layer in Yanagida-1. Indeed, both Yanagida-1 and Yanagida-2 teach an insulating layer comprising an oxide, and POSAs would have understood that a TEOS layer would be a low-temperature oxide suitable for BSI fabrication.

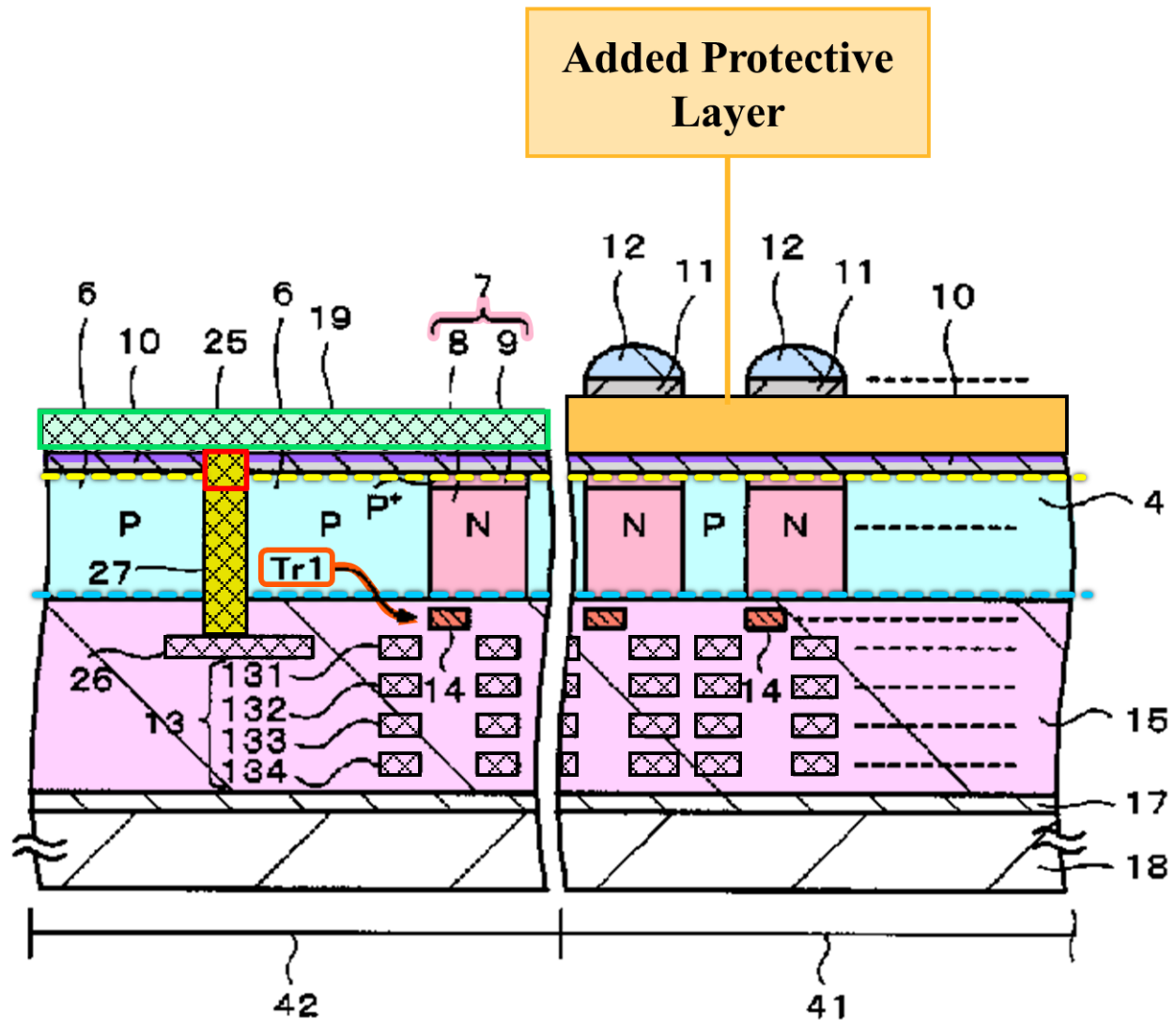
### **c. Claim [4A] – “The image sensor of claim 1, further comprising: a protective layer formed over the insulating layer; and”**

232. Yanagida-1 teaches “a color filter 11 is formed via an antireflective film (oxide film and nitride film) 10.” Yanagida-1, [0026]. Similarly, Yanagida-2,

as shown below, also teaches a continuous protective layer 110 formed on the anti-reflection film 90 on the surface of the substrate. Yanagida-2, [0034].



233. POSAs would have been motivated to combine the protective layer taught in Yanagida-2 with the color filter 11 in Yanagida-1 to improve robustness to intrusion of moisture and mobile ions.



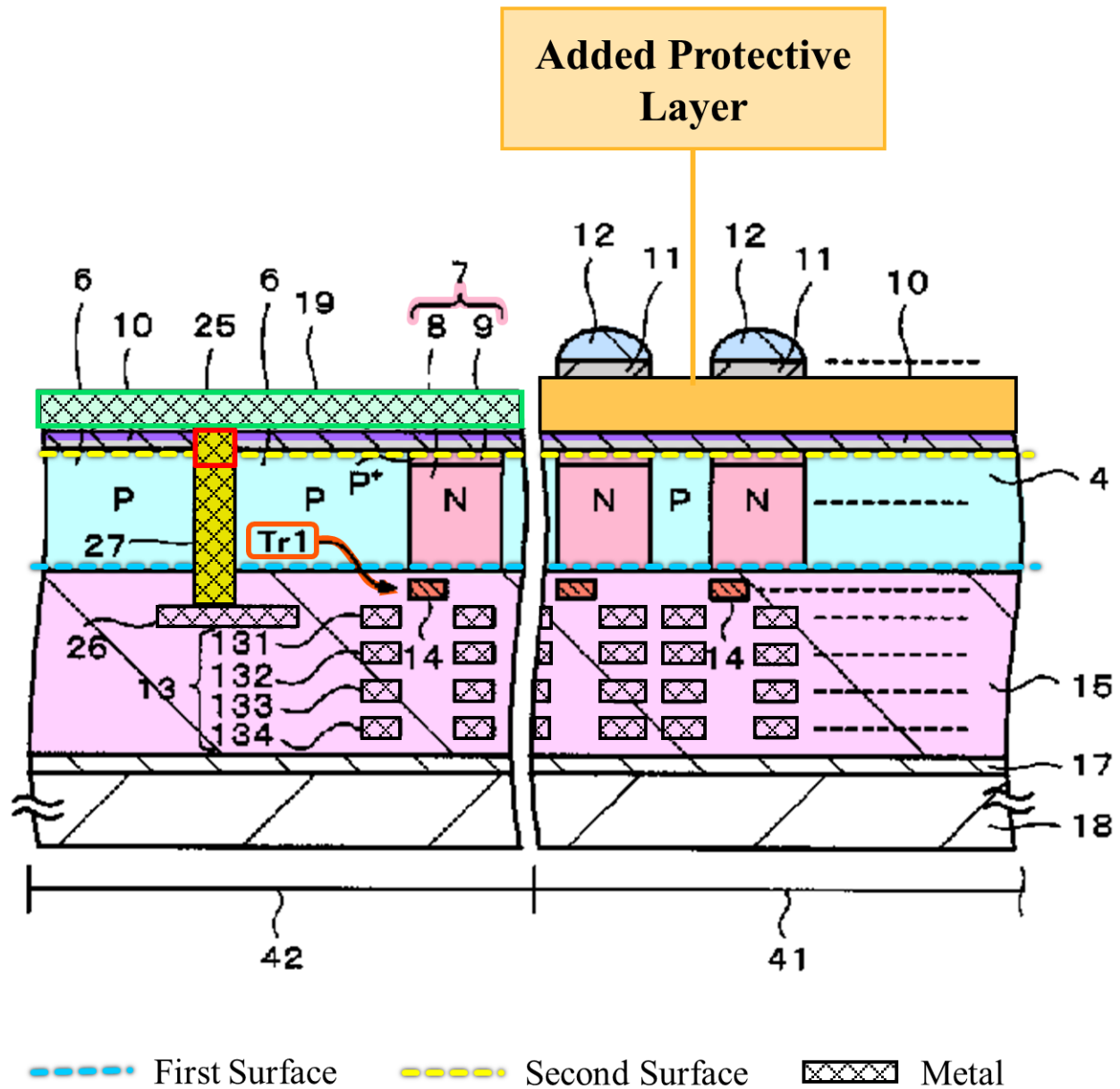
- - - First Surface     
 - - - Second Surface     
 X X X X Metal

234. As such, the combination of Yanagida-1 and Yanagida-2 render this element obvious.

**d. Claim [4B] – “a micro-lens formed on the protective layer in a region corresponding to the photodiode area.”**

235. Yanagida-1 teaches “on-chip lenses 12 are formed on the color filter 11 at the positions corresponding to the photoelectric conversion elements 7.” Yanagida-1, [0026]. Similarly, Yanagida-2 teaches a micro-lens formed over the protective layer. Specifically, Yanagida-2 states that “[o]n the protective film 110, a color filter 111 is formed to pass only light in a desired wavelength region. In addition, on the color filter 111, an on-chip lens 112 is formed to focus the incident light onto the photodiode 21.” Yanagida-2, [0035].

236. As previously discussed, POSAs would have been motivated to combine the teachings of Yanagida-1 and Yanagida-2 to form a protective layer on the antireflective film.



237. POSAs would have understood that the on-chip lenses in Yanagida-1 may be formed over the protective layer on the antireflective film. POSAs would understand that this would increase the light reaching the photodiode and allow control over which wavelengths of light will be allowed to pass. Yanagida-2, [0035]. Further, forming the micro-lens over a protective layer better passivates the

sensor. As such, this element is rendered obvious over Yanagida-1 in view of Yanagida-2.

\* \* \*

I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

Dated: 12/19/2022

A handwritten signature in black ink, reading "R. Michael Guidash", written over a horizontal line.

R. Michael Guidash

## APPENDIX A TO THE DECLARATION OF R. MICHAEL GUIDASH

### CLAIM LISTING

| Ref             | Claim                                                                                                                                                                                             |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Preamble</b> | An image sensor comprising:                                                                                                                                                                       |
| <b>[1A]</b>     | a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;                                                                                       |
| <b>[1B]</b>     | a metal interconnection layer formed on the first surface;                                                                                                                                        |
| <b>[1C]</b>     | a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface; |
| <b>[1D]</b>     | an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and           |
| <b>[1E]</b>     | a metal pad formed on the insulating layer such that the metal pad covers the projection part,                                                                                                    |
| <b>[1F]</b>     | wherein the insulating layer has a thickness thinner than a projection height of the projection part.                                                                                             |
| <b>2</b>        | The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.                                                                                                                 |
| <b>3</b>        | The image sensor of claim 1, wherein the insulating layer is formed on a portion of the projection part extending from the second surface.                                                        |
| <b>[4A]</b>     | The image sensor of claim 1, further comprising: a protective layer formed over the insulating layer; and                                                                                         |
| <b>[4B]</b>     | a micro-lens formed on the protective layer in a region corresponding to the photodiode area.                                                                                                     |