

Filed on behalf of Petitioner by:

Paper No. ____

Randy J. Pritzker, Reg. No. 35,986

Michael N. Rader, Reg. No. 52,146

Marc S. Johannes, Reg. No. 64,978

Sushmitha Rajeevan (pending admission *pro hac vice*)

Charles T. Steenburg (pending admission *pro hac vice*)

WOLF, GREENFIELD & SACKS, P.C.

600 Atlantic Avenue

Boston, MA 02210

(617) 646-8000 Phone

(617) 646-8646 Fax

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY GROUP CORPORATION,
Petitioner,
v.

VISIONX TECHNOLOGIES, LLC,
Patent Owner.

Case No. TBD
Patent No. 8,035,143

**PETITION FOR INTER PARTES REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq**

TABLE OF CONTENTS

MANDATORY NOTICES.....	x
A. Related Matters.....	x
B. Real Parties-In-Interest.....	x
A. Counsel and Service Information - § 42.8(b)(3) and (4).....	x
I. INTRODUCTION	1
II. NOTICE OF FEES PAID	4
III. CERTIFICATION OF GROUNDS FOR STANDING	4
IV. IDENTIFICATION OF CHALLENGED CLAIMS	4
V. GROUNDS FOR UNPATENTABILITY	4
VI. THE '143 PATENT	5
A. Described Embodiments.....	5
B. Person of Ordinary Skill in the Art	7
C. Prosecution History	7
VII. CLAIM INTERPRETATION	8
VIII. <u>GROUND 1</u> : CLAIMS 1-3 WOULD HAVE BEEN OBVIOUS OVER SUMI'S RELATED-ART EMBODIMENT	9
A. Sumi (Ex. 1005).....	9
1. Overview of Sumi	9
2. The Related-Art Embodiment	11
B. Obviousness of Implementing Sumi's Related-Art Embodiment With Metal Components	15
1. The Use of Metal Was Well-Known.....	15
2. Reasons For Using Metal	16
3. Reasonable Expectation of Success	17
4. Resultant Metal-Related-Art Sensor	18
C. Claim 1	19
1. Preamble – “An image sensor comprising:”	19
2. [1A] – “a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;”	19

3. [1B] – “a metal interconnection layer formed on the first surface;”	25
4. [1C] – “a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface;”	27
5. [1D] – “an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and”	30
6. [1E] – “a metal pad formed on the insulating layer such that the metal pad covers the projection part,”	31
7. [1F] – “wherein the insulating layer has a thickness thinner than a projection height of the projection part.”	32
D. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”	34
E. Claim 3 – “The image sensor of claim 1, wherein the insulating layer is formed on a portion of the projection part extending from the second surface.”	35
IX. <u>GROUND 2: CLAIMS 2 AND 4 WOULD HAVE BEEN OBVIOUS OVER SUMI’S RELATED-ART EMBODIMENT IN VIEW OF YANAGIDA-2</u>	36
A. Yanagida-2 (Ex. 1007)	37
B. Combination of Sumi’s Related Art Embodiment and Yanagida-2.....	39
C. Claims 1 and 3	43
D. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”	43
E. Claim 4 – [4A] “further comprising: a protective layer formed over the insulating layer; [4B] and a micro-lens formed on the protective layer in a region corresponding to the photodiode area.”	43
X. <u>GROUND 3: CLAIMS 1-3 WOULD HAVE BEEN OBVIOUS OVER SHIRAIWA IN VIEW OF SUMI’S RELATED-ART EMBODIMENT</u>	45
A. Shiraiwa (Ex. 1008).....	45

1. Overview of Shiraiwa.....	45
B. Shiraiwa-Sumi Combination	47
C. The Metal-Shiraiwa-Sumi Sensor	50
D. Claim 1	50
1. Preamble – “An image sensor comprising:”	50
2. [1A] – “a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;”	51
3. [1B] – “a metal interconnection layer formed on the first surface;”	52
4. [1C] – “a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface;”	54
5. [1D] – “an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and”	55
6. [1E] – “a metal pad formed on the insulating layer such that the metal pad covers the projection part,”	56
7. [1F] – “wherein the insulating layer has a thickness thinner than a projection height of the projection part.”	57
E. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”	58
F. Claim 3 – “The image sensor of claim 1, wherein the insulating layer is formed on a portion of the projection part extending from the second surface.”	58
XI. <u>GROUND 4: CLAIMS 2 AND 4 WOULD HAVE BEEN OBVIOUS OVER SHIRAIWA IN VIEW OF SUMI’S RELATED-ART EMBODIMENT AND YANAGIDA-2</u>	59
XII. <u>GROUND 5: CLAIMS 1-3 WOULD HAVE BEEN OBVIOUS OVER YANAGIDA-1</u>	61
A. Overview of Yanagida-1	61
B. Obviousness of Implementing Yanagida-1 Using Metal-Based Film.....	62

1. Reasons for Using Metal	62
2. Resultant Metal-Yanagida-1 Sensor	63
3. Reasonable Expectation of Success	64
C. Claim 1	65
1. Preamble – “An image sensor comprising:”	65
2. Claim [1A] – “a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;”	66
3. Claim [1B] – “a metal interconnection layer formed on the first surface;”	69
4. Claim [1C] – “a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface;”	70
5. Claim [1D] – “an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and”	71
6. Claim [1E] – “a metal pad formed on the insulating layer such that the metal pad covers the projection part,”	72
7. Claim [1F] – “wherein the insulating layer has a thickness thinner than a projection height of the projection part.”	74
D. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”	74
E. Claim 3 – “The image sensor of claim 1, wherein the insulating layer is formed on a portion of the projection part extending from the second surface.”	75
XIII. <u>GROUND 6: CLAIMS 2 AND 4 WOULD HAVE BEEN OBVIOUS OVER YANAGIDA-1 IN VIEW OF YANAGIDA-2</u>	75
A. Combination of Yanagida-1 and Yanagida-2.....	75
1. Reasons for Incorporating Yanagida-2’s Teachings	75
2. Resultant Metal-Yanagida-1-Yanagida-2 Sensor	76
3. Reasonable Expectation of Success	78

B. Claims 1 and 3	78
C. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”	78
D. Claim 4	79
1. Claim [4A] – “The image sensor of claim 1, further comprising: a protective layer formed over the insulating layer; and”	79
2. Claim [4B] – “a micro-lens formed on the protective layer in a region corresponding to the photodiode area.”	81
XIV.NO BASIS EXISTS FOR DISCRETIONARY DENIAL	83
A. Discretionary Denial Not Warranted Under Section 314(a)	83
1. Factor 1: Potential for litigation stay	83
2. Factor 2: Trial date relative to FWD deadline	83
3. Factor 3: Investment in parallel proceedings	84
4. Factor 4: Issue Overlap	84
5. Factor 5: Parties.....	84
6. Factor 6: Other considerations	84
B. Discretionary Denial Not Warranted Under Section 325(d).....	85
1. The References Cited Were Not “Presented to the Office”	85
2. Even if Yanagida-1 Was “Presented to the Office,” the Office Made a Material Error by Overlooking Its Impact	86
XV. CONCLUSION.....	87

TABLE OF AUTHORITIES

CASES

<i>Advanced Bionics v. Med-El Elektromedizinsche Gerate,</i> IPR2019-01469, Paper 6 (Feb. 13, 2020).....	86, 87
<i>Align Tech., Inc. v. 3Shape A/S,</i> IPR2021-01309, Paper 11 (Feb. 9, 2022).....	87
<i>Apple v. Fintiv,</i> IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential).....	84
<i>Apple v. Scramoge Tech.,</i> IPR2022-00573, Paper 12 (Sept. 13, 2022)	84
<i>Arista Networks v. Cisco Sys.,</i> IPR2016-00303, Paper 53 (May 25, 2017)	14
<i>Autostore Sys. v. Ocado Innovation Ltd.,</i> IPR2022-00673, Paper 7 (Sept. 14, 2022)	84, 85
<i>Cellco P’ship v. Huawei Device Co.,</i> IPR2020-01117, Paper 10 (Feb. 3, 2021).....	87
<i>Intel Corp. v. Qualcomm Inc.,</i> IPR2018-01429, Paper 8 (Feb. 15, 2019).....	14
<i>KSR Int’l Co. v. Teleflex Inc.,</i> 550 U.S. 398 (2007)	16, 34, 76
<i>Microsoft v. IPA Techs.,</i> IPR2018-00794, Paper 11 (Oct. 15, 2018).....	14
<i>Nidec Motor Corp. v. Zhongshan,</i> 868 F.3d 1013 (Fed. Cir. 2017)	8, 9
<i>Nokia of Am. Corp. v. TQ Delta,</i> IPR2022-00664, Paper 10 (Sept. 27, 2022)	85
<i>Puma North America v. Nike,</i> IPR2019-01058, Paper 10 (Oct. 31, 2019).....	87

<i>Samsung Elecs. v. Jawbone Innovations</i> , IPR2022-00630, Paper 10 (Sept. 13, 2022)	85
--	----

<i>Sand Revolution II v. Continental Intermodal Group-Trucking</i> , IPR2019-01393, Paper 24 (June 16, 2020)	85
---	----

STATUTES

35 U.S.C. § 103	5
-----------------------	---

35 U.S.C. § 325(d)	87
--------------------------	----

35 U.S.C. §102(b)	passim
-------------------------	--------

OTHER AUTHORITIES

83 Fed Reg. 51,340 (Oct. 11, 2018).....	9
---	---

REGULATIONS

37 C.F.R. § 42.100(b)	8
-----------------------------	---

APPENDIX LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 8,035,143 (“the ’143 patent”)
1002	Prosecution History of U.S. Patent No. 8,035,143
1003	Declaration of Michael Guidash (“Guidash”)
1004	Curriculum Vitae of Michael Guidash
1005	U.S. Patent Publication No. US 2006/0094151 A1 (“Sumi”)
1006	Certified English Translation of Japanese Publication No. JP 2006-032497 A (“Yanagida-1”)
1007	Certified English Translation of Japanese Publication No. JP 2006-339566 A (“Yanagida-2”)
1008	Certified English Translation of Japanese Patent Publication No. JP 2005-353996 A (“Shiraiwa”)
1009	U.S. Patent No. 7,875,948 (“Hynecek”)
1010	“Sony develops back-illuminated CMOS image sensor, realizing high picture quality, nearly twofold sensitivity(*1) and low noise”, Sony Group Portal - Sony Global Headquarters (June 11, 2008), https://www.sony.com/en/SonyInfo/News/Press/200806/08-069E/
1011	U.S. Patent Publication No. US 2006/0076590 A1 (“Pain-1”)
1012	U.S. Patent Publication No. US 2007/0117254 A1 (“Pain-2”)
1013	Jean-Luc Leray et al., An Overview of Buried Oxides on Silicon: New Processes and Radiation Effects. Journal de Physique III, EDP Sciences, 1996, 6 (12), 1625-1646 (“Leray”)
1014	Michael Quirk and Julian Serda, Semiconductor Manufacturing Technology, 257-333 (2001) (“Quirk”)
1015	Metallization by Chemical Vapor Deposition of W and Cu, 1 in Handbook of 3D integration: Technology and applications of 3D Integrated Circuits (Philip Garrou, Christopher Bower & Peter Ramm, eds., 2008) (“Garrou”)
1016	British Library Public Availability Date Authentication Letter
1017	Garrou Vol. 1 Public Availability Date Authentication
1018	Declaration of Mary Bolin
1019	H. C.M Knoop et al., “Deposition of TiN and TaN by Remote Plasma ALD for Cu and Li Diffusion Barrier Applications” Journal of The Electrochemical Society (Oct. 10, 2008)
1020	Japanese-language Publication of Japanese Publication No. JP 2006-032497 A

1021	Japanese-language Publication of Japanese Publication No. JP 2006-339566 A
1022	Japanese-language Publication of Japanese Publication No. JP 2005-353996 A
1023	U.S. Patent Publication No. US 2005/0179053 A1 (“Ezaki”)
1024	McGraw-Hill, McGraw-Hill Dictionary of Scientific and Technical Terms (6th ed. 2003) (“McGraw-Hill”)
1025	Electrical Engineering Dictionary (Phillip A. Laplante et al. eds., 2000) (“Laplante”)
1026	Robert S. Patti, “Three-Dimensional Integrated Circuits and the Future of the System-on-Chip Designs,” Proceedings of the IEEE, vol. 94, no. 6, 1214-1224, 2006 (“Patti”)

MANDATORY NOTICES

A. Related Matters

A decision in this proceeding could affect or be affected by the following:

VisionX Technologies, LLC v. Sony Group Corporation et al., Case No. 2:22-cv-00178 (E.D. Tex.) (“the Texas Litigation”).

B. Real Parties-In-Interest

Along with Petitioner Sony Group Corporation, the other defendants in the Texas Litigation—Sony Corporation, Sony Semiconductor Manufacturing Corporation, and Sony Semiconductor Solutions Corporation—are additional real parties-in-interest. In an abundance of caution, Petitioner states that other Sony affiliates—in particular Sony Corporation of America (SCA) and Sony Electronics Inc. (SEL)—could be additional real parties in interest.

A. Counsel and Service Information - § 42.8(b)(3) and (4)

Lead Counsel	Randy J. Pritzker, Reg. No. 35,986
Backup Counsel	Michael N. Rader, Reg. No. 52,146 Marc S. Johannes, Reg. No. 64,978 Sushmitha Rajeevan (<i>pro hac vice</i> application to be filed) Charles T. Steenburg (<i>pro hac vice</i> application to be filed)
Service Information	E-mail: RPritzker-PTAB@wolfgreenfield.com Mrader-PTAB@wolfgreenfield.com MJohannes-PTAB@wolfgreenfield.com Charles.Steenburg@wolfgreenfield.com Sushmitha.Rajeevan@wolfgreenfield.com

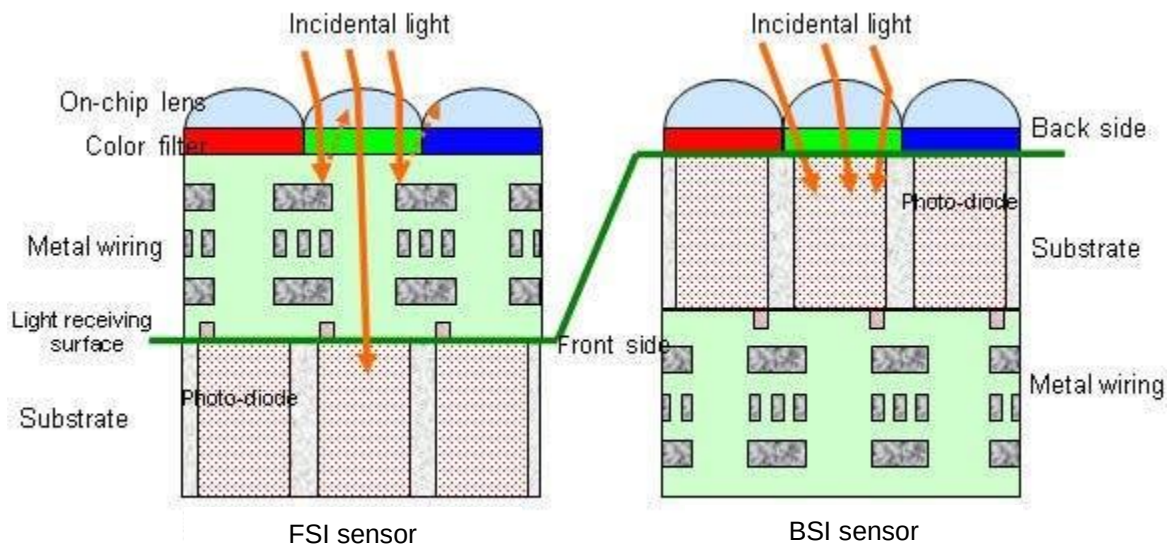
	<u>Post and hand delivery:</u> Wolf, Greenfield & Sacks, P.C. 600 Atlantic Avenue Boston, MA 02210-2206 <u>Telephone:</u> 617-646-8000 <u>Facsimile:</u> 617-646-8646
--	--

A power of attorney is submitted with the Petition. Counsel for Petitioner consent to service of all documents via electronic mail.

Petitioner requests *inter partes* review and cancellation of claims 1-4 (the “Challenged Claims”) of U.S. Patent No. 8,035,143 (“the ’143 patent,” Ex. 1001).

I. INTRODUCTION

The Challenged Claims concern backside-illuminated (“BSI”) image sensors—including those incorporating complementary metal-oxide semiconductor (“CMOS”) technology—for converting light into electrical signals. BSI CMOS image sensors had been described by 2004 (Pain-1 (Ex. 1011), [0001])—long before the ’143 patent. Unlike traditional frontside-illuminated (“FSI”) sensors, circuitry in BSI sensors is behind a photosensitive layer—maximizing the light reaching the sensor’s photodiodes. Guidash (Ex. 1003), ¶¶38-42; Ex. 1010.



Specifically, in FSI sensors, metal wiring connected to transistors (not shown above) that read out charge accumulated by the photodiodes are provided between the photodiodes formed in the substrate and corresponding on-chip lenses.

As illustrated above, the metal wiring in FSI sensors prevents some of the light incident on the on-chip lenses from reaching corresponding photodiodes. This reduced collection efficiency reduces the sensor's sensitivity—degrading image quality. Guidash, ¶38.

In contrast, BSI sensors allow more light to reach the photodiodes by positioning the wiring opposite the illuminated side of the semiconductor substrate—improving collection efficiency and image quality relative to FSI sensors. *Id.*, ¶40. Manufacturing BSI sensors typically begins by forming transistors and corresponding metal wiring layers on a front surface of a semiconductor substrate similar to FSI sensor fabrication. Guidash, ¶¶41-42; *see also* Sumi (Ex. 1005), [0009]-[0013], [0063]-[0067]. Instead of forming optical lenses on top of the wiring layers, the substrate is flipped over and optical lenses (and other layers) are formed on the **rear** surface. Guidash, ¶¶41-42; *see also* Sumi, [0015]-[0017], [0069]-[0070].

Because the semiconductor substrate in BSI sensors separates wiring layers (on one side) from the optical components and metal pad for connections (on another), a vertical connection via is formed through the semiconductor substrate—thereby electrically connecting the wiring and the pad. Guidash, ¶¶41-42; Sumi, [0016]-[0017]; Hyncek (Ex. 1009), 1:30-45, 4:7-14, 10:58-65; *See* Pain-1 (Ex. 1011), [0077].

Independent claim 1 concerns this conventional BSI image sensor structure; it recites a semiconductor substrate with a metal wiring layer formed on a first surface of the substrate and an insulating layer formed on a second surface. A metal via extends from the substrate's first surface to its second, and a metal pad is formed on the insulating layer—covering a projection part of the metal via that extends beyond the second surface of the substrate.

As detailed below, the examiner deemed the above structure unpatentable over the prior art. The claims were allowed following incorporation of a dependent claim requiring the insulating layer to have “a thickness thinner than a projection height of the projection part.” However, numerous prior art BSI sensors disclosed this structure, and claim 1 merely recites an obvious implementation of such BSI technology.

For example, Sumi discloses each limitation of claim 1 aside from not specifying the material for the sensor's electrical interconnects—*i.e.*, the disclosed wiring layers, connection via, and electrode pad. But using metal for these interconnects was standard practice and had well-known benefits (*see* §VIII.B). Thus, the routine use of metal interconnects in Sumi's sensors render obvious claim 1.

Japanese Patent Publication No. JP 2005-353996 A (Shiraiwa, Ex. 1008) in view of Sumi likewise discloses each limitation of claim 1 aside from specifying

the material used for all of the electrical interconnects of the sensor. As with Sumi, POSAs would have routinely implemented Shiraiwa in view of Sumi using industry-standard metal interconnects—rendering claim 1 obvious.

Japanese Patent Publication No. JP 2006-032497 A (Yanagida-1, Ex. 1006) also discloses each limitation of claim 1 aside from specifying the material used for all of the electrical interconnects of the sensor. POSAs would have routinely implemented Yanagida-1's sensor using industry-standard metal interconnects—rendering claim 1 obvious.

The additional limitations in dependent claims 2-4 likewise recite well-known components of CMOS image sensors, and these claims are therefore also unpatentable as obvious.

II. NOTICE OF FEES PAID

Fees are submitted herewith. If any additional fees are due, the undersigned authorizes charge to Deposit Account No. 23/2825.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies that the '143 patent is available for *inter partes* review and that Petitioner is not estopped from requesting such review.

IV. IDENTIFICATION OF CHALLENGED CLAIMS

Petitioners request cancellation of claims 1-4 of the '143 patent.

V. GROUNDS FOR UNPATENTABILITY

The table below identifies the applicable grounds for unpatentability.

Ground Number and Reference(s)		Claims	Basis
1	Obvious over Sumi	1-3	§103
2	Obvious over Sumi in view of Yanagida-2	2, 4	§103
3	Obvious over Shiraiwa in view of Sumi	1-3	§103
4	Obvious over Shiraiwa in view of Sumi and Yanagida-2	2, 4	§103
5	Obvious over Yanagida-1	1-3	§103
6	Obvious over Yanagida-1 in view of Yanagida-2	2, 4	§103

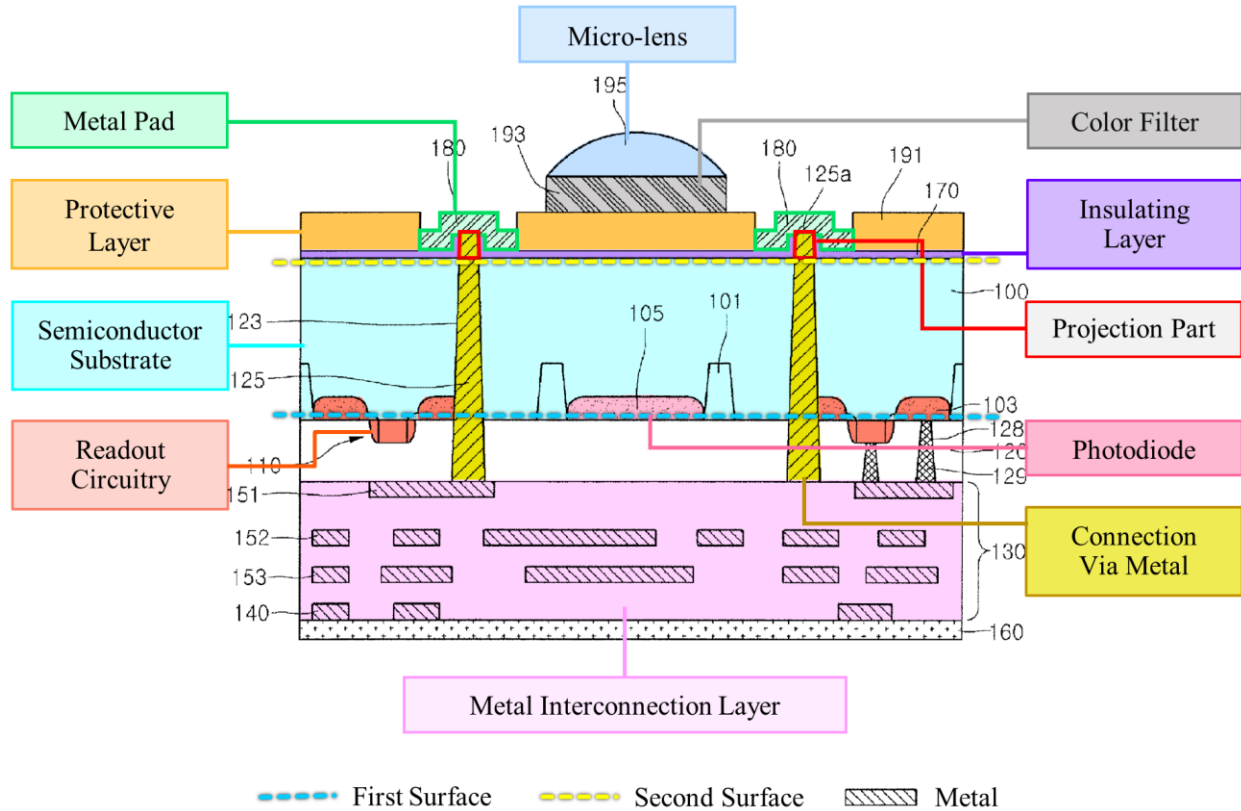
VI. THE '143 PATENT

The '143 patent was filed on November 2, 2009 and claims the benefit of a Korean application filed on November 5, 2008. '143 Patent, 1. Without conceding priority entitlement, the Grounds herein demonstrate why the Challenged Claims were unpatentable as of November 5, 2008.

A. Described Embodiments

The '143 patent discloses a BSI CMOS image sensor. The figure below provides an annotated cross-sectional view. See '143 patent, Fig. 9.¹

¹ Images are annotated throughout unless otherwise noted.



As illustrated, substrate 100 comprises transistors 110 (disclosed as part of readout circuitry) and photodiode area 105. '143 patent, 5:47-54; *see also id.*, 3:18-19, 3:26-31. Metal interconnection layer 130 is formed on one side of the substrate 100 (*id.*, 4:26-31), and connection via metal 125 having a projection part 125a (*id.*, 4:57-60) leads up to insulating layer 170 (*id.*, 5:4-9) and metal pad 180 (*id.*, 5:43-49). The insulating layer 170—specifically, a liner oxide—has a thickness thinner than the height of projection part 125a along the vertical direction. The claimed image sensor further comprises a metal pad formed on the insulating layer such

that the pad covers the projection part. In this embodiment, metal pad 180 is formed on insulating layer 170 and covers projection part 125a.

B. Person of Ordinary Skill in the Art

Persons having ordinary skill in the art (“POSAs”) in the 2008 timeframe would have had at least a Bachelor’s degree in electrical engineering, physics, microelectronics, or material science and approximately 3-5 years of industrial experience or equivalent research or teaching experience, or a Master’s degree in the same fields and 1-3 years of industrial experience or equivalent research or teaching experience in the field of semiconductor image sensor design and fabrication. Guidash, ¶32. The levels of education, experience and knowledge may trade off against one another. *Id.*

C. Prosecution History

The application for the ’143 patent was filed on November 2, 2009. Ex. 1002, 1. The Applicant subsequently filed an Information Disclosure Statement (“IDS”) listing Yanagida-1 and Japanese Patent Application No. JP 2005-150463 A (“Yamamoto”). Aside from the Japanese-language originals, Applicant submitted incomplete English-language abstracts of Yanagida-1 and Yamamoto. *Id.*, 71-119; *see also infra* §XIV.B.

The Examiner never cited these Japanese applications or the incomplete English-language abstracts. Instead, on February 25, 2011, the Examiner rejected

the original independent claims and most of the dependent claims over English-language patent publications not relied upon herein. Ex. 1002, 133-140. Neither the Examiner's rejection nor the Applicant's IDS identified Sumi, Shiraiwa, Yanagida-2 (Ex. 1007).

The Examiner's rejection noted that the English-language publications disclosed all elements of the Challenged Claims aside from originally-filed claim 2's requirement that "the insulating layer has a thickness thinner than a projection height of the projection part." Ex. 1002, 138-139. Applicant subsequently rewrote independent claim 1 with this limitation, and the Examiner allowed the claims without further prior-art rejections. *Id.*, 148-154, 157-162.

However, both Sumi (which was not of record) and Yanagida-1 (which was of record, but never cited) teach this feature (*i.e.*, an insulating layer with a thickness thinner than a projection height of the projection part) despite the Examiner's misunderstanding—based on an incomplete record—that these dimensions created a point of novelty.

VII. CLAIM INTERPRETATION

Claim terms are construed in accordance with the "ordinary and customary meaning" as understood by POSAs and the patent's prosecution history. 37 C.F.R. § 42.100(b). The Board need only interpret terms to the extent necessary to resolve disputes between parties. *Nidec v. Zhongshan*, 868 F.3d 1013, 1017 (Fed. Cir.

2017); *see also* 83 Fed Reg. 51,340, 51,353 (Oct. 11, 2018) (citing *Nidec*).

Petitioner does not believe any term requires construction for purposes herein.²

VIII. GROUND 1: CLAIMS 1-3 WOULD HAVE BEEN OBVIOUS OVER SUMI’S RELATED-ART EMBODIMENT

A. Sumi (Ex. 1005)

Sumi published as U.S. Patent Publication No. US 2006/0094151 A1 on May 4, 2006 and is therefore prior art under pre-AIA 35 U.S.C. §102(b). Sumi, 1.

1. Overview of Sumi

Like the ’143 patent, Sumi describes how FSI sensors suffered from suboptimal efficiency and sensitivity because of “light scattered by [] multi-layered wirings” positioned between optical lenses and the corresponding photodiodes.

Sumi, [0004]; Guidash, ¶¶51-53, 64-68. To address these problems, Sumi describes BSI sensors in which optical components are formed on an opposing side of the semiconductor substrate from the wiring layers—keeping the wiring from blocking light. Sumi, [0004]; Guidash, ¶¶64-68.

Sumi discloses two BSI sensor manufacturing approaches, which differ by the choice of substrate.

First, in the “Description of the Related Art” (“Related-Art Embodiment”), Sumi discloses using a Silicon-On-Insulator (“SOI”) substrate comprising a base

² Petitioner does not waive any arguments necessary for other proceedings.

silicon substrate (e.g., a silicon wafer) with an insulating layer separating the silicon at the bottom of the substrate with a thin top layer of silicon on which the read-out transistors and wiring layers are formed. Sumi, [0009]-[0013]; Guidash, ¶65.

Second, in the “Detailed Description” section (“First Embodiment”), Sumi discloses using just the silicon wafer as the substrate on which the read-out transistors and corresponding wiring layers are formed. *See e.g.*, Sumi, [0063]-[0070]; Guidash, ¶66. Both known approaches had respective advantages and disadvantages. SOI substrates were advantageous because SOI’s insulating layer provided an etch-stop preventing uneven etch-back of the substrate’s rear surface. Sumi, [0009], [0015]-[0017]; Guidash, ¶67; *see also* Shiraiwa, [0006]-[0008].

However, producing SOI substrates requires processing steps on the silicon wafer (or wafers) to interpose the insulating layer with the substrate (*see infra* §X), increasing manufacturing costs relative to the alternative approach of using just the silicon wafer as the substrate. Sumi, [0018], [0064]; Guidash, ¶68.

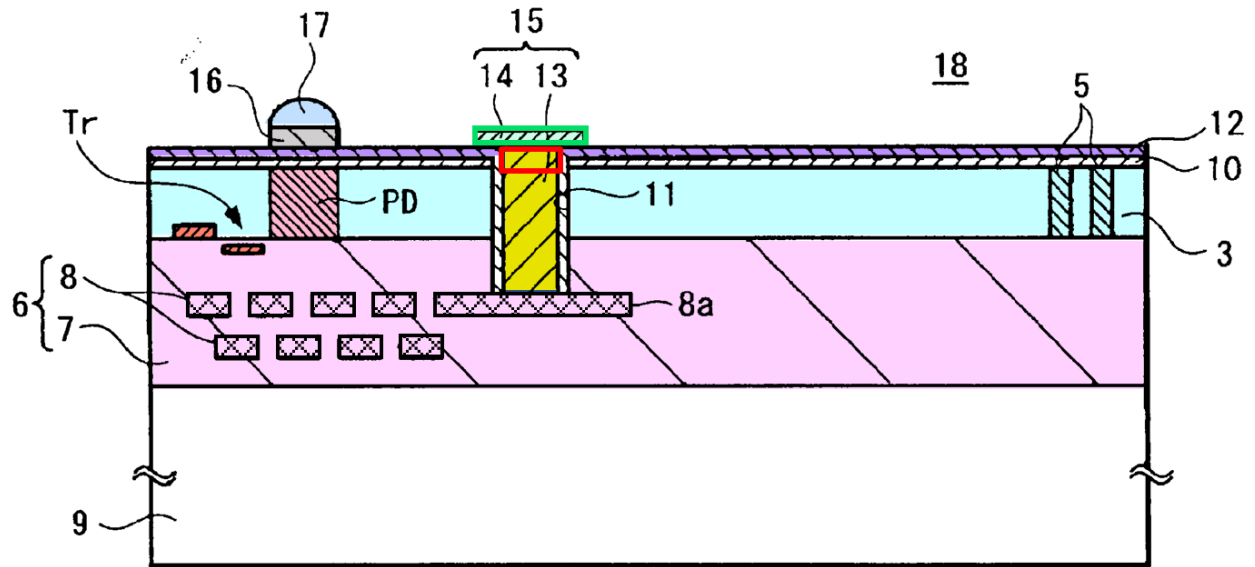
But because the silicon wafer lacks the SOI substrate’s insulating layer, etch stop layer(s) may be formed in the silicon substrate so that rear-side etch-back process thins the silicon substrate to the appropriate (and even) thickness prior to the rear-surface fabrication of the sensor’s optical components. *See e.g.*, Sumi, [0064], [0069]; Guidash, ¶68.

Ground 1 relies on Sumi's Related-Art Embodiment, which discloses the connection via structure electrically connecting the substrate's front and rear surfaces.³

2. The Related-Art Embodiment

The BSI sensor in Sumi's Related-Art Embodiment comprises a "silicon layer 3" on which "MOS transistors [Tr]", corresponding "photodiodes PD" and "multi-layered wiring layer 6" are formed on a "front surface side" of the silicon layer, with "color filter 16" and "on-chip lens 17" formed on a "rear surface" of silicon layer 3—yielding "back-illuminated type [sensor] 18," as illustrated in Sumi's Figure 3B reproduced below with color annotation for elements recited in claim 1. Sumi, [0011]-[0017]; Guidash, ¶69.

³ Sumi's Detailed Description does not detail the electrical connections between the front and backside of the sensor; instead, it focuses on new techniques for providing etch-stop layers.



A “rear surface electrode 15” is provided by depositing “conductive layer 13” inside “opening 11” to connect “wiring layer 8a” on the front surface to forming “electrode pad 14” on the rear surface. Sumi, [0016]; Guidash, ¶70. The region of conductive layer 13 boxed in red shows that a portion of conductive layer 13 projects beyond the rear surface of silicon layer 3 by an amount greater than the thickness of “insulation film 12.” Comparison with Figure 9 of the ’143 patent—reproduced below with the same color coding for the elements of claim 1—shows that Sumi’s sensor 18 includes all of the claimed structural elements illustrated in Figure 9.

“Prentice-Hall” and bearing a 2001 copyright date (Quirk, 1-2)⁴—and Garrou—an excerpt of “Handbook of 3D Integration” published by “Wiley-VCH Verlag GmbH & Co. KGaA” and bearing a 2008 copyright date (Garrou, 1-4). Garrou was publicly available from the British Library at least as early as October 10, 2008 and is therefore pre-AIA §102(b) art, as confirmed by an expert declaration (Ex. 1018, 5) and supporting materials (Exs. 1016-17), including citation in a separate paper published by October 10, 2008 (Ex. 1019).

⁴ The Board has recognized Prentice-Hall as “a well-known publisher.” *Intel v. Qualcomm*, IPR2018-01429, Paper 8, 15 (PTAB Feb. 15, 2019); *Arista Networks v. Cisco Sys.*, IPR2016-00303, Paper 53, 18 (PTAB May 25, 2017) (finding “book published by a well-known publisher, i.e., Prentice Hall” prior art as of copyright date). For such established publishers, “absent some indication that the reference was not publicly available, demonstrating a date of publication is alone sufficient for showing accessibility to the public.” *Microsoft v. IPA Techs.*, IPR2018-00794, Paper 11, 10-11 (PTAB Oct. 15, 2018); *see also Arista* at 21 (“[I]t serves the interest of justice to allow the Petitioners to rely on the copyright date of technical references published by a well-known publisher....”). Quirk therefore constitutes §102(b) prior art.

B. Obviousness of Implementing Sumi's Related-Art Embodiment With Metal Components

Claim 1 recites a “*metal* interconnection layer,” a “connection via *metal*,” and a “*metal* pad.” Sumi's Related-Art Embodiment discloses these same electrical connections (*i.e.*, “multi-layered wiring layer 6,” “conductive layer 13,” and “electrode pad 14,” respectively), but does not specify any particular material for these conductors. Sumi, [0013]-[0016]; Guidash, ¶¶72-73. However, metal (*e.g.*, copper, aluminum, tungsten, etc.) was the industry-standard choice for fabricating each of these interconnect types. Guidash, ¶73 (citing Quirk, 299-308).

1. The Use of Metal Was Well-Known

To the extent any of Sumi's electrical connections theoretically could have been implemented with non-metal materials, metal would at minimum have been an obvious choice for implementing Sumi's connections. For example, Pain-1 discloses a BSI sensor using metal for each of the wiring layers, vertical connection vias, and pads connected to the wiring layers through the vias. *See, e.g.*, Pain-1, [0036] (“metal layers 150 for interconnection of circuits and photo-detectors”), [0048] (“metal pads 525 resid[ing] on the same side of light entrance”), [0077] (“Metal pads 700 [] connected with ILD 610 [metal wiring] by means of interconnect metal 710 [vertical connection via]”), Fig. 10; Hynecek, 4:7-14 (“The align key 112 may be formed of a conductive material, for example, a metal or an alloy.”), 8:53-57 (“The first to fourth interconnection layers 113, 116,

119 and 122 are formed of a conductive material, for example, a metal, or an alloy containing at least two metals. Preferably, the first to fourth interconnection layers 113, 116, 119 and 122 are formed of aluminum (Al).”); Guidash, ¶74.

Thus, it would have been obvious for POSAs to use metal for each of Sumi’s electrical connections discussed above because doing so would have merely involved using a known material (metal) for its intended function (electrical conductance) to yield the predictable result of providing the electrical connections in Sumi’s sensor with metal’s advantageous conductivity properties. *KSR Int’l v. Teleflex*, 550 U.S. 398, 415-421 (2007); Guidash, ¶¶75-77. Additionally, POSAs would have had numerous reasons to choose metal for Sumi’s interconnections.

2. Reasons For Using Metal

The high conductivity, durability and relatively low cost of using metal to implement electrical connections in semiconductor devices, including image sensors, would have made using metal conductors an obvious and desirable choice for implementing all of the disclosed electrical connections of Sumi’s sensor 18 (*i.e.*, wiring layers 8 of multi-layered wiring layer 6, conductive layer 13 and electrode pad 14). Guidash, ¶78; Pain-1 [0077]; Quirk, 300-306; Garrou, 157-173.

Furthermore, processes for metal deposition were well-established and understood, for example, chemical vapor deposition (“CVD”) suitable for low temperature fabrication and for metallizing deep high aspect ratio structures such

as vertical vias. Guidash, ¶79; Pain-1, [0060]; Quirk, 305-306; Garrou, 157-173. POSAs therefore would have had multiple reasons to use metal as the conductive material for multi-layered wiring layer 6, conductive layer 13 and electrode pad 14 of Sumi's Related-Art Embodiment. Guidash, ¶79.

3. Reasonable Expectation of Success

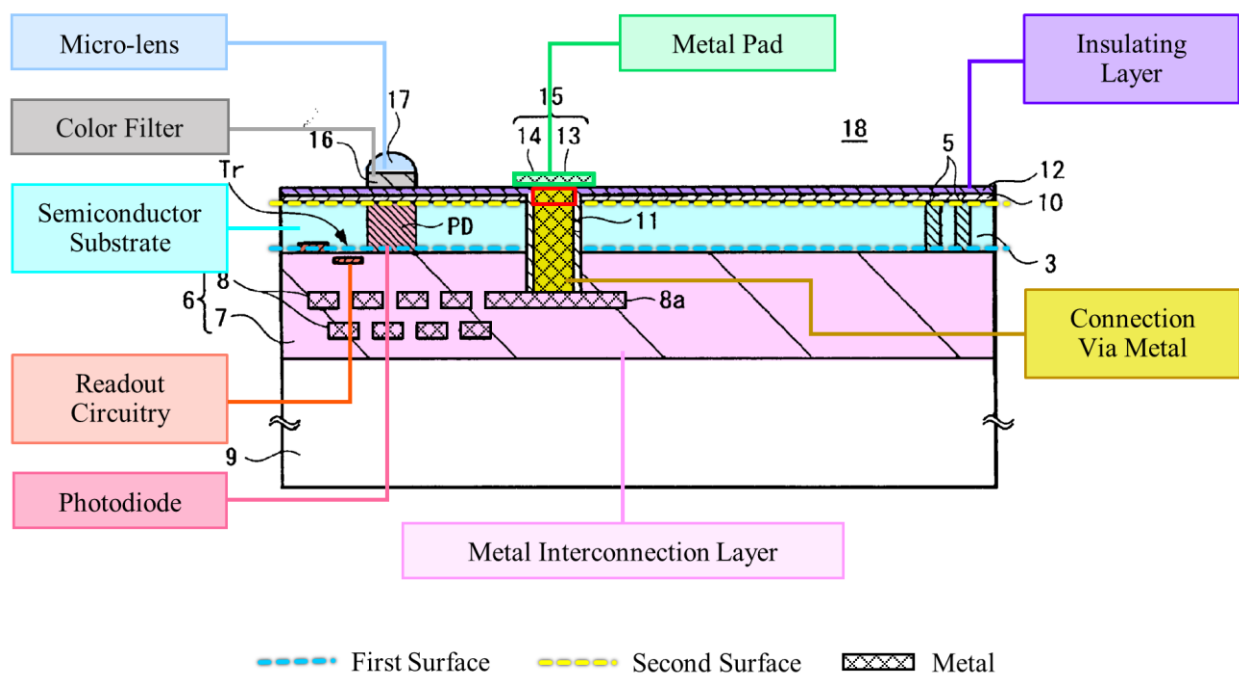
POSAs would have had a reasonable expectation success in using metal for any of the electrical connections in Sumi's Related-Art Embodiment. As discussed above, providing metal conductors for electrical connections in semiconductor devices, including BSI sensors, was well-established and well-understood; POSAs would have had a reasonable expectation in succeeding in implementing the Sumi's Metal-Related-Art Sensor. Indeed, Pain disclosed a BSI sensor in which the equivalent structures were all made of metal—including the metal wiring on a first surface of the semiconductor substrate, the pad formed on a second surface of the substrate, and the vertical via electrically connecting the pad and wiring. Pain-1, [0036], [0048], [0077], Fig. 10; Guidash, ¶80.

Additionally, POSAs understood that metal was compatible with BSI sensor fabrication processes and thus suitable for each of the conductors in Sumi's Related-Art Embodiment given the ability to deposit metal at low temperatures and high aspect ratios (*e.g.*, within deep holes or trenches). Guidash, ¶81; Quirk 271-272. Indeed, metal was the commonly and routinely used material for fabricating

each of Sumi's disclosed interconnect types, and POSAs would have expected success in implementing metal connections in Sumi's sensor 18.

4. Resultant Metal-Related-Art Sensor

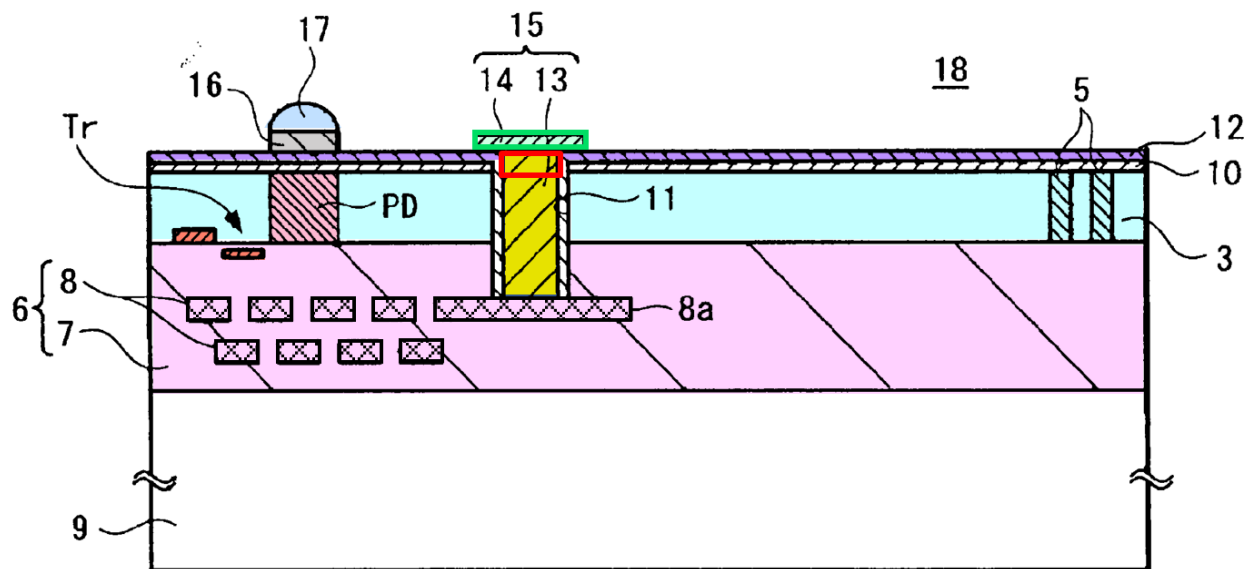
The cross-hatching added to Figure 3B of Sumi below illustrates Sumi's sensor 18 implemented using metal to fabricate multi-layer wiring 8, conductive layer 13 and electrode pad 14. This "Metal-Related-Art Sensor" has the same structure as Sumi's sensor 18 and, as demonstrated in the limitation-by-limitation analysis below, satisfies all limitations of claims 1 and 3. Guidash, ¶¶82-86.



C. Claim 1

1. Preamble – “An image sensor comprising:”

Sumi’s Related-Art Embodiment discloses “a CMOS solid-state *image sensor* of a back-illuminated type”⁵ (Sumi, [0004]-[0005])—satisfying the preamble’s “image sensor” requirement. Guidash, ¶88.

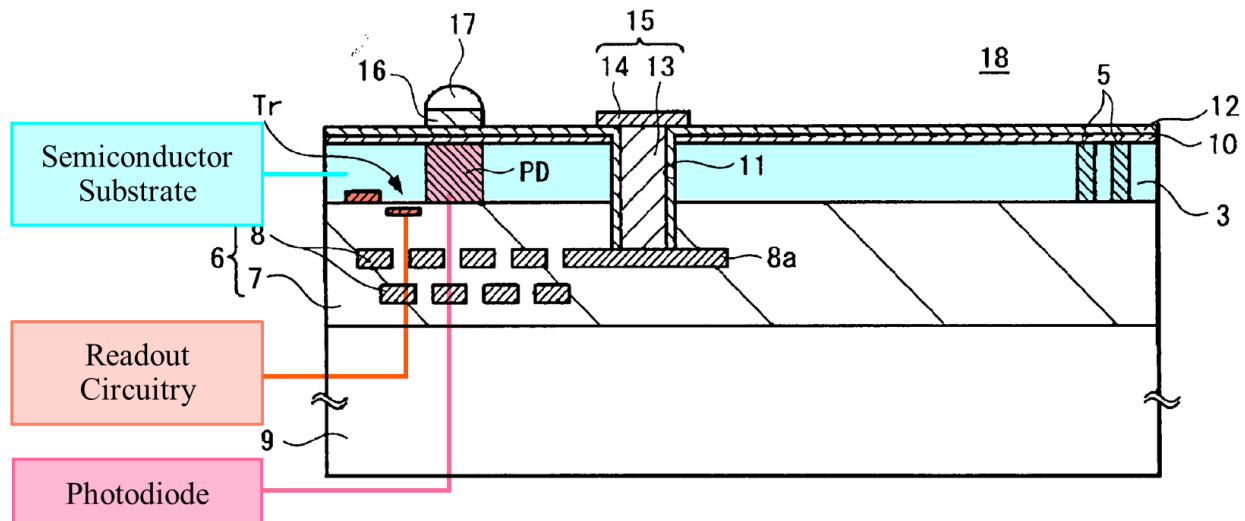


2. **[1A] – “a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;”**

Silicon layer 3 in Sumi's Related-Art Embodiment on which a plurality of MOS transistors Tr and photodiodes PD are formed meets [1A]. Specifically, as illustrated in Sumi's Figure 3B (reproduced below), Sumi's related art embodiment uses "SOI substrate 4" in which "silicon layer 3" forms the top layer providing the substrate on which a "plurality of MOS transistors [Tr]" and "photodiodes PD" are

⁵ Emphasis added unless otherwise noted.

formed on silicon layer 3's "front surface side." Sumi, [0011]-[0012]; Guidash, ¶89.



After multi-layered wiring layer 6 is formed thereon, the bottom two layers of SOI substrate 4 are removed (*see* Sumi, Fig. 2B), exposing silicon layer 3's "rear surface" on which further sensor components (*e.g.*, color filter 16 and lens 17) are formed (*see id.*, Figs. 3A, 3B). *Id.*, [0015]-[0017]; Guidash, ¶100. POSAs would have understood that silicon layer 3 of the SOI substrate, both surfaces of which provide the substrate on which components of the sensor are fabricated, constitutes the claimed "semiconductor substrate." Guidash, ¶100.

As evidence of such understanding, Yanagida-1 discloses a BSI image sensor wherein “MOS type transistors Tr1” and corresponding “photoelectric conversion elements 7” are formed on a first side of the top “silicon layer 4” of a “SOI substrate 30,” and wherein “color filter[s] 11” and “chip lenses 12” are

formed on a second side of silicon layer 4 after removing the bottom two layers of SOI substrate 30. Yanagida-1, [0025]-[0026], [0054]-[0057], [0060]-[0061], [0066]; Guidash, ¶92. Yanagida-1 describes this silicon layer 4 (*i.e.*, the same top silicon layer of a SOI substrate as Sumi’s silicon layer 3) as a “**semiconductor substrate**.” Yanagida-1, [0005], [0007], [0013]-[0019], [0025] (“[P]hotoelectric conversion elements 7...[are] formed in the semiconductor substrate (e.g., single crystal silicon layer) 4.”); Guidash, ¶92.

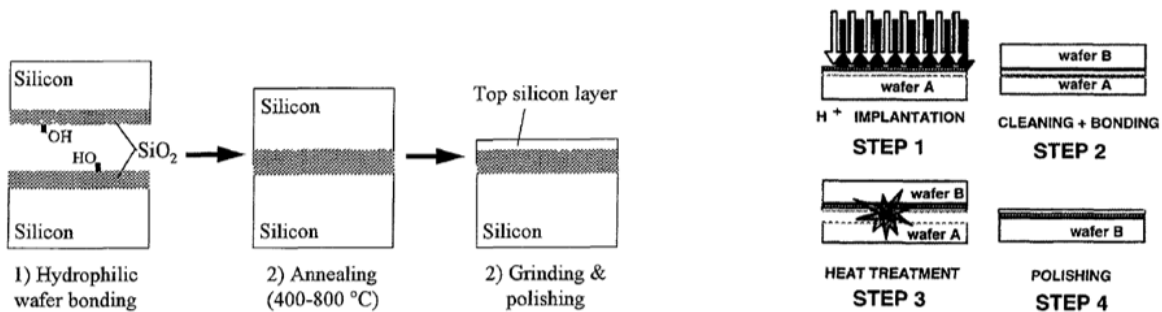
Likewise, Ezaki (Ex. 1023) also describes the top “silicon layer 1” of “SOI substrate 23” as a “**semiconductor substrate** 1” on which “readout circuits” and “photoelectric conversion elements are respectively formed on one surface of the single-crystal silicon layer 1” and “on-chip lenses...are formed on the other surface of the silicon layer 1.” Ezaki, [0047], [0085]-[0088], [0098], [0106]; *see also* Yanagida-2, [0029], [0047]; Guidash, ¶93.

Such usage in the art (*i.e.*, describing as a “semiconductive substrate” the top layer of a SOI substrate in which the bottom two layers are removed) confirms that POSAs understood silicon layer 3 in Sumi’s Related-Art Embodiment as a “semiconductor substrate” as claimed. Guidash, ¶94.

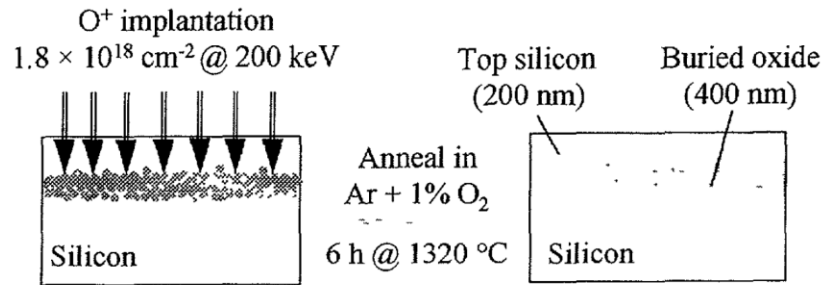
Moreover, the ’143 patent states that a “semiconductor substrate may include a wafer having a single crystalline structure, or a silicon substrate in which an epitaxial layer is formed on a wafer.” ’143 patent, 3:13-15. Depending on the

technique used to manufacture the SOI substrate, the top silicon layer is either a single-crystalline silicon wafer, or a thin silicon layer deposited on such a wafer. Guidash, ¶95. Specifically, SOI substrates were manufactured in one of two ways: 1) a bond and etch-back SOI (“BESOI”) process; and 2) separation by implantation of oxygen (“SIMOX”) process. Guidash, ¶95; Leray (Ex.1013), 1631-1637.

The BESOI process involves bonding together two silicon wafers, one or both of which have an oxide layer formed thereon, and etching-back one of the wafers to a desired thickness for the top silicon layer, as illustrated in Leray’s Figures 11 (left) and 12 (right) below. Guidash, ¶96; Leray, 1635-1637.



SIMOX involves implanting oxygen ions in a silicon wafer at a desired depth, then annealing to form a buried oxide (“BOX”) layer having a thin layer of the silicon wafer above the BOX layer and a thicker base below it. See Leray, Fig. 6 below.



In both processes, the top silicon layer of a SOI substrate is formed by a silicon wafer, which the '143 patent describes as a semiconductor substrate. Depending on the desired application for the SOI substrate, a thin silicon film may be deposited using the top portion of the silicon wafer as a seed, but this too is a semiconductor substrate as understood by POSAs and confirmed by the '143 patent. '143 patent, 3:13-15 (“a semiconductor substrate may include a wafer...or *a silicon substrate in which an epitaxial layer is formed on a wafer*”). Thus, POSAs understood Sumi’s silicon layer 3 is a semiconductor substrate. Guidash, ¶98.

Additionally, POSA’s understood that the “**plurality of MOS transistors** [Tr] of a HAD (Hole Accumulation Diode) structure which **constitute a pixel** with the photodiodes PD” meets the claimed “readout circuitry.” Guidash, ¶101; Sumi, [0012], Figs. 1-3 (illustrating MOS transistors with label Tr). That is, these transistors “constitute a pixel with the photodiodes” because the transistors read out the charge accumulated in the corresponding photodiode. Guidash, ¶101.

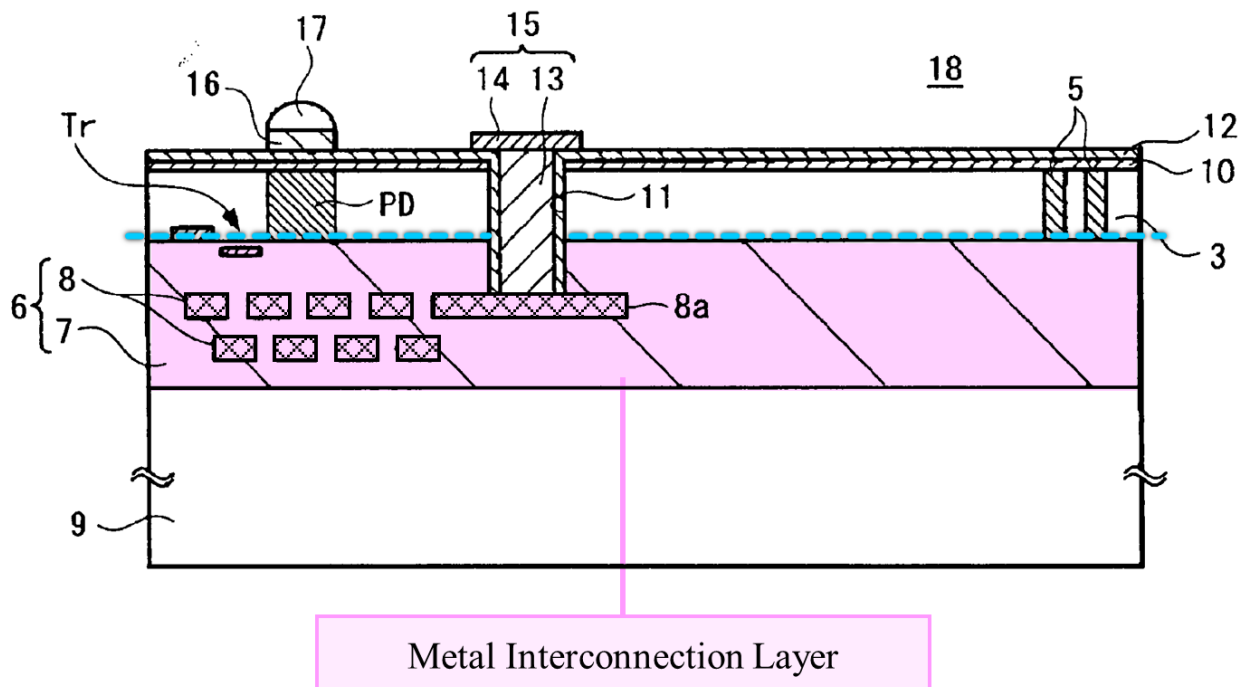
Sumi's Related-Art Embodiment does not detail the operation of these MOS transistors Tr, but it was well-known that such transistors provided readout circuitry for the sensor, as discussed in Sumi's First Embodiment disclosing that the "plurality of MOS transistors Tr that read out signal electric-charge from a photodiode" and comprise "an electric-charge readout transistor, a reset transistor, an amplifier transistor and a vertical selection transistor." Sumi, [0065]-[0066]; Guidash, ¶102.

Thus, POSA's understood that the plurality of MOS transistors in Sumi's Related-Art Embodiment provide "readout circuitry" for the corresponding photodiode (which has a "photodiode area" where the photo diode is formed), like these transistors do in Sumi's First Embodiment and which is the very purpose of these transistors in CMOS imaging sensors. Sumi, [0065]-[0066]; Ezaki, [0047]-[0050]; Guidash, ¶103.

As discussed above, implementing the Related-Art Embodiment using metal interconnects (*i.e.*, the Metal-Related-Art Sensor) does not alter the structure of the Related-Art Embodiment and, therefore, Sumi's silicon layer 3 ("semiconductor substrate") having a plurality of MOS transistors Tr ("readout circuitry") and corresponding photodiodes PD (formed in a "photodiode area") on a front surface side ("first surface") of silicon layer 3 in the Metal-Related-Art Sensor meets [1A]. Guidash, ¶104.

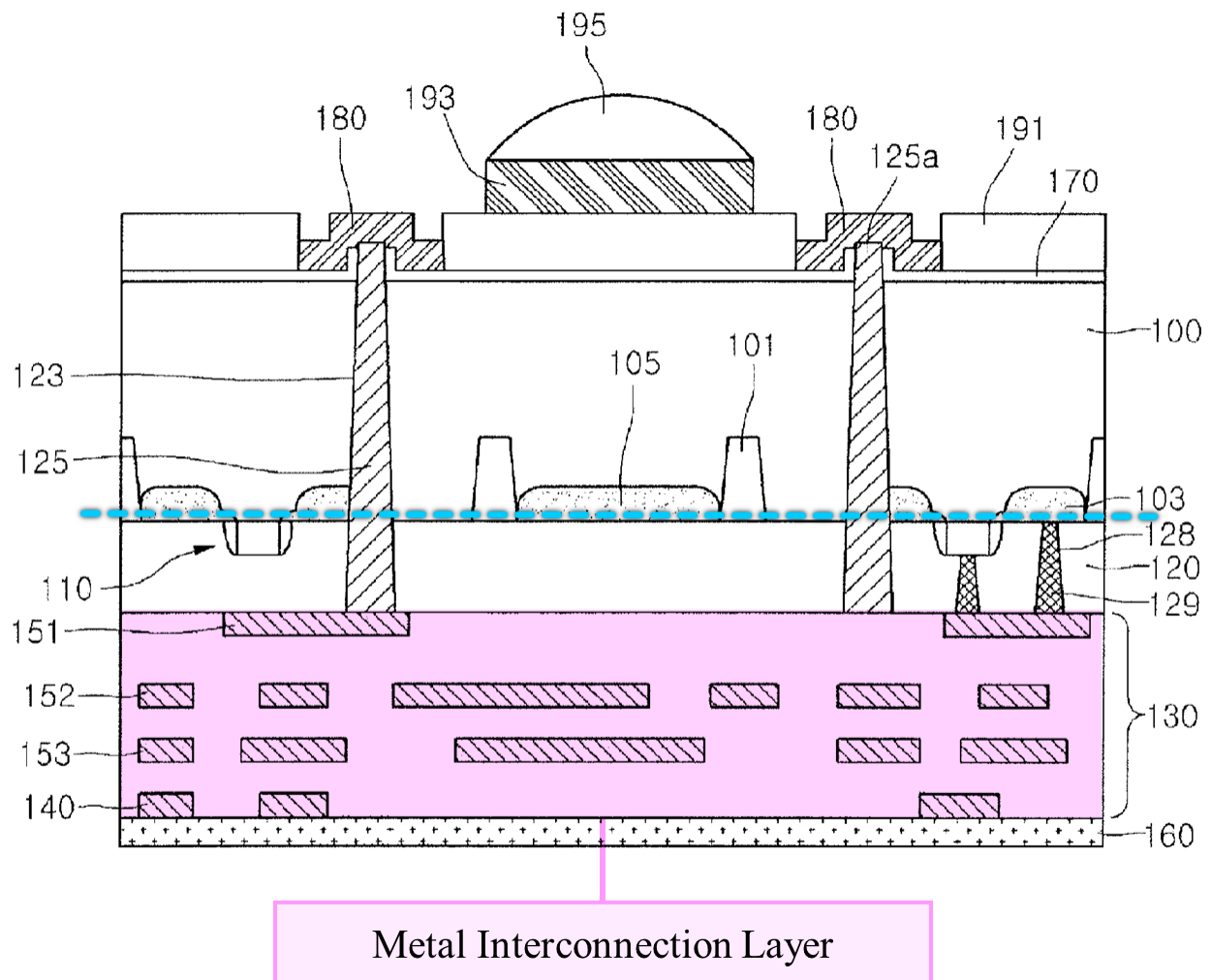
3. [1B] – “a metal interconnection layer formed on the first surface;”

Using metal for “multi-layer wiring 8” of “multi-layered wiring layer 6” in Sumi’s Metal-Related-Art Sensor meets [1B]. Guidash, ¶105. As illustrated in Sumi’s Figure 3B below, a “multi-layered wiring layer 6” comprising “multi-layer wiring 8” with an “interlayer insulation layer 7” therebetween formed on the front surface side (*i.e.*, the claimed “first surface”) of silicon layer 3. Sumi, [0013]; Guidash, ¶105.



The '143 patent describes and illustrates this same multilayer structure as a “metal interconnection layer,” as illustrated in Figure 9 reproduced below. The '143 patent states that “metal interconnection layer 130 can include a stacked

structure of second and third metal interconnections 152 and 153 and a plurality of interlayer dielectric layers.” ’143 patent, 4:28-31.



Thus, Sumi’s multi-layered wiring layer 6 comprising multiple stacked wiring layers 8 with insulation layer 7 in between is a “interconnection layer” as recited in [1B] for the same reason. Guidash, ¶107. Sumi does not explicitly state that wiring 8 is made of metal, but, as discussed *supra* §VIII.B, implementing multi-layer wiring 8 using metal would have been obvious and desirable given

metal's high conductivity, durability, low cost, and ease of deposition. Metal additionally provides good adherence to silicon and silicon dioxide—an additional reason to implement wiring 8 using metal. Guidash, ¶107. Thus, wiring 8 made of metal in the Metal-Related-Art Sensor meets the claimed “metal interconnection layer.”

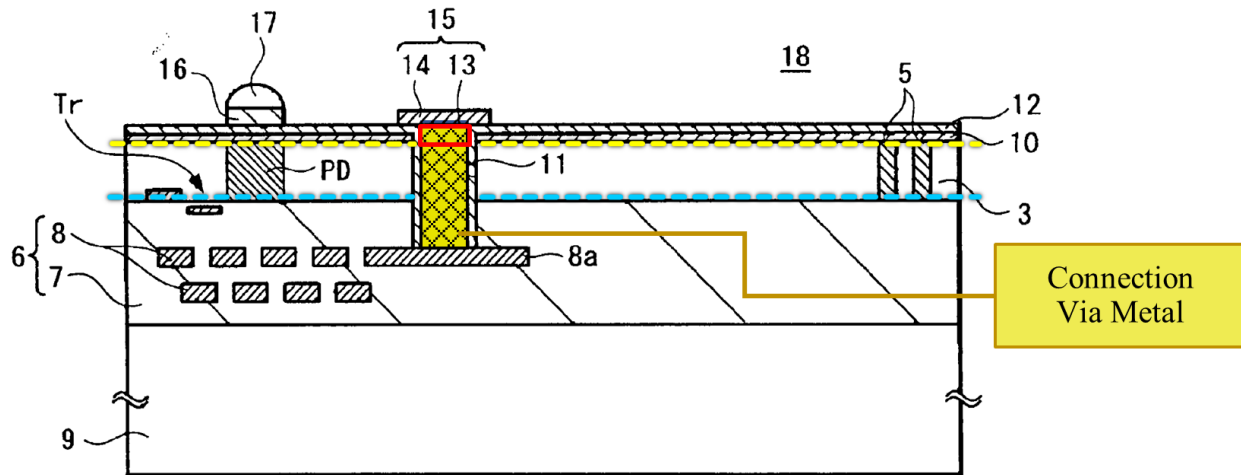
Sumi discloses that the multi-layered wiring layer 6 is “laminated thereon”—*i.e.*, formed on the “front surface side” of silicon layer 3. Sumi, [0012]-[0013]. To the extent there are intervening layers between multi-layered wiring layer 6 and silicon layer 3, multi-layered wiring layer 6 is still “formed on” the front surface side (*i.e.*, the claimed “first surface”) of silicon layer 3 because the '143 patent states that when a layer is formed “on” another layer “intervening layers may also be present.” '143 patent, 3:1-4.

Thus, multi-layered wiring layer 6 of the Metal-Related-Art Sensor meets [1B].

4. **[1C] – “a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface;”**

The “conductive layer 13” of the Metal-Related-Art Sensor meets [1C]. Sumi states that “an opening 11 that reaches a wiring layer 8a is formed” and a “conductive layer 13 that connects to the wiring layer 8a inside the opening 11 is formed and an electrode pad 14 that connects to the conductive layer 13 and faces

to the rear surface is formed,” as illustrated in Figure 3B of Sumi reproduced below. Sumi, [0016]; Guidash, ¶111.



Sumi describes the structure comprising electrode pad 14 connected to wiring layer 8a via conductive layer 13 as a “rear surface electrode 15.” Sumi, [0016]. Conductive layer 13 is a “connection via” because it forms an electrical pathway from one metal layer to another by way of an opening (“opening 11”) formed through one or more intervening layers, just like the ’143 patent’s connection via metal 125 through connection via 123. *Compare* Sumi, [0016] with ’143 patent, 3:41-55; Guidash, ¶112 (citing Quirk, 300).

Indeed, Sumi’s “rear surface electrode 15” forms the same structure as the ’143 patent’s pad 180, connection metal via 125 and metal interconnection 151 (see, e.g., ’143 patent, Fig. 8) and performs the same function—*i.e.*, connecting the pad on the second surface of the semiconductor substrate with the wiring layers on the first surface. Sumi, [0016]; ’143 patent, 3:41-55, 5:39-42; Guidash, ¶113.

As discussed *supra* §VIII.B, Sumi’s Metal-Related-Art Sensor uses metal for conductive layer 13 as was commonplace when forming connection vias—including through-silicon vias connecting the front and backside electrical circuitry in imaging sensors. Pain-1, [0077], Fig. 10; Guidash, ¶114.

Thus, conductive layer 13 provided in opening 11 extends from wiring layer 8a formed on the first surface (*i.e.*, “front surface side” of silicon layer 3) to a second surface (*i.e.*, “rear surface of silicon layer 3”), and therefore metal conductive layer 13 of the Metal-Related-Art Sensor meets “a connection via metal extending from the first surface to a second surface of the semiconductor substrate,” as recited in [1C]. Sumi, [0012]-[0016]; Guidash, ¶115.

As illustrated above, conductive layer 13 (yellow) includes a portion (boxed in red) projecting from the second surface. Specifically, silicon nitride film 10 is provided on silicon layer 3’s rear surface, and opening 11 is formed through the silicon nitride film 10 and silicon layer 3. Sumi, [0016]. Subsequently, insulation film 12 is formed, covering nitride film 10 and the inside wall of opening 11. *Id.* Thus, when conductive layer 13 is thereafter deposited, the portion of conductive layer 13 boxed in red above extends above silicon layer 3 to form “a projection part projecting from the second surface” as claimed. *Id.*; Guidash, ¶116.

Thus, the metal conductive layer 13 of the Metal-Related-Art Sensor meets [1C]. Guidash, ¶117.

5. [1D] – “an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and”

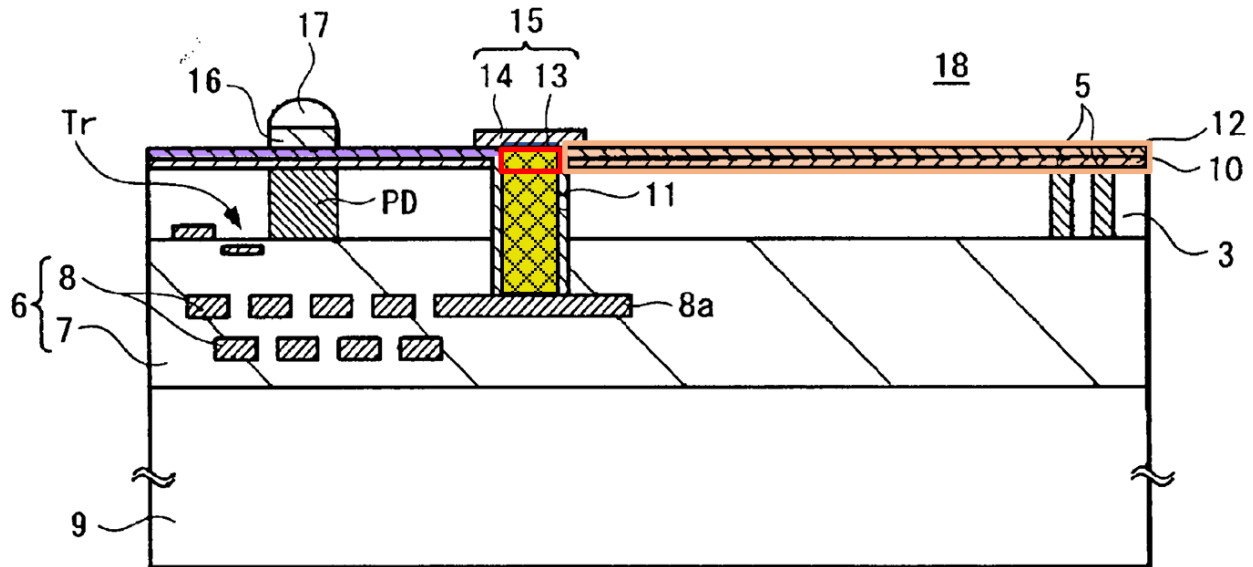
“Insulation film 12” in Sumi’s Related-Art Embodiment meets [1D]. Sumi discloses that “insulation film 12...is formed from the inside wall of the opening 11 to cover the surface of the silicon nitride film 10,” which film 10 is “formed on the rear surface of the silicon layer 3.” Sumi, [0016]. Thus, insulation film 12 is “formed on the second surface of the semiconductor substrate” as claimed because the ’143 patent defines “on” as meaning “directly on” or where “intervening layers may also be present.” ’143 patent, 3:1-4; Guidash, ¶119.

Conductive layer 13 is then formed inside opening 11 on insulation film 12 to expose the top surface of conductive layer 13, while the lateral sides of conductive layer 13 extending beyond silicon layer 3—*i.e.*, the “projection part”—are surrounded by insulation film 12, as illustrated below. Sumi, [0016]. Thus, insulation film 12 (purple) surrounding the lateral sides of the projection part (red) of conductive layer 13 and leaving exposed the top of the portion of the projection part meets [1D]; Guidash, ¶120.

silicon layer 3 by forming an electrode pad 14 on insulation film 12 over the exposed portion of conductive layer 13 such that electrode pad 14 “connects to the conductive layer 13” to provide the electrical connection to wiring layer 8a, as illustrated in Sumi’s Figure 3B reproduced below. Guidash, ¶127.

As discussed *supra* §VIII.B, the Metal-Related-Art Sensor uses metal to form electrode pad 14 as was commonly done to provide a highly conductive, durable pad formed using well-established processes (*e.g.*, CVD) compatible with BSI fabrication. Guidash, ¶123. Thus, Metal-Related-Art Sensor's metal electrode pad 14 formed on insulating film 12 and covering the exposed portion of conductive layer 13 extending above silicon layer 3 meets [1E].

Sumi's insulation film 12 meets [1F] because this layer is thinner than the projection part of conductive layer 13, as illustrated in the enlarged portion of Sumi's Figure 3B reproduced below. Guidash, ¶124.



Because the projection part of conductive layer 13 (highlighted red) extends beyond the rear surface of silicon layer 3 by an amount at least the sum of the thicknesses of insulation film 12 and silicon nitride film 10 (together highlighted orange), the thickness of insulation film 12 (highlighted purple) is thinner than the projection part by at least the thickness of silicon nitride film 10. Guidash, ¶125. Using metal for electrical interconnects would not change this relationship, and the Metal-Related-Art Sensor's insulation film 12 therefore meets [1F]. Guidash, ¶125.

D. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”

Sumi discloses that “insulation film 12” may be a “silicon oxide film” but does not expressly describe it as a TEOS layer. However, TEOS was a well-known silicon oxide insulating material used in semiconductor fabrication, including BSI sensors. Guidash, ¶¶126-129 (citing Pain-2 (Ex. 1012), [0074]; Quirk, 271-272; Hynecek, 6:33-46; Yanagida-2, [0037], [0040], [0042]-[0043], [0047], [0054], [0061]).

For example, Pain-2 discloses a BSI sensor incorporating TEOS for a variety of layers, including sidewall insulation films on the inner walls of through-holes. Pain-2, [0074]. Similarly, Yanagida-2 discloses a BSI sensor incorporating TEOS for an insulation (Yanagida-2, [0051]-[0054]) and in conjunction with a nitride film underneath the sensor lenses to provide an anti-reflective layer (*id.*, [0043] (demonstrating the suitability of TEOS for Sumi’s insulation film 12)). Guidash, ¶129.

Accordingly, it would have been obvious to implement insulation film 12 as a TEOS layer at least because doing so is merely the use of a known material (TEOS) for its intended function (insulating) to yield the predictable result of providing the insulation film 12 in Sumi’s sensor 18. *KSR*, 550 U.S. at 415-421. Furthermore, TEOS was known to facilitate low-temperature fabrication, and POSAs would have been motivated to use TEOS for insulation film 12 to avoid

Related-Art Embodiment renders claim 3 obvious for the same reasons it renders claim 1 obvious.

IX. GROUND 2: CLAIMS 2 AND 4 WOULD HAVE BEEN OBVIOUS OVER SUMI'S RELATED-ART EMBODIMENT IN VIEW OF YANAGIDA-2

Yanagida-2 (discussed below) discloses a light-shielding layer that POSAs would have recognized as desirable to incorporate into Sumi's Metal-Related-Art Sensor. Guidash, ¶¶136-137.

Early BSI sensors suffered from image degradation problems because light incident on the active regions of transistors formed in the substrate (read out transistors in particular) could produce a current in regions of the transistors—causing the transistors to produce a read-out signal (*e.g.*, a voltage or current) having a component not corresponding to the charge accumulation measured in the corresponding photodiode. In addition, light incident on the border regions of a pixel with a color filter of one color produced charge that could be collected by adjacent pixels having color filters of different colors. This effect caused color mixing and degraded the color accuracy and signal-to-noise ratios of the captured images. Guidash, ¶133.

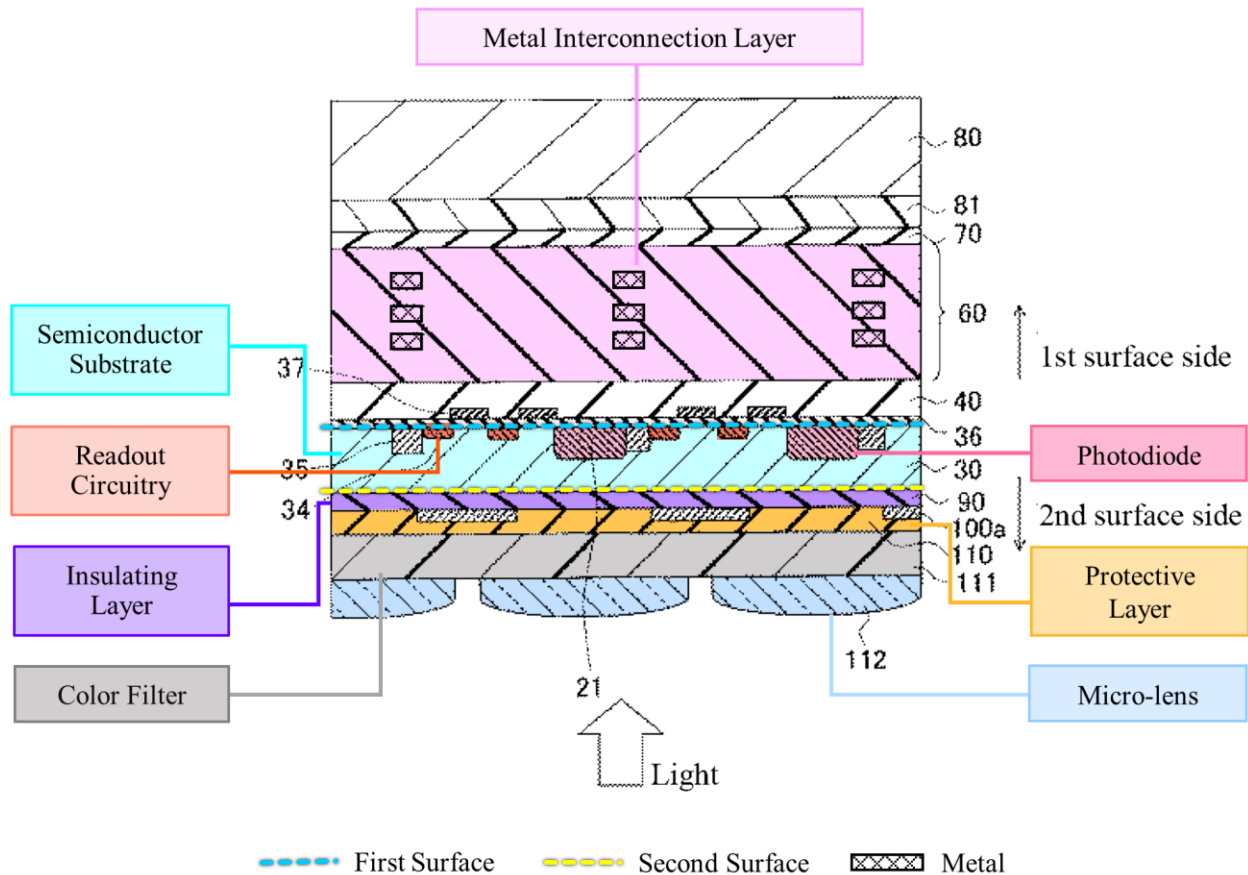
A known solution to this problem was to form and pattern a light-shielding layer (as disclosed in Yanagida-2) to block light from penetrating into the substrate in areas other than the intended photoactive regions. Guidash, ¶134.

A light-shielding layer also prevented light from adjacent pixel regions from reaching the photodiode and allowed reference transistors to be provided to measure “dark current” in the substrate that could be subtracted from the read-out signals to remove this additional source of noise. Guidash, ¶135; Yanagida-1, [0024].

A. Yanagida-2 (Ex. 1007)

Yanagida-2 published as Japanese Publication No. JP 2006-339566 A on December 14, 2006 and is therefore pre-AIA §102(b) prior art. Yanagida-2, 1. Yanagida-2 was published in Japanese (Ex. 1021) and a certified English translation is provided herein (Yanagida-2, 2-16).

Like Sumi, Yanagida-2 describes a backside-illuminated CMOS image sensor in which photodiodes 21, corresponding transistor 22-25 and wiring layer 60 are formed on a first side of a silicon substrate 30 (*Id.*, [0029]-[0033]) and a color filter 111 and on-chip lens 112 are formed on a second side of the silicon substrate 30 (Yanagida-2, [0034]-[0035]), as illustrated in Yanagida-2’s Figure 3—reproduced below. Guidash, ¶136.



Also, like Sumi, Yanagida-2 discloses providing a silicon nitride film and an insulating film (“TEOS film”) on the silicon substrate, which Yanagida-2 references as anti-reflective layer 90 illustrated in the drawing above. Yanagida-2, [0034], [0043]. A light shielding film 100a is formed on anti-reflective layer 90 and patterned to provide openings over each photodiode 21, and a protective film 110 is formed to cover the light shielding film 100a before forming color filter 111 and on-chip lens 112. Yanagida-2, [0034]; Guidash, ¶137.

B. Combination of Sumi's Related Art Embodiment and Yanagida-2

Although Sumi's description of related art does not discuss light shielding, POSAs would have understood that without light shielding, light would interact with the transistors—thereby corrupting read-out signals (*i.e.*, by introducing components not corresponding to light detected by the photodiode) and produce color mixing, thus degrading color accuracy and signal-to-noise ratios of captured images. Guidash, ¶138.

Thus, it would have been obvious and desirable to include Yanagida-2's light shielding layer and protective covering over the light shielding layer (*i.e.*, “protective film 110 [] formed to cover the light shielding film 100a,” (Yanagida-2, [0034]) to shield the underlying transistors to prevent signal contribution from sources other than charge accumulation in the photodiode.

Additionally, Sumi discloses a silicon oxide film 12 that covers a silicon nitride film 10—a dual-film layer known to provide passivation and anti-reflection for the sensor. Sumi, [0016]; *see also* Shiraiwa, [0027] (disclosing “passivation film (also serving as an anti-reflection film) 38 composed of a silicon nitride film 36 and a silicon oxide film 37”), [0039]; Yanagida-2, [0043]; Guidash, ¶140.

Yanagida-2 discloses that the silicon oxide film of anti-reflective layer 90 of this same dual-film structure is a TEOS layer—a well-known silicon oxide Yanagida-2

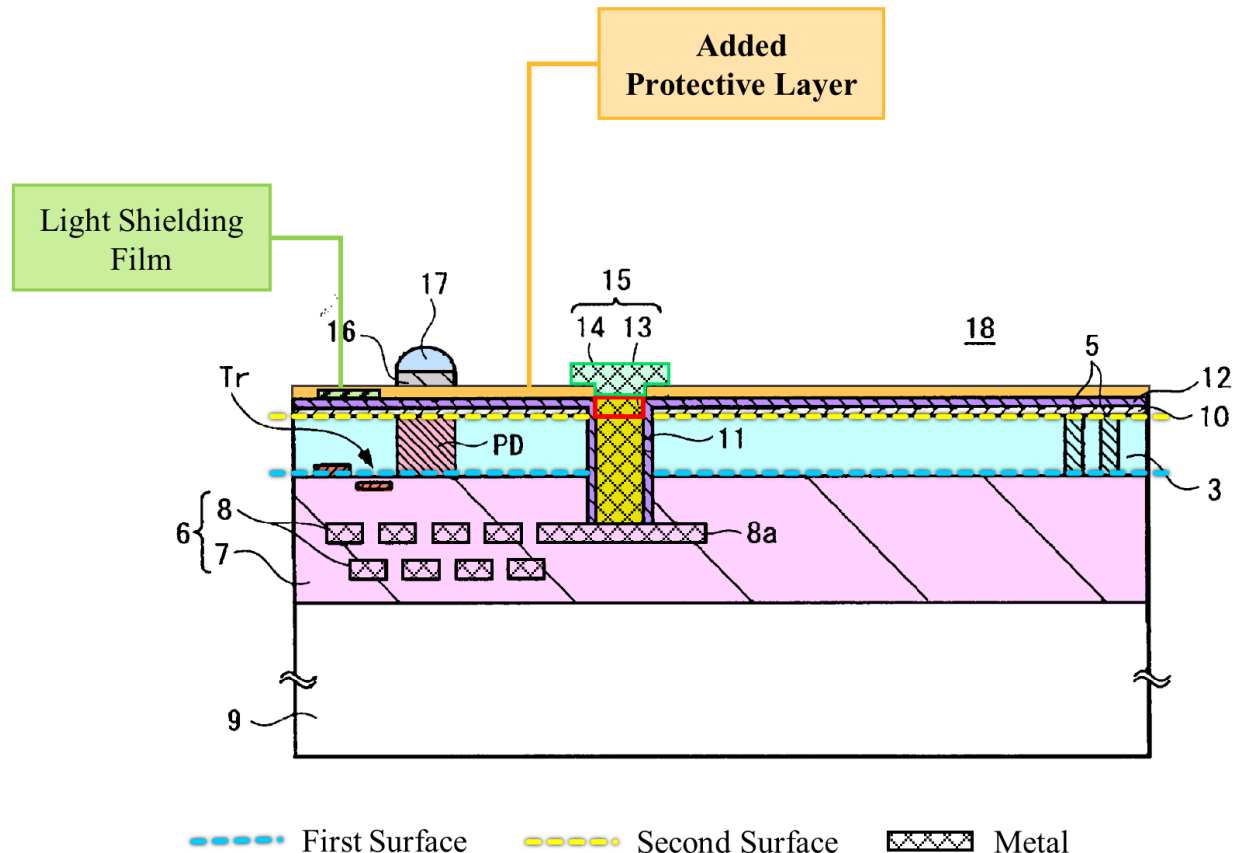
uses for various insulating layers, including to cover the sidewalls of through-holes. Yanagida-2, [0050]-[0051]; Guidash, ¶140.

Thus, it would have been obvious to use a TEOS layer for Sumi's silicon oxide film 12 at least because, as Yanagida-2 confirms, TEOS was a known silicon oxide material suitable for both ways Sumi uses silicon oxide film 12 (*i.e.*, as an insulating film for the sidewalls of through-holes and as part of a dual-film stack with a silicon nitride film). Sumi, [0016]; Guidash, ¶141. In addition, POSAs would have recognized the desirability of implementing silicon oxide film 12 as a TEOS layer given that TEOS can be applied at low temperatures, avoiding high-temperature deposition and the associated risks for previously formed BSI structures. Guidash, ¶141; Quirk, 271-272.

POSAs would have recognized a very straightforward way to provide Sumi's electrode pad 14 when using Yanagida-2's light shielding layer and corresponding protective layer to cover it. Guidash, ¶142. One obvious implementation would have been to form Yanagida-2's light shielding film 100a on Sumi's insulating film 12 (implemented as a TEOS layer on silicon nitride film 10), pattern the light shielding film 100a to provide openings for corresponding diodes, and deposit protective film 110 "to cover the light shielding film 100a"—*i.e.*, the same order disclosed in Yanagida-2 ([0034]). Guidash, ¶142.

This would be followed by pattern and etching of the protective layer to provide an opening over the connection via. Next, deposition, patterning and etching of electrode pad 14 is performed in the same manner as disclosed by Sumi. Guidash, ¶143. Color filter 16 and on-chip lens 17 are then formed on protective layer 110. For example, electrode pad layer 14 could be selectively patterned and etched using a photoresist layer. POSAs would have also understood that there were multiple other ways to implement Yanagida-2’s light shielding layer and protective covering in Sumi’s sensor. Guidash, ¶144.

Regardless of the exact method, the end result would be the “Metal-Sumi-Yanagida-2 Sensor” illustrated below. Guidash, ¶144.



This design blocks light from interacting with Sumi’s read out transistors, and prevents color mixing—improving image quality by preventing corruption of the read-out signals and preventing the light incident on one pixel from being collected by the photodiodes of adjacent pixels. Guidash, ¶145. In addition, the light shielding layer would allow reference transistors to be formed in the substrate to measure “dark current” in the substrate—allowing this additional noise to be subtracted from the read-out signals. Yanagida-1, [0024]; Guidash, ¶145. POSAs would also understand that Sumi’s Metal-Related-Art Sensor provides a small level difference at the backside surface of only the thickness of the pad 14, which according to Yanagida-2 can prevent uneven application of color filter and lens materials. Yanagida-2, [0067]-[0068].

POSAs would have had reasonable expectation of success in fabricating the Metal-Sumi-Yanagida-2 Sensor because the same steps used to form Yanagida-2’s light shielding layer and protective film on Yanagida’s anti-reflection film 90 (*i.e.*, a dual-film nitride-oxide (TEOS) layer) could have been used to form these same layers on Sumi’s dual film nitride-oxide layer (*i.e.*, silicon nitride film 10 and silicon oxide film 12). Guidash, ¶146.

Additionally, metal electrode pad 14 could be formed using any well-known and well-established semiconductor fabrication technique, such as by etching an opening in the protective film to expose a top surface of the projection part, and

depositing metal to form the metal electrode pad 14 similar to formation of pad 100 in Yanagida-2. See Guidash, ¶146.

C. Claims 1 and 3

The combination of Sumi and Yanagida-2 (and in particular Metal-Sumi-Yanagida-2 Sensor) satisfies claims 1 and 3 for the same reasons as Sumi's Related-Art Embodiment alone discussed *supra* §§VIII.C, VIII.E.

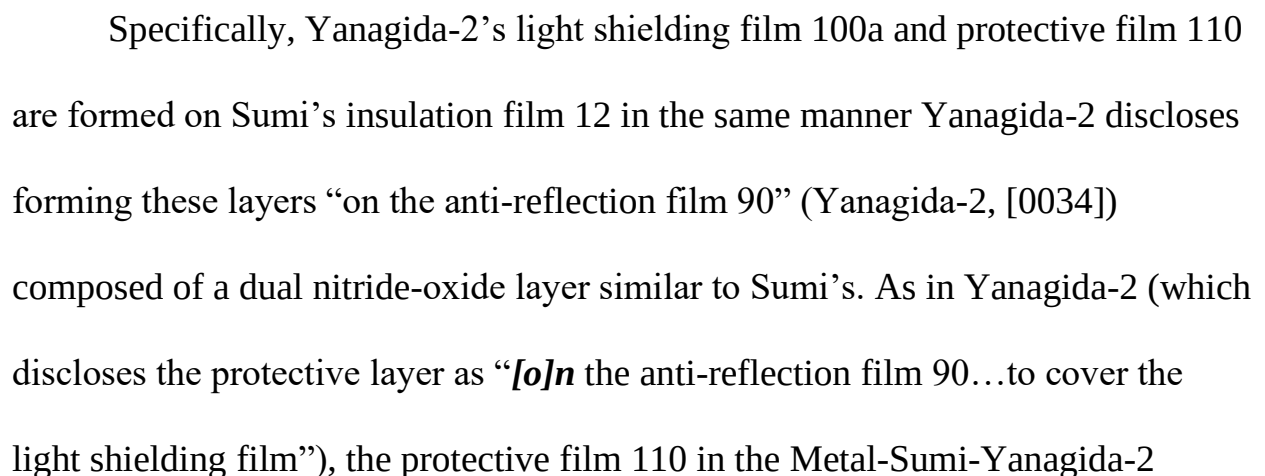
D. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”

As discussed *supra* §VIII.D, it would have been obvious to fabricate Sumi's Metal-Related-Art Sensor using TEOS for insulating film 12 as disclosed in Yanagida-2. In addition to TEOS being a common selection for oxide layers, TEOS would have been particularly desirable given good step coverage for deposition on the sidewalls of opening 11 and low-temperature deposition for rear surface fabrication of a BSI sensor. Guidash, ¶154. Accordingly, insulating film 12 implemented as a TEOS layer in the Metal-Sumi-Yanagida-2 Sensor meets the limitations of claim 2.

E. Claim 4 – [4A] “further comprising: a protective layer formed over the insulating layer; [4B] and a micro-lens formed on the protective layer in a region corresponding to the photodiode area.”

As discussed in §IX.B, the Metal-Sumi-Yanagida-2 Sensor implements Yanagida-2's light shielding film 100a and protective film 110 by forming these layers on Sumi's insulation film 12 (implemented as a TEOS layer as disclosed in

Guidash, ¶¶155-157. As illustrated below, the Metal-Sumi-Yanagida-2 Sensor meets each limitation in claim 4.



Sensor is formed on insulation film 12. '143 patent, 3:1-4 (defining “over” another layer to mean directly over or with intervening layers); Guidash, ¶156.

Likewise, with the introduction of the light shielding layer and the protective film to cover it in the Metal-Sumi-Yanagida-2 Sensor, on-chip lens 17 is positioned on the protective film 110 with intervening color filter 16 in a region corresponding to the photodiode area (*i.e.*, over the region of the substrate in which photodiode PD is formed), thereby meeting [4B]. Guidash, ¶¶158-161.

X. GROUND 3: CLAIMS 1-3 WOULD HAVE BEEN OBVIOUS OVER SHIRAIWA IN VIEW OF SUMI’S RELATED-ART EMBODIMENT

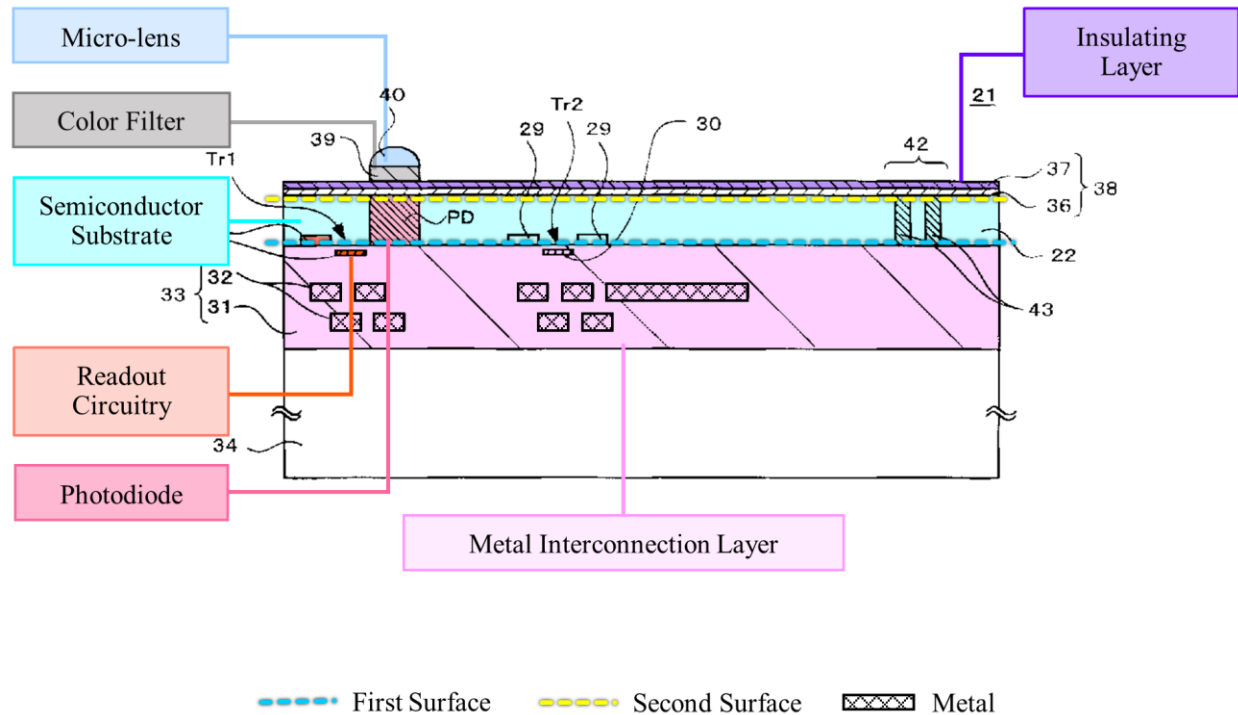
A. Shiraiwa (Ex. 1008)

Shiraiwa published as Japanese Publication No. JP 2005-353996 A on December 22, 2005 and is therefore pre-AIA §102(b) prior art. Shiraiwa, 2. Shiraiwa was published in Japanese (Ex. 1022) and a certified English translation is provided (Shiraiwa, 2-13).

1. Overview of Shiraiwa

Like Sumi, Shiraiwa discloses sensors manufactured from either a SOI substrate (Shiraiwa, [0007]-[0012]) or a silicon wafer (“a normal silicon substrate”) (*id.*, [0012], [0026]-[0044]). Concerning the latter, Shiraiwa discloses a BSI sensor in which read-out transistors Tr1 for “reading signal charges of the photodiode PD” and a multilayer wiring layer 33 are formed on a “front surface

side” of a thinned semiconductor substrate 22, as illustrated in Shiraiwa’s Figure 1 reproduced below. Shiraiwa, [0026]-[0027]; Guidash, ¶162.

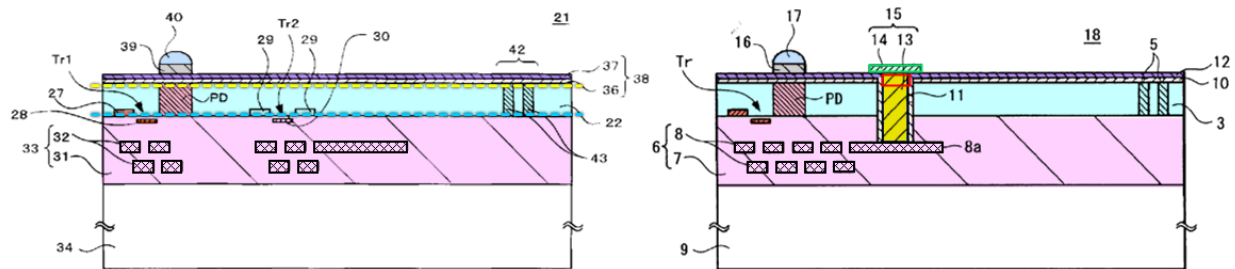


On substrate 22’s “back surface side,” a color filter 39 and an on-chip lens 40 corresponding to each pixel 25 is formed on passivation film 38, which comprises silicon nitride film 36 and silicon oxide film 37. Shiraiwa, [0026], [0032], [0039]; Guidash, ¶163. Shiraiwa discloses (but does not illustrate) that a pad is formed on the rear surface side to connect to wiring 32 prior to forming color filter 39 and on-chip lens 40. Shiraiwa, [0040]-[0041]; Guidash, ¶163; *see also* Shiraiwa, [0040] (disclosing same pad connecting to wiring on front-surface side of SOI-based sensor).

That is, Shiraiwa discloses a rear-surface pad connected to the front-surface wiring layer, but does not describe the details of its manufacture or illustrate this connection component in the drawings.

B. Shiraiwa-Sumi Combination

As discussed *supra* §VIII, Sumi discloses a rear surface electrode 15 providing the vertical connection for accessing the wiring on the substrate's front-side surface. Sumi, [0016]; Guidash, ¶165. Sumi's rear surface electrode 15 is implemented in virtually the identical BSI sensor disclosed in Shiraiwa, as illustrated by the side-by-comparison of Shiraiwa's Figure 1 (left) and Sumi's Figure 3B (right) below.



Thus, it would have been obvious to POSAs to use Sumi's rear surface electrode 15 as a known way to implement Shiraiwa's disclosed (but not illustrated) electrical connection between a rear-surface "pad" and "wiring 32" of Shiraiwa's sensor 21. Shiraiwa, [0040]; Guidash, ¶166. Moreover, POSAs would have been motivated to adopt Sumi's rear surface electrode 15 as doing so would

not require changing the structure of Shiraiwa's sensor or significantly altering the fabrication process. Guidash, ¶166.

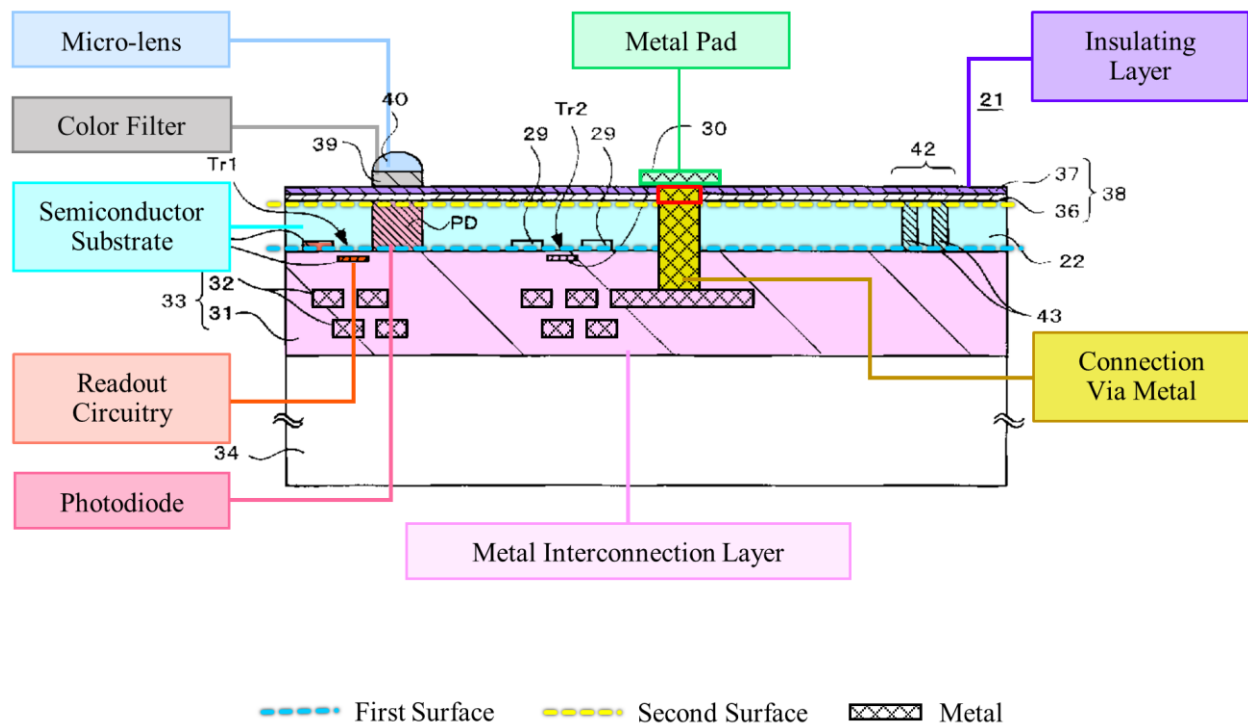
In particular, Shiraiwa and Sumi both disclose forming layered silicon nitride and oxide insulating films on the rear-surface side of the semiconductor substrate (Shiraiwa, [0027], [0039]; Sumi, [0016]) and, prior to forming a color filter and on-chip lens on top of the oxide insulating film (Shiraiwa, [0027], [0041]; Sumi, [0016]), providing electrical connection between a pad on the rear surface and the wiring on the front surface (Shiraiwa, [0040]; Sumi, [0016]). Guidash, ¶167. Thus, POSAs would have recognized the desirability of implementing Sumi's rear surface electrode 15 in Shiraiwa's sensor given the simplicity of this straightforward implementation. Guidash, ¶167.

Specifically, implementing Sumi's rear surface electrode 15 in Shiraiwa's sensor could have been integrated into the same rear-surface fabrication steps disclosed in Shiraiwa. After depositing Shiraiwa's silicon nitride film 36 on semiconductor 22's rear surface (Shiraiwa, [0039], Fig. 5F), Sumi's opening 11 would be formed through nitride film 36 and semiconductor substrate 22 to reach wiring 32, as disclosed in Sumi (Sumi, [0016]). Guidash, ¶168.

Next, Shiraiwa's silicon oxide film 37 would be formed over nitride film 36 (Shiraiwa, [0039]), which would also therefore cover the inside wall of the opening (Sumi, [0016]). Guidash, ¶169. Sumi's conductive layer 13 would then be formed

inside the opening to electrically connect to Shiraiwa's wiring 32 (Sumi, [0016]), followed by Sumi's electrode pad 14 that connects to conductive layer 13 to provide rear surface electrode 15 (*id.*). Thereafter, the optical components are formed on silicon oxide film 37 (Shiraiwa, [0041]). Guidash, ¶169.

Thus, formation of Sumi's rear surface electrode 15 can be integrated in Shiraiwa's disclosed BSI fabrication process. Guidash, ¶170. The resulting "Metal-Shiraiwa-Sumi Sensor" is illustrated below—incorporating Sumi's rear surface electrode 15 into Shiraiwa's sensor 21.



Sumi's rear surface electrode was positioned as shown above for clarity to illustrate how this structure would have been implemented to connect a rear facing electrode pad to the wiring on the front-side surface of the substrate without

obscuring the structure illustrated in Shiraiwa's Figure 1. Guidash, ¶171. However, POSAs understood that Sumi's rear surface electrode would have been implemented at locations where electrical connections to the wiring were needed—*i.e.*, at a “required position” in the BSI sensor, as disclosed in Shiraiwa (Shiraiwa, [0011], [0040]). Guidash, ¶171.

POSAs would have had a reasonable expectation of success at least because the same fabrication processes performed on the same material layers used to provide Sumi's rear surface electrode 15 can be applied to implement this structure in Shiraiwa's sensor. Guidash, ¶172.

C. The Metal-Shiraiwa-Sumi Sensor

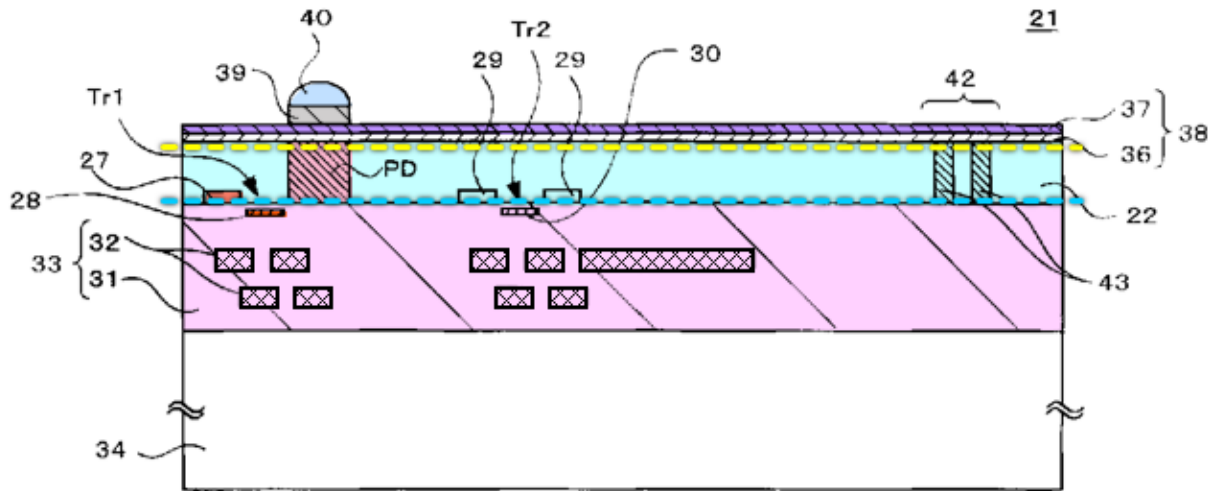
Like Sumi, Shiraiwa does not specify the material used for the wiring 32 or the pad (disclosed by not illustrated), but it would have been obvious and desirable to use metal for all electrical connections in the Shiraiwa-Sumi sensor, including “multilayer wiring 32” and Sumi's rear surface electrode 15 (*i.e.*, conductive layer 13 and electrode pad 14), as explained *supra* §VIII.B. This Metal-Shiraiwa-Sumi Sensor renders obvious claims 1-3.

D. Claim 1

1. Preamble – “An image sensor comprising:”

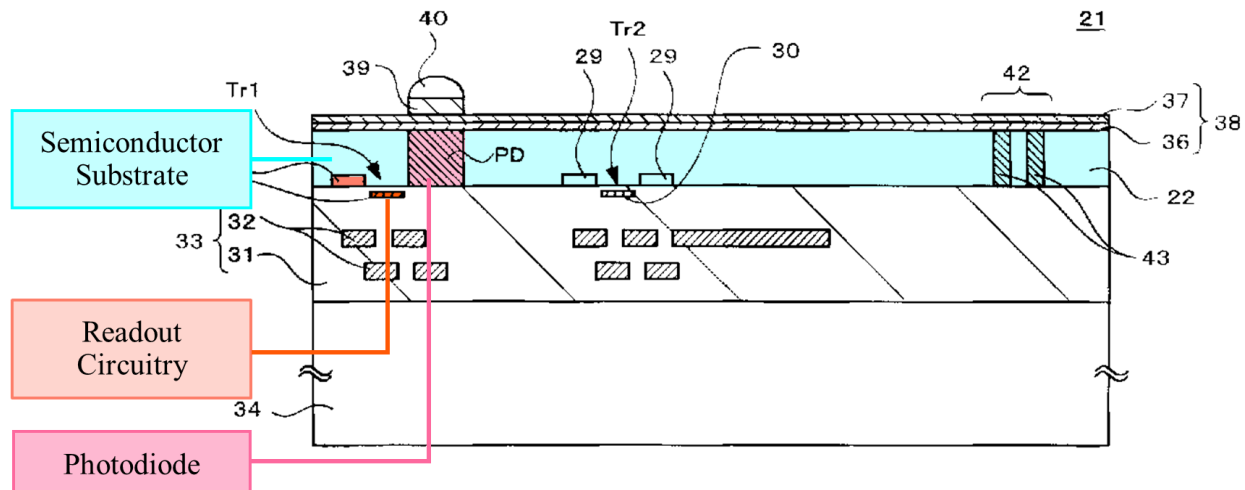
Shiraiwa discloses “a back-lit CMOS solid-state imaging element” comprising “light-receiving” photodiodes and read-out transistors (Shiraiwa,

[0026]), which imaging element POSAs understood is an “image sensor,” as recited in the preamble. Guidash, ¶174.



2. [1A] – “a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;”

Shiraiwa discloses “a plurality of unit pixels 25,” each configured from a “*photodiode* PD” and “a plurality of MOS transistors Tr1 serving as means for *reading signal charges* of the photodiode PD,” formed on the “front surface side” of “silicon *semiconductor substrate* 22,” as illustrated in Shiraiwa’s Figure 1 reproduced below. Shiraiwa, [0026]-[0027], [0035]; Guidash, ¶175.



The Metal-Shiraiwa-Sumi Sensor implements these same elements.

Accordingly, semiconductor substrate 22 of the Metal-Shiraiwa-Sumi Sensor having a photodiode area in which photodiode PD and corresponding readout transistors Tr1 are formed on the front surface side of the semiconductor substrate meets [1A]. Guidash, ¶176.

3. [1B] – “a metal interconnection layer formed on the first surface;”

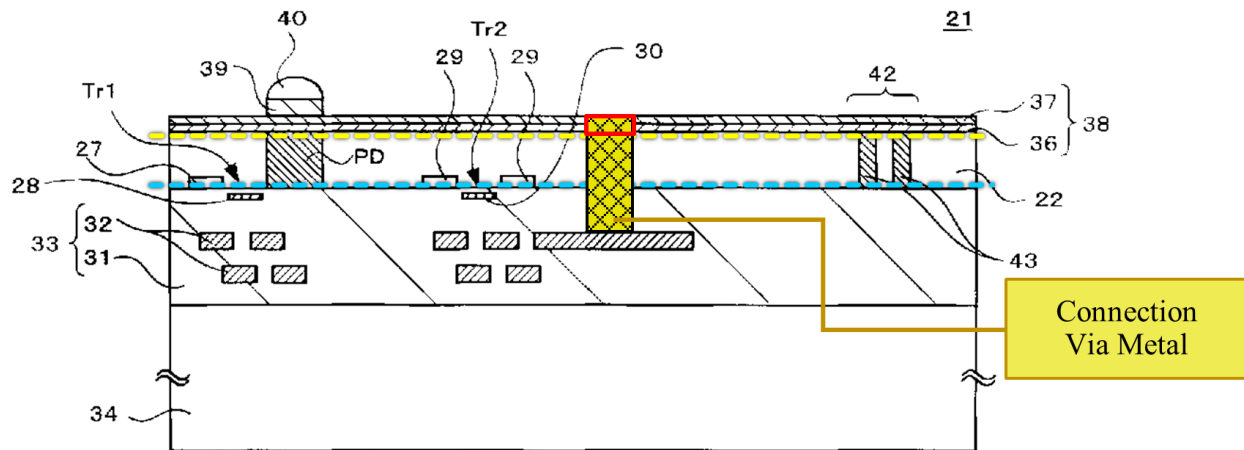
Using metal for “multilayer wiring 32” in “multilayer wiring layer 33” of the Metal-Shiraiwa-Sumi Sensor meets [1B]. Figure 1 of Shiraiwa reproduced below illustrates multi-layered wiring layer 33 comprising wiring 32 and interlayer insulating film 31. Shiraiwa, [0027], [0035]; Guidash, ¶177.

'143 patent, 3:1-4; Guidash, ¶179. When multi-layered wiring layer 33 is formed, the “front surface side” of semiconductor substrate is facing up, as illustrated in Shiraiwa’s Figure 4C. Shiraiwa, [0035]; Guidash, ¶179.

Thus, multi-layered wiring layer 33 of the Metal-Shiraiwa-Sumi Sensor meets [1B]. Guidash, ¶180.

4. **[1C] – “a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface;”**

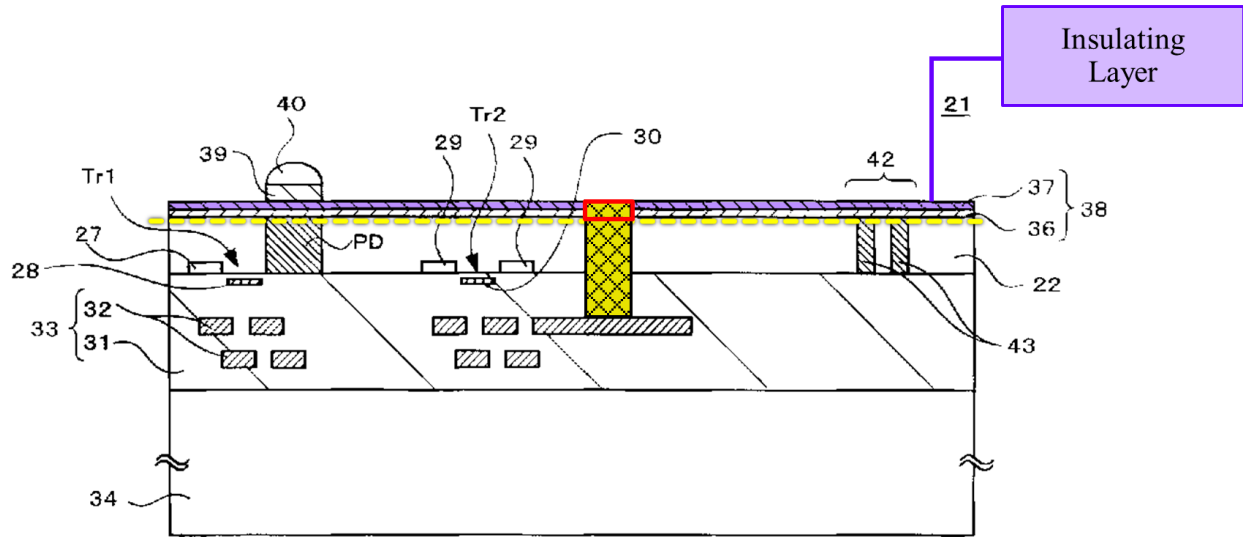
As discussed *supra* §X.C, the Metal-Shiraiwa-Sumi Sensor uses the rear surface electrode 15 of the Metal-Related-Art Sensor (*i.e.*, by using metal for conductive layer 13 and electrode pad 14 of Sumi’s rear surface electrode 15) to provide the electrical connection to multi-layered wiring layer 33 on the opposing side (*i.e.*, the claimed “first surface”) of semiconductor substrate 22, as illustrated in Shiraiwa Figure 1 modified to include the metal-based conductive layer 13 (the claimed “connection via metal”), which will be connected to metal pad 14 forming a rear surface electrode 15.



Thus, metal conductive layer (highlighted above) formed through semiconductor substrate 22 of the Metal-Shiraiwa-Sumi Sensor meets [1C] for the same reasons discussed in §VIII.B. Guidash, ¶¶181-182.

5. **[1D] – “an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and”**

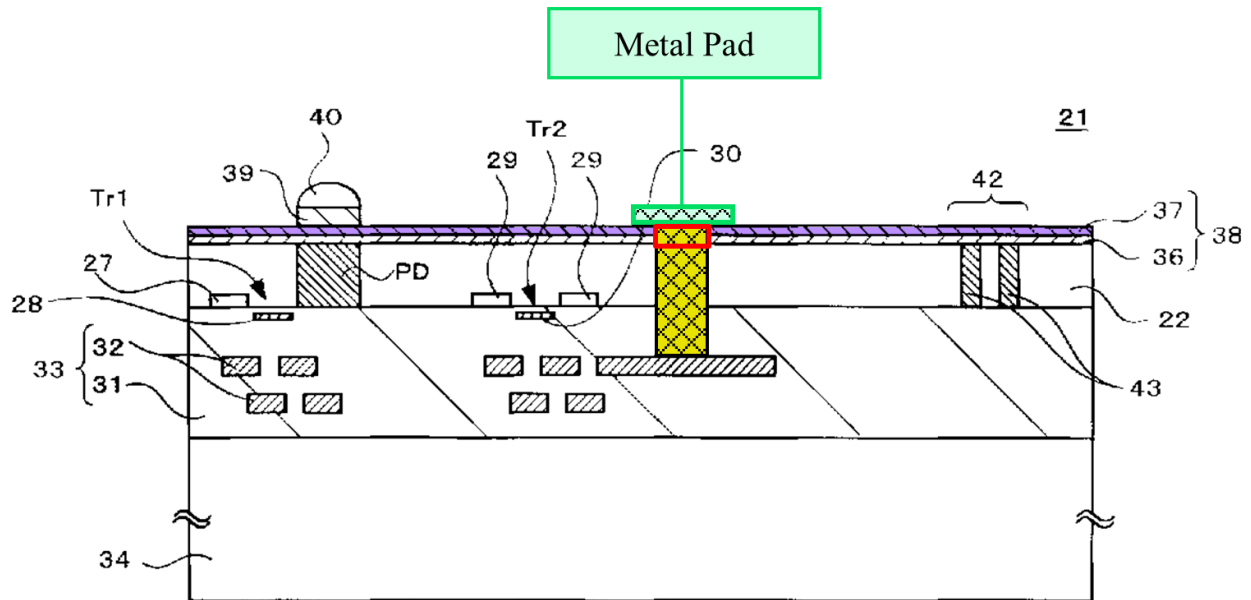
Silicon oxide film 37 of the Metal-Shiraiwa-Sumi Sensor meets [1D] for the same reasons discussed in §VIII.C.5 that Sumi’s insulation film 12 meets [1D] because Sumi’s rear surface electrode 15 is formed in Shiraiwa’s sensor in the manner described in Sumi, as discussed *supra* §X and illustrated in the Metal-Shiraiwa-Sumi Sensor below.



That is, after silicon nitride film 36 is formed on semiconductor substrate 22, Sumi's opening 11 is formed to reach wiring 32 and silicon oxide film 37 is formed on the inside wall of opening 11 and covering silicon nitride film 36. Guidash, ¶184; §X.B. Thus, when conductive layer 13 is formed in the opening, the top surface of conductive layer 13 is exposed, while the lateral sides of the projection part (red)—*i.e.*, the portion of conductive layer 13 extending beyond semiconductor substrate 22—are surrounded by silicon oxide film 37 (purple). Guidash, ¶184; §X.B.

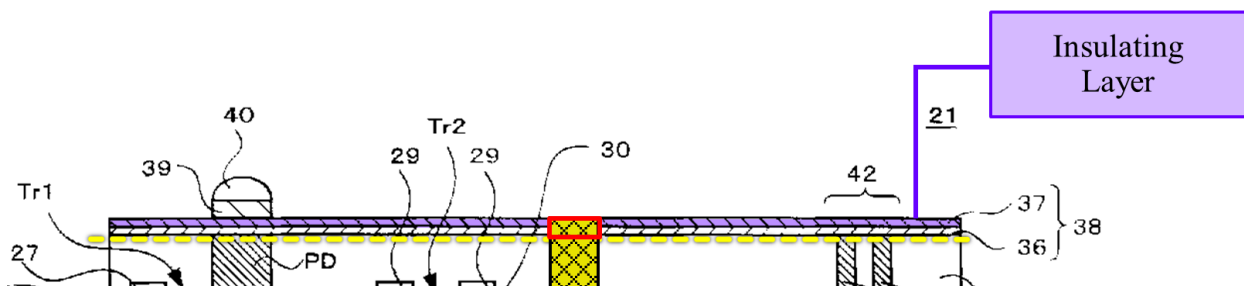
6. [1E] – “a metal pad formed on the insulating layer such that the metal pad covers the projection part,”

As discussed *supra* §§X.B-X.C, the Metal-Shiraiwa-Sumi Sensor uses Sumi's Metal-Related-Art Sensor's rear surface electrode 15 and, therefore, the metal electrode pad 14 highlighted in the Metal-Shiraiwa-Sumi Sensor illustrated below meets [1E] for the same reasons discussed *supra* §VIII.C.6. Guidash, ¶185.



7. [1F] – “wherein the insulating layer has a thickness thinner than a projection height of the projection part.”

As discussed *supra* §X.B, because Sumi’s rear surface electrode 15 is formed in Shiraiwa’s sensor in the same manner disclosed in Sumi, the height of the portion of the conductive layer 13 extending beyond semiconductor substrate 22 in the Metal-Shiraiwa-Sumi Sensor (illustrated below) is at least equal to the sum of the thicknesses of nitride film 36 and oxide film 37. Thus, oxide film 37 (*i.e.*, the insulating layer) is “thinner than a projection height of the projection part,” as recited in [1F] by at least the thickness of film 36. Guidash, ¶186.

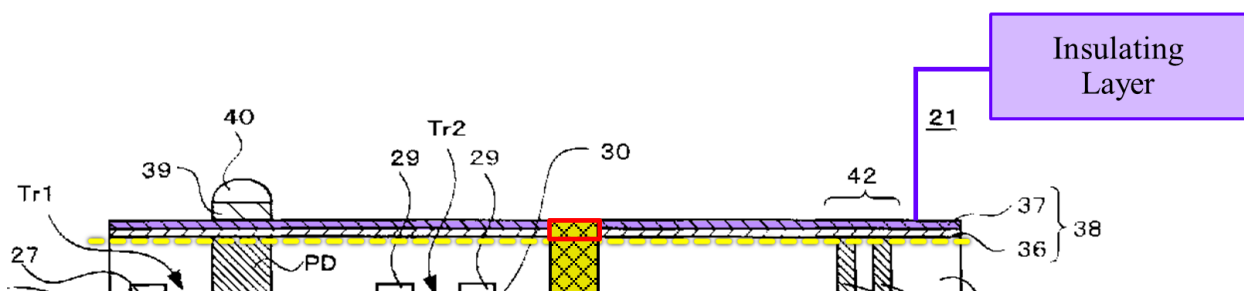


E. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”

Like Sumi’s description of “insulation film 12,” Shiraiwa describes the insulating film 37 as “silicon oxide,” but does not expressly describe it as a TEOS layer. Shiraiwa, [0008]. However, it would have been obvious to implement film 37 as a TEOS layer for the same reasons described *supra* §VIII.D concerning Sumi’s film 12. Guidash, ¶187.

F. Claim 3 – “The image sensor of claim 1, wherein the insulating layer is formed on a portion of the projection part extending from the second surface.”

The Metal-Shiraiwa-Sumi Sensor discloses a stacked dual-layer insulating layer formed on the substrate’s second surface. The figure below shows the insulating layer in the stacked dual-layer insulation film formed on the lateral sides of the portion of the projection part of the connection via extending from the second surface of semiconductor substrate 22.



Using a metal to form the connection via would not impact the deposition of the insulating layer on the projection part. Guidash, ¶189. The insulating layer in the stacked dual-layer insulation in the Metal-Shiraiwa-Sumi Sensor comprises a

silicon oxide film commonly fabricated on metal connection vias. Sumi, [0064]; see also Pain-1, [0077]. Accordingly, the Metal-Shiraiwa-Sumi Sensor renders claim 3 obvious.

XI. GROUND 4: CLAIMS 2 AND 4 WOULD HAVE BEEN OBVIOUS OVER SHIRAIWA IN VIEW OF SUMI'S RELATED-ART EMBODIMENT AND YANAGIDA-2

As discussed *supra* §IX, Yanagida-2 discloses a light-shielding layer that POSAs would have recognized as desirable to incorporate into the Metal-Shiraiwa-Sumi Sensor. The light-shielding layer (as disclosed in Yanagida-2) blocks light from penetrating into the substrate in areas other than the photoactive regions, and prevented light from adjacent pixel regions from reaching the photodiode. Guidash, ¶¶190-192. It would have been obvious to a POSA to incorporate Yanagida-2's protective layer and light shielding film into the Metal-Shiraiwa-Sumi Sensor. As with Sumi's Metal-Related-Art Sensor, POSAs would understand that the Metal-Shiraiwa-Sumi Sensor provides a small level difference at the backside surface of only the thickness of the pad 14, preventing the uneven application of color filter and lens materials. Yanagida-2, [0067]-[0068].

Further, Yanagida-2 discloses a TEOS layer. It would have been obvious when implementing the Metal-Shiraiwa-Sumi Sensor to incorporate TEOS as the silicon oxide, as taught in Yanagida-2, for the same reasons discussed *supra* §§IX.A-D. Guidash, ¶191.

XII. GROUND 5: CLAIMS 1-3 WOULD HAVE BEEN OBVIOUS OVER YANAGIDA-1

A. Overview of Yanagida-1

Yanagida-1 published as Japanese Publication No. JP 2006-032497 A on February 2, 2006. Yanagida-1, 1. Yanagida-1 is therefore pre-AIA §102(b) prior art. Yanagida-1 was published in Japanese (Ex. 1020) and a certified English translation is provided herein (Yanagida-1, 1-17).

Yanagida-1 describes BSI CMOS image sensors and their advantages over front-side-illuminated sensors, but also notes the risk of problems if the “semiconductor well region formed at the periphery of the photoelectric conversion elements were grounded via the wiring disposed from the front face side of the single crystal silicon layer.” *Id.*, [0008]. Such configurations may cause high resistance in the well region—inhibiting extraction of photoelectric elements. *Id.*, [0008]-[0010]. Yanagida-1 instead describes a BSI sensor “capable of allowing the minority carriers generated in the photoelectric conversion elements to be easily extracted.” *Id.*, [0011].

Yanagida-1’s image sensor comprises a solid-state substrate, interconnection layers, a through silicon via, an antireflective layer, a bonding pad, and a microlens. *Id.*, [0012], [0018], [0026]; *see also* Guidash, ¶¶193-195.

B. Obviousness of Implementing Yanagida-1 Using Metal-Based Film

Yanagida-1 does not disclose particular materials for the interconnection layer (wiring 26) and pad (light shielding film). POSAs would have been motivated to use metal for these structures. Guidash, ¶196.

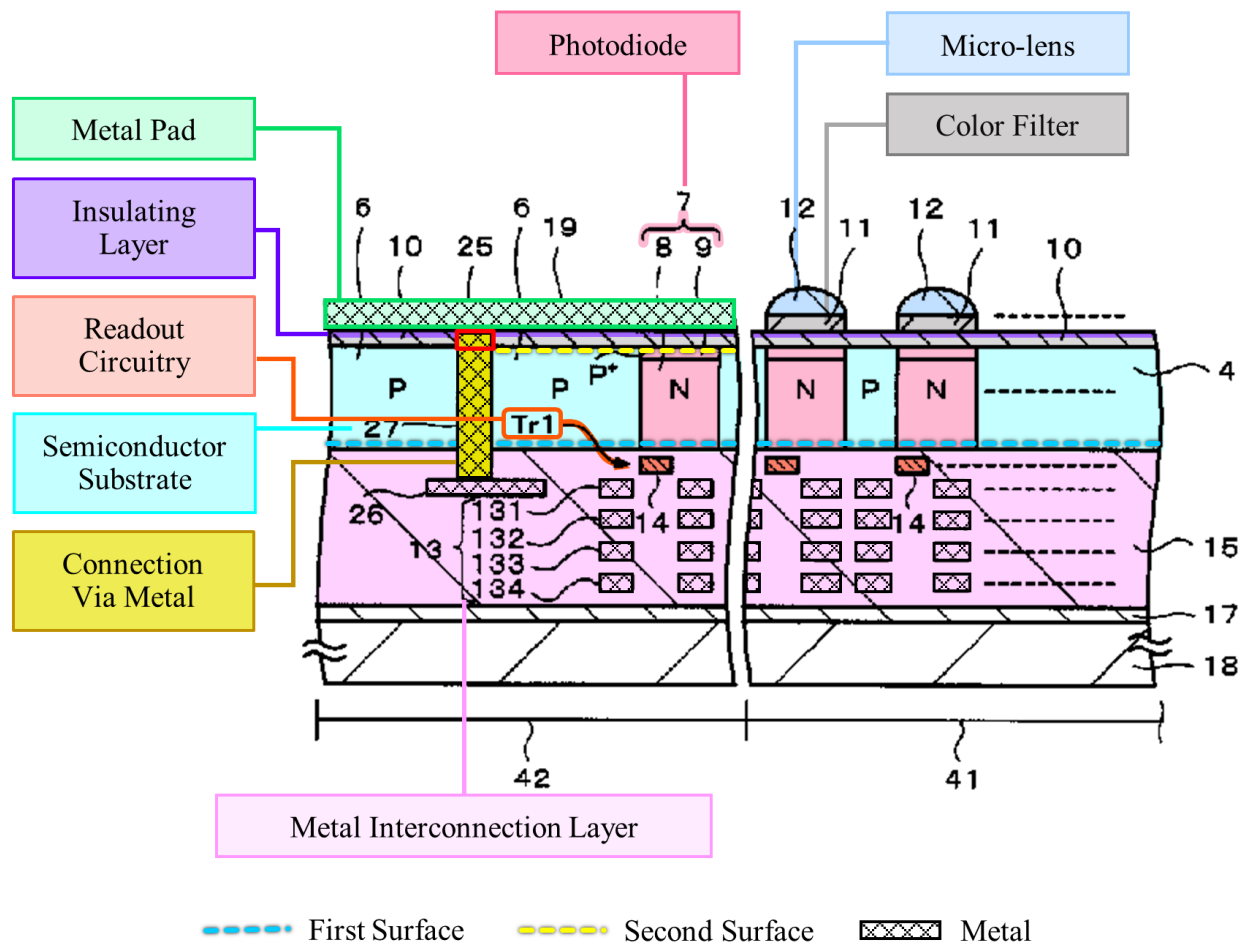
1. Reasons for Using Metal

POSAs implementing Yanagida-1 would have had reason to incorporate a metal-based interconnection layer. Guidash, ¶197; Pain-1, [0036]. Fabricating wiring 26 using a low-resistivity metal such as copper would ensure that the wiring serves its disclosed function, including electrically connecting to the conductive material in the connection via. Guidash, ¶197; Pain-1 [0036]; Quirk, 305-306; Garrou, 157-173. Further, Yanagida-1 states, “a conductive material layer 25 is formed in an element separation region 5 of the optical black region 42, a voltage application means is constructed to apply a voltage to the conductive material layer 25 from the front face side of the single crystal silicon layer 4.” Yanagida-1, [0075]. Metal conductors, especially copper, were commonly used in image sensors by 2008 to provide high conductivity. Guidash, ¶198; Pain-1 [0077]; Quirk, 305-306; Garrou, 157-173. POSAs therefore would have used metal in Yanagida-1’s wiring in the ordinary course of implementing Yanagida-1’s design. Guidash, ¶197.

Similarly, POSAs would have had reason to fabricate Yanagida-1's light shielding film using metal to fulfill the film's disclosed function of electrically connecting to the conductive material in the hole. Guidash, ¶198; Yanagida-1, [0064]. As with the conductive material, metal would have been an obvious choice to ensure the electrical connection. Guidash, ¶198.

2. Resultant Metal-Yanagida-1 Sensor

The image sensor resulting from implementing Yanagida-1's design using metal in the interconnection layer and pad ("Metal-Yanagida-1 Sensor") is shown in the figure below. Guidash, ¶199.



As the figure illustrates, Yanagida-1's device is not impacted by the above-discussed selection of metal for wiring 26 and light shielding film 19.

Wiring 26 (*i.e.*, the metal interconnection layer) is formed on the front side of the sensor and connected to the metal conductive material 25 in connection via (hole 27). Guidash, ¶201. The wiring layer 26 is formed after the photodiodes and transistors have been formed, and therefore must be formed with a low temperature process that will not affect the characteristics of the photodiodes and transistors. Metals such as copper can be deposited at low temperatures—confirming the above-noted reasons for using metal.

As with the interconnection layer, the pad (light shielding film 19) can be implemented using metal without impacting the sensor's structure. Guidash, ¶202. The metal pad would be formed over the projection part of the connection via using a low-temperature process compatible with rear-side fabrication. Guidash, ¶202. The resultant metal pad in Yanagida-1 may be patterned and routed to other elements to conduct electrical signals the same way as Yanagida-1's design. Guidash, ¶202; Yanagida-1, [0075].

3. Reasonable Expectation of Success

POSAs would have had a reasonable expectation success in implementing Yanagida-1's sensor using metal for wiring 26 and light shielding film 19.

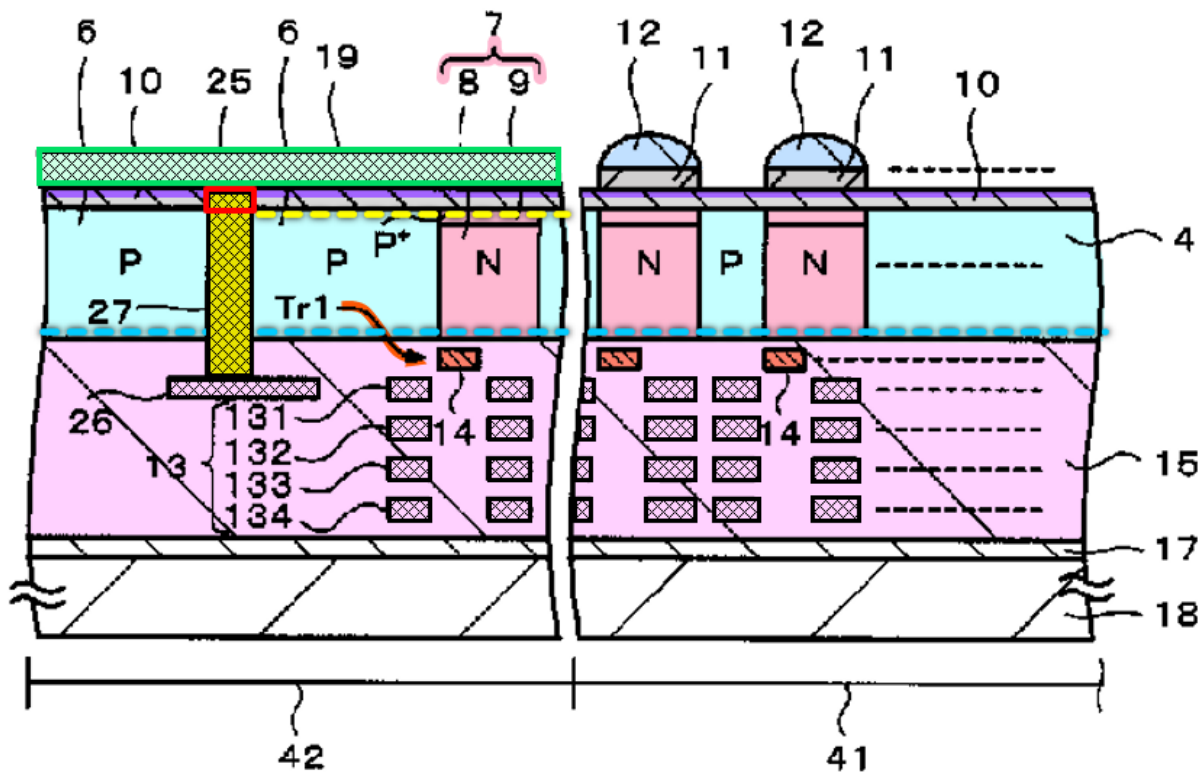
Guidash, ¶203; Pain-1, [0077]; Quirk, 302-306; Garrou, 157-173. Yanagida-1 itself

does not disclose specify particular materials for these components. Yanagida-1, [0039], [0044]. POSAs would have had a reasonable expectation of success when using any suitable material consistent with the physical design and fabrication requirements of the Yanagida-1 device. Guidash, ¶203. Metal would have been desirable due to its high conductivity, low resistivity, and compatibility with the low-temperature methods required for the backside fabrication process. Guidash, ¶203. Metals indeed were the standard choice for wiring layers and electrode pads for semiconductor devices in the relevant timeframe of the '143 patent. Guidash, ¶73.

C. Claim 1

1. Preamble – “An image sensor comprising:”

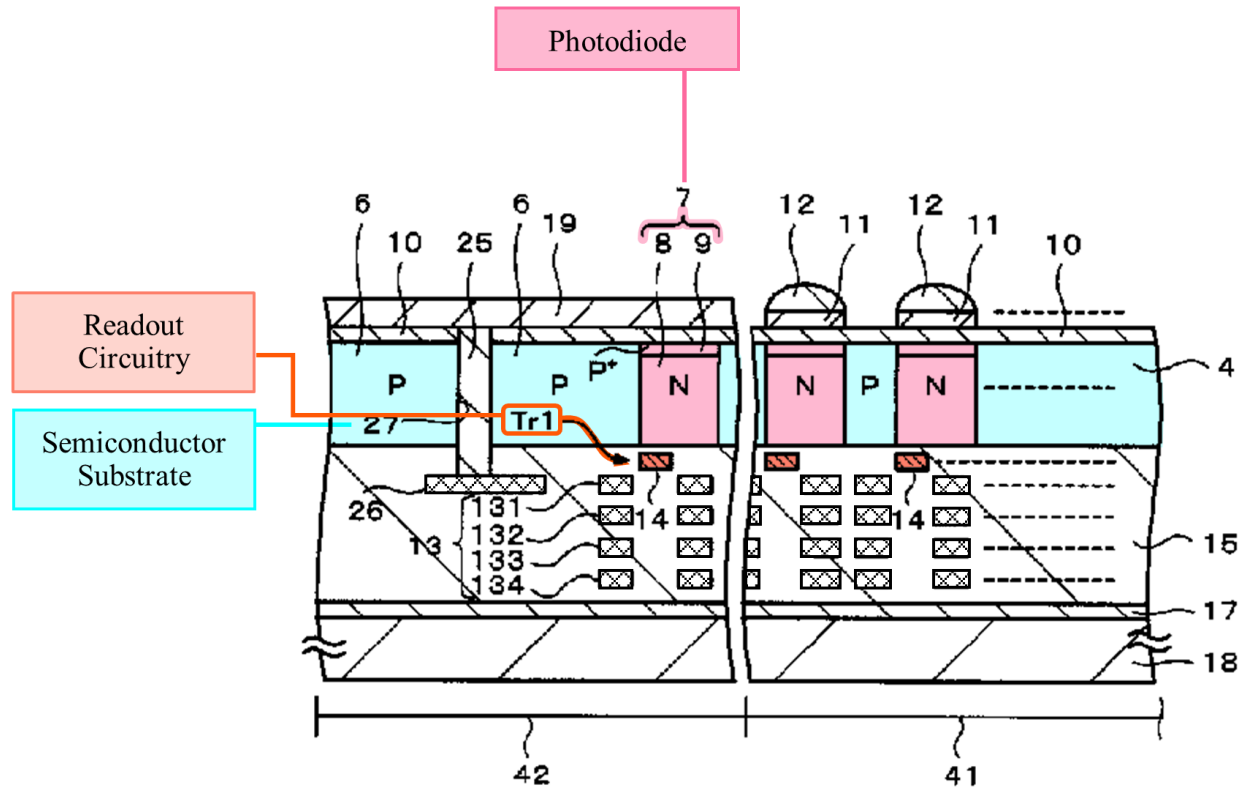
Yanagida-1 discloses a “solid-state image sensor,” which constitutes an “image sensor” per the preamble. Yanagida-1, [0012]; Guidash, ¶205.



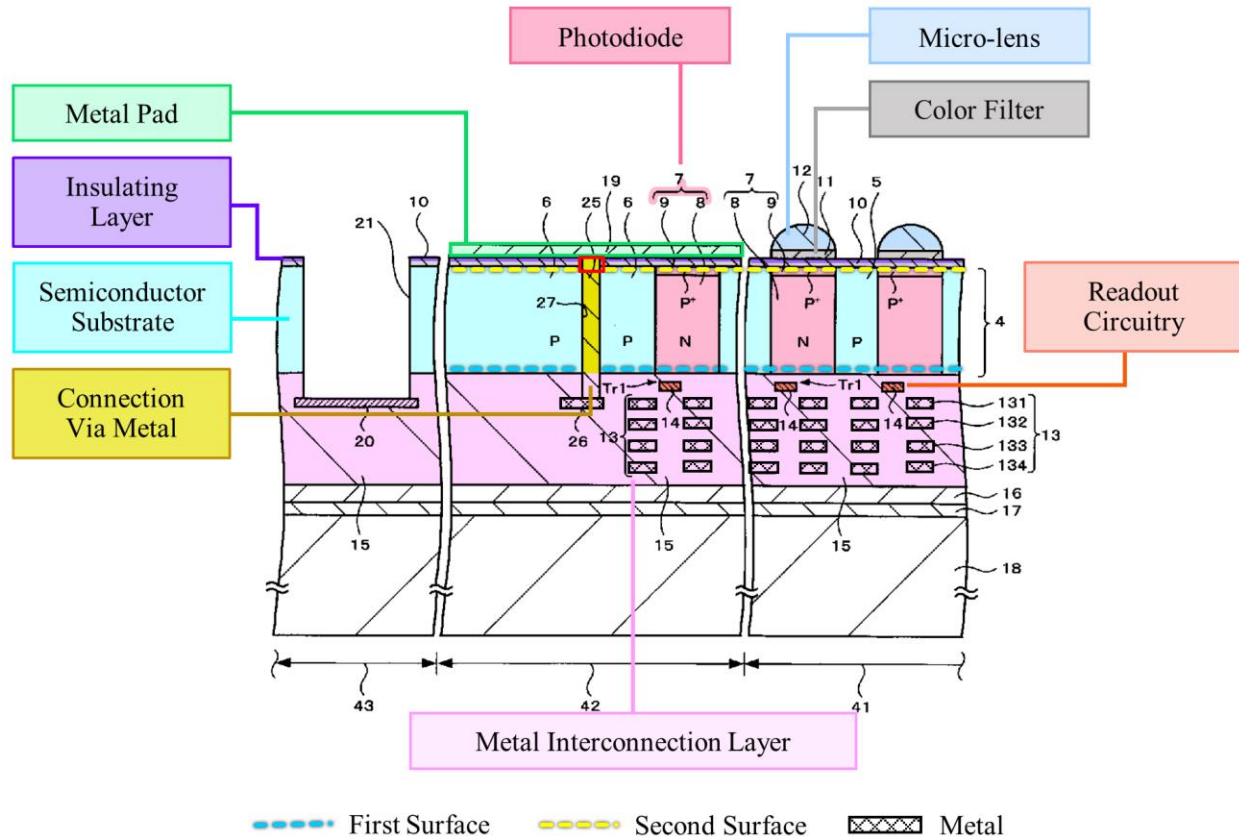
2. Claim [1A] – “a semiconductor substrate formed on a first surface thereof with a readout circuitry and a photodiode area;”

Yanagida-1’s image sensor includes a semiconductor substrate formed on a first surface with readout circuitry and a photodiode area. Guidash, ¶206.

Yanagida-1 discloses a sensor in which lights is “irradiated against the photoelectric conversion elements from the back face side of the **semiconductor substrate**, wherein the solid-state image sensor is constructed with a semiconductor region formed in the semiconductor substrate at the periphery of the photoelectric conversion elements...” Yanagida-1, [0012].



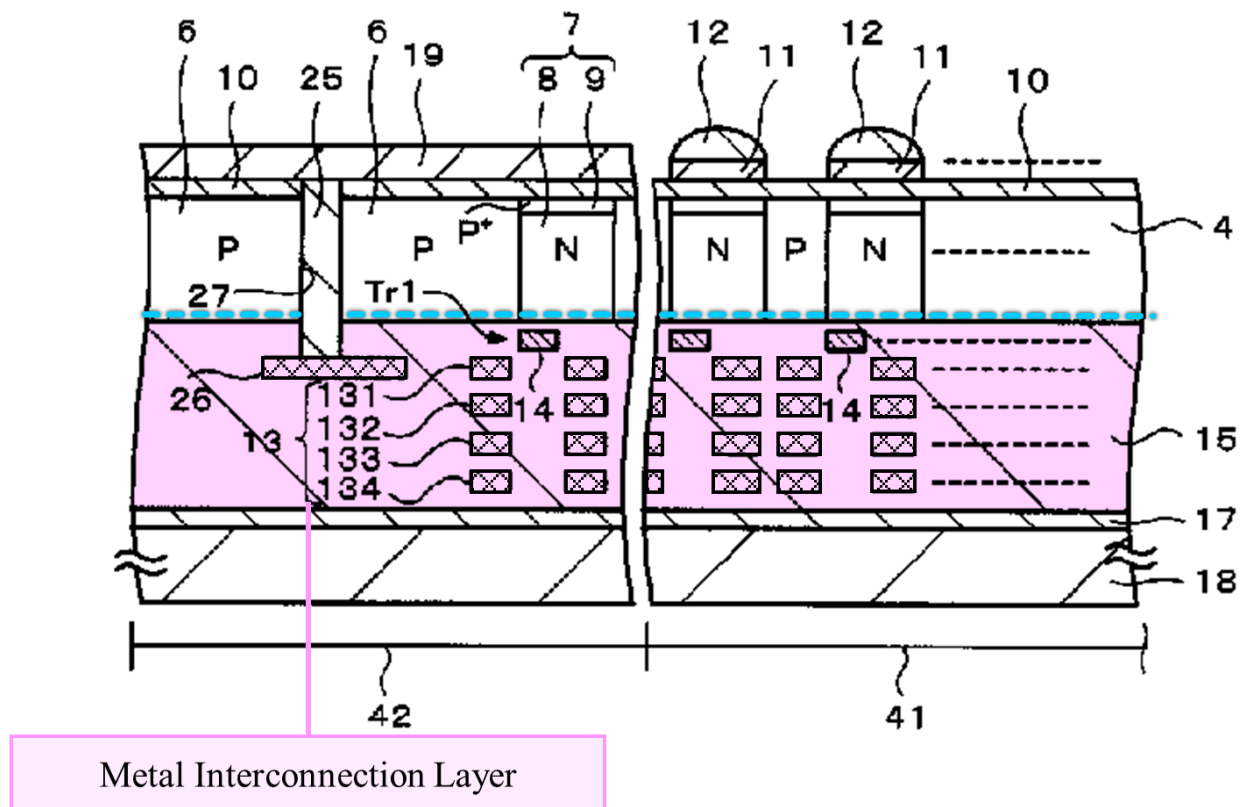
Regarding the photodiode, Yanagida-1 states “[i]n the image pickup region 41, as shown in Fig. 2 below, **photoelectric conversion elements 7** comprising N-type semiconductor regions are formed in unit pixel regions divided by the element separation regions 5 formed in the semiconductor substrate (e.g., single crystal silicon layer) 4. The photoelectric conversion elements 7 are each formed with a charge accumulation region 8 comprising an N-type semiconductor region, and a positive charge accumulation region 9 comprising a high concentration P-type semiconductor region.” *Id.*, [0025]. POSAs would have understood the photoelectric conversion elements as photodiodes, as illustrated below. Guidash, ¶207.



Further, readout circuitry is formed with the photo conversion elements. Specifically, “[o]n the other principal face side of the single crystal silicon layer 4, i.e., the front face side (lower side in the figure), **MOS type transistors Tr1**, for example, are formed in correspondence to the photoelectric conversion elements 7, and multilayer wiring layers 13 are formed on the transistors Tr1.” *Id.*, [0026]. POSAs would have understood the transistors as readout circuitry. Guidash, ¶208.

3. **Claim [1B] – “a metal interconnection layer formed on the first surface;”**

Yanagida-1 discloses **wiring layers 13** on the front face side of the semiconductor well region 6. Yanagida-1, [0036]. POSAs would understand Yanagida-1’s wiring layers 13 as an interconnection layer. Guidash, ¶209.

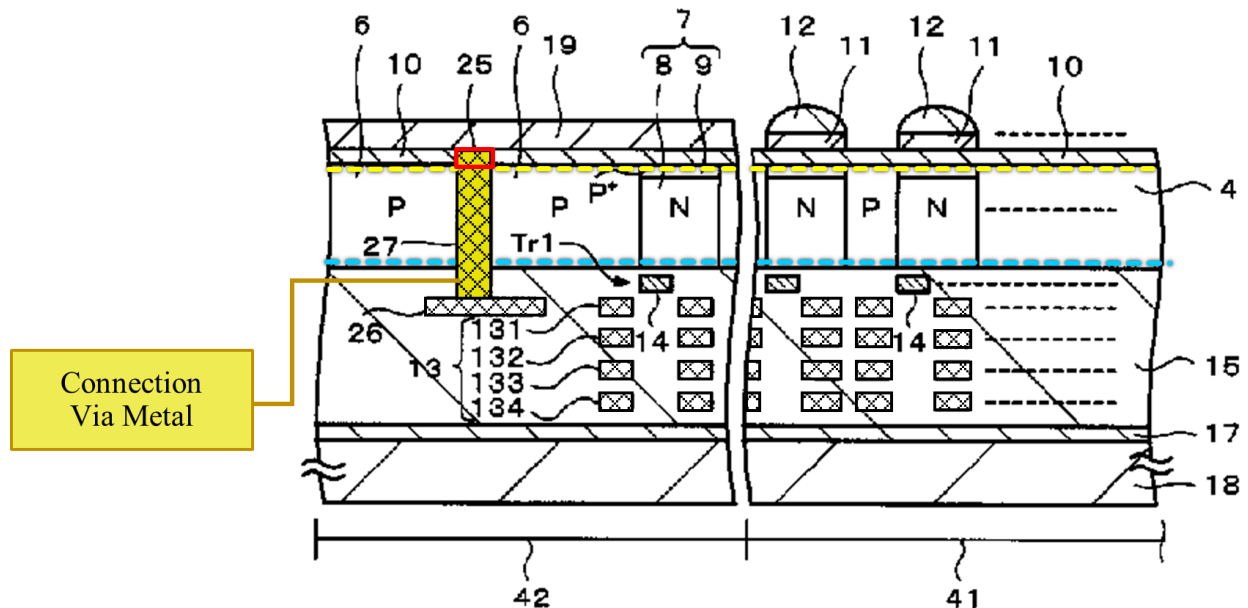


As discussed *supra* §XII.B, it would have been obvious when implementing Yanagida-1 to incorporate metal-based wiring, therefore forming a metal interconnection layer.

As shown in the figure above, metal interconnection layer 13 is formed on a first surface of the substrate.

4. **Claim [1C] – “a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface;”**

As illustrated below, Yanagida-1 discloses a connection via (hole 27) extending from the substrate’s first surface to the second surface. The figure illustrates the projection part (red box) of the connection via of the hole projecting from the substrate’s second surface. Guidash, ¶212.



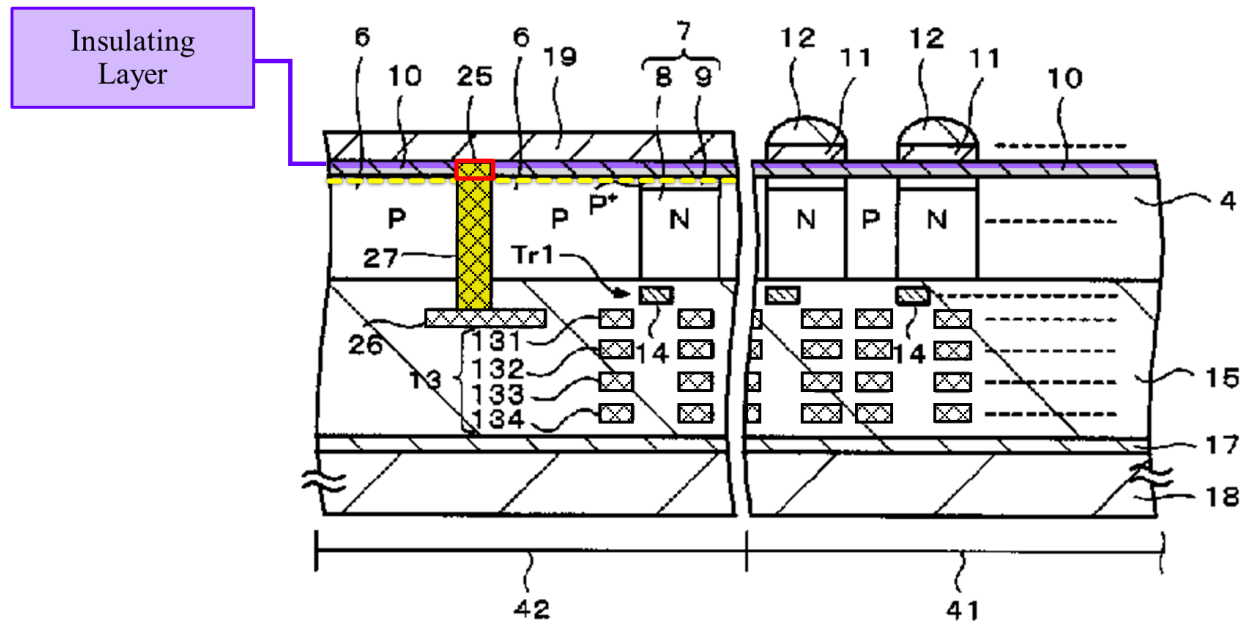
Further, Yanagida-1 teaches the connection via 27 comprises a metal material film. Yanagida-1, [0036] (“conductive material layer 25 is formed by being embedded in the **hole 27**.”). Yanagida-1 states, “[f]or the conductive material layer 25, a conductive material, for example, **metal materials, such as AlCu, Al, AlSi, or W can be used**. When such a metal material is used, the

resistance of the conductive material layer 25 will be lower than that within the semiconductor well region 6.” *Id.*, [0037]. Guidash, ¶213.

5. Claim [1D] – “an insulating layer formed on the second surface of the semiconductor substrate to expose the projection part while surrounding a portion of a lateral side of the projection part; and”

Yanagida-1 discloses an antireflective film 10 comprising oxide and nitride layers. Yanagida-1, [0026]. POSAs would recognize the oxide layer itself as an insulating layer. Guidash, ¶214.

The antireflective film comprising the oxide layer is formed on the second surface of the substrate. “More specifically, in the state where the single crystal silicon layer 4 of the SOI substrate 30 is exposed [], an antireflective film is formed on the single crystal silicon layer 4, then a photoresist film is formed on the antireflective film, and then the resist mask having the pattern for forming the opening and the hole is formed by a known lithography process.” *Id.*, [0063]. The ’143 patent discloses a liner oxide layer 170 such that the “liner oxide layer 170” itself constitutes the “insulating layer.” ’143 patent, 5:4-38. As discussed *supra* §VI.A, in the ’143 patent’s disclosure, the insulation layer comprises only an oxide layer. As such, the oxide film alone in Yanagida-1’s antireflective film 10 corresponds to the insulating layer recited in the ’143 patent.



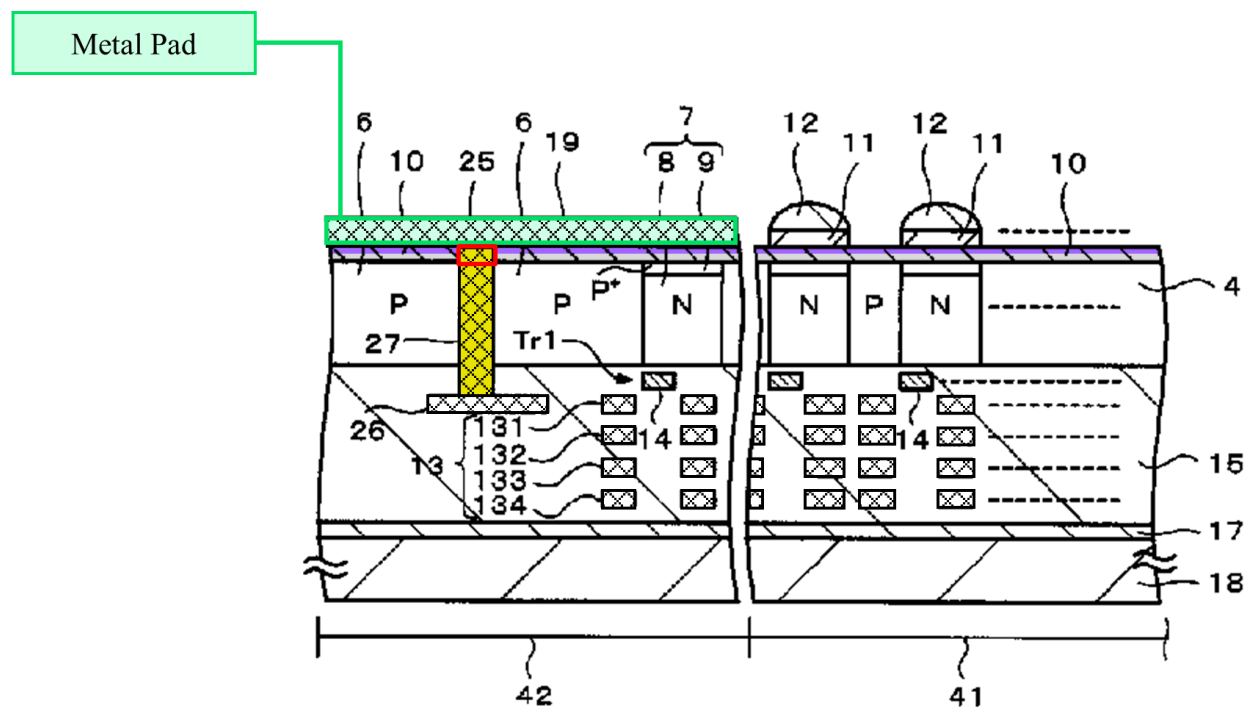
As seen in the figure above, the antireflective film 10 (purple) comprising the oxide film exposes the projection part (red box) and surrounds the lateral sides of the projection part.

6. Claim [1E] – “a metal pad formed on the insulating layer such that the metal pad covers the projection part,”

Yanagida-1’s light shielding film is a pad. A bonding pad is “a metallized area on the surface of a semiconductor device, to which connections can be made.” McGraw-Hill (Ex. 1024), 266; *see also* Laplante (Ex. 1025), 6. Although Yangida-1 does not specifically state the light shielding film is metal, the use of metal was well-known. POSAs would have known how to implement these structures using metal, and the use of metal would have yielded predictable results.

Yanagida-1 states, “[i]n the optical black region 42, a light shielding film 19 is formed on the back face side of the single crystal silicon layer 4 via the

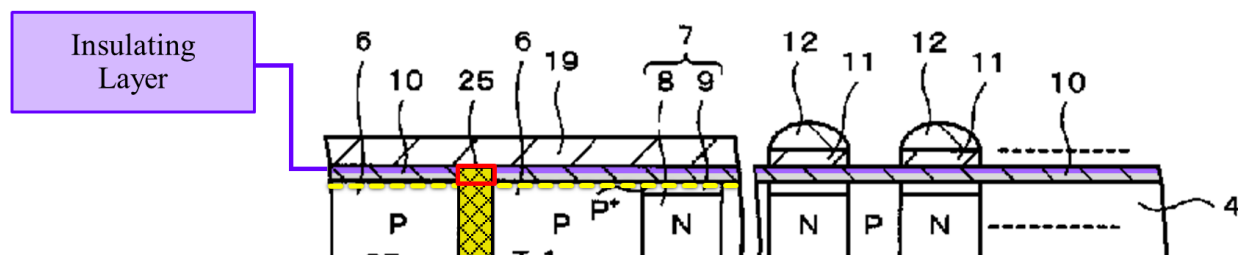
antireflective film 10.” Yanagida-1, [0031]. “The light shielding film 19 is formed so as to cover all the photoelectric conversion elements formed in the optical black region 42.” *Id.* Further, “voltage can be applied to the conductive material layer 25 via the light shielding film 19.” *Id.*, [0075]. POSAs would have recognized that Yanagida-1’s light shielding film 19 is a pad; the design is similar to structures commonly used as backside bond pads. Guidash, ¶218. Similar to the metal pad described in the ’143 patent, Yanagida-1’s light shielding film 19 connects to a super via. *Id.* The connection of the structure to the via is consistent with a metal pad. Guidash, ¶219.



Yanagida-1 does not describe the material composition of light shielding film 19; however, it would have been obvious when implementing Yanagida-1 to select a metal-based film for the reasons discussed *supra* §XII.B.

7. Claim [1F] – “wherein the insulating layer has a thickness thinner than a projection height of the projection part.”

As the figure below illustrates, the projection part extends past the substrate through Yanagida-1’s antireflective film 10 and has a thickness that is at least equal the film’s height. The antireflective film comprises both an oxide film and nitride film. Yanagida-1, [0026]. The thickness of the projection part is the sum of the thicknesses of the oxide film and nitride film in Yanagida-1. In sum, the thickness of the projection part in Yanagida-1 exceeds the thickness of the oxide insulating layer in antireflective film 10. Guidash, ¶221.



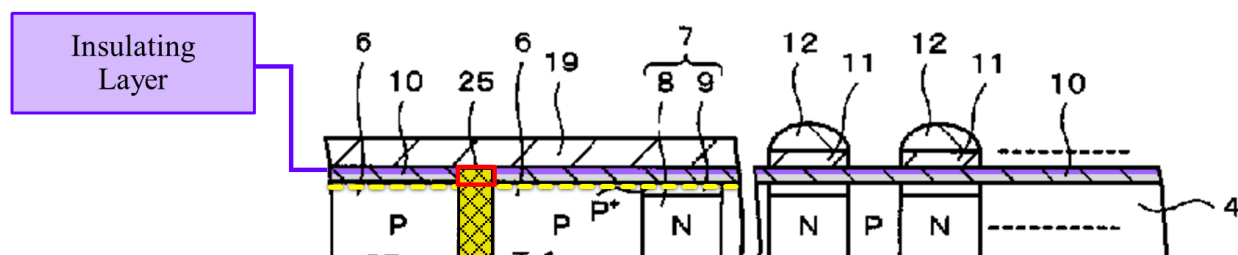
D. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”

While Yanagida-1 does not disclose the exact composition of the oxide film (*i.e.*, the insulating layer as discussed above), POSAs would have had reason to select TEOS for the same reasons discussed *supra* §VIII.D. Incorporating a TEOS layer would have constituted the use of a known material (TEOS) for its intended

function (insulating) to yield the predictable result of providing the oxide film in Yanagida-1's sensor. *KSR*, 550 U.S. at 415-421.

E. Claim 3 – “The image sensor of claim 1, wherein the insulating layer is formed on a portion of the projection part extending from the second surface.”

Yanagida-1's oxide film (*i.e.*, the insulating layer as discussed above) is formed on a portion of the projection part extending from the second surface. Guidash, ¶223. The figure below shows the oxide insulating layer in antireflective film 10 is formed on the lateral sides of the projection part of hole 27.



XIII. GROUND 6: CLAIMS 2 AND 4 WOULD HAVE BEEN OBVIOUS OVER YANAGIDA-1 IN VIEW OF YANAGIDA-2

A. Combination of Yanagida-1 and Yanagida-2

POSAs implementing Yanagida-1 would have had reason to incorporate Yanagida-2's teachings (discussed *supra* §IX) concerning the desirability of TEOS and a protective layer.

1. Reasons for Incorporating Yanagida-2's Teachings

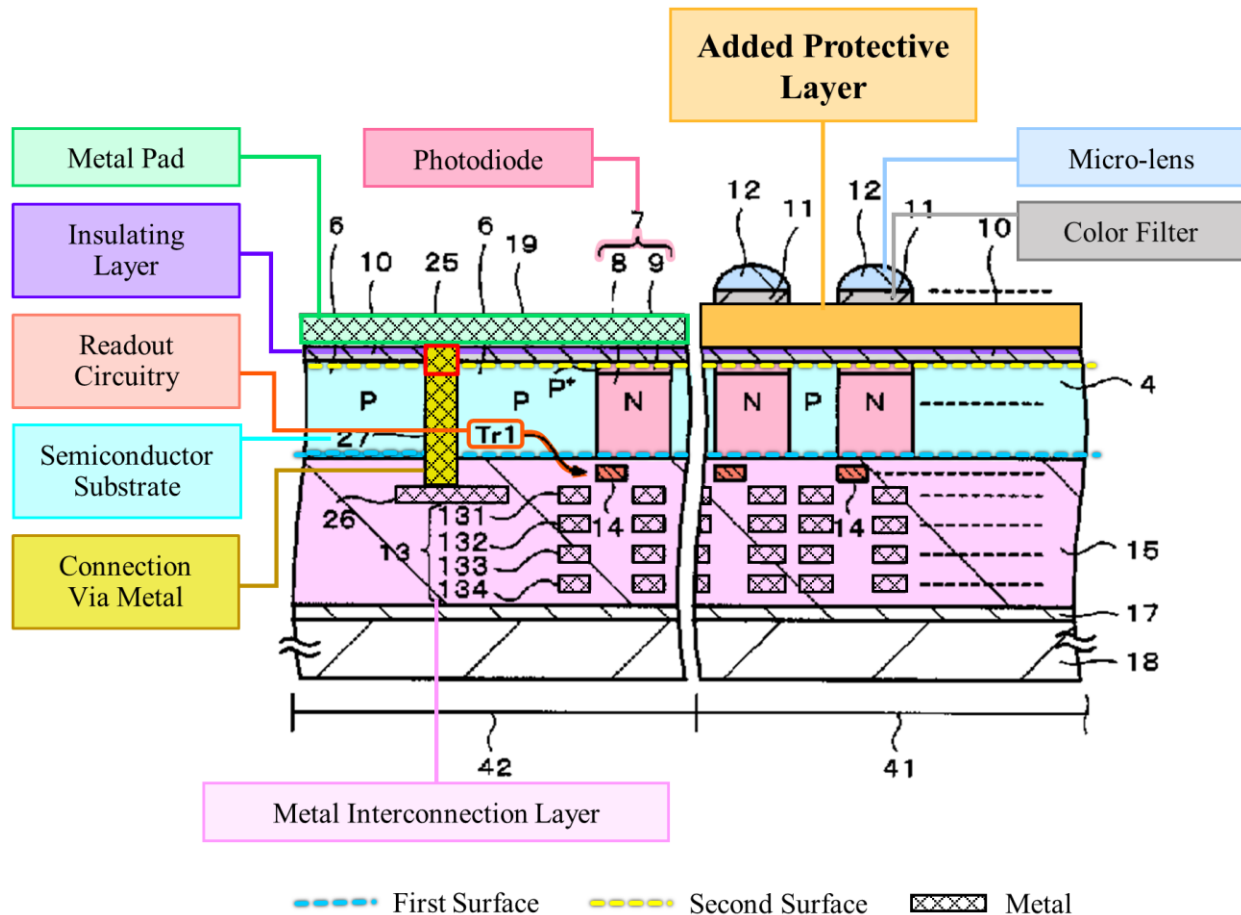
Yanagida-1 and Yanagida-2 both describe backside-illuminated image sensors and address the same problem of light inefficiency and sensitivity caused by frontside-illuminated sensors. Yanagida-1 and Yanagida-2 teach insulation

elements, comprising at least an oxide layer, formed on the light incident side of the substrate. Yanagida-1, [0026]; Yanagida-2, [0034]. They also both describe the oxide layer as paired with a nitride film. Yanagida-1, [0026] (components of Yanagida-1's "antireflective film 10"); Yanagida-2, [0043] (components of Yanagida-2's "anti-reflection film 90"). Yanagida-2 specifically discloses TEOS as the oxide layer in the antireflection film (Yanagida-2, [0043]), and POSAs likewise would have recognized TEOS as a very commonly used material and as a particularly desirable type of oxide for Yanagida-1's film. Guidash, ¶225. Using a TEOS layer, as Yanagida-2 discloses, as a low-temperature insulator formed on the backside and using a protective layer above the oxide insulating layer would better passivate the device. Guidash, ¶225.

2. Resultant Metal-Yanagida-1-Yanagida-2 Sensor

The sensor resulting from implementing the Metal-Yanagida-1 Sensor design using a TEOS layer would not change the device's physical structure or methods for fabrication. Guidash, ¶226. The TEOS material would be used in the oxide insulating layer in antireflective film 10. As taught in Yanagida-1, the insulation layer comprises an oxide film. *See supra* §XII.C.5. As discussed previously, TEOS is a common oxide material. Pain-2. [0074].

The sensor resulting from modifying the Metal-Yanagida-1 Sensor to include a protective layer on the oxide insulating layer (“Metal-Yanagida-1-Yanagida-2 Sensor”) is illustrated below. Guidash, ¶227.



As seen above, the protective layer will form a thick layer above the insulating layer. Further, when formed on the insulating layer, the protective layer will be etched in the process of forming the connecting via connecting Yanagida-1's wiring layer 26 to metal pad 19. Guidash, ¶228. This is consistent with Yanagida-1's color filter and microlenses; Yanagida-2 discloses that both can be formed on the protective layer. Yanagida-2, [0035].

3. Reasonable Expectation of Success

POSAs would have had a reasonable expectation of success in using a TEOS layer as the Metal-Yanagida-1-Yanagida-2 Sensor's oxide film and also forming a protective layer on the film. Both procedures are known in the art and would require no modification to Yanagida-1's physical design. *See* §XIII.A.1-2; *see also* Guidash, ¶229; Pain-2, [0074]; Quirk 271-272.

B. Claims 1 and 3

The combination of Yanagida-1 and Yanagida-2 satisfies claims 1 and 3 for the same reasons as Yanagida-1 alone discussed *supra* §XII, which are unchanged in the combination. Guidash, ¶230.

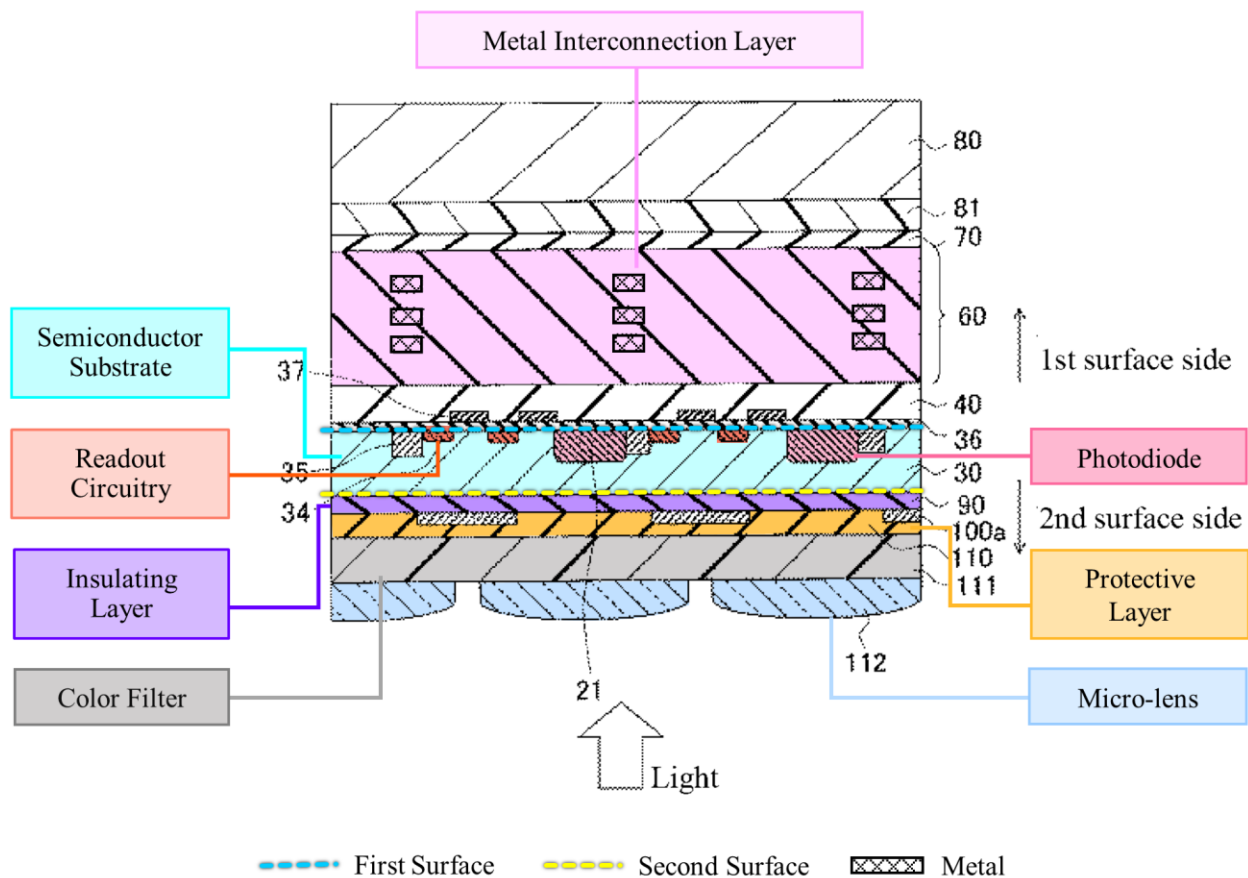
C. Claim 2 – “The image sensor of claim 1, wherein the insulating layer comprises a TEOS layer.”

As discussed *supra* §§XII.B and XIII.A, TEOS was a commonly known material for oxide layers and facilitates the low-temperature fabrication required for BSI sensors such as Yanagida-1. Guidash, ¶231. POSAs accordingly would have been motivated to use a TEOS layer as described in Yanagida-2 as an insulating layer in Yanagida-1. Indeed, both Yanagida-1 and Yanagida-2 teach an insulating layer comprising an oxide, and POSAs would have understood that a TEOS layer would be a low-temperature oxide suitable for BSI fabrication. Guidash, ¶231.

D. Claim 4

1. **Claim [4A] – “The image sensor of claim 1, further comprising: a protective layer formed over the insulating layer; and”**

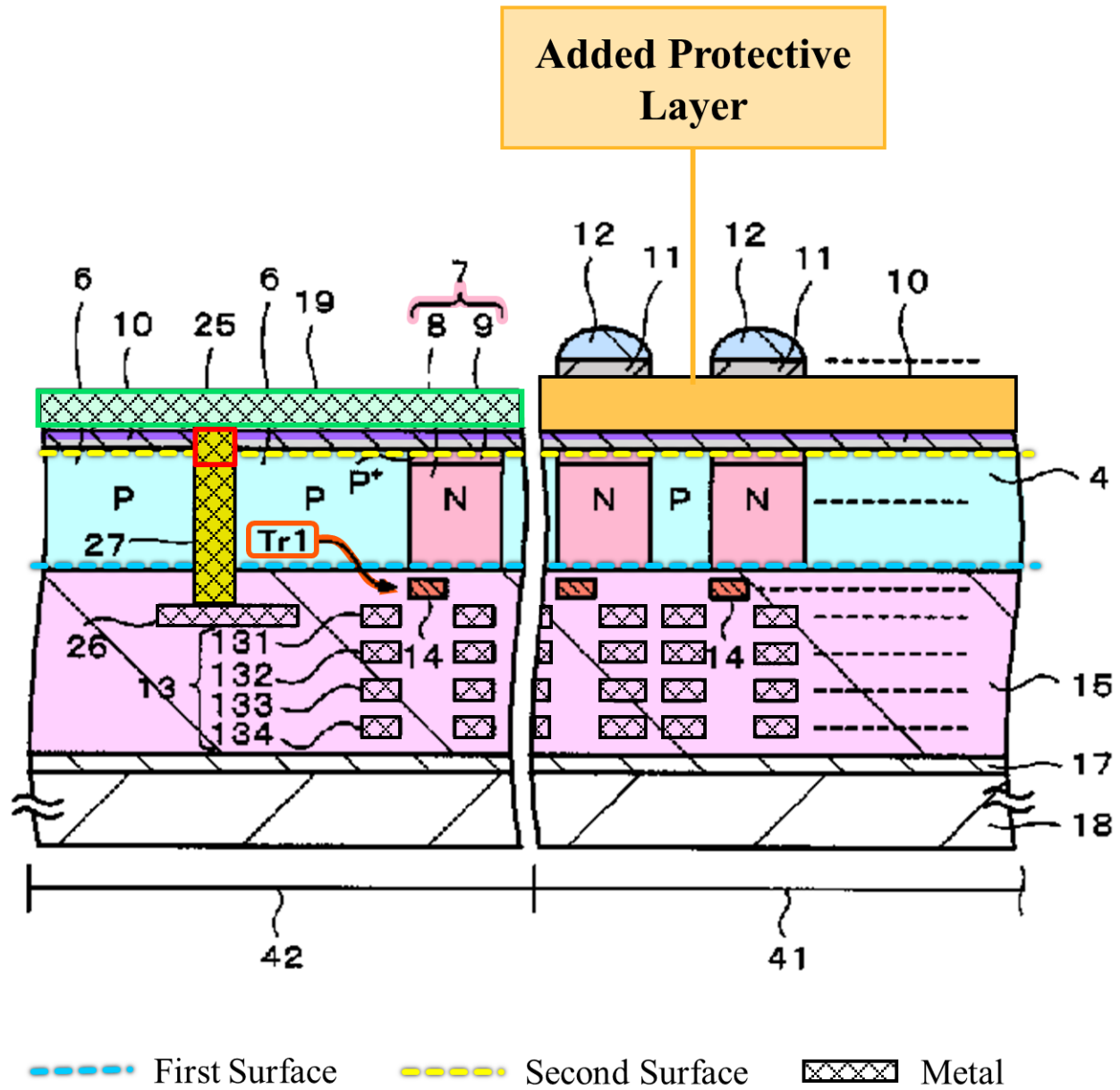
Yanagida-1 teaches “a color filter 11 is formed via an antireflective film (oxide film and nitride film) 10.” Yanagida-1, [0026]. Similarly, as shown below, Yanagida-2 also teaches a continuous protective layer 110 formed on the anti-reflection film 90 on the surface of the substrate. Yanagida-2, [0034].



POSAs would have been motivated to combine the protective layer taught in Yanagida-2 with the color filter 11 in Yanagida-1 to improve efficiency and

passivation and to increase the quantity of photons absorbed in the photodiode.

Guidash, ¶233.



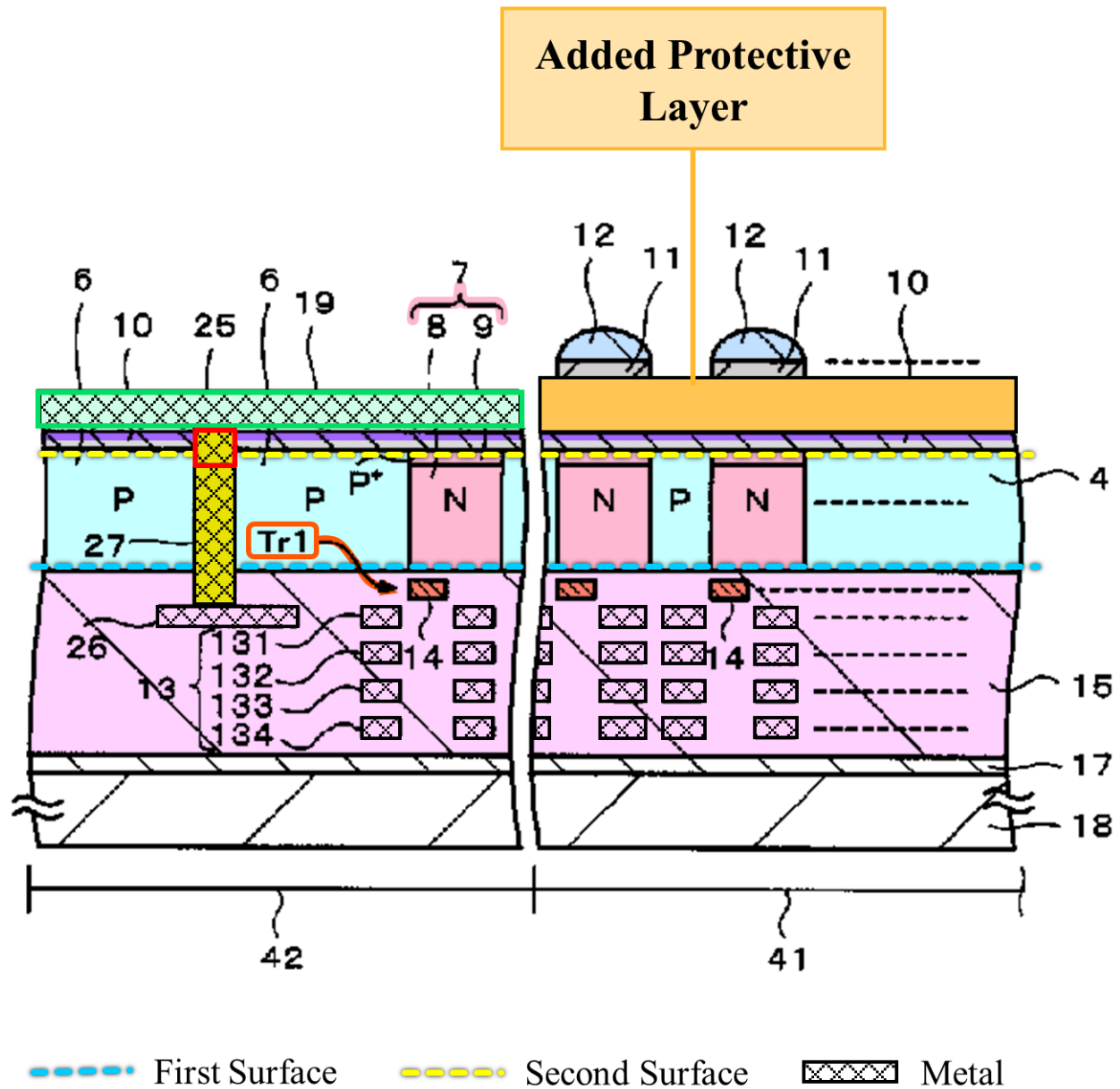
As such, the combination of Yanagida-1 and Yanagida-2 render this element obvious.

2. Claim [4B] – “a micro-lens formed on the protective layer in a region corresponding to the photodiode area.”

Yanagida-1 teaches “on-chip lenses 12 are formed on the color filter 11 at the positions corresponding to the photoelectric conversion elements 7.” Yanagida-1, [0026]. Similarly, Yanagida-2 teaches a micro-lens formed over the protective layer. Specifically, Yanagida-2 states that “[o]n the protective film 110, a color filter 111 is formed to pass only light in a desired wavelength region. In addition, on the color filter 111, an on-chip lens 112 is formed to focus the incident light onto the photodiode 21.” Yanagida-2, [0035].

As previously discussed *supra* §XIII.A, POSAs would have been motivated to combine the teachings of Yanagida-1 and Yanagida-2 to form a protective layer on the antireflective film. Guidash, ¶236.

Specifically, Yanagida-2’s protective film 110 is formed on Yanagida-1’s antireflective film 12 in the same manner Yanagida-2 discloses forming these layers “on the anti-reflection film 90” (Yanagida-2, [0034]). With the introduction of the protective film to cover it, Yanagida-1’s on-chip lenses 12 is positioned on the protective film 110 with intervening color filters 11 in a region corresponding to the photodiode area—*i.e.*, over the region of the substrate in which photodiode PD is formed—in the Metal-Yanagida-1-Yanagida-2 Sensor (below), thereby meets [4B]. Guidash, ¶236.



POSAs would have understood that the on-chip lenses in Yanagida-1 may be formed over the protective layer on the antireflective film as seen above. Guidash, ¶237. Further, forming the micro-lens over a protective layer better passivates the sensor. *Id.* As such, this element is rendered obvious over Yanagida-1 in view of Yanagida-2.

XIV. NO BASIS EXISTS FOR DISCRETIONARY DENIAL

A. Discretionary Denial Not Warranted Under Section 314(a)

The Texas Litigation does not justify denying institution under the *Fintiv* factors.

1. Factor 1: Potential for litigation stay

Factor 1 is neutral, as no party has requested a stay. *Autostore Sys. v. Ocado Innovation Ltd.*, IPR2022-00673, Paper 7, 9-10 (PTAB Sept. 14, 2022).

2. Factor 2: Trial date relative to FWD deadline

Per the Office’s recent memorandum⁶ (“Memo”), the PTAB considers “median time from filing to disposition of the civil trial for the district in which the parallel litigation resides.” Here that is 24.5 months, projecting trial in June 2024—after the anticipated date for a final written decision. This factor therefore favors institution, notwithstanding the slightly earlier (March 2024) trial date currently scheduled. *Apple v. Scramoge Tech.*, IPR2022-00573, Paper 12, 8-9 (PTAB Sept. 13, 2022) (citing median statistics and instituting review, notwithstanding earlier scheduled trial).

⁶ https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

3. Factor 3: Investment in parallel proceedings

The “investment” factor favors institution because the claim construction hearing in the Texas Litigation is not scheduled until September 6, 2023, and “the parties have not begun expert discovery or work on dispositive motions.” *Autostore*, IPR2022-00673, Paper 7, 11-12.

4. Factor 4: Issue Overlap

The “issue overlap” factor favors institution because Petitioner stipulates that, should the Board institute review, Petitioner and the other defendants will not rely upon any invalidity grounds based on Sumi, Shiraiwa, and/or Yanagida-1 (*i.e.*, the primary references herein). *Sand Revolution II v. Cont’l Intermodal Group-Trucking*, IPR2019-01393, Paper 24, 11–12 (PTAB June 16, 2020) (informative).

5. Factor 5: Parties

The “parties” factor is neutral because “there is uncertainty as to whether the district court will go to trial before the final written decision is due in this proceeding.” *Samsung Elecs. v. Jawbone Innovations*, IPR2022-00630, Paper 10, 13-14, 17 (PTAB Sept. 13, 2022) (citing median time-to-trial).

6. Factor 6: Other considerations

Petitioner presents a “meritorious” challenge “in which the evidence, if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence.” *Nokia of Am. Corp. v. TQ Delta*, IPR2022-00664, Paper 10, 8-9 (PTAB Sept. 27, 2022) (quoting Memo).

Both Sumi (Grounds 1-4) and Yanagida-1 (Grounds 5-6) confirm that the purported point of novelty suggested during prosecution was well known in the art.

B. Discretionary Denial Not Warranted Under Section 325(d)

The Petition asserts substantial new, noncumulative prior art and arguments. The Examiner never considered the claims in view of Sumi, Shiraiwa, Yanagida-1, or Yanagida-2. The first *Advanced Bionics* step is not met. *Advanced Bionics v. Med-El Elektromedizinsche Gerate*, IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020) (precedential).

1. The References Cited Were Not “Presented to the Office”

None of the references relied upon in the Petition was before the Office during prosecution of the ’143 patent except for a Japanese-language version of Yanagida-1 and an English translation of Yanagida-1’s Abstract. Ex. 1002, 71-123. The English translation of the Abstract fails to disclose several elements disclosed by Yanagida-1, including at least, (1) the connection via metal with a projection part, (2) the insulation layer (*i.e.*, the oxide film in the antireflective layer), (3) a metal pad, and (4) the thickness of the insulation layer being less than the height of the projection part. Guidash, ¶45. The English translation of the Abstract is not cumulative of Yanagida-1 itself, which the Examiner never cited or otherwise discussed.

This Petition’s other references were not presented in any form. Where several grounds “challenge[] the patent with a combination of references...not previously presented to the Office,...part one of the *Advanced Bionics* framework” is unmet, and §325(d) denial is inappropriate. *Align Tech. v. 3Shape A/S*, IPR2021-01309, Paper 11, 15 (Feb. 9, 2022).

2. Even if Yanagida-1 Was “Presented to the Office,” the Office Made a Material Error by Overlooking Its Impact

Even if the Board reached part two of *Advanced Bionics* and focused on Yanagida-1, to the extent the Examiner even considered Yanagida-1, “specific teachings of [Yanagida-1] impact[ing] patentability of the challenged claims” were “misapprehend[ed] or overlook[ed].” *Cellco P’ship v. Huawei Device Co.*, IPR2020-01117, Paper 10, 12 (PTAB Feb. 3, 2021). The “fact that [Yanagida-1 was] not the basis of rejection weighs strongly against exercising [the Board’s] discretion to deny institution under 35 U.S.C. § 325(d).” *Id.*, 13.

The Petition is supported by an English translation of the entirety of Yanagida-1, and a new expert declaration (Guidash) explaining how POSAs would have understood Yanagida-1. This “new non-cumulative evidence” weighs against discretionary denial. *Puma North America v. Nike*, IPR2019-01058, Paper 10, 19 (PTAB Oct. 31, 2019). For these reasons, discretionary denial under § 325(d) is not warranted.

XV. CONCLUSION

The Board should institute review and cancel claims 1-4 of the '143 patent.

Dated: December 22, 2022

Respectfully submitted,
Sony Group Corporation

/Randy J. Pritzker/

Randy J. Pritzker, Reg. No. 35,986

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (E)(4)

I certify that on December 22, 2022, I will cause a copy of the foregoing document, including any exhibits or appendices filed therewith, to be served via Overnight FedEx at the following correspondence address of record for the patent:

Farjami & Farjami LLP
26522 La Alameda Avenue, Suite 360
Mission Viejo, CA
92691

Date: December 22, 2022

/MacAulay Rush/
MacAulay Rush
Paralegal
WOLF, GREENFIELD & SACKS, P.C.

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,942 words excluding a table of contents, a table of authorities, Mandatory Notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing, but including annotations added to figures. Petitioner has relied on the word count feature of the word processing system used to create this paper in making this certification, manually adding to that the number of words present in annotations to figures.

Date: December 22, 2022

/MacAulay Rush/
MacAulay Rush
Paralegal
WOLF, GREENFIELD & SACKS, P.C.