IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

VISIONX TECHNOLOGIES, LLC Plaintiff, v. SONY GROUP CORPORATION, SONY CORPORATION, SONY SEMICONDUCTOR MANUFACTURING CORPORATION, AND SONY SEMICONDUCTOR SOLUTIONS CORPORATION. Defendants.	Civil Action No. 2:22-CV-00178-RSP

DEFENDANTS' INVALIDITY CONTENTIONS AND IDENTIFICATION OF DOCUMENT PRODUCTION ACCOMPANYING DISCLOSURE

Pursuant to the Court's Amended Docket Control Order (Dkt. No. 31) and the Rules of Practice for Patent Cases for the Eastern District of Texas ("Patent Rules" or "P.R."), Defendants Sony Group Corporation ("SGC"), Sony Corporation ("SC"), Sony Semiconductor Manufacturing Corporation ("SSMC"), and Sony Semiconductor Solutions Corporation ("SSSC") (collectively "Defendants" or "Sony") hereby disclose their Invalidity Contentions and provide their corresponding document production. Sony contends that each of the claims identified by Plaintiff VisionX Technologies ("VisionX") in VisionX's Disclosure of Asserted Claims and Infringement Contentions and Identification of Document Production Accompanying Disclosure pursuant to P.R. 3-1 and 3-2 is invalid under one or more of 35 U.S.C. §§ 102, 103, and 112.[1]

[1] All citations to title 35 of the U.S. Code are to pre-AIA versions unless otherwise noted.

Pat. Owner VisionX Exhibit 2009
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I. GENERAL STATEMENTS AND OBJECTIONS

A. Asserted Claims

On September 8, 2022, VisionX served Sony with Infringement Contentions alleging infringement of U.S. Patent No. 7,867,808 ("the '808 Patent"); U.S. Patent No. 7,868,366 ("the '366 Patent"); and U.S. Patent No. 8,035,143 ("the '143 Patent") (collectively, the "Asserted Patents").

VisionX alleges that Sony infringes:

- Claims 1, 2 and 4–9 of the '808 Patent (collectively the "'808 Patent Asserted Claims");
- Claims 1, 2 and 4–8 of the '366 Patent (collectively the "'366 Patent Asserted Claims"); and
- Claims 1–4 of the '143 Patent (collectively the "'143 Patent Asserted Claims").

The '808 Patent Asserted Claims, the '366 Patent Asserted Claims, and the '143 Patent Asserted Claims are together referenced herein as the "Asserted Claims."

Pursuant to the Patent Rules, Sony does not provide any invalidity contentions regarding nonasserted claims. In the event that the Court permits VisionX to assert additional claims against Sony in the future, Sony reserves its rights to disclose new or supplemental invalidity contentions regarding such claims.

Moreover, VisionX's Infringement Contentions are deficient in multiple respects and do not provide Sony with sufficient information to understand the specific accused features and components and the alleged factual and evidentiary bases for VisionX's allegations. Among other things, the Infringement Contentions lack the specificity required by Patent Rule 3-1, fail to properly identify accused instrumentalities, and do not adequately explain VisionX's infringement theory for numerous claim elements. VisionX has thus prejudiced Sony's ability to

understand, for purposes of preparing these Invalidity Contentions, what VisionX alleges to be the scope of the Asserted Claims.

To the extent the Patent Rules allow, or the Court allows, VisionX to modify any assertion or contention in VisionX's Infringement Contentions, or to present any new assertion or contention relevant to these Invalidity Contentions, Sony reserves the right to modify, amend, and/or supplement these Invalidity Contentions.

B. Claim Construction

The Court has not yet construed the Asserted Claims. Sony reserves the rights to modify, amend, and/or supplement these Invalidity Contentions in accordance with Patent Rule 3-6 following the Court's claim construction ruling or upon disclosure, alteration, or clarification by VisionX of its asserted claim construction to the extent permitted by this Court. Sony also reserves the rights to modify, amend, and/or supplement these Invalidity Contentions in response to any proposed claim constructions or alleged supporting evidence offered by VisionX, any report from any expert witness for VisionX regarding claim construction issues, any claim construction briefing filed by VisionX, and any position taken by VisionX concerning claim construction, infringement, or validity issues.

To the extent these Invalidity Contentions reflect constructions of claim terms that may be consistent with or implicit in VisionX's Infringement Contentions, no inference is intended to be drawn, nor should any inference be drawn, that Sony agrees with such claim constructions.

Sony takes no position on any matter of claim construction in these invalidity contentions. Any statement herein describing or tending to describe any claim element is provided solely for the purpose of understanding the relevant prior art. Sony expressly reserves the right to propose any claim construction they consider appropriate and/or to contest any claim construction they consider inappropriate. Nothing contained in these Invalidity Contentions or

any accompanying appendices or claim charts should be understood or deemed to be an express or implied admission or contention with respect to the proper constructions of any terms in the Asserted Claims. Moreover, nothing herein admits that any of Sony's accused products or services, or any of Sony's other products or services, infringe any of the Asserted Claims.

C. Ongoing Discovery and Disclosure

Discovery in this case is in its early stages and Sony's investigation, including Sony's search for prior art, is ongoing. Sony reserves the right to modify, amend, and/or supplement these Invalidity Contentions based on any supplemental materials received through the discovery process, to the extent permitted by this Court.

Sony bases these Invalidity Contentions on its current knowledge and understanding of the Asserted Patents, VisionX's Infringement Contentions, the prior art identified to date, and other facts and information available to date. Sony has not yet completed its investigation, collection of information, discovery, or analysis relating to this action, and additional discovery may require Sony to modify, amend, and/or supplement these contentions.

For example:

- VisionX has not produced all of the documents and information relevant to Sony's counterclaims and defenses, including but not limited to information concerning prior art products manufactured and sold by the original assignee of the Asserted Patents and/or partners of the original assignee.
- Sony has not yet deposed the named inventors of the Asserted Patents and/or other persons having potentially relevant documents and information, but may engage in this and other such discovery consistent with this Court's Orders.

Sony therefore reserves the right to modify, amend, and/or supplement these Invalidity Contentions including, without limitation, the prior art and grounds of invalidity set forth herein, to take into account information that may come to light as a result of these continuing efforts and any additional information obtained after the parties engage in claim construction, the Court construes any disputed terms from the Asserted Claims, or the parties complete full fact discovery.

Moreover, although VisionX has asserted certain invention dates earlier than the corresponding alleged priority dates for particular Asserted Patents, the materials that VisionX produced with its disclosures under P.R. 3-1 and 3-2 fail to evidence the conception or reduction to practice of the applicable claimed inventions on or before the corresponding alleged priority date identified by VisionX pursuant to P.R. 3-1(e). P.R. 3-2(b) and the Court's Docket Control Order required that any such production be made no later than September 8, 2022. Thus, the Asserted Patents are not entitled to any date of invention earlier than their alleged effective filing dates, and Sony objects to VisionX alleging or providing evidence of any earlier date of invention. If VisionX is nevertheless permitted to assert an earlier date of invention for any of the Asserted Patents, Sony further reserves its right to modify, amend, and/or supplement its Invalidity Contentions, including, but not limited to their identification and production of prior art.

Further, Sony intends to pursue discovery to demonstrate earlier invention by other parties under 35 U.S.C. § 102(g)(2). Sony further intends to take discovery from VisionX and third parties on the issues of improper inventorship and/or derivation under 35 U.S.C. § 102(f), public use and/or the on-sale bar under 35 U.S.C. § 102(b), and/or applicants' failure to comply with 35 U.S.C. § 112. Sony further intends to take discovery from VisionX and third parties on

the issues of public use and/or the on-sale bar under 35 U.S.C. § 102(b). Sony therefore reserves all rights to modify, amend, and/or supplement these Invalidity Contentions if and when further information becomes available.

D. Prior Art Identification and Citation

Sony's prior art reference charts under P.R. 3-3(a) (attached hereto as Exhibits A-1 to A-19 concerning the '808 Patent Asserted Claims, Exhibits B-1 to B-7 concerning the '366 Patent Asserted Claims, and Exhibits C-1 to C-11 concerning the '143 Patent Asserted Claims) identify where in each alleged item of prior art each element of each Asserted Claim is found, citing particular teachings/disclosure of the referenced art as applied to features of the Asserted Patents. The citations are exemplary and not exclusive. Sony reserves the right to rely on uncited portions of the prior art references and on other publications and expert testimony that aids in understanding and interpreting the cited portions, that provides context for them, and as additional evidence that the prior art discloses a claimed feature.

A statement that a given prior art reference "discloses" a particular claim element includes express disclosures, inherent disclosures, and implicit disclosures taking into account the knowledge that persons of ordinary skill ("POSAs") and the inferences that POSAs would reasonably be expected to draw from the specific teachings of the prior art reference against the backdrop of such knowledge.

Sony also reserves the right to establish what was known to POSAs through other publications, products, and/or testimony. Further, Sony reserves the right to rely on uncited portions of the prior art references, other publications, and testimony to establish that a person of skill in the art would have been motivated to combine certain of the cited references so as to render the claims obvious. Where Sony cites to a figure or a figure reference numeral in an item

of prior art, Sony incorporates by reference the discussion and/or explication of such figure or feature referenced by the reference numeral.

Sony reserves the right to prove the invalidity of the Asserted Claims on bases other than those required to be disclosed in these disclosures and contentions pursuant to P.R. 3–3.

II. IDENTIFICATION OF PRIOR ART- LOCAL PATENT RULE 3-3(A)

Pursuant to P.R. 3-3, Sony identifies at least the following prior art references now known to them to anticipate and/or render obvious the Asserted Claims, either expressly, implicitly, or inherently as understood by a person having ordinary skill in the art. The alignment of these contentions with particular sections of 35 U.S.C. § 102 is based upon currently available information and subject to revision as further information becomes available in discovery. For example, Sony contends that the references identified below qualify as prior art under 35 U.S.C. § 102(a), § 102(e),[2] or § 102(g)(2) if they do not qualify as prior art under 35 U.S.C. § 102(b). Sony also contends that any references identified below are pertinent to § 103 if they do not qualify as prior art under 35 U.S.C. § 102. *E.g., Geo M. Martin Co. v. Alliance Machine Sys. Int'l LLC*, 618 F.3d 1294 1305 (Fed. Cir. 2010) (emphasizing that independent inventions "within a comparatively short space of time" are "persuasive evidence" of obviousness); *Monarch Knitting Mach. Corp. v. Sulzer Morat GmbH*, 139 F.3d 877, 884 (Fed. Cir. 1998) (products did not qualify as prior art, yet were "relevant to obviousness as a secondary consideration"); *Newell v. Kenney*, 864 F.2d 757, 766 n.12 (Fed. Cir. 1988) (evidence admissible even though not "technically prior art"); *Thomas & Betts v. Litton Sys.*, 720 F.2d 1572, 1580-81

[2] Pursuant to P.R. 3-3, the tables below indicate "issue" and/or "publication" dates. This is without prejudice to Sony's right to rely upon applicable filing dates for § 102(e) references as indicated in the subsequent discussion below, in the accompanying exhibits, and/or on the face of the applicable patents or published patent applications along with any corresponding priority documents.

(Fed. Cir. 1983) (unpublished evidence was "properly used as indicators of the level of ordinary skill in the art to which the invention pertained"); *Medtronic Vascular v. Abbott Cardiovascular Sys.*, 614 F. Supp. 2d 1006, 1028 (N.D. Cal. 2009) (references that were not prior art were still "admissible as evidence of…the level of ordinary skill in the art").

For all of the reasons stated in Part I above, Sony reserves the right to supplement this identification as appropriate.

A. Prior Art to U.S. Patent No. 7,867,808

1. Prior Art Patents and Published Patent Applications

The following patents and published patent applications are prior art to the Asserted Claims of the '808 Patent under at least 35 U.S.C. §§ 102(a), (b), (e), (g), and/or 35 U.S.C. § 103, as indicated in the attached charts in Exhibits A-1 through A-19.

Reference	Short Name	Country of Origin	Filing Date	Date of Issue or Publication	Prior Art Basis	Bates range
U.S. Pat. No. 8,049,256	Guidash '256	U.S.	Oct. 4, 2007[3]	Nov. 1, 2011	§ 102(e)	SONYVX-PRIOR ART-0001126 – SONYVX-PRIOR ART-0001143
U.S. Pat. App. Pub. No. 20060091290	Yoshihara '290	U.S.	Oct. 18, 2005	May 4, 2006	§ 102(b)	SONYVX-PRIOR ART-0001224- SONYVX-PRIOR ART-0001238
U.S. Patent No. 7,781,715	Uya	U.S.	Sept. 17, 2007	Aug. 24, 2010	§ 102(e)	SONYVX-PRIOR ART-0001057- SONYVX-PRIOR ART-0001125
International Pat. Pub. No. WO2006129762 A1	Iwabuchi '762	WO (JP)	Jun. 1, 2006	Dec. 7, 2006	§ 102(b)	SONYVX-PRIOR ART-0001901- SONYVX-PRIOR ART-0002160
U.S. Patent No. 7,294,873	Suzuki	U.S.	Jul. 10, 2002	Nov. 13, 2007	§ 102(b)	SONYVX-PRIOR ART-0001041- SONYVX-PRIOR ART-0001056
U.S. Patent App. Pub. No. 2006/0043519	Ezaki '519	U.S.	Aug. 22, 2005	Mar. 2, 2006	§ 102(b)	SONYVX-PRIOR ART-0001212- SONYVX-PRIOR ART-0001223

[3] Guidash is entitled to an effective filing date of Oct. 5, 2006, the filing date of provisional application No. 60/828,259 (SONYVX-PRIOR ART-0000339-357).

Reference	Short Name	Country of Origin	Filing Date	Date of Issue or Publication	Prior Art Basis	Bates range
U.S. Patent App. Pub. No. 2006/0270096	Brady	U.S.	May 24, 2005	Nov. 30, 2006	§ 102(b)	SONYVX-PRIOR ART-0001281-SONYVX-PRIOR ART-0001295
U.S. Patent No. 6,809,008	Holm '008	U.S.	Aug 28, 2003	Oct. 26, 2004	§ 102(b)	SONYVX-PRIOR ART-0000985-SONYVX-PRIOR ART-0001009
U.S. Patent App. Pub. No. 2007/0018075	Cazaux	U.S.	Jul. 20, 2006	Jan. 25, 2007	§ 102(b)	SONYVX-PRIOR ART-0001296-SONYVX-PRIOR ART-0001304
U.S. Patent App. Pub. No. 2006/0214249	Nam	U.S.	Mar 27, 2006	Sept. 28, 2006	§ 102(b)	SONYVX-PRIOR ART-0001239-SONYVX-PRIOR ART-0001259
U.S. Patent App. Pub. No. 2007/0023801	Hynecek '801	U.S.	May 5, 2006	Feb. 1, 2007	§ 102(b)	SONYVX-PRIOR ART-0001305-SONYVX-PRIOR ART-0001318
U.S. Patent No. 7,217,589	Rhodes	U.S.	Dec. 13, 2004	May 15, 2007	§ 102(b)	SONYVX-PRIOR ART-0001023-SONYVX-PRIOR ART-0001040
U.S. Patent App. Pub. No. 2006/0244020	Lee '020	U.S.	Dec. 29, 2005	Nov. 2, 2006	§ 102(b)	SONYVX-PRIOR ART-0001260-SONYVX-PRIOR ART-0001280
U.S. Patent App. Pub. No. 2003/0038336	Mann	U.S.	Aug. 22, 2001	Feb. 27, 2003	§ 102(b)	SONYVX-PRIOR ART-0001886-SONYVX-PRIOR ART-0001898
JP Patent App. Pub. No. 2006-93587 A	Murayama	JP	Sept. 27, 2004	Apr. 6, 2006	§ 102(b)	SONYVX-PRIOR ART-0000510-SONYVX-PRIOR ART-0000534
U.S. Patent App. Pub. No. 2006/0197007	Iwabuchi '007	U.S.	Mar. 6, 2006	Sep.7, 2006	§ 102(b)	SONYVX-PRIOR ART-0001383-SONYVX-PRIOR ART-0001415
International Pat. Pub. No. WO 2006/109937	Lee '937	KR	Mar. 29, 2006	Oct. 19, 2006	§ 102(b)	SONYVX-PRIOR ART-0002368-SONYVX-PRIOR ART-0002386
U.S. Patent No. 5,695,810	Dery	U.S.	Sept. 23, 1997	June 13, 2000	§ 102(b)	SONYVX-PRIOR ART-0000925-SONYVX-PRIOR ART-0000936
U.S. Patent No. 8,507,960	Itonaga	U.S.	Nov. 27, 2006	Aug. 13, 2013	§ 102(e)	SONYVX-PRIOR ART-0001144-SONYVX-PRIOR ART-0001172
U.S. Patent Application Publication No. U.S. 2007/0128954 A1	Itonaga-954	U.S.	Nov. 27, 2006	June 7, 2007	§ 102(b)	SONYVX-PRIOR ART-0002292-SONYVX-PRIOR ART-0002321
U.S. Patent No. 6,590,242	Kozuka	U.S.	Feb. 24, 2000	July 8, 2003	§ 102(b)	SONYVX-PRIOR ART-0000937-SONYVX-PRIOR ART-0000984

Reference	Short Name	Country of Origin	Filing Date	Date of Issue or Publication	Prior Art Basis	Bates range
U.S. Patent Pub. No. 2005/0285215A1	Lee '215	U.S.	Feb. 22, 2005	Dec. 29, 2005	§ 102(b)	SONYVX-PRIOR ART-0001319-SONYVX-PRIOR ART-0001351
U.S. Patent No. 6,861,686	Lee '686	U.S.	Aug. 5, 2003	Mar. 1, 2005	§ 102(b)	SONYVX-PRIOR ART-0000762-SONYVX-PRIOR ART-0000806
JP Patent App. Pub. No. 2006303385A	Masagaki	JP	Apr. 25, 2005	Nov. 2, 2006	§ 102(b)	SONYVX-PRIOR ART-0000678-SONYVX-PRIOR ART-0000704
U.S. Patent Pub. No. 2006/0183265A1	Oh	U.S.	Oct. 5, 2005	Aug. 17, 2006	§ 102(b)	SONYVX-PRIOR ART-0001352-SONYVX-PRIOR ART-0001382
JP Patent App. Pub. No. 2005-353996A	Shiraiwa	JP	Aug. 25, 2006	Mar. 1, 2007	§ 102(b)	SONYVX-PRIOR ART-0000535-SONYVX-PRIOR ART-0000559
U.S. Patent Pub. No. 2006/0094151A1	Sumi	U.S.	Oct. 28. 2005	May 4, 2006	§ 102(b)	SONYVX-PRIOR ART-0000844-SONYVX-PRIOR ART-0000871
U.S. Patent Pub. No. 2004/0235266 A1	Tong '266	U.S.	May 19, 2003	Nov. 25, 2004	§ 102(b)	SONYVX-PRIOR ART-0000901-SONYVX-PRIOR ART-0000924
U.S. Patent No. 6,902,987	Tong '987	U.S.	Feb. 16, 2000	June 7, 2005	§ 102(b)	SONYVX-PRIOR ART-0000872-SONYVX-PRIOR ART-0000900
U.S. Patent No. 6,127,697	Guidash '697	U.S.	Nov. 14, 1997	Oct. 3, 2000	§ 102(b)	SONYVX-PRIOR ART-0002398-SONYVX-PRIOR ART-0002401
U.S. Pat. App. Publ. No. 2004/0157407	Tong '407	U.S.	Feb. 7, 2003	Aug. 12, 2004	§ 102(b)	SONYVX-PRIOR ART-0002346-SONYVX-PRIOR ART-0002367
U.S. Pat. App. Publ. No. 2003/0211705	Tong '705	U.S.	June 13, 2003	Nov. 13, 2003	§ 102(b)	SONYVX-PRIOR ART-0002322-SONYVX-PRIOR ART-0002345
U.S. Patent App. Pub. No. US 2005/0161795 A1	Tong '795	U.S.	Mar 22, 2005	July 28, 2005	§ 102(b)	SONYVX-PRIOR ART-0002206-SONYVX-PRIOR ART-0002225

2. Other Prior Art Publications

The following publications are prior art to the Asserted Claims of the '808 Patent under

at least 35 U.S.C. §§ 102(a), (b), (e), (g), and/or 35 U.S.C. § 103, as indicated in the attached charts in Exhibits A-1 through A-19.

Title and Author/Publisher (if known)	Short Name	Date of Publication	Prior Art Basis	Bates Range
Gambino, J., et al., "CMOS Imager with Copper Wiring and Lightpipe," Conference Proceedings at the 2006 International Electron Devices Meeting (IEEE)	Gambino	2006	§ 102(b)	SONYVX-PRIOR ART-0000674-SONYVX-PRIOR ART-0000677
B. Pain et al., "A Back-Illuminated Megapixel CMOS Image Sensor," in *Proceedings IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, pp. 35-38, 2005	Pain2005	2005	§ 102(b)	SONYVX-PRIOR ART-0000807-SONYVX-PRIOR ART-0000822
Supplemental Material to Suntharalingam, Vyshnavi, "Megapixel CMOS Image Sensor Fabricated in Three-Dimensional Integrated Circuit Technology," 2005 IEEE International Solid-State Circuits Conference (IEEE)	Suntharali ngam	2005	§ 102(b)	SONYVX-PRIOR ART-0000560-SONYVX-PRIOR ART-0000595
V. Suntharalingam et al., "Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology," ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005, 2005, pp. 356-357 Vol. 1, doi: 10.1109/ISSCC.2005.1494016 ("ISSCC 2005").	ISSCC 2005	2005	§ 102(b)	SONYVX-PRIOR ART-0001899-SONYVX-PRIOR ART-0001900
Patti, R.S., "Three-Dimensional Integrated Circuits and the Future of the System-on-Chip Designs." Proceedings of the IEEE (IEEE)	Patti-IEEE	June 2006	§ 102(b)	SONYVX-PRIOR ART-0000823-SONYVX-PRIOR ART-0000833
S.H. Christiansen et al. "Wafer Direct Bonding: From Advanced Substrate Engineering to Future Applications in Micro/Nanoelectronics," Proceedings of the IEEE, vol. 94, no. 10, pp. 2060-2106 (2006).	Christians en	Dec. 2006	§ 102(b)	SONYVX-PRIOR ART-0000623-SONYVX-PRIOR ART-0000669
Burns, James, et al., A Wafer-Scale 3-D Circuit Integration Technology, Transactions on Electronic Devices (IEEE)	Burns	October 2006	§ 102(b)	SONYVX-PRIOR ART-0000613 SONYVX-PRIOR ART-0000622
Balcerak, Raymond, et al, "Progress in the development of vertically integrated sensor arrays." Proceedings of SPIE	Balcerak	May 2005	§ 102(b)	SONYVX-PRIOR ART-0000604-SONYVX-PRIOR ART-0000612

Title and Author/Publisher (if known)	Short Name	Date of Publication	Prior Art Basis	Bates Range
V. Dragoi and P. Lindner. "Plasma Activated Wafer Bonding of Silicon: In Situ and Ex Situ Processes," ECS Transactions, vol. 3, no. 6, pp. 147-154 (2006)	Dragoi	2006	§ 102(b)	SONYVX-PRIOR ART-0000596-SONYVX-PRIOR ART-0000603
A. Fan et al. "Copper Wafer Bonding," Electrochemical and Solid-State Letters, vol. 2, no. 10, pp. 534-536 (1999)	Fan	1999	§ 102(b)	SONYVX-PRIOR ART-0000670-SONYVX-PRIOR ART-0000673
Gambino, J., et al., Optimization of Cu Interconnect Layers for CMOS Image Sensor Technology, Conference Proceedings AMC XXI (Materials Research Society, "MRS")	Gambino2	Sept. 2005	§ 102(b)	SONYVX-PRIOR ART-0001789-SONYVX-PRIOR ART-0001815
T.H. Kim et al. "Room temperature Cu-Cu direct bonding using surface activated bonding method," J. Vacuum Science & Technology A, vol. 21, no. 2, pp. 449-453 (2003)	Kim (2003)	Feb. 11, 2003	§ 102(b)	SONYVX-PRIOR ART-0000705-SONYVX-PRIOR ART-0000710
T. Suga et al. "Surface Activated Bonding for New Flip Chip and Bumpless Interconnect Systems," in 52nd Electronic Components and Technology Conference 2002 (Cat. No. 02CH37345), pp. 105-111 (2002)	Suga	2002	§ 102(b)	SONYVX-PRIOR ART-0000837-SONYVX-PRIOR ART-0000843
Garrou, Handbook of 3D Integration	Garrou	2008		SONYVX-PRIOR ART-0002402-SONYVX-PRIOR ART-0002453
Schaper, L., Architectural Implications and Process Development of 3-D VLSI Z-Axis Interconnects Using Through Silicon Vias, IEEE Transactions on Advanced Packaging, Vol. 28, No. 3, August 2005	Schaper	2005	§ 102(b)	SONYVX-PRIOR ART-0002387-SONYVX-PRIOR ART-0002397
Horn, S., Vertically-integrated sensor arrays - VISA, Proc. of SPIE Vol. 5406, pp. 332-340	Horn	2004	§ 102(b)	SONYVX-PRIOR ART-0002454-SONYVX-PRIOR ART-0002462
Kavusi, S., Architectures for High Dynamic Range, His Speed Image Sensor Readout Circuits, Dept. of Electrical Eng., Stanford University, Stanford, CA	Kavusi	2006	§ 102(b)	SONYVX-PRIOR ART-0002463-SONYVX-PRIOR ART-0002468

3. Items Offered for Sale or Publicly Used or Known

The following items offered for sale or publicly used or known are prior art to the

Asserted Claims of the ’808 Patent under at least 35 U.S.C. §§ 102(a), (b), (g), and/or 35 U.S.C. § 103.

Item	Short Name	Date of Offer, Use, and/or Knowledge	Identity of the Relevant Person or Entity	Prior Art Basis
Tezzaron 3D CMOS Image Sensor	Tezzaron Sensor	At least as early as April, 2004	Tezzaron Robert Patti	§ 102(b) § 102(g)
DARPA Vertically Integrated Sensor Array Program (“VISA”) Focal Plane Array demonstrated by Lincoln Laboratory	VISA Array – Lincoln Lab	At least as early as 2005	MIT Lincoln Laboratory	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Raytheon Vision Systems and State University of New York at Albany	VISA Array – Raytheon/SUNY	At least as early as 2005	Raytheon SUNY at Albany	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Rockwell Scientific	VISA Array – Rockwell	At least as early as 2005	Rockwell Scientific	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by DRS Infrared Technology and MCNC	VISA Array – DRS/MCNC	At least as early as 2005	DRS Infrared Technology MCNC Research & Development Institute	§ 102(b) § 102(g)

Item	Short Name	Date of Offer, Use, and/or Knowledge	Identity of the Relevant Person or Entity	Prior Art Basis
ISA Focal Plane Array demonstrated by HiDEC/University of Arkansas	VISA Array – HiDEC/University of Arkansas	At least as early as 2005	High Density Electronics Center University of Arkansas Leonard W. Schaper Susan L. Burkett Silke Spiesshoefer Gowtham V. Vangara Ziaur Rahman Swetha Polamreddy	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Ziptronix	VISA Array – Ziptronix	At least as early as 2005	Ziptronix	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by RTI International	VISA Array – RTI	At least as early as 2005	RTI International	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Stanford University	VISA Array – Stanford	At least as early as 2006	Stanford University Abbas El Gamal Bruce A. Wooley Sam Kavusi Sang-Min Lee Kunal Ghosh	§ 102(b) § 102(g)
Neuromorphic Vision Chip demonstrated by Tohoku University	Tohoku 3D Imager	At least as early as 2001	University of Tohoku M. Koyanagi Y. Nakagawa Kang-Wook Lee T. Nakamura Y. Yamada K. Inamura Ki-Tae Park	§ 102(b) § 102(g)

Item	Short Name	Date of Offer, Use, and/or Knowledge	Identity of the Relevant Person or Entity	Prior Art Basis
3D ROIC high energy physics detector demonstrated by Fermilab	Fermilab 3D Detector	At least as early as 2007	Fermilab Ray Yarema	§ 102(b) § 102(g)

See SONYVX-PRIOR ART-0001416-1424; SONYVX-PRIOR ART-0001441-1468; SONYVX-PRIOR ART-0001469-1505; SONYVX-PRIOR ART-0001506-1556; SONYVX-PRIOR ART-0001569; and SONYVX-PRIOR ART-0002417-0002440 (concerning Tezzaron) and SONYVX-PRIOR ART-0000604-612; SONYVX-PRIOR ART-0002441-0002452; SONYVX-PRIOR ART-0002387-0002397; SONYVX-PRIOR ART-0002454-0002462; and SONYVX-PRIOR ART-0002463-0002468 (concerning VISA Array).

4. Prior Art Under § 102(f)

Sony reserves the right, to the extent permitted by the Court and the applicable statutes and rules, to assert that the asserted claims are invalid under 35 U.S.C. § 102(f) in the event Sony obtains additional evidence that the named inventor of the ’808 patent did not invent (either alone or in conjunction with others) the subject matter claimed in the ’808 patent. Should Sony obtain such evidence, it will provide the name of the person(s) from whom, and the circumstances under which, the invention or any part of it was derived as required under P.R. 3-3(a).

5. Prior Art Under § 102(g)

The items offered for sale or publicly used or known identified in § II.A.3 also constitute prior art under § 102(g)(2), with the persons, entities, and circumstances identified as in § II.A.3. Sony reserves the right, to the extent permitted by the Court and the applicable statutes and rules,

to assert that the asserted claims are invalid under 35 U.S.C. § 102(g) for additional reasons in the event Sony obtains additional evidence that before VisionX's alleged invention, the inventions claimed in the '808 patent were made in this country by another inventor who had not abandoned, suppressed, or concealed it. Should Sony obtain such evidence, it will provide the identities of the person(s) or entities involved in and the circumstances surrounding the making of the invention before the patent applicant(s) under P.R. 3-3(a).

B. Prior Art to U.S. Patent No. 7,868,366

1. Prior Art Patents and Published Patent Applications

The following patents and published patent applications are prior art to the Asserted Claims of the '366 Patent under at least 35 U.S.C. §§ 102(a), (b), (e), (g), and/or 35 U.S.C. § 103, as indicated in the attached charts in Exhibits B-1 to B-6 and in Sony's IPR Petition concerning the '366 Patent provided in Exhibit B-7.

Reference	Short Name	Country of Origin	Filing Date	Date of Issue or Publication	Prior Art Basis	Bates Range
U.S. Pat. No. 5,695,810	Dublin	U.S.	Nov. 20, 1996	Dec. 9, 1997	§ 102(b)	SONYVX-PRIOR ART-0000411-SONYVX-PRIOR ART-0000422
U.S. Pat. No. 7,342,269	Yuzurihara	U.S.	Aug. 4, 2000	Mar. 11, 2008	§ 102(e)	SONYVX-PRIOR ART-0002186-SONYVX-PRIOR ART-0002205
U.S. Pat. No. 8,049,256	Guidash '256	U.S.	Oct. 4, 2007[4]	Nov. 1, 2011	§ 102(e)	SONYVX-PRIOR ART-0001126-SONYVX-PRIOR ART-0001143
U.S. Pat. App. Pub. No. 2003/0197228 Al	Okuda	U.S.	Feb.27, 2003	Oct. 23, 2003	§ 102(b)	SONYVX-PRIOR ART-0002161-SONYVX-PRIOR ART-0002187
U.S. Pat. App. Pub. No. 2005/0012166 A1	Choi	U.S.	June 16, 2004	Jan. 20, 2005	§ 102(b)	SONYVX-PRIOR ART-0000423-SONYVX-PRIOR ART-0000455

[4] Guidash '256 is entitled to an effective filing date of Oct. 5, 2006, the filing date of provisional application No. 60/828,259 (SONYVX-PRIOR ART-0000339-357).

Reference	Short Name	Country of Origin	Filing Date	Date of Issue or Publication	Prior Art Basis	Bates Range
U.S. Pat. App. Pub. No. 2005/0029643 A1	Koyanagi	U.S.	Nov. 5, 2002	Feb. 10, 2005	§ 102(b)	SONYVX-PRIOR ART-0001173-SONYVX-PRIOR ART-0001211
U.S. Pat. App. Pub. No. 2006/0113622 A1	Adkisson	U.S.	Nov. 30, 2004	June 1, 2006	§ 102(b)	SONYVX-PRIOR ART-0000456-SONYVX-PRIOR ART-0000481
U.S. Pat. Appl. Pub. No. 2008/0087921 A1	Yu	U.S.	Oct. 3, 2006	April 17, 2008	§ 102(e)	SONYVX-PRIOR ART-0000482-SONYVX-PRIOR ART-0000509
Korean Pat. No. 10-0644020	Pyo2	KR	Dec. 30, 2004	Nov. 10, 2006	§ 102(b)	SONYVX-PRIOR ART-0000299-SONYVX-PRIOR ART-0000317
Korean Pat. No. 10-0664864	Yun	KR	Dec. 30, 2004	Jan. 3, 2007	§ 102(b)	SONYVX-PRIOR ART-0000231-SONYVX-PRIOR ART-0000263
Korean Pat. App. Pub. No. 10-2006-0077082	Lee '082	KR	Dec. 30, 2004	July 5, 2006	§ 102(b)	SONYVX-PRIOR ART-0000318-SONYVX-PRIOR ART-0000338
Korean Pat. App. Pub. No. 10-2006-0077132	Pyo	KR	Dec. 30, 2004	July 5, 2006	§ 102(b)	SONYVX-PRIOR ART-0000212-SONYVX-PRIOR ART-0000230
Japanese Pat. Pat. No. 3800335	Imaoka	JP	April 16, 2003	May 12, 2006	§ 102(b)	SONYVX-PRIOR ART-0000264-SONYVX-PRIOR ART-0000298
Japanese Pat. App. Pub. No. 2006-32497	Yanagida	JP	July 13, 2004	Feb. 2, 2006	§ 102(b)	SONYVX-PRIOR ART-0000393-SONYVX-PRIOR ART-0000410
Japanese Pat. App. Pub. No. 2006-339566	Yanagida2	JP	June 6, 2005	Dec. 14, 2006	§ 102(b)	SONYVX-PRIOR ART-0000181-SONYVX-PRIOR ART-0000211
Japanese Pat. App. Pub. No. 2001-339057	Koyanagi2	JP	May 30, 2000	Dec. 7, 2001	§ 102(b)	SONYVX-PRIOR ART-0001621-SONYVX-PRIOR ART-0001639
U.S. Patent No. 6,576,550	Brase	U.S.	June 30, 2000	June 10, 2003	§ 102(b)	SONYVX-PRIOR ART-0000358-SONYVX-PRIOR ART-0000370

2. Other Prior Art Publications

The following publications are prior art to the Asserted Claims of the ’366 patent under at least 35 U.S.C. §§ 102(a), (b), (e), (g), and/or 35 U.S.C. § 103, as indicated in the attached charts in Exhibits B-1 to B-6 and in Sony’s IPR Petition provided in Exhibit B-7.

Title and Author/Publisher (if known)	Short Name	Date of Publication	Prior Art Basis	Bates Range
Edelstein, D., Heidenreich, J., et al., Full copper wiring in a sub-0.25 µm CMOS ULSI technology. International Electron Devices Meeting Technical Digest (Electron Devices Society of IEEE)	Edelstein	1997	§ 102(b)	SONYVX-PRIOR ART-0001689-SONYVX-PRIOR ART-0001701
Quirk, Michael and Julian Serda, Semiconductor Manufacturing Technology (Prentice-Hall, Inc.)	Quirk	2001	§ 102(b)	SONYVX-PRIOR ART-0001702-SONYVX-PRIOR ART-0001788
Ramm, Peter, et al., InterChip Via Technology for Vertical System Integration, 2001 IEEE International Interconnect Technical Conference Technical Digest (IEEE)	Ramm	2001	§ 102(b)	SONYVX-PRIOR ART-0000834-SONYVX-PRIOR ART-0000836
Yadid-Pecht, Orly and Ralph Etienne-Cummings, CMOS Imagers: From Phototransduction to Image Processing (Kluwer Academic Publishers)	Yadid-Pecht	2004	§ 102(b)	SONYVX-PRIOR ART-0001816-SONYVX-PRIOR ART-0001885
Suntharalingam, Vyshnavi, “Megapixel CMOS Image Sensor Fabricated in Three-Dimensional Integrated Circuit Technology,” 2005 IEEE International Solid-State Circuits Conference (IEEE)	Suntharalingam	2005	§ 102(b)	SONYVX-PRIOR ART-0000560-SONYVX-PRIOR ART-0000595
Gambino, J., et al., “CMOS Imager with Copper Wiring and Lightpipe,” Conference Proceedings at the 2006 International Electron Devices Meeting (IEEE)	Gambino	2006	§ 102(b)	SONYVX-PRIOR ART-0000674-SONYVX-PRIOR ART-0000677

Title and Author/Publisher (if known)	Short Name	Date of Publication	Prior Art Basis	Bates Range
Gambino, J., et al., Optimization of Cu Interconnect Layers for CMOS Image Sensor Technology, Conference Proceedings AMC XXI (Materials Research Society, "MRS")	Gambino2	Sept. 2005	§ 102(b)	SONYVX-PRIOR ART-0001789-SONYVX-PRIOR ART-0001815
Patti, R.S., "Three-Dimensional Integrated Circuits and the Future of the System-on-Chip Designs." Proceedings of the IEEE (IEEE)	Patti-IEEE	June 2006	§ 102(b)	SONYVX-PRIOR ART-0000823-SONYVX-PRIOR ART-0000833
Burns, James, et al., A Wafer-Scale 3-D Circuit Integration Technology, Transactions on Electronic Devices (IEEE)	Burns	October 2006	§ 102(b)	SONYVX-PRIOR ART-0000613-SONYVX-PRIOR ART-0000622
Doering, Robert and Yoshio Nishi, Handbook of Semiconductor Manufacturing Technology (CRC Press, Taylor & Francis Group, LLC)	Doering	2008	n/a	SONYVX-PRIOR ART-0001640-SONYVX-PRIOR ART-0001688
Annabelle Pratt, Overview of the Use of Copper Interconnects in the Semiconductor Industry (Advanced Energy Industries)	Pratt	2006	§ 102(b)	SONYVX-PRIOR ART-0000371-SONYVX-PRIOR ART-0000392

3. Items Offered for Sale or Publicly Used or Known

The following items offered for sale or publicly used or known are prior art to the Asserted Claims of the '366 Patent under at least 35 U.S.C. §§ 102(a), (b), (g), and/or 35 U.S.C. § 103.

Item	Short Name	Date of Offer, Use, and/or Knowledge	Identity of the Relevant Person or Entity	Prior Art Basis
Tezzaron 3D CMOS Image Sensor	Tezzaron Sensor	At least as early as April, 2004	Tezzaron Robert Patti	§ 102(b) § 102(g)
DARPA Vertically Integrated Sensor Array Program ("VISA") Focal Plane Array demonstrated by Lincoln Laboratory	VISA Array – Lincoln Lab	At least as early as 2005	MIT Lincoln Laboratory	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Raytheon Vision Systems and State University of New York at Albany	VISA Array – Raytheon/SUNY	At least as early as 2005	Raytheon SUNY at Albany	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Rockwell Scientific	VISA Array – Rockwell	At least as early as 2005	Rockwell Scientific	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by DRS Infrared Technology and MCNC	VISA Array – DRS/MCNC	At least as early as 2005	DRS Infrared Technology MCNC Research & Development Institute	§ 102(b) § 102(g)

Item	Short Name	Date of Offer, Use, and/or Knowledge	Identity of the Relevant Person or Entity	Prior Art Basis
VISA Focal Plane Array demonstrated by HiDEC/University of Arkansas	VISA Array – HiDEC/University of Arkansas	At least as early as 2005	High Density Electronics Center University of Arkansas Leonard W. Schaper Susan L. Burkett Silke Spiesshoefer Gowtham V. Vangara Ziaur Rahman Swetha Polamreddy	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Ziptronix	VISA Array – Ziptronix	At least as early as 2005	Ziptronix	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by RTI International	VISA Array – RTI	At least as early as 2005	RTI International	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Stanford University	VISA Array – Stanford	At least as early as 2006	Stanford University Abbas El Gamal Bruce A. Wooley Sam Kavusi Sang-Min Lee Kunal Ghosh	§ 102(b) § 102(g)
Neuromorphic Vision Chip demonstrated by Tohoku University	Tohoku 3D Imager	At least as early as 2001	University of Tohoku M. Koyanagi Y. Nakagawa Kang-Wook Lee T. Nakamura Y. Yamada K. Inamura Ki-Tae Park	§ 102(b) § 102(g)

Item	Short Name	Date of Offer, Use, and/or Knowledge	Identity of the Relevant Person or Entity	Prior Art Basis
3D ROIC high energy physics detector demonstrated by Fermilab	Fermilab 3D Detector	At least as early as 2007	Fermilab Ray Yarema	§ 102(b) § 102(g)

See SONYVX-PRIOR ART-0001416-1424; SONYVX-PRIOR ART-0001441-1468; SONYVX-PRIOR ART-0001469-1505; SONYVX-PRIOR ART-0001506-1556; SONYVX-PRIOR ART-0001569; and SONYVX-PRIOR ART-0002417-0002440 (concerning Tezzaron) and SONYVX-PRIOR ART-0000604-612; SONYVX-PRIOR ART-0002441-0002452; SONYVX-PRIOR ART-0002387-0002397; SONYVX-PRIOR ART-0002454-0002462; and SONYVX-PRIOR ART-0002463-0002468 (concerning VISA Array).

4. Prior Art Under § 102(f)

Sony reserves the right, to the extent permitted by the Court and the applicable statutes and rules, to assert that the asserted claims are invalid under 35 U.S.C. § 102(f) in the event Sony obtains additional evidence that the named inventor of the ’366 patent did not invent (either alone or in conjunction with others) the subject matter claimed in the ’366 patent. Should Sony obtain such evidence, it will provide the name of the person(s) from whom, and the circumstances under which, the invention or any part of it was derived as required under P.R. 3-3(a).

5. Prior Art Under § 102(g)

The item offered for sale or publicly used or known identified in § II.B.3 also constitutes prior art under § 102(g)(2), with the persons, entities, and circumstances identified as in § II.B.3. Sony reserves the right, to the extent permitted by the Court and the applicable statutes and rules,

to assert that the asserted claims are invalid under 35 U.S.C. § 102(g) for additional reasons in the event Sony obtains additional evidence that before VisionX's alleged invention, the inventions claimed in the '366 patent were made in this country by another inventor who had not abandoned, suppressed, or concealed it. Should Sony obtain such evidence, it will provide the identities of the person(s) or entities involved in and the circumstances surrounding the making of the invention before the patent applicant(s) under P.R. 3-3(a).

C. Prior Art to U.S. Patent No. 8,035,143

1. Prior Art Patents and Published Patent Applications

The following patents and published patent applications are prior art to the Asserted Claims of the '143 Patent under at least 35 U.S.C. §§ 102(a), (b), (e), (g), and/or 35 U.S.C. § 103.

Reference	Short Name	Country of Origin	Filing Date	Date of Issue or Publication	Prior Art Basis	Bates Range
U.S. Pat. No. 7,875,948	Hynecek '948	U.S.	October 21, 2008	January 25, 2011	§ 102(e)	SONYVX-PRIOR ART-0000042-SONYVX-PRIOR ART-0000063
U.S. Pat. Pub. No. 20060043438A1	Holm	U.S.	August 26, 2004	March 2, 2006	§ 102(b)	SONYVX-PRIOR ART-0000016-SONYVX-PRIOR ART-0000041
U.S. Pat. Pub. No. 20060076590A1	Pain	U.S.	September 13, 2005	April 13, 2006	§ 102(b)	SONYVX-PRIOR ART-0000116-SONYVX-PRIOR ART-0000131
U.S. Pat. Pub. No. 2006/0094151A1	Sumi	U.S.	October 28, 2005	May 4, 2006	§ 102(b)	SONYVX-PRIOR ART-0000844-SONYVX-PRIOR ART-0000871
U.S. Pat. Pub. No. 20060197007A1	Iwabuchi '007	U.S.	March 6, 2006	September 7, 2006	§ 102(b)	SONYVX-PRIOR ART-0001383-SONYVX-PRIOR ART-0001415
U.S. Pat. Pub. No. 20070048973A1	Koizumi	U.S.	Aug. 25, 2006	Mar. 1, 2007	§ 102(b)	SONYVX-PRIOR ART-0000094-SONYVX-PRIOR ART-0000112
U.S. Pat. Pub. No. 20070155044A1	Shim	U.S.	Dec. 19, 2006	July 5, 2007	§ 102(b)	SONYVX-PRIOR ART-0000162-SONYVX-PRIOR ART-0000169
U.S. Pat. Pub. No. 20080083939A1	Guidash '939	U.S.	Oct. 4, 2007	April 10, 2008	§ 102(b)	SONYVX-PRIOR ART-0002469-SONYVX-PRIOR ART-0002486
International Pat. Pub. No. WO2006129762A1	Iwabuchi '762	WO (JP)	June 1, 2006	Dec. 7, 2006	§ 102(b)	SONYVX-PRIOR ART-0001901-SONYVX-PRIOR ART-0002160
Japanese Pat. App. Pub. No. 2006-32497	Yanagida-1	JP	July 13, 2004	Feb. 2, 2006	§ 102(b)	SONYVX-PRIOR ART-0000393-SONYVX-PRIOR ART-0000410
Japanese Pat. Pub. No. 2006-339566	Yanagida-2	JP	June 6, 2005	Dec. 14, 2006	§ 102(b)	SONYVX-PRIOR ART-0000181-SONYVX-PRIOR ART-0000211
U.S. Patent No. 7,928,534	Hsu	U.S.	Dec. 31, 2008[5]	Apr. 19, 2011	§ 102(e)	SONYVX-PRIOR ART-0000170-SONYVX-PRIOR ART-0000180
U.S. Pat. Pub. No. 20070210395A1	Maruyama '395	U.S.	Feb. 22, 2007	Sept. 13, 2007	§ 102(b)	SONYVX-PRIOR ART-0001570-SONYVX-PRIOR ART-0001615
Japanese Pat. Pub. No. 2005-353996A	Shiraiwa	JP	Aug. 25. 2006	Mar. 1, 2007	§ 102(b)	SONYVX-PRIOR ART-0000535-SONYVX-PRIOR ART-0000559
International Patent Publication No. WO2007148891A1	Lee '891	WO (KR)	June 14, 2007	Dec. 27, 2007	§ 102(b)	SONYVX-PRIOR ART-0001425-SONYVX-PRIOR ART-0001440

2. Other Prior Art Publications

The following publications are prior art to the Asserted Claims of the ’143 Patent under at least 35 U.S.C. §§ 102(a), (b), (e), (g), and/or 35 U.S.C. § 103, as indicated in the attached charts in Exhibits C-1 to C-11.

Title and Author/Publisher (if known)	Short Name	Date of Publication	Prior Art Basis	Bates Range
Patti, R.S., “Three-Dimensional Integrated Circuits and the Future of the System-on-Chip Designs.” Proceedings of the IEEE, vol. 94, no. 6, pp. 1214-1224, 2006	Patti IEEE	June 2006	§ 102(b)	SONYVX-PRIOR ART-0000823-SONYVX-PRIOR ART-0000833
Ramm, Peter, et al., InterChip Via Technology for Vertical System Integration, 2001 IEEE International Interconnect Technical Conference Technical Digest, 160-162 (2001)	Ramm	2001	§ 102(b)	SONYVX-PRIOR ART-0000834-SONYVX-PRIOR ART-0000836
Morrow, P.R., et. al., “Three-Dimensional Wafer Stacking Via Cu-Cu Bonding Integrated With 65-nm Strained-Si/Low-k CMOS Technology.” IEEE Electron Device Letters, vol. 27, no. 5, pp. 335-337, 2006	Morrow	2006	§ 102(b)	SONYVX-PRIOR ART-0000113-SONYVX-PRIOR ART-0000115
Quirk, Michael and Julian Serda, Semiconductor Manufacturing Technology (Prentice-Hall, Inc.)	Quirk	2001	§ 102(b)	SONYVX-PRIOR ART-0001702-SONYVX-PRIOR ART-0001788
Presentation on FaStack® Technology 3D:Design to Volume, A Look at Various 3D Applications, Their Designs, and Ultimate Silicon Results, Tezzaron Semiconductor (June 15, 2005)	Tezzaron 1	June 15, 2005	§ 102(b)	SONYVX-PRIOR ART-0001469-SONYVX-PRIOR ART-0001505

[5] Hsu is entitled to an effective filing date of Oct. 9, 2008, the filing date of provisional application No. 61/104,186 (SONYVX-PRIOR ART-0000001- SONYVX-PRIOR ART-0000015).

Title and Author/Publisher (if known)	Short Name	Date of Publication	Prior Art Basis	Bates Range
Tezzaron Semiconductor, FaStack® Technology 3D:Design to Volume, A Look at Various 3D Applications, Their Designs, and Ultimate Silicon Results, 3D Architectures for Semiconductor Integration and Packaging (June 13-15, 2005)	Tezzaron 2	June 2005	§ 102(b)	SONYVX-PRIOR ART-0001506-SONYVX-PRIOR ART-0001556
Robert Patti, FaStack Technology, Tezzaron Semiconductor Corp. (Oct. 4, 2005)	Tezzaron 3	Oct. 4, 2005	§ 102(b)	SONYVX-PRIOR ART-0001441-SONYVX-PRIOR ART-0001468
Twenty Second International VLSI Multilevel Interconnection Conference Proceedings, VMIC Catalog No. 05 IMC – 040, 1-12 (Oct. 4-6, 2005)	Tezzaron 4	Oct. 2005	§ 102(b)	SONYVX-PRIOR ART-0001557-SONYVX-PRIOR ART-0001569
Gupta, S., et. al., 3D-IC Integration: Process and Results, 2005 VMIC Conference, 61-69 (Oct. 4, 2005)	Tezzaron 5	Oct. 4, 2005	§ 102(b)	SONYVX-PRIOR ART-0001416-SONYVX-PRIOR ART-0001424

3. Items Offered for Sale or Publicly Used or Known

The following items offered for sale or publicly used or known are prior art to the Asserted Claims of the ’143 Patent under at least 35 U.S.C. §§ 102(a), (b), (e), (g), and/or 35 U.S.C. § 103, as indicated in the attached charts in Exhibits C-7.

Item	Short Name	Date of Offer, Use, and/or Knowledge	Identity of the Relevant Person or Entity	Prior Art Basis
Tezzaron 3D CMOS Image Sensor	Tezzaron Sensor	At least as early as April, 2004	Tezzaron Robert Patti	§ 102(b) § 102(g)
DARPA Vertically Integrated Sensor Array Program (“VISA”) Focal Plane Array demonstrated by Lincoln Laboratory	VISA Array – Lincoln Lab	At least as early as 2005	MIT Lincoln Laboratory	§ 102(b) § 102(g)

Item	Short Name	Date of Offer, Use, and/or Knowledge	Identity of the Relevant Person or Entity	Prior Art Basis
VISA Focal Plane Array demonstrated by Raytheon Vision Systems and State University of New York at Albany	VISA Array – Raytheon/SUNY	At least as early as 2005	Raytheon SUNY at Albany	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Rockwell Scientific	VISA Array – Rockwell	At least as early as 2005	Rockwell Scientific	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by DRS Infrared Technology and MCNC	VISA Array – DRS/MCNC	At least as early as 2005	DRS Infrared Technology MCNC Research & Development Institute	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by HiDEC/University of Arkansas	VISA Array – HiDEC/University of Arkansas	At least as early as 2005	High Density Electronics Center University of Arkansas Leonard W. Schaper Susan L. Burkett Silke Spiesshoefer Gowtham V. Vangara Ziaur Rahman Swetha Polamreddy	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by Ziptronix	VISA Array – Ziptronix	At least as early as 2005	Ziptronix	§ 102(b) § 102(g)
VISA Focal Plane Array demonstrated by RTI International	VISA Array – RTI	At least as early as 2005	RTI International	§ 102(b) § 102(g)

Item	Short Name	Date of Offer, Use, and/or Knowledge	Identity of the Relevant Person or Entity	Prior Art Basis
VISA Focal Plane Array demonstrated by Stanford University	VISA Array – Stanford	At least as early as 2006	Stanford University Abbas El Gamal Bruce A. Wooley Sam Kavusi Sang-Min Lee Kunal Ghosh	§ 102(b) § 102(g)
Neuromorphic Vision Chip demonstrated by Tohoku University	Tohoku 3D Imager	At least as early as 2001	University of Tohoku M. Koyanagi Y. Nakagawa Kang-Wook Lee T. Nakamura Y. Yamada K. Inamura Ki-Tae Park	§ 102(b) § 102(g)
3D ROIC high energy physics detector demonstrated by Fermilab	Fermilab 3D Detector	At least as early as 2007	Fermilab Ray Yarema	§ 102(b) § 102(g)

See SONYVX-PRIOR ART-0001416-1424; SONYVX-PRIOR ART-0001441-1468; SONYVX-PRIOR ART-0001469-1505; SONYVX-PRIOR ART-0001506-1556; SONYVX-PRIOR ART-0001569; and SONYVX-PRIOR ART-0002417-0002440 (concerning Tezzaron) and SONYVX-PRIOR ART-0000604-612; SONYVX-PRIOR ART-0002441-0002452; SONYVX-PRIOR ART-0002387-0002397; SONYVX-PRIOR ART-0002454-0002462; and SONYVX-PRIOR ART-0002463-0002468 (concerning VISA Array).

4. Prior Art Under § 102(f)

Sony reserves the right, to the extent permitted by the Court and the applicable statutes and rules, to assert that the asserted claims are invalid under 35 U.S.C. § 102(f) in the event Sony obtains additional evidence that the named inventor of the ’143 patent did not invent (either

alone or in conjunction with others) the subject matter claimed in the ’143 patent. Should Sony obtain such evidence, it will provide the name of the person(s) from whom, and the circumstances under which, the invention or any part of it was derived as required under P.R. 3-3(a).

5. Prior Art Under § 102(g)

The item offered for sale or publicly used or known identified in § II.C.3 also constitutes prior art under § 102(g)(2), with the persons, entities, and circumstances identified as in § II.C.3. Sony reserves the right, to the extent permitted by the Court and the applicable statutes and rules, to assert that the asserted claims are invalid under 35 U.S.C. § 102(g) for additional reasons in the event Sony obtains additional evidence that before VisionX’s alleged invention, the inventions claimed in the ’143 patent were made in this country by another inventor who had not abandoned, suppressed, or concealed it. Should Sony obtain such evidence, it will provide the identities of the person(s) or entities involved in and the circumstances surrounding the making of the invention before the patent applicant(s) under P.R. 3-3(a).

III. ANTICIPATION AND OBVIOUSNESS REFERENCES- LOCAL PATENT RULE 3-3 (B) AND (C)

Each of the prior art references identified in Part II above and/or discussed in this Part either anticipates one or more of the Asserted Claims and/or renders obvious one or more of the Asserted Claims alone and/or when viewing in combination with other prior art references.

VisionX appears to contend in its infringement contentions that certain limitations of the Asserted Claims have a similar meaning, or encompass similar feature(s) and/or functions as other limitations in different claims. Thus, to the extent any prior art reference cited by Sony anticipates or renders obvious a particular limitation, it likewise anticipates or renders obvious any other limitations that VisionX contends have similar meaning or encompass similar features

or functions. Sony reserves the right to contend that each of the anticipatory references renders the claims obvious either in view of the reference alone or in combination with other references. The identification of any patent or patent application should be deemed an identification of any counterpart patent or application; the identification of any article or publication should be deemed a disclosure of any substantially similar article if published in some other form, or of any patent or patent application corresponding to such article or publication; and the identification of any patent, patent application or article should be deemed an identification of any product described therein.

Sony also reserves the right to rely upon parent or ancestor patents or patent applications (including provisional applications) to which any of the patents or patent applications listed in Exhibits A-1 to A-19, B-1 to B-7, or C-1 to C-11 claim priority.

Moreover, Sony reserves the right to rely on any references cited during prosecution of any of the Asserted Patents as well as any ancestors, descendants, or counterpart applications, whether in the United States or elsewhere in the world.

The cited portions of the prior art references are exemplary and representative of the content of the prior art references. They should be understood in the context of the reference as a whole, as understood by one of ordinary skill in the art. For example, a reference to a figure should be deemed to refer to the text describing the figure and vice-versa. To the extent that VisionX contends that a prior art reference does not expressly, inherently, or implicitly disclose a particular claim limitation, that claim would nonetheless have been obvious to POSAs at the time of the invention over the reference itself or by the combination of the prior art reference with one or more other prior art references that disclose, teach, or suggest those claim limitations. Sony cannot know which such elements VisionX may contend are so limited, and reserve the right to

propose additional obviousness combinations to address VisionX's contentions, if necessary. In addition, where a claim chart does not cite an express teaching of a particular limitation, Sony reserves the right to argue that such teaching is inherent in the reference and/or that the reference implicitly discloses the limitation given the inferences that a POSA would reasonably be expected to draw from the specific teachings of the prior art reference in light of a POSA's background knowledge.

In addition to the anticipatory references described in these Invalidity Contentions, the Asserted Claims are invalid based on obviousness under 35 U.S.C. § 103. In general, a claimed invention is unpatentable if the differences between it and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a); *Graham v. John Deere Co.*, 383 U.S. 1, 13-14 (1966).

Each prior art reference identified above and described in the charts attached in Exhibits A-1 to A-19, B-1 to B-7, or C-1 to C-11, either alone or in combination with other prior art, also renders the Asserted Claims invalid as obvious. In particular, each prior art reference may be combined with (1) information known to POSAs at the time of the alleged invention, (2) any of the other anticipatory prior art references, and/or (3) any of the additional prior art identified above and in the charts attached hereto. Specific combinations of prior art, by way of example, are provided below. In addition, Sony incorporates by reference each and every prior art reference of record in the prosecution of the Asserted Patents and related applications, including the statements made therein by the applicant, as well as the prior art discussed in the specifications of the Asserted Patents.

In view of the Supreme Court's *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 127 S.Ct. 1727, 1739 (2007) decision, the USPTO issued a set of Examination Guidelines. *See* Examination Guidelines for Determining Obviousness Under 35 U.S.C. § 103 in View of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.*, 72 Fed. Reg. 57,526 (Oct. 10, 2007). Those Guidelines summarized the *KSR* decision, and identified various rationales for finding a claim obvious, including those based on other precedents. Those rationales include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of known technique to improve similar devices (methods, or products) in the same way;
- applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- "obvious to try" – choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Id. at 57,529. These rationales are consistent with the Supreme Court's emphasis in *KSR* that "the results of ordinary innovation" from the perspective of POSAs are not patentable, and further that "[a] person of ordinary skill is also a person of ordinary creativity, not an automaton." *KSR*, 550 U.S. at 421, 427.

Sony contends that one or more of these rationales apply in considering the obviousness of the Asserted Claims. As discussed in more detail below and as demonstrated in the appended claim charts, the image sensor industry was actively pursuing a number of well-developed solutions in connection with known products and related fabrication methods pertinent to the subject matter of the Asserted Patents.

As the Supreme Court emphasized in *KSR*, issued patent claims may be determined to be invalid as obvious even without a teaching, suggestion, or motivation to combine particular references. Nevertheless, POSAs would have been motivated to combine each of the above-identified references with the others identified with respect to the same Asserted Patent. Sony contends that POSAs at the time the alleged inventions of the Asserted Claims were made, would have been motivated to combine the references disclosed herein in such a way to reach the alleged inventions. The teaching, suggestion, or motivation to combine these references, although not required, is found, explicitly or implicitly in one or more of at least the following: the knowledge or common sense of one of ordinary skill in the art; the prior art references themselves and/or the prior art as a whole, including interrelated teachings of multiple prior art references; the common fields of technology of the references; the subject matter acknowledged as prior art in the applicable patent (i.e., among the Asserted Patents); the nature of the problem to be solved and the existence of similar improvements in similar applications; design incentives and other market forces, including the advantages of creating a superior and more desirable

product and the effects of demands known to the design community or present in the marketplace; the ability to implement the alleged invention as a predictable variation of the prior art; improvements in similar devices; any needs or problems known in the fields addressed by the applicable patent (i.e., among the Asserted Patents); the teachings in the references directed to solving the problems that the applicable patent (i.e., among the Asserted Patents) was allegedly directed to solving; and the number of identified, predictable solutions to the problems addressed by these patents. In addition, the simultaneous (and/or prior) inventions described above (and elsewhere in these contentions) are evidence that motivation to combine the concepts described in the various prior art references did, in fact, exist, and they were, in fact, combined.

These references and inventions identify and address many of the same technical issues and suggest similar solutions to those issues. Moreover, many of these references and inventions cross-reference and discuss one another, further illustrating the close technical relationship among this group of references and inventions. Accordingly, the teachings of the individual prior art references and inventions, combined with the industry knowledge of POSAs at the time of the alleged inventions of the Asserted Patents, would render obvious the Asserted Claims for at least the reasons described below and in the incorporated exhibits. POSAs at the time of the alleged inventions had reason to combine or modify one or more of the references listed and charted in Exhibits A-1 to A-19, B-1 to B-7, and C-1 to C-11 in light of the knowledge of POSAs at the time of the invention and information in the prior art cited herein. Thus, these references would logically have been combined pursuant to 35 U.S.C. § 103, and there was abundant motivation to combine such references at the time of the purported inventions of the Asserted Patents.

Sony's discussion below identifies exemplary features disclosed by the references. These features should be understood to be more fully set out in the appended claim charts (i.e., Exhibits A-1 to A-19, B-1 to B-7, or C-1 to C-11) for these references.

Sony may rely upon a subset of the references or all of the references listed in Part II, depending upon the Court's claim construction and further investigation. Sony's contentions that the references contained in these contentions, in various combinations, render the Asserted Claims obvious under 35 U.S.C. § 103 are in no way an admission or suggestion that each reference does not independently anticipate the Asserted Claims under 35 U.S.C. § 102.

Sony identifies the following anticipatory references and put forth the below exemplary combinations that further demonstrate the obviousness of the Asserted Claims. The combinations are not intended to be exhaustive, as there are many possible combinations of these references, and it is not practical, particularly at this early stage before further factual investigation and claim construction proceedings, to identify and list all potentially relevant combinations. In particular, the Asserted Claims are rendered obvious under 35 U.S.C. § 103 in view of at least, and without limitation, the following combinations of references.

A. Anticipation and Obviousness of U.S. Patent No. 7,867,808

1. Overview of Teachings in the Prior Art

POSAs would have been familiar with several manufacturing processes and techniques that were widely known and used in semiconductor fabrication generally and in photodetector design and fabrication in particular at the time of invention. This background knowledge would have informed the POSA's reasons to combine prior art references, and the POSA's reasonable expectation that such combinations would have worked as intended, for each combination described herein, at least because such combinations would have used known methods in known ways to achieve predictable results, and such methods had been used to improve other device

designs and fabrication processes in similar ways. These teachings are evidenced, for example, by at least the following sets of prior art references.

a. Forming Isolation Layers by Ion Implantation

It was well-known in the art to form layers in crystalline semiconductor material by ion implantation, which was a standard semiconductor manufacturing tool and technique. Compared to other diffusion processes to introduce dopants, ion implantation provided much finer feature resolution, more flexibility in forming doping profiles, and finer control over doping profile, placement, and feature shape in crystalline materials. Ion implantation also reduced the time at high temperatures required for diffusion. By the time of invention, virtually all semiconductor device structures were formed by ion implantation, making it possible to form devices with sub-micron features.

It was also well-known in the art to form isolation layers in photodetectors in order to block electrical carriers originating outside the volume of a photodetector associated with a pixel from being electrically detected in that photodetector. Isolation layers have long been used in semiconductor devices generally, not just in solid state imaging devices, such as to electrically isolate adjacent transistors. Earlier methods for providing isolation included forming isolation features using local oxidation of silicon ("LOCOS") or shallow trench isolation. These processes, and the resulting isolation features, introduced defects in the crystalline layer that generated unwanted dark current or noise that the photodetector would detect along with the desired signal of photogenerated carriers. It was well-known to form isolation layers in photodetectors by ion implantation in order to avoid, or mitigate, the dark current introduced by these earlier methods of forming isolation layers. It was also known to form isolation layers to block dark current from surface interfaces.

POSAs would have had several reasons to form isolation layers in photodetectors using ion implantation including at least avoiding or mitigating the dark current generation by earlier shallow trench isolation or LOCOS isolation, and to take advantage of the benefits provided by ion implantation including at least finer feature resolution, finer control over doping levels, and finer control over doping placement within a crystalline semiconductor. In addition to the reasons for forming combinations outlined above, POSAs would have had a reasonable expectation that forming isolation layers by ion implantation would work at least because ion implantation was a known method of forming semiconductor device features in a predictable art, and because ion implantation worked as described in at least any of the following references, regardless of whether ion implantation is described for forming isolation layers in particular or conduction layers in general.

Accordingly, POSAs would have had reasons to form isolation layers by ion implantation as described in at least any one or more of the following references (collectively the "Ion Implantation References"):

Reference	**Citation**	**Bates Range**
Japanese Patent Application Publication No. JP 2006-303385 A ("Masagaki"), published November 2, 2006	*E.g.,* Masagaki, ¶¶ [0030], [0037], [0040]	SONYVX-PRIOR ART-0000678-SONYVX-PRIOR ART-0000704
Japanese Patent Application Publication No. JP 2006-93587 A ("Maruyama"), published April 6, 2006	*E.g.,* Maruyama, ¶¶ [0005]. [0012]-[0013], [0015], [0023], [0027], [0029], [0032], [0041], claims 5-6	SONYVX-PRIOR ART-0000510-SONYVX-PRIOR ART-0000534
U.S. Patent Application Publication No. US 2003/0038336 A1 ("Mann"), published February 27, 2003	*E.g.,* Mann, ¶¶ [0020]-[0025], claims 8, 11-12, 26-27, 30, 48, 50, 52-53, 55-56, 59-62	SONYVX-PRIOR ART-0001886-SONYVX-PRIOR ART-0001898
U.S. Patent No. 6,809,008 ("Holm-008"), issued October 26, 2004	*E.g.*, Holm-008, 7:41-67, 8:42-60, 11:21-38, 12:6-34,	SONYVX-PRIOR ART-0000985-SONYVX-PRIOR ART-0001009

Reference	Citation	Bates Range
	13:23-39, 13:43-14:6, 15:7-17, claim 1	
United States Patent No. 7,781,715 ("Uya"), filed September 17, 2007, issued August 24, 2010	*E.g.,* Uya, 7:16-50, 12:8-21, 42-50, 24:16-29, 25:51-58, 26:30-51, 28:57-29:35, 35:5-27, 35:8-18)	SONYVX-PRIOR ART-0001057-SONYVX-PRIOR ART-0001125
United States Patent No. 8,507,960 ("Itonaga"), filed November 27, 2006, issued August 13, 2013	*E.g.*, Itonaga, Figs. 16A & 16B, 19A & 19B, 3:35-43, 4:28-48, 9:12-28, 10:9-56, 13:4-11, 13:53-14:3, claims 6-7, 11	SONYVX-PRIOR ART-0001144-SONYVX-PRIOR ART-0001172
United States Patent Application Publication No. U.S. 2007/0128954 A1 ("Itonaga-954"), published June 7, 2007	*E.g.*, Itonaga-954, Figs. 16A & 16B, 19A & 19B, [0016], [0025]-[0026], [0075], [0080]-[0084], [0103], [0107], claims 3, 6, 9	SONYVX-PRIOR ART-0002292-SONYVX-PRIOR ART-0002321
United States Patent Application Publication No. U.S. 2006/0270096 A1 ("Brady"), published November 30, 2006	*E.g.*, Brady, ¶¶ [0005], [0008], [0012]-[0014], [0018], [0030], [0036]-[0038], [0040]-[0041], [0043]-[0045], [0047]-[0049], [0051]-[0053], [0057]-[0058], claims 1, 5-7, 12-21, 27-29, 32, 39-40, 47-48, 56-57, 67, 69, 71, 87, 98	SONYVX-PRIOR ART-0001281-SONYVX-PRIOR ART-0001295
United States Patent Application Publication No. U.S. 2006/0197007 Al ("Iwabuchi-007"), published September 7, 2006	*E.g.*, Iwabuchi-007, ¶¶ [0007]-[0008], [0034], [0144], [0176]	SONYVX-PRIOR ART-0001383-SONYVX-PRIOR ART-0001415
United States Patent No. 6,590,242 ("Kozuka"), issued July 8, 2003	*E.g.*, Kozuka, 12:1-27, 13:40-59, 14:13-25, 20:60-62, 24:44-53, 25:62-26:4, 28:18-23	SONYVX-PRIOR ART-0000937-SONYVX-PRIOR ART-0000984

b. Forming a Light Passage by Removing a Portion of a Substrate to Expose a Photodiode

It was well-known that active-pixel CMOS image sensors may include wiring and interlayer dielectric structures, often times in multiple layers, at the front surface of a

semiconductor substrate above the photodiode. This is evidenced, for example, by these exemplary disclosures (collectively the "Lightpipe References"):

Reference	Citation	Bates Range
U.S. Patent Application Publication No. US 2005/0285215 A1 ("Lee 215"), published December 29, 2005	*E.g.,* [0008], [0054], Figs. 5, 7A	SONYVX-PRIOR ART-0001319-SONYVX-PRIOR ART-0001351
U.S. Patent Application Publication No. US 2006/0183265 A1 ("Oh"), published August 17, 2006	*E.g.,* [0042]-[0043], Fig. 2H, 2I, 3	SONYVX-PRIOR ART-0001352-SONYVX-PRIOR ART-0001382
U.S. Patent No. 6,861,686 ("Lee 686"), issued March 1, 2005	*E.g.,* Fig. 1	SONYVX-PRIOR ART-0000762-SONYVX-PRIOR ART-0000806
J. Gambino et al. "CMOS Imager with Copper Wiring and Lightpipe," in 2006 International Electron Devices Meeting, 2006, pp. 1-4, IEEE	*E.g.,*at 1-2, Figs. 2-3	SONYVX-PRIOR ART-0000674-SONYVX-PRIOR ART-0000677

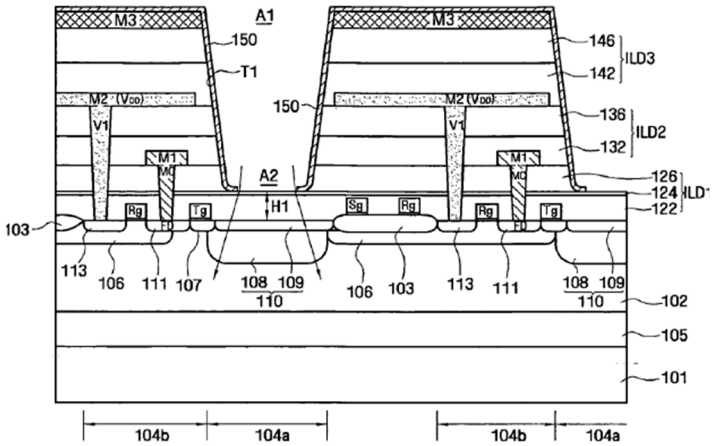
As shown therein, it was well-known to POSAs that the layers of wiring on the front surface can undesirably reflect light and reduce the sensitivity of the imager. Gambino, page 1, ("The SiN capping layers used to passivate the surface of the Cu introduce discontinuities in the refractive index, that can reflect light and reduce the sensitivity of the imager.") Optical crosstalk from the incident light between adjacent photodiodes presents a further problem. *Id*. ("Another problem common to all image sensors is the decreasing photodiode size as the pixel size decreases. Because of the small photodiode size, pixel sensitivity is reduced and crosstalk increases.") Lee '215, Figure 5, [0008] ("Generally, to provide a best resolution image, it is desirable with a sensor array, such as an active pixal sensor array, that light passing through an aperture A1 be incident only on the corresponding associated photoelectric conversion element 51. However, as illustrated by the various rays R1, R2, R3 in FIG. 5, degradation may be caused

by various incident light rays passing through the aperture A1 and striking adjacent photoelectric conversion elements. Refracted rays R1 may be generated as a result of the respective interlayer dielectric layers 55, 55′, 55″ having different indices of refraction.”).

One known solution to the above problems is to form a light passage or aperture above the photodiode by removing a portion of a substrate to guide light to the photodiode. Lee ‘215, Figure 7A, [0054], (“the trench T1 defines a light transmissive region extending towards the photoelectric conversion element 110 from the aperture A1 to allow passage of light.”). Lee ‘686, Figures 1, 2O, 2R, 5:3-5 (“Light is transmitted to the p/n photodiode 110 through a light passageway 272 positioned in alignment with the p/n photodiode 110.”), 2:58-61 (“forming a light passageway having a light inlet in alignment with the photodiode by removing portions of the interlayer dielectric structure over the photodiode.”). Oh, Figure 2H, [0042] (“Then, by etching the interlayer dielectric structure 200 of the action pixel region, including contact 114, contact 128 and interconnection 130, second openings (cavities) 178 above the photo conversion elements 106 are formed.”). Gambino, page 1, (“an air-gap guard ring has been used for a CMOS imager with Al wiring, to guide light into the pixel.”)

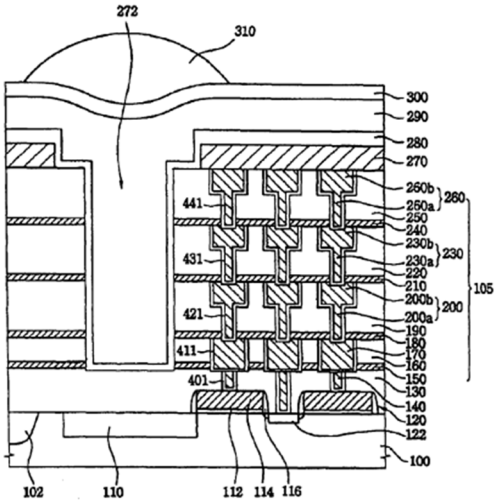
Lee '215

FIG. 7A



Lee '686

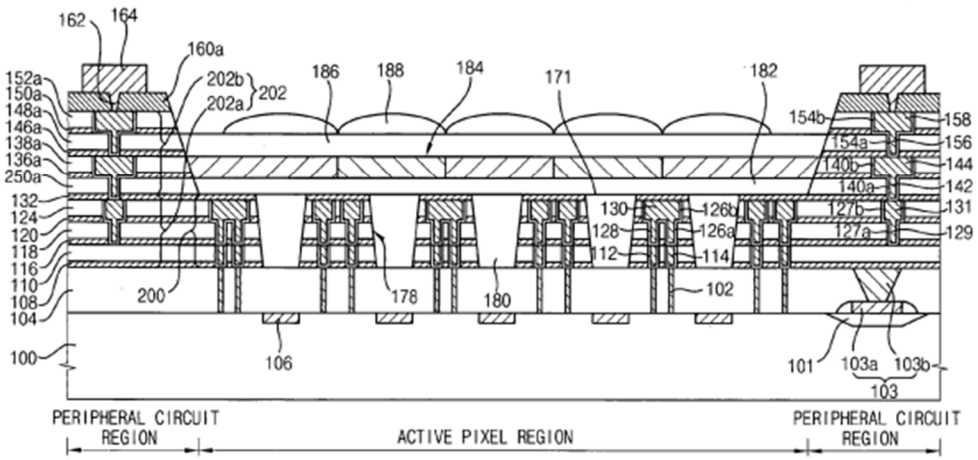
FIG. 1



It was also common to fill the light passage after removal with a transparent material to form a lightpipe to provide the benefit of guide incoming light to a pixel and to prevent light penetration to an adjacent pixel. Oh, Figures 2I, 3, [0043] ("a transparent filling material 180 is deposited in the cavity openings 178. The transparent filling material 180 preferably has a higher refractive index than other interlayer dielectric layers to prevent the loss of light to the outside environment and to prevent penetration of light to an adjacent pixel."). Gambino, Figures 2 & 3, at 1 ("a light-pipe process is described that is compatible with Cu wiring. Using this technology, high quantum efficiency and high angular response are achieved for a 2.2 μm pixel, and high reliability is demonstrated"), 1-2 ("[T]he lightpipe is formed by etching through the entire dielectric stack above the photodiode, then coating the surface with an SiN layer. The lightpipe is then filled with an organic planarizing layer. Color filters and microlenses are formed using conventional processing[.]").

Oh

FIG. 3



Gambino

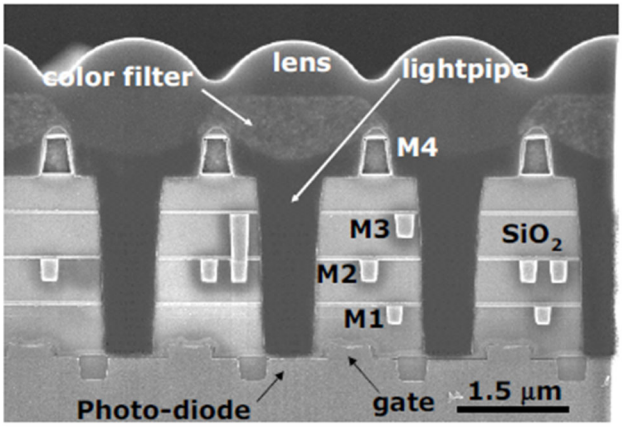


Fig. 3. SEM cross-section of 2.2 µm pixel with lightpipe and Cu wiring

Accordingly, POSAs would have been motivated to remove a portion of a substrate in a front-side illuminated image sensor to expose the photodiode for at least several reasons, such as

to form a light passage or a light pipe to reduce optical crosstalk between adjacent pixels and improve pixel sensitivity. POSAs would have a reasonable expectation the removal would work at least because forming a light passage or a light pipe is a known technique to guide incident light to a photodiode.

c. Process For Thinning Substrate When Fabricating A Backside-Illuminated Sensor

It was well-known in the art that fabricating backside-illuminated photodetectors or image sensors involved a process step of thinning substrate so that the photodiode could receive incident light. It was well-known that there were a limited number of ways to accomplish this step. One well-known approach was to form end point detection features in the sensor substrate, like the crystalline silicon in which the photodetector is formed. The end point detection feature then set the thickness of the resulting substrate by marking the end point of the thinning step done with chemical mechanical polishing, etching, or other mechanisms.

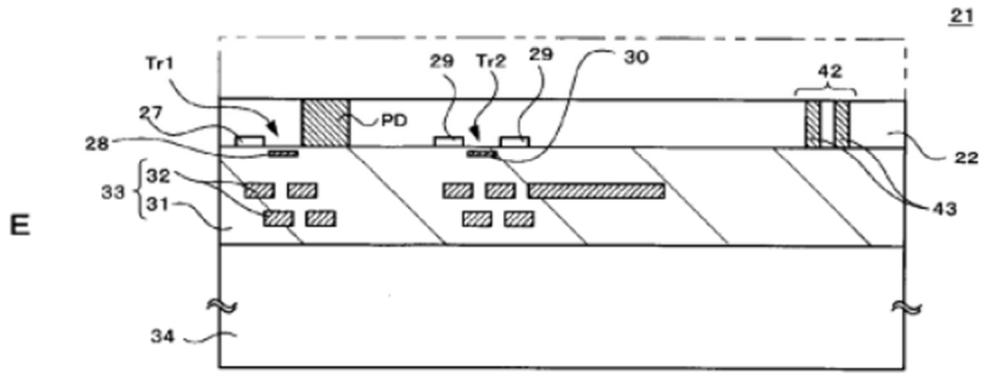
This methodology resulted in well-controlled substrate thickness and planar backside surfaces with very low variations in thickness or flatness, suitable for subsequent process steps, and could be used to generate very thin sensor substrates. These results were known to be superior to other methods for controlling the stopping point of the backside thinning step, such as relying on etching sensitive to differences in doping levels in the substrate. This latter method often resulted in uneven surfaces because of lower sensitivity to variations in the doping concentrations, and because the doping concentrations themselves often did not present planar stopping points in a cross sectional profile of the substrate. The end point detection methodology also facilitated backside thinning in the crystalline layer and avoided backside thinning methods that used the oxide layer in a SOI wafer as the etch stop. Because the end point detection did not require using SOI wafers, which were known to be more expensive that using crystalline silicon,

as the substrate for the photodetectors, this process step was known to avoid the costs of the more expensive SOI wafers. For all these reasons POSAs would have been motivated to use the known end point detection methodology when performing backside thinning process steps on backside-illuminated photodetector sensors, as disclosed in at least the following references (collectively the "End Point References"):

Reference	Citation	Bates Range
Japanese Patent Application Publication No. JP 2005-353996 (Shiraiwa"), published December 22, 2005.	*E.g.,* [0014]-[0024], [0037], Fig. 5E	SONYVX-PRIOR ART-0000535-SONYVX-PRIOR ART-0000559
U.S. Patent Application Publication No. US 2006/0094151 A1 ("Sumi"), published May 4, 2006	*E.g.*, [0008], [0017], [0024], [0027], [0029], [0081], [0085], Figs. 13, 15	SONYVX-PRIOR ART-0000844-SONYVX-PRIOR ART-0000871

For example, Shiraiwa describes a method for thinning the backside of a semiconductor substrate without using the oxide layer in an SOI wafer as an etch stop. Shiraiwa, [0014]-[0024]. Figure 5E shows thinning silicon substrate 22 to expose the photodiode ("PD") by setting end point detection portion 42 that defines the stopping point for the backside thinning at the same thickness as the photodiode. Id., [0037], Fig. 5E.

[FIG. 5]



Sumi likewise discloses backside thinning in bulk silicon using edge detection portions 63 surrounding an image area to set the stopping depth for the removing step. *E.g.*, Sumi ¶¶ 24, 27, 81 & Figs. 13, 15.

FIG. 13

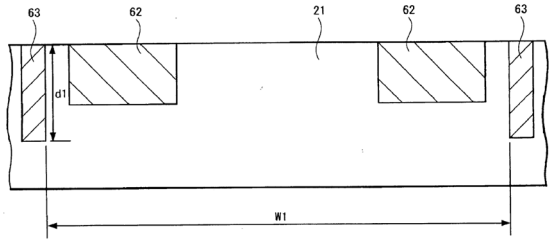
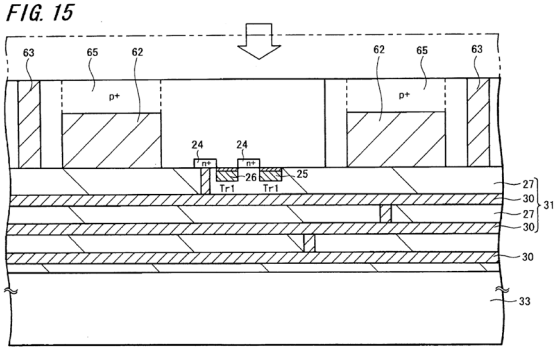


FIG. 15



d. Plasma Activation

It was well-known in the art to enhance the surface energy of bonding surfaces with plasma activation. It was also well-known even earlier in the art that plasma treatment of bonding surfaces would increase resulting bonding strength even if the physical reasons for this improved bond strength were not understood and the process was not yet called plasma activation.

POSAs would have had several reasons to apply plasma activation when bonding sensor ("second substrate") and support ("first substrate") substrates together including at least improving resulting bond strength and reliability, improving device yield, facilitating bonding at lower temperatures, facilitating bonding smaller conductive pads, achieving cost savings, and other reasons as articulated in the following references (collectively the "Plasma Activation References").

Reference	Citation	Bates Range
A. Fan et al. "Copper Wafer Bonding," *Electrochemical and Solid-State Letters*, vol. 2, no. 10, pp. 534-536 (1999) ("Fan")	*E.g.*, 534 ("In previous metal-metal bonding studies, surface preparation (in particular, Ar beam surface activation) was an important element in obtaining a strong bond.")	SONYVX-PRIOR ART-0000670-SONYVX-PRIOR ART-0000673
S.H. Christiansen et al. "Wafer Direct Bonding: From Advanced Substrate Engineering to Future Applications in Micro/Nanoelectronics," *Proceedings of the IEEE*, vol. 94, no. 10, pp. 2060-2106 (2006) ("Christiansen")	*E.g.*, 2066 (discussing surface activation)	SONYVX-PRIOR ART-0000623-SONYVX-PRIOR ART-0000669
T. Suga et al. "Surface Activated Bonding for New Flip Chip and Bumpless Interconnect Systems," in *52nd Electronic Components and Technology Conference 2002 (Cat. No. 02CH37345)*, pp. 105-111 (2002) ("Suga")	*E.g.*, 105 ("The idea of SAB is based on the fact that two atomically clean solid surfaces under contact develop an extremely strong adhesive force. The clean and activated surfaces can be obtained by Ar fast atom beam (FAB) bombardment in a certain clean atmosphere such as ultrahigh vacuum."), *passim*	SONYVX-PRIOR ART-0000837-SONYVX-PRIOR ART-0000843
T.H. Kim et al. "Room temperature Cu-Cu direct bonding using surface activated bonding method," *J. Vacuum Science & Technology A*, vol. 21, no. 2, pp. 449-453 (2003) ("Kim")	*E.g.*, 450 (discussing surface activation)	SONYVX-PRIOR ART-0000705-SONYVX-PRIOR ART-0000710
U.S. Patent Application Publication No. US 2004/0235266 A1 ("Tong '266"), published November 25, 2004	*E.g.*, [0028] ("FIG. 4 is a graph of bonding energy as a function of storage time for bonded wafers processed with and without plasma treatment") & Fig. 4, [0044], [0046]	SONYVX-PRIOR ART-0000901-SONYVX-PRIOR ART-0000924

Reference	Citation	Bates Range
U.S. Patent No. 6,074,895 ("Dery"), issued June 13, 2000	*E.g.*, Abstract ("A plasma is applied, to chemically modify the a surface of the chip carrier and the passivation layer of the IC chip substantially without roughening the surface of the passivation layer. The plasma is either an O2 plasma or a microwave-generated Ar and N2O plasma. … The plasma treatment may be performed after the step of joining. Then, the chip and chip carrier are treated with the plasma simultaneously. Alternatively, the IC chip and chip carrier may be treated with the plasma before they are joined to one another."), *passim*	SONYVX-PRIOR ART-0000925-SONYVX-PRIOR ART-0000936
U.S. Patent No. 6,902,987 ("Tong-987"), issued June 7, 2005	*E.g.*, 1:58-60 ("A gas plasma treatment prior to bonding in ambient is known to enhance the bonding energy of bonded silicon pairs at low or room temperature."), 11:1-11, 12:15-36, 12:54-67, *generally passim*	SONYVX-PRIOR ART-0000872-SONYVX-PRIOR ART-0000900
V. Dragoi and P. Lindner. "Plasma Activated Wafer Bonding of Silicon: *In Situ* and *Ex Situ* Processes," *ECS Transactions*, vol. 3, no. 6, pp. 147-154 (2006) ("Dragoi")	*E.g.*, 147 ("Plasma activated wafer bonding generated a high interest in last decade due to the important process temperature reduction.") & *passim*	SONYVX-PRIOR ART-0000596 SONYVX-PRIOR ART-0000603
United States Patent Application Publication No. U.S. 2003/0211705 ("Tong-705"), published November 13, 2003	*E.g.,* Tong-705, [0008]-[0021], [0041], [0044]-[0045], [0055]-[0056], [0059], [0063], claims 13-15, 33, 40, 47-49	SONYVX-PRIOR ART-0002322-SONYVX-PRIOR ART-0002345
United States Patent Application Publication No. U.S. 2004/0157407 ("Tong-407"), published	*E.g.*, Tong-407, [0013], [0048], [0074], [0080]-[0081], claims 18-19, 24, 52	SONYVX-PRIOR ART-0002346-SONYVX-PRIOR ART-0002367

e. Three-Dimensional Vertically Integrated Solid State Imager

It was well-known in the art at the time of invention to make solid-state imagers in a three-dimensional package that vertically integrated electronics on one or more wafers or substrates with a focal plane array or sensor on another wafer or substrate. POSAs had several reasons to pursue this approach.

First, by making the photodetector and electronics on different wafers or substrates, the fabrication techniques – and materials – could be optimized for each particular application. This was important because semiconductor fabrication processes optimized for forming CMOS devices in silicon were often not optimized to form photodetectors in silicon, or other material systems with different bandgaps and optoelectronic properties that might be preferred as a substrate for a sensor layer. *E.g.*, Holm '008, 1:23-40. For example, "thick absorbing layers and deep junctions may be needed to achieve high efficiency; these same design criteria generally being in conflict with those for high performance electronic applications." *Id.*, 1:36-40.

Second, the electronics and photodetectors are also subject to different scaling trends, so that while reducing the electronics dimensions in advanced process nodes provided benefits for advanced electronics, reducing the pixel area and volume for photodetectors is associated with increased dark current and, consequently, photodetectors with reduced signal to noise ratios. *E.g., id.*, 1:41-52. Additionally, "reduced lateral dimensions" in the pixel "are generally attended by reduced vertical dimensions leading to thinner layers and shallower junctions as well as higher doping levels and reduced carrier diffusion lengths. Reduced supply voltages also may negatively impact charge collection and storage capability of the PD. Moreover, an ever-increasing number of interconnect levels and corresponding isolating dielectric layers generally decreases the optical throughput and coupling efficiency to the photodetector and introduces additional sources of reflection and scattering that can lead to elevated levels of optical

crosstalk." *Id.*, 2:2-12. It is thus desirable to scale the pixels and readout and other electronics differently, using different processes for their fabrication. Forming the sensor layer and the supporting electronics layers in different substrates, then bonding the wafers or die together, makes it possible to optimize the fabrication techniques separately for each layer.

Third, it was known in the art to increase the transistor count associated with each pixel to provide "digital pixel sensors" with enhanced functionality compared to 3 or 4 transistors in a typical readout circuit for an "active pixel sensor." *E.g.*, *id.*, 1:53-62. "This desire for increased signal processing functionality within the pixel escalates competition for real estate within the pixel area creating additional problems generally associated with shrinking the PD active area, reducing the fill factor within the pixel, and applying advanced process technologies." *Id.*, 1:57-62.

Fourth, "[e]fforts to improve the level of PD performance can limit flexibility and performance in the CMOS electronics as well. Minimizing the number of interconnect levels to improve the optical coupling to the PD, for example, may make interconnect routing more difficult and less area-efficient." *Id.*, 2:14-18.

In short, "[t]he co-integration of the photosensor with the CMOS electronics (i.e., within the same material layer, using the same processes, etc.) within the pixel of CMOS imagers may severely limit both the performance of the photosensor and the flexibility of the system architectural design. This problem may be further complicated by progression to more advanced CMOS technology generations which generally utilize… non-transparent silicides, and increasing numbers of interconnect levels. The… trend toward increase functionality within the pixel (as with digital pixel sensors-DPS) adds more electronic circuitry within the pixel creating competition for pixel area, decreasing fill factor and further compromising of performance." *Id.*

2:19-32. POSAs knew that vertical integration provides improved performance, lower system cost, increased functionality, lower power consumption and smaller form factors.

For any one or more of these reasons, POSAs would have known to form known photodetectors in a sensor layer using processes optimized for the photodetector fabrication, and bond that sensor layer to one or more support layers having relevant electronics such as readout circuits, analog to digital converters, power conditioning and supply, or digital signal processing, which would be fabricated in processes optimized for the particular electronics. In that fashion a known photodetector design could be implemented in a sensor layer and combined with any of the following exemplary three-dimensional imager references (collectively the "Vertically Integrated 3D Imager References"), with the relevant teachings described in the associated exhibits:

Reference	**Citation**
Guidash '256	Ex. A-1
Iwabuchi '762	Ex. A-4
Holm '008	Ex. A-8
Patti IEEE	Ex. A-14
Suntharalingam	Ex. A-16

f. Forming a BSI image sensor or an FSI image sensor

In CMOS image sensors, it was well-known that the image sensor can be formed in one of two configurations: a backside illuminated (BSI) and a frontside illuminated (FSI) configuration. The BSI detector receives incident light through the "backside" surface of the substrate where the photodiode is formed, whereas the FSI detector receives incident light through the "frontside" surface of that substrate. The "frontside" conventionally referred to the surface that was presented as the surface of a workpiece in semiconductor fabrication. For example, this was often the surface through which dopant was typically introduced to the

substrate, by processes such as ion implantation. In conventional planar integrated circuits, the electronics were formed on the frontside of the substrate using well-known fabrication processes like ion implantation or photolithography. In a semiconductor-on-insulator (SOI) wafer, for example, the "frontside" conventionally refers to the surface of the top crystalline layer opposite the oxide layer insulating the crystalline layer from the underlying dielectric substrate (such as silicon or sapphire) that adds rigidity to the wafer, whereas "backside" conventionally refers to the surface of the crystalline layer at the interface with the oxide insulator layer.

Forming a BSI sensor entailed additional process steps, like thinning the backside substrate so that the photodetector presented a suitable absorber thickness and the photodiode was exposed to light through the backside surface. It was known that photodetector structures designed for FSI sensors could be used in a BSI format, in which the POSA would form same conduction and isolation layers in a BSI format as described in an FSI format, but the sensor would accept incident light through the backside surface rather than the frontside. *See*, *e.g.*, Pain2005. In other words, for example, an accumulation layer positioned near the frontside surface in a FSI detector would still be formed in that location in a BSI detector, but the BSI detector would have the backside thinned and the backside presented for receiving incident light.

This has the consequence of moving the photodetector contact or floating diffusion, and any other associated read out electronics, to the back of the pixel, relative to the backside incident surface, with at least two immediate benefits. First, this left more of the area on the backside incident surface available for light collection, rather than being allocated to forming electronics. This is often described as increasing the sensor fill factor, e.g., the portion of the incident surface area useful for light collection. On the same die this allowed forming imagers with either the same number of pixels with larger light collecting area (increasing fill factor), or a

larger number of the pixels that had smaller light collecting areas as was provided with the smaller fill factor. The former alternative, by collecting more light per pixel, would provide better sensitivity, while the latter alternative, by introducing more pixels, would provide larger format density with higher image resolution. Both alternatives resulted in more effective photodetectors. Second, moving the photodetector contact or floating diffusion, and other read out electronics, to the back of the pixel, relative to the incident surface, made them more easily contacted by subsequent layers adding increased functionality. This easily facilitated three dimensional system integration by providing ready connections to electronics formed on different layers and bonded to the imager on a sensor layer. For at least these reasons POSAs would have known to take photodetector designs for FSI sensors and implement the same conduction and isolation layers in BSI detectors.

2. Guidash '256 (Ex. A-1)

Guidash '256 discloses a method for fabricating a vertically-integrated active pixel sensor that includes a sensor wafer connected to a support circuit wafer, and describes embodiments in which the sensor wafer can be a backside illuminated (BSI) image sensor or a front-side illuminated (FSI) image sensor. The following combinations, based on Guidash '256, render obvious claims 1-2 and 4-9. Exhibit A-1 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below.

a. BSI embodiments

Guidash '256 renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-1.

Guidash '256 in view of either Uya or Maruyama, renders obvious claim 2. *See* Ex. A-1.

Guidash '256 in view of any Plasma Activation Reference, renders obvious claim 7. *See* Ex. A-1.

Guidash '256 in view of any one of the End Point References, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-1.

Guidash '256 in view of any one of the End Point References, and further in view of either Uya or Maruyama, renders obvious claim 2. *See* Ex. A-1.

Guidash '256 in view of any one of the End Point References, and further in view of any Plasma Activation Reference, renders obvious claim 7. *See* Ex. A-1.

Guidash '256 in view of any one of the Ion Implantation References renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-1.

Guidash 256 in view of any one of the Ion Implantation References, and further in view of either Uya or Maruyama, renders obvious claims 2. *See* Ex. A-1.

Guidash '256 in view of any one of the Ion Implantation References, and further in view of any Plasma Activation Reference, renders obvious claim 7. *See* Ex. A-1.

Guidash '256 in view of any one of the Ion Implantation References, and further in view of any one of the End Point References, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-1.

Guidash '256 in view of any one of the Ion Implantation References, any one of the End Point References, and further in view of either Uya or Maruyama, renders obvious claim 2. *See* Ex. A-1.

Guidash '256 in view of any one of the Ion Implantation References, any one of the End Point References, and any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-1.

b. FSI embodiments

Guidash '256 in view of any one of the Lightpipe References, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-1.

Guidash ‘256 in view of any one of the Lightpipe References, and further in view of either Uya or Maruyama, renders obvious claims 2. *See* Ex. A-1.

Guidash ‘256 in view of any one of the Lightpipe References, and further in view of any Plasma Activation Reference, renders obvious claim 7. *See* Ex. A-1.

Guidash ‘256 in view of any one of the Ion Implantation References, and further in view of any one of the Lightpipe References, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-1.

Guidash ‘256 in view of any one of the Ion Implantation References, any one of the Lightpipe References, and further in view of either Uya or Maruyama, renders obvious claims 2. *See* Ex. A-1.

Guidash ‘256 in view of any one of the Ion Implantation References, any one of the Lightpipe References, and further in view of any Plasma Activation Reference, renders obvious claim 7. *See* Ex. A-1.

3. Yoshihara ’290 (Ex. A-2)

Yoshihara ’290 discloses methods of manufacturing a semiconductor image sensor module in which a semiconductor image sensor chip and an image signal processing chip are connected with a minimum parasitic resistance and parasitic capacity and efficient heat dissipation of the image signal processing chip and shielding of light are simultaneously obtained.

For the following analysis, Guidash ’256 (Ex. A-1), Uya (Ex. A-3), Iwabuchi 762 (Ex. A-4), Suntharalingam (Ex. A-16), or Maruyama (Ex. A-17) (collectively the “Backside Thinning References”) each disclose thinning the substrate for a BSI sensor by removing a lower portion of the substrate to expose the photodiode.

The following combinations, based on Yoshihara ’290, render obvious claims 1-2 and 4-9. Exhibit A-2 provides a chart identifying where specifically in each alleged item of prior art

each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Yoshihara ’290 in view of any one of the Backside Thinning References, renders obvious claims 1, 4-6, and 8-9.

Yoshihara ’290 in view of any one of the Backside Thinning References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2.

Yoshihara ’290 in view of any one of the Backside Thinning References, further in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Plasma Activation References, renders obvious claim 7.

Yoshihara ’290 in view of any one of the Backside Thinning References, further in view of any one of the End Point References, renders obvious claims 1, 4-6, and 8-9.

Yoshihara ’290 in view of any one of the Backside Thinning References, further in view of any one of the End Point References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2.

Yoshihara ’290 in view of any one of the Backside Thinning References, further in view of any one of the End Point References, further in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Plasma Activation References, renders obvious claim 7.

Yoshihara ’290 in view of any one of the Ion Implantation References, further in view of any one of the Backside Thinning References, renders obvious claims 1, 4-6, and 8-9.

Yoshihara ’290 in view of any one of the Ion Implantation References, further in view of any one of the Backside Thinning References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2.

Yoshihara ’290 in view of any one of the Ion Implantation References, further in view of any one of the Backside Thinning References, further in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Plasma Activation References, renders obvious claim 7.

Yoshihara ’290 in view of any one of the Ion Implantation References, further in view of any one of the Backside Thinning References, further in view of any one of the End Point References, renders obvious claims 1, 4-6, and 8-9.

Yoshihara ’290 in view of any one of the Ion Implantation References, further in view of any one of the Backside Thinning References, further in view of any one of the End Point References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2.

Yoshihara ’290 in view of any one of the Ion Implantation References, further in view of any one of the Backside Thinning References, further in view of any one of the End Point References, further in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Plasma Activation References, renders obvious claim 7.

4. Uya (Ex. A-3)

Uya discloses methods for forming a solid-state backside-illuminated imaging device and reading the detected image signal from the front side of the substrate. As explained below, POSAs would have had reasons to combine Uya’s backside imager with any one of the Vertically Integrated 3D Imager References to form a three-dimensional imager. The following combinations, based on Uya, render obvious claims 1-2 and 4-9. Exhibit A-3 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Uya in view of any one of the Vertically Integrated 3D Imager References renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-3.

Uya in view of any one of the Vertically Integrated 3D Imager References, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-3.

Uya in view of any one of the Vertically Integrated 3D Imager References, and further in view of any one of the Ion Implantation References, renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-3.

Uya in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Ion Implantation References, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-3.

Uya in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Ion Implantation References, further in view of any one of the End Point References, renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-3.

Uya in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Ion Implantation References, further in view of any one of the End Point References, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-3.

5. Iwabuchi ’762 (Ex. A-4)

Iwabuchi ’762 discloses a method of manufacturing a CMOS semiconductor image sensor module that has an increased pixel aperture ratio while also achieving better chip usage efficiency and enables simultaneous shuttering of all pixels. The method for manufacturing a semiconductor image sensor module of the present invention makes it possible to manufacture a semiconductor image sensor module comprising a CMOS image sensor that has an increased aperture ratio of photoelectric conversion elements, a better chip utilization rate, and also enables simultaneous shuttering of all pixels.

The following combinations, based on Iwabuchi ’762, render obvious claims 1-2 and 4-8. Exhibit A-4 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Iwabuchi ’762 renders obvious claims 1, 4-6, and 8. *See* Ex. A-4.

Iwabuchi ’762 in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders claim 2 obvious. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the Plasma Activation References renders obvious claim 7. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the Ion Implantation References renders obvious claims 1, 4-6, and 8. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the Ion Implantation References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders claim 2 obvious. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the Ion Implantation References, further in view of any one of the Plasma Activation References renders obvious claim 7. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the End Point References renders obvious claims 1, 4-6, and 8. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the End Point References and further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders claim 2 obvious. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the End Point References, and further in view of any one of the Plasma Activation References renders obvious claim 7. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the Ion Implantation References, further in view of any one of the End Point References renders obvious claims 1, 4-6, and 8. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the Ion Implantation References, further in view of any one of the End Point References and further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders claim 2 obvious. *See* Ex. A-4.

Iwabuchi ’762 in view of any one of the Ion Implantation References, further in view of any one of the End Point References, and further in view of any one of the Plasma Activation References renders obvious claim 7. *See* Ex. A-4.

6. Suzuki (Ex. A-5)

Suzuki discloses a backside illuminated CMOS image sensor and methods of making it. The following combinations, based on Suzuki, render obvious claims 1-2 and 4-9. Exhibit A-5 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Suzuki anticipates claims 1, 4-6, and 8-9.

Suzuki renders obvious claims 1, 4-6, and 8-9.

Suzuki in view of Uya (Ex. A-3) or Murayama (Ex. A-17), renders obvious claim 2.

Suzuki in view of any one of the Plasma Activation References, renders obvious claim 7.

7. Ezaki ’519 (Ex. A-6)

Ezaki ’519 discloses methods for manufacturing back-illuminated photodetectors with the photoelectric conversion element formed in a such a way that the photodetector substrate, conduction layers, and isolation layers, provide color selectivity that eliminates the need to add color filters on the backside illuminated surface. As explained below, POSAs would have had reasons to combine Ezaki ’519’s backside imager with any one of the Vertically Integrated 3D

Imager References to form a three-dimensional imager. The following combinations, based on Ezaki ’519, render obvious claims 1-2 and 4-9. Exhibit A-6 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

As explained at step 1[f] in the accompanying charts these references each describe the process step of thinning the lower portion of a substrate on a BSI photodetector: Guidash ’256 (Ex. A-1), Uya (Ex. A-3), Iwabuchi 762 (Ex. A-4), Suntharalingam (Ex. A-16), and Maruyama (Ex. A-17) (collectively the “BSI Thinning References”).

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, and further in view of any one of the BSI Thinning References, renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, and further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, and further in view of any one of the End Point References, renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, further in view of any one of the End Point

References, and further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, further in view of any one of the End Point References, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Ion Implantation References, and further in view of any one of the BSI Thinning References, renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Ion Implantation References, further in view of any one of the BSI Thinning References, and further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Ion Implantation References, further in view of any one of the BSI Thinning References, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Ion Implantation References, further in view of any one of the BSI Thinning References, and further in view of any one of the End Point References, renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-6.

Ezaki ’519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Ion Implantation References, further in view of any one of the BSI

Thinning References, further in view of any one of the End Point References, and further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2. *See* Ex. A-6.

Ezaki '519 in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Ion Implantation References, further in view of any one of the BSI Thinning References, further in view of any one of the End Point References, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-6.

8. Brady (Ex. A-7)

Brady describes an FSI photodetector having a barrier implanted region of a first conductivity type formed in lieu of an isolation region of a pixel sensor cell that provides physical and electrical isolation of photosensitive elements of adjacent pixel sensor cells of a CMOS imager. The barrier implanted region comprises a first region having a first width and a second region having a second width greater than the first width, the second region being located below the first region. The first region is laterally spaced from doped regions of a second conductivity type of adjacent photodiodes of pixel sensor cells of a CMOS imager.

As explained below, POSAs would have had reasons to combine Brady's photodetector with any one of the Vertically Integrated 3D Imager References to form a three-dimensional imager. The following combinations, based on Brady, render obvious claims 1-2 and 4-9. Exhibit A-7 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

a. BSI embodiments

As discussed in Section III.A.1.f, it was known to use conduction and isolation layers from a FSI photodetector like Brady in a BSI format. As explained at step 1[f] in the accompanying charts these references each describe the process step of thinning the lower

portion of a substrate on a BSI photodetector: Guidash ’256 (Ex. A-1), Uya (Ex. A-3), Iwabuchi 762 (Ex. A-4), Suntharalingam (Ex. A-16), and Maruyama (Ex. A-17) (collectively the “BSI Thinning References”).

Brady in view of any one of the Vertically Integrated 3D Imager References, and further in view of any one of the BSI Thinning References, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-7.

Brady in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, and further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2. *See* Ex. A-7.

Brady in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-7.

Brady in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, and further in view of any one of the End Point References, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-7.

Brady in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, further in view of any one of the End Point References, and further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2. *See* Ex. A-7.

Brady in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the BSI Thinning References, further in view of any one of the End Point References, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-7.

b. FSI embodiments

As demonstrated by at least the Guidash ’256 FSI embodiment, POSAs would also have known to combine Brady with Guidash ’256 to provide a vertically-integrated FSI imager, as follows:

Brady in view of Guidash ’256, further in view of the Lightpipe references, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-7.

Brady in view in view of Guidash ’256, further in view of the Lightpipe references, and further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2. *See* Ex. A-7.

Brady in view of in view of Guidash ’256, further in view of the Lightpipe references, and further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-7.

9. Holm ’008 (Ex. A-8)

Holm ’008 describes methods for providing an integrated photosensing element for use in CMOS imaging applications. The following combinations, based on Holm ’008, render obvious claims 1-2 and 4-8. Exhibit A-8 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Holm ’008 in view of Brady renders obvious claims 1, 4-6, and 8. Ex. A-8.

Holm ’008 in view of Brady, and further in view of Uya (Ex. A-3), Nam (Ex. A-10), or Maruyama (Ex. A-17) renders obvious claim 2. Ex. A-8.

Holm ’008 in view of Brady, and further in view of any one of the Plasma Activation References renders obvious claim 7. Ex. A-8.

10. Cazaux (Ex. A-9)

Cazaux describes an image sensor with a pixel assembly including photodiodes formed in a first substrate, readout electronics formed in a second substrate, and bonding the substrates together. The following combinations, based on Cazaux, render obvious claims 1-2 and 4-9. Exhibit A-9 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Cazaux in view of Maruyama renders obvious claims 1-2, 4-5, 8-9. Ex. A-9.

Cazaux in view of Maruyama, further in view of any one of the Vertically Integrated 3D Imager References, renders obvious claim 6. Ex. A-9.

Cazaux in view of Maruyama, further in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Plasma Activation References, renders obvious claim 7. Ex. A-9.

11. Nam (Ex. A-10)

Nam describes a method of making a FSI image sensor. The following combinations, based on Nam, render obvious claims 1-2 and 4-9. Exhibit A-10 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Nam in view of any one of the Vertically Integrated 3D Imager References renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-10.

Nam in view of any one of the Vertically Integrated 3D Imager References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders obvious claim 2. *See* Ex. A-10.

Nam in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-10.

12. Hynecek '801(Ex. A-11)

Hynacek '801 describes methods for forming a solid state CMOS image sensor with stacked photo-sites, high sensitivity, and low dark current. The following combinations, based on Hynacek, render obvious claims 1-2 and 4-9. Exhibit A-11 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Hynacek '801 in view of any one of the Lightpipe References, further in view of Guidash '256, renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-11, Ex. A-1.

Hynacek '801 in view of any one of the Lightpipe References, further in view of Guidash '256, further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-11, Ex. A-1.

13. Rhodes (Ex. A-12)

Rhodes describes methods for forming a barrier implanted region below an isolation region in a pixel sensor cell for a photodiode. The following combinations, based on Rhodes, render obvious claims 1-2 and 4-9. Exhibit A-12 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Rhodes in view of any one of the Lightpipe References, further in view of Guidash '256 renders obvious claims 1-2, 4-6, and 8-9. *See* Ex. A-12.

Rhodes in view of any one of the Lightpipe References, further in view of Guidash '256, further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-12.

14. Lee ’020 (Ex. A-13)

Lee ’020 describes methods of making CMOS image sensors configured to reduce dark current. The following combinations, based on Lee ’020, render obvious claims 1-2 and 4-9. Exhibit A-13 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Lee ’020 in view of any one of the Lightpipe References, further in view of Guidash ’256, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-13.

Lee ’020 in view of any one of the Lightpipe References, further in view of Guidash ’256, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders obvious claim 2. *See* Ex. A-13.

Lee ’020 in view of any one of the Lightpipe References, further in view of Guidash ’256, further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-13.

15. Patti IEEE (Ex. A-14)

Patti IEEE describes a three-dimensional integrated CMOS sensor where the sensor, comprising a photodiode array, and supporting circuitry, are processed separately then brought together in an integrated vertical stack.

In this analysis, Uya (Ex. A-3), Iwabuchi ’762 (Ex. A-4), Ezaki ’519 (Ex. A-6), Brady (Ex. A-7), Mann (Ex. A-15), or Maruyama (Ex. A-17) (collectively the “Photodetector References”) each disclose photodetectors and unit pixels compatible with Patti IEEE as explained in Ex. A-14. Moreover, Guidash ’256 (Ex. A-1), Uya (Ex. A-3), Iwabuchi 762 (Ex. A-4), Suntharalingam (Ex. A-16), or Maruyama (Ex. A-17) (collectively the “Backside Thinning

References") each disclose thinning the substrate for a BSI sensor by removing a lower portion of the substrate to expose the photodiode.

The following combinations, based on Patti IEEE, render obvious claims 1-2 and 4-9. Exhibit A-14 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Patti IEEE in view of any one of the Photodetector References, and further in view of any one of the Backside Thinning References, renders obvious claims 1, 4-6, and 8.

Patti IEEE in view of any one of the Photodetector References, further in view of any one of the Backside Thinning References, further in view of Uya or Maruyama, renders obvious claim 2.

Patti IEEE in view of any one of the Photodetector References, further in view of any one of the Backside Thinning References, further in view of any one of the Plasma Activation References, renders obvious claim 7.

Patti IEEE in view of any one of Uya (Ex. A-3), Ezaki '519 (Ex. A-6), Brady (Ex. A-7), Mann (Ex. A-15), or Maruyama (Ex. A-17), and further in view of any one of the Backside Thinning References, renders obvious claim 9.

Patti IEEE in view of any one of the Photodetector References, further in view of any one of the Backside Thinning References, further in view of any End Point Reference, renders obvious claims 1, 4-6, and 8.

Patti IEEE in view of any one of the Photodetector References, further in view of any one of the Backside Thinning References, further in view of any End Point Reference, further in view of Uya or Maruyama, renders obvious claim 2.

Patti IEEE in view of any one of the Photodetector References, further in view of any one of the Backside Thinning References, further in view of any End Point Reference, further in view of any one of the Plasma Activation References, renders obvious claim 7.

Patti IEEE in view of any one of Uya (Ex. A-3), Ezaki '519 (Ex. A-6), Brady (Ex. A-7), Mann (Ex. A-15), or Maruyama (Ex. A-17), and further in view of any one of the Backside Thinning References, further in view of any End Point Reference, renders obvious claim 9.

16. Mann (Ex. A-15)

Mann describes an FSI photodetector that reduces reverse bias junction leakage in a photodiode by using a junction isolation region to isolate the photodiode from a trench isolation region. The improved semiconductor device improves image quality for different applications such as stand-alone digital cameras and digital cameras embedded in other imaging devices such as cellular phones and personal digital assistants.

As explained below, POSAs would have had reasons to combine Mann's photodetector with any one of the Vertically Integrated 3D Imager References to form a three-dimensional imager. The following combinations, based on Mann, render obvious claims 1-2 and 4-9. Exhibit A-15 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Mann in view of any one of the Lightpipe References renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-15.

Mann in view of any one of the Lightpipe References, further in view of Uya (Ex. A-3) or Murayama (Ex. A-17) renders obvious claim 2. *See* Ex. A-15.

Mann in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Lightpipe References, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-15.

Mann in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Lightpipe References, further in view of Uya (Ex. A-3) or Murayama (Ex. A-17) renders obvious claim 2. *See* Ex. A-15.

Mann in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Lightpipe References, further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-15.

Mann in view of any one of the Vertically Integrated 3D Imager References, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-15.

Mann in view of any one of the Vertically Integrated 3D Imager References, further in view of Uya (Ex. A-3) or Murayama (Ex. A-17) renders obvious claim 2. *See* Ex. A-15.

Mann in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-15.

Mann in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the End Point References, renders obvious claims 1, 4-6, and 8-9. *See* Ex. A-15.

Mann in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the End Point References, further in view of Uya (Ex. A-3) or Murayama (Ex. A-17) renders obvious claim 2. *See* Ex. A-15.

Mann in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the End Point References, further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-15.

17. Sunthraralingam (Ex. A-16)

Sunthraralingam describes three-dimensional integrated circuit technology that was used to make a vertically integrated CMOS image sensor in which the sensor was formed on one tier, then bonded to circuitry was formed on a circuit tier. Suntharalingam was presented in session 19 at ISSCC 2005 in February 2005 and published in IEEE Xplore on August 29, 2005, as supplemental material to the underlying paper, V. Suntharalingam et al., "Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology," ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005, 2005, pp. 356-357 Vol. 1, doi: 10.1109/ISSCC.2005.1494016 ("ISSCC 2005").

The following combinations, based on Suntharalingam, render obvious claims 1-2 and 4-9. Exhibit A-16 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Sunthraralingam in view of Mann or Brady renders obvious claims 1, 4-6, 8-9. *See* Ex. A-16.

Sunthraralingam in view of Mann or Brady, further in view of Uya or Maruyama, renders obvious claim 2. *See* Ex. A-16.

Sunthraralingam in view of Mann or Brady, further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-16.

Sunthraralingam in view of ISSCC 2005, further in view of Mann or Brady, renders obvious claims 1, 4-6, 8-9. *See* Ex. A-16.

Sunthraralingam in view of ISSCC 2005, further in view of Mann or Brady, further in view of Uya or Maruyama, renders obvious claim 2. *See* Ex. A-16.

Sunthraralingam in view of ISSCC 2005, further in view of Mann or Brady, further in view of any one of the Plasma Activation References, renders obvious claim 7. *See* Ex. A-16.

18. Maruyama (Ex. A-17)

Maruyama describes a method of making a back-illuminated solid-state imaging device wherein no color mixing occurs even if a unit pixel is decreased in size and wherein dark-current generation in an accumulation layer is suppressed. The following combinations, based on Maruyama, render obvious claims 1-2 and 4-9. Exhibit A-17 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Maruyama in view of any one of the Vertically Integrated 3D Imager References renders obvious claims 1-2, 4-6, and 8-9.

Maruyama in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the Plasma Activation References, renders obvious claim 7.

Maruyama in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the End Point references, renders obvious claims 1-2, 4-6, and 8-9.

Maruyama in view of any one of the Vertically Integrated 3D Imager References, further in view of any one of the End Point references, further in view of any one of the Plasma Activation References, renders obvious claim 7.

19. Iwabuchi ’007 (Ex. A-18)

Iwabuchi ’007 describes manufacturing a CMOS image sensor with backside-illuminated photodetectors. Iwabuchi separates the image sensor and signal processing circuitry into different chips, and describes multiple ways to integrate the sensor and signal processing chips,

including through an interposer or by direct bonding. The following combinations, based on Iwabuchi ’007, render obvious claims 1-2 and 4-9. Exhibit A-18 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Iwabuchi ’007 renders obvious claims 1,4-6, and 8-9. Ex. A-18.

Iwabuchi ’007 in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders obvious claim 2. Ex. A-18.

Iwabuchi ’007 in view of any one of the Plasma Activation References renders obvious claim 7. Ex. A-18.

Iwabuchi ’007 in view of any one of the Endpoint References renders obvious claims 1,4-6, and 8-9. Ex. A-18.

Iwabuchi ’007 in view of any one of the Endpoint References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders obvious claim 2. Ex. A-18.

Iwabuchi ’007 in view of any one of the Endpoint References, further in view of any one of the Plasma Activation References renders obvious claim 7. Ex. A-18.

Iwabuchi ’007, in view of any one of the Ion Implantation References, renders obvious claims 1,4-6, and 8-9. Ex. A-18.

Iwabuchi ’007 in view of any one of the Ion Implantation References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders obvious claim 2. Ex. A-18.

Iwabuchi ’007 in view of any one of the Ion Implantation References, further in view of any one of the Plasma Activation References renders obvious claim 7. Ex. A-18.

Iwabuchi ’007 in view of any one of the Ion Implantation References, further in view of any one of the Endpoint References renders obvious claims 1,4-6, and 8-9. Ex. A-18.

Iwabuchi ’007 in view of any one of the Ion Implantation References, further in view of any one of the Endpoint References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17) renders obvious claim 2. Ex. A-18.

Iwabuchi ’007 in view of any one of the Ion Implantation References, further in view of any one of the Endpoint References, further in view of any one of the Plasma Activation References renders obvious claim 7. Ex. A-18.

20. Lee ‘937 (Ex. A-19)

Lee describes manufacturing a solid-state imager with a “3D structure” by bonding a sensor wafer to a circuit wafer. The sensor wafer provides an array of unit pixels, while remaining readout transistors, and additional circuitry, are formed on a second wafer. Lee bonds the wafers together with interconnections including vias and conduction pads taking the image signal to the second wafer from the unit pixel.

The following combinations, based on Lee, render obvious claims 1-2 and 4-9. Exhibit A-19 provides a chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, as well as the reasons to combine references as explained below:

Lee ‘937 renders obvious claims 1, 4-6, 8.

Lee ‘937 in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2.

Lee ‘937 in view of any one of the Plasma Activation References, renders obvious claim 7.

Lee ‘937 in view of Masagaki or Ezaki ’519 (Ex. A-6) renders obvious claims 1, 4-6, 8-9.

Lee ‘937 in view of Masagaki or Ezaki ’519 (Ex. A-6), further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2.

Lee ‘937 in view of Masagaki or Ezaki ’519 (Ex. A-6), further in view of any one of the Plasma Activation References, renders obvious claim 7.

Lee ‘937 in view of any one of the Endpoint References, renders obvious claims 1, 4-6, 8.

Lee ‘937 in view of any one of the Endpoint References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2.

Lee ‘937 in view of any one of the Endpoint References, further in view of any one of the Plasma Activation References, renders obvious claim 7.

Lee ‘937 in view of Masagaki or Ezaki ’519 (Ex. A-6), further in view of any one of the Endpoint References, renders obvious claims 1, 4-6, 8-9.

Lee ‘937 in view of Masagaki or Ezaki ’519 (Ex. A-6), further in view of any one of the Endpoint References, further in view of Uya (Ex. A-3) or Maruyama (Ex. A-17), renders obvious claim 2.

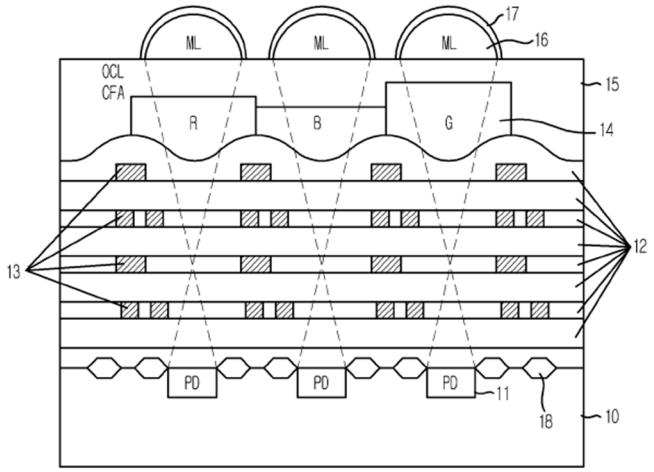
Lee ‘937 in view of Masagaki or Ezaki ’519 (Ex. A-6), further in view of any one of the Endpoint References, further in view of any one of the Plasma Activation References, renders obvious claim 7.

B. Anticipation and Obviousness of U.S. Patent No. 7,868,366

1. Background Knowledge of a POSA

a. CMOS Sensor Design

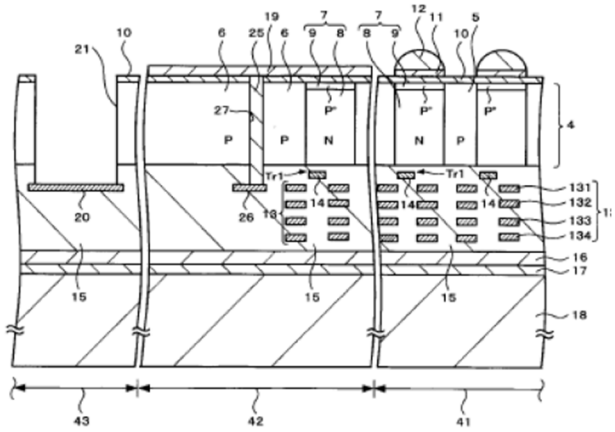
In the mid-2000s, some complementary metal-oxide semiconductor (“CMOS”) image sensors had a single substrate with interconnections above photodiodes. Yun, Figure 1 (below).



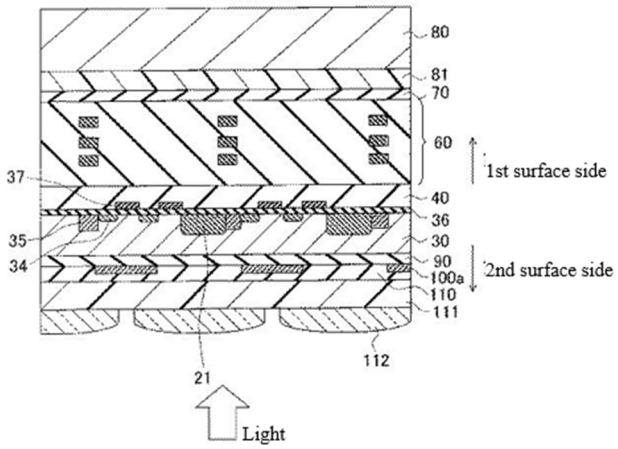
The problem was as image resolution increased, "the size of the unit pixel is gradually reduced, so that the area ratio of the photodiode 11 per unit pixel is reduced." Yun, 8. This "reduced sensitivity with respect to incident light." Yanagida, 1, 3.

One known solution to increase the CMOS sensor efficiency was to flip the CMOS sensor upside-down such that incident light entered from the back side of the silicon, relocating microlens array and color filters to the back side of the silicon substrate as taught by at least Yanagida and Yanagida2.

Yanagida



Yanagida2

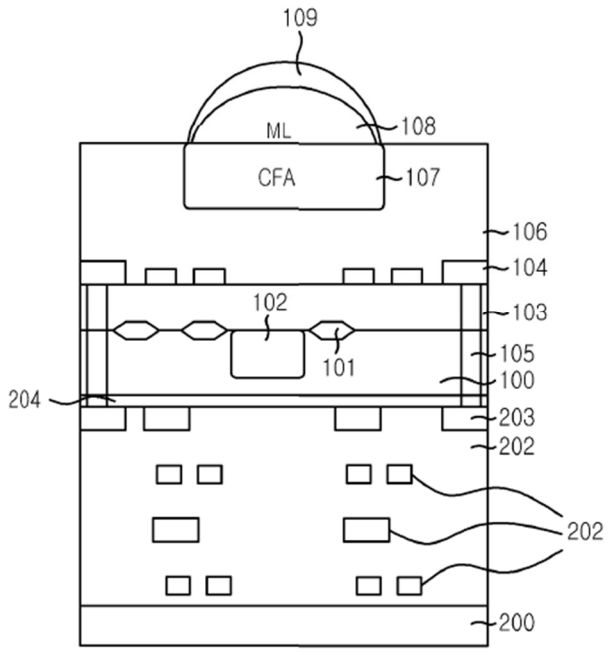


In this configuration, the incident light's optical path is shorter, and there are no metal interconnections in between the microlens and the photodiode—thereby allowing the microlens array to better focus light on individual photodiodes.

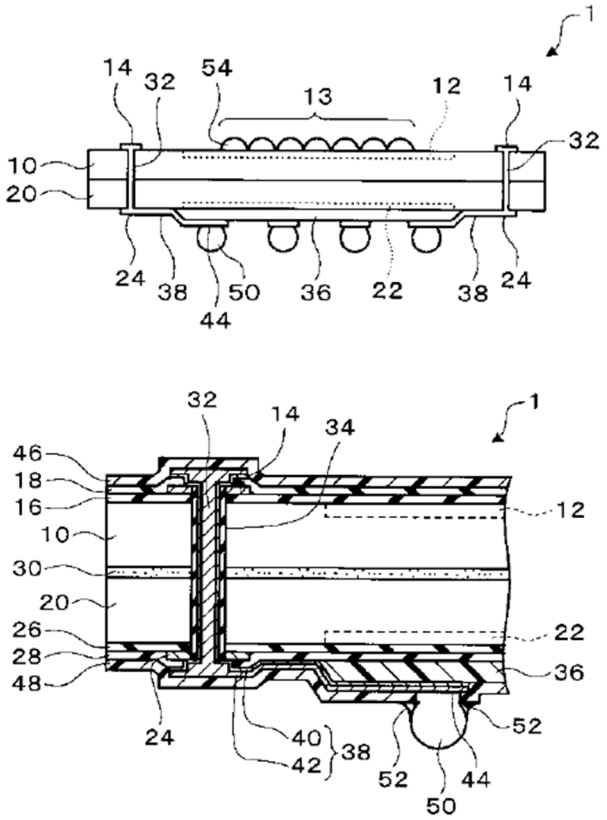
A different known solution to increase the CMOS sensor light focusing efficiency was to relocate the metal interconnects required to form peripheral circuits to a separate substrate stacked underneath the first containing the photodiodes as taught by at least Pyo, Imaoka, Koyanagi, Pyo2, Lee, and Guidash '256.

Pyo

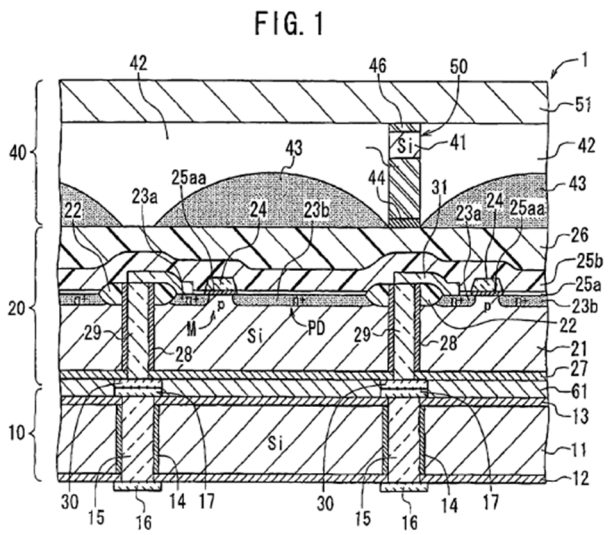
FIG. 3



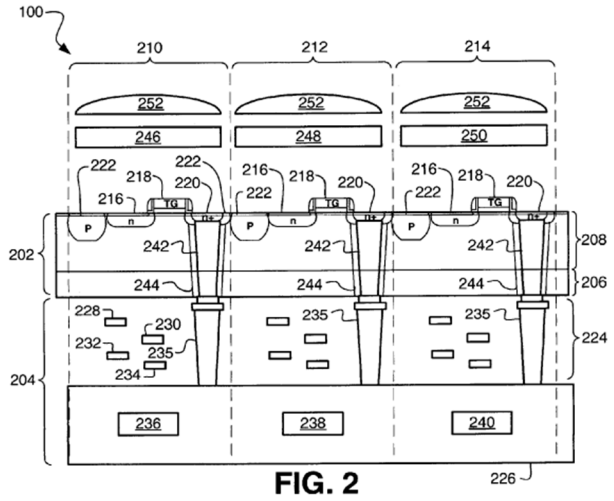
Imaoka



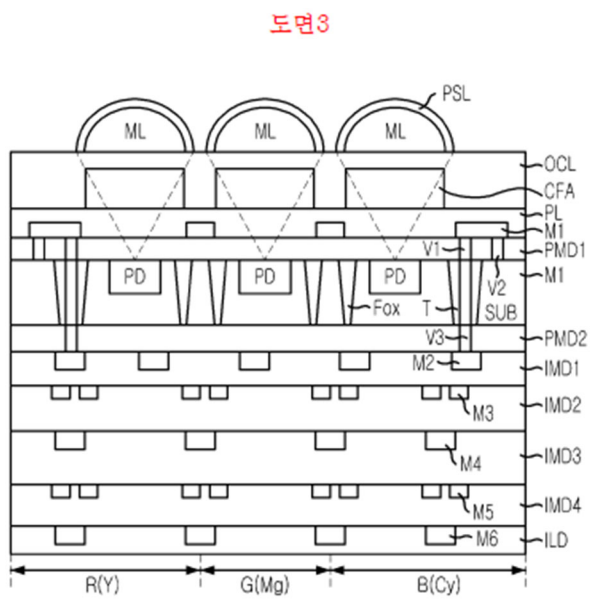
Koyanagi



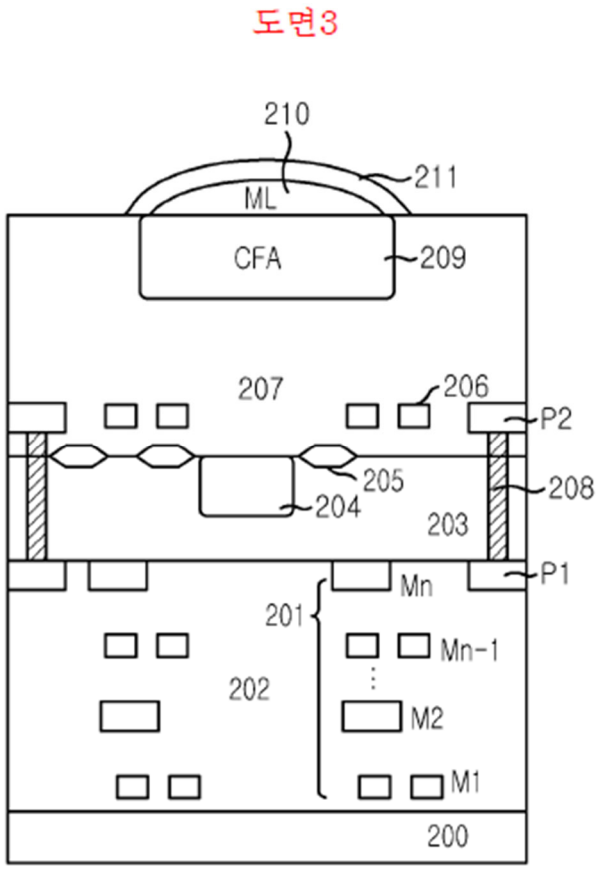
Guidash '256



Lee



Pyo2



In this configuration, the number of metal layers used in the pixel array substrate is reduced by connecting electrical signals from the photodiode array to the interconnects on the second

substrate through one or more conductive vias which are connected to column output lines and/or the peripheral circuits.

b. Copper Interconnections

CMOS image sensors have much the same structure as other types of CMOS chips used in computers, such as memory chips. *See, e.g.*, Yadid-Pecht, 99-100. Where memory chips employ multiple rows and columns of transistors to record and readout electrical data, CMOS image sensors contain rows and columns of photodiodes coupled with transistors to control the collection and readout of the electric signal in the photodiodes. CMOS image sensors also have peripheral analog and digital circuits outside of the pixel array to perform timing and control, analog to digital conversion and other image processing functions. This means that CMOS image sensors can be manufactured by modifying the same processes used to produce memories, microprocessors and other chips. *Id.* ("active pixel sensors (APS) are fabricated in a commonly used CMOS process").

Aluminum, or aluminum-copper alloys, had historically been the dominant interconnect material in semiconductor manufacturing. Pratt, 2. Copper began to be used instead, due to a number of advantages over aluminum and aluminum-copper alloys as described further below.

Lower resistivity. A 2001 textbook by Quirk disclosed that "interconnect wiring resistivity reduces from 2.65 μΩ-cm for aluminum to 1.678 μΩ-cm at 20°C for copper, reducing RC signal delay." Quirk, 305. A 1997 paper by Edelstein disclosed that "Cu wiring has advantages of significantly lower resistance." Edelstein, 8. And a U.S. patent publication to Choi disclosed "copper having a low resistance, thereby minimizing problems." Choi, [0139]. Other references similarly disclose copper's low resistivity over aluminum. Pratt, 2-4; Doering, 4; Brase, 1:15-21.

Reduction in power consumption. Lower resistivity results in narrower lines, which have lower capacitance and can be driven by lower current drivers, which "consume less power." Quirk, 305. The Doering textbook disclosed that "the resistivity advantage of copper over aluminum … allowed for smaller line dimensions." Doering, 4-5. And Pratt discloses "copper results in a power consumption reduction of 30%." Pratt, 5.

Resistance to electromigration. "Electromigration causes transport of the conductor material as a result of high current densities, which can ultimately lead to a void in the conductor." Pratt, 5. "[C]opper has ten to 100 times more resistance to electromigration failures than aluminum." *Id.*; *see also* Quirk, 306; Doering, 5; Brase, 1:23-25.

Fewer processing steps resulting in higher yields. Narrower lines mean "interconnect routing can be simplified, reducing the number of interconnect levels and resulting in fewer process steps." Pratt, 5; Doering, 5 ("the advantages of copper interconnects result in … fewer interconnect metal levels"); Quirk, 328 ("Reducing process steps in wafer fabrication is important for improving the yield of the process, since fewer process steps translate to fewer sources of error that reduce assembly yield.").

Tighter packing density. "Narrower lines permit tighter circuitry packing." Quirk, 306. "As wafer fabrication design rules reduce to 0.15-urn linewidths and below, the increased packing density … leads to improved chip performance." *Id.* One of the reasons tighter packing density leads to improved chip performance is by reducing the dimensions of the circuitry, that increases the aperture to allow light to reach the photodiodes as shown in the figure at paragraph **Error! Reference source not found.**, above at page **Error! Bookmark not defined.**. Tighter circuitry packing is particularly important due to the industry's constant push to miniaturization, as shown in Table 1 of Pratt, reproduced below.

Table 1 Attributes of microprocessor chips at different technology nodes [3]

Year	2001	2003	2005	2007
Technology node	130 nm	100 nm	80 nm	65 nm
Transistors/chip	276 M	439 M	697 M	1106 M
Transistors/cm² (including on-chip SRAM)	38.6 M	61.2 M	97.2 M	154.3 M
Chip size	3.1 cm²	3.1 cm²	3.1 cm²	3.1 cm²
Local wiring pitch	350 nm	245 nm	185 nm	150 nm
Number of metal layers	8	8	10	10
Total interconnect length (excluding global wiring)	7.8 mi	11.1 mi	17.5 mi	21.5 mi
Interconnect RC delay 1 mm line	86 psec	176 psec	256 psec	342 psec

These benefits of using copper interconnects were long recognized, but replacement of aluminum by copper in the early 1990s was an obstacle for semiconductor process engineers, since aluminum is deposited over the entire wafer surface and then patterned by reactive ion etching (RIE), and efforts to apply RIE to copper failed. Pratt, 5.

The breakthrough came in the later 1990s when the damascene and dual-damascene processes were invented and developed. The damascene processes started with a planar dielectric layer. The dielectric layer was first patterned and etched to form trenches and vias where the interconnects would be placed and connected to an underlying layer respectively. Next , copper was used to fill in the trenches and vias in the dielectric. The first working microprocessor using copper was made by IBM in 1997, and by 1998 the process was used in high-volume manufacturing in IBM's Burlington, Vermont, facility. *Id.*

The invention and development of the damascene and dual-damascene processes was of great value because it was easier to manufacture copper lines and vias below about 0.13 to 0.10 µm than fabricating aluminum interconnects at that same narrow width. Choi discloses, for example, that "[w]hen manufacturing semiconductor devices having a pattern size less than about 0.13 µm, aluminum is no longer satisfactory as an electrical interconnection material." Choi, [0007]; *see also* Adkisson, [0007] ("it would be highly desirable to provide a CMOS image sensor having damascene Copper (Cu) metal lines for the metallization (e.g., M1, M2)

levels which would require a thinner interlevel dielectric stack which has less thickness variability due to the elimination of the dielectric CMP step required with subtractive etch AlCu wiring, thus increasing the sensitivity of the pixel array as more light will reach the photodiode.”). The Doering textbook disclosed “aluminum etch to circuit dimensions below 0.10 μm has been difficult.” Doering, 5.

Copper did not have this minimum width limitation. Choi discloses “multi-layered interconnections [using] copper having a low resistance, thereby minimizing problems, … under a process condition having a design rule of about 0.13 micrometer.” Choi, [0139]. As early as 2004, semiconductor fabrication machinery manufacturers were offering tools for copper interconnect fabrication “extendable beyond the 65 nm node” and “[s]everal advanced chipmakers have announced breakthrough technologies down to 45 nm.” Pratt, 7.

The combination of the ease of fabricating narrow copper interconnects and the difficulty of fabricating aluminum interconnects of the same dimensions meant that “nearly all high performance logic devices have made the transition to copper, as of 2004.” Doering, 5. Because CMOS image sensors were commonly made using similar fabrication machinery, using copper interconnections was the natural choice for CMOS image sensors as well in the same time period. Yadid-Pecht, 99-100 (noting image sensors “are fabricated in a commonly used CMOS process” and that the “continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays a viable alternative to the popular charge-coupled devices (CCD) sensor technology”); *see also id*., 88 (“CMOS process development is funded by high-volume sales of standard CMOS logic and memory chips,” hence, “CMOS imaging technology does not have to bear the process development costs and consequently has cheaper process costs than CCD imagers.”).

For example, Gambino discloses fabricating a 0.18 μm CMOS imager sensor that used three levels of copper interconnections. Gambino, 3. The CMOS imager sensor was fabricated using a 0.18 μm foundry process disclosed in 1999 with changes made only "to (1) optimize the photodiode, (2) optimize the optical path through the dielectric stack, and (3) to add color filters and microlenses." *Id.* Yu states "Copper is currently the metal of choice for metal lines 32." Yu, [0005] (disclosing the use of copper for interconnections on a CMOS image sensor).

c. Damascene Process

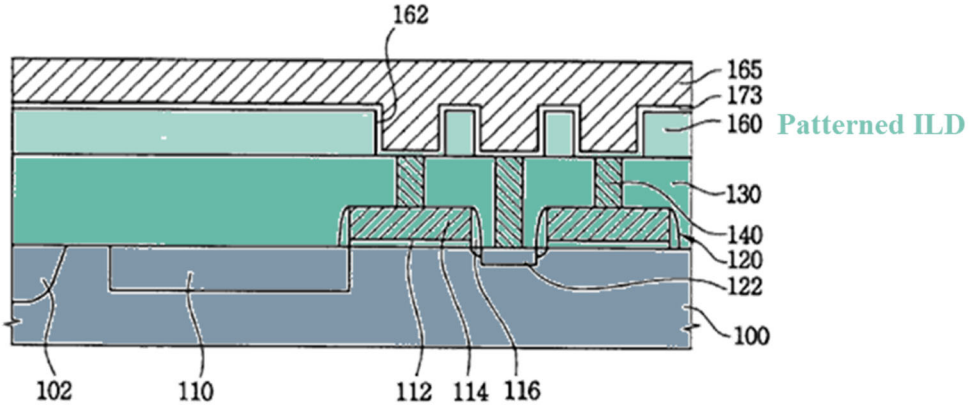
i. Single-Damascene

"The Damascene process makes use of a series of trenches formed in an insulating layer. After the trenches are overfilled with copper, a chemical mechanical polishing process (CMP) is used to remove the overfill." Brase, 1:36-40. In addition to Brase, Choi also teaches how to use the single-damascene process by separately fabricating metal lines and vias. Choi, [0118]-[0123], Figures 5A – 5D; *see also* Yun, Figures 3a-3d, 11-12. Yu also discloses single-damascene copper interconnections. Yu, [0032]-[0033], Figures 2-6, 10-18. The single-damascene process was an "industry standard" and thus a routine means for incorporating copper interconnections. Pratt, 5-7.

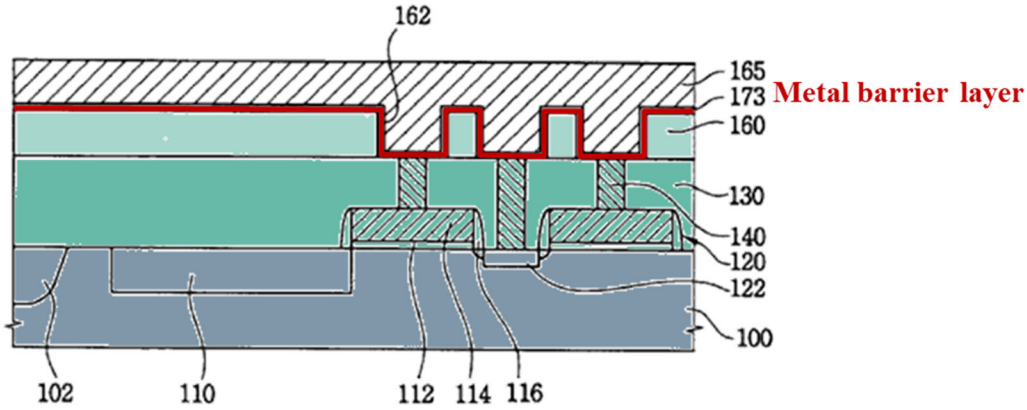
At least Choi ([0118]-[0123], Figures 5A – 5D), Yun (11-12, Figures 3a-3d), and Dublin, 8:1-9:36, Figures 6-10) teach the steps fabricating copper interconnections using a single-damascene process, below.

ILD and Patterning: "[A]n interlayer dielectric layer" ("ILD") is used when fabricating copper interconnections (Choi, [0007]), also referred to as an "insulating interlayer." *Id.*, [0118]. Choi discloses the ILD ("insulating interlayer 160") is formed after which it is "partially removed, e.g., etched using photolithography, to form the lower trench 162." Choi, [0118],

Figure 5A (below, annotated). *See also* Yun, 11-12, Figure 3a (disclosing using a mask to selectively deposit the ILD layer); Dublin 8:1-24, Figure 6 (disclosing etching an ILD layer).

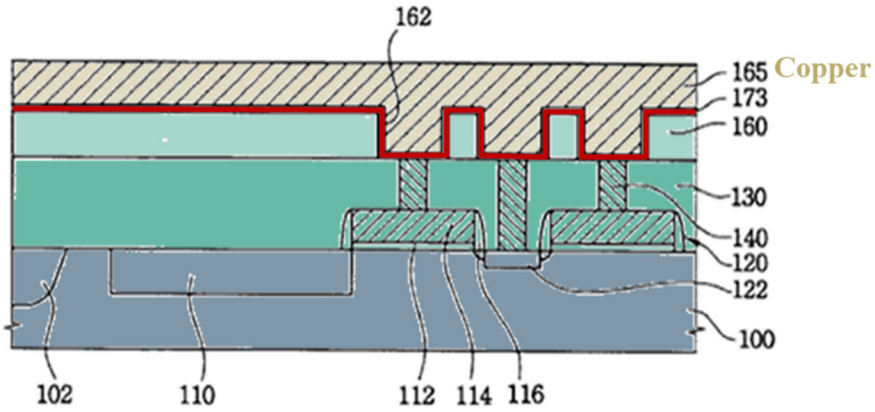


<u>Bottom Metal Barrier Layer</u>: A metal barrier layer is required to "prevent diffusion of the copper into surrounding materials." Choi, [0008]. Choi discloses tantalum (Ta) and tantalum nitride (TaN) as suitable as a barrier. *Id.*, [0066]. Choi discloses the "barrier metal layer 173 is formed along a profile of the lower trench 162 to cover the [ILD]." *Id.*, [0119], Figure 5A (below, annotated). *See also* Yun, 11-12, Figure 3b; Dublin, 8:25-51, Figures 7 and 8 (separately depositing barrier layers on the sides and bottom of the trenching).

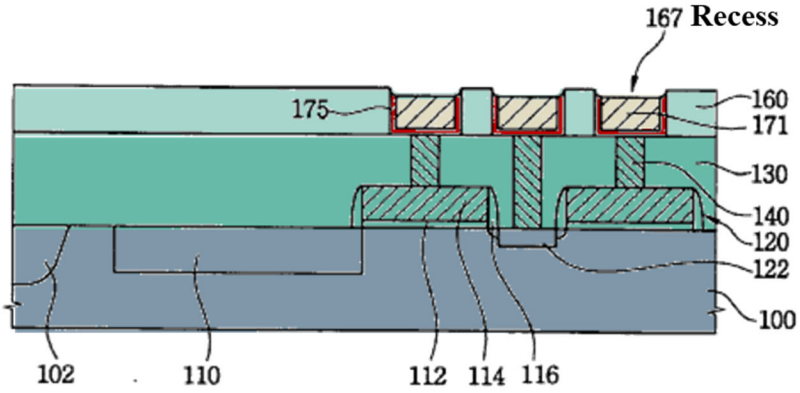


<u>Copper Deposition</u>: Next, a "copper layer 165 is formed on the first barrier metal layer 173." Choi, [119], Figure 5A (below, annotated). *See also* Yun, 11-12, Figure 3b; Dublin, 8:43-

51, Figure 9 (selectively plating copper in trench only, thus not requiring subsequent CMP step, below).

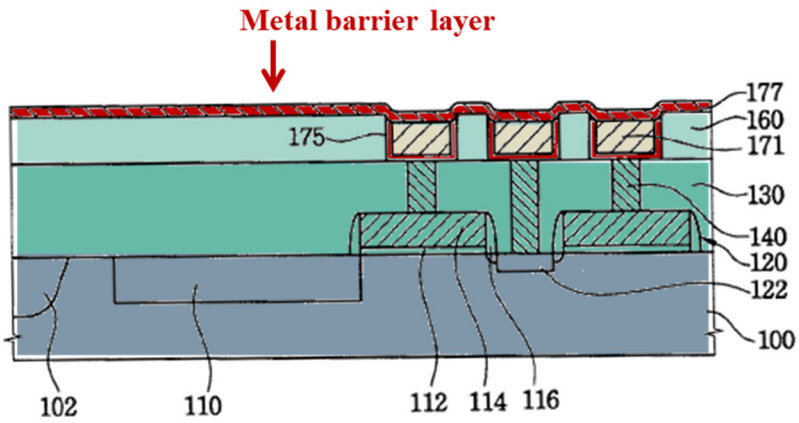


<u>Chemical Mechanical Polishing ("CMP")</u>: The "copper layer 165 is [then] removed, e.g., using CMP, so that the upper surface of the first insulating interlayer 160 is exposed, and a lower copper interconnection 171 is formed." Choi, [0120]. CMP is continued until the "upper surface of the lower copper interconnection 171 is positioned at a position lower than the upper surface of the first insulating interlayer 160," forming a "recess 167." Choi, [0120], Figure 5B (below, annotated). *See also* Yun, 11-12, Figure 3c.

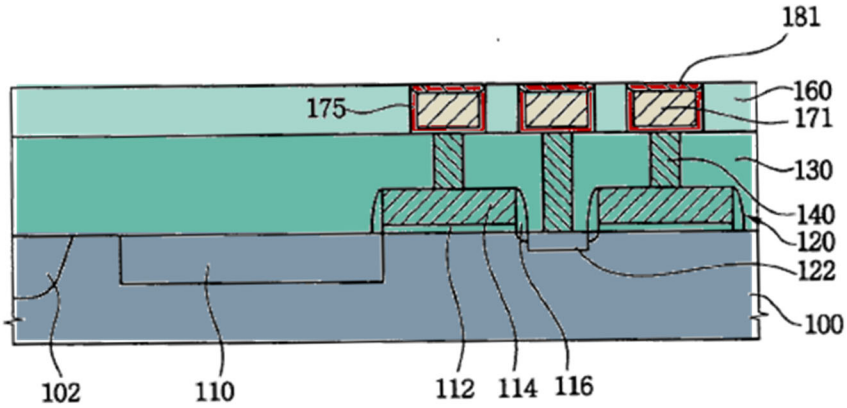


<u>Top Metal Barrier Layer</u>: Next, a "diffusion preventing pattern is formed in the first recess 167." Choi, [0121]-[0122], Figure 5C (Figure 5B (below, annotated). Choi disclosed tungsten and tungsten nitride were suitable. Choi, [0122]. *See also* Yun, 11-12, Figure 3d;

Dublin, 8:52-9:7 (selectively depositing the barrier layer so as to not require subsequent planarization step, below).



<u>Planarization</u>: Next is planarizing the "diffusion preventing layer 177," "e.g., by CMP, such that [it] remains only in the first recess 167, thereby forming the first diffusion preventing pattern 181 on the lower copper interconnection 171." Choi, [0123], Figure 5D (below, annotated). *See also* Yun, 11-12, Figure 3d.



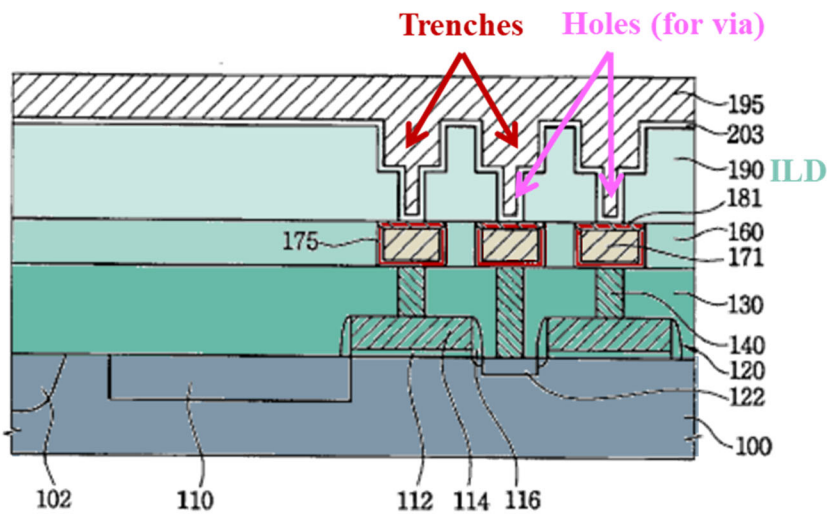
ii. Dual-Damascene

The "dual Damascene process requires that both vias and trenches be etched into the … insulating layers between different levels of the conductive interconnection pattern … before the copper is deposited … during one deposition process … so that there is a metal to metal contact between the first level copper lines and the first vias." Brase, 4:29-40. In addition to Brase,

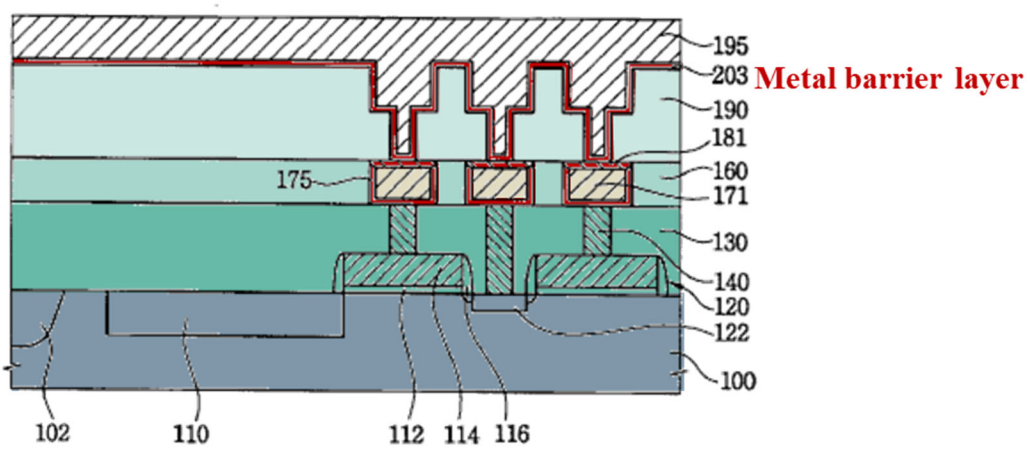
Choi also teaches how to implement the dual-damascene process by fabricating the metal lines and vias together. Choi, [0124]-[0132], Figures 5E – 5G; *see also* Quirk, 326-328 (teaching the dual-damascene process); Yun, Figures 3g-3j, 11-12. Yu also discloses dual-damascene copper interconnections. Yu, [0032]-[0033], Figures 2-6, 10-18. The dual-damascene process was also ubiquitous by at least 2004. As of at least 2001, "the dual-damascene process became the consensus process for copper metallurgy" and thus a routine means for incorporating copper interconnections. Quirk, 326; Doering, 4 ("A variation of the damascene process, known as the dual damascene process, has been widely implemented as the most cost-effective means of producing copper interconnect circuitry.").

At least Choi ([0124]-[0132], Figures 5E – 5G), Yun (11-12, Figures 3e-3j), and Quirk, 326-328) teach the steps fabricating copper interconnections using a dual-damascene process, below.

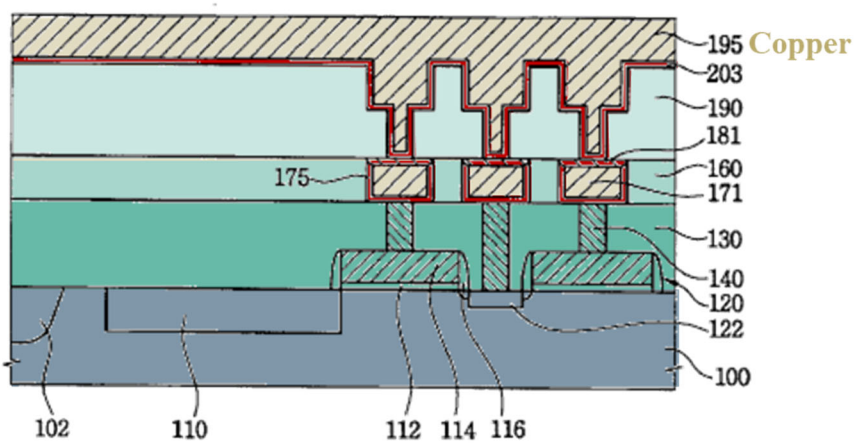
ILD and Patterning: The process starts with forming an "insulating interlayer 190" which is then "partially removed, e.g., etched using photolithography." Choi, [0124]-[0125], Figure 5E (below, annotated). While Choi patterns the trenches and holes in the same etch, POSAs would have known two etches could be used and in various orders interchangeably (*see, e.g.*, Quirk, 326-328, Brase, 1:47-2:6, 2:7-2:10) but that the result would be the same. *See also* Yun, 11-12, Figure 3g (fabricating ILD in an additive process).



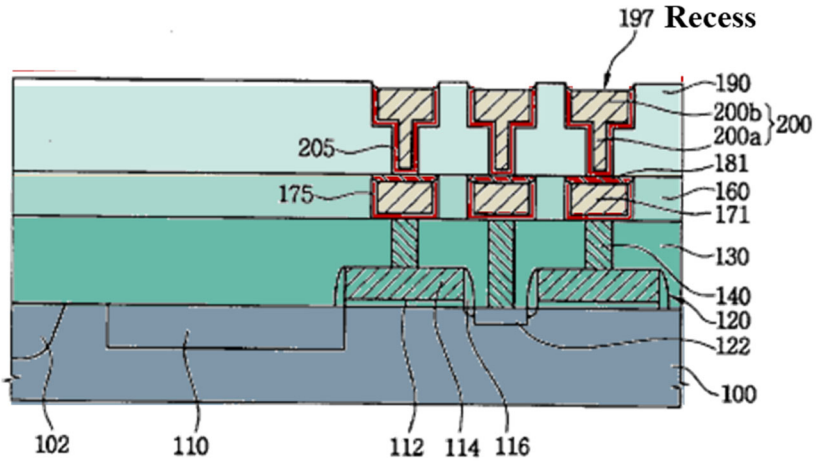
Bottom Metal Barrier Layer: Choi next deposits a metal barrier layer over the patterned ILD. Choi, [0126], Figure 5E (below, annotated). Choi discloses tantalum (Ta) and tantalum nitride (TaN) as suitable as a barrier. *Id.*, [0066]. *See also* Yun, 11-12, Figure 3h; Quirk, 326-328.



Copper Deposition: Next, copper fills the trenches and holes ("vias"). Choi, [0126], Figure 5E (below, annotated). See also Yun, 11-12, Figure 3j; Quirk, 326-328.



<u>Chemical Mechanical Polishing ("CMP")</u>: Choi uses CMP to create a recess (197) above the copper interconnections. Choi, [0128], Figure 5F (below, annotated). See also Yun, 11-12 ("excessive polishing is performed so that the copper layer 313 and the third barrier layer 312 filled in the upper trench are recessed"), Figure 3i; Quirk, 326-328.



<u>Top Metal Barrier Layer</u>: Choi next deposits a metal barrier layer across the surface (although "not shown" in Choi's figures), using the same materials as for the first level. Choi, [0129]. Choi disclosed tungsten and tungsten nitride were suitable. Choi, [0122]. *See also* Yun, 11-12, Figure 3i (below).

FIG. 3i

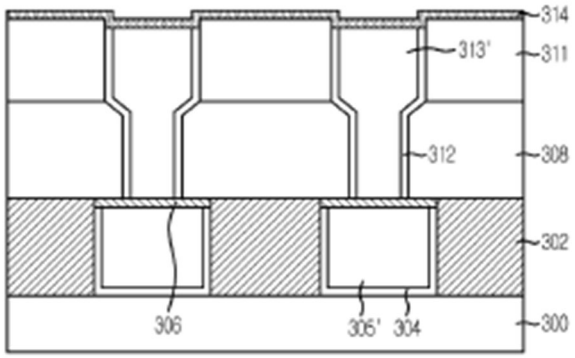
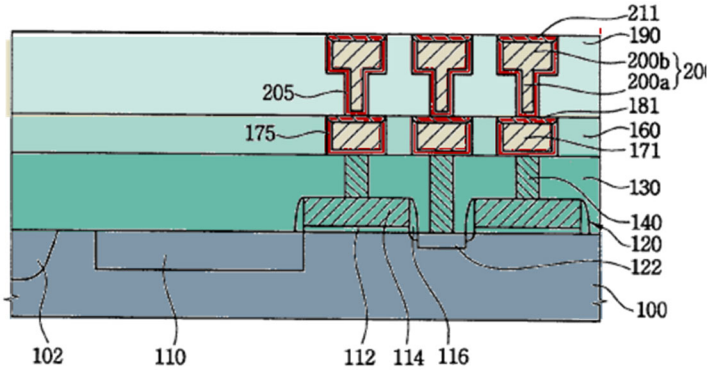


FIG. 3j

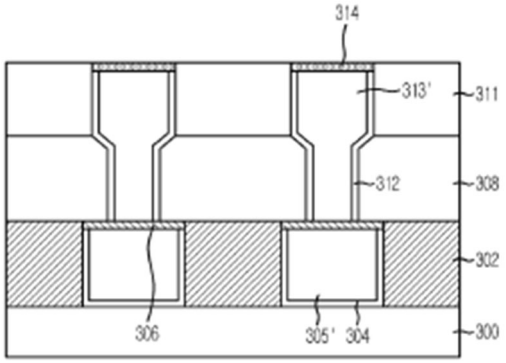
<u>Planarization</u>: Choi then planarizes the surface. Choi, [0129], Figure 5G (below, annotated). *See also* Yun, 11-12, Figure 3j (below).

<u>Choi</u>



<u>Yun</u>

FIG. 3j



d. Interconnection Barrier Layers

The use of barrier layers for interconnections has long been known. For example, Okuda discloses using a TiN barrier layer for tungsten (W) interconnections. Okuda, [0090]-[0094], Fig. 11. The barrier layers are "effective to effectively reduce the natural oxide film after opening of the contact window, maintaining good contact condition, and to simultaneously realize stabilization and close contact conduction of the upper metal wiring layer." *Id.*, [0105].

Yuzurihara discloses the use of barrier metals for aluminum, copper, and tungsten interconnections. Yuzurihara, 13:46-14:7, Fig. 10.

Similarly, one known step in both the single- and dual-damascene processes was depositing a metal barrier layer both before copper plating and after planarizing the copper. Choi (Ex. 1007), [0008]; *see also id*., [0126] (A "barrier metal layer 203 is formed along a profile of the first trench and the first via to cover the second insulating interlayer 190."), Figure 5E; Quirk, 308, see also id. 327 ("7. Deposit barrier metal"); Yun, Figures 3b, 3c, 3h, 3i, 11-12; Dublin, Figs. 2, 5, 8, 10, 5:63-6:35, 7:42-67, 8:39-9:36; Gambino, 7; Yu, [0005] ("Using copper typically requires barrier layers. Also, when forming the metal lines 32 using a copper damascene or dual-damascene method, it is typically desirable to use barrier layers 42 for copper diffusion barrier.").

It was common for the metal barrier layer on top of the copper interconnection to be deposited in a recess above the copper interconnection such that the top surface of the barrier layer and the top surface of the surrounding interlayer dielectric were flush. *See, e.g.* Choi, [0128], Figure 5F; Yun, 12 ("excessive polishing is performed so that the copper layer 313 and the third barrier layer 312 filled in the upper trench are recessed"), Figure 3i; Yu Figures 2-6, 10-18, .

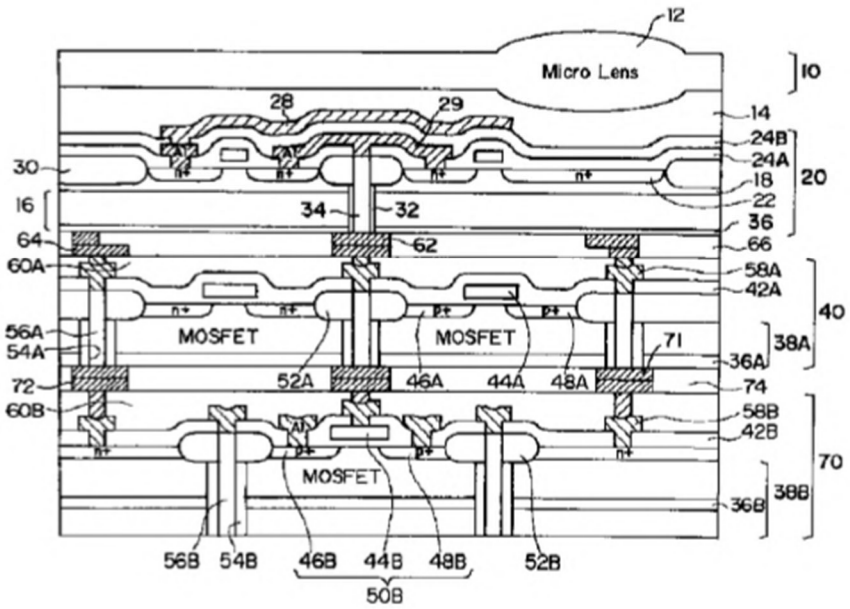
As early as 1997, a "variety of materials [were] known for forming diffusion barriers on copper." Dublin (Ex. 1008), 2:25-28. Such materials included tungsten (W) and tungsten nitride (WN) (Choi, [0071]), tantalum (Ta) and tantalum nitride (TaN) (*id*., [0066]), and others such as titanium tungsten alloy (TiW) (Dublin, 2:25-28). *See also* Quirk, 308-309 (listing copper barrier metals). Of the known barrier materials, cobalt tungsten phosphide alloy (CoWP) was known to "significantly enhance[] the barrier properties" and was "preferred since copper can be

electrolessly deposited on CoWP without the need for activation of the CoWP material surface for fabricating subsequent layers of lines and vias. Dublin, 3:1-7. Such CoWP barrier materials were used for copper interconnections in CMOS image sensors as well. Gambino, 7; Yu, [0008], [0033], claims 5 and 18.

e. Thru-Silicon Vias ("TSVs")

In implementing stacked substrate sensor configurations, POSAs knew how to etch or otherwise form thru-silicon via holes to electrically connect the image sensor with the logic chip. *E.g.*, Tezzaron Sensor; Koyanagi2, [0024] ("a trench (deep groove) is provided on the photoelectric conversion substrate 20, the trench penetrating through the element isolation film 30 until it reaches the rear surface of the photoelectric conversion substrate 20. Note that such a trench can be formed by inductively coupled plasma etching or the like. An insulation film 32 is formed on the inner surface of the trench, and the inside of the trench is filled with a conductive material to form embedded wiring 34."), Fig. 5 (below).

[FIG. 5]



POSAs knew how make a hole partially through the silicon, for example by etching. *See, e.g.* Patti-IEEE, 1217-1221 (disclosing etching for form the hole for the "Super-Contact," below);

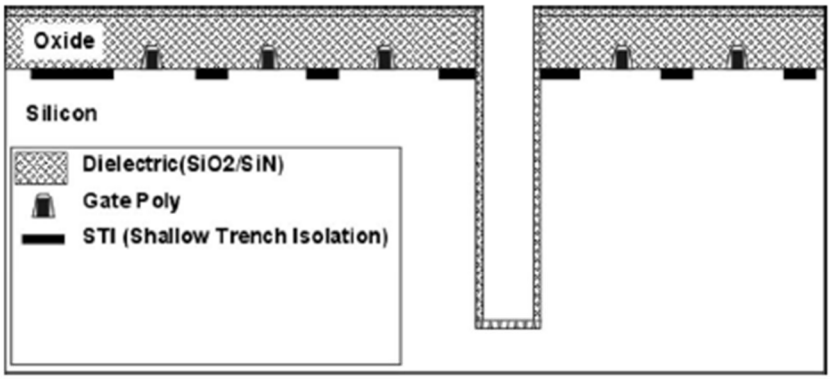
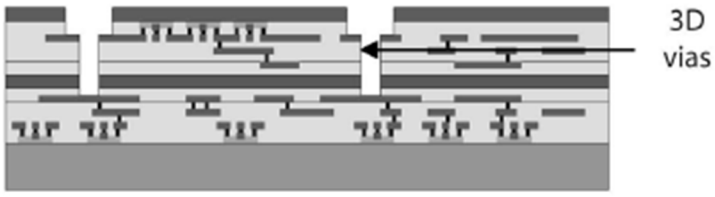


Fig. 6. ***The vertical "Super-Contact" is etched through the oxide and into the silicon substrate approximately 6 μm. The walls are lined with SiO2/SiN.***

Burns, 2508 (disclosing using etching to create "3-D vias" connecting multiple stacked SOI substrates, below);



(c)

Ramm, 160 (disclosing fabricating "interchip vias" as follows).

> Prior to wafer stacking, the interchip vias are prepared on the top wafer by etching through all dielectric layers, followed by a typically 12 pm deep silicon trench etch into the substrate. The top wafer is then adhesively bonded to a handling wafer and thinned with high uniformity until the trenches are opened from the rear. The front of the bottom wafer is planarised and coated with polyimide, which serves as an intermediate layer. The stabilized top wafer and the primed bottom wafer are then optically adjusted and stacked. After bonding at approximately 400 "C, the handling wafer is removed, leaving the desired wafer stack that can be further processed like a standard silicon wafer in a CMOS line. The

interchip vias are opened to a metallization level of the bottom wafer using a Si_3N_4 layer as hard mask. For lateral via isolation, a dielectric spacer technique is applied wing highly conformal CVD of 03/TEOS-oxide and the interchip vias are metallized by refilling with highly conformal CVD of TiNW bilayer. Subsequently, a W etch black process is applied for W plug formation. The lateral electrical connection of the metallized interchip via with the metal level of the top wafer is done by opening contact windows on the top wafer followed by a standard metallization (e.g., TiN/AlSiCu) and passivation. The schematic cross section of the vertically integrated device stack is shown in Figure 2. Finally, the bond pads tue opened and the 3D-integrated devices can be tested, separated and mounted by use of standard procedures.

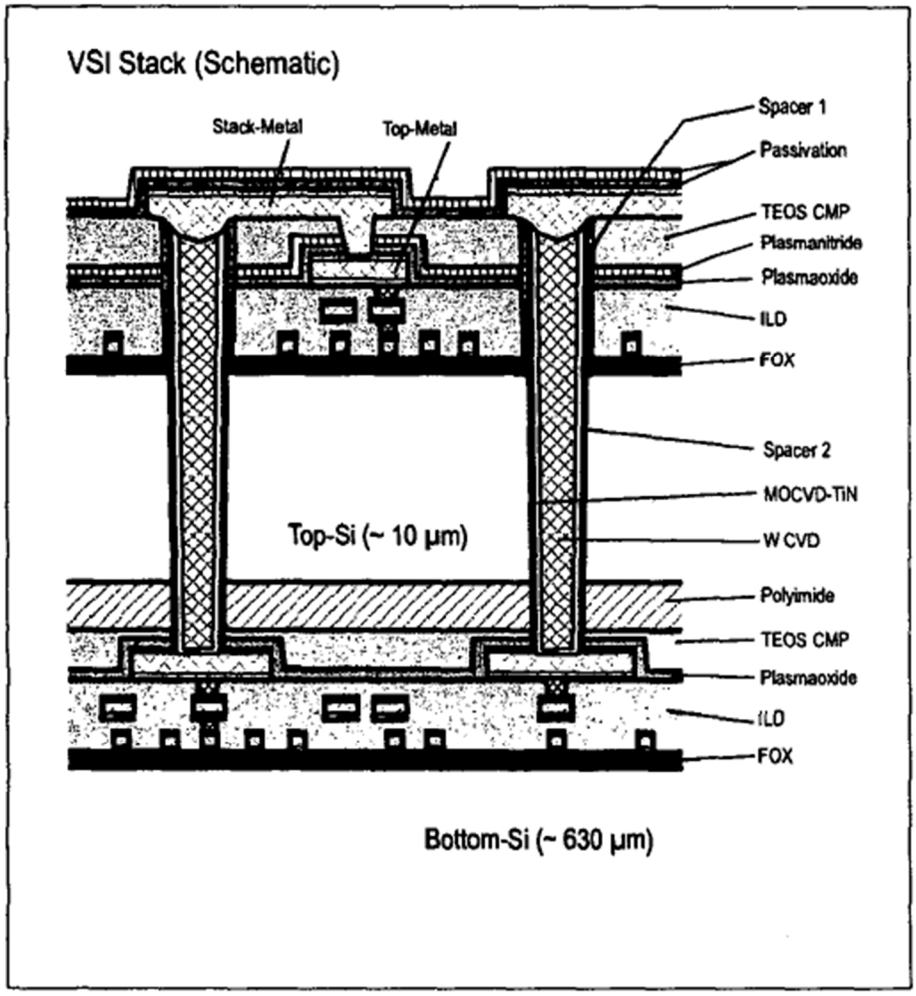


Fig. 2: ICV technology – schematic of a vertically integrated device stack

See also Suntharalingam (disclosing 3-D vias).

2. Koyanagi (Ex. B-1)

a. Koyanagi in view of POSAs' Knowledge Renders Claims 1 and 8 Obvious

Koyanagi in view of POSAs' knowledge renders claims 1 and 8 obvious. As set out in Exhibit B-1, Koyanagi discloses each element of claims 1and 8 except for a color filter (claim 1) and a second substrate with metal interconnections for a power line (claim 8).

Modifying the Koyanagi image sensor by adding a color filter on the first interlayer dielectric on the unit pixel would have been obvious to a POSA because color image sensors were ubiquitous by 2007. *See, e.g.* Pyo, 4 (disclosing a CMOS sensor with "a color filter array"), 5 (noting "color filter array 107" in Figure 3), Figure 3; Imaoka, [0013] (disclosing a CMOS sensor with an "optical part 13" with a "color filter (not illustrated)," "formed between the micro-lenses 54 and the light-receiving elements"), Figure 1; Guidash '256, 5:17-28 ("Color filters 246, 248, 250 are formed over sensor wafer 202 and are used to filter the bandwidth of incident light received by each photodetector 216"), Figure 2; Yanagida2, [0035] ("On the protective film 110, a color filter 111 is formed to pass only light in a desired wavelength region. In addition, on the color filter 111, an on-chip lens 112 is formed to focus the incident light onto the photodiode 21.").

Modifying the Koyanagi image sensor by adding interconnections for a power line associated with the second substrate would have been obvious because POSAs would have understood the desirability of incorporating a power line to make the Koyanagi image sensor operational. An obvious place to locate such interconnection for a power line would be in the output layer with the signal interconnections. *See, e.g.* Guidash '256, 2:33-38 ("The Support wafer includes conductive interconnects and additional analog and digital circuits used by the active pixel sensor. Examples of the additional circuits formed on the Support circuit wafer

include, but are not limited to, timing generators, control circuitry such as transfer gate drivers, decoders, output circuits, and power supplies."); Yanagida2, [0027] ("“The reset transistor 25 is connected between the power supply Vdd and the floating diffusion FD. When a reset signal is given to the gate, the potential of the floating diffusion FD is reset to the potential of the power supply Vdd. These operations are performed simultaneously for each pixel in a row, since the gates of the transfer transistor 22, address transistor 24, and reset transistor 25 are connected on a row basis.").

Such modification would involve combining prior art elements according to known methods to yield predictable results and simple substitution of known elements.

b. Koyanagi in view of Any One of Choi, Yun, Dublin, or Yu and POSAs' Knowledge Renders All Asserted Claims Obvious

Koyanagi in view of any one of Choi, Yun, Dublin, or Yu and POSAs' knowledge renders claims 1, 2, and 4-8 obvious.

Claims 1 and 8: It would have been obvious to include a color filter on the first interlayer dielectric on the unit pixel and an interconnection for a power line for the reasons discussed in Part III.B.2.a. To the extent that VisionX argues, or it is otherwise found, that Koyanagi does not disclose a pre-metal dielectric on the first semiconductor substrate, a first via penetrating the pre-metal dielectric, a first interlayer dielectric on the pre-metal dielectric including the first via, a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel, and/or a conductive barrier layer on the first metal interconnection, it would have been obvious to modify the teachings of Koyanagi to additionally include such limitations based on implementing Koyanagi's conductive plug (15), microbump electrodes (16, 17, and 30), conductive plug (29), and conductive wiring film (31) (collectively,

"interconnections") in copper using the common and well-known single-or dual-damascene processes and structures disclosed by each of Choi, Yun, Dublin, and Yu.

Koyanagi does not disclose the material used for its interconnections. As of 2007, however, there were only a few natural choices for POSAs to select to make interconnections, including copper. POSAs would have had reasons to pick copper over the alternatives, such as aluminum or tungsten (*i.e*. lower resistivity, reduced power consumption, resistance to electromigration, and tighter packing density). *See* Part III.B.1.b. And in implementing Koyanagi's interconnections in copper, POSAs would have used the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because such processes had become the natural choice for fabricating copper interconnections (lines, pads, and vias) by the date of the alleged invention of the '366 patent. *See* Part III.B.1.c. POSAs could have readily implemented Koyanagi's interconnections in copper by using either the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because applying those processes to create copper interconnections had been well known in both CMOS chip manufacturing generally (*see* Part III.B.1.c) as well as specifically for CMOS image sensors. *See generally* Gambino; Adkisson.

When implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Koyanagi's interconnections out of copper, the resulting modified Koyanagi sensor would have a pre-metal dielectric on the first semiconductor substrate, a first via penetrating the pre-metal dielectric, a first interlayer dielectric on the pre-metal dielectric including the first via, a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel, and a conductive barrier layer on the first metal interconnection, satisfying every limitation of claims 1 and 8, rendering those claims obvious. *See* Part III.B.1.c; Exhibit B-1.

Claims 2 and 4-7: Moreover, when implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Koyanagi's interconnections out of copper, the resulting modified Koyanagi sensor would have additionally had:

- A first metal interconnection comprising copper (Cu);
- A first metal interconnection with a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference;
- A second metal interconnection comprising copper (Cu);
- A conductive barrier layer with a top surface substantially even with the top surface of the first interlayer dielectric; and
- A first via and a second via comprising the same material (copper).

See Part III.A.3-4. The modified Koyanagi sensor would, therefore, have satisfied every limitation of claims 2 and 4-7, rendering those claims obvious.

3. Guidash '256 (Ex. B-2)

a. Guidash '256 in view of Any One of Choi, Yun, Dublin, or Yu Renders All Asserted Claims Obvious

Guidash '256 in view of any one of Choi, Yun, Dublin, or Yu renders claims 1, 2, and 4-8 obvious.

Claims 1 and 8: Guidash '256 does not mention a conductive barrier layer on the first metal interconnection, but as of 2007, there were only a few natural choices for POSAs to select to make interconnections, including copper. *See* Part III.B.1.b. POSAs would have known that it would have been highly desirable to add a conductive barrier layer when implementing Guidash's interconnections in copper. *See* Part III.B.1.d.

Guidash ’256 does not disclose the material used for its metal interconnect layers (228, 230, 232, 234), inter-wafer connectors (104, 235 and 242), and transfer gate interconnect (404) (collectively, “interconnections”). As of 2007, however, there were only a few natural choices for POSAs to select to make interconnections, including copper. POSAs would have had reasons to pick copper over the alternatives, such as aluminum or tungsten (*i.e*. lower resistivity, reduced power consumption, resistance to electromigration, and tighter packing density). *See* Part III.B.1.b. And in implementing Guidash ’256’s interconnections in copper, POSAs would have used the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because such processes had become the natural choice for fabricating copper interconnections (lines, pads, and vias) by the date of the alleged invention of the ’366 patent. *See* Part III.B.1.c. POSAs could have readily implemented Guidash ’256’s interconnections in copper by using either the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because applying those processes to create copper interconnections had been well known in both CMOS chip manufacturing generally (*see* Part III.B.1.c) as well as specifically for CMOS image sensors. *See generally* Gambino; Adkisson.

When implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Guidash’256’s interconnections out of copper, the resulting modified Guidash ’256 sensor would have a pre-metal dielectric on the first semiconductor substrate, a first via penetrating the pre-metal dielectric, a first interlayer dielectric on the pre-metal dielectric including the first via, a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel, and a conductive barrier layer on the first metal interconnection, satisfying every limitation of claims 1 and 8, rendering those claims obvious. *See* Part III.B.1.c; Exhibit B-2.

Claims 2 and 4-7: Moreover, when implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Guidash '256's interconnections out of copper, the resulting modified Guidash '256 sensor would have additionally had:

- A first metal interconnection comprising copper (Cu);
- A first metal interconnection with a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference;
- A second metal interconnection comprising copper (Cu);
- A conductive barrier layer with a top surface substantially even with the top surface of the first interlayer dielectric; and
- A first via and a second via comprising the same material (copper).

See Part III.B.1.c. The modified Guidash '256 sensor would, therefore, have satisfied every limitation of claims 2 and 4-7, rendering those claims obvious.

4. Yanagida2 (Ex. B-3)

a. Yanagida2 Anticipates Claims 1, 4, 6, and 8

As set forth in Exhibit B-3, Yanagida2 anticipates claims 1, 4, 6, and 8.

b. Yanagida2 in view of Any One of Choi, Yun, Dublin, or Yu Renders All Asserted Claims Obvious

Yanagida2 in view of any one of Choi, Yun, Dublin, or Yu renders claims 1, 2, and 4-8 obvious.

Claims 1 and 8: To the extent that VisionX argues, or it is found, that Yanagida2 does not disclose a pre-metal dielectric on the first semiconductor substrate, a first via penetrating the pre-metal dielectric, a first interlayer dielectric on the pre-metal dielectric including the first via,

a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel, and/or a conductive barrier layer on the first metal interconnection, it would have been obvious to modify the teachings of Yanagida2 to include such additional limitations based on implementing Yanagida2's 1st contact (C1), 2nd contact (C2), wiring layer (60), and conductive layer (102) (collectively, "interconnections") in copper using the common and well-known single-or dual-damascene processes and structures disclosed by each of Choi, Yun, Dublin, and Yu.

Yanagida2 does not disclose the material used for its interconnections. As of 2007, however, there were only a few natural choices for POSAs to select to make interconnections, including copper. POSAs would have had reasons to pick copper over the alternatives, such as aluminum or tungsten (*i.e*. lower resistivity, reduced power consumption, resistance to electromigration, and tighter packing density). *See* Part III.B.1.b. And in implementing Yanagida2's interconnections in copper, POSAs would have used the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because such processes had become the natural choice for fabricating copper interconnections (lines, pads, and vias) by the date of the alleged invention of the '366 patent. *See* Part III.B.1.c. POSAs could have readily implemented Yanagida2's interconnections in copper by using either the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because applying those processes to create copper interconnections had been well known in both CMOS chip manufacturing generally (*see* Part III.B.1.c) as well as specifically for CMOS image sensors. *See generally* Gambino; Adkisson.

When implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Yanagida2's interconnections out of copper, the resulting modified Yanagida2 sensor would have a pre-metal dielectric on the first

semiconductor substrate, a first via penetrating the pre-metal dielectric, a first interlayer dielectric on the pre-metal dielectric including the first via, a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel, and a conductive barrier layer on the first metal interconnection, satisfying every limitation of claims 1 and 8, rendering those claims obvious. *See* Part III.B.1.c; Exhibit B-3.

Claims 2 and 4-7: Moreover, when implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Yanagida2's interconnections out of copper, the resulting modified Yanagida2 sensor would have additionally had:

- A first metal interconnection comprising copper (Cu);
- A first metal interconnection with a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference;
- A second metal interconnection comprising copper (Cu);
- A conductive barrier layer with a top surface substantially even with the top surface of the first interlayer dielectric; and
- A first via and a second via comprising the same material (copper).

See Part III.B.1.c. The modified Yanagida2 sensor would, therefore, have satisfied every limitation of claims 2 and 4-7, rendering those claims obvious.

5. Pyo2 (Ex. B-4)

a. Pyo2 in view of POSAs' Knowledge Renders Claims 1, 2, 4, 5, 7 and 8 Obvious

Pyo2 in view of POSAs' knowledge renders claims 1, 2, 4, 5, 7, and 8 obvious. As set out in Exhibit B-4, Pyo2 discloses each element of those claims except for a barrier layer on the

first metal interconnection (claim 1) and a second substrate with metal interconnections for signal and power lines (claim 8).

Pyo2 discloses that its interconnections may be made of copper. *E.g*. Pyo2 at 4 (The "plurality of transistors and the plurality of metal wirings 201 (M1 to Mn) are connected to each other through pads P1 and P2, and the via contact 208 comprises a metal such as tungsten, aluminum, or copper." (3). The "metal wirings 201 (M1 to Mn) are formed using copper, aluminum, or the like."). POSAs implementing Pyo2 would have selected one of these metals for the wiring (206) and pads (P2), including using copper. POSAs would have known, however, that it would have been desirable to encapsulate the copper interconnections in a conductive barrier layer. *See* Part III.A.4. Thus, in implementing copper wiring in Pyo2, POSAs would have incorporated a conductive barrier layer on the copper interconnections (206 and P2).

Modifying the Pyo2 image sensor by adding interconnections for signal and power lines associated with the second substrate would have been obvious because POSAs would have understood the desirability of incorporating an external signal line and a power line to make the Pyo2 image sensor operational. An obvious place to locate such interconnections would be in the output layer with the signal interconnections. *See, e.g.* Guidash '256, 2:33-38 ("The Support wafer includes conductive interconnects and additional analog and digital circuits used by the active pixel sensor. Examples of the additional circuits formed on the Support circuit wafer include, but are not limited to, timing generators, control circuitry such as transfer gate drivers, decoders, output circuits, and power supplies."); Yanagida2, [0027] (""The reset transistor 25 is connected between the power supply Vdd and the floating diffusion FD. When a reset signal is given to the gate, the potential of the floating diffusion FD is reset to the potential of the power supply Vdd. These operations are performed simultaneously for each pixel in a row, since the

gates of the transfer transistor 22, address transistor 24, and reset transistor 25 are connected on a row basis.”).

Such modification would involve combining prior art elements according to known methods to yield predictable results and simple substitution of known elements.

b. Pyo2 in view of Any One of Choi, Yun, Dublin, or Yu and the Knowledge of a POSA Renders All Asserted Claims Obvious

Pyo2 in view of any one of Choi, Yun, Dublin, or Yu and the knowledge of a POSA renders claims 1, 2, and 4-8 obvious.

Claims 1, 2, 4, 5, 7, and 8: It would have been obvious to include interconnections for an external signal line and a power line as part of the second substrate for the reasons explained in Part III.B.5.a. To the extent that VisionX argues, or it is found, that Pyo2 does not disclose using copper for the second via and second metal interconnections, a pre-metal dielectric on the first semiconductor substrate, a first copper via penetrating the pre-metal dielectric, a first interlayer dielectric on the pre-metal dielectric including the first via, a first copper metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel, a first metal interconnection with a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference, and/or a conductive barrier layer on the first metal interconnection, it would have been obvious to modify the teachings of Pyo2 to additionally include such limitations based on implementing Pyo2’s metal wiring (201), pads (P1 and P2), wiring (206), and via contact (208) (collectively, “interconnections”) in copper using the common and well-known single-or dual-damascene processes and structures disclosed by each of Choi, Yun, Dublin, and Yu.

Pyo2 does not disclose the material used for its wiring (206), but discloses that the “plurality of transistors and the plurality of metal wirings 201 (M1 to Mn) are connected to each

other through pads P1 and P2, and the via contact 208 comprises a metal such as tungsten, aluminum, or copper." Pyo2, 3. The "metal wirings 201 (M1 to Mn) are formed using copper, aluminum, or the like." Pyo2, 4. As of 2007, there were in fact only a few natural choices for POSAs to select to make interconnections, including copper. POSAs would have had reasons to pick copper over the alternatives, such as aluminum or tungsten (*i.e*. lower resistivity, reduced power consumption, resistance to electromigration, and tighter packing density). *See* Part III.A.2. And in implementing Pyo2's interconnections in copper, POSAs would have used the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because such processes had become the natural choice for fabricating copper interconnections (lines, pads, and vias) by the date of the alleged invention of the '366 patent. *See* Part III.B.1.c. POSAs could have readily implemented Pyo2's interconnections in copper by using either the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because applying those processes to create copper interconnections had been well known in both CMOS chip manufacturing generally (*see* Part III.B.1.c) as well as specifically for CMOS image sensors. *See generally* Gambino; Adkisson.

When implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Pyo2's interconnections out of copper, the resulting modified Pyo2 sensor would have copper interconnections (pads, wiring, and vias), a pre-metal dielectric on the first semiconductor substrate, a first via penetrating the pre-metal dielectric, a first interlayer dielectric on the pre-metal dielectric including the first via, a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel, a first metal interconnection with a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height

difference, and a conductive barrier layer on the first metal interconnection, satisfying every limitation of claims 1, 2, 4, 5, 7, and 8, rendering those claims obvious. *See* Part III.B.1.c; Exhibit B-4.

Claim 6: Moreover, when implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Pyo2's interconnections out of copper, the resulting modified Pyo2 sensor would have had a conductive barrier layer with a top surface substantially even with the top surface of the first interlayer dielectric. *See* Part III.B.1.c-d. The modified Pyo2 sensor would, therefore, have satisfied every limitation of claim 6, rendering that claim obvious.

6. Lee (Ex. B-5)

a. Lee in view of Any One of Choi, Yun, Dublin, or Yu Renders All Asserted Claims Obvious

Lee in view of any one of Choi, Yun, Dublin, or Yu renders claims 1, 2, and 4-8 obvious.

Claim 1: Lee does not mention a conductive barrier layer on the first metal interconnection, but as of 2007, there were only a few natural choices for POSAs to select to make interconnections, including copper. *See* Part III.B.1.b. POSAs would have known that it would have been highly desirable to add a conductive barrier layer when implementing Lee's interconnections in copper. *See* Part III.B.1.d.

Lee discloses that "[t]he first metal line M1 comprises a metal layer such as W or Al." Lee at 6. Lee does not address the materials used for the vias or metal lines M2-M5. As of 2007, however, there were only a few natural choices for POSAs to select to make interconnections (metal lines, pads, and vias), including copper. POSAs would have had reasons to pick copper over the alternatives, such as aluminum or tungsten (*i.e.* lower resistivity, reduced power consumption, resistance to electromigration, and tighter packing density). *See* Part

III.B.1.b. And in implementing Lee's interconnections in copper, POSAs would have used the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because such processes had become the natural choice for fabricating copper interconnections (lines, pads, and vias) by the date of the alleged invention of the '366 patent. *See* Part III.B.1.c. POSAs could have readily implemented Lee's interconnections in copper by using either the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because applying those processes to create copper interconnections had been well known in both CMOS chip manufacturing generally (*see* III.B.1.c) as well as specifically for CMOS image sensors. *See generally* Gambino; Adkisson.

When implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Lee's interconnections out of copper, the resulting modified Lee sensor would have a pre-metal dielectric on the first semiconductor substrate, a first via penetrating the pre-metal dielectric, a first interlayer dielectric on the pre-metal dielectric including the first via, a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel, and a conductive barrier layer on the first metal interconnection, satisfying every limitation of claims 1 and 8, rendering those claims obvious. *See* Part III.B.1.c; Exhibit B-5.

Claims 2 and 4-7: Moreover, when implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Lee's interconnections out of copper, the resulting modified Lee sensor would have additionally had:

- A first metal interconnection comprising copper (Cu);

- A first metal interconnection with a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference;
- A second metal interconnection comprising copper (Cu);
- A conductive barrier layer with a top surface substantially even with the top surface of the first interlayer dielectric; and
- A first via and a second via comprising the same material (copper).

See Part III.B.1.c. The modified Lee sensor would, therefore, have satisfied every limitation of claims 2 and 4-7, rendering those claims obvious.

Claim 8: Lee discloses, in reference to prior art image sensors, that "[t]he first to fourth metal lines M1 to M4 are for connecting a power line or a signal line to a unit pixel and a logic circuit, and serve as a shield to prevent light from entering areas other than the photodiode PD." Lee at 2. While Lee discloses its sensor also "comprises a second metal line (M1) to a sixth metal line (M6) and a plurality of insulating film structures (PMD2, IMD1 to IMD4, ILD (Inter-Layer Dielectric)) on the rear surface thereof" (Lee at 4), to the extent that VisionX argues, or it is found, that Lee does not disclose interconnections for an external signal and power lines, POSAs would have had reasons to add these interconnections to M2-M6 layer to make Lee's sensor operational like the prior art image sensors it discloses. Moreover, including interconnections for an external signal line and power line was common and well-known by 2007. *See, e.g.* Guidash, '256 2:33-38 ("The Support wafer includes conductive interconnects and additional analog and digital circuits used by the active pixel sensor. Examples of the additional circuits formed on the Support circuit wafer include, but are not limited to, timing generators, control circuitry such as transfer gate drivers, decoders, output circuits, and power

supplies."); Yanagida2, [0027] (""The reset transistor 25 is connected between the power supply Vdd and the floating diffusion FD. When a reset signal is given to the gate, the potential of the floating diffusion FD is reset to the potential of the power supply Vdd. T hese operations are performed simultaneously for each pixel in a row, since the gates of the transfer transistor 22, address transistor 24, and reset transistor 25 are connected on a row basis."); Imaoka, [0017] (teaching an "external terminal 50" as part of the" second semiconductor substrate 20"), [0049] (teaching a "power supply terminal" and an "input/output terminal.").

7. Koyanagi2 (Ex. B-6)

a. Koyanagi2 in view of Any One of Choi, Yun, Dublin, or Yu and the Knowledge of a POSA Renders All Asserted Claims Obvious

Koyanagi2 in view of any one of Choi, Yun, Dublin, or Yu renders claims 1, 2, and 4-8 obvious.

Claims 1 and 8: As set out in Exhibit B-1, Koyanagi2 discloses each element of claims 1and 8 except for a color filter (claim 1), a conductive barrier layer on the first metal interconnection (claim 1) and a second substrate with metal interconnections for a power line (claim 8).

Modifying the Koyanagi2 image sensor by adding a color filter on the first interlayer dielectric on the unit pixel would have been obvious to a POSA because color image sensors were ubiquitous by 2007. *See, e.g.* Pyo, 4 (disclosing a CMOS sensor with "a color filter array"), 5 (noting "color filter array 107" in Figure 3), Figure 3; Imaoka, [0013] (disclosing a CMOS sensor with an "optical part 13" with a "color filter (not illustrated)," "formed between the micro-lenses 54 and the light-receiving elements"), Figure 1; Guidash '256, 5:17-28 ("Color filters 246, 248, 250 are formed over sensor wafer 202 and are used to filter the bandwidth of incident light received by each photodetector 216"), Figure 2; Yanagida2, [0035] ("On the

protective film 110, a color filter 111 is formed to pass only light in a desired wavelength region. In addition, on the color filter 111, an on-chip lens 112 is formed to focus the incident light onto the photodiode 21.”). Such modification would involve combining prior art elements according to known methods to yield predictable results and simple substitution of known elements.

Modifying the Koyanagi2 image sensor by adding interconnections for a power line associated with the second substrate would have been obvious because POSAs would have understood the desirability of incorporating a power line to make the Koyanagi2 image sensor operational. An obvious place to locate such interconnection for a power line would be in the output layer with the signal interconnections. *See, e.g.* Guidash ’256, 2:33-38 (“The Support wafer includes conductive interconnects and additional analog and digital circuits used by the active pixel sensor. Examples of the additional circuits formed on the Support circuit wafer include, but are not limited to, timing generators, control circuitry such as transfer gate drivers, decoders, output circuits, and power supplies.”); Yanagida2, [0027] (““The reset transistor 25 is connected between the power supply Vdd and the floating diffusion FD. When a reset signal is given to the gate, the potential of the floating diffusion FD is reset to the potential of the power supply Vdd. These operations are performed simultaneously for each pixel in a row, since the gates of the transfer transistor 22, address transistor 24, and reset transistor 25 are connected on a row basis.”). Such modification would involve combining prior art elements according to known methods to yield predictable results and simple substitution of known elements.

Modifying the Koyanagi2 image sensor to use copper for electrode 28, wiring 58A and 58B, embedded wiring 34 and 56A, and other interconnections would have been obvious. Koyanagi2 discloses “a low-resistance metal such as low-resistance polycrystalline silicon or tungsten doped with impurities is used as the conductive material for forming the embedded

wiring 34." [0024]. Koyanagi2 discloses "[t]he n-type impurity layer 22 serving as the source of the MOS transistor is connected to a source electrode 28 composed of, for example, aluminum, and the n-type impurity layer 22 serving as the drain is connected to a drain electrode 29 composed of, for example, aluminum insulated from the source electrode 28 by an insulation film 24B." [0025]. Koyanagi2 discloses "the conductive material for forming the embedded wiring 56A, a low-resistance metal such as low-resistance polycrystalline silicon or tungsten doped with impurities is used." [0029]. Koyanagi2 discloses "aluminum wiring 58A." [0029]-[0030]. Koyanagi2 discloses "aluminum wiring 58B." [0035]-[0036]. Koyanagi2 also discloses "the conductive material for forming the embedded wiring 104, a low-resistance metal such as copper, tungsten, or gold is used" [0038].

POSAs would have had reasons to use copper instead for electrode 28, wiring 58A and 58B, embedded wiring 34 and 56A, and other interconnections due to its lower resistivity, reduced power consumption, resistance to electromigration, and tighter packing density). *See* Part III.B.1.b. And in implementing Koyanagi2's interconnections in copper, POSAs would have used the single- or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because such processes had become the natural choice for fabricating copper interconnections (lines, pads, and vias) by the date of the alleged invention of the '366 patent. *See* Part III.B.1.c. POSAs could have readily implemented Koyanagi2's interconnections in copper by using either the single– or dual-damascene process disclosed by Choi, Yun, Dublin, and Yu because applying those processes to create copper interconnections had been well known in both CMOS chip manufacturing generally (*see* Part III.B.1.c) as well as specifically for CMOS image sensors. *See generally* Gambino; Adkisson.

When implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Koyanagi2's interconnections out of copper, the resulting modified Koyanagi2 sensor would have a pre-metal dielectric on the first semiconductor substrate, a first via penetrating the pre-metal dielectric, a first interlayer dielectric on the pre-metal dielectric including the first via, a first metal interconnection on the first interlayer dielectric and connected to the first via and the unit pixel, and a conductive barrier layer on the first metal interconnection, satisfying every limitation of claims 1 and 8, rendering those claims obvious. *See* Part III.B.1.c; Exhibit B-6.

Claims 2 and 4-7: Moreover, when implementing the common and well-known single- and dual-damascene structures disclosed by Choi, Yun, Dublin, or Yu to make Koyanagi2's interconnections out of copper, the resulting modified Koyanagi2 sensor would have additionally had:

- A first metal interconnection comprising copper (Cu);
- A first metal interconnection with a top surface lower than that of the first interlayer dielectric, such that the first metal interconnection and the first interlayer dielectric have a height difference;
- A second metal interconnection comprising copper (Cu);
- A conductive barrier layer with a top surface substantially even with the top surface of the first interlayer dielectric; and
- A first via and a second via comprising the same material (copper).

See Part III.B.1.c. The modified Koyanagi2 sensor would, therefore, have satisfied every limitation of claims 2 and 4-7, rendering those claims obvious.

8. Pyo & Imaoka Each Anticipate and/or Render Obvious All Asserted Claims (Ex. B-7)

On December 2, 2022, Sony filed a petition for *inter partes* review ("IPR") alleging six grounds of invalidity based on Pyo and Imaoka as primary references. Specifically, the IPR petition sets forth the basis for the invalidity of the Asserted Claims (along with claim 3) as follows:

Ground 1: the Asserted Claims are obvious over Pyo in view of Choi;

Ground 2: claim 3 is obvious over Pyo in view of Choi in further view of Dublin;

Ground 3: the Asserted Claims are anticipated by Imaoka;

Ground 4: claim 3 is obvious over Imaoka in view of Dublin;

Ground 5: the Asserted Claims are obvious over Imaoka in view of Choi; and

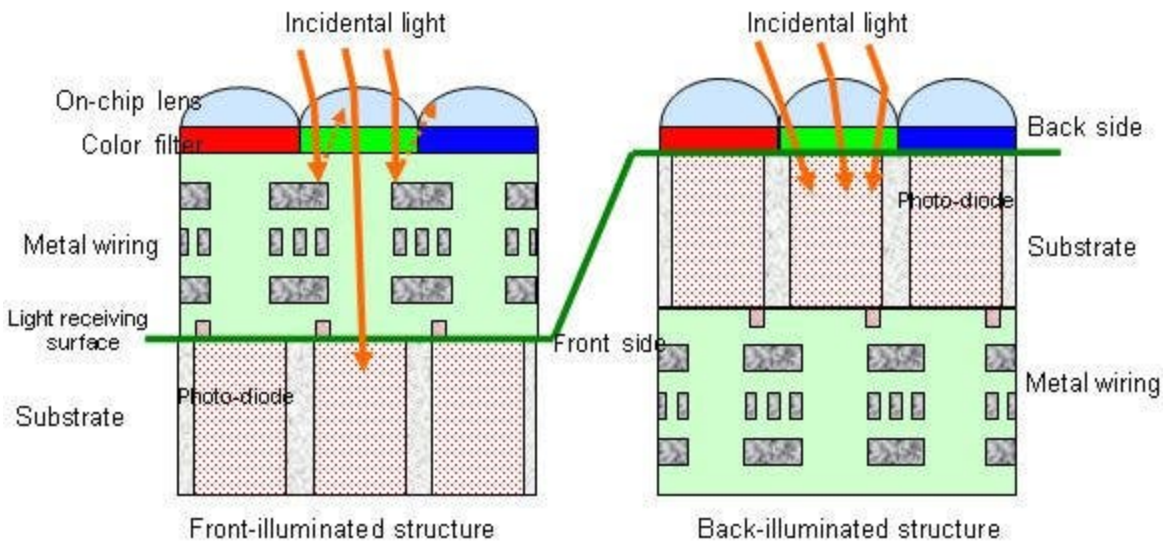
Ground 6: claim 3 is obvious over Imaoka in view of Choi in further view of Dublin.

See Exhibit B-7. Sony incorporates by reference its IPR petition provided in Exhibit B-7. However, per the stipulation included in Sony's IPR petition, Sony will not pursue on any invalidity grounds based on Pyo and/or Imaoka (i.e., the primary references in the IPR) in this district court proceeding should the Patent Trial & Appeal Board institute review.

C. Anticipation and Obviousness of U.S. Patent No. 8,035,143

1. Background Knowledge of a POSA

Backside-illuminated ("BSI") image sensors—including sensors incorporating CMOS technology—had been described at least as early as 2004. Unlike traditional frontside-illuminated ("FSI") sensors, BSI sensors position the sensor circuitry behind a photosensitive layer to minimize the amount of light that is blocked from reaching the photo-diode for detection. Hynecek '948, 1:30-45; Pain, [0004]-[0005]. The distinction between the two types of sensors is illustrated below.



Comparison between frontside and backside illuminated sensors

As the figure illustrates, the metal wiring in FSI sensors is between the lenses and the substrate. Uya, Abstract. This reduces light collection efficiency and sensitivity because the metal layer partially blocks the photodiode. *Id*., 1:25-55. As a result of these effects, only a fraction of the light incident on the on-chip lenses is incident on the photodiode, reducing image quality. *Id*.; Sumi, [0004] ("However, in this CMOS Solid-state image sensor of the front-illuminated type, it is known that efficiency in using light is reduced and sensitivity is lowered, because multi-layered wirings exist on the route of light illuminated, particularly, on the optical path of oblique light in the vicinity of the effective pixel area and the light is scattered by the multi-layered wirings."); Pain, [0007] ("The main problem of imaging with a structure as shown schematically in FIG. 1 is the increased distance between the point 70 where light enters the system and the silicon 30 where light is detected, i.e. converted to photoelectrons. As shown in FIG. 1, light has to travel through many layers of dielectric and interconnect metal layers (metal bus lines) suffering multiple reflections, obscurations, and deflections, before it is actually collected by silicon. For a small sized pixel, the aspect ratio between the vertical distance to the

photodiode width can be as high as 3:1. This is akin to shining a flashlight in a canyon. Due to the increased distance between the color-filter/micro-lens and the silicon surface, the device suffers from poor collection efficiency, low sensitivity, low quantum efficiency (QE), increased cross-talk, and poor angular response."). A solution to this problem was to eliminate intervening metal wiring layers opposite between the lens and substrate, as seen in BSI sensors. Sumi, [0008]. The design of BSI sensors ensure that the photodiodes are not obscured by the circuitry in the metal wiring layer—allowing more light to reach the substrate. This improved light sensitivity and detection efficiency as compared to FSI sensors. Pain, [0017]-[0020].

The backside layers on BSI sensors are fabricated using low-temperature manufacturing processes. Maruyama '395 [0006]. The process begins with a wafer similar to those used in other CMOS manufacturing processes. Guidash '256, 1:66-2:62. As described above, a CMOS sensor wafer is fabricated in the same manner as FSI sensor wafers, but the layout of the metal lines on the front side is modified since light will not be incident on the front side. The metal layers can be placed anywhere in the pixel—improving the pixel's electrical performance. After completion of the standard CMOS wafer processing flow, the wafer is bonded to a carrier wafer or "handle," then turned over. *Id*. The wafer is reversed and the optical components are formed on the rear—allowing light to strike the photodiode. A low temperature process is used to avoid impacting previously deposited components. Maruyama '395, [0006].

All of the limitations in the asserted claims of the '143 patent were well-known in the context of BSI sensors before November 5, 2008—the earliest possible effective filing date of the '143 patent. The asserted claims simply combine these components to serve the same functions the prior art already disclosed.

For example, U.S. Patent No. 7,875,948 ("Hynecek '948") is indisputable prior art and discloses all limitations of claims 1-4 of the '143 patent aside from specifying what material was used for the sensor's insulating layer—i.e., TEOS. But the use of TEOS for an insulating material had known benefits. For example, TEOS is a common low-temperature oxide, and a low-temperature oxide formed on the backside is highly desirable to prevent the disruption of components already formed on the device.

As another example, U.S. Patent Publication No. 20060076590A1 ("Pain") is likewise indisputable prior art, and discloses all limitations of claims 1, 3 and 4. As with Hynecek '948, it would have been obvious to implement Pain's sensor using industry-standard TEOS—thereby yielding a sensor falling within the scope of claim 2 under Plaintiff's interpretation in the infringement contentions.

a. Readout Circuitry

POSAs would have has reason to incorporate readout circuitry in BSI image sensors. Shiraiwa, [0009]. Readout circuitry is used to read optical signals incident upon the photodiodes. In an image sensor, each pixel region in the imaging region comprises a photodiode and at least one transistor (i.e. readout circuitry). *Id*. The readout circuitry reads the signal charge to each unit pixel cell by transferring the photocharge from the respective photodiode. *Id*. It would have been obvious to a POSA that incorporating readout circuitry would ensure image sensors can fulfill their intended function.

b. Use of Metal

While certain references do not expressly disclose the materials used for a sensor's interconnects (i.e., the disclosed wiring layers, vertical vias and electrode pads), POSAs knew that metal interconnects offered multiple benefits. For example, metal's low resistivity made it a commonplace choice when fabricating interconnection layers, pads and connection vias (i.e.,

connections between different layers of a substrate). Patti-IEEE, 1218. Further, metal can be deposited at low temperatures in deep high aspect ratio vias. Quirk, 302. Copper—with particularly low resistivity—was routinely used when fabricating vias to form an electrical connection through the insulation separating the layers. *Id*. While there were theoretically alternatives to metal (e.g., polysilicon or indium tin oxide), they were expensive and required high temperatures unsuitable for BSI fabrication. The use of metal as well as the process for fabrication were known in the art by 2008, and many references disclose the advantages of metal connection vias in CMOS image sensor design. *Id*. It would have been obvious to fabricate BSI sensors using industry-standard metal interconnections.

c. Metal Pad

It would have been obvious to POSAs that a structure formed on the insulating layer, covering the projection part of the connection via, and electrically connected to the metal interconnection layer through the connection via, would meet the claimed "metal pad." For example, both Hynecek '948 and Pain teach a metal pad under Plaintiff's apparent understanding of those claims as reflected in Plaintiff's Infringement Contentions.

Further, it would have been obvious to incorporate a protruding via with a concave metal pad formed on the protrusion. For example, Hynecek '948 teaches a protruding via, which may be modified to comprise a concave metal pad over said protruding via as shown in U.S. Patent No. 7,928,534 to Hsu et al. (hereinafter "Hsu") for an image sensor comprising a concave metal pad over a protruding via.

d. An Insulating Layer Having a Thickness Thinner Than the Height of a Projection of a Connection Via Metal

POSAs also would have had reason to fabricate BSI image sensors such that the insulating layer had a thickness thinner than the height of a projection of a connection via metal.

POSAs would have known that an insulating layer having a thickness less than the height of a projection part would allow the insulating layer to be etched back such that the projection part can be exposed. For example, Hynecek '948 teaches a protruding via comprising a projection part surrounded by an insulating layer which may be modified such that the projection height of the projection part is greater than the thickness of the insulating layer as shown in U.S. Patent Publication No. 20070048973 to Koizumi et al. (hereinafter "Koizumi"). POSAs would have been motivated to modify at least this structure in order to fabricate additional layers between the insulating later as metal as shown in Koizumi. Koizumi, [0056]-[0059].

Alternatively, it would have been obvious to POSAs to use a stacked insulating layer – comprising at least one nitride layer and one oxide layer – to insulate the connection via. *E.g.*, Quirk, 275-276. POSAs would have known that the oxide layer would isolate the structure from the semiconductor substrate and the nitride layer enhanced protection against the diffusion of impurities and moisture. *Id.* Further, it would have been obvious to POSAs that a projection part of a connection via will extend through the entire modified stack to a metal pad. As such, the height of the projection part is at least the sum of the thicknesses of the stack of at least one oxide layer and one nitride layer. According to the'143 Patent, only the oxide layer within such a stack would be the claimed insulating layer. If the height of the projection part is the sum of the thicknesses of the insulating layer (i.e. the oxide layer) and the nitride layer, then it would have been obvious that the insulating layer by itself has a thickness thinner than the height of the projection part because a subpart in an addition of positive values is necessarily smaller than the sum.

e. TEOS Insulating Layer

Claim 2's requirement that "the insulating layer comprises a TEOS [tetraethyl orthosilicate] layer" was a previously recognized industry standard for CMOS image sensors. It

would have been obvious when manufacturing BSI image sensors to incorporate a low-temperature oxide layer such as TEOS (which was well known by 2008) to insulate the substrate on a CMOS sensor. Quirk, 271 ("A common APCVD application is to deposit oxide by reacting TEOS, which is tetraethylorthosilicate ($Si(C_2H_5O)_4$) or tetraethoxysilane, with ozone (O_3) ... the process can be done at low temperatures"). POSAs would have been motivated to. For example, POSAs would have been motivated to improve the insulation film in Hynecek '948 with a TEOS layer because a low-temperature oxide formed on the backside is highly desirable to prevent the disruption of components already formed on the device and TEOS is common low-temperature oxide, as taught in Quirk or Yanagida-2. Quirk, 271-272 ("The deposited oxide film has improved profiles over steps, is conformal, and has excellent electrical characteristics as a dielectric…This reflow adds a process step and reduces the thermal budget.[29] Doping uniformity is also a concern, as this can lead to problems for nonuniform removal rates during chemical mechanical planarization. The primary advantage of APCVD TEOS- O_3 is the improved step coverage for high-aspect ratio gaps for applications such as shallow trench isolation (see Figure 11.13). Another advantage to APCVD TEOS- O_3 is that it is just a basic thermal CVD process to deposit oxide, which could avoid wafer surface damage and wafer corner damage at steps.") Further, POSAs would know that TEOS is commonly used an interlayer dielectric, and, as such, could be combined with the image sensor in Hynecek '948. *Id*. The resulting modified Hynecek '948 sensor would have been structurally and functionally unchanged. The modified Hynecek '948 sensor would, therefore, have satisfied every limitation of claims 1-4, rendering those claims obvious.

f. Forming a Protective Layer on the Insulating Layer

Claim 4 recites a protective layer formed over the insulating layer and a micro-lens formed over the protective layer. It would have been obvious when manufacturing image

sensors, including Hynecek ’948’s and Pain’s sensors, to incorporate a protective layer such as an antireflective film between the insulating layer and the micro-lens (which Hynecek ‘948 and Pain already disclose) to reduce the reflection of incident light and improves photodiode light collection efficiency.

In particular, at least Hynecek ’948 or Pain in combination with a POSA’s knowledge as well as Yanagida-2 or U.S. Patent Publication No. 20070155044A1 to Shim (“Shim”) discloses all limitations of claim 4 and renders those claim limitations unpatentable under § 103. For example, as illustrated by Yanagida-2, the use of nitride protection in combination with an insulation layer, where the nitride protective layer is an antireflective film, was known in the art. Yanagida-2, [0034]. POSAs would have recognized that a BSI image sensor could be improved by incorporating a protective layer to protect the photodiode from corrosion. Quirk, 295. Passivation enhances the performance of the BSI image sensor by avoiding deterioration caused by moisture or undesirable mobile ions. *Id*. Passivating the image sensor with a protective layer on the insulating film will better protect the sensor and prevent it from losing sensitivity. *Id*. POSAs would understand that Yanagida-2, also directed to a BSI sensor, teaches a protective layer on the insulation layer to passivate the sensor and guard against degradation. POSAs would have known to apply a similar protective layer to other BSI sensors to achieve the same result of passivating the image sensor.

g. Forming a Micro-lens on the Protective Layer

The formation of the micro-lens on the protective layer would have been obvious to a POSA. For example, Shim discloses a micro-lens formed on a protective layer. Shim, [0053]-[0058]. POSAs would know that a micro-lens is the outermost layer in an image sensor and is used to increase light collection efficiency in CMOS sensors. Maruyama ’395, [0149]; Yanagida-2, [0035]. Using a micro-lens in a BSI sensor enables collecting and focusing light that may have

otherwise been incident upon non-sensitive areas of the sensor. *Id*. Forming a micro-lens on the protective layer would have the known result of increasing the amount of light detected by the photodiodes while protecting and passivating the photodiodes. *Id*. The modification would have been routine and would have provided expected results.

2. Hynecek '948 (Ex. C-1)

a. Hynecek in view of POSAs' Knowledge Renders Claims 1, 3, and 4 Obvious

Hynecek in view of POSAs' knowledge renders claims 1, 3, and 4 obvious. As set out in Exhibit C-1, Hynecek '948 discloses each element of claims 1, 3, and 4.

To the extent Plaintiff argues Hynecek '948 does not disclose a metal pad formed on the insulating layer such that the metal pad covers the projection part (claim 1), it would have been obvious to a POSA that the transparent conductive layer 126 in Hynecek '948 is a pad under Plaintiff's apparent understanding of those claims as reflected in Plaintiff's Infringement Contentions.

b. Hynecek '948 in view of any of Yanagida-2 or Quirk and POSAs' Knowledge Renders All Asserted Claims Obvious

Hynecek '948 in view of any of Yanagida-2 or Quirk and POSAs' knowledge renders claims 1-4 obvious.

Claims 1, 3 and 4: Hynecek '948 in view of POSAs' knowledge renders claims 1, 3, and 4 obvious for the reasons discussed above in §III.C.2.a.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer. POSAs would have been motivated to modify Hynecek '948's image sensor in view of Yanagida-2's or Quirk's teachings. For example, Yanagida-2 is also directed to backside-illuminated image sensors, and teaches an insulation element formed on the light incident side of the substrate. Yanagida-2, [0007], [0034]; *see also* Quirk, 271-272. POSAs would have been

motivated to improve the insulation film in Hynecek '948 with a TEOS layer because a low-temperature oxide formed on the backside is highly desirable to prevent the disruption of components already formed on the device and TEOS was a well-known low-temperature oxide, as taught in Yanagida-2. Quirk, 271-272. Further, POSAs would know that TEOS is commonly used an interlayer dielectric, and, as such, could be combined with the image sensor in Hynecek '948. *Id*. The resulting modified Hynecek '948 sensor would have been structurally and functionally unchanged. The modified Hynecek '948 sensor would, therefore, have satisfied every limitation of claims 1-4, rendering those claims obvious.

3. Holm (Ex. C-2)

a. Holm in view of Guidash '939 Knowledge Renders Claims 1 and 3 Obvious

Holm in view of POSAs' knowledge renders claims 1 and 3 obvious. As set out in Exhibit C-2, Holm discloses each element of claims 1 and 3 except for readout circuitry formed on a first surface of a semiconductor substrate (claim 1).

Modifying the Holm image sensor by adding readout circuitry would have been obvious to a POSA by 2004. As previously discussed in §III.C.1.a, a POSA would have known to include readout circuitry to process signals detected by the photodiodes.

Specifically, it would have been obvious for a POSA to modify the active pixels of Holm to provide a readout circuitry in view of U.S. Patent Publication No. 20080083939 to Guidash (hereinafter "Guidash '939"). Guidash '939 recognizes a problem with pixel interconnects directly connecting highly doped ohmic contact region similar to Holm leading to increased dark current. Guidash '939 at [0005] ("Although this approach separates the processing of the photodetector and circuits, it degrades photodetector performance due to the direct contact or connection with the photodetector. Specific examples of such performance degradation include,

but are not limited to, increased dark current due to damage from the contact etch process, increased metallic contamination in the photodetector leading to point defects, and high dark current due to being connected to a highly doped ohmic contact region."). Guidash '939 describes an improved vertically-integrated active pixel sensor that provides a transfer gate 218 and a charge-to-voltage conversion mechanism 220 in the sensor wafer that alleviates the degradation problems. Id. Figs. 3, 4, [0014], ("The connection between the sensor wafer and the support circuit wafer can be achieved through the charge-to-voltage conversion mechanism on the sensor wafer, a voltage domain contact, and a node on the support circuit wafer, thereby avoiding performance degradation of the photodetectors."). The transfer gate is a readout circuitry. Id. [0009], ("[O]ne example of the readout circuitry is a transfer gate"). POSAs would have modified Holm to implement the improved pixel design of Guidash '939 to avoid performance degradations from making direct contact with a photodetector.

Such modification would involve combining prior art elements according to known methods to yield predictable results and simple substitution of known elements.

b. Holm in view of any of Yanagida-2, Quirk, Shim, Sumi or Maruyama '395 and POSAs' Knowledge Renders All Asserted Claims Obvious

Holm in view of any of Yanagida-2, Quirk, Shim, Sumi or Maruyama '395 and POSAs' knowledge renders claims 1-4 obvious.

Claims 1 and 3: Modifying Holm in view of Guidash '939 to include readout circuitry formed on the first surface of the semiconductor substrate would have been obvious for the reasons discussed above in §III.C.2.b.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer (as taught in Quirk or Yanagida-2, for example) for the same reasons discussed above in § III.C.1.e.

Claim 4: Further, it would have been obvious to include a micro-lens formed on a protective layer by 2004. As discussed above in §III.C.1.g, POSAs would have known that a micro-lens advantageously enhances the collection of light incident upon the image sensor. Shim, [0053]-[0058]; Maruyama '395, [0149]; Yanagida-2, [0035]. POSAs would have known to form the micro-lens on a protective layer to protect the photodiode from corrosion. Sumi [0017]. Passivation enhances the performance of the BSI image sensor by avoiding deterioration caused by moisture or undesirable mobile ions. Passivating the image sensor with a protective layer on the insulating film and forming the micro-lens on the protective layer will better protect the sensor and prevent it from losing sensitivity. Forming the micro-lens on the protective layer will allow focusing the light onto the photodiode while passivating the sensors as described above.

The modifications of the Holm sensor to include a micro-lens would have been routine, as taught in any Yanagida-2, Quirk, Shim, Sumi or Maruyama '395, and the results (i.e., a sensor with enhanced insulative, protective, and light-collecting functionalities) would have been predictable.

4. Pain (Ex. C-3)

a. Pain Renders Claims 1, 3, and 4 Obvious

Pain renders claims 1, 3, and 4 obvious. As set out in Exhibit C-3, Pain discloses each element of claims 1, 3, and 4, except an insulating layer with a thickness thinner than a projection height of the projection part. To the extent Plaintiff argues that a passivation layer is not an insulation layer, it would have been obvious to POSAs the passivation layer in Pain would be insulating. For example, Hynecek '948 teaches a backside passivation layer 125 comprising a stack structure of a first insulation layer and a second insulation layer having different refractive indexes. Hynecek '948, 10:6-8. Similarly, Quirk discloses materials (e.g. silicon nitride) may be

used to both insulate and passivate. Quirk, 271-272. POSAs would have known that a material used to electrically isolate may be an insulating layer. *Id.* The same material may be used to passivate as an antireflective film and to protect against environmental corrosion. *Id*.

Modifying the sensor in Pain to include an insulating layer having a thickness less than the projection height of the projection part would have been obvious to a POSA at least for the reasons discussed above in § III.C.1.d.

b. Pain in view of any of Yanagida-2 or Quirk Renders All Asserted Claims Obvious

Pain in view of any of Yanagida-2 or Quirk of renders claims 1-4 obvious.

Claims 1, 3 and 4: Pain renders claims 1, 3, and 4 obvious for the reasons discussed above in §III.C.4.a.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer (as taught in Quirk or Yanagida-2, for example) in Pain's image sensor for the reasons discussed above in §III.C.1.e. Such modification would involve combining prior art elements according to known methods to yield predictable results and simple substitution of known elements.

5. Iwabuchi '007 (Ex. C-4)

a. Iwabuchi '007 in view of POSAs' Knowledge Renders Claims 1, 3, and 4 Obvious

Iwabuchi '007 in view of POSAs' knowledge renders claims 1, 3, and 4 obvious under Plaintiff's apparent understanding of those claims (and in particular Plaintiff's apparent understanding of "pad") as reflected in Plaintiff's Infringement Contentions. As set out in Exhibit C-4, under that understanding Iwabuchi '007 discloses each element of claims 1 and 3 except for interconnection layer, connection via, and pad comprising metal, and an insulating

layer having a thickness thinner than a projection height of the projection part of the connection via metal (claim 1).

Modifying the Iwabuchi ’007 image sensor such that the interconnection layer, connection via, and pad are metal would have been obvious to a POSA by 2006. To the extent that any of Iwabuchi ’007’s electrical connections could have been implemented with a non-metal alternative, the well-known use metal at minimum would have been an obvious choice for implementing the electrical connections in Iwabuchi ’007’s sensor. For example, Pain discloses a BSI sensor that uses metal for each of the metal wiring layers, vertical connection vias, and the pads connected to the wiring layers through the vertical connection vias. *See e.g.*, Pain, [0036] (disclosing “metal layers 150 for interconnection of circuits and photo-detectors”), [0048] (disclosing “metal pads 525 resid[ing] on the same side of light entrance”), [0077] (disclosing “Metal pads 700 [] connected with ILD 610 [metal wiring] by means of interconnect metal 710 [vertical connection via].”).

Thus, it would have been obvious to a POSA to use metal for each of the electrical connections discussed above at least because doing so is nothing more than the use of a known material (metal) for its intended function (electrical conductance) to yield the predictable result of providing the electrical connections in Iwabuchi ’007’s sensor with the advantageous conductivity properties of metal. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-421 (2007). Additionally, POSAs would have had numerous reasons to choose metal for the electrical conductors of Iwabuchi ’007’s sensors. The high conductivity, durability and relatively low cost of using metal to implement electrical connections in semiconductor devices, including image sensors, would have made using metal conductors an obvious and desirable choice for implementing all of the disclosed electrical connections of Iwabuchi ’007’s sensor. For one,

POSAs implementing Iwabuchi ’007’s sensor would have had reason to use a metal to fill vias. A low resistivity conductor within the described connection via in Iwabuchi ’007’s sensor would electrically and thermally connect the layers. Incorporating metal conductors in image sensors was standard practice by 2006; aside from being less expensive than alternatives, metal provided higher conductivity and better durability.

Furthermore, processes for metal deposition were well-established and understood, for example, POSAs would have known that a metal could be easily deposited in BSI sensors using chemical vapor deposition (“CVD”) suitable for low temperature fabrication and for metallizing deep high aspect ratio structures such as vertical vias. POSAs therefore would have had multiple reasons to incorporate use metal as the conductive material for the interconnection layer, connection via and pad 14 during the ordinary course of implementing Iwabuchi ’007’s sensor.

Similarly, POSAs would have had reason to fabricate Iwabuchi ’007’s pad using metal. Since the pad is electrically connected to the connection via, it would have been obvious to a POSA to use a conductive material to electrically couple the two elements. As with the connection via, metal would have been an obvious material to use for the pad given its high conductivity and low price.

Such modifications of the Iwabuchi ’007 sensor would have been routine and would have provided expected results, including improved electrical conductivity.

Further, modifying the Iwabuchi ’007 image sensor such that the insulating layer has a thickness thinner than the projection height of the projection part of the connection via metal would have been obvious to a POSA by 2006 at least for the reasons discussed above in § III.C.1.d.

Iwabuchi ’007 also discloses that, although not shown, the various image sensors disclosed comprise a color filter and an on-chip microlens “formed on the back surface side of the substrate through an insulating film.” Iwabuchi ’007 [0012], [0016], [0105].

b. Iwabuchi ’007 in view of any of Yanagida-2, Quirk, Shim, Sumi, or Maruyama ’395 and POSAs’ Knowledge Renders All Asserted Claims Obvious

Iwabuchi ’007 in view of any of Yanagida-2, Quirk, Shim, Sumi, or Maruyama ’395 and POSAs’ knowledge renders claims 1-4 obvious.

Claims 1, 3 and 4: It would have been obvious to modify the image sensor in Iwabuchi ’007 to use metal for the interconnection layer, connection via, and pad as well as to include an insulating layer having a thickness thinner than a projection height of the projection part of the connection via metal for the reasons discussed above in §III.C.5.a.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer (as taught in Quirk or Yanagiada-2, for example) for the same reasons discussed above in §III.C.1.e.

Claim 4: As discussed previously, Iwabuchi ’007 discloses that, although not shown, the various image sensors disclosed comprise a color filter and an on-chip microlens “formed on the back surface side of the substrate through an insulating film.” Iwabuchi ’007, [0016]. However, to the extent Plaintiff argues Iwabuchi ’007 does not disclose a micro-lens, it would have been obvious to include a micro-lens formed on a protective layer (for example, as disclosed in Shim, Sumi, or Maruyama ’395) for the reasons discussed above in § III.C.1.g.

6. Iwabuchi ’762 (Ex. C-5)

a. Iwabuchi ’762 in view of POSAs’ knowledge renders claims 1, 3, and 4 obvious.

Iwabuchi ’762 in view of POSAs’ knowledge renders claims 1, 3, and 4 obvious under Plaintiff’s apparent understanding of those claims (and in particular Plaintiff’s apparent understanding of “pad”) as reflected in Plaintiff’s Infringement Contentions. As set out in Exhibit C-5, under that understanding Iwabuchi ’762 discloses each element of claims 1 and 3 except for interconnection layer, connection via, and pad comprising metal, and an insulating layer having a thickness thinner than a projection height of the projection part of the connection via metal (claim 1).

It would have been obvious to modify the image sensor in Iwabuchi to use metal for the interconnection layer, connection via, and pad as well as to include an insulating layer having a thickness thinner than a projection height of the projection part of the connection via metal for the reasons discussed above in §III.C.1.b and §III.C.1.d.

Further, Iwabuchi ’762 discloses “an on-chip microlens 73 corresponding to each pixel is further formed on the color filter 72,” although not illustrated in Fig. 48. Iwabuchi ’762 [0031].

b. Iwabuchi ’762 in view of any of Yanagida-2 or Quirk and Guidash ’939 knowledge renders claims 1-4 obvious.

Iwabuchi ’762 in view of any of Yanagida-2 or Quirk and POSAs’ knowledge renders claims 1-4 obvious.

Claims 1, 3 and 4: It would have been obvious to modify the image sensor in Iwabuchi ’762 to use metal for the interconnection layer, connection via, and pad as well as to include an insulating layer having a thickness thinner than a projection height of the projection part of the connection via metal for the reasons discussed above in §III.C.6.a.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer (as taught in Quirk or Yanagiada-2, for example) for the same reasons discussed above in §III.C.1.e.

Claim 4: As discussed previously, Iwabuchi '762 discloses an on-chip microlens, although not shown in Fig. 48. Iwabuchi '762, [0031]. However, to the extent Plaintiff argues Iwabuchi '762 does not disclose a micro-lens in the embodiment in Fig. 48, it would have been obvious to include a micro-lens formed on a protective layer (for example, as disclosed in Shim, Sumi, or Maruyama '395) for the reasons discussed above in §III.C.3.b.

7. Patti-IEEE (Ex. C-6)

a. Patti-IEEE in view of POSAs' knowledge renders claims 1, 3, and 4 obvious.

Patti-IEEE in view of POSAs' knowledge renders claims 1, 3, and 4 obvious under Plaintiff's apparent understanding of those claims as reflected in Plaintiff's Infringement Contentions. As set out in Exhibit C-6, under that understanding Patti-IEEE discloses each element of claims 1, 3 and 4 except a protective layer formed over the insulating layer, and a micro-lens formed on the protective layer in a region corresponding to the photodiode area (claim 4).

Modifying the sensor in Patti-IEEE to include at least a protective layer formed over the insulating layer, and a micro-lens formed on the protective layer in a region corresponding to the photodiode area would have been obvious to a POSA for the reasons discussed above in §§III.C.1.f-g.

b. Patti-IEEE in view of any of Yanagida-2, Quirk, Shim, Sumi, or Maruyama '395 and POSAs' knowledge renders claims 1-4 obvious.

Patti-IEEE in view of any of Yanagida-2, Quirk, Shim, Sumi, or Maruyama '395 and POSAs' knowledge renders claims 1-4 obvious.

Claims 1, 3 and 4: The sensor in Patti-IEEE renders claims 1, 3, and 4 obvious for the reasons discussed above in §III.C.7.a.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer (as taught in Quirk or Yanagida-2, for example) for the same reasons discussed above in §III.C.1.e.

Claim 4: To the extent Plaintiff argues Patti-IEEE does not disclose a protective layer formed over the insulating layer, and a micro-lens formed on the protective layer in a region corresponding to the photodiode area, it would have been obvious to include a protective layer and micro-lens formed on the protective layer by 2006 for the reasons discussed above in §III.C.1.f-g. Teachings such as Pain and Guidash '256 further confirm the desirability of incorporating a micro-lens to provide high sensitivity and good angular response (e.g., as taught in Pain at [0008]) as well as the practicality of including such a micro-lens in a vertically stacked sensor (with transistors in a bottom wafer) (e.g., as illustrated in Guidash '256 at Figs. 9, 11). Such incorporation would have been routine, as it was known that metal pads such as those in Patti-IEEE's sensor can serve as backside alignment marks to permit positioning of micro-lens arrays. *See* Pain at [0086].

8. *Tezzaron* sensor (Ex. C-7)

a. The *Tezzaron* sensor in view of POSAs' knowledge renders claims 1, 3, and 4 obvious.

The *Tezzaron* sensor in view of POSAs' knowledge renders claims 1, 3, and 4 obvious under Plaintiff's apparent understanding of those claims (and in particular Plaintiff's apparent understanding of "pad") as reflected in Plaintiff's Infringement Contentions. As set out in Exhibit C-7, under that understanding the *Tezzaron* sensor discloses each element of claims 1, 3, and 4 except a protective layer formed over the insulating layer, and a micro-lens formed on the protective layer in a region corresponding to the photodiode area (claim 4).

Modifying the *Tezzaron* sensor to include at least a protective layer formed over the insulating layer, and a micro-lens formed on the protective layer in a region corresponding to the photodiode area would have been obvious to a POSA for the reasons discussed above in §§III.C.1.f-g.

b. The *Tezzaron* sensor in view of any of Yanagida-2, Quirk, Shim, Sumi, or Maruyama '395 and POSAs' knowledge renders claims 1-4 obvious.

The *Tezzaron* sensor in view of any of Yanagida-2, Quirk, Shim, Sumi, or Maruyama '395 and POSAs' knowledge renders claims 1-4 obvious.

Claims 1, 3 and 4: The Tezzaron sensors renders obvious claims 1, 3, and 4 for the reasons discussed above in §III.C.8.a.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer (as taught in Quirk or Yanagida-2, for example) for the same reasons discussed above in §III.C.1.e.

Claim 4: To the extent Plaintiff argues the *Tezzaron* sensor does not disclose a protective layer formed over the insulating layer, and a micro-lens formed on the protective layer in a

region corresponding to the photodiode area, it would have been obvious to include a protective layer and micro-lens formed on the protective layer by 2004 for the reasons discussed above in §III.C.1.f-g.

9. Lee '891 (Ex. C-8)

a. Lee '891 in view of POSAs' Knowledge Renders Claims 1, 3, and 4 Obvious

Lee '891 in view of POSAs' knowledge renders claims 1, 3, and 4 obvious under Plaintiff's apparent understanding of those claims (and in particular Plaintiff's apparent understanding of "pad") as reflected in Plaintiff's Infringement Contentions. As set out in Exhibit C-8, under that understanding Lee '891 discloses each element of Claims 1, 3, and 4 except an insulating layer has a thickness thinner than a projection height of the projection part (claim 1).

To the extent Plaintiff argues that a passivation layer is not an insulation layer, it would have been obvious to POSAs that the passivation layer of Lee '891 is insulating for the same reasons discussed above in §III.C.4.a. For example, Hynecek '948 teaches a backside passivation layer 125 comprising a stack structure of a first insulation layer and a second insulation layer having different refractive indexes. Hynecek '948, 10:6-8. Similarly, Quirk discloses materials (e.g. silicon nitride) that may be used to insulate and passivate. Quirk, 271-272.

Modifying the Lee '891 image sensor such that the insulating layer has a thickness thinner than the projection height of the projection part would have been obvious to a POSA by 2007. To the extent that Lee '891's sensor could be modified to include a stack of insulation films having at least one oxide layer and one nitride layer, such modifications of the Lee sensor would have been routine and would have provided expected results as discussed above in §III.C.1.d.

b. Lee '891 in view of any of Yanagida-2 or Quirk and POSAs' Knowledge Renders All Asserted Claims Obvious

Lee '891 in view of any of Yanagida-2 or Quirk and POSAs' knowledge renders claims 1-4 obvious.

Claims 1, 3, and 4: It would have been obvious to modify the image sensor in Lee '891 to include an insulating layer having a thickness thinner than a projection height of the projection part for the same reasons discussed above in §III.C.9.a.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer for the same reasons discussed above in §III.C.1.e.

10. Yanagida-1 (Ex. C-9)

a. Yanagida-1 in view of POSAs' Knowledge Renders Claims 1, 3, and 4 Obvious

Yanagida-1 in view of POSAs' knowledge renders Claims 1, 3, and 4 obvious. As set out in Exhibit C-9, under that understanding Yanagida-1 discloses each element of claims 1, 3, and 4, except using metal for the interconnection layer and pad.

It would have been obvious to modify the image sensor in Yanagida-1 to use metal for the interconnection layer and pad for the reasons discussed above in §III.C.1.b.

b. Yanagida-1 in view of any of Yanagida-2 or Quirk and POSAs' Knowledge Renders All Asserted Claims Obvious

Yanagida-1 in view of any of Yanagida-2 or Quirk and POSAs' knowledge renders claims 1-4 obvious.

Claims 1, 3, and 4: It would have been obvious to implement the image sensor in Yanagida-1 using metal for the interconnection layer and pad for the reasons discussed above in §III.C.1.b.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer for the same reasons discussed above in §III.C.1.e.

11. Shiraiwa (Ex. C-10)

a. Shiraiwa in view of POSAs' Knowledge Renders Claims 1, 3, and 4 Obvious

Shiraiwa in view of POSAs' knowledge renders Claims 1, 3, and 4 obvious. As set out in Exhibit C-10, Shiraiwa discloses each element of Claims 1, 3, and 4 except for a connection via metal extending from the first surface to a second surface of the semiconductor substrate, the connection via metal having a projection part projecting from the second surface and a metal pad formed on the insulating layer such that the metal pad covers the projection part (claim 1).

Modifying the Shiraiwa image sensor to include a connection via metal having a projection part and metal pad formed on an insulating layer such that the metal pad covers the projection part would have been obvious to a POSA by 2006.

Specifically, to the extent Plaintiff argues Shiraiwa does not disclose a connection via metal extending from the first surface to a second surface of the semiconductor substrate, it would have been obvious to a POSA in 2006 to include at least a connection via metal to electrically connect the on-chip lens to the interconnection layer. Sumi, [0016]; Pain, [0077]; Yanagida-1 [0036]-[0039]. It would also have been obvious to a POSA in 2006 to modify the connection via metal to have a projection part projecting from the second surface to improve the structure and function of the device. *Id*.

Such modifications of the Shiraiwa sensor would have been routine and would have provided expected results.

Further, it would have been obvious to a POSA to modify the Shiraiwa sensor to include a metal pad for the same reasons discussed above in §III.C.1.c.

To the extent Plaintiff argues that a passivation layer is not an insulation layer, it would have been obvious to POSAs that the passivation layer of Shiraiwa is insulating for the same reasons discussed above in §III.C.4.a. For example, Hynecek '948 teaches a backside passivation layer 125 comprising a stack structure of a first insulation layer and a second insulation layer having different refractive indexes. Hynecek '948, 10:6-8. Similarly, Quirk discloses materials (e.g. silicon nitride) that may be used to insulate and passivate. Quirk, 271-272.

b. Shiraiwa in view of any of Yanagida-2 or Quirk and POSAs' Knowledge Renders All Asserted Claims Obvious

Shiraiwa in view of any of Yanagida-2 or Quirk and POSAs' knowledge renders claims 1-4 obvious.

Claims 1, 3, and 4: It would have been obvious to modify the image sensor in Shiraiwa to use metal for the interconnection layer, connection via, and pad for the reasons discussed above in §III.C.11.a.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer for the same reasons discussed above in §III.C.1.e.

12. Sumi (Ex. C-11)

a. Sumi in view of POSAs' Knowledge Renders Claims 1 and 3 Obvious

Sumi in view of POSAs' knowledge renders claims 1 and 3 obvious. As set out in Exhibit C-11, under that understanding Sumi discloses each element of claims 1 and 3 except for expressly teaching that the interconnection layer, connection via, and pad comprise metal (claim 1).

Fabricating the Sumi image sensor such that the interconnection layer, connection via, and pad are metal would have been obvious to a POSA by 2006. To the extent that any of Sumi's electrical connections could have been implemented with a non-metal alternative, the

well-known use metal would have been an obvious choice for implementing the electrical connections in Sumi's sensor. Such modifications of the Sumi sensor would have been routine and would have provided expected results.

b. Sumi in view of any of Yanagida-2 or Quirk and POSAs' Knowledge Renders All Asserted Claims Obvious

Sumi in view of any of Yanagida-2 or Quirk and POSAs' knowledge renders claims 1-4 obvious.

Claims 1 and 3: It would have been obvious to fabricate the image sensor in Sumi to use metal for the interconnection layer, connection via, and pad for the reasons discussed above in §III.C.9.a.

Claim 2: It would have been obvious to include an insulating layer comprising a TEOS layer for the same reasons discussed above in §III.C.1.e.

Claim 4: Further, it would have been obvious to include a protective layer formed on the insulating layer by 2006 for the reasons discussed above in §III.C.1.f. As set out in Exhibit C-11, Sumi discloses a micro-lens.

IV. INVALIDITY UNDER 35 U.S.C. § 112 – LOCAL PATENT RULE 3-3(D)

Sony lists below the grounds upon which the Asserted Claims of the Asserted Patents are invalid based on indefiniteness under 35 U.S.C. § 112, ¶ 2, lack of written description under 35 U.S.C. § 112, ¶ 1, and/or lack of enablement under 35 U.S.C. § 112, ¶ 1. Sony's contentions that the following claims are invalid under 35. U.S.C. § 112 are made in the alternative, and do not constitute, and should not be interpreted as, admissions regarding the construction or scope of the Asserted Claims, or that any of the Asserted Claims are not anticipated or rendered obvious by any prior art.

A. Invalidity for Indefiniteness Under 35 U.S.C. § 112, ¶ 2

The second paragraph of 35 U.S.C. § 112 requires that a patent claim "particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention." A patent is indefinite "if its claims, read in light of the patent's specification and prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014).

Based on VisionX's Infringement Contentions, Sony identifies below the grounds upon which they presently contend that the Asserted Claims are invalid for indefiniteness under 35 U.S.C. § 112, ¶ 2. With respect to each of the below-mentioned claim limitations, the relevant Asserted Patent does not particularly point out and distinctly claim the subject matter that the inventor regards as the invention. Where Sony identifies a claim term in an independent claim, Sony further contends that the dependent claims depending therefrom are invalid based on the presence of the same term in the asserted dependent claim.

1. '808 Patent

Claim 5 requires "the ion implantation isolation layer comprises a P0 layer." The term "P0" is not defined in the claims, the specification, or the prosecution history. The '808 patent refers to "P0" doping but never explains what that means. The term has no meaning in the art. This fails to define the metes and bounds of claim 5 or give the public notice of the limits of the alleged invention as required by *General Electric*. To the extent that "P0" refers to the degree of doping, and not just p-type doping, this fails the statutory requirements under § 112.

B. Invalidity for Lack of Enablement Under 35 U.S.C. § 112, ¶ 1

35 U.S.C. § 112, paragraph 1, includes an enablement requirement. *See* 35 U.S.C. § 112, ¶ 1 ("The specification shall contain a written description . . . of the manner and process of making and using [the invention] in such full, clear, concise and exact terms as to enable any

person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same.”).

To satisfy the enablement requirement of 35 U.S.C § 112, ¶ 1, the disclosure “must teach those skilled in the art how to make and use the full scope of the claimed invention without ‘undue experimentation.’” *Genentech, Inc. v. Novo Nordisk, A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (citations omitted). Moreover, “[i]t is the specification, not the knowledge of one skilled in the art, that must supply the novel aspects of [the] invention in order to constitute adequate enablement.” *Genentech*, 108 F.3d at1366. “The full scope of the claimed invention must be enabled.” *Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 999-1000 (Fed. Cir. 2008) (“Because the asserted claims are broad enough to cover both movies and video games, the patents must enable both embodiments.”). The Federal Circuit has enumerated several factors to consider in determining whether a disclosure would require “undue experimentation”: (1) the quantity of experimentation necessary; (2) the amount of direction or guidance presented; (3) the presence or absence of working examples; (4) the nature of the invention; (5) the state of the prior art; (6) the relative skill of those in the art; (7) the predictability or unpredictability of the art; and (8) the breadth of the claims. *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988).

Sony lists below the grounds upon which it presently contends that the Asserted Claims are invalid under 35 U.S.C. § 112, ¶ 1 for failure to provide an enabling disclosure.

1. ’366 Patent

Claims 1, 2, and 4-8 of the ’366 patent are invalid under 35 U.S.C. § 112, first paragraph, because the specification does not enable one of ordinary skill in the art to make and use the full scope of the claimed invention without undue experimentation. For example, the claims require a first via penetrating the pre-metal dielectric and the first semiconductor substrate, the first via being connected to the second via. The specification, however, does not enable one of ordinary

skill in the art to fabricate a via that penetrates the pre-metal dielectric and the first semiconductor substrate to connect directly to another via and the claims are not limited to indirect connections of the first via and the second via through an intermediary interconnection, such as a pad.

C. Invalidity for Lack of Written Description Under 35 U.S.C. § 112, ¶ 1

The first paragraph of 35 U.S.C. § 112 also requires a patent specification to contain "a written description of the invention." The written description "must do more than merely disclose that which would render the claimed invention obvious." *ICU Med., Inc. v. Alaris Med. Sys., Inc.*, 558 F.3d 1368, 1377 (Fed. Cir. 2009). To satisfy the written description requirement, the description must "clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Ariad Pharmaceuticals, Inc. v. Eli Lilly and Co.,* 598 F.3d 1336, 1351 (Fed. Cir. 2010) (internal citation omitted). In other words, the test for sufficiency is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date. *Id.*

The test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed. "Whether the written description requirement is satisfied is a fact-based inquiry that will depend on the nature of the claimed invention, and the knowledge of one skilled in the art at the time an invention is made and a patent application is filed." *Carnegie Mellon Univ. v. Hoffmann La Roche Inc.*, 541 F.3d 1115, 1122 (Fed. Cir. 2008).

Actual "possession" or reduction to practice outside of the specification is not enough. Rather, as stated above, it is the specification itself that must demonstrate possession. And while the description requirement does not demand any particular form of disclosure, id., or that the specification recite the claimed invention in haec verba, a description that merely renders the invention obvious does not satisfy the requirement, *Lockwood v. Am. Airlines*, 107 F.3d 1565, 1571-72 (Fed. Cir. 1997).

Based on VisionX's apparent construction of the Asserted Claims, as expressed in VisionX's Infringement Contentions, Sony lists below the grounds upon which they presently contend that the Asserted Claims are invalid under 35 U.S.C. § 112, ¶ 1 for inadequate written description. For the avoidance of any doubt, where Sony identifies a claim term in an independent claim, Sony further contends any asserted dependent claim is invalid based on the presence of the same term in the asserted dependent claim.

1. '366 Patent

Claim 1 of the '366 patent requires that various elements of the claimed sensor (a first semiconductor substrate, a pre-metal dielectric, a first interlayer dielectric, a first metal interconnection, a conductive barrier layer, and a color filter and a microlens) to be "on" a counterpart element of the claimed sensor (the second interlayer dielectric, the first semiconductor substrate, the pre-metal dielectric, the first interlayer dielectric, the first metal interconnection, the first interlayer dielectric, respectively). The '366 patent states: "[w]hen the terms "on" or "over" are used herein, when referring to layers, regions, patterns, or structures, it is understood that the layer, region, pattern or structure can be directly on another layer or structure, or intervening layers, regions, patterns, or structures may also be present." '366 patent, 2:17-22. This claim lacks written description support because it only discloses a first semiconductor substrate above the second interlayer dielectric; a pre-metal dielectric above the

first semiconductor substrate; a first interlayer dielectric above the pre-metal dielectric; a first metal interconnection above or next to the first interlayer dielectric; a conductive barrier layer above the first metal interconnection; and a color filter and a microlens above the first interlayer dielectric. Notably, the '366 patent fails to provide a written description of any of the claimed elements being *below* the counterpart element. If claim 1 is found to encompass an image sensor with the claimed element being below the counterpart element, then claim 1 and all claims depending from claim 1 are invalid for this reason.

V. OTHER GROUNDS OF UNENFORCEABILITY

Discovery is ongoing and additional discovery may reveal that the Asserted Patents are also unenforceable for other reasons, including the doctrines of laches, equitable estoppel, implied license, or fraud.

In particular, the '366 patent was procured through inequitable conduct, in part, by failing to disclose the Korean examiner's rejection of the sensor claims in the corresponding Korean patent application (KR 10-2007-0024914) ("KR '914") (SONYVX-PRIOR ART-0001616-SONYVX-PRIOR ART-0001620). The '366 patent's Korean priority application, KR '914, was filed with 15 claims. Claims 1-6 were directed to an image sensor and claims 7-15 were directed to a method of manufacturing an image sensor. On February 21, 2008, the Korean examiner rejected claim 1 because it was "similar to the configuration in [Pyo]." The Korean examiner identified only one difference, "the conductive barrier film on the metal wiring," but noted that "this is commonly used in this field," citing a Japanese application "in which a barrier metal is formed on the wiring layer." The Korean examiner similarly rejected dependent claims 2-6 because "these limitations limit simple materials or are merely structural changes, and it is not technically difficult to apply these limitations." The Korean examiner thus rejected the sensor claims over Pyo in view of commonly used barrier layers.

Claims 1-5 rejected by the Korean examiner (as translated in to English in a certified English translation) were substantially the same as claims 1 and 3-5 of the '366 patent. While the Applicant amended the method of manufacturing claims 7-15 to traverse the rejection, the Applicant canceled ("deleted") the sensor claims 1-6 without responding to the Korean examiner's arguments rejecting them.

The application that led to the '336 patent was filed on March 14, 2008 – three weeks after the Korean examiner had rejected substantially similar claims in the Korean prosecution on February 21, 2008. The Applicant filed an Information Disclosure Statement ("IDS") listing Pyo and provided an English-language translation of the Pyo abstract, but submitted the entire Pyo reference only in the original Korean. The Applicant did not submit a copy of the Korean examiner's rejection or the Applicant's cancelation of the sensor claims.

The English translation of the Pyo Abstract attached to the IDS fails to expressly disclose several elements the are disclosed by Pyo, including at least, (1) a first and a second interlayer dielectric, (2) a pre-metal dielectric, (3) a first metal interconnection (the abstract only discloses metal lines on the second substrate), and (4) a color filter.

Apparently unaware of the significance of Pyo and without the Korean examiner's rejection as a guide, the U.S. Examiner allowed the Challenged Claims without rejection over any prior art. The '366 patent is thus unenforceable due to the Applicant's inequitable conduct of failing to disclose the Korean examiner's rejection of the corresponding sensor claims in the '366 patent's priority Korean application.

VI. ACCOMPANYING DOCUMENT PRODUCTION

Pursuant to Patent Rule 3-4(b), Sony is producing or making available for inspection copies of each item of prior art identified pursuant to Patent Rule 3-3(a) which does not appear in

the file history of an Asserted Patent. Sony reserves the right to identify and produce additional documents pursuant to the Patent Rules and the orders of the Court.

Respectfully submitted,

Date: December 2, 2022

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CERTIFICATE OF SERVICE

I certify that a true copy of this document was served on counsel of record via electronic mail on December 2, 2022, with the accompanying exhibits A-1 through A-19, B-1 through B-7, and C-1 through C-11 made available for download.

/s/ *Lisa Woodbury*
Lisa Woodbury