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A Brief History of Data Conversion

A Tale of Nozzles, Relays, Tubes, Transistors, and CMOS

The need for better communication has been one of the driving forces behind technology advancements, including those in the field of data converters. To extend communication beyond the limits of speech, various methods were developed to allow communication over longer distances, such as drum beating and smoke signaling. The fundamentals of coding and decoding are apparent in these early techniques.

While other early applications of the principles of conversion can be found (see "A Tale of Two DACs: Hydraulic and Electronic"), it took the advancements in electrical science during the late 1800s to usher in the age of electronic communication, and this is where true data conversion had its beginnings, with the development of the telegraph and the telephone.

Early Electronic Data Converter History and Driving Forces

Telegraph and Telephone

Although the earliest proposals for the electric telegraph date from about 1753, most significant developments

occurred from about 1825 to 1875 [4], and the Morse code became the standard code for the telegraph.

The telegraph network rapidly expanded and ultimately led to the invention of the telephone and the subsequent formation of the Bell System. The invention of the telephone in 1875 by Alexander Graham Bell [10], [11] was probably the most significant event in the history of communications. The proliferation of the telephone generated a huge need to increase channel capacity to minimize the cost and complexity of the copper infrastructure.

This resulted in various studies regarding time-division multiplexing, and in a 1903 patent [12] Willard M. Miner described an experiment using an electromechanical rotating commutator to multiplex several analog telephone conversations onto a single pair of wires as shown in Figure 1. He determined that, to quote from his patent, each channel must be sampled at

... a frequency or rapidity approximating the frequency or average frequency of the finer or more complex vibrations which are characteristic of the voice or of articulate speech, ... as high as 4320 closures per second, at which rate

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I find that the voice with all its original timbre and individuality may be successfully reproduced in the receiving instrument. ... I have also succeeded in getting what might be considered as commercial results by using rates of closure that, comparatively speaking, are as low as 3500 closures per second, this being practically the rate of the highest note which characterizes vowel sounds.

At higher rates of rotation (corresponding to higher sample rates per channel), Miner found no perceptible improvement in speech quality, probably because of other artifacts and errors in his rather crude system. There was no follow-up to Miner's work on sampling and time division multiplexing because, at the time, no adequate electrical components were available to make it practical. However, it did illustrate the requirement that a signal must be sampled at some minimum rate to preserve the information.

Enabling Technology: Vacuum Tubes (1906) and the Feedback Amplifier (1927)

Except for early, relatively inefficient electromechanical amplifiers [6], electronic amplifier development started with the invention of the vacuum tube by Lee de Forest in 1906 [13], [14].

By 1914, vacuum tube amplifiers had been introduced into the telephone plant. Amplifier development has always been critical to data converter development, starting with the early vacuum tube circuits. Key to the technology was the invention of the feedback amplifier by Harold S. Black in 1927 [15]–[17]. The use of feedback stabilized the gain of amplifiers and made them much more suitable in repeater applications.

Figure 2 shows a drawing from a later article published by Black defining the feedback amplifier. Eventually the feedback amplifier (later called the operational amplifier, or op-amp) became a key building block

in signal conditioning circuits and data converters.

Frequency Division Multiplexing in the Bell System (1930s)

Over this period, Bell Labs developed a technology for multiplexing multiple voice channels on a single channel using a technique called frequency division multiplexing (FDM). This technique made use of Black's feedback amplifiers for the repeaters (Figure 3). FDM systems were widely used in the 1930s, but Bell Labs engineers were searching for transmission methods that were less sensitive to noise and distortion, while still allowing multiplexing.

The Invention of Pulse Code Modulation (1921)

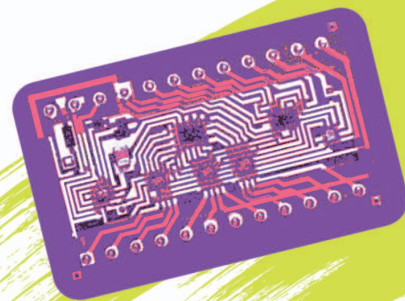
Pulse code modulation was first disclosed in a relatively obscure patent issued to Paul M. Rainey of Western Electric in 1921 [18]. The patent describes a method to transmit facsimile information in coded form over a telegraph line using 5-bit pulse control modulation (PCM). The figure from the patent is shown in Figure 4; additional labels have been added for clarity.

Rainey proposed that a light beam be focused on a transparency of the material to be transmitted. A photocell is placed on the other side of the transparency to gather the light and produce a current proportional to the intensity of the light. This current drives a galvanometer, which in turn moves another beam of light that activates one of 32 individual photocells, depending upon the amount of galvanometer deflection. Each individual photocell output activates a corresponding relay. The five relay outputs are connected in such a way as to generate the appropriate code corresponding to the photocell location. The digital code is thus generated from an "m-hot out of 32 code," similar to modern flash converters. The output of this simple electro-optical-mechanical "flash" converter is then

transmitted serially using a rotating electromechanical commutator, called a distributor.

The serial data is transmitted, received, and converted into a parallel format using a second distributor and a bank of relays. The received code determines the combination of relays to be activated, and the relay outputs are connected across appropriate taps of a resistor, which is in series with the receiving lamp. The current through the receiving lamp therefore changes depending upon the received code, thereby varying its intensity proportionally to the received code and performing the digital-to-analog conversion. The receiving lamp output is focused on a photographically sensitive receiving plate, thereby reproducing the original image in quantized form.

Rainey's patent illustrates several important concepts: quantization using a flash ADC, serial data transmission, and reconstruction of the quantized data using a digital-to-analog converter (DAC). These are the fundamentals of PCM. However, his invention aroused little interest at the time and was forgotten by Bell System engineers. His



A TALE OF TWO DACs: HYDRAULIC AND ELECTRONIC

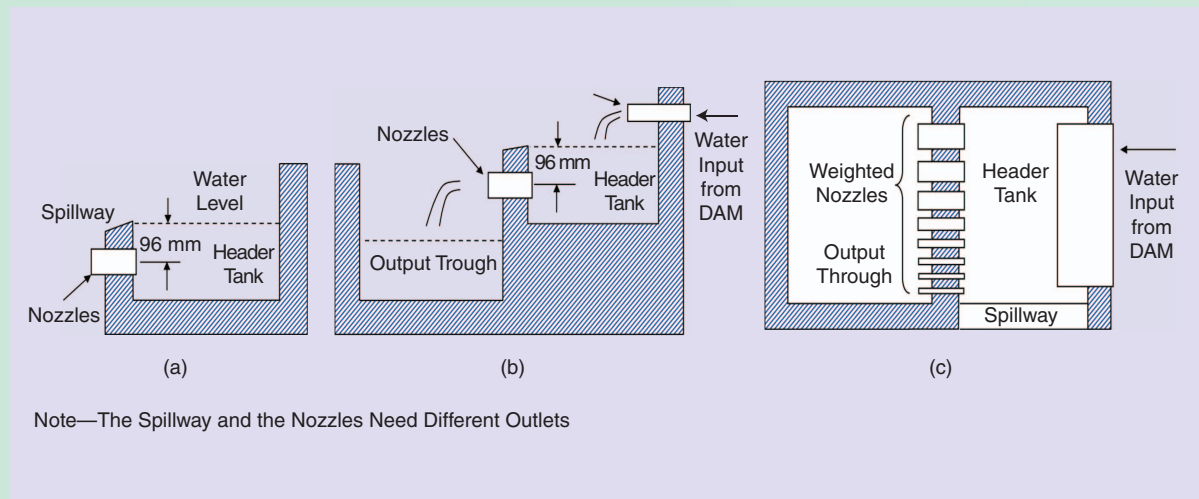
It is difficult to determine exactly when the first data converter was made or what form it took. One of the earliest recorded digital-to-analog converters (DACs) known to the author of this article is not electronic at all, but hydraulic. Turkey, under the Ottoman Empire, had problems with its public water supply, and sophisticated systems were built to meter water. One of these, dating to the 1700s, is shown in Figure S1. An example of an actual dam using this metering system was the Mahmud II Dam built in the early 1800s near Istanbul and described in [3].

The metering system uses reservoirs (labeled *header tank* in the figure diagrams) maintained at a constant depth (corresponding to the reference potential) by means of a spillway over which water *just* trickled (the criterion was that it be sufficient flow to float a straw). This is illustrated in Figure S1(a). The water output from the header tank is controlled by a series of gated *nozzles* of different sizes submerged 96 mm below the surface of the water [3]. The output of the nozzles feeds an *output trough* as shown in Figure S1(b). A photo of the nozzle system is shown in Figure S2.

The flow rates were measured in the basic unit of 1 lüle (= 36 liter/min or 52 m³/day). Details of the metering system using the weighted nozzles are shown in Figure S1(c). This is functionally a DAC with manual (rather than digital, no doubt) input and a wet output, and it may be the oldest DAC in the world.

With the expansion of electrical power in the 1800s, one of the first electronic DACs was invented by Lord Kelvin (William Thomson) and C.F. Varley and is shown in Figure S3. The first resistor divider stage is simply called a “Kelvin divider” or, in modern terms, a resistor “string DAC.” The Kelvin–Varley divider consists of a number of stages of precision resistors interconnected with switches or relays to generate a precision output voltage.

The Kelvin–Varley DAC’s relative accuracy is determined only by the accuracy of the precision resistors, assuming that the switch resistance is negligible and the output is buffered. Modern instruments such as the Fluke 720A use this technique and achieve 0.1 ppm resolution (7 decades) and 0.1 ppm absolute linearity. Variations of this architecture are found in modern IC DACs and are often referred to as “segmented” string DACs.



Note—The Spillway and the Nozzles Need Different Outlets

FIGURE S1: Early 1700s weighted water metering system: (a) header system, (b) sectional view, and (c) top view. Adapted from Kâzım Çeçen, *Sinan’s Water Supply System in Istanbul*, Istanbul Technical University/Istanbul Water and Sewage Administration, Istanbul, Turkey, 1992–1993, pp. 165–167.

patent was discovered years later after many other PCM patents had already been issued.

The Mathematical Foundations of PCM (1924)

In the mid-1920s, Harry Nyquist studied telegraph signaling with the objective of finding the maximum signaling rate possible over a channel with a given bandwidth, W . His results are summarized in two classic papers

published in 1924 [19] and 1928 [20], respectively.

If the telegraph signal is band-limited to a frequency W by the transmission channel, Nyquist’s conclusion was that the telegraph pulse rate, $1/T$, could not be increased beyond $2W$ pulses per second without the loss of information. Another way of stating this conclusion is *if a signal is sampled instantaneously at regular intervals*

at a rate at least twice the highest significant signal frequency, then the samples contain all the information in the original signal. This is the basis of sampling theory. Except for a somewhat general article by Hartley in 1928 [21], there were no significant additional publications on the specifics of sampling until 1948 in the classic papers by Shannon, Bennett, and Oliver [22]–[25], which solidified PCM theory for all time.



FIGURE S2: Nozzle outputs from the header tank in the Mahmud II Dam. (From Kâzım Çeçen, *Sinan's Water Supply System in Istanbul*, Istanbul Technical University/Istanbul Water and Sewage Administration, Istanbul, Turkey, 1992-1993, pp. 165-167. Reproduced with the permission of Istanbul Technical University, Istanbul, Turkey.)

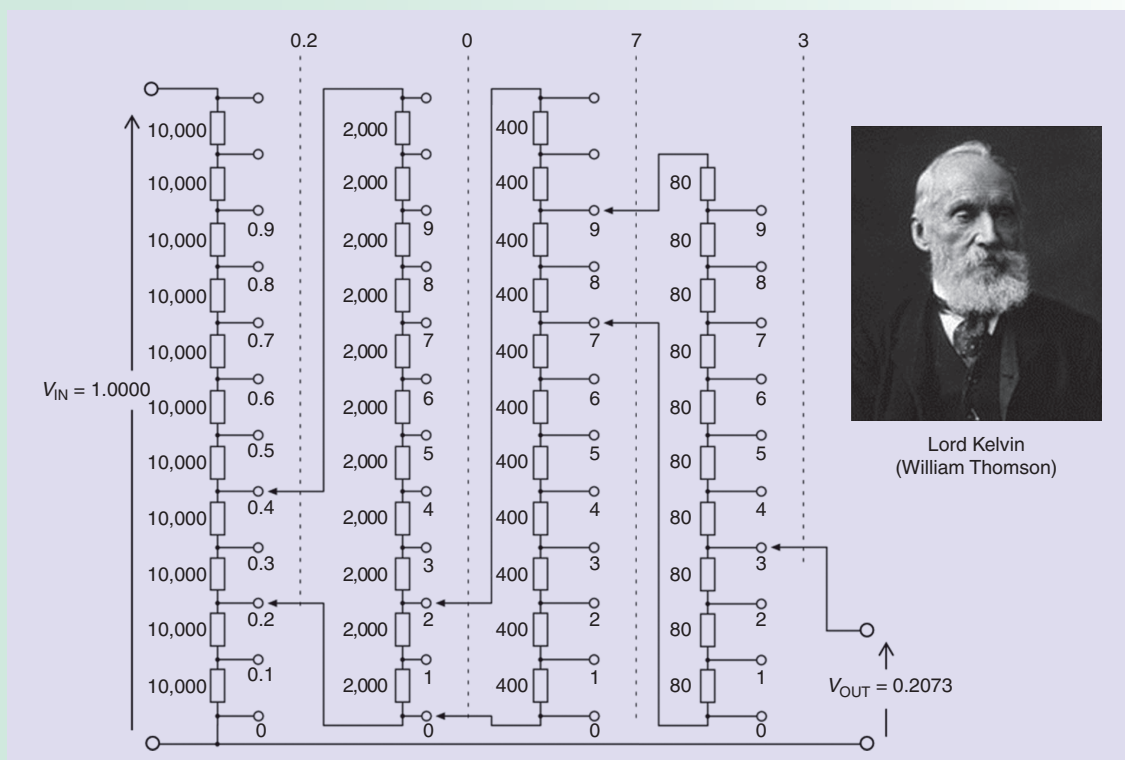


FIGURE S3: Kelvin-Varley DAC invented in the 1800s.

The PCM Patents of Alec Harley Reeves (1937)

By 1937 FDM based on vacuum tube technology was widely used in the telephone industry for long-haul routes. However, noise and distortion were the limiting factors in expanding the capacity of these systems. Although wider bandwidths were becoming available on microwave links, the additional noise and distortion made them difficult to adapt to FDM signals.

Alec Harley Reeves had studied analog-to-time conversion techniques using pulse-time modulation (PTM) during the beginning of his career in the 1920s. In fact, he was one of the first to make use of counter chains to accurately define time bases using bistable multivibrators invented by Eccles and Jordan a few years earlier [4, p. 21]. In PTM, the amplitude of the pulses is constant, and the analog information is contained in the relative timing of

the pulses. This technique gave better noise immunity than strictly analog transmission, but Reeves was shortly to invent a system that would completely revolutionize communications from that point forward.

It was, therefore, the need for a system with the noise immunity similar to the telegraph system that led to the (re-)invention of pulse PCM by Reeves at the Paris labs of the International Telephone and

Telegraph Corporation in 1937. The very first PCM patent by Reeves was filed in France, but it was immediately followed by similar patents in Britain and the United States, all listing Reeves as the inventor [26]. These patents were very comprehensive and covered the far-reaching topics of 1) general principles of quantization and encoding; 2) the choice of resolution to suit the noise and bandwidth of the transmission medium; 3) transmission of signals in digital format serially, in parallel, and as modulated carriers; and 4) a counter-based design for the required 5-bit, 6-kS/s ADCs and DACs. Unlike the previous PCM patent by Rainey in 1926, Reeves took full advantage of existing vacuum tube technology in his design.

The ADC and DAC developed by Reeves represent one of the first all-electronic data converters on record. The ADC technique basically uses a sampling pulse to take a sample of the analog signal, set an R/S flip-flop, and simultaneously start a controlled ramp voltage. The ramp voltage is compared with the input, and when they are equal, a pulse is generated that resets the R/S flip-flop. The output of the flip-flop is a pulse whose width is proportional to the analog signal

at the sampling instant. This pulse-width modulated (PWM) pulse controls a gated oscillator, and the number of pulses out of the gated oscillator represents the quantized value of the analog signal. This pulse train can be easily converted to a binary word by driving a counter. In Reeves' system, a master clock of 600 kHz is used, and a 100:1 divider generates the 6-kHz sampling pulses. The system uses a 5-bit counter, and 31 counts (out of the 100 counts between sampling pulses) therefore represent a full-scale signal.

The DAC uses a similar counter and clock source. The received binary code is first loaded into the counter, and the R/S flip-flop is reset. The counter is then allowed to count upward by applying the clock pulses. When the counter overflows and reaches 00000, the clock source is disconnected, and the R/S flip-flop is set. The number

of pulses counted by the encoding counter is thus the complement of the incoming data word. The output of the R/S flip-flop is a PWM signal whose analog value is the complement of the input binary word. Reeves uses a simple low-pass filter to recover the analog signal from the PWM output. The phase inversion in the DAC is easily corrected in either the logic or in an amplifier further down the signal chain [26].

Reeves' patents covered all the essentials of PCM: sampling, quantizing, and coding the digitized samples for serial, parallel, phase-modulated, and other transmission methods. On the receiving end, Reeves proposed a suitable decoder to reconstruct the original analog signal. In spite of the significance of his work, it is interesting to note that after the patent disclosures, Reeves shifted his attention to the shortwave transmission of speech using pulse-amplitude modulation, pulse-duration modulation, and pulse-position modulation, rather than pursuing PCM techniques.

A block diagram of a PCM system from the patent is shown in Figure 5.

PCM and the Bell System: World War II Through 1948

Under a cross-licensing arrangement with the International Telephone and Telegraph Corporation, Bell Telephone Laboratories' engineers reviewed Reeves' circuit descriptions and embarked upon their own pursuit of PCM technology. Starting in about 1940 and during World War II, studies were conducted on a speech secrecy system that made PCM techniques mandatory.

By the end of the war, several groups at Bell Labs were studying PCM; however, most of the wartime results were not published until several years later because of security issues. The work of H.S. Black, J.O. Edson, and W.M. Goodall were published between 1947

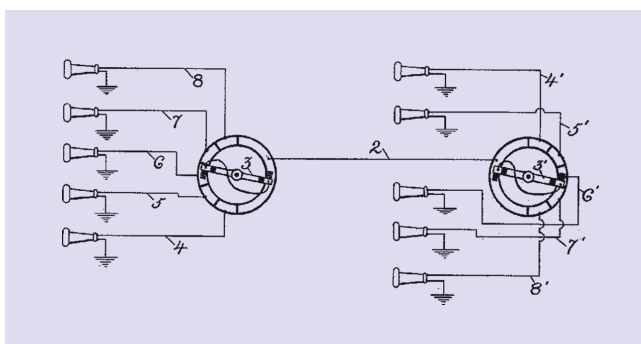


FIGURE 1: One of the earliest references to a criterion for determining the minimum sampling rate required to reconstruct a signal. Extracted from Williard M. Miner, "Multiplex Telephony," U.S. Patent 745, 734, filed 26 February 1903, issued 1 December 1903.

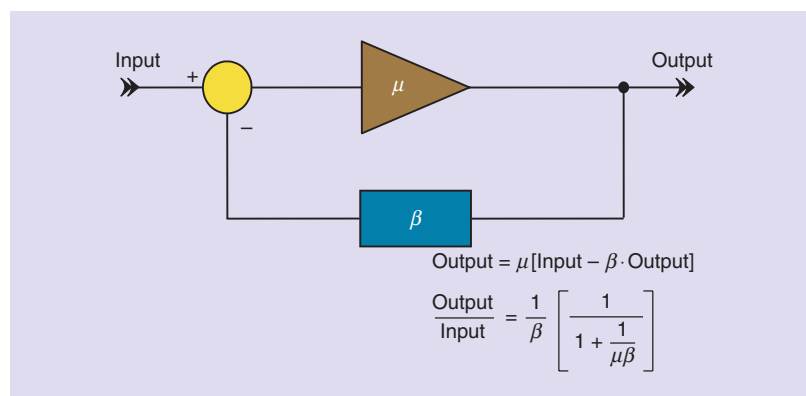


FIGURE 2: Harold Black's feedback amplifier of 1927. Harold S. Black, "Stabilized feedback amplifiers," *Bell System Technical Journal*, vol. 13, no. 1, January 1934.

and 1948. [27]–[29]. Their emphasis was on speech encryption systems based on PCM techniques, and many significant developments came out of their work. A PCM system which digitized the entire voice band to 5 bits, sampling at 8 kS/s using a successive approximation ADC, was described by Edson and Black [27], [28]. W.M. Goodall described an experimental PCM system in his classic paper based on similar techniques [29].

Some of the significant developments that came out of this work were the successive approximation ADC, the electron-beam coding tube, the Shannon-Rack decoder, and the logarithmic spacing of quantization levels (companding), along with practical demonstrations that PCM was feasible. The results were nicely summarized in a 1948 article by L.A. Meacham and E. Peterson describing an experimental 24-channel PCM system [30].

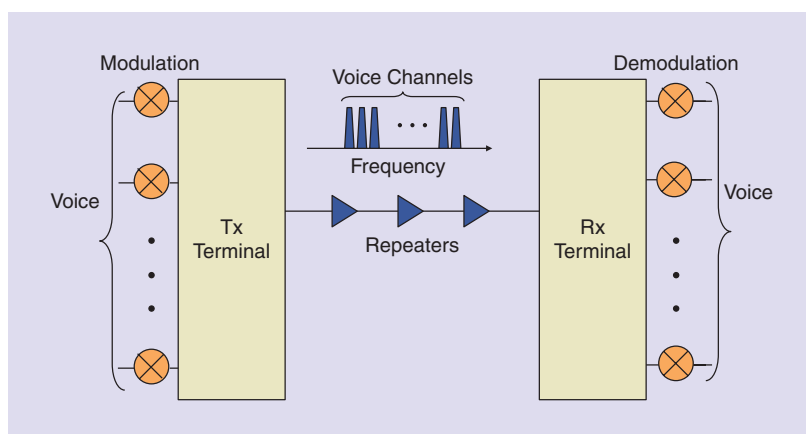


FIGURE 3: An FDM system.

A significant development in ADC technology during the period was the electron-beam coding tube shown in Figure 6. The tube described by R.W. Sears [31] was capable of sampling at 96 kS/s with 7-bit resolution. The basic electron beam

coder concepts are shown in Figure 6 for a 4-bit device. The early tubes operated in the serial mode [Figure 6(a)]. The analog signal is first passed through a sample-and-hold, and during the “hold” interval, the beam is swept horizontally across the

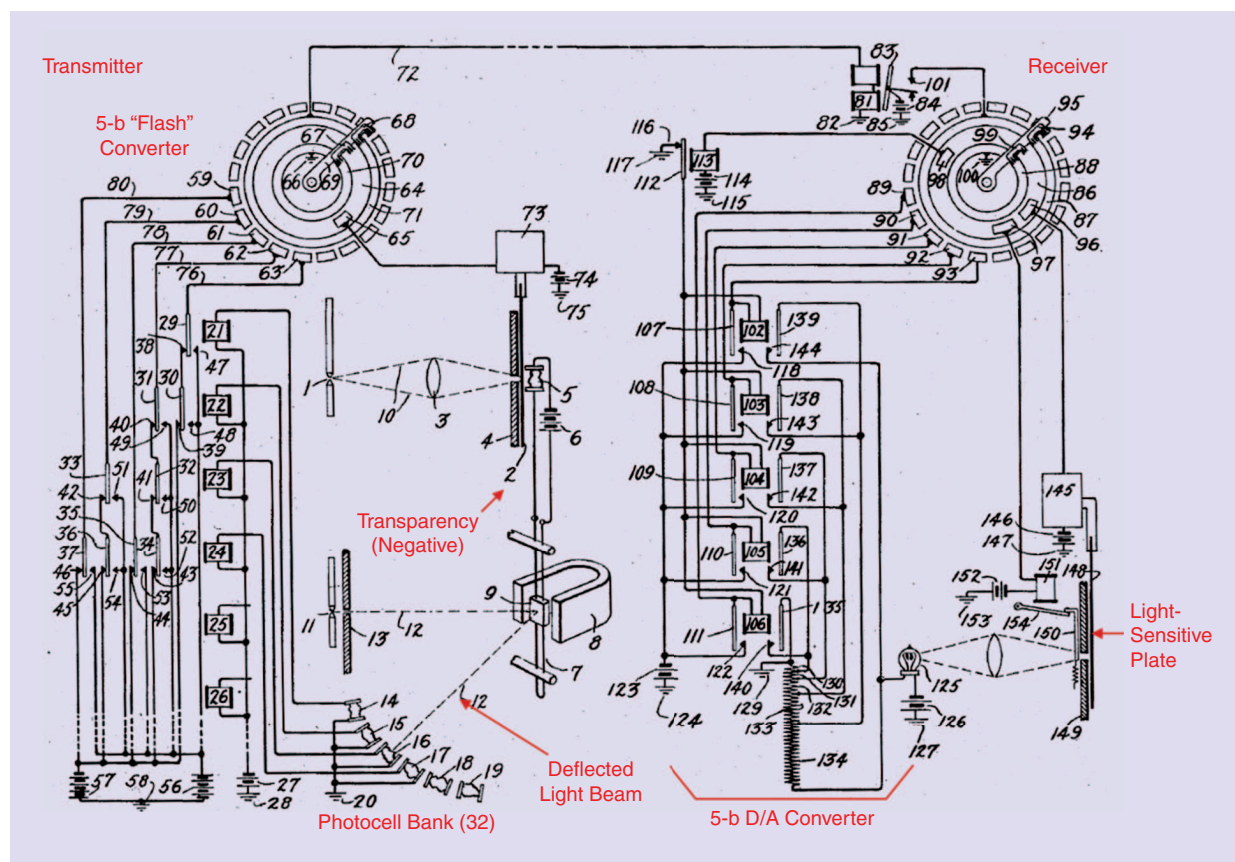


FIGURE 4: The first disclosure of PCM. Paul M. Rainey, “Facsimile Telegraph System,” U.S. Patent 1,608,527, filed 20 July 1921, issued 30 November 1926.

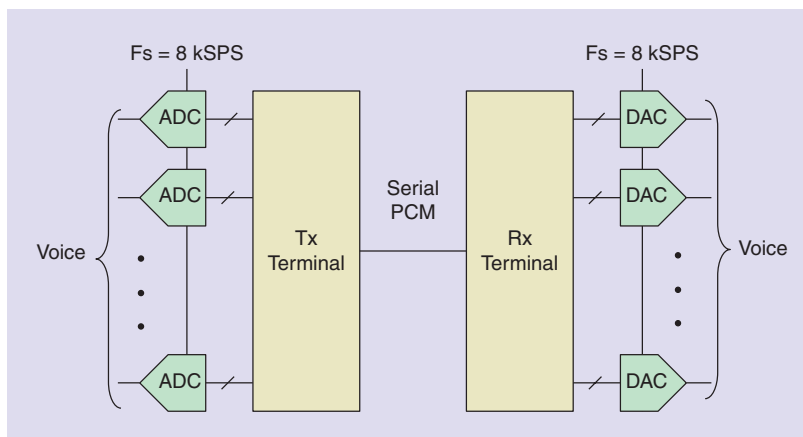


FIGURE 5: The PCM system proposed by Alec Harley Reeves. Alec Harley Reeves, “Electric Signaling System,” U.S. Patent 2,272,070, filed 22 November 1939, issued 3 February 1942.

tube. The Y-deflection for a single sweep therefore corresponds to the value of the analog signal from the sample-and-hold. The shadow mask is coded to produce the proper binary code, depending on the vertical deflection. The code is registered by the collector, and the bits are generated in serial format. Later tubes used a fan-shaped beam [shown in Figure 6(b)], creating the first electronic “flash” converter delivering a parallel output word.

Early electron tube coders used a binary-coded shadow mask, and large errors (sparkle codes) could occur if the beam straddled two adjacent codes and illuminated both of them. The way these errors occur is illustrated in Figure 7(a), where the horizontal line represents the beam sweep at the mid-scale transition

point (transition between code 0111 and code 1000). For example, an error in the most significant bit (MSB) produces an error of $1/2$ scale. These errors were minimized by placing fine horizontal sensing wires across the boundaries of each of the quantization levels. If the beam initially fell on one of the wires, a small voltage was added to the vertical deflection voltage, which moved the beam away from the transition region.

The errors associated with binary shadow masks were eliminated by using a Gray code shadow mask as shown in Figure 7(b). This code was originally called the “reflected-binary” code, and was invented by Elisha Gray in 1878, and later re-invented by Frank Gray in 1949 [32]. The Gray code has the property that adjacent levels differ by only one

digit in the corresponding Gray-coded word. Therefore, if there is an error in a bit decision for a particular level, the corresponding error after conversion to binary code is only one least significant bit (LSB). In the case of mid-scale, note that only the MSB changes. It is interesting to observe that this same phenomenon can occur in modern comparator-based flash converters due to comparator metastability. With small overdrive, there is a finite probability that the output of a comparator will generate the wrong decision in its latched output, producing the same effect if straight binary decoding techniques are used. In many cases, Gray code, or “pseudo-Gray” codes, are used to decode the comparator bank output before finally converting to a binary code output.

In spite of the many mechanical and electrical problems relating to beam alignment, electron tube coding technology reached its peak in the mid-1960s with an experimental 9-bit coder capable of 12-mega-samples per second (Ms/s) sampling rates [33]. Shortly thereafter, however, advances in solid-state ADC techniques quickly made the electron tube converter technology obsolete.

Op-Amps and Regenerative Repeaters: The Transition from Vacuum Tubes to Solid State (1950s)

The invention of the germanium transistor in 1947 [34]–[36] was key to the development of PCM and all other

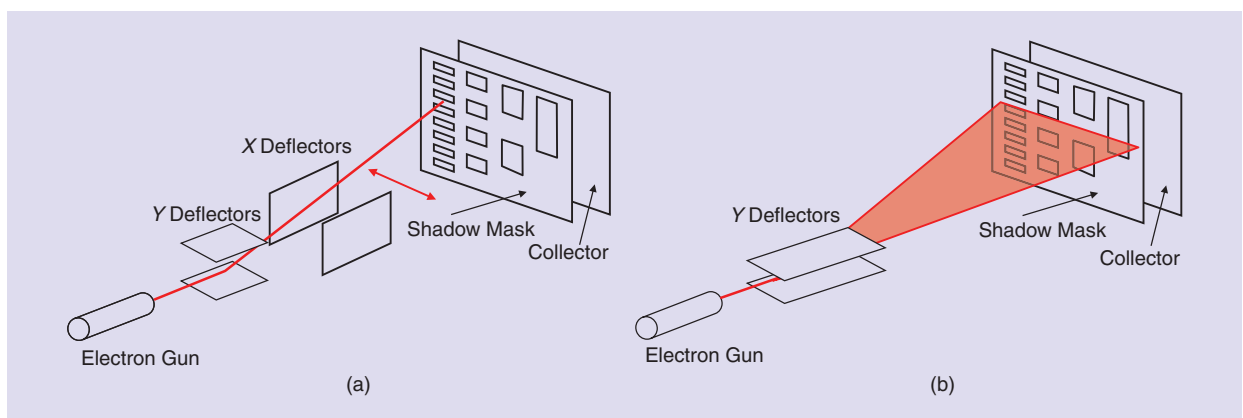


FIGURE 6: The electron-beam coder: (a) serial mode and (b) parallel mode.

Datrac was the first commercial ADC suitable for digitizing ac waveforms, such as speech.

During the same period, a few other companies manufactured lower speed ADCs suitable for digital voltmeter measurement applications, and there were offerings of optical converters based on coded discs for measuring the angular position of shafts in avionics applications [44]. Converters of the middle to late 1950s used a combination of vacuum tubes, solid-state diodes, and transistors to implement the conversion process. A few of the companies in the data converter business at the time, in addition to Epsco, were Non-Linear Systems, Inc., J.B. Rea, and Adage. To gain further insight to the converters of the 1950s, [42], [44]–[47] are excellent sources.

Commercial Data Converters of the 1960s Drivers: Industrial, PCM, and Defense

During the mid-1950s through the early 1960s, electronic circuit designs began to migrate from vacuum tubes to transistors, thereby opening up many new possibilities in data conversion products. As indicated earlier, the silicon transistor was responsible for the increased interest in solid-state designs. There was more and more interest in data converter products, as indicated in survey articles published in 1964 [47] and 1967 [48]. Because these devices were basically unfamiliar to new customers, efforts



- ◆ 19 in × 15 in × 26 in
- ◆ 500 W
- ◆ 150 lb
- ◆ US\$8,500

FIGURE 8: 1954 Epsco Datrac 11-bit, 50-kSPS vacuum tube ADC designed by Bernard M. Gordon of EPSCO. (Reproduced with the permission of Analogic Corporation, Peabody, Massachusetts.)

were begun to define specifications and testing requirements for converter products [49]–[58].

The IBM-360 mainframe computer and solid-state minicomputers (such as the Digital Equipment Corporation's Programmed Data Processor series starting in 1963) added to the general interest in data analysis applications. Other driving forces requiring data converters in the 1960s were industrial process control, measurement, PCM, and military systems.

Efforts continued during the 1960s at Bell Labs to develop high speed

converters (e.g., 9 bits, 5 Ms/s) for PCM applications [59], and the military division of Bell Labs began work on developing hardware and software for an anti-ballistic missile system.

In 1958 the U.S. Army began the development of the Nike-Zeus anti-ballistic missile system, with Bell Labs responsible for much of the hardware design. This program was replaced by Nike-X in 1963, which was the first program to propose a digitally controlled phased-array radar for guiding the short- and long-range interceptor missiles. The objective of the system was to intercept and destroy incoming Soviet nuclear warheads above the atmosphere, thereby protecting U.S. population centers. The program continued under the Johnson administration as Sentinel and under the Nixon administration as Safeguard, until it was terminated after the SALT talks in 1975.

Key to the Nike-X/Sentinel/Safeguard systems was the use of digital techniques to control the phased-array radar and perform other command and control tasks. The logic was resistor-transistor-logic mounted in hybrid packages. Also important to the system were the high-speed ADCs used in the phased-array radar receiver. Early prototypes for the required 8-bit 10-Ms/s ADC were developed by John M. Eubanks and Robert C. Bedingfield at Bell Labs between 1963 and 1965. In 1966, these two pioneers in high speed data conversion left Bell Labs and founded Computer Labs—a company based in Greensboro, North Carolina—and introduced a commercial version of this ADC.

The 8-bit, 10-Ms/s converter was rack-mounted, contained its own linear power supply, dissipated nearly 150 W, and sold for approximately US\$10,000 (see Figure 9). The same technology was used to produce 9-bit, 5-Ms/s and 10-bit 3-Ms/s versions. Although the next generation of Computer Labs' designs would take advantage of modular op-amps (Computer Labs OA-125 and FS-125), ICs such as the Fairchild μ A710/711 comparators, and 7400 transistor-transistor logic



FIGURE 9: The HS-810, an 8-bit, 10-Ms/s ADC released by Computer Labs in 1966.

(TTL), the first ADCs offered used all discrete devices.

The early high-speed ADCs produced by Computer Labs were primarily used in research and development projects associated with radar receiver development by companies such as Raytheon, General Electric, and MIT Lincoln Labs.

In the mid-1960s, development of lower speed instruments, PC-boards, and modular ADCs was pioneered by such companies as Analogic (founded by Bernard M. Gordon) and Pastoriza Electronics (founded by James Pastoriza). Other companies in the data converter business were Adage, Burr Brown, General Instrument Corporation, Radiation, Inc., Redcor Corporation, Beckman Instruments, Reeves Instruments, Texas Instruments, Raytheon Computer, Preston Scientific, and Zeltex, Inc. Many of the data converters of the 1960s took the form of digital voltmeters that used integrating architectures, although Adage introduced an 8-bit, 1-Ms/s sampling ADC, the Voldicon VF7, in the early 1960s [47].

In addition to the widespread proliferation of discrete transistor circuits in the 1960s, various IC building blocks became available, which led to size and power reductions in data converters. In 1964 and 1965, Fairchild introduced two famous Bob Widlar IC designs: the $\mu A709$ op-amp and the $\mu A710/\mu A711$ comparators. These were quickly followed by a succession of linear ICs from Fairchild and other manufacturers. The 7400-series of TTL and high-speed emitter-coupled-logic (ECL) also emerged during this period as well as the 4000-series CMOS logic from RCA in 1968. In addition to these devices, Schottky diodes, Zener reference diodes, field-effect transistors (FETs) suitable for switches, and matched dual junction-gate FETs also made up some of the building blocks required in data converter designs of the period.

In 1965 Ray Stata and Matt Lorber founded Analog Devices, Inc. (ADI) in Cambridge, Massachusetts. The

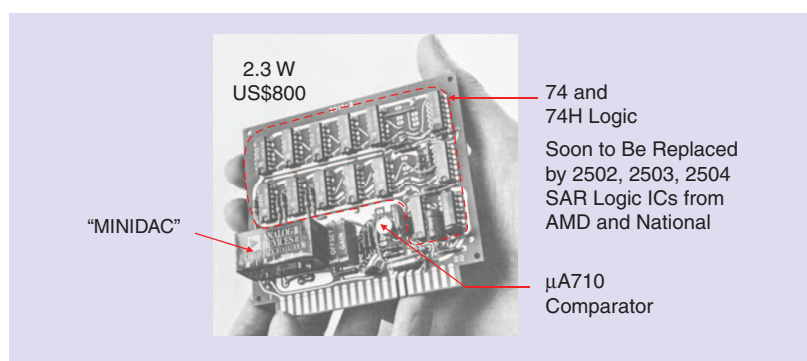


FIGURE 10: The ADC-12U, a 12-bit, 10- μ s successive-approximation ADC from the Pastoriza Division of Analog Devices, 1969.

initial product offerings were high performance modular op-amps, but in 1969 ADI acquired Pastoriza Electronics, a leader in data converter products, thereby making a solid commitment to both data acquisition and linear products.

Pastoriza had a line of data acquisition products; Figure 10 shows a photograph of a 1969 12-bit, 10- μ s general purpose successive-approximation ADC, the ADC-12U, that sold for approximately US\$800. The architecture was successive approximation, and the ADC-12U utilized a $\mu A710$ comparator, a modular 12-bit "MiniDAC," and 14 7400-series logic packages to perform the successive-approximation conversion algorithm.

The MiniDAC module was actually constructed from quad-switch

ICs (AD550) and a thin film network (AD850) as shown in Figure 11. Figure 12 shows details of the famous quad switch patented by James Pastoriza [60].

Notice that in the ADC-12U, the implementation of the successive approximation algorithm required 14 logic packages. In 1958 Bernard Gordon had filed a patent on the logic to perform the successive approximation algorithm [43], and in the early 1970s, Advanced Micro Devices and National Semiconductor introduced commercial successive-approximation register logic ICs: the 2502 (8-bit, serial, not expandable), 2503 (8-bit, expandable), and 2504 (12-bit, serial, expandable). These were designed specifically to perform the register and control

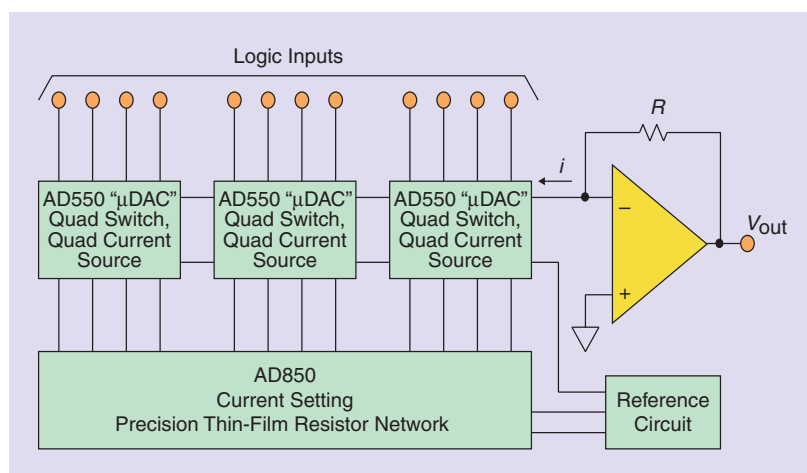


FIGURE 11: A 1969-vintage 12-bit MiniDAC using quad current switches, a thin film resistor network, a voltage reference, and an op-amp.

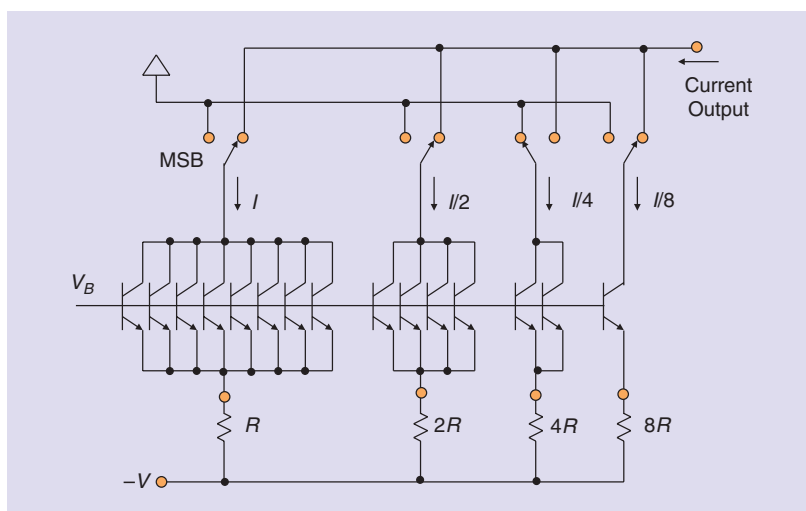


FIGURE 12: The quad-switch DAC building block with external thin film resistor network.

functions in successive approximation ADCs. These became standard building blocks in many modular and hybrid data converters. In fact, the acronym SAR actually stands for “successive-approximation register,” and hence the term “SAR ADC.” Earlier converters utilizing the successive-approximation architecture were simply referred to as *sequential coders*, *feedback coders*, or *feedback subtractor coders*.

Specifications and Testing of Data Converters in the 1960s

There were no guidelines or industry standards for specifying and testing the early data converter of the 1960s, so the manufacturers did the best they could based on their knowledge of their products and potential applications. Bernard Gordon was active in this area along with a few others, and [49]–[58] show the evolution of the thinking relating to data converter specifications and testing in the 1960s (see also “Data Converter Architectures”).

During the 1960s, it became clear that dynamic specifications (SNR, SFDR, THD, etc.) were important for many applications, and in the early 1970s minicomputers such as the PDP-11 enabled data analysis of ADC outputs including FFTs and histograms. Prior to this time, dynamic

testing generally consisted of “back-to-back” tests where the ADC output drove a DAC, and analog test equipment was used to examine the reconstructed DAC output. The use of computers to analyze the ADC output directly eliminated errors due to the reconstruction DAC.

Data Converters of the 1970s and the Beginnings of Integration

The year 1970 began one of the most exciting decades in the history of data converters. The ADC/DAC market was driven by many emerging applications, including high resolution digital voltmeters, industrial process control, digital video, military phased-array radar, medical imaging, vector scan displays, and raster scan displays. Most of these systems had formerly utilized conventional analog signal processing techniques, and the increased availability of low-cost computing technology generated a desire to take advantage of the increased performance and flexibility offered by digital signal processing and analysis—and, of course, the need for compatible data converters.

As a result, a number of companies entered the data converter field, including Analog Devices, Analogic Corporation (initially Epsco and later Gordon Engineering), Burr Brown,

Computer Labs, Dattel, Hybrid Systems, ILC/Data Device Corporation, Micronetworks, National Semiconductor, Teledyne Philbrick, and Zeltex.

IC building blocks, as well as complete IC data converters of the 1970s, came from Analog Devices, Advanced Micro Devices, Fairchild, Signetics, Intersil, Micro Power Systems, Motorola, National Semiconductor, TRW (LSI Division), and Precision Monolithics.

The data converters of the 1970s made maximum use of all the technologies available: monolithic, modular, and hybrid, with the modular and hybrid products typically offering higher resolution and faster speed than the existing monolithic parts.

Monolithic Bipolar DACs of the 1970s

The earliest monolithic DACs were made using bipolar process technology; they included only the basic core of a complete DAC—the array of switches and resistors to set the weight of each bit. Some examples were the Motorola 1408 and a later higher speed derivative, the DAC08, introduced in 1975 by PMI (Precision Monolithics).

These converters were produced by several manufacturers and were available at low cost. However, they required many additional external components to be usable in a system design. These external components included several resistors, a voltage reference, a latch, an output op-amp, possibly a compensation capacitor, and usually one or more trimming potentiometers.

Converters like the 1408 and DAC08 were limited to 8-bit accuracy by the matching and tracking limitations of the diffused resistors. When higher accuracy is required, lower temperature coefficient resistors are needed, and some means of post-fabrication adjustment is desirable.

Thin film resistors exhibit low temperature coefficients and can be trimmed with a laser—they are well suited for use in data converters. By the mid-1970s, Analog Devices had developed considerable expertise, not only in the deposition of thin

DATA CONVERTER ARCHITECTURES

The basic algorithm used in the successive approximation (initially called *feedback subtraction*) ADC conversion process can be traced back to the 1500s, relating to the solution of a certain mathematical puzzle regarding the determination of an unknown weight by a minimal sequence of weighing operations [61]. The familiar electronic implementation of the successive

approximation ADC using the balance scale analogy is shown in Figure S4.

It is interesting to note that many of the fundamental ADC architectures used today were discovered and published in one form or another by the late 1960s; these are listed in Table S1. The dates given are of first publication or patent filings, whichever occurred first.

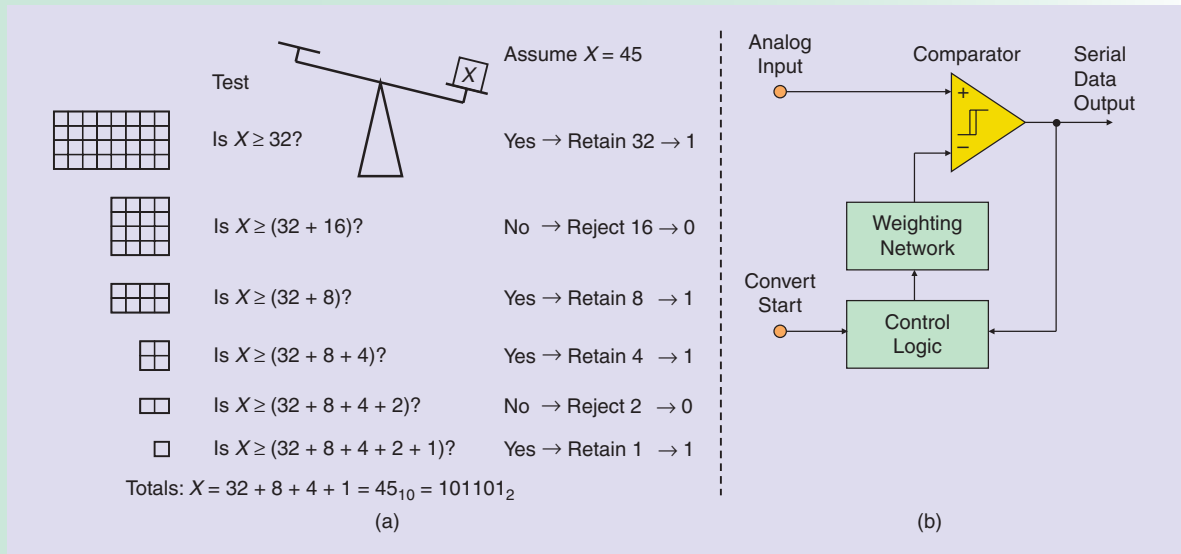


FIGURE S4: A successive approximation ADC: (a) balance scale analogy and (b) electronic implementation (feedback subtraction ADC).

TABLE S1. DATA CONVERTER ARCHITECTURES BY DATE OF APPEARANCE.

ARCHITECTURE	DATE	REFERENCE
SAR algorithm	1500s	[61]
Reeves' counting ADC	1939	[26]
Successive approximation ADC	1947	[29]
Flash or parallel ADC (electron tube coder)	1948	[31]
Tracking ADC	1950	[62]
Delta modulation and differential PCM	1950	[63]
Voltage-to-frequency converter	1952	[64]
First- and second-order loops, multibit, with oversampling with noise shaping (sigma-delta, but without the digital part)	1954	[65]
Bit-per-stage ADC (binary and Gray)	1956	[66]
Subranging ADC	1956	[67]
Dual-slope ADC	1957	[68]
Multibit sigma-delta implementation	1961	[69]
Sigma-delta ADC (first use of the name)	1962	[70]
Folding ADC (Gray code)	1962	[71]
Subranging ADC with error correction (redundancy)	1964	[72]
Pipelined ADC with error correction (redundancy)	1966	[73]
Triple-slope ADC	1967	[74]
Complete sigma-delta ADC with digital filtering	1969	[75]
Generalized pipelined architecture	1971	[76]
Quad-slope ADC	1973	[77]
Continuous time sigma-delta	1976	[78]
Bandpass sigma-delta	1988	[79]

film resistors, but also in trimming at the wafer level.

Analog Devices's AD562, designed by Bob Craven and introduced in 1974, was originally a "compound monolithic" manufactured using two IC chips mounted in the same package, without the traditional hybrid substrate for mounting and interconnection. Instead, the two chips were designed so that a set of wire bonds between the two chips (in addition to the usual ones to the package pins) were all that were necessary to assemble a 12-bit accurate DAC in an IC package. In the original AD562, one chip contained the thin film resistor network (including the bit weight-setting resistors and output gain-setting resistors), and the other chip contained the reference control amplifier and the current switches for the 12 bits. As the processing matured, the manufacture of larger chips became more practical. The two chips of the original AD562 were later merged into a single-chip version. It became the first 12-bit DAC qualified by the U.S. Department of Defense under MIL-M-38510.

While the AD562 was the first 12-bit IC DAC and embodied the solution to some extremely difficult design problems, it was still really only a building block, since it lacked *buffer latches*, a *voltage reference*, and an *output amplifier*. Shortly after the two-chip AD562 was introduced [80], [81], a version with a third chip was developed. The third chip was a 2.5 V bandgap reference designed by Paul Brokaw and described in detail in [82], [83]. This made DAC function much more complete. The resulting product, known as the AD563, also became quite popular and eventually made the transition to a completely monolithic single-chip device.

Another limitation of the AD562 was that, while reasonably fast, it lacked sufficient speed for many applications—its settling time was approximately 1 μ s. Later advances in switch design and Zener diode

fabrication led to a higher speed DAC, the AD565, introduced in 1978 (later followed by the AD565A in 1981).

The bit switches used in the AD565 were much smaller than those used in the AD562, allowing a substantial reduction in chip area and increasing the yield of good chips per wafer. The new switches yielded a settling time of 200 ns to 1/2 LSB. The AD565 used a buried Zener reference which had less noise than the bandgap reference used in the AD563. The AD565 retained the same pinout as the earlier AD563, allowing drop-in replacement with improved performance and lower price.

It should be noted that the first monolithic single-chip 10-bit DAC with thin film laser wafer trimmed resistors and internal reference was the AD561, designed by Peter Holloway, which was introduced by Analog Devices in 1976 [84]. This DAC utilized a method of compensating for errors produced by operating the internal current source transistors at different current densities. This idea is patented by Paul Brokaw and is one of the most widely cited patents in data conversion [85].

Monolithic CMOS DACs of the 1970s

As we have seen, the early commercially available monolithic DACs were principally processed by conventional bipolar linear processing techniques. Before 1974, when the AD7520 CMOS DAC was introduced, 10-bit conversion had been difficult to obtain with good yields (and low cost) because of the finite β of switching devices, the V_{BE} -matching requirement, the matching and tracking requirements on the diffused resistor ladders, and the tracking limitations caused by the thermal gradients produced by high internal power dissipation.

Most of these problems were solved or avoided with CMOS devices. The CMOS transistors have nearly infinite current gain, eliminating β problems. There is no equivalent in CMOS circuitry to a bipolar transistor's V_{BE} drop; instead, a CMOS

switch in the ON condition is almost purely resistive, with the resistance value controllable by device geometry. The temperature problems of diffused resistors were eliminated by using thin film resistors instead. The first CMOS IC DAC—the AD7520 10-bit, 500-ns multiplying DAC designed by Hank Krabbe—was introduced in 1974.

The AD7520 architecture was extended to 12-bit resolution in the AD7541 by merely adding additional switch cells and resistors. However, to achieve 12-bit linearity, laser trimming at the wafer level was required. The AD7541, introduced in 1978, was the first 12-bit CMOS multiplying DAC. Settling time to 1/2 LSB was 1 μ s.

The AD7520 and AD7541 were the beginning of an entirely product line of general purpose multiplying CMOS DACs from Analog Devices. Future DAC products added a second latch and are referred to as "double-buffered" DACs. The input latch is used to load the data (either serial, parallel, or in bytes), and when the second parallel "DAC latch" is clocked, the DAC output is updated.

Data converter designers soon realized the importance of making them easy to interface to microprocessors and digital signal processors (DSPs), and this trend added additional functionality to the devices and continues to this day.

Monolithic ADCs of the 1970s

Although most of the ADCs of the early 1970s were modular or hybrid, there was considerable effort by data converter manufacturers to produce an all-monolithic ADC. The first complete monolithic ADC was the 10-bit, 25- μ s AD571 SAR ADC introduced in 1978 and designed by Paul Brokaw [86]. The AD571 was designed on a bipolar process with laser wafer trimmed thin film resistors. To implement the logic functions required in the SAR ADC, integrated-injection logic (I^2L) was added to the bipolar process. This process allowed reasonably dense low voltage logic to be included on

The I²L process was particularly useful in manufacturing ADCs, because only a single additional diffusion step was required beyond those used in the standard linear process. Furthermore, this diffusion did not significantly interfere with the other steps in the process, so the analog circuitry was relatively unaffected by the addition of the logic.

Probably the most significant SAR ADC ever introduced was the 12-bit, 35- μ s AD574 in 1978. The AD574 represents a complete solution, including buried Zener reference, timing circuits, and three-state output buffers for direct interfacing to an 8-, 12-, or 16-bit microprocessor bus. In its introductory form, the AD574 was manufactured using compound monolithic construction, based on two chips—one an AD565 12-bit current-output DAC, including reference and thin film scaling resistors; the other containing the successive approximation register (SAR) and microprocessor interface logic functions as well as a precision latching comparator. The AD574 soon emerged as the industry-standard 12-bit ADC in the early 1980s. In 1985, the device became available in single-chip monolithic form for the first time—thereby making low-cost commercial plastic packaging possible. A simplified block diagram of the AD574 is shown in Figure 14.

[illegible]

the AM6688 4-bit, 100-Ms/s flash ADC, designed by Jim Giles, who had previously designed the AM685 and AM687 fast ECL comparators.

Although a few more instrument-type rack-mounted data converters were developed in the early 1970s (such as the VHS-series and 7000-series from Computer Labs, Inc.), the demand for lower cost, more compact high performance data converters led manufacturers to turn toward hybrid and modular techniques—as the monolithic technology of the period was not yet capable of supporting the high-end converter functions in single-chip form. Hybrid and modular data converter designers of the 1970s had a virtual smorgasbord of components from which to choose, including IC op-amps, IC DACs, comparators, discrete transistors, various logic chips, etc.

film conductors. Individual die are bonded to the substrate (usually with epoxy), and wire bonds make the connections between the bond pads and the conductors. The hybrid is usually hermetically sealed in some sort of ceramic or metal package. Accuracy was achieved by trimming thick or thin film resistors after assembly and interconnection, but before sealing. Manufacturers used thin film networks, discrete thin film resistors, deposited thick or thin film resistors, or some combination of the above.

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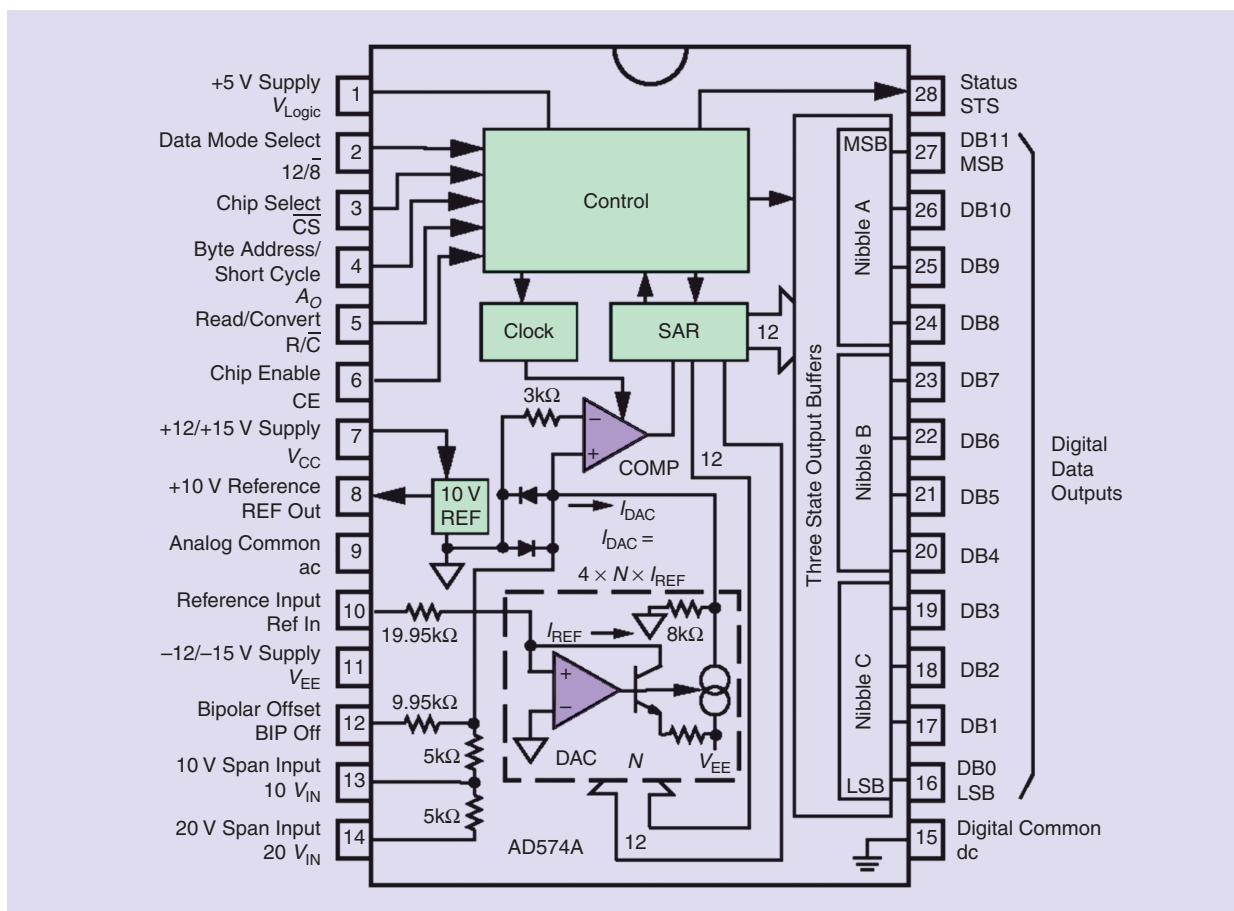


FIGURE 14: The industry-standard AD574 12-bit, 35- μ s IC ADC, 1978.

mid-1970s as a hybrid device consisting of 11 chips: three quad switch arrays, two op-amps, two resistor networks, a Zener diode, two clamp diodes, and a chip capacitor [see Figure 15(a)]. In 1978, when monolithic technology had progressed to the point where it was possible to combine the switch and resistor network into a single chip, a three-chip DAC80 was reintroduced as shown in Figure 15(b). The three chips in this design included a voltage reference, an output op-amp, and the switch/resistor/control-amplifier chip.

The newer design offered performance identical to that of the original DAC80 but with a tremendous improvement in reliability and at

a much lower cost. Then, in 1983, the first single-chip DAC80 became available [Figure 15(c)]. It, of course, provided further cost reduction and

reliability improvement, compared to the three- and 11-chip versions. Finally, in 1984, this popular device was offered in a low-cost plastic DIP package. Thus, in approximately ten years the DAC80 evolved from a relatively high-cost hybrid to a high-volume commodity IC.

Another excellent example of hybrid technology was the AD572 12-bit, 25- μ s SAR ADC introduced in 1977. The AD572 was the first military-approved 12-bit ADC processed to MIL-STD-883B and specified over the full operating temperature range of -55°C to $+125^{\circ}\text{C}$.

It should be noted at this point that none of the monolithic or hybrid ADCs of the 1970s were sampling

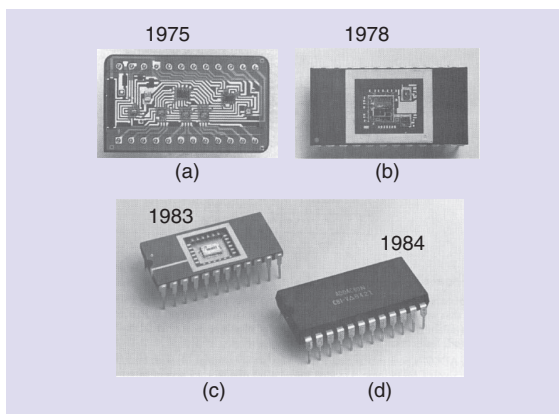


FIGURE 15: DAC80 12-bit DAC evolution from hybrid to monolithic: (a) an early industry-standard version with 11 chips, (b) a three-chip version, (c) a single-chip ceramic package, and (d) a single-chip plastic package.

ADCs with internal sample-and-hold amplifiers (SHAs). To process ac signals, a separate SHA had to be connected to the ADC (with the appropriate interface and timing circuits). This generated the need for hybrid SHAs, such as the HTC-0300 and the faster HTS-0025.

Modular ADCs and DACs of the 1970s

Designers of modular data converters in the 1970s had even more flexibility than hybrid designers. In fact, modular technology began in the late 1960s before hybrids became popular, and it still exists to this day for certain products (the modern three-letter acronym SiP is for “Silicon in Package”). Figure 16 shows two of the early popular modular ADCs: the ADC-12QZ and the MAS-1202. The modular technology was quite straightforward—components were mounted on a small printed circuit board and encapsulated in a potted module after trimming (usually done with manually selected resistors). The potting compound served to distribute the heat throughout the module, provided some degree of thermal tracking between critical components, and made it somewhat more difficult for competitors to reverse engineer the circuits.

The ADC-12QZ 12-bit, 40- μ s SAR ADC was introduced by Analog Devices in 1972, an outgrowth of Pastoriza Electronics’s early converter product line acquired in 1969. The ADC-12QZ utilized a DAC made up of three quad-switch building blocks previously discussed and a matching pre-trimmed thin film resistor network. A SAR logic chip, a comparator, a reference, and miscellaneous other components completed the parts list. The MAS-1202 12-bit, 2- μ s SAR ADC designed at Computer Labs, Inc., was released in 1975 and utilized an internal DAC based on fast PNP transistor switches and manually-selected precision resistors. The ADC-12QZ and the MAS-1202 each dissipated approximately 2 W and commanded

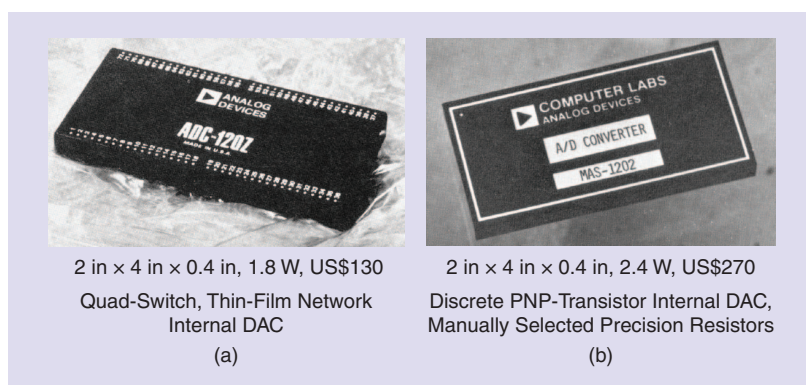


FIGURE 16: Early modular ADCs of the 1970s: (a) the ADC-12QZ general-purpose 12-bit, 40- μ s SAR ADC introduced in 1972 and (b) the MAS-1202 12-bit, 2- μ s SAR ADC introduced in 1975.

premium prices of US\$130 and US\$270, respectively.

One of the first modular ADCs of the 1970s to include the sample-and-hold function—required for processing transient or varying signals—utilized an open-card construction with a combination of hybrid, IC, and discrete building blocks. The MOD-815 8-bit, 15-Ms/s ADC was introduced by Computer Labs in 1976. The design utilized two 4-bit flash converters in a subranging architecture. Each 4-bit flash converter was constructed of eight dual AM687 ECL comparators. The MOD-815 was one of the first commercial ADCs used in the rapidly emerging field of digital television.

Other popular card-level modules included the MOD-1205 12-bit, 5-Ms/s ADC and the MOD-1020 10-bit, 20-Ms/s

ADC introduced by Analog Devices/Computer Labs in 1979. The MOD-1205 was widely used in defense applications, and the MOD-1020 was an enabling technology for the first ultrasound systems.

These products made use of the first flash converters on the market: the Advanced Micro Devices’ AM6688 4-bit, 100-Ms/s flash and the TRW TDC-1007J (8-bit) and TDC-1014J (6-bit) flash converters. Figure 17 shows a photo of the MOD-1020 with the key devices labeled. The architecture was sub-ranging, with two “stacked” AM6688s providing the first 5-bit conversion, and the 6-bit TDC-1014J the second 6-bit conversion. The extra bit was used for error correction. The MOD-1020 utilized quite a bit of ECL logic

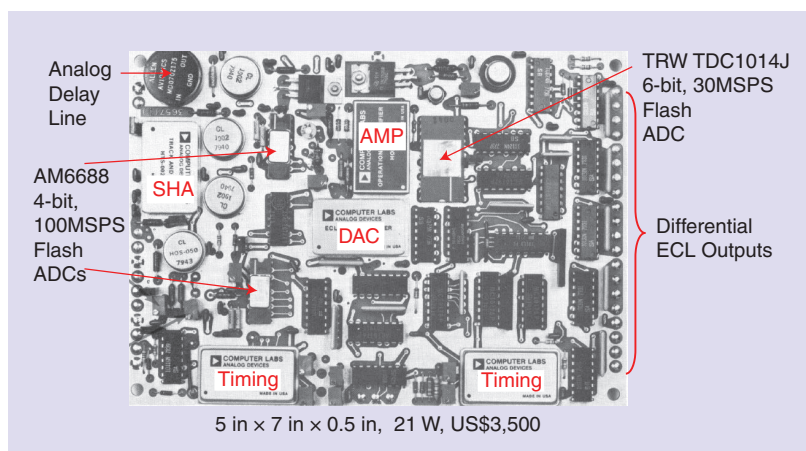


FIGURE 17: The MOD-1020 10-bit, 20-Ms/s sampling ADC introduced in 1979.

and dissipated a total of 21 W. Due to the high level of performance and the large number of costly hybrid and IC building blocks, the MOD-1020 commanded a premium price of US\$3,500.

Data Converters of the 1980s

The 1980s represented high growth years for both IC, hybrid, and modular data converters. The driving market forces were instrumentation, data acquisition, medical imaging, professional and consumer audio/video, computer graphics, and a host of others. The increased availability of

18-bit ADCs and DACs, and the emergence of the compact disk (CD) player fueled the need for low-cost audio DACs.

In the 1980s, general purpose ADCs and DACs began to offer more resolution, more functionality, and more complete solutions to the problems of data acquisition and distribution, including multichannel ADCs and DACs. The development of linear-compatible CMOS processes (such as Analog Devices's LC²MOS and BiCMOS II in the mid-1980s) allowed data converter designers to provide more functionality by the

with the 14-bit TDA1540 fabricated on a bipolar process [88], [89] and the 16-bit TDA1541 [90].

Phillips later developed a 16-bit self-calibrating CMOS audio DAC in the late 1980s [91].

Monolithic ADCs of the 1980s

The two-chip AD574, introduced in 1978, was well on its way to becoming an industry standard converter by the time of the introduction of the single-chip AD574 12-bit, 35- μ s SAR ADC in 1985. Since that time, this converter did become an industry standard, and is still in production today.

It is interesting to note the emergence of the *sampling* monolithic ADC starting in the mid-1980s. The addition of sample-and-holds, references, and buffer amplifiers was made considerably easier with the addition of bipolar capability to the CMOS process (LC²MOS and BiCMOS). Another trend which emerged was the addition of front-end multiplexers to the basic ADC, as in the case of the 4-channel AD7582 in 1984, thereby providing a more complete data acquisition solution.

While most precision ADCs of the 1970s utilized thin film resistors and bipolar processes, the ground breaking work of J. L. McCreary and Paul R. Gray at Berkeley [92] paved the way for charge redistribution (switched capacitor) techniques that would dominate CMOS converters of the 1980s.

The first pipelined CMOS ADC was described by S. Masuda, et. al, in a 1984 paper at the Custom Integrated Circuits conference [93].

Although the basic $\Sigma\Delta$ ADC architecture had been well known since the 1950s and 1960s, the first actual commercial offering of a monolithic $\Sigma\Delta$ ADC was in 1988 by Crystal Semiconductor (CSZ5316). The device had 16-bit resolution and an effective throughput rate of 20 kS/s, making it suitable for voice-band digitization. The digital audio market (both professional and consumer) generated a demand for

Pulse code modulation was first disclosed in a relatively obscure patent issued to Paul M. Rainey of Western Electric in 1921.

relatively low-cost microprocessors, high-speed memory, and DSPs and the emergence of the IBM-compatible PC increased the interest in all areas of signal processing. The emphasis in ADCs began to rapidly shift to include ac performance and wide dynamic range—hence, a great demand for ADCs with an internal sample-and-hold function. Specifications such as signal-to-noise ratio (SNR), signal-to-noise and distortion (SINAD), effective number of bits (ENOB), noise power ratio (NPR), spurious free dynamic range (SFDR), aperture time jitter, etc. began to appear on most ADC data sheets; and glitch impulse area, SFDR, etc., on DAC data sheets.

There was a proliferation of high-speed bipolar and CMOS flash ADCs in the 1980s, with 4-, 6-, 8-, 9-, and 10-bit at sampling rates from 20 Ms/s to 100 Ms/s. Digital video was a chief driving force for the 8-, 9-, and 10-bit devices. In the graphics display area, high-speed video RAM-DACs emerged, with CMOS being the ideal process for these memory-intensive devices.

Voiceband and audio signal processing led to the demand for 16- and

addition of features such as on-chip voltage references and buffer amplifiers, for example.

Another important process development in the mid-1980s was the introduction of Analog Devices's first-generation complementary bipolar (CB) process, which offered high-speed, high-performance matching PNP and NPN transistors. The high-speed op-amps produced in the CB process made excellent drivers for many of the new ADCs, and the CB process eventually yielded some extremely high performance intermediate frequency (IF)-sampling ADCs in the 1990s.

Monolithic DACs of the 1980s

In the 1980s CMOS emerged as the preferred technology for general purpose DACs. The addition of microprocessor-compatible interfaces, multiple DACs in a package, and voltage and current output capability represented some of the trends. Special DACs were developed for popular consumer applications such as digital video and digital audio products.

Phillips was one of the early manufacturers of audio DACs, beginning

$\Sigma\Delta$ ADCs with higher throughput rates and greater resolution; and the precision measurement market required 20+ bit resolution, although at much lower throughput rates. Both these needs would be addressed during the 1990s by an explosion of ADCs and DACs using the $\Sigma\Delta$ architecture.

Monolithic Flash and Folding ADCs of the 1980s

As previously mentioned, the rapidly growing digital video market, coupled with the introduction of the TRW TDC-1007J 8-bit, 30-Ms/s flash ADC in 1979, spurred many IC manufacturers to develop similar, but lower powered flash ADCs with resolutions ranging from 4 to 10 bits, and sampling rates as high as high as 500 Ms/s. The peak years for flash converters were approximately 1979 to 1990.

Both bipolar and CMOS technology was used to produce these devices, with the CMOS converters offering lower power, but at the expense of somewhat inferior performance—especially in the early offerings. The chief problem with the early CMOS flash converters were error codes known as “sparkle codes” produced by comparator metastability (the inability of the comparator output to reach a valid logic level with small overdrive). The bipolar process comparator designs were less susceptible because they typically had much higher regenerative gain. Today, metastability problems still exist in ADCs, although they have been minimized in pipelined CMOS devices designed on submicron processes. In most frequency domain applications, an occasional random error code is not troublesome, but in time domain applications such as digital oscilloscopes, for example, error codes can be misinterpreted as “runt” errors when monitoring a circuit for random logic errors. Special care must be taken in both the ADC design and testing for these sensitive applications.

Although bipolar and CMOS flash converter designs were used in many of the 6- to 10-bit video ADCs of the 1980s, they were costly, relatively high power, and somewhat difficult to drive because of the large input capacitance of the parallel comparator bank.

To reduce power and cost, Rudy van de Plassche of Phillips developed a sub-ranging architecture that used double folding stages rather than flash stages to accomplish the conversion [94], [95]. This technique led to the release of the 8-bit, 40-Ms/s TDA8703 in the late 1980s.

The advancements in electrical science during the late 1800s ushered in the age of electronic communication, and this is where true data conversion had its beginnings.

Hybrid and Modular DACs and ADCs of the 1980s

The demand for hybrid and modular DACs and ADCs peaked in the 1980s, primarily because of the three- to five-year lead time hybrids and modules held compared to single-chip monolithic converters with equivalent performance. In addition, the large number of flash converters and other components served as building blocks for higher resolution sub-ranging ADCs.

An interesting thick film hybrid family, introduced by Analog Devices in 1980, was the HDG-series 4-, 6-, and 8-bit video ECL DACs. Designed for raster scan red-green-blue (RGB) graphics displays, these DACs had an 8-bit settling time of approximately 5 ns. In addition to fast settling, these were among the first video DACs to allow the *sync*, *blanking*, *10% white*, and *reference white* levels to be set with separate internal switches. This allowed the full 8-bit DAC range to be dedicated to the *active video* region. The HDG-series was a precursor to the fully monolithic CMOS video DACs and RAM-DACs which were introduced later in the 1980s.

High performance hybrid sub-ranging ADCs also appeared during the 1980s, most utilizing high speed flash converters as internal building blocks. Most were *sampling* devices (implying an internal sample-and-hold function), complete with ac specifications.

Data Converters of the 1990s

The markets influencing data converters in the 1990s were even more diverse and demanding than those of the 1980s. Some of the major applications were industrial process control, measurement, instrumentation,

medical imaging, audio, video, and computer graphics. In addition, communications became an even bigger driving force for low-cost, low-power, high-performance data converters in modems, cell phone handsets, and wireless infrastructures (base stations).

Other trends were the emphases on lower power and single-supply voltages for portable battery-powered applications. While the reduced supply voltages were compatible with the higher speed, lower voltage processes, the reduced signal range and headroom made the converter designs more sensitive to noise. Packaging trends also changed in the 1990s from the traditional dual in-line package to smaller surface mount packages suitable for high-volume automatic mass-assembly manufacturing techniques. These included both leaded types and non-leaded types such as ball grid array and chip-scale packages.

Even in the general purpose data converter market, there was a demand for more analog and digital functionality, such as putting an entire data acquisition system on a chip including the input multiplexer, programmable gain

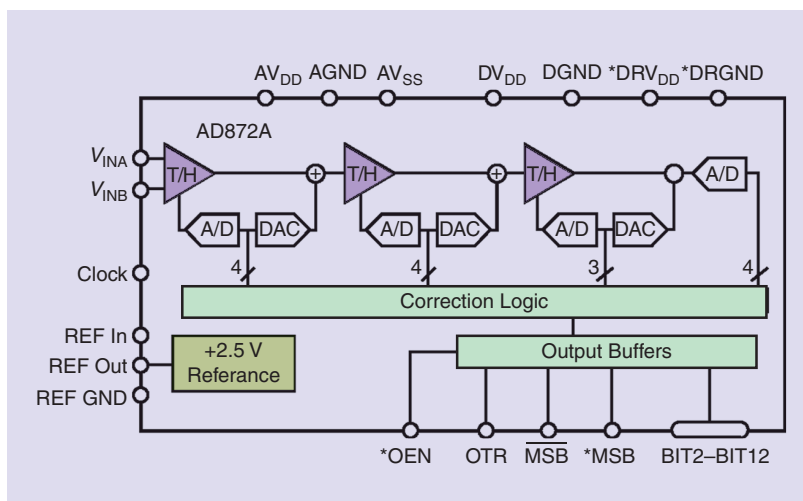


FIGURE 18: A schematic for an AD872 12-bit, 10-Ms/s BiCMOS sampling ADC, 1992.

amplifier (PGA), sample-and-hold, and the ADC function. Many applications required both the ADC and DAC function; and this led to the integration of both on a single chip, called a coder-decoder, or CODEC. Specially designed analog front ends and mixed-signal front ends were included with the basic ADC function in applications such as charge-couple device image processors and IF-sampling receivers.

In the TxDAC family, digital functions such as interpolation filters and digital modulators were integrated with a high-speed, low-distortion CMOS DAC core. Data converter designers made more use of “core” designs to yield several products with various options, such as serial or parallel output parts, etc. The TxDAC-series is a good illustration of the application of this concept, where a variety of resolutions, update rates, and internal digital processing are offered across a broad number of individual products, all of which use essentially the same DAC core.

Because of the increase in frequency-domain signal processing applications, there was even greater emphasis on dynamic range and ac performance in practically all data converters, and a large number of monolithic *sampling* ADCs were introduced to meet the demand. The pipelined sub-ranging architecture

virtually replaced the higher power flash ADCs of the 1980s, where some of the key ac specifications were SNR, SINAD, ENOB, and SFDR.

In the 1990s, CMOS became the process-of-choice for general-purpose data converters, with BiCMOS reserved for the high-end devices. In a few cases, high-speed complementary bipolar processes were utilized for ultra high performance data converters. CMOS is also the ideal process for the sigma-delta architecture, which became the topology of choice for ADCs and DACs used in voiceband and audio applications, as well as in higher resolution, low-frequency measurement converters.

A major process technology shift occurred in the 1990s, when parasitics ultimately became the performance-limiting factor for high-speed chip-and-wire hybrid data converters. The newer ICs, with their smaller feature size and reduced parasitics, allowed them to achieve higher levels of performance than attainable in a chip-and-wire hybrid or a module—a reversal of the situation that existed throughout the 1970s and most of the 1980s.

Monolithic DACs of the 1990s

A significant trend in general purpose DACs of the 1990s was toward more functionality in all areas, especially with respect to the input structure. DACs were designed

specifically to handle parallel, serial, and byte-wide loading, and the inputs were generally double-buffered. The serial interface became popular for interfacing to microprocessors and DSPs. In many cases, the same core DAC design was utilized to provide these various options as separate products in the appropriate packages. Obviously, this required the introduction of many individual DAC products to cover all the desired options.

A variety of options existed with respect to the output structure also. Audio and video DACs tended to use current outputs, while some of the more general-purpose DACs offered either current or voltage output options.

Consumer audio CD players spurred the market for low-distortion 16+ bit DACs in the late 1980s, and the first audio DACs were parallel linear DACs capable of oversampling at rates of eight or 16 times the basic CD update rate of 44.1 kS/s. Resolutions ranged from 16 bits with the early audio DACs to 18 and 20 bits with later versions.

By the mid-1990s, the sigma-delta architecture began to replace the parallel DACs in audio applications. Sigma-delta offered much higher oversampling ratios, thereby relaxing output filter requirements, and also provided higher dynamic range with lower distortion.

In the video DAC arena, CMOS continued as the process of choice, and many were triple DACs with RGB lookup tables, such as the 8-bit, 80-Ms/s ADV471/ADV478. Later, higher resolution 10-bit video DACs such as the 10-bit, 80-Ms/s ADV7121/ADV7122 became available. The Philips TDA8775 10-bit, 50-Ms/s CMOS video DAC, introduced in the mid-1990s [96], was used in the popular Sony PlayStation 1.

The *digital potentiometer*, another highly popular component today, had its origins in 1989 with the release of the AD8800 TrimDAC, the first in a series. The digital potentiometers were basically 8-bit voltage-output DACs designed and optimized to

replace mechanical potentiometers. The basic concept behind the digital pot was simply to use a CMOS “string DAC” as a variable resistor. The offerings expanded to include some with non-volatile memory.

Monolithic ADCs of the 1990s

During the decade of the 1990s, monolithic ADC performance overtook that of modular and hybrid converters, primarily because of the greatly reduced parasitics in the new IC processes.

Progress was also being made in CMOS sampling ADCs, such as the AD872 12-bit, 10-Ms/s sampling ADC introduced in 1992. This ADC used the pipelined architecture with digital error correction shown in Figure 18.

The pipelined architecture was crystallized in a number of ground-breaking papers by Stephen H. Lewis over the period from 1987 to 1992 [97]–[100].

A true breakthrough in wide dynamic range IF-sampling ADCs occurred in 1995 with the release of the 12-bit, 41-Ms/s AD9042 [101]. A functional diagram of the AD9042 is shown in Figure 19. This converter was the first to achieve greater

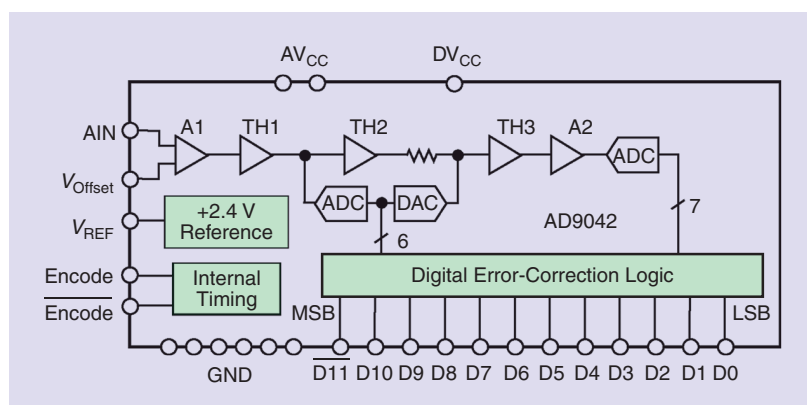


FIGURE 19: A schematic for an AD9042 12-bit, 41-Ms/s XFCB sampling ADC, 1995.

than 80-dB SFDR for signals over a 20-MHz Nyquist bandwidth. It was fabricated on the Analog Devices's XFCB high-speed complementary bipolar process.

A significant technology change occurred in the 1990s, when the high-power 8-, 9-, and 10-bit flash converters of the 1980s were gradually replaced by lower power pipelined architectures.

Switched capacitor techniques replaced thin film resistors for the internal DACs within SAR ADCs, and self-calibration techniques emerged

based on the work of H.S. Lee that replaced expensive laser trimming [102], [103].

CMOS sigma-delta ADCs became the architecture of choice for measurement, voiceband, and audio ADCs beginning in the early 1990s. These converters include on-chip multiplexers and PGAs and are designed for direct interfacing to many sensors, such as thermocouples, bridges, resistance temperature detectors, etc. A significant product in the family is the AD7730, introduced in 1997, which allows a

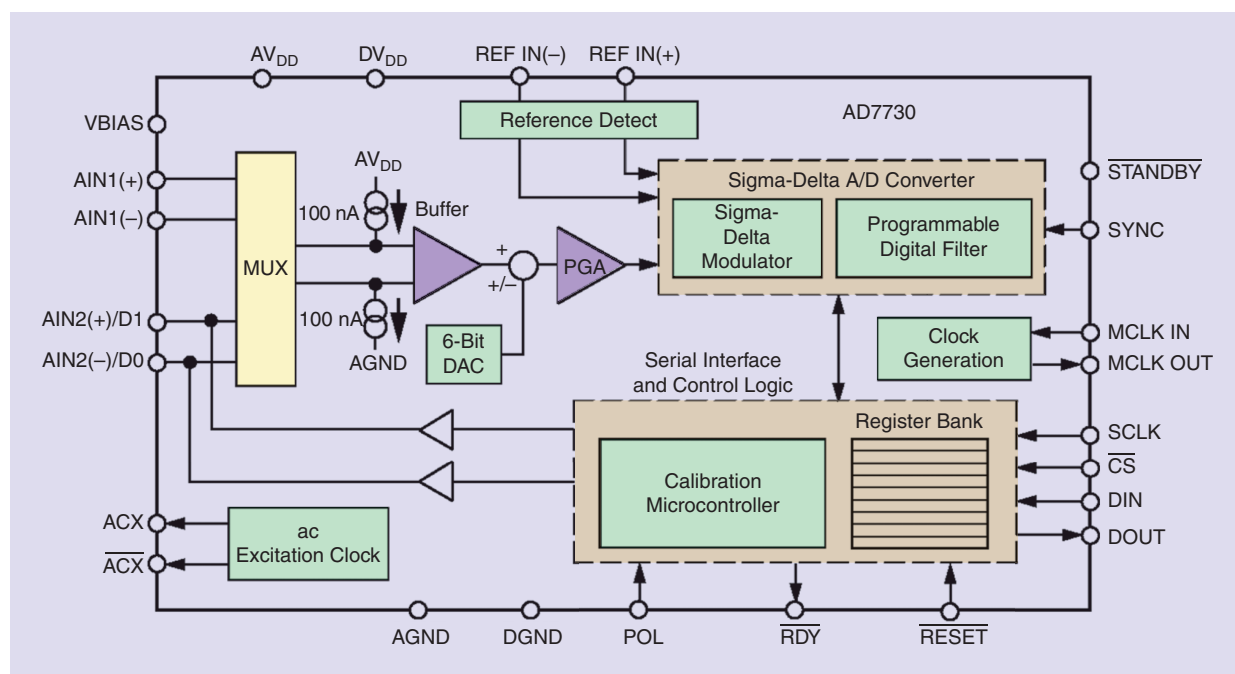


FIGURE 20: A schematic for an AD7730 24-bit signal-conditioning $\Sigma\Delta$ ADC, 1997.

load cell output with a 10-mV full-scale voltage to be digitized to over 80,000 noise-free codes (16.5 bits). A simplified block diagram of the AD7730 is shown in Figure 20.

Although certain versions of early microcontrollers, such as the Intel 8048 series introduced in 1976 [104], included on-chip 8-bit SAR ADCs (8022), the resolution of the integrated ADCs was not sufficient for many industrial applications. During the 1980s, the on-chip ADC performance improved, and resolution increased to 10 bits.

One of the first attempts to integrate a microprocessor with a high performance ADC and DAC was Analog Devices's ADSP-21MSP50, a 16-bit audio codec with on-chip DSP. In 1999 the ADuC812 MicroConverter *precision analog microcontroller* was introduced. The MicroConverter includes not only precision signal conditioning circuitry (ADCs, DACs, multiplexers, voltage reference, temperature sensor, etc.) but also flash memory and an 8051-based microprocessor core. Later products include 16–24-bit sigma-delta ADCs and use more powerful cores, such as the ARM7 time division multiplexor and the ARM Cortex M3 and M4. This level of integration represents an optimum solution for many general-purpose sensor signal conditioning, smart sensor, and signal processing applications.

Summary

This article has traced converter history approximately to the end of the 20th century. We have seen the progression from early rack-mounted instruments to modules, hybrids, and ultimately ICs.

Modern converters make full use of the power and speed scaling qualities of CMOS to achieve higher levels of dc and ac performance, and the specifications on converters have become more standardized as well as the associated test methodology.

In the next article, Dave Robertson examines the continuation of data converter technology in the 21st

century as well as how applications drive converters and how data converter technology in turn influences system architecture.

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