ANALOG-DIGITAL CONVERSION

Walt Kester

Editor

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CHAPTER 1
DATA CONVERTER HISTORY

Walt Kester

Chapter Preface

This chapter was inspired by Walt Jung's treatment of op amp history in the first chapter of his book, *Op Amp Applications* (Reference 1). His writing on the subject contains references to hundreds of interesting articles, patents, etc., which taken as a whole, paints a fascinating picture of the development of the operational amplifier—from Harold Black's early feedback amplifier sketch to modern high performance IC op amps.

We have attempted to do the same for the history of data converters. In considering the scope of this effort—and the somewhat chaotic and fragmented development of data converters—we were faced with a difficult challenge in organizing the material. Rather than putting all the historical material in this single chapter, we have chosen to disperse some of it throughout the book. For instance, most of the historical material related to data converter architectures is included in Chapter 3 *(Data Converter Architectures)* along with the individual converter architectural descriptions. Likewise, Chapter 4 *(Data Converter Process Technology)* includes most of the key events related to data converter process technology. Chapter 5 *(Testing Data Converters)* touches on some of the key historical developments relating to data converter testing.

In an effort to make each chapter of this book stand on its own as much as possible, some of the historical material is repeated in several places—therefore, the reader should realize that this repetition is intentional and not the result of careless editing.

SECTION 1.1: EARLY HISTORY

It is difficult to determine exactly when the first data converter was made or what form it took. The earliest recorded binary DAC known to the authors of this book is not electronic at all, but hydraulic. Turkey, under the Ottoman Empire, had problems with its public water supply, and sophisticated systems were built to meter water. One of these is shown in Figure 1.1 and dates to the 18th Century. An example of an actual dam using this metering system was the Mahmud II dam built in the early 19th century near Istambul and described in Reference 2.

The metering system used reservoirs (labeled *header tank* in the diagrams) maintained at a constant depth (corresponding to the reference potential) by means of a spillway over which water *just* trickled (the criterion was sufficient flow to float a straw). This is illustrated in Figure 1.1A. The water output from the header tank is controlled by gated binary-weighted *nozzles* submerged 96 mm below the surface of the water. The output of the nozzles feeds an *output trough* as shown in Figure 1.1B. The nozzle sizes corresponded to flows of binary multiples and sub-multiples of the basic unit of 1 lüle (= 36 l/min or 52 m^3/day). An eight-lüle nozzle was known as a "sekizli lüle," a

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four lüle nozzle a "dörtlü lüle," a ¼ lüle nozzle a "kamuş," an eighth lüle a "masura," and a thirty-second lüle a "çuvaldiz." Details of the metering system using the binary weighted nozzles are shown in Figure 1.1C. This is functionally an 8-bit DAC with manual (rather than digital, no doubt) input and a wet output, and it may be the oldest DAC in the world. There are probably other examples of early data converters, but we will now turn our attention to those based on more familiar electronic techniques.

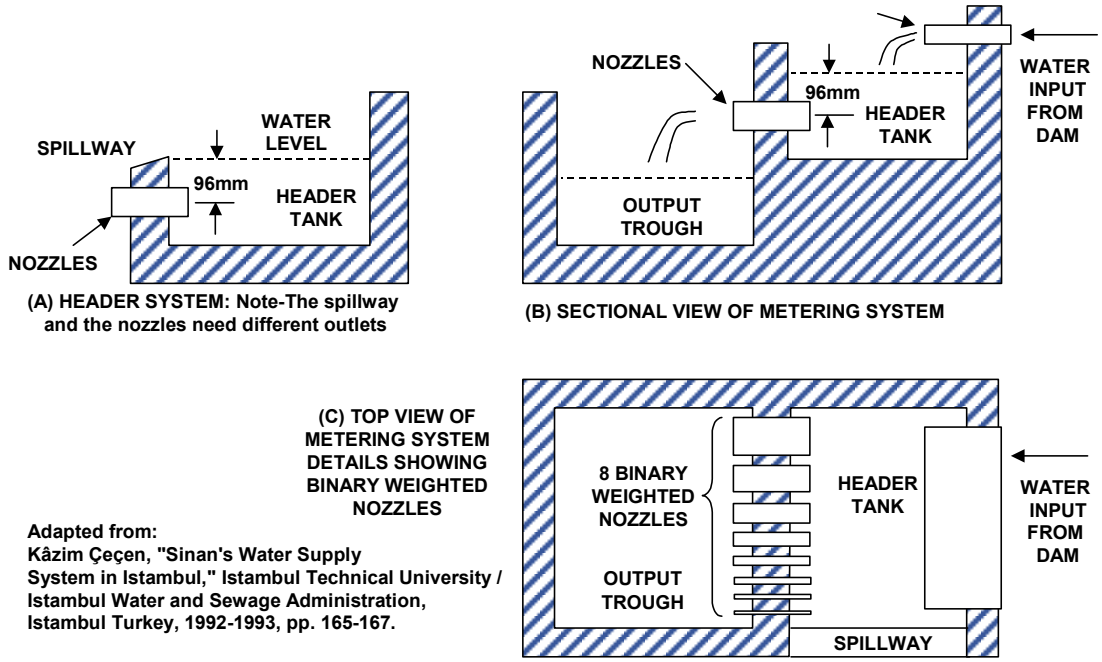


Figure 1.1: *Early 18th Century Binary Weighted Water Metering System*

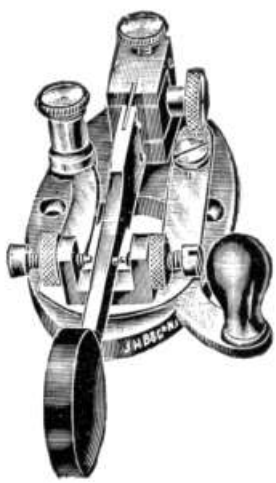
Probably the single largest driving force behind the development of electronic data converters over the years has been the field of communications. The telegraph led to the invention of the telephone, and the subsequent formation of the Bell System. The proliferation of the telegraph and telephone, and the rapid demand for more capacity, led to the need for multiplexing more than one channel onto a single pair of copper conductors. While time division multiplexing (TDM) achieved some measure of popularity, frequency division multiplexing (FDM) using various carrier-based systems was by far the most successful and widely used. It was pulse code modulation (PCM), however, that put data converters on the map, and understanding its evolution is where we begin.

The material in the following sections has been extracted from a number of sources, but K. W. Cattermole's classic 1969 book, *Principles of Pulse Code Modulation* (Reference 3), is by far the most outstanding source of historical material for both PCM and data converters. In addition to the historical material, the book has excellent tutorials on sampling theory, data converter architectures, and many other topics relating to the subject. An extensive bibliography cites the important publications and patents behind the major developments. In addition to Cattermole's book, the reader is also referred to an

excellent series of books published by the Bell System under the title of *A History of Engineering and Science in the Bell System* (References 4 through 8). These Bell System books are also excellent sources for background material on the entire field of communications.

The Early Years: Telegraph to Telephone

According to Cattermole (Reference 3), the earliest proposals for the electric telegraph date from about 1753, but most actual development occurred from about 1825-1875. Various ideas for binary and ternary numbers, codes of length varying inversely with probability of occurrence (Schilling, 1825), reflected-binary (Elisha Gray, 1878—now referred to as the *Gray* code), and chain codes (Baudot, 1882) were explored. With the expansion of telegraphy came the need for more capacity, and multiplexing more than one signal on a single pair of conductors. Figure 1.2 shows a typical telegraph key and some highlights of telegraph history.

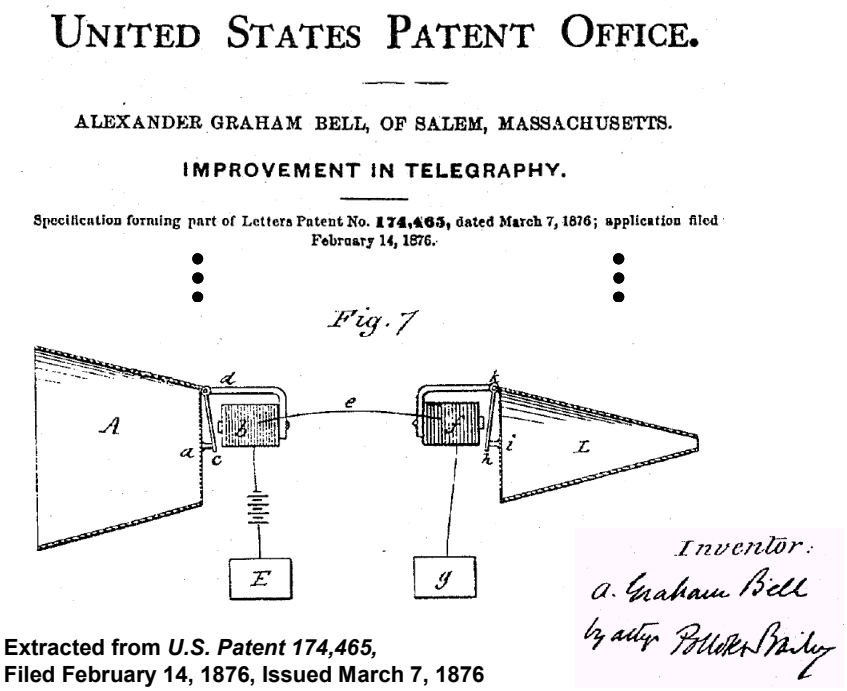


- **Telegraph proposals: Started 1753**
- **Major telegraph development: 1825 - 1875**
- **Various binary codes developed**
- **Experiments in multiplexing for increased channel capacity**
- **Telephone invented: 1875 by A. G. Bell while working on a telegraph multiplexing project**
- **Evolution:**
  - **Telegraph: Digital**
  - **Telephone: Analog**
  - **Frequency division multiplexing (FDM): Analog**
  - **Pulse code modulation (PCM): Back to Digital**

Figure 1.2: *The Telegraph*

The invention of the telephone in 1875 by Alexander Graham Bell (see References 9 and 10) was probably the most significant event in the entire history of communications. It is interesting to note, however, that Bell was actually experimenting with a telegraph multiplexing system (Bell called it the *harmonic* telegraph) when he recognized the possibility of transmitting the voice itself as an analog signal.

Figure 1.3 shows a diagram from Bell's original patent which puts forth his basic proposal for the telephone. Sound vibrations applied to the transmitter *A* cause the membrane *a* to vibrate. The vibration of *a* causes a vibration in the armature *c* which induces a current in the wire *e* via the electromagnet *b*. The current in *e* produces a corresponding fluctuation in the magnetic field of electromagnet *f*, thereby vibrating the receiver membrane *i*.



Extracted from *U.S. Patent 174,465,*
Filed February 14, 1876, Issued March 7, 1876

Figure 1.3: *The Telephone*

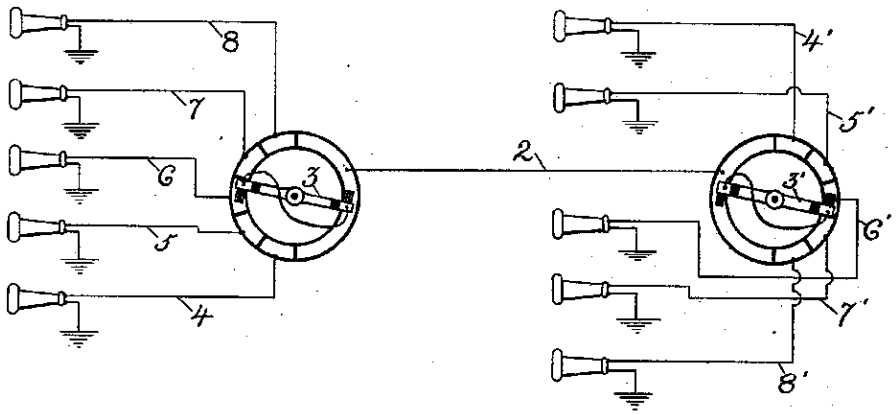
The proliferation of the telephone generated a huge need to increase channel capacity by multiplexing. It is interesting to note that studies of multiplexing with respect to telegraphy led to the beginnings of information theory. Time division multiplexing (TDM) for telegraph was conceived as early as 1853 by a little known American inventor, M. B. Farmer; and J. M. E. Baudot put it into practice in 1875 using rotating mechanical commutators as multiplexers.

In a 1903 patent (Reference 11), Willard M. Miner describes experiments using this type of electromechanical rotating commutator to multiplex several analog telephone conversations onto a single pair of wires as shown in Figure 1.4. Quoting from his patent, he determined that each channel must be sampled at

"... a frequency or rapidity approximating the frequency or average frequency of the finer or more complex vibrations which are characteristic of the voice or of articulate speech, ..., as high as 4320 closures per second, at which rate I find that the voice with all its original timbre and individuality may be successfully reproduced in the receiving instrument. ... I have also succeeded in getting what might be considered as commercial results by using rates of closure that, comparatively speaking, are as low as 3500 closures per second, this being practically the rate of the highest note which characterizes vowel sounds."

At higher sampling rates, Miner found no perceptible improvement in speech quality, probably because of other artifacts and errors in his rather crude system.

There was no follow-up to Miner's work on sampling and TDM, probably because there were no adequate electrical components available to make it practical. FDM was well established by the time adequate components did arrive.



Extracted from: Williard M. Miner, "Multiplex Telephony," *U.S. Patent 745,734,* Filed February 26, 1903, Issued December 1, 1903

Figure 1.4: *One of the Earliest References to a Criteria for Determining the Sampling Rate*

The Invention of PCM

Pulse code modulation was first disclosed in a relatively obscure patent issued to Paul M. Rainey of Western Electric in 1921 (Reference 12). The patent describes a method to transmit facsimile information in coded form over a telegraph line using 5-bit PCM. The figure from the patent is shown in Figure 1.5 (additional labels have been added for clarity).

Rainey proposed that a light beam be focused on the transparency of the material to be transmitted. A photocell is placed on the other side of the transparency to gather the light and produce a current proportional to the intensity of the light. This current drives a galvanometer which in turn moves another beam of light which activates one of 32 individual photocells, depending upon the amount of galvanometer deflection. Each individual photocell output activates a corresponding relay. The five relay outputs are connected in such a way as to generate the appropriate code corresponding to the photocell location. The digital code is thus generated from an "m-hot out of 32 code" , similar to modern flash converters. The output of this simple electo-optical-mechanical "flash" converter is then transmitted serially using a rotating electromechanical commutator, called a distributor.

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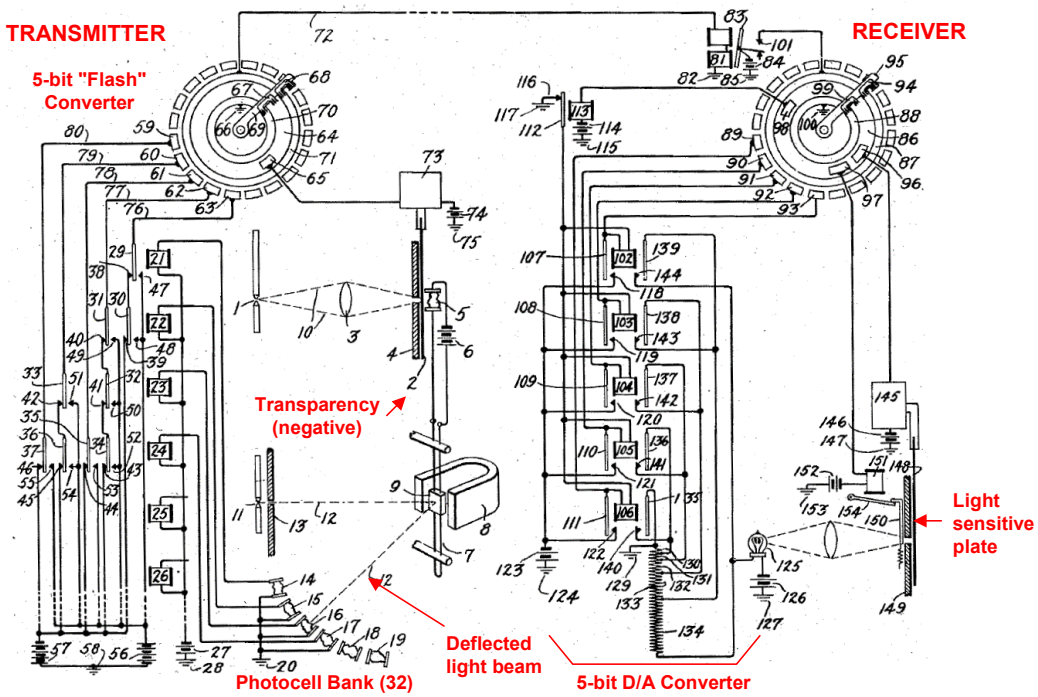

Figure 1.5: *The First Disclosure of PCM: Paul M. Rainey, "Facimile Telegraph System," U.S. Patent 1,608,527, Filed July 20, 1921,Issued November 30, 1926*

The serial data is transmitted, received, and converted into a parallel format using a second distributor and a bank of relays. The received code determines the combination of relays to be activated, and the relay outputs are connected across appropriate taps of a resistor which is in series with the receiving lamp. The current through the receiving lamp therefore changes depending upon the received code, thereby varying its intensity proportionally to the received code and performing the digital-to-analog conversion. The receiving lamp output is focused on a photographically sensitive receiving plate, thereby reproducing the original image in quantized form.

Rainey's patent illustrates several important concepts: quantization using a flash A/D converter, serial data transmission, and reconstruction of the quantized data using a D/A converter. These are the fundamentals of PCM. However, his invention aroused little interest at the time and was, in fact, forgotten by Bell System engineers. His patent was discovered years later after many other PCM patents had already been issued.

The Mathematical Foundations of PCM

In the mid-1920's, Harry Nyquist studied telegraph signaling with the objective of finding the maximum signaling rate that could be used over a channel with a given bandwidth. His results are summarized in two classic papers published in 1924 (Reference 13) and 1928 (Reference 14), respectively.

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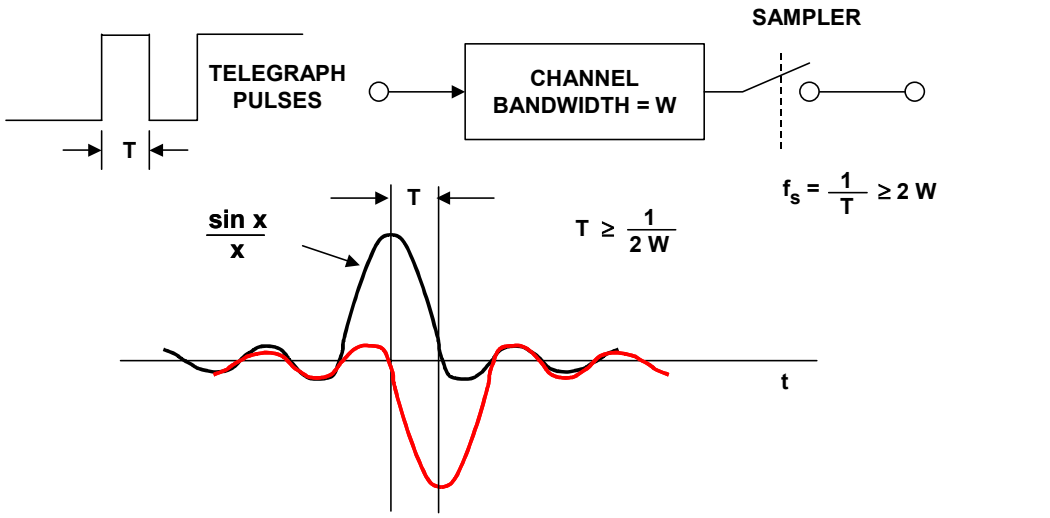
In his model of the telegraph system, he defined his signal as:

$$s(t) = \sum_k a_k f(t - kT). \qquad \text{Eq. 1.1}$$

In the equation, f(t) is the basic pulse shape, a_k is the amplitude of the kth pulse, and T is the time between pulses. DC telegraphy fits this model if f(t) is assumed to be a rectangular pulse of duration T, and a_k equal to 0 or 1. A simple model is shown in Figure 1.6. The signal is bandlimited to a frequency W by the transmission channel.



- Up to 2W pulses per second can be transmitted over a channel which has a bandwidth W.
- If a signal is sampled instantaneously at regular intervals at a rate at least twice the highest significant signal frequency, then the samples contain all the information in the original signal.

Figure 1.6: *Harry Nyquist's Classic Theorem: 1924*

His conclusion was that the pulse rate, 1/T, could not be increased beyond 2W pulses per second. Another way of stating this conclusion is *if a signal is sampled instantaneously at regular intervals at a rate at least twice the highest significant signal frequency, then the samples contain all the information in the original signal*. This is clear from Figure 1.6 if the filtered rectangular pulses are each represented by a sinx/x response. The sinx/x time domain impulse response of an ideal lowpass filter of bandwidth W has zeros at intervals of 1/2W. Therefore, if the output waveform is sampled at the points indicated in the diagram, there will be no interference from adjacent pulses, provided $T \geq 1/2W$ (or more commonly expressed as: $f_S \geq 2W$), and the amplitude of the individual pulses can be uniquely recovered.

Except for a somewhat general article by Hartley in 1928 (Reference 15), there were no significant additional publications on the specifics of sampling until 1948 in the classic papers by Shannon, Bennett, and Oliver (References 16-19) which solidified PCM theory for all time. A summary of the classic papers on PCM is shown in Figure 1.7.

- **Multiplexing experiments such as Williard Miner, "Multiplex Telephony," U.S. Patent 745,734, filed February 26, 1903, issued December 1, 1903.**
- **H. Nyquist, "Certain Factors Affecting Telegraph Speed," Bell System Technical Journal, Vol. 3, April 1924, pp. 324-346.**
- **H. Nyquist, Certain Topics in Telegraph Transmission Theory, A.I.E.E. Transactions, Vol. 47, April 1928, pp. 617-644.**
- **R.V.L. Hartley, "Transmission of Information," Bell System Technical Journal, Vol. 7, July 1928, pp. 535-563,.**

- **Note: Shannon's classic paper was written in 1948, well after the invention of PCM:**

- **C. E. Shannon, "A Mathematical Theory of Communication," Bell System Technical Journal, Vol. 27, July 1948, pp. 379-423, and October 1948, pp. 623-656.**
- **W. R. Bennett, "Spectra of Quantized Signals," Bell System Technical Journal, Vol 27, July 1948, pp. 446-471.**
- **B. M. Oliver, J. R. Pierce, C. E. Shannon, "The Philosophy of PCM," IRE Proceedings, Vol. 36, November 1948, pp. 1324-1331.**
- **W. R. Bennett, "Noise in PCM Systems," Bell Labs Record, Vol. 26, December 1948, pp. 495-499**

Figure 1.7: *Mathematical Basis of PCM*

The PCM Patents of Alec Harley Reeves

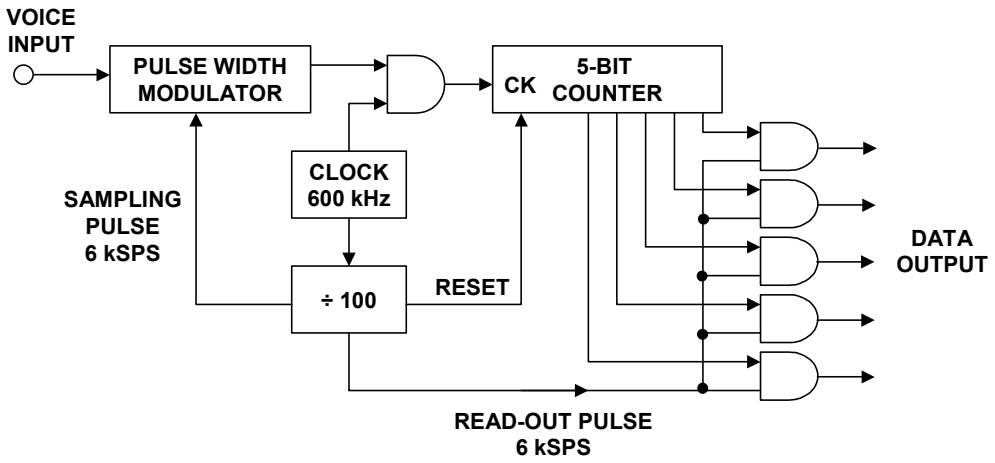
By 1937, frequency division multiplexing (FDM) based on vacuum tube technology was widely used in the telephone industry for long-haul routes. However, noise and distortion were the limiting factors in expanding the capacity of these systems. Although wider bandwidths were becoming available on microwave links, the additional noise and distortion made them difficult to adapt to FDM signals.

Alec Harley Reeves had studied analog-to-time conversion techniques using pulse time modulation (PTM) during the beginning of his career in the 1920's. In fact, he was one of the first to make use of counter chains to accurately define time bases using bistable multivibrators invented by Eccles and Jordan a few years earlier. In PTM, the amplitude of the pulses is constant, and the analog information is contained in the relative timing of the pulses. This technique gave better noise immunity than strictly analog transmission, but Reeves was shortly to invent a system that would completely revolutionize communications from that point forward.

It was therefore the need for a system with the noise immunity similar to the telegraph system that led to the (re-) invention of pulse code modulation (PCM) by Reeves at the Paris labs of the International Telephone and Telegraph Corporation in 1937. The very first PCM patent by Reeves was filed in France, but was immediately followed by similar patents in Britain and the United States, all listing Reeves as the inventor (Reference 20). These patents were very comprehensive and covered the far-reaching topics of (1) general principles of quantization and encoding, (2) the choice of resolution to suit the noise and bandwidth of the transmission medium, (3) transmission of signals in digital format serially, in parallel, and as modulated carriers, and (4) a counter-based design for

the required 5-bit ADCs and DACs. Unlike the previous PCM patent by Rainey in 1926, Reeves took full advantage of existing vacuum tube technology in his design.

The ADC and DAC developed by Reeves deserves some further discussion, since they represent one of the first all-electronic data converters on record. The ADC technique (see Figure 1.8) basically uses a sampling pulse to take a sample of the analog signal, set an R/S flip-flop, and simultaneously start a controlled ramp voltage. The ramp voltage is compared with the input, and when they are equal, a pulse is generated that resets the R/S flip-flop. The output of the flip-flop is a pulse whose width is proportional to the analog signal at the sampling instant. This pulse width modulated (PWM) pulse controls a gated oscillator, and the number of pulses out of the gated oscillator represents the quantized value of the analog signal. This pulse train can be easily converted to a binary word by driving a counter. In Reeves' system, a master clock of 600 kHz is used, and a 100:1 divider generates the 6-kHz sampling pulses. The system uses a 5-bit counter, and 31 counts (out of the 100 counts between sampling pulses) therefore represents a fullscale signal.



Adapted from: Alec Harley Reeves, "Electric Signaling System," *U.S. Patent 2,272,070*, Filed November 22, 1939, Issued February 3, 1942

Figure 1.8: *A. H. Reeves' 5-bit Counting ADC*

The DAC uses a similar counter and clock source as shown in Figure 1.9. The received binary code is first loaded into the counter, and the R/S flip-flop is reset. The counter is then allowed to count upward by applying the clock pulses. When the counter overflows and reaches 00000, the clock source is disconnected, and the R/S flip-flop is set. The number of pulses counted by the encoding counter is thus the complement of the incoming data word. The output of the R/S flip-flop is a PWM signal whose analog value is the complement of the input binary word. Reeves uses a simple lowpass filter to recover the analog signal from the PWM output. The phase inversion in the DAC is easily corrected in either the logic or in an amplifier further down the signal chain.

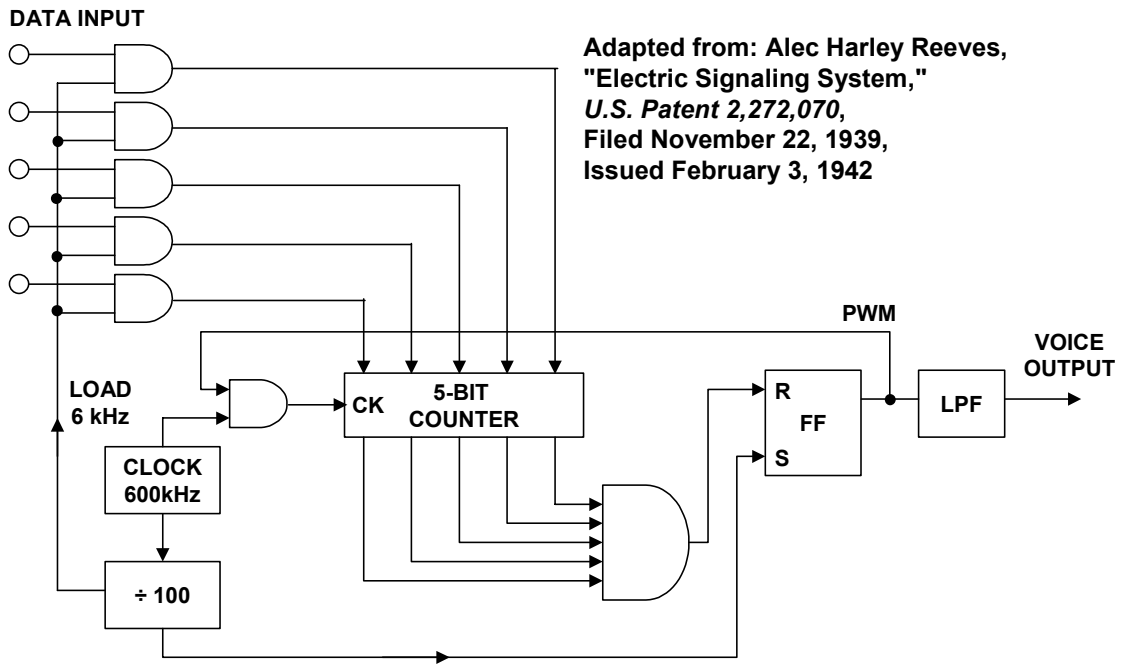


Figure 1.9: *A. H. Reeves' 5-bit Counting DAC*

Reeves' patents covered all the essentials of PCM: sampling, quantizing, and coding the digitized samples for serial, parallel, phase-modulated, and other transmission methods. On the receiving end, Reeves proposed a suitable decoder to reconstruct the original analog signal. In spite of the significance of his work, it is interesting to note that after the patent disclosures, Reeves shifted his attention to the shortwave transmission of speech using pulse-amplitude modulation, pulse-duration modulation, and pulse-position modulation, rather than pursuing PCM techniques.

PCM and the Bell System: World War II through 1948

Under a cross-licensing arrangement with International Telephone and Telegraph Corporation, Bell Telephone Laboratories' engineers reviewed Reeves' circuit descriptions and embarked upon their own pursuit of PCM technology. Starting in about 1940 and during World War II, studies were conducted on a speech secrecy system that made PCM techniques mandatory.

The highly secret "Project-X" to develop a speech secrecy system was started in 1940 by Bell Labs and is described in detail in Reference 6 (pp. 296-317). It used a complex technique based on vacuum tube technology that made use of the previously developed "vocoder," PCM techniques, and a unique data scrambling technique utilizing a phonograph recording containing the electronic "key" to the code. This system was designed at Bell Labs and put into production by Western Electric in late 1942. By April, 1943, several terminals were completed and installed in Washington, London, and North Africa. Shortly thereafter, additional terminals were installed in Paris, Hawaii, Australia, and the Philippines.

By the end of the war, several groups at Bell Labs were studying PCM; however most of the wartime results were not published until several years later because of secrecy issues. The work of H. S. Black, J. O. Edson, and W. M. Goodall were published in 1947-1948. (References 21, 22, and 23). Their emphasis was on speech encryption systems based on PCM techniques, and many significant developments came out of their work. A PCM system which digitized the entire voice band to 5-bits, sampling at 8 kSPS using a successive approximation ADC was described by Edson and Black (Reference 21 and 22). W. M. Goodall described an experimental PCM system in his classic paper based on similar techniques (Reference 23).

Some of the significant developments which came out of this work were the successive approximation ADC, the electron beam coding tube, the Shannon-Rack decoder, the logarithmic spacing of quantization levels (companding), and the practical demonstrations that PCM was feasible. The results were nicely summarized in a 1948 article by L. A. Meacham and E. Peterson describing an experimental 24-channel PCM system (Reference 24). A summary of PCM work done at Bell Labs through 1948 is shown in Figure 1.10.

- **"Project-X" voice secrecy system using PCM, 1940-1943.**
- **5-bit, 8kSPS successive approximation ADC**
- **Logarithmic quantization of speech (companding)**
- **Electron beam coding tube, 7-bit, 100kSPS**
- **"Shannon-Rack" decoder (DAC)**
- **Successful demonstration of experimental PCM terminals**
- **Theoretical PCM work expanded and published by Shannon**

- **Germanium transistor invented: 1947**

Figure 1.10: *Bell Laboratories' PCM Work: World War II through 1948.*

A significant development in ADC technology during the period was the electron beam coding tube shown in Figure 1.11. The tube described by R. W. Sears in Reference 25 was capable of sampling at 96 kSPS with 7-bit resolution. The basic electron beam coder concepts are shown in Figure 1.11 for a 4-bit device. The early tubes operated in the serial mode (Figure 1.11A). The analog signal is first passed through a sample-and-hold, and during the "hold" interval, the beam is swept horizontally across the tube. The Y-deflection for a single sweep therefore corresponds to the value of the analog signal from the sample-and-hold. The shadow mask is coded to produce the proper binary code, depending on the vertical deflection. The code is registered by the collector, and the bits are generated in serial format. Later tubes used a fan-shaped beam (shown in Figure 1.11B), creating the first electronic "flash" converter delivering a parallel output word.

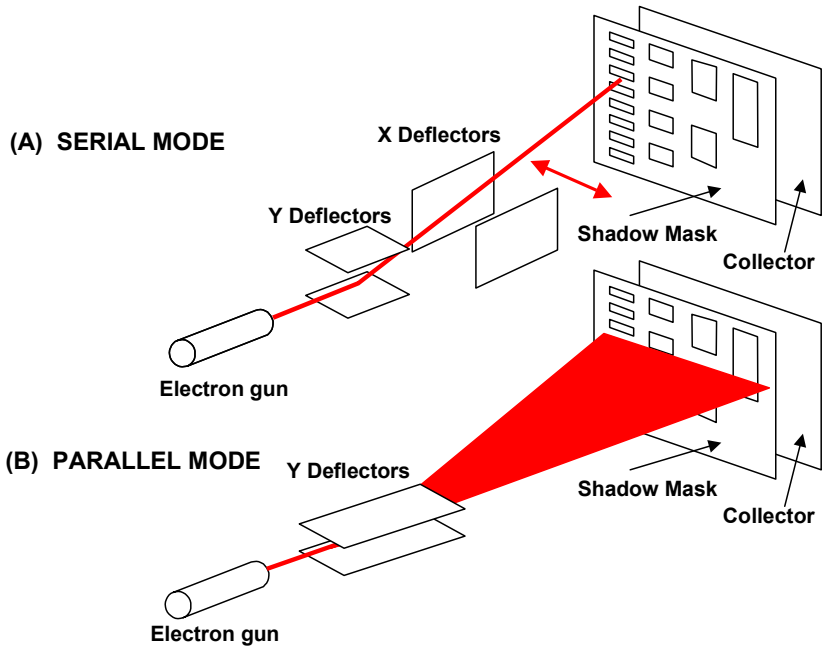


Figure 1.11: *The Electron Beam Coder*

Early electron tube coders used a binary-coded shadow mask, and large errors could occur if the beam straddled two adjacent codes and illuminated both of them. The way these errors occur is illustrated in Figure 1.12A, where the horizontal line represents the beam sweep at the midscale transition point (transition between code 0111 and code 1000). For example, an error in the most significant bit (MSB) produces an error of ½ scale. These errors were minimized by placing fine horizontal sensing wires across the boundaries of each of the quantization levels. If the beam initially fell on one of the wires, a small voltage was added to the vertical deflection voltage which moved the beam away from the transition region.

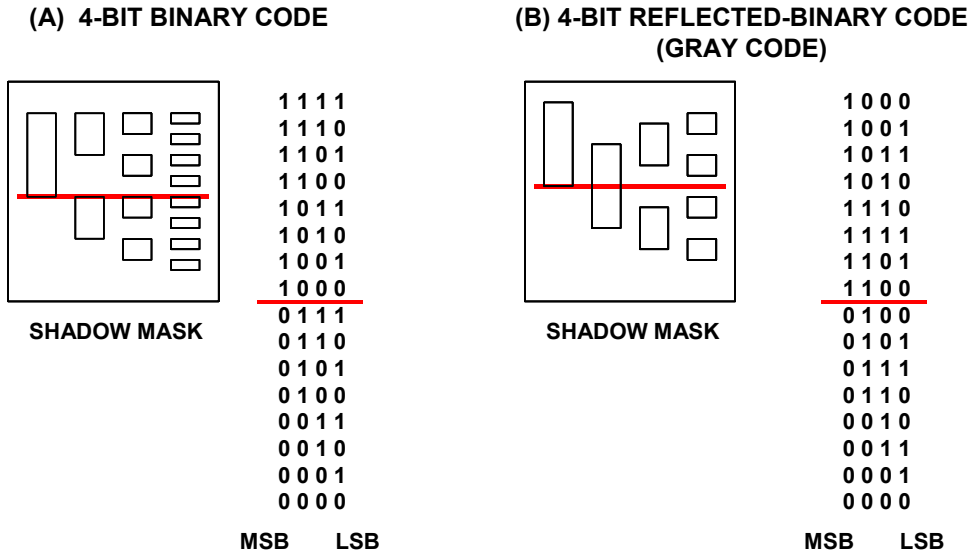


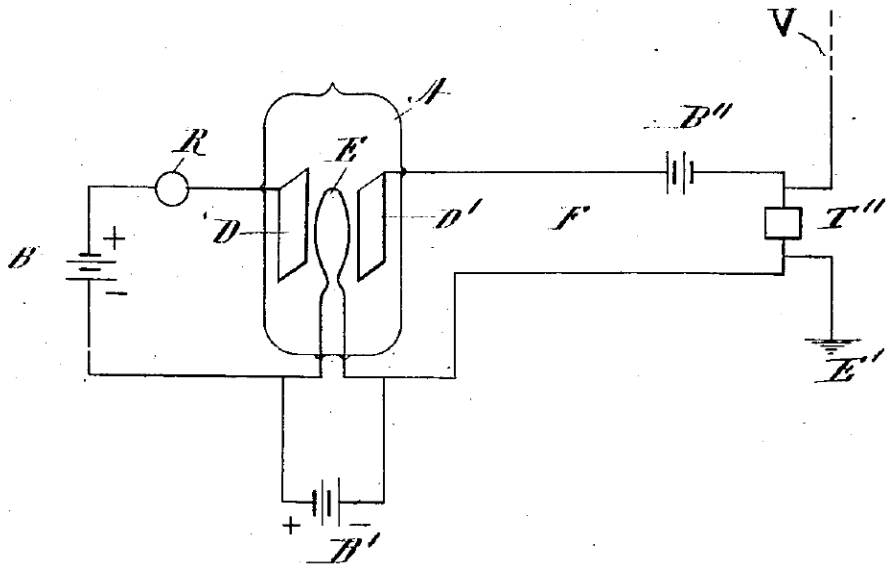
Figure 1.12: *Electron Beam Coder Shadow Masks for Binary and Gray Code*

The errors associated with binary shadow masks were eliminated by using a Gray code shadow mask as shown in Figure 1.12B. This code was originally called the "reflected binary" code, and was invented by Elisha Gray in 1878, and later re-invented by Frank Gray in 1949 (see Reference 26). The Gray code has the property that adjacent levels differ by only one digit in the corresponding Gray-coded word. Therefore, if there is an error in a bit decision for a particular level, the corresponding error after conversion to binary code is only one least significant bit (LSB). In the case of midscale, note that only the MSB changes. It is interesting to note that this same phenomenon can occur in modern comparator-based flash converters due to comparator metastability. With small overdrive, there is a finite probability that the output of a comparator will generate the wrong decision in its latched output, producing the same effect if straight binary decoding techniques are used. In many cases, Gray code, or "pseudo-Gray" codes are used to decode the comparator bank output before finally converting to a binary code output (refer to Chapter 3 for further architectural descriptions).

In spite of the many mechanical and electrical problems relating to beam alignment, electron tube coding technology reached its peak in the mid-l960s with an experimental 9-bit coder capable of 12-MSPS sampling rates (Reference 27). Shortly thereafter, however, advances in solid-state ADC techniques quickly made the electron tube converter technology obsolete.

Op Amps and Regenerative Repeaters: Vacuum Tubes to Solid-State

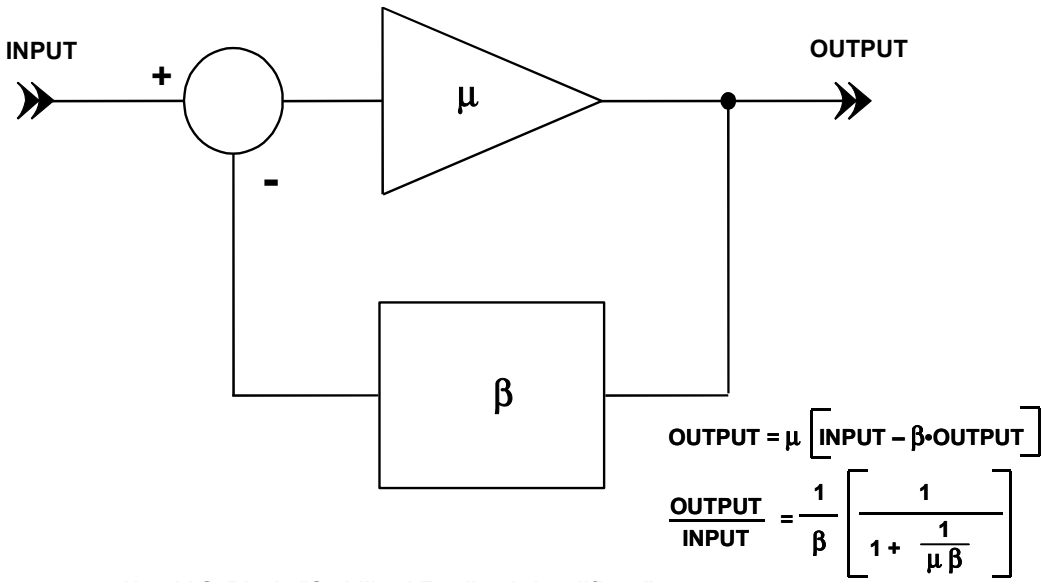
Except for early relatively inefficient electro-mechanical amplifiers (see Reference 5), electronic amplifier development started with the invention of the vacuum tube by Lee de Forest in 1906 (References 28 and 29). A figure from the original de Forest patent is shown in Figure 1.13.



Extracted from: Lee De Forest, "Device for Amplifying Feeble Electrical Currents," *U.S. Patent 841,387*, Filed October 25, 1906, Issued January 15, 1907

Figure 1.13: *The Invention of the Vacuum Tube: 1906*

By 1914, vacuum tube amplifiers had been introduced into the telephone plant. Amplifier development has always been critical to data converter development, starting with these early vacuum tube circuits. Key to the technology was the invention of the feedback amplifier by Harold S. Black in 1927 (References 30, 31, and 32). Amplifier circuit development continued throughout World War II, and many significant contributions came from Bell Labs. (The complete history of op amps is given in Reference 1). Figure 1.14 shows a drawing from a later article published by Black defining the feedback amplifier.



Harold S. Black, "Stabilized Feedback Amplifiers,"
Bell System Technical Journal, Vol. 13, No. 1, January 1934

Figure 1.14: *Harold Black's Feedback Amplifier of 1927*

The invention of the germanium transistor in 1947 (References 33, 34, and 35) was key to the development of PCM and all other electronic systems. In order for PCM to be practical, regenerative repeaters had to be placed periodically along the transmission lines. Vacuum tube repeaters had been somewhat successfully designed and used in the telegraph and voice network for a number of years prior to the development of the transistor, but suffered from obvious reliability problems. However, the solid state regenerative repeater designed by L. R. Wrathall in 1956 brought the PCM research phase to a dramatic conclusion (Reference 36). This repeater was demonstrated on an experimental cable system using repeater spacings of 2.3 miles on 19-gage cable, and 0.56 miles on 32-gauge cable. A schematic diagram of the repeater is reproduced in Figure 1.15.

The Wrathall repeater used germanium transistors designed by Bell Labs and built by Western Electric. The silicon transistor was invented in 1954 by Gordon Teal at Texas Instruments and gained wide commercial acceptance because of the increased temperature performance and reliability. Finally, the invention of the integrated circuit (References 37 and 38) in 1958 followed by the planar process in 1959 (Reference 39) set the stage for future PCM developments. These key solid state developments are summarized in Figure 1.16 and discussed in greater depth in Chapter 4 of this book.

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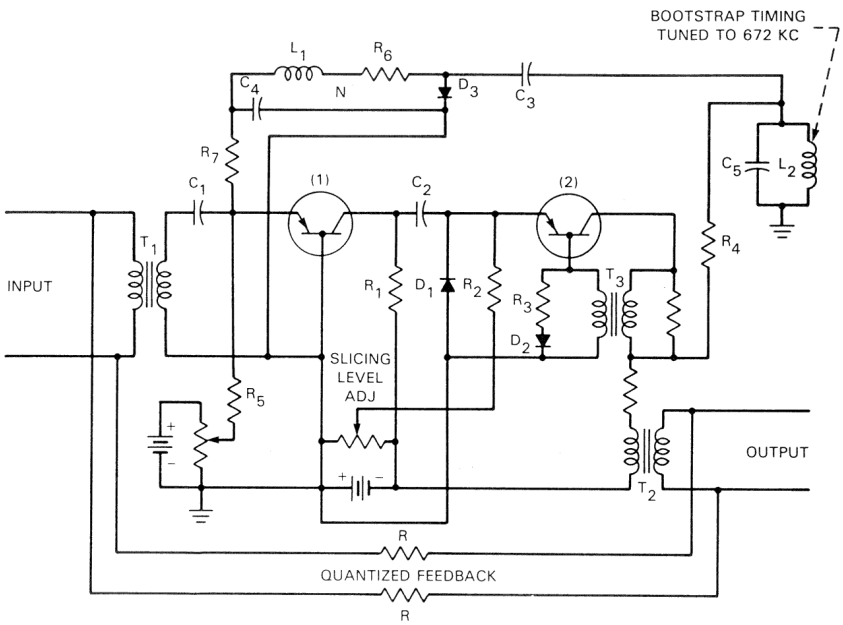

From: L.R. Wrathall, "Transistorized Binary Pulse Regenerator,"
***Bell System Technical Journal*, Vol. 35, September 1956, pp. 1059-1084**

Figure 1.15: *L. R. Wrathall's Solid State PCM Repeater: 1956*

- **Invention of the (Germanium) transistor at Bell Labs: John Bardeen, Walter Brattain, and William Shockley in 1947.**
- **Silicon Transistor: Gordon Teal, Texas Instruments, 1954.**
- **Birth of the Integrated Circuit:**
  - **Jack Kilby, Texas Instruments, 1958 (used bond wires for interconnections).**
  - **Robert Noyce, Fairchild Semiconductor, 1959 (used metallization for interconnections).**
- **The Planar Process: Jean Hoerni, Fairchild Semiconductor, 1959.**

Figure 1.16: *Key Solid-state Developments: 1947-1959*

With the development of the Wrathall repeater, it was therefore clear in 1956 that PCM could be effectively used to increase the number of voice channels available on existing copper cable pairs. This was especially attractive in metropolitan areas where many cable conduits were filled to capacity. Many of these pairs were equipped with loading coils at a spacing of 1.8 kM to improve their response in the voice band. It was natural to consider replacing the loading coils with solid-state repeaters and to extend the capacity from 1 to 24 channels by using PCM.

For these reasons, a decision was made at Bell Labs to develop a PCM carrier system, and a prototype 24-channel system was designed and tested during 1958 and 1959 on a link between Summit, New Jersey and South Orange, New Jersey. This system, called the T-1 carrier system, transmitted 24 voice channels using a 1.544-MHz pulse train in a bipolar code. The system used 7-bit logarithmic encoding with 26-dB of companding, and was later expanded to 8-bit encoding. The solid-state repeaters were spaced at 1.8-kM intervals, corresponding to the placement of the existing loading coils. The first T-1 operating link went into service in 1962, and by 1984 there were more than 200 million circuit-kilometers of T-1 carrier in the United States.

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NOTES:

SECTION 1.2: DATA CONVERTERS OF THE 1950s AND 1960s

Walt Kester

Commercial Data Converters: 1950s

Up until the mid-1950s, data converters were primarily developed and used within specialized applications, such as the Bell System work on PCM, and message encryption systems of World War II. Because of vacuum tube technology, the converters were very expensive, bulky, and dissipated lots of power. There was practically no commercial usage of these devices.

The digital computer was a significant early driving force behind commercial ADC development. The ENIAC computer development project was started in 1942 and was revealed to the general public in February 1946. The ENIAC led to the development of the first commercially available digital computer, the UNIVAC, by Eckert and Mauchly. The first UNIVAC was delivered to the United States Census Bureau in June 1951.

Military applications, such as ballistic trajectory computation, were early driving forces behind the digital computer, but as time went on, the possibilities of other applications in the area of data analysis and industrial process control created more general interest in digital processing, and hence the need for data converters. In 1953 Bernard M. Gordon, a pioneer in the field of data conversion, founded a company called Epsco Engineering in his basement in Concord MA. Gordon had previously worked on the UNIVAC computer, and saw the need for commercial data converters. In 1954 Epsco introduced an 11-bit, 50-kSPS vacuum-tube based ADC. This converter is believed to be the first commercial offering of such a device.

The Epsco "Datrac" converter dissipated 500 watts, was designed for rack mounting (19" × 15" × 26") and sold for $8,000 to $9,000 (see Reference 1). A photograph of the instrument is shown in Figure 1.17. The Datrac was the first commercially offered ADC to utilize the shift-programmable successive approximation architecture, and Gordon was granted a patent on the logic required to perform the conversion algorithm (Reference 2). Because it had a sample-and-hold function, the Epsco Datrac was the first commercial ADC suitable for digitizing ac waveforms, such as speech.

During the same period, a few other companies manufactured lower speed ADCs suitable for digital voltmeter measurement applications, and there were offerings of optical converters based on coded discs for measuring the angular position of shafts in avionics applications (see Reference 1). Converters of the mid to late 1950s used a combination of vacuum tubes, solid-state diodes, and transistors to implement the conversion process. A few of the companies in the data converter business at the time were Epsco, Non-Linear Systems, Inc., J.B. Rea, and Adage. In order to gain further insight to the converters of the 1950s, References 1, 3, 4, 5, and 6 are excellent sources.

- 19" × 15" × 26"
- 500W
- 150 lbs
- $8,500.00

Courtesy,
Analogic Corporation
8 Centennial Drive
Peabody, MA 01960

http://www.analogic.com

Figure 1.17: *1954 "DATRAC" 11-bit, 50-kSPS Vacuum Tube ADC Designed by Bernard M. Gordon at EPSCO*

Commercial Data Converter History: 1960s

During the mid 1950s through the early 1960s, electronic circuit designs began to migrate from vacuum tubes to transistors, thereby opening up many new possibilities in data conversion products. As was indicated earlier, the silicon transistor was responsible for the increased interest in solid state designs. There was more and more interest in data converter products, as indicated in two survey articles published in 1964 (Reference 5) and 1967 (Reference 6). Because these devices were basically unfamiliar to new customers, efforts were begun to define specifications and testing requirements for converter products (References 7-16).

The IBM-360 mainframe computer and solid state minicomputers (such as the DEC PDP-series starting in 1963) added to the general interest in data analysis applications. Other driving forces requiring data converters in the 1960s were industrial process control, measurement, PCM, and military systems.

Efforts continued during the 1960s at Bell Telephone Labs to develop high speed converters (e.g., 9 bits, 5 MSPS) for PCM applications (Reference 17), and the military division of Bell Labs began work on the development of hardware and software for an anti-ballistic missile (ABM) system.

In 1958, the U.S. Army began the development of the Nike-Zeus anti-ballistic missile system, with Bell Laboratories responsible for much of the hardware design. This program was replaced by Nike-X in 1963, which was the first program to propose a

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digitally controlled phased array radar for guiding the short and long-range interceptor missiles. The objective of the system was to intercept and destroy incoming Soviet nuclear warheads above the atmosphere and thereby protect U.S. population centers.

In 1967, President Lyndon Johnson and Secretary of Defense Robert McNamara redefined the ABM program and changed the name to Sentinel. This system used basically the same hardware as Nike-X, but the threat definition was changed from the Soviet Union to China, where work was underway on less sophisticated ICBMs, and nuclear capability had been demonstrated. This program provoked large scale public protests when it became clear that nuclear tipped interceptor missiles would be deployed very close to the cities they were meant to defend.

Richard Nixon became President in 1969, and the ABM program objective and name was once again changed for political reasons, but still using basically the same hardware. This time the program was called Safeguard, and the new objective was to protect Minuteman ICBM fields, Strategic Air Command bases, and Washington DC. The system would be deployed at up to 12 sites and utilize both short- and long-range missiles.

The Safeguard program became entangled in the politics of the SALT talks with the Soviet Union, and was eventually scaled back significantly. In the end, the Grand Forks, North Dakota site was the only site ever built; it became operational on October 1, 1975. On October 2, 1975, the House of Representatives voted to deactivate the Safeguard program.

Key to the Nike-X/Sentinel/Safeguard systems was the use of digital techniques to control the phased array radar and perform other command and control tasks. The logic was resistor-transistor-logic (RTL), and was mounted in hybrid packages. Also important to the system were the high speed ADCs used in the phased array radar receiver. Early prototypes for the required 8-bit 10-MSPS ADC were developed by John M. Eubanks and Robert C. Bedingfield at Bell Labs between 1963 and 1965. In 1966, these two pioneers in high speed data conversion left Bell Labs and founded Computer Labs—a Greensboro, NC based company—and introduced a commercial version of this ADC.

The 8-bit, 10-MSPS converter was rack mounted, contained its own linear power supply, dissipated nearly 150 watts, and sold for approximately $10,000 (see Figure 1.18). The same technology was used to produce 9-bit, 5-MSPS and 10-bit 3-MSPS versions. Although the next generation of Computer Labs' designs would take advantage of modular op amps (Computer Labs OA-125 and FS-125), ICs such as the Fairchild µA710/711 comparators, as well as 7400 TTL logic, the first ADCs offered used all discrete devices.

The early high speed ADCs produced by Computer Labs were primarily used in research and development projects associated with radar receiver development by companies such as Raytheon, General Electric, and MIT Lincoln Labs.

In the mid-1960s, development of lower speed instrument, PC-board, and modular ADCs was pioneered by such companies as Analogic (founded by Bernard M. Gordon) and Pastoriza Electronics (founded by James Pastoriza). Other companies in data converter business were Adage, Burr Brown, General Instrument Corp, Radiation, Inc., Redcor

Corporation, Beckman Instruments, Reeves Instruments, Texas Instruments, Raytheon Computer, Preston Scientific, and Zeltex, Inc. Many of the data converters of the 1960s were in the form of digital voltmeters which used integrating architectures, although Adage introduced an 8-bit, 1-MSPS sampling ADC, the Voldicon VF7, in the early 1960s (Reference 5).

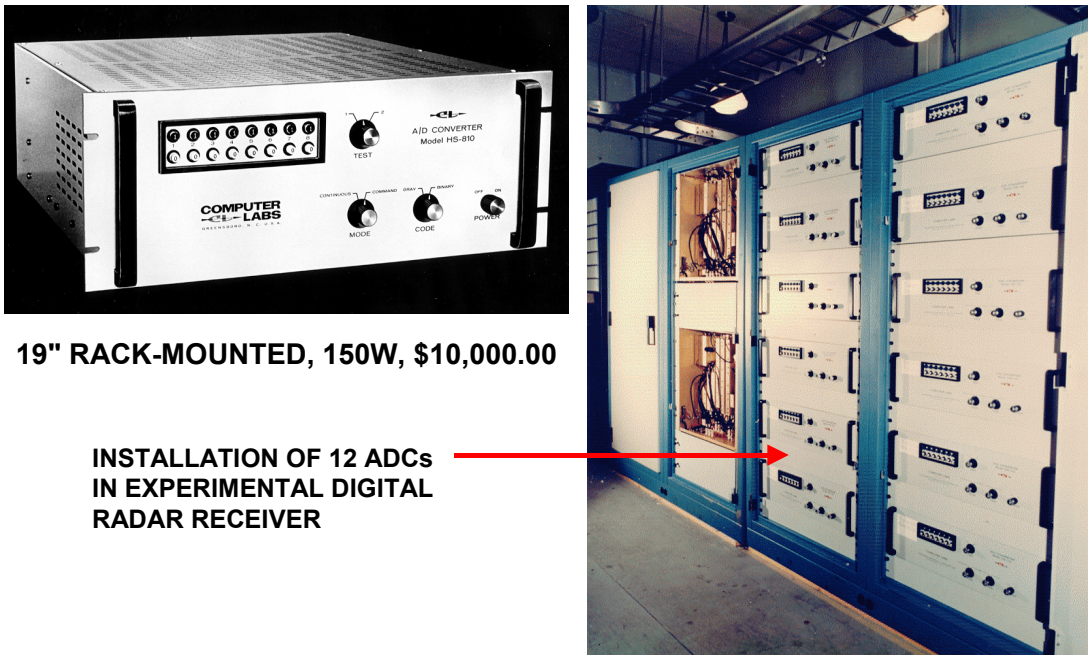

Figure 1.18: *HS-810, 8-bit, 10-MSPS ADC Released by Computer Labs, Inc. in 1966*

In addition to the widespread proliferation of discrete transistor circuits in the 1960s, various integrated circuit building blocks became available which led to size and power reductions in data converters. In 1964 and 1965, Fairchild introduced two famous Bob Widlar IC designs: the µA709 op amp and the µA710/µA711 comparator. These were quickly followed by a succession of linear ICs from Fairchild and other manufacturers. The 7400-series of transistor-transistor-logic (TTL) and high-speed emitter-coupled-logic (ECL) also emerged during this period as well as the 4000-series CMOS logic from RCA in 1968. In addition to these devices, Schottky diodes, Zener reference diodes, FETs suitable for switches, and matched dual JFETs also made up some of the building blocks required in data converter designs of the period.

In 1965, Ray Stata and Matt Lorber founded Analog Devices, Inc. (ADI) in Cambridge, MA. The initial product offerings were high performance modular op amps, but in 1969 ADI acquired Pastoriza Electronics, a leader in data converter products, thereby making a solid commitment to both data acquisition and linear products.

Pastoriza had a line of data acquisition products, and Figure 1.19 shows a photograph of a 1969 12-bit, 10-µs general purpose successive approximation ADC, the ADC-12U, that sold for approximately $800.00. The architecture was successive approximation, and the ADC-12U utilized a µA710 comparator, a modular 12-bit "Minidac," and 14 7400-series logic packages to perform the successive approximation conversion algorithm.

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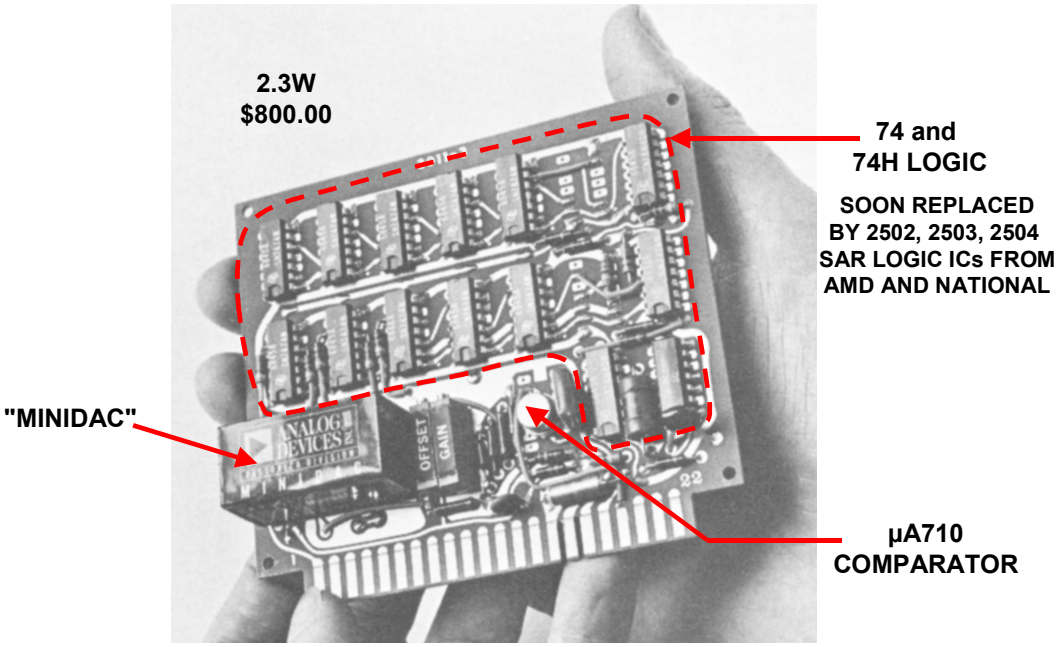

Figure 1.19: *ADC-12U 12-Bit, 10-μs SAR ADC from Pastoriza Division of Analog Devices, 1969*

The "Minidac" module was actually constructed from "quad switch" ICs (AD550) and a thin film network (AD850) as shown in Figure 1.20. Figure 1.21 shows details of the famous quad switch that was patented by James Pastoriza (Reference 18). Chapter 3 of this book contains more discussion on the quad switch and other DAC architectures.

Notice that in the ADC-12U, the implementation of the successive approximation algorithm required 14 logic packages. In 1958, Bernard M. Gordon had filed a patent on the logic to perform the successive approximation algorithm (Reference 19), and in the early 1970s, Advanced Micro Devices and National Semiconductor introduced commercial *successive approximation register* logic ICs: the 2502 (8-bit, serial, not expandable), 2503 (8-bit, expandable) and 2504 (12-bit, serial, expandable). These were designed specifically to perform the register and control functions in successive approximation ADCs. These became standard building blocks in many modular and hybrid data converters. In fact, the acronym *SAR* actually stands for *successive approximation register*, and hence the term *SAR* ADC. Earlier converters utilizing the successive approximation architecture were simply referred to as *sequential coders*, *feedback coders*, or *feedback subtractor coders*.

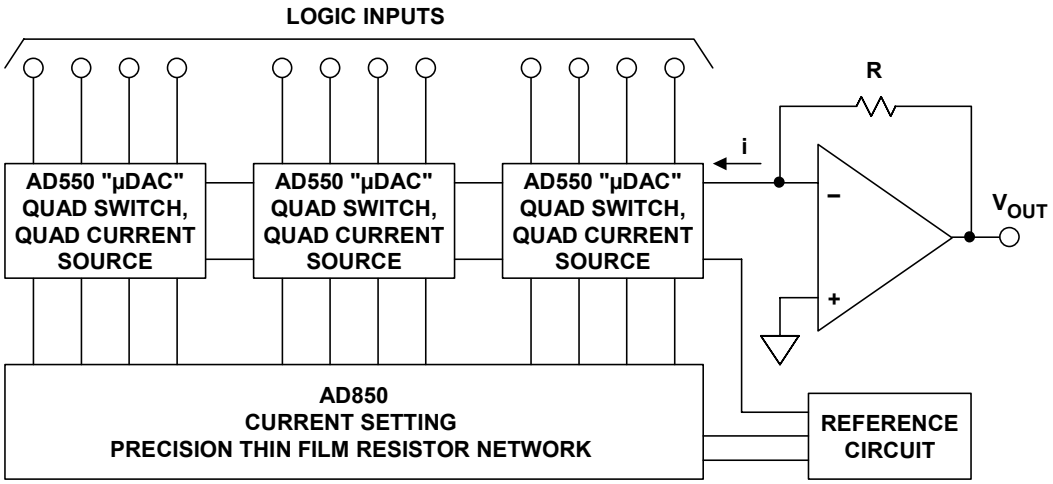

Figure 1.20: *A 1969 Vintage 12-bit "MiniDAC" Using Quad Current Switches, a Thin Film Resistor Network, a Voltage Reference, and an Op Amp*

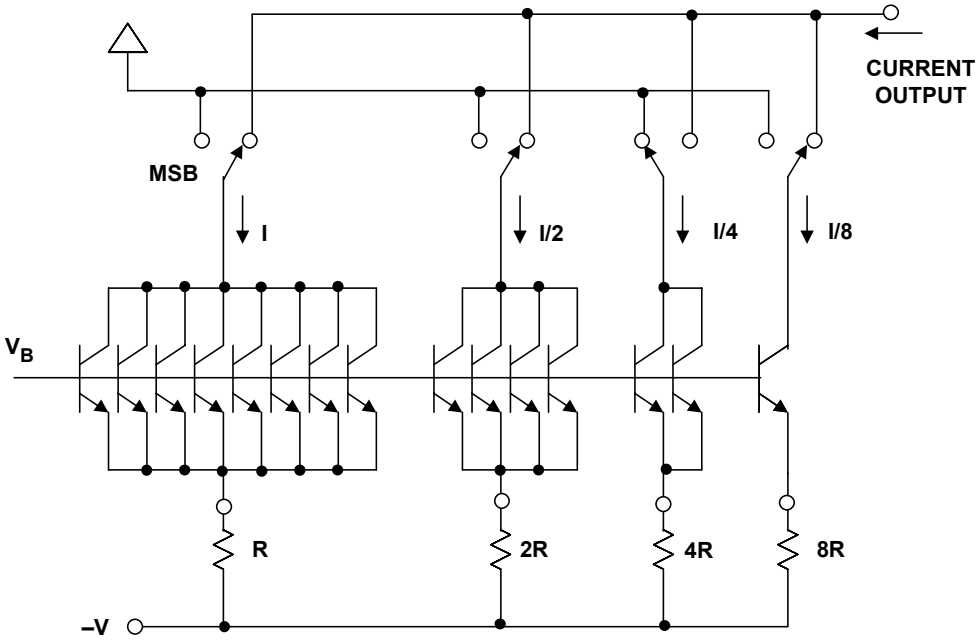

Figure 1.21: *"Quad Switch" DAC Building Block with External Thin Film Resistor Network*

Data Converter Architectures

Details of the history of the various data converter architectures are contained in Chapter 3 of this book, so for now, we will just summarize the key developments.

The basic algorithm used in the successive approximation (initially called *feedback subtraction*) ADC conversion process can be traced back to the 1500s relating to the solution of a certain mathematical puzzle regarding the determination of an unknown weight by a minimal sequence of weighing operations (Reference 20). In this problem, as stated, the object is to determine the least number of weights which would serve to weigh an integral number of pounds from 1 lb to 40 lb using a balance scale. One solution put forth by the mathematician Tartaglia in 1556, was to use the series of weights 1 lb, 2 lb, 4 lb, 8 lb, 16 lb, and 32 lb. The proposed weighing algorithm is the same as used in modern successive approximation ADCs. (It should be noted that this solution will actually measure unknown weights up to 63 lb rather than 40 lb as stated in the problem). The algorithm is shown in Figure 1.22 where the unknown weight is 45 lbs. The balance scale analogy is used to demonstrate the algorithm. The electronic implementation of the successive approximation ADC is shown in Figure 1.23.

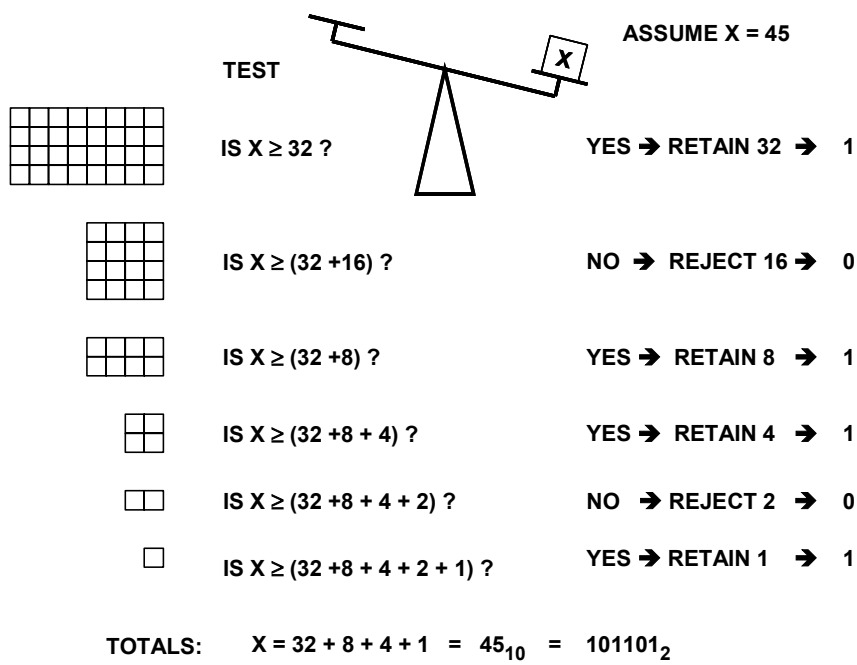

Figure 1.22: *Successive Approximation ADC Algorithm Analogy Using Binary Weights*

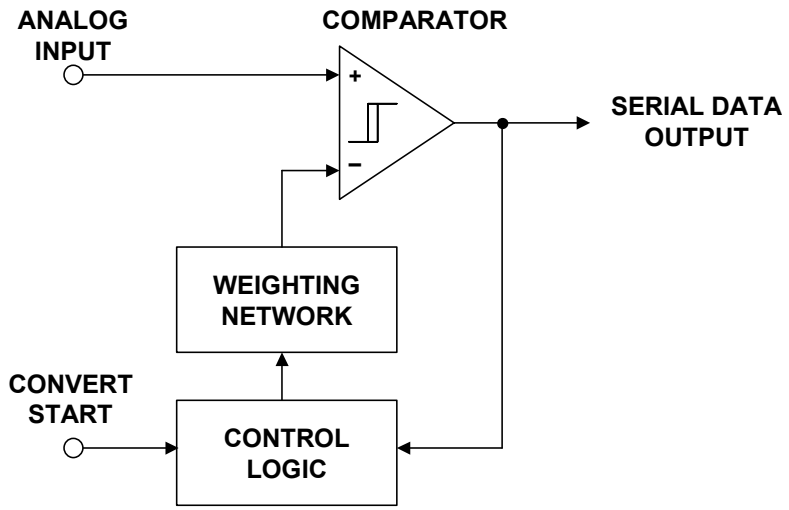

Figure 1.23: *Basic Successive Approximation ADC (Feedback Subtraction ADC)*

It is interesting to note that all the fundamental ADC architectures used today had been discovered and published in one form or another by the mid-1960s. Figure 1.24 shows a detailed timeline for the development of the successive approximation ADC. Figure 1.25 shows the timeline high speed ADC architectures, and Figure 1.26 shows the timeline for counting and integrating ADCs. Even the Σ-Δ ADC architecture had been explored as shown in Figure 1.27. A much more detailed discussion of each individual architecture and its history can be found in Chapter 3 of this book.

- **SAR algorithm dates back to the 1500's**
- **Early SAR ADCs used individually switched binary reference voltages rather than internal DAC (Schelling: 1946, Goodall: 1947)**
- **Use of internal DAC rather than switched reference voltages to perform conversion (Kaiser: 1953, B. D. Smith: 1953)**
- **Use of non-uniformly weighted DAC to produce companding transfer function (B. D. Smith: 1953)**
- **First commercial vacuum tube SAR ADC, 11-bits, 50kSPS (Bernard M. Gordon - Epsco: 1954)**
- **Design of specific logic function to perform SAR algorithm (Gordon: 1958)**
  Led to popular SAR logic ICs: 2503, 2504 from National Semiconductor and Advanced Micro Devices in the early 1970's

Figure 1.24: *SAR ADC Development Summary*

◆ **Reeve's counting ADC**	**1939**
◆ **Successive approximation**	**1946**
◆ **Flash (electron tube coders)**	**1948**
◆ **Bit-per-stage (binary and Gray)**	**1956**
◆ **Subranging**	**1956**
◆ **Subranging with error correction**	**1964**
◆ **Pipeline with error correction**	**1966**

Note: Dates are first publications or patent filings

Figure 1.25: *High Speed ADC Architecture Timeline*

◆ **Reeve's counting ADC**	**1939**
◆ **Charge run-down:**	**1946**
◆ **Ramp run-up**	**1951**
◆ **Tracking**	**1950**
◆ **Voltage-to-frequency converter (VFC)**	**1952**
◆ **Dual Slope**	**1957**
◆ **Triple Slope**	**1967**
◆ **Quad Slope**	**1973**

Note: Dates are first publications or patent filings

Figure 1.26: *Counting and Integrating ADC Architecture Timeline*

- **Delta Modulation** **1950**
- **Differential PCM** **1950**
- **Single and multibit oversampling with noise shaping** **1954**
- **First called Δ-Σ, "delta-sigma"** **1962**
- **Addition of digital filtering and decimation for Nyquist ADC** **1969**
- **Bandpass Sigma-Delta** **1988**

Note: Dates are first publications or patent filings

Figure 1.27: *Sigma-Delta ADC Architecture Timeline*

By the end of the 1960s, the key architectures and building blocks were available to allow for modular and ultimately hybrid converters, and significant work was already underway to produce the first monolithic converters which were to appear in the early 1970s.

DISH 1028

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1.2 DATA CONVERTERS OF THE 1950s AND 1960s

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15. Bernard M. Gordon, "Speaking Out on Analog to Digital Converters," **EEE Magazine**, December 1968.

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17. J. O. Edson and H. H. Henning, "Broadband Codecs for an Experimental 224Mb/s PCM Terminal," **Bell System Technical Journal**, Vol. 44, pp. 1887-1940, Nov. 1965.

18. James J. Pastoriza, "Solid State Digital-to-Analog Converter," **U.S. Patent 3,747,088**, filed December 30, 1970, issued July 17, 1973. *(the first patent on the quad switch approach to building high resolution DACs).*

19. Bernard M. Gordon and Evan T. Colton, "Signal Conversion Apparatus," **U.S. Patent 2,997,704**, filed February 24, 1958, issued August 22, 1961. *(classic patent describes the logic to perform the successive approximation algorithm in a SAR ADC).*

20. W. W. Rouse Ball and H. S. M. Coxeter, **Mathematical Recreations and Essays**, Thirteenth Edition, Dover Publications, 1987, pp. 50, 51. *(describes a mathematical puzzle for measuring unknown weights using the minimum number of weighing operations. The solution proposed in the 1500's is the same basic successive approximation algorithm used today).*

Note on Anti-Ballistic Missile (ABM) system history:

Although most of the information regarding the various ABM systems was classified at the time, today the information is in the public domain. There are several excellent websites which can provide further information and references:

http://www.ucsusa.org is a site maintained by the Union of Concerned Scientists, 2 Brattle Square, Cambridge, MA 02238. There is a section on the site under the security section titled "From Nike-Zeus to Safeguard: US Defenses Against ICBMs, 1958-1976.

http://www.paineless.id.au/missiles is a site maintained by an individual with an excellent collection of references about the ABM programs. A good whitepaper on the site is titled "Nuclear ABM Defense of the USA."

In addition to the websites, the following book published by the Bell System provides a good discussion of the development of the ABM system:

M. D. Fagen, **A History of Engineering and Science in the Bell System: National Service in War and Peace (1925-1975)**, Bell Telephone Laboratories, 1978, ISBN 0-932764-00-2.

SECTION 1.3: DATA CONVERTERS OF THE 1970s

Introduction

The year 1970 began one of the most exciting decades in the history of data converters. The ADC/DAC market was driven by a number of applications, including high resolution digital voltmeters, industrial process control, digital video, military phased array radar, medical imaging, vector scan displays, and raster scan displays. Most of these systems had formerly utilized conventional analog signal processing techniques, and the increased availability of low cost computing technology generated a desire to take advantage of the increased performance and flexibility offered by digital signal processing and analysis—and of course, the need for compatible data converters.

As a result, a number of companies entered the data converter field, including Analog Devices, Analogic Corporation (initially Epsco and later Gordon Engineering), Burr Brown, Computer Labs, Datel, Hybrid Systems, ILC/Data Device Corporation, Micronetworks, National Semiconductor, Teledyne Philbrick, and Zeltex.

Integrated circuit building blocks, as well as complete IC data converters of the 1970s, came from Analog Devices, Advanced Micro Devices, Fairchild, Signetics, Intersil, Micro Power Systems, Motorola, National Semiconductor, TRW (LSI Division), and Precision Monolithics.

The data converters of the 1970s made maximum utilization of all the technologies available: monolithic, modular, and hybrid, with the modular and hybrid products typically offering higher resolution and faster speed than the existing monolithic parts.

An often overlooked fact is that both customer education and high quality application support is required in order to take full advantage of an emerging technology such as data conversion. From the beginning, Analog Devices has always realized the importance of excellent application material, starting with a set of tutorial articles on op amps by its founder, Ray Stata (Reference 1). These articles were published in 1965—the same year Analog Devices was founded—and are still recognized as classic tutorials on basic op amp theory and applications.

The ADI continuing thread of customer support through applications information was enhanced considerably in 1967, when the *Analog Dialogue* magazine was launched (see Reference 2). The initial charter for the magazine was stated as "A Journal for the Exchange of Operational Amplifier Technology," later on this was broadened to "A Journal for the Exchange of Analog Technology."

Dissemination of analog circuit information is what the early *Analog Dialogue* did, and did it well. The premier issue featured an op amp article by Ray Stata that is still available as an application note (see Reference 3). A similar comment can also be made for a subsequent Ray Stata article (see Reference 4).

A milestone in the life of the young magazine was the arrival of Dan Sheingold as editor, in 1969 (see Reference 5). Already highly experienced as a skilled op amp expert and

editorial writer from vacuum tube and early solid-state years at George A. Philbrick Researches (GAP/R), Dan Sheingold brought a unique set of skills to the task of editorial guidance for *Analog Dialogue*. Dan's leadership as editor continues today, in 2004. For more than 35 years his high technical communication standards have been an industry benchmark.

Realizing the need for a comprehensive book on the newly emerging field of data conversion, Analog Devices published the first edition of the *Analog-Digital Conversion Handbook* in 1972, under the excellent editorship of Dan Sheingold (Reference 6). An interim revision, *Analog-Digital Conversion Notes*, was published in 1977 (Reference 7). In 1986, in conjunction with Prentice-Hall, Sheingold published a third revision, again titled *Analog-Digital Conversion Handbook* (Reference 8). All of these books provided detailed information on data converter architectures, specifications, design, and applications, and helped in the adoption of uniform terminology and performance metrics throughout the industry.

Monolithic Data Converters of the 1970s

Bipolar Process IC DACs of the 1970s

The earliest monolithic DACs were made using bipolar process technology; they included only the basic core of a complete DAC—the array of switches and resistors to set the weight of each bit. An example is the 1408 and a later higher speed derivative, the DAC08, introduced in 1975 and shown in Figure 1.28.

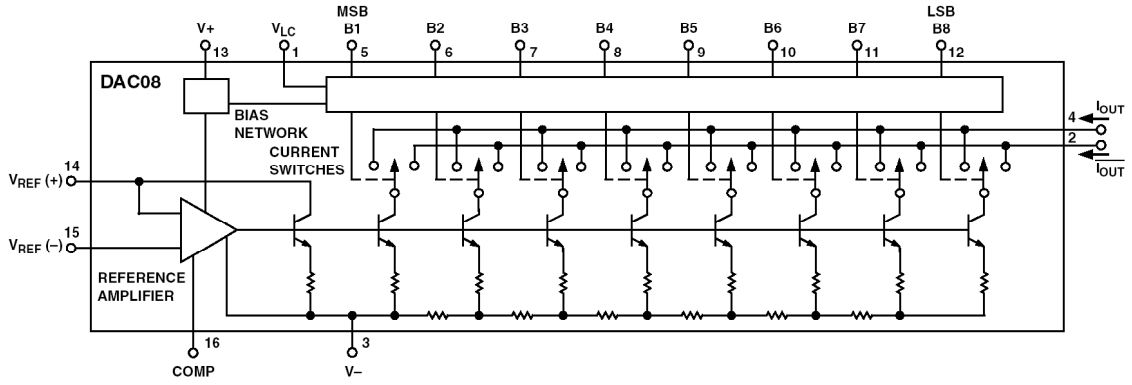


Figure 1.28: *DAC08 8-Bit 85-ns IC DAC, 1975*

These converters were produced by several manufacturers and were available at low cost. However, they required many additional external components in order to be usable in a system design. These external components included several resistors, a voltage reference, a latch, an output op amp, possibly a compensation capacitor, and usually one or more trimming potentiometers.

Converters like the 1408 and DAC08 were limited to 8-bit accuracy by the matching and tracking limitations of the diffused resistors. When higher accuracy is required, lower tempco resistors are needed, and some means of post-fabrication adjustment is desirable.

Thin film resistors exhibit low tempcos and can be trimmed with a laser—they are well suited for use in data converters. By the mid 1970s, Analog Devices had developed considerable expertise, not only the deposition of thin film resistors, but also trimming at the wafer level.

The Analog Devices' AD562, designed by Bob Craven and introduced in 1974, was originally a "compound monolithic" manufactured using two IC chips mounted in the same package, without the traditional hybrid substrate for mounting and interconnection. Instead, the two chips were designed so that a set of wire bonds between the two chips (in addition to the usual ones to the package pins) were all that were necessary to assemble a 12-bit accurate DAC in an IC package. In the original AD562, one chip contained the thin film resistor network (including the bit weight-setting resistors and output gain-setting resistors), and the other chip contained the reference control amplifier and the current switches for the 12 bits. As the processing matured, the manufacture of larger chips became more practical. The two chips of the original AD562 were later merged into a single-chip version. It became the first 12-bit DAC qualified by the U.S. Department of Defense under MIL-M-38510.

While the AD562 was the first 12-bit IC DAC and embodied the solution to some extremely difficult design problems; it was still really only a building block, since it lacked *buffer latches*, a *voltage reference*, and an *output amplifier*. Shortly after the two-chip AD562 was introduced (Reference 9, 10), a version with a third chip was developed. The third chip was a 2.5-V bandgap reference (designed by Paul Brokaw and described in detail in Reference 11 and 12). This made the DAC function much more complete. The resulting product, known as the AD563, also became quite popular and eventually made the transition to a completely monolithic single-chip device.

Another problem with the AD562 was that, while reasonably fast, it lacked sufficient speed for many applications—its settling time was approximately 1 µs. Later advances in switch design and Zener diode fabrication led to a higher speed DAC, the AD565, introduced in 1978 (later followed by the AD565A in 1981). A simplified diagram of the AD565 is shown in Figure 1.29.

The bit switches used in this design were much smaller than those used in the AD562, allowing a substantial reduction in chip area and increasing the yield of good chips per wafer. The new switches yielded a settling time of 200 ns to ½ LSB. The AD565 used a buried Zener reference which had less noise than the bandgap reference used in the AD563.

The AD565 retained the same pinout as the earlier AD563, allowing drop-in replacement with improved performance and lower price.

It should be noted that the first monolithic single-chip 10-bit DAC with thin film laser wafer trimmed (LWT) resistors and internal reference was the AD561, designed by Peter Holloway, which was introduced by Analog Devices in 1976 (Reference 13). This DAC utilized a method of compensating for errors produced by operating the internal current source transistors at different current densities. This idea is patented by Paul Brokaw and is one of the most widely referenced patents in data conversion (Reference 14).

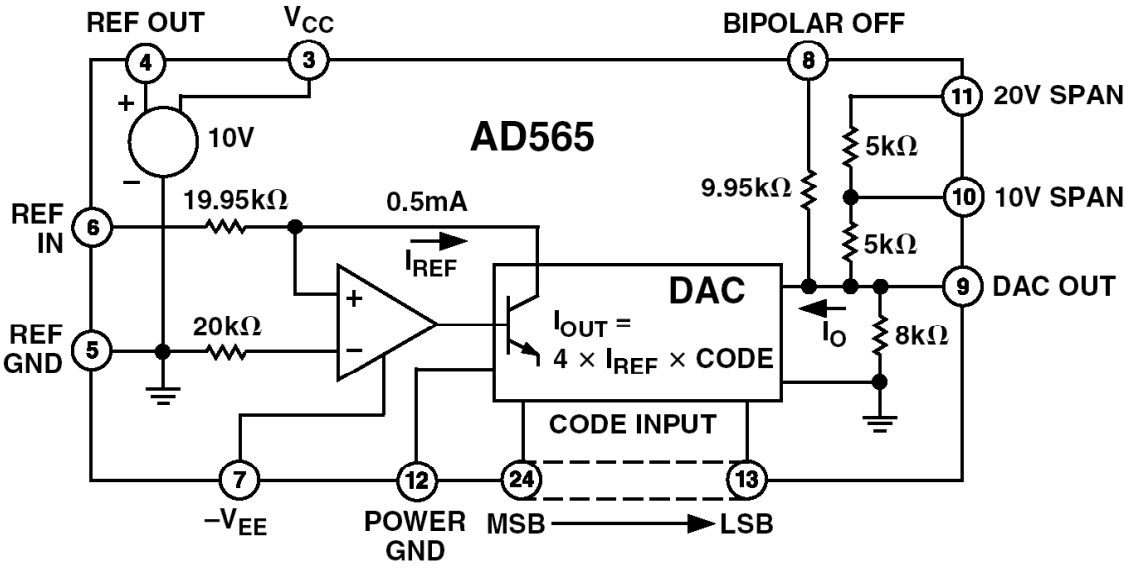


Figure 1.29: *AD565, 12-Bit, 200-ns DAC, 1978*

CMOS IC DACs of the 1970s

As we have seen, the early commercially available monolithic DACs were principally processed by conventional bipolar linear processing techniques. Before 1974, when the AD7520 CMOS DAC was introduced, 10-bit conversion had been difficult to obtain with good yields (and low cost) because of the finite β of switching devices, the V_{BE}-matching requirement, the matching and tracking requirements on the diffused resistor ladders, and the tracking limitations caused by the thermal gradients produced by high internal power dissipation.

Most of these problems were solved or avoided with CMOS devices. The CMOS transistors have nearly infinite current gain, eliminating β problems. There is no equivalent in CMOS circuitry to a bipolar transistor's V_{BE} drop; instead, a CMOS switch in the ON condition is almost purely resistive, with the resistance value controllable by device geometry. The temperature problems of diffused resistors were eliminated by using thin film resistors instead. A simplified diagram of the AD7520 10-bit, 500-ns CMOS multiplying DAC introduced in 1974 is shown in Figure 1.30.

The AD7520 architecture is a standard current-mode R-2R (also referred to as an "inverted R-2R") and is described further in Chapter 3 of this book. The output drives the inverting input of an external op amp connected as an I/V converter. The 10-kΩ feedback resistor for the op amp is internal to the AD7520 to provide good tracking. The key to the linearity of the AD7520 is that the geometries of the switches corresponding to the first six bits are tapered so as to obtain ON resistances that are related in binary fashion.

The AD7520 architecture was extended to 12-bit resolution in the AD7541 by merely adding additional switch cells and resistors. However, in order to achieve 12-bit linearity, laser trimming at the wafer level was required. The AD7541, introduced in 1978, was the first 12-bit CMOS multiplying DAC. Settling time to ½ LSB was 1 µs.

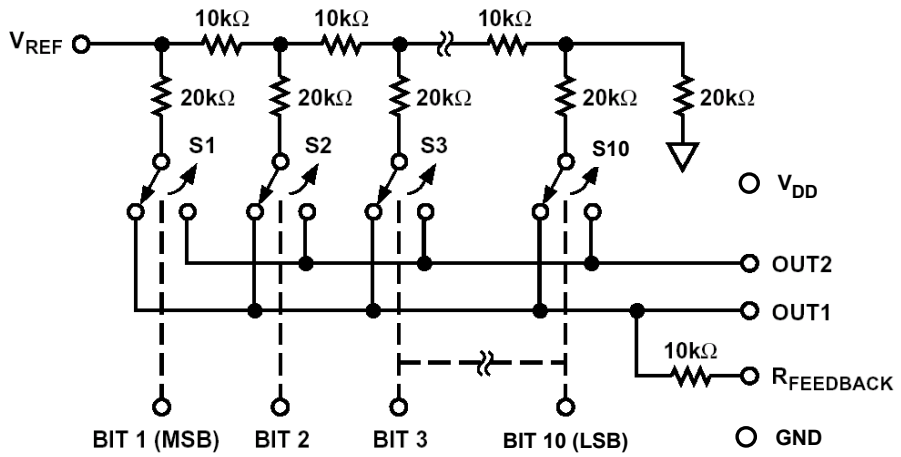


Figure 1.30: *AD7520, the First Monolithic CMOS Multiplying 10-Bit DAC, 1974*

The AD7520 and AD7541 were the beginning of an entire product line of general purpose multiplying CMOS DACs from Analog Devices. Some of these products will be discussed in Section 1.3, *Data Converters of the 1980s*.

Another useful feature for a DAC is the addition of an on-chip latch (generally referred to as a "buffered" DAC). The latch allows the DAC to be connected to a microprocessor data bus. The AD7524, shown in Figure 1.31, was an 8-bit multiplying CMOS DAC which had an on-chip latch. Data is loaded into the DAC by first asserting the $\overline{\text{CHIP SELECT}}$ pin. Data is then written into the latch by asserting the $\overline{\text{WRITE}}$ pin. Returning the $\overline{\text{WRITE}}$ pin to 0 disconnects the latch from the data bus, and the bus can then be connected to another device if desired.

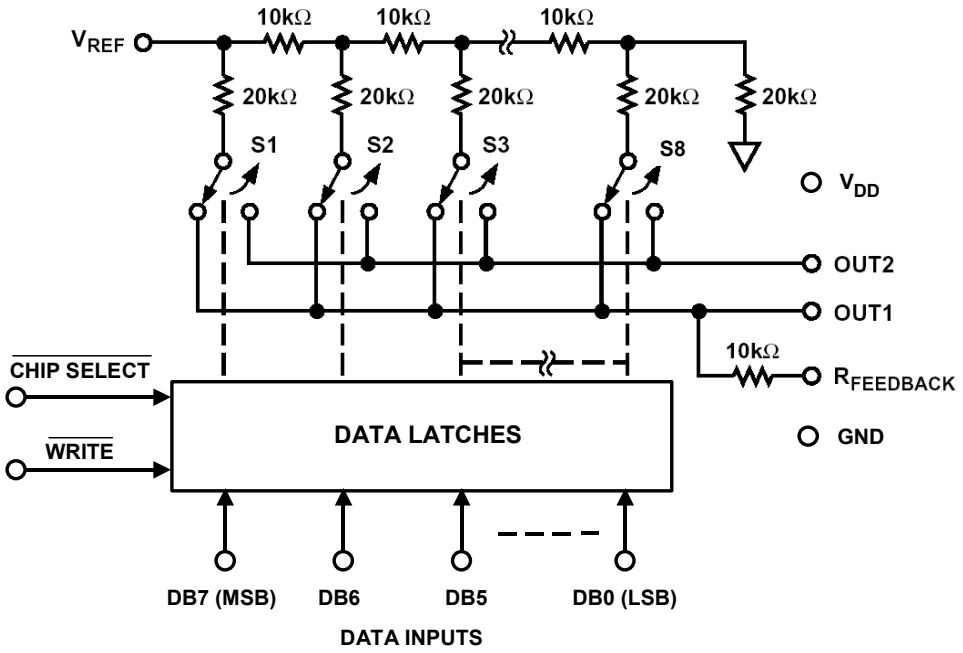


Figure 1.31: *AD7524 8-Bit Buffered µP Compatible DAC, 1978*

Future DAC products added a second latch, and are referred to as a "double-buffered" DAC. The input latch is used to load the data (either serial, parallel, or in bytes), and when the second parallel "DAC latch" is clocked, the DAC output is updated.

Data converter designers soon realized the importance of making them easy to interface to microprocessors and DSPs, and this trend added additional functionality to the devices and continues to this day.

A summary of the monolithic DAC developments during the 1970s is shown in Figure 1.32.

- **Bipolar:**
  - **AD550 "µDAC" Building Block Quad Switch, 1970**
  - **AD562 12-Bit, 1.5µs (2-chip, compound monolithic) DAC, 1974**
  - **1408 8-Bit 250ns DAC, 1975**
  - **DAC08 8-Bit, 80ns DAC, 1976**
  - **AD561 10-Bit, 250ns, LWT Current-Output DAC with Reference, 1976**
  - **AD565 12-Bit, 200ns, LWT Current-Output DAC with Reference, 1978**

- **CMOS:**
  - **AD7520 10-Bit, 500ns, Multiplying DAC, 1974**
  - **AD7541 12-Bit, 1µs, LWT Multiplying DAC, 1978**
  - **AD7524, 8-Bit, 150ns LWT Multiplying DAC with DAC buffer latch, µP interface, 1978**

Figure 1.32: *Summary: Monolithic DACs of the 1970s*

Monolithic ADCs of the 1970s

Although most of the ADCs of the early 1970s were modular or hybrid, there was considerable effort by data converter manufacturers to produce an all-monolithic ADC. An early attempt was the AD7570 10-bit, 20-µs CMOS SAR ADC introduced in 1975. However, due to the difficulty of designing good comparators, amplifiers, and references on the early CMOS process, the AD7570 required an external LM311 comparator as well as a voltage reference.

The integrating ADC architecture was suitable for the early CMOS processes, and in 1976, Analog Devices introduced the 13-bit AD7550 which utilized a unique architecture called "quad slope." The architecture was patented by Ivar Wold (Reference 15).

The first complete monolithic ADC was the 10-bit, 25-µs AD571 SAR ADC introduced in 1978 and designed by Paul Brokaw (Reference 16). The AD571 was designed on a bipolar process with LWT thin film resistors. In order to implement the logic functions required in the SAR ADC, integrated-injection logic (I^2L) was added to the bipolar process. This process allowed reasonably dense low voltage logic to be included on the same chip as high-breakdown precision linear circuitry.

The I^2L process was particularly useful in manufacturing ADCs, because only a single additional diffusion step was required beyond those used in the standard linear process. Furthermore, this diffusion did not significantly interfere with the other steps in the process, so the analog circuitry was relatively unaffected by the addition of the logic.

The 10-bit AD571 (and the 8-bit AD570) were completely self-contained monolithic ADCs with internal clock, buried Zener voltage reference, laser-trimmed DAC (based on the design in Reference 14), and three-state output buffers. A simplified diagram of the AD571 is shown in Figure 1.33.

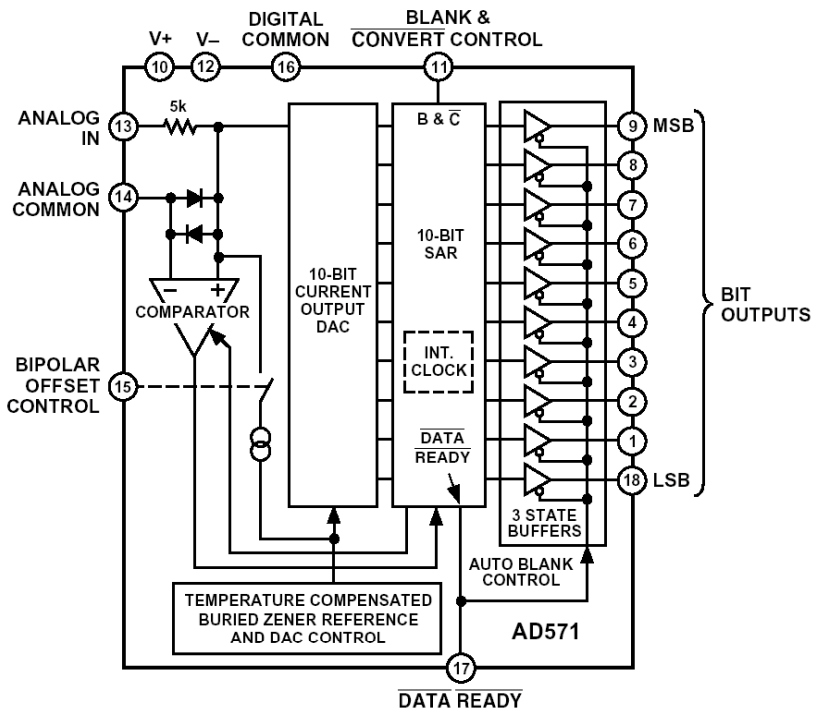


Figure 1.33: *AD571 Complete 10-Bit, 25-µs IC ADC, 1978*

Probably the most significant SAR ADC ever introduced was the 12-bit, 35-µs AD574 in 1978. The AD574 represents a complete solution, including buried Zener reference, timing circuits, and three-state output buffers for direct interfacing to an 8-, 12-, or 16-bit microprocessor bus. In its introductory form, the AD574 was manufactured using compound monolithic construction, based on two chips—one an AD565 12-bit current-output DAC, including reference and thin film scaling resistors; and the other containing the successive approximation register (SAR) and microprocessor interface logic functions as well as a precision latching comparator. The AD574 soon emerged as the industry-standard 12-bit ADC in the early 1980s. In 1985, the device became available in single-chip monolithic form for the first time; thereby making low-cost commercial plastic packaging possible. A simplified block diagram of the AD574 is shown in Figure 1.34.

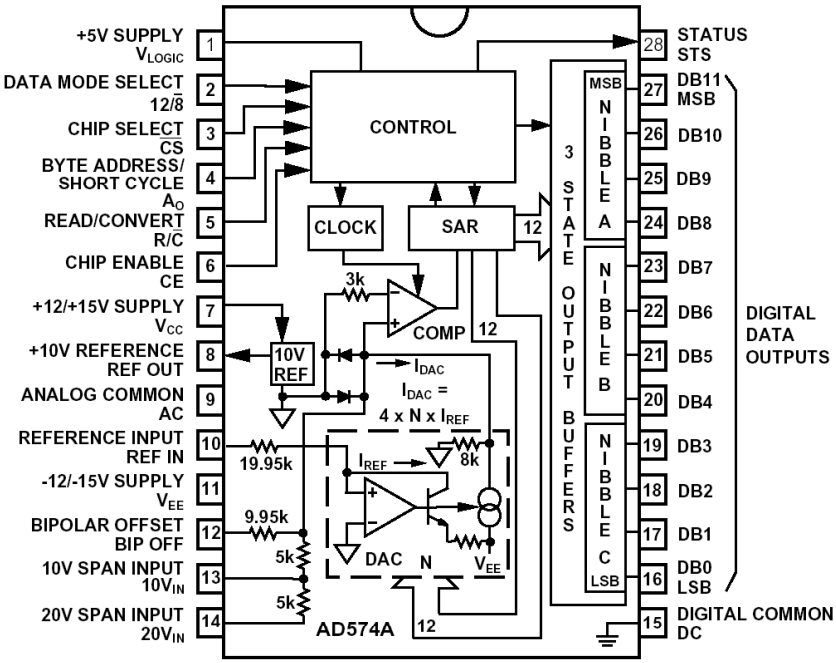


Figure 1.34: *The Industry-Standard AD574 12-Bit, 35-µs IC ADC, 1978*

As the 1970s came to a close, the first high-speed video flash ADCs emerged, starting with the TDC-1007J 8-bit, 30-MSPS from the LSI division of TRW in 1979 (Reference 17). TRW also introduced a lower power 6-bit version, the TDC-1014J. Also in 1979, Advanced Micro Devices introduced the AM6688 4-bit, 100-MSPS flash ADC, designed by Jim Giles, who had previously designed the AM685 and AM687 fast ECL comparators. There is more discussion on the history of flash converters in *Section 1.4, Data Converters of the 1980s*. A summary of key monolithic ADC developments in the 1970s is given in Figure 1.35.

- **AD7570, 10-bit, 20µs CMOS SAR ADC, (required external comparator, reference) 1975**
- **AD7550, 13-bit integrating ADC based on "quad slope" technique, 1976**
- **AD571, Complete 10-bit, 25µs monolithic SAR ADC, *with reference*, using I^2L and LWT thin film resistors, designed by Paul Brokaw, 1978**
- **AD574, 12-bit, 35µs two-chip, compound monolithic complete SAR ADC: AD565 DAC + logic chip), 1978; single-chip version 1985**
- **Flash ADCs:**
  - **TRW TDC-1007J / TDC-1016J, 8-bit / 6-bit 30MSPS ADCs, 1979**
  - **AM6688 4-bit, 100MSPS ADC, 1979**

Figure 1.35: *Summary: Monolithic ADCs of the 1970s*

Hybrid Data Converters of the 1970s

Although a few more instrument-type rack-mounted data converters were developed in the early 1970s (such as the VHS-series and 7000-series from Computer Labs, Inc.), the demand for lower cost more compact high performance data converters led manufacturers to turn toward hybrid and modular techniques—as the monolithic technology of the period was not yet capable of supporting the high-end converter functions in single-chip form.

Hybrid and modular data converter designers of the 1970s had a virtual smorgasbord of components from which to choose, including IC op amps, IC DACs, comparators, discrete transistors, various logic chips, etc. Figure 1.36 lists some of the more popular hybrid and modular building blocks for the 1970s.

- **Quad switches (AD550 µDAC)**
- **Precision thin film resistor networks (AD850)**
- **IC DACs: AD562, AD563, AD565, 1408, DAC08**
- **IC Comparators: µA710, µA711, NE521, LM311, LM361, MC1650, AM685, AM687**
- **Successive approximation registers (SARs): 2502, 2503, 2504**
- **IC and hybrid op amps**
- **IC voltage references, Zener references**
- **Fast PNP and fast NPN discrete transistors**
- **Matched monolithic dual FETs**
- **Monolithic transistor arrays (RCA CA-series)**
- **Schottky diodes**
- **CMOS and DMOS switches**
- **TTL, CMOS, ECL logic**
- **4, 6, 8-bit monolithic flash ADCs (starting in 1979)**

Figure 1.36: *Building Block Components for 1970s Hybrid and Modular Data Converters*

Hybrids generally utilize ceramic substrates with either thick or thin film conductors. Individual die are bonded to the substrate (usually with epoxy), and wire bonds make the connections between the bond pads and the conductors. The hybrid is usually hermetically sealed in some sort of ceramic or metal package. Accuracy was achieved by trimming thick or thin film resistors after assembly and interconnection, but before sealing. Manufacturers used thin film networks, discrete thin film resistors, deposited thick or thin film resistors, or some combination of the above.

Although the chip-and-wire hybrid was certainly more expensive to manufacture than an IC, it allowed performance levels that could not be achieved with existing monolithic technology of the period. The popular hybrid circuits followed an evolutionary path to monolithic form, generally over a 5- to 10-year period, depending upon the particular device. One of the most popular 12-bit DACs of the 1970s was the DAC80, originally

introduced in the mid 1970s as a hybrid device consisting of 11 chips: three quad switch arrays, two op amps, two resistor networks, a Zener diode, two clamp diodes, and a chip capacitor (see Figure 1.37A). In 1978, when monolithic technology had progressed to the point where it was possible to combine the switch and resistor network into a single chip, a three-chip DAC80 was introduced as shown in Figure 1.37B. The three chips in this design included a voltage reference, an output op amp, and the switch/resistor/control-amplfier chip.

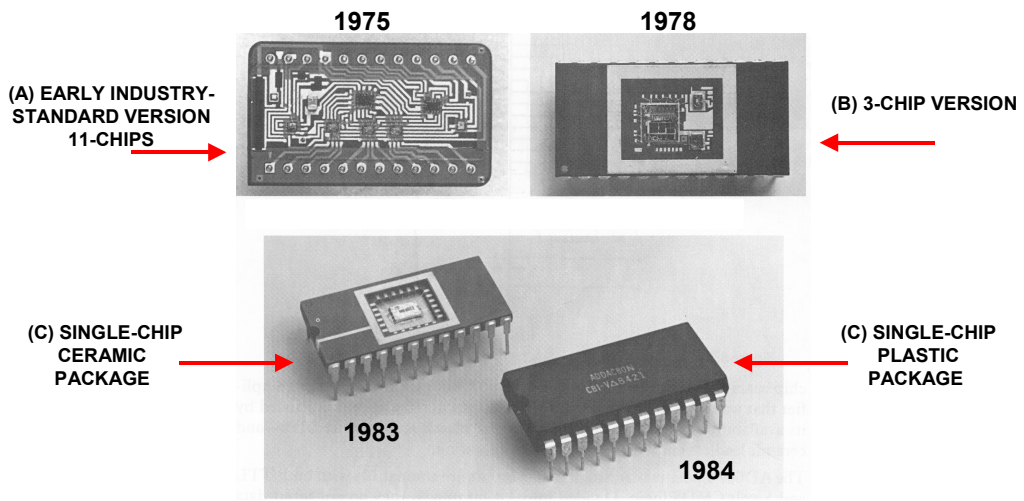


Figure 1.37: *DAC-80 12-Bit DAC Evolution*

The newer design offered performance identical to that of the original DAC80, but with a tremendous improvement in reliability and at a much lower cost. Then, in 1983, the first single-chip DAC80 became available (Figure 1.37C). It, of course, provided further cost reduction and reliability improvement, compared to the 3- and 11-chip versions. Finally, in 1984, this popular device was offered in a low-cost plastic DIP package. Thus, in approximately 10 years, the DAC80 evolved from a relatively high-cost hybrid to a high-volume commodity IC.

Another excellent example of hybrid technology was the AD572 12-bit, 25-µs SAR ADC introduced in 1977. The AD572 was complete with internal clock, voltage reference, comparator, and input buffer amplifier. The SAR register was the popular 2504. The internal DAC was comprised of a 12-bit switch chip and an actively trimmed thin film ladder network (separately packaged as the two-chip AD562 DAC). The AD572 was the first military-approved 12-bit ADC processed to MIL-STD-883B, and specified over the full operating temperature range of –55°C to +125°C. A photograph of the AD572 is shown in Figure 1.38.

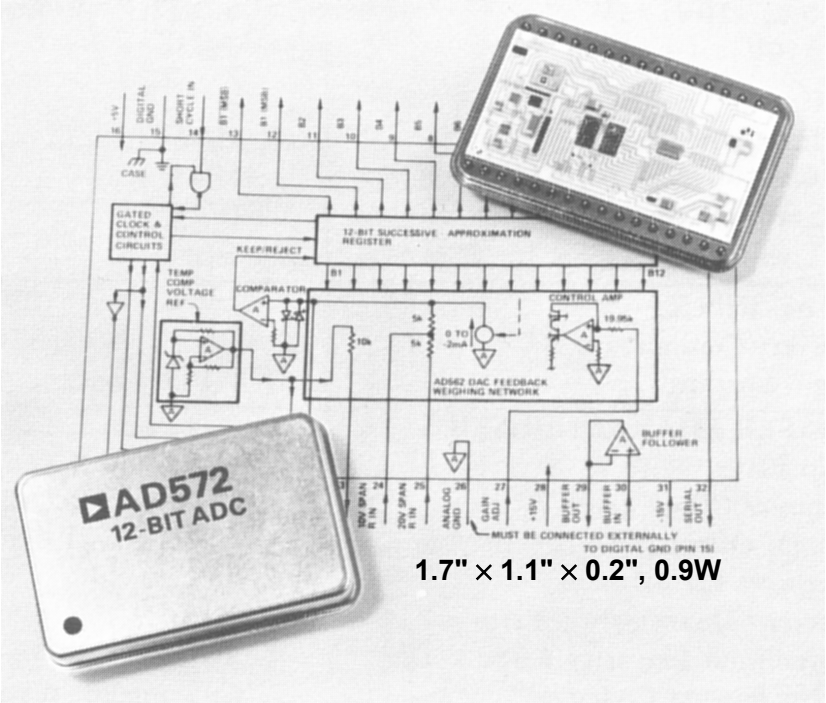


Figure 1.38: *AD572 12-Bit, 25-µs Mil-Approved Hybrid ADC, 1977*

Many hybrid circuits were introduced in the 1970s, and a few of the key ones are listed in Figure 1.39. Toward the end of the 1970s, Computer Labs, Inc., introduced a number of very fast hybrid data converters based on thick film laser trimmed resistor technology (Computer Labs was acquired by Analog Devices in 1978). The thick film resistor technology developed at Computer Labs during the 1970s was capable of 12-bit accuracy, which was quite remarkable, as most hybrid manufacturers used more expensive thin film resistors for 12-bit devices.

- **DAC80, 12-bit DAC, 1975**
- **ADC80, 12-bit, 25µs SAR ADC, 1975**
- **AD572, 12-bit, 25µs Mil-Approved ADC, 1977**
- **HDS-1250 12-bit, 35ns DAC (also 8-, 10-bit versions), 1979**
- **HAS-1202, 12-bit, 2.2µs SAR ADC (also 8-, 10-bit versions), 1979**
- **HTC-0300, 300ns SHA; HTS-0025, 25ns SHA, 1979**

Figure 1.39: *Hybrid ADC and DAC Milestones of the 1970s*

Both the HDS-series DACs and the HAS-series ADCs utilized actively trimmed thick film resistors and discrete PNP transistor switches for the internal DACs.

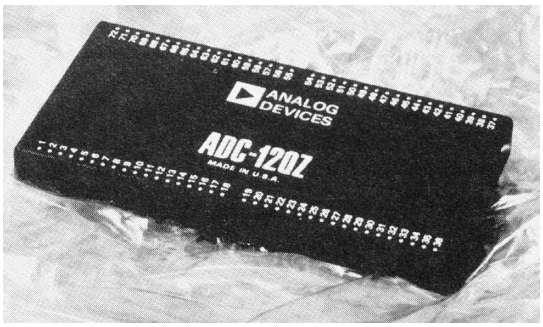
It should be noted at this point that none of the monolithic or hybrid ADCs of the 1970s were sampling ADCs with internal sample-and-holds (SHAs). In order to process ac signals, a separate SHA had to be connected to the ADC (with the appropriate interface

and timing circuits). This generated the need for hybrid SHAs, such as the HTC-0300 and the faster HTS-0025.

Modular Data Converters of the 1970s

Designers of modular data converters in the 1970s had even more flexibility than hybrid designers. In fact, modular technology began in the late 1960s before hybrids became popular, and still exists to this day for certain products. Figure 1.40 shows two of the early popular modular ADCs: the ADC-12QZ and the MAS-1202. The modular technology was quite straightforward—components were mounted on a small PC board and encapsulated in a potted module after trimming (usually done with manually selected resistors). The potting compound served to distribute the heat throughout the module, provided some degree of thermal tracking between critical components, and made it somewhat more difficult for competitors to reverse engineer the circuits.

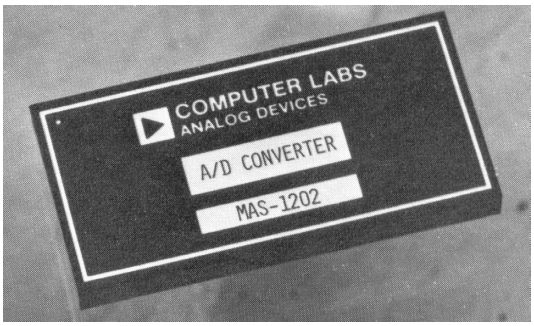
ADC-12QZ GENERAL PURPOSE 12-BIT, 40µs SAR ADC INTRODUCED IN 1972



2" × 4" × 0.4", 1.8W, $130.00

Quad-Switch, Thin-Film Network Internal DAC

MAS-1202 12-BIT, 2µs SAR ADC INTRODUCED IN 1975



2" × 4" × 0.4", 2.4W, $270.00

Discrete PNP-Transistor Internal DAC, Manually Selected Precision Resistors

Figure 1.40: *Early Modular ADCs of the 1970s*

The ADC-12QZ 12-bit, 40-µs SAR ADC was introduced by Analog Devices in 1972, an outgrowth of the Pastoriza Electronics' early converter product line acquired in 1969. The ADC-12QZ utilized a DAC made up of three "quad switch" building blocks previously discussed and a matching pre-trimmed thin film resistor network. A SAR logic chip, comparator, a reference, and miscellaneous other components completed the parts list.

The MAS-1202 12-bit, 2-µs SAR ADC designed at Computer Labs, Inc., was released in 1975 and utilized an internal DAC based on fast PNP transistor switches and manually-selected precision resistors.

The ADC-12QZ and the MAS-1202 each dissipated approximately 2 W, and commanded premium prices of $130.00 and $270.00, respectively.

One of the first complete modular *sampling* ADCs of the 1970s utilized an open-card construction with a combination of hybrid, IC, and discrete building blocks. The MOD-815 8-bit, 15-MSPS ADC was introduced by Computer Labs in 1976. The design

utilized two 4-bit flash converters in a subranging architecture (see Chapter 3 of this book). Each 4-bit flash converter was constructed of 8 dual AM687 ECL comparators. The MOD-815 was one of the first commercial ADCs used in the rapidly emerging field of digital television.

Other popular card-level modules included the MOD-1205 12-bit, 5-MSPS ADC and the MOD-1020 10-bit, 20-MSPS ADC introduced by Analog Devices/Computer Labs in 1979. These products made use of the first flash converters on the market: the Advanced Micro Devices' AM6688 4-bit, 100-MSPS flash and the TRW TDC-1007J (8-bit) and TDC-1014J (6-bit) flash converters. Figure 1.41 shows a photo of the MOD-1020 with the key devices labeled. The architecture was subranging, with two "stacked" AM6688s providing the first 5-bit conversion, and the 6-bit TDC-1014J the second 6-bit conversion. The extra bit was used for error correction. The MOD-1020 utilized quite a bit of ECL logic and dissipated a total of 21 W. Due to the high level of performance and the large number of costly hybrid and IC building blocks, the MOD-1020 commanded a premium price of $3,500.00.

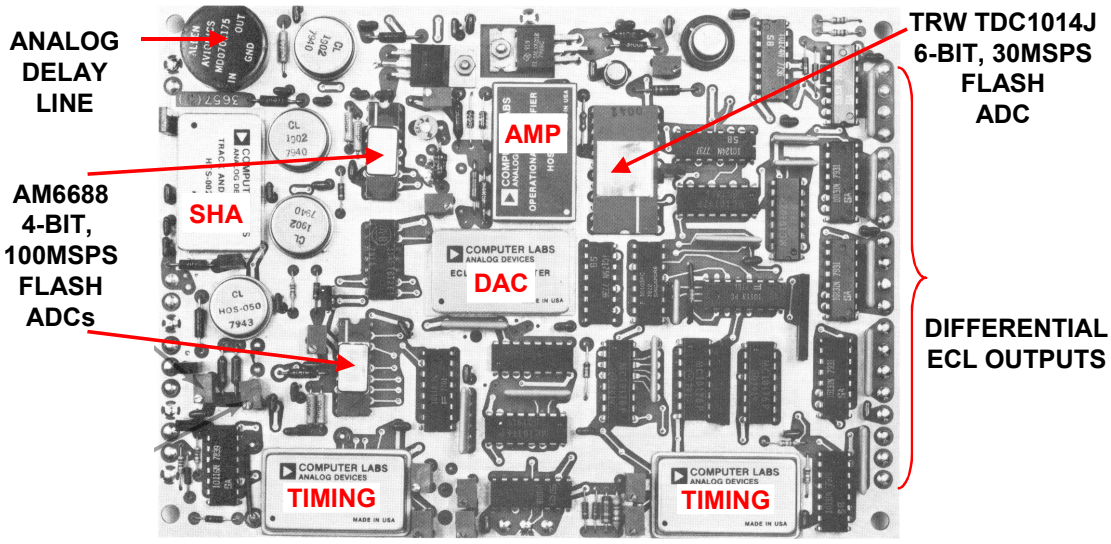


Figure 1.41: *MOD-1020, 10-Bit, 20-MSPS Sampling ADC Introduced in 1979*

Starting in the mid-1970s, most of the modular sampling converters were tested using FFT techniques to measure SNR, ENOB, and distortion. (See Chapter 5 of this book, *Testing Data Converters*).

A summary of some of the popular modular ADCs and DACs of the 1970s is given in Figure 1.42.

- **DAC-12QZ, 12-bit DAC, 1970**
- **ADC-12QZ, 12-bit, 40µs SAR ADC, 1972**
- **MAS-1202, 12-bit, 2µs SAR ADC (also 8- 10-bit versions) 1975**
- **ADC1130, 14-bit, 12µs SAR ADC, 1975**
- **MDS-1250, 12-bit, 50ns DAC, (also 8-, 10-bit versions) 1975**
- **THS-0300, 300ns SHA; THS-0025, 25ns SHA, 1975**
- **MOD-815, 8-bit, 15MSPS Video, *sampling* ADC, 1976**
- **SDC1700, Synchro-to-Digital Converter, 1977**
- **DAC1138, 18-bit DAC, (most accurate DAC for 10 years), 1977**
- **MOD-1205, 12-bit, 5MSPS, *sampling* ADC, 1979**
- **MOD-1020, 10-bit, 20MSPS, *sampling* ADC, 1979**

Figure 1.42: *Modular ADC and DAC Milestones of the 1970s*

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NOTES:

SECTION 1.4: DATA CONVERTERS OF THE 1980s

Walt Kester

Introduction

The 1980s represented high growth years for both IC, hybrid, and modular data converters. The driving market forces were instrumentation, data acquisition, medical imaging, professional and consumer audio/video, computer graphics, and a host of others. The increased availability of relatively low-cost microprocessors, high-speed memory, DSPs, and the emergence of the IBM-compatible PC increased the interest in all areas of signal processing. The emphasis in ADCs began to rapidly shift to include ac-performance and wide dynamic range; and hence, a great demand for *sampling* ADCs at all frequencies. Specifications such as signal-to-noise ratio (SNR), signal-to-noise and distortion (SINAD), effective number of bits (ENOB), noise power ratio (NPR), spurious free dynamic range (SFDR), aperture time jitter, etc., began to appear on most ADC data sheets; and glitch impulse area, SFDR, etc., on DAC data sheets.

There was a proliferation of high-speed bipolar and CMOS flash ADCs in the 1980s, with 4-, 6-, 8-, 9-, and 10-bit at sampling rates from 20 MSPS to 100 MSPS. Digital video was a chief driving force for the 8-, 9-, and 10-bit devices. In the graphics display area, high-speed video RAM-DACs emerged, with CMOS being the ideal process for these memory-intensive devices.

Voiceband and audio signal processing led to the demand for 16- and 18-bit ADCs and DACs, and the emergence of the compact disk (CD) player fueled the need for low-cost audio DACs.

In the 1980s, general purpose ADCs and DACs began to offer more resolution, more functionality, and more complete solutions to the problems of data acquisition and distribution, including multichannel ADCs and DACs. The development of linear-compatible CMOS processes (such as the Analog Devices' LC^{2}MOS and BiCMOS II in the mid-1980s) allowed data converter designers to provide more functionality by the addition of features such as on-chip voltage references and buffer amplifiers, for example.

Another important process development in the mid-1980s was the introduction of Analog Devices' first-generation complementary bipolar (CB) process, which offered high-speed, high-performance matching PNP and NPN transistors. The high-speed op amps produced on the CB process made excellent drivers for many of the new ADCs, and the CB process eventually yielded some extremely high performance IF-sampling ADCs in the 1990s. Refer to Chapter 4 of this book, *Data Converter Process Technology*, for more discussion regarding this topic.

Monolithic DACs of the 1980s

A listing of key IC DAC product introductions during the 1980s is shown in Figure 1.43. Rather than discuss each one individually, we will simply point out examples which illustrate the general trends in the product line.

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- **AD558, 8-bit, 1µs, *µP compatible*, *voltage output*, Bipolar/I²L DAC, 1980**
- **AD7528, *Dual* 8-bit, *buffered*,CMOS MDAC, 1981**
- **AD7546, *16-bit*, *segmented*, CMOS voltage mode DAC (required external amps), 1982**
- **AD7545, *Buffered*,12-bit CMOS MDAC, 1982**
- **AD390, *Quad* 12-bit voltage output DAC (compound monolithic), 1982**
- **AD7240, *12-bit*, *voltage mode*, CMOS DAC, 1983**
- **AD7226, *Quad* 8-bit, *double-buffered*, *voltage output*, *LC²MOS* DAC, 1984**
- **AD9700, 125MSPS, 8-bit *Video* ECL DAC, 1984**
- **AD7535, *14-bit*, double-buffered LC²MOS MDAC, 1985**
- **AD569, *16-bit*, *segmented*, double-buffered voltage output, *BiCMOS* DAC, 1986**
- **AD7245, 12-bit, double-buffered, voltage output, LC²MOS DAC, *with reference*, 1987**
- **AD1856/AD1860, 16-/18-bit *audio* BiCMOS DACs for CD players, 1988**
- **ADV453/ADV471/ADV476/ADV478 CMOS *Video RAM-DACs*, 1988**
- **AD7840, *14-bit*, double-buffered, voltage output, LC²MOS DAC, *with reference*, 1989**
- **AD7846, *16-bit*, *segmented*, *voltage output*, LC²MOS DAC, 1989**

Figure 1.43: *Monolithic DACs of the 1980s*

The AD558 8-bit, 1-µs CMOS DAC introduced in 1980 illustrates the trend toward microprocessor compatible interfaces, which are almost universal today for general-purpose DACs and ADCs. Later products would utilize double-buffered digital inputs, where an input register accepted parallel, serial, or byte-wide data, and a second parallel latch was used to actually update the DAC switches.

The AD7546, although requiring two external op amps to perform the complete 16-bit DAC function, illustrates the trend toward higher resolution. The segmented architecture used in the AD7546 was later utilized in the 16-bit AD569, which integrated the entire function onto one chip.

The introduction of multiple DACs in the same package is illustrated by the dual AD7528, the quad AD390 (compound monolithic), and the quad AD7226 (single-chip).

The initial CMOS DACs were current-output, requiring an external op amp to perform the current-to-voltage conversion; but with the advent of LC²MOS and BiCMOS processes, a number of DACs provided voltage-output capability. These same processes also allowed the integration of the voltage reference on-chip, thereby providing a more complete solution.

Audio and video monolithic DACs began to appear in the mid 1980s. The AD1856/AD1860 16-/18-bit audio DACs were targeted toward the emerging compact disk (CD) player market. The AD9700 DAC, introduced in 1984, was the first monolithic IC DAC designed for raster scan graphics applications which allowed the *sync*, *blanking*, *10% white*, and *reference white* levels to be set with separate internal switches. This allowed the full 8-bit range to be dedicated to the *active* video region. The AD9700 was based on the HDG-series of hybrid DACs previously introduced in 1980. The AD9700

would later be replaced by the ADV-series of CMOS video RAM-DACs which included on-chip color palette memory as well as the basic DAC function.

Monolithic ADCs of the 1980s

The two-chip AD574, introduced in 1978, was well on its way to becoming an industry standard converter by the time of the introduction of the single-chip AD574 12-bit, 35-µs SAR ADC in 1985. Since that time, this converter did become an industry standard, and is still in production today.

Figure 1.44 lists some of the important monolithic ADCs introduced during the 1980s. It is interesting to note the emergence of the *sampling* monolithic ADC starting in the mid-1980s. The addition of sample-and-holds, references, and buffer amplifiers was made considerably easier with the addition of bipolar capability to the CMOS process (LC^2MOS and BiCMOS). Another trend which emerged was the addition of front-end multiplexers to the basic ADC, as in the case of the 4-channel AD7582 in 1984, thereby providing a more complete data acquisition solution.

Although the basic Σ-Δ ADC architecture had been well known since the 1950s and 1960s, the first actual commercial offering of a monolithic Σ-Δ ADC was in 1988 by Crystal Semiconductor (CSZ5316). The device had 16-bit resolution and an effective throughput rate of 20 kSPS, making it suitable for voiceband digitization. The digital audio market (both professional and consumer) generated a demand for Σ-Δ ADCs with higher throughput rates and greater resolution; and the precision measurement market required 20^+ bit resolution, although at much lower throughput rates. Both these needs would be addressed during the 1990s by an explosion of ADCs and DACs using the Σ-Δ architecture.

- **AD574, 12-bit, 35µs, industry-standard, single-chip ADC, 1985**
- **AD673, 8-bit, complete ADC, 1983**
- **AD7582, *4-channel* muxed input 12-bit CMOS ADC, 1984**
- **AD670, 8-bit, 10µs ADCPORT, 1984**
- **AD7820, 8-bit, 1.36µs half-flash, *sampling* ADC, 1985**
- **AD7572, 12-bit, 5µs SAR LC^2MOS ADC with reference, 1986**
- **AD7575, 8-bit, 5µs SAR LC^2MOS *sampling* ADC, 1986**
- **AD7579, 10-bit, 50kSPS, LC^2MOS SAR *sampling* ADC with AC specs, 1987**
- **AD7821, 8-bit, 1MSPS half-flash *sampling* ADC with AC specs, 1988**
- **AD674, 12-bit,15µs ADC, 1988**
- **AD7870, 12-bit, 100kSPS LC^2MOS SAR *sampling* ADC with AC specs, 1989**
- **AD7871, 14-bit, 83kSPS LC^2MOS SAR *sampling* ADC with AC specs, 1989**

- **First commercial 16-bit *sigma-delta* ADC, Crystal Semiconductor, 1988**

Figure 1.44: *Monolithic ADCs of the 1980s*

Monolithic Flash ADCs of the 1980s

As previously mentioned, the rapidly growing digital video market, coupled with the introduction of the TRW TDC-1007J 8-bit, 30-MSPS flash ADC in 1979, spurred many IC manufacturers to develop similar, but lower powered flash ADCs with resolutions ranging from 4- to 10-bits, and sampling rates as high as high as 500 MSPS. Most, but certainly not all, are listed in Figure 1.45 which covers the period from approximately 1979 to 1990, the peak years for flash converters.

- **TDC1007J, 8-bit, 30MSPS, (TRW, LSI), 1979**
- **TDC1016J, 6-bit, 30MSPS, (TRW, LSI), 1979**
- **AM6688, 4-bit, 100MSPS, (AMD), 1979**
- **SDA6020, 6-bit, 50MSPS, (Siemens) 1980**
- **TLM1070, 7-bit, 20MSPS, CMOS (Telmos), 1982**
- **MP7684, 8-bit, 20MSPS, CMOS (Micro Power), 1983**
- **TDC1048, 8-bit, 30MSPS, (TRW, LSI), 1983**
- **AD9000, 6-bit, 75MSPS, 1984**
- **AD9002, 8-bit, 150MSPS, 1987**
- **AD770, 8-bit, 200MSPS, 1988**
- **AD9048, 8-bit, 35MSPS, 1988**
- **AD9006/AD9016, 6-bit, 500MSPS, 1989**
- **AD9012, 8-bit, 100MSPS, TTL, 1988**
- **AD9028/AD9038 8-bit, 300MSPS, 1989**
- **AD9020, 10-bit, 60MSPS, 1990**
- **AD9058, Dual 8-bit, 50MSPS, 1990**
- **AD9060, 10-bit, 75MSPS, 1990**

Figure 1.45: *Monolithic Flash ADCs of the 1980s*

Both bipolar and CMOS technology was used to produce these devices, with the CMOS converters offering lower power, but at the expense of somewhat inferior performance—especially in the early offerings. The chief problem with the early CMOS flash converters were error codes known as "sparkle codes" produced by comparator metastability (see *Data Converter Architectures*, Chapter 3 for details). The bipolar process comparator designs were less susceptible because they typically had much higher regenerative gain. Today, these metastability problems have largely been overcome in CMOS devices designed on submicron processes; however, they still may occur if care is not taken in the design.

Although bipolar and CMOS flash converter designs were used in most of the 6- to 10-bit video ADCs of the 1980s, the lower power subranging and pipelined architectures became prevalent in the 1990s, as ADC designers gained experience with faster CMOS and BiCMOS processes. Today, the flash converter architecture is widely used as a building block within pipelined ADCs. There are, however, a few GaAs flash converters

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of 6- or 8-bits resolutions which serve the relatively niche markets requiring sampling rates of 1 GSPS or greater.

Hybrid and Modular DACs and ADCs of the 1980s

The demand for hybrid and modular DACs and ADCs peaked in the 1980s, primarily because of the 3- to 5-year lead time hybrids and modules held compared to single-chip monolithic converters with equivalent performance. In addition, the large number of flash converters and other components served as building blocks for higher resolution subranging ADCs. Some examples of important hybrid and modular data converters introduced in the 1980s are shown in Figure 1.46.

- **Hybrids:**
  - **HDS-1240E, 12-bit, 40ns ECL DAC, 1980**
  - **HDG-Series, 4-, 6-, 8-bit, 5ns *video* ECL DACs, 1980**
  - **HAS-1409, 14-bit, 1.25MSPS *sampling* ADC, 1983**
  - **HAS-1201, 12-bit, 1MSPS *sampling* ADC, 1984**
  - **AD376, 16-bit, 20µs SAR ADC, 1985**
  - **AD1332, 12-bit, 125kSPS *sampling* ADC with 32-word FIFO, 1988**
  - **AD9003, 12-bit, 1MSPS *sampling* ADC, 1988**
  - **AD9005, 12-bit, 10MSPS *sampling* ADC, 1988**
  - **AD1377, 16-bit, 10µs SAR ADC, 1989**
- **Modules:**
  - **ADC1140, 16-bit, 35µs SAR ADC, 1982**
  - **CAV-1220, 12-bit, 20MSPS *sampling* ADC, 1986**
  - **CAV-1040, 10-bit, 40MSPS *sampling* ADC, 1986**
  - **AD1175, *22-bit integrating* ADC, 1987**

Figure 1.46: *High Performance Hybrid and Modular DACs and ADCs of the 1980s*

An interesting thick film hybrid family, introduced by Analog Devices in 1980, was the HDG-series 4-, 6-, and 8-bit video ECL DACs. Designed for raster scan RGB graphics displays, these DACs had an 8-bit settling time of approximately 5 ns. In addition to fast settling, these were among the first video DACs to allow the *sync*, *blanking*, *10% white*, and *reference white* levels to be set with separate internal switches. This allowed the full 8-bit DAC range to be dedicated to the *active video* region. The HDG-series was a precursor to the fully monolithic CMOS video DACs and RAM-DACs which were introduced later in the 1980s (ADV-series in Figure 1.43).

High performance hybrid subranging ADCs also appeared during the 1980s, most utilizing high speed flash converters as internal building blocks. Most were *sampling*

devices, complete with ac specifications, culminating in the 12-bit 10-MSPS AD9005 introduced in 1988.

Hybrids of the 1980s also achieved resolutions not yet attainable in monolithic technology, such as the AD1377 16-bit, 10-µs SAR ADC introduced in 1989.

Also worthy of notice were several modules introduced in the 1980s which also pushed the speed and resolution envelope. The CAV-1220 12-bit, 20-MSPS ADC and the CAV-1040 10-bit, 40-MSPS ADC introduced in 1986 set new standards in high-speed dynamic range performance, while the AD1175 22-bit integrating ADC set the standard for high resolution when it was introduced in 1987.

SECTION 1.5: DATA CONVERTERS OF THE 1990s

Walt Kester

Introduction

The markets influencing data converters in the 1990s were even more diverse and demanding than those of the 1980s. Some of the major applications were industrial process control, measurement, instrumentation, medical imaging, audio, video, and computer graphics. In addition, communications became an even bigger driving force for low-cost, low-power, high-performance data converters in modems, cell phone handsets, and wireless infrastructure (basestations).

Other trends were the emphasis on lower power and single-supply voltages for portable battery-powered applications. While the reduced supply voltages were compatible with the higher speed, lower voltage processes, the reduced signal range and headroom made the converter designs more sensitive to noise. Packaging trends also changed in the 1990s from the traditional DIP to smaller surface mount packages suitable for high-volume automatic mass-assembly manufacturing techniques. These included both leaded types and non-leaded types such as ball grid array (BGA) and chip-scale packages (CSP).

Even in the general purpose data converter market, there was a demand for more analog and digital functionality, such as putting an entire data acquisition system on a chip including the input multiplexer, programmable gain amplifier (PGA), sample-and-hold, and the ADC function. Many applications required both the ADC and DAC function; and this led to the integration of both on a single chip, called a coder-decoder, or CODEC. Specially designed analog front ends (AFEs) and mixed-signal front ends (MxFE™) were included with the basic ADC function in applications such as CCD image processors and IF sampling receivers.

In the TxDAC® family, digital functions such as interpolation filters and digital modulators were integrated with a high-speed, low-distortion CMOS DAC core. Data converter designers made more use of "core" designs to yield several products with various options, such as serial or parallel output parts, etc. The TxDAC-series is a good illustration of the application of this concept, where a variety of resolutions, update rates, and internal digital processing are offered across a broad number of individual products, all of which use essentially the same DAC core.

Because of the increase in frequency-domain signal processing applications, there was even greater emphasis on dynamic range and ac performance in practically all data converters, and a large number of monolithic *sampling* ADCs were introduced to meet the demand. The pipelined subranging architecture virtually replaced the higher power flash ADCs of the 1980s, and some of the key ac specifications were SNR, SINAD, ENOB, and SFDR.

In the 1990s, CMOS became the process-of-choice for general-purpose data converters, with BiCMOS reserved for the high-end devices. In a few cases, high-speed complementary bipolar processes were utilized for ultra high performance data converters. CMOS is also the ideal process for the Σ-Δ architecture, which became the

topology of choice for ADCs and DACs used in voiceband and audio applications, as well as in higher resolution, low frequency measurement converters.

A major process technology shift occurred in the 1990s, when parasitics ultimately became the performance-limiting factor for high-speed chip-and-wire hybrid data converters. The newer ICs, with their smaller feature size and reduced parasitics, allowed them to achieve higher levels of performance than attainable in a chip-and-wire hybrid or a module—a reversal of the situation that existed throughout the 1970s and most of the 1980s.

In the following sections, we will examine the data converter trends of the 1990s and 2000s, using a few example products as illustrations. It would be impossible to cover the individual products in as much detail as we did for the 1970s and 1980s, simply because of the large number of individual data converters introductions in the 1990s. Many of these products are discussed in Chapter 8 of this book, *Data Converter Applications*.

Monolithic DACs of the 1990s

A significant trend in general purpose DACs of the 1990s was toward more functionality in all areas, especially with respect to the input structure. DACs were designed specifically to handle parallel, serial, and byte-wide loading, and the inputs were generally double-buffered. The serial interface became popular for interfacing to microprocessors and DSPs. In many cases, the same core DAC design was utilized to provide these various options as separate products in the appropriate packages. Obviously, this required the introduction of many individual DAC products to cover all the desired options.

A variety of options existed with respect to the output structure also. Audio and video DACs tended to use current outputs, while some of the more general-purpose DACs offered either current or voltage output options.

The trend toward multiple DACs is illustrated by an early example of an octal DAC, the AD7568 12-bit LC^{2}MOS DAC shown in Figure 1.47, introduced in 1991. This DAC utilized the popular multiplying architecture and provided current outputs designed to drive an op amp connected as an I/V converter. Notice that the DAC is double buffered—the input shift register accepts the serial input data and loads it into the appropriate input latch, and asserting $\overline{\text{LDAC}}$ simultaneously latches the data into the eight parallel individual DAC latches.

Consumer audio compact disk players spurred the market for low distortion 16+ bit DACs in the late 1980s, and the first audio DACs were parallel linear DACs capable of oversampling at rates of 8 times or 16 times the basic CD update rate of 44.1 kSPS. Resolutions ranged from 16-bits with the early audio DACs to 18 and 20 bits with later versions. For example, the AD1865 dual 18-bit stereo DAC was introduced in 1991 and was capable of 16-times oversampling.

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By the mid-1990s, the Σ-Δ architecture began to replace the parallel DACs in audio applications. Sigma-delta offered much higher oversampling ratios, thereby relaxing output filter requirements, as well as provided higher dynamic range with lower distortion. Some early offerings were the AD1857, AD1858, and AD1859 introduced in 1996. These DACs offered resolutions ranging from 16 bits to 20 bits, used serial interfaces, and were single-supply devices.

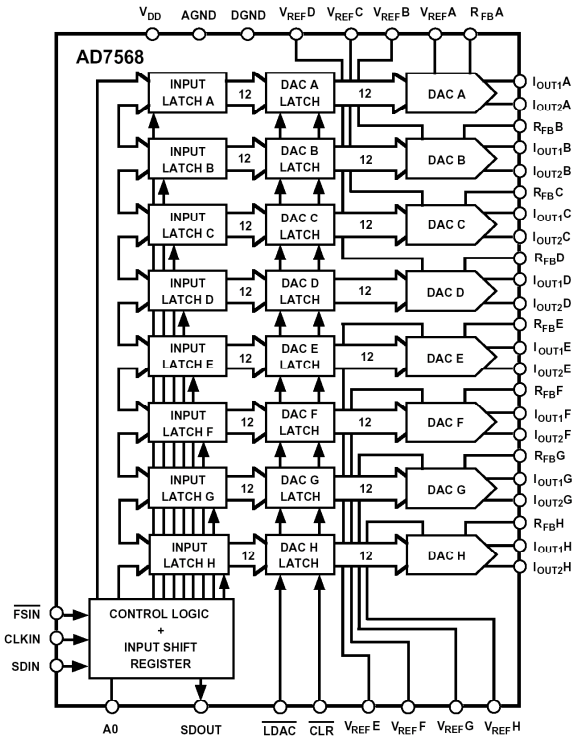

Figure 1.47: *AD7568 Octal 12-Bit LC^{2}MOS MDAC, 1991*

Although there were a few bipolar process high speed ECL DACs introduced in the early 1990s, such as the AD9712 12-bit, 100-MSPS DAC and the AD9720 10-bit, 400-MSPS DAC, the majority of video and communications DACs were low-power, low-glitch, low-distortion CMOS devices. The ADV-series of video CMOS RAM-DACs continued to expand during the 1990s, and an entire family of 8-, 10-, 12-, 14-, and 16-bit transmit-DACs (TxDAC®) for communications was started in 1996, with new introductions continuing to this day (AD976x, AD977x, and AD978x-series).

Direct digital synthesis (DDS) systems on a single chip emerged in the 1990s, largely because of the relative ease with which digital logic could be added to a high performance CMOS DAC core. The first of these was the AD7008, 10-bit, 50-MSPS DDS introduced in 1993 (see Figure 1.48). This was soon followed by additional offerings, such as the 10-bit, 125-MSPS AD9850 in 1996. Later DDS systems added phase and frequency modulation capability, on-chip clock multipliers, more resolution, and update rates as high as 1 GHz.

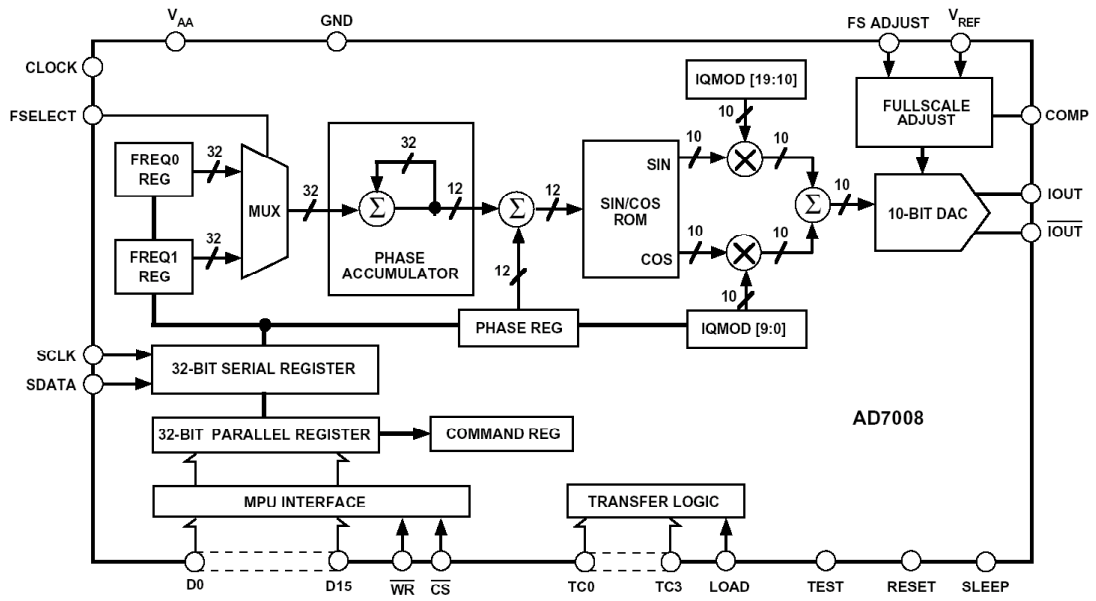

Figure 1.48: *AD7008 10-Bit, 50-MSPS Complete CMOS DDS, 1993*

The *digital potentiometer*, another highly popular component today, had its origins in 1989 with the release of the AD8800 TrimDAC®, the first in a series. The TrimDACs were basically 8-bit voltage-output DACs designed and optimized to replace mechanical potentiometers. The TrimDAC family became popular, and in 1995, the first DigiPOTs® were introduced. The basic concept behind the digital pot was simply to use a CMOS "string DAC" as a variable resistor. The AD8402 2-channel (8-bits), AD8403 4-channel (8-bits) were the first offerings in 1995. Since then the product line has been expanded to include many more products including some with non-volatile memory (AD51xx and AD52xx series).

Figure 1.49 summarizes some of the key DAC developments during the 1990s.

- **Multiple DACs: AD7568, 12-bit octal single +5V supply CMOS MDAC, 1991**
- **Audio DACs**
  - **Parallel 8×, 16× oversampling, early 1990s**
  - **Sigma-delta, starting with the AD1857, AD1858, AD1859 in 1996**
- **Video RAM-DACs-continued expansion of product line**
- **Transmit DACs (TxDACs) for communications, 1996**
- **Direct Digital Synthesis (DDS) Systems, AD9008, 1993**
- **TrimDACs, 1989**
- **Digital potentiometers, 1995**

Figure 1.49: *Summary: Monolithic DACs of the 1990s*

Monolithic ADCs of the 1990s

During the decade of the 1990s, monolithic ADC performance overtook that of modular and hybrid converters, primarily because of the greatly reduced parasitics in the new IC processes. The AD1674 12-bit, 100-kSPS sampling SAR ADC introduced in 1990 was pin-compatible with the industry-standard AD574 introduced a decade earlier. A simplified block diagram of the AD1674 is shown in Figure 1.50. This represented a trend toward sampling ADCs that was to continue throughout the 1990s, because of the increased interest in the digital processing of ac signals.

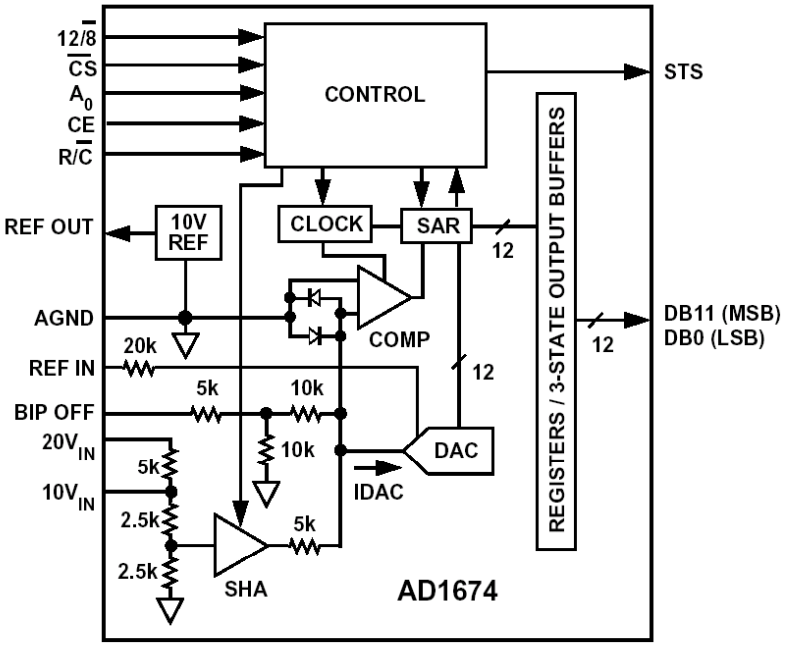

Figure 1.50: *AD1674, 12-Bit, 100-kSPS Sampling ADC (AD574 Pin-Compatible), 1990*

Progress was also being made in CMOS sampling ADCs, as illustrated by the introduction of the AD7880 12-bit, 66-kSPS ADC in 1990. A simplified block diagram is shown in Figure 1.51. Although the AD7880 required an external reference, it still represented a breakthrough because of its low power (25 mW) and single +5-V operation.

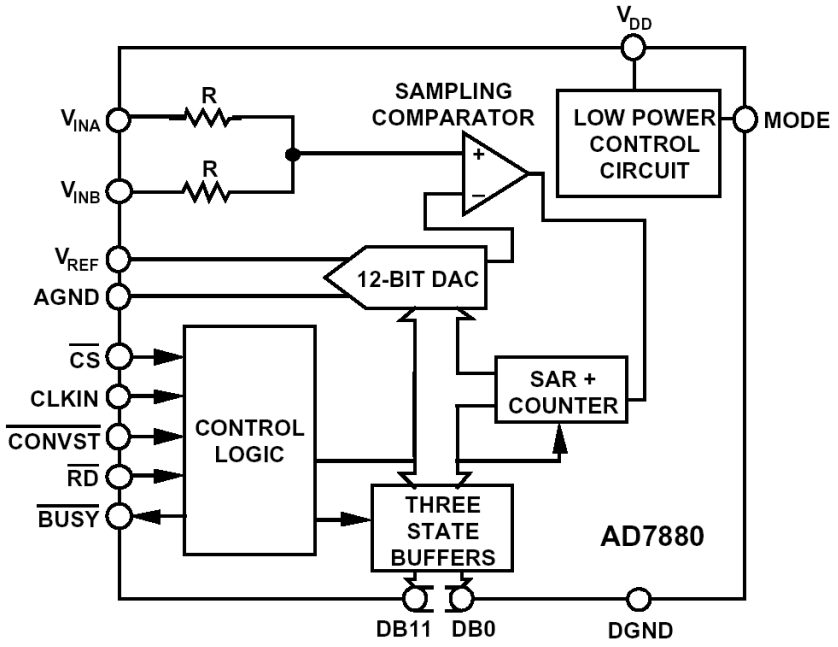

Figure 1.51: *AD7880 12-Bit, 66-kSPS, Single +5 V, LC²MOS Sampling SAR ADC, 1990*

In 1992, the 12-bit, 1.25-MSPS AD1671 BiCMOS sampling ADC was introduced. The basic subranging pipelined architecture utilized in the AD1671 was based on a previous non-sampling version, the 2-MSPS AD671, which had been introduced in 1990. A simplified block diagram of the AD1671 is shown in Figure 1.52.

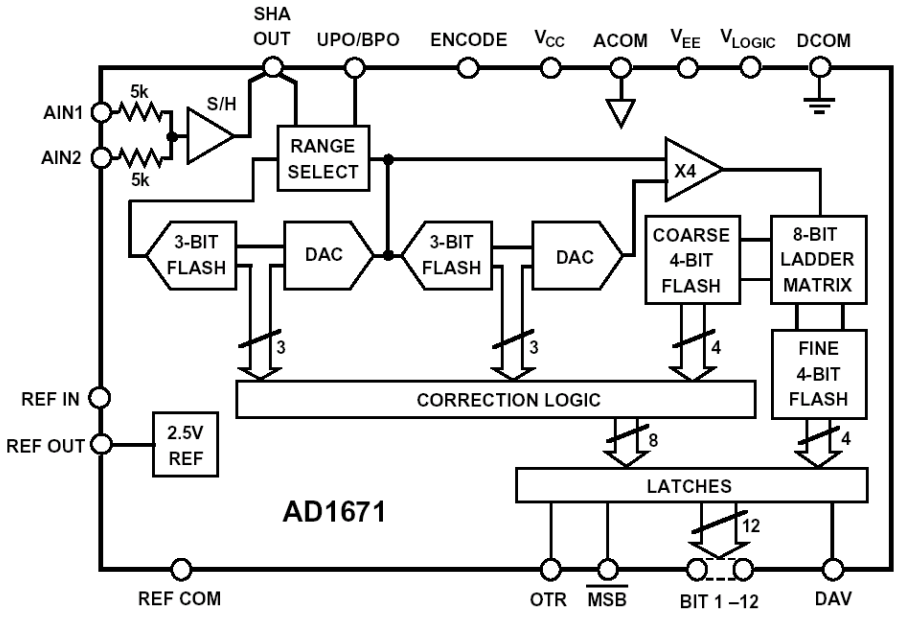

Figure 1.52: *AD1671 12-Bit, 1.25-MSPS Sampling BiCMOS ADC, 1992*

A significant breakthrough in speed and performance was also achieved in 1992 with the release of the AD872 12-bit, 10-MSPS BiCMOS sampling ADC, shown in Figure 1.53. This ADC also used the pipelined architecture with error correction.

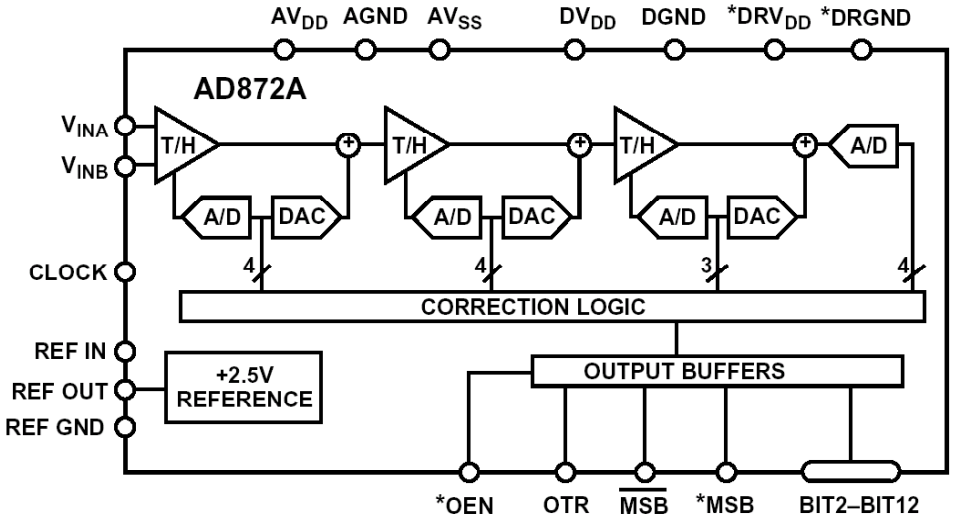

Figure 1.53: *AD872 12-Bit 10-MSPS BiCMOS Sampling ADC, 1992*

In 1996, three single supply (+5 V) CMOS ADCs were released using an architecture similar to the 12-bit AD872: the AD9220 (10 MSPS), the AD9221 (1 MSPS), and AD9223 (3 MSPS). All three parts utilized the same basic design, with the operating current scaled to yield the three sampling rate options. Power dissipation for the three devices is 250 mW (AD9220, 10 MSPS), 60 mW (AD9221, 1 MSPS), and 100 mW (AD9223, 3 MSPS).

A true breakthrough in wide dynamic range IF-sampling ADCs occurred in 1995 with the release of the 12-bit, 41-MSPS AD9042. A functional diagram of the AD9042 is shown in Figure 1.54. This converter was the first to achieve greater than 80-dB SFDR for signals over a 20-MHz Nyquist bandwidth. It was fabricated on the Analog Devices' XFCB high-speed complementary bipolar process.

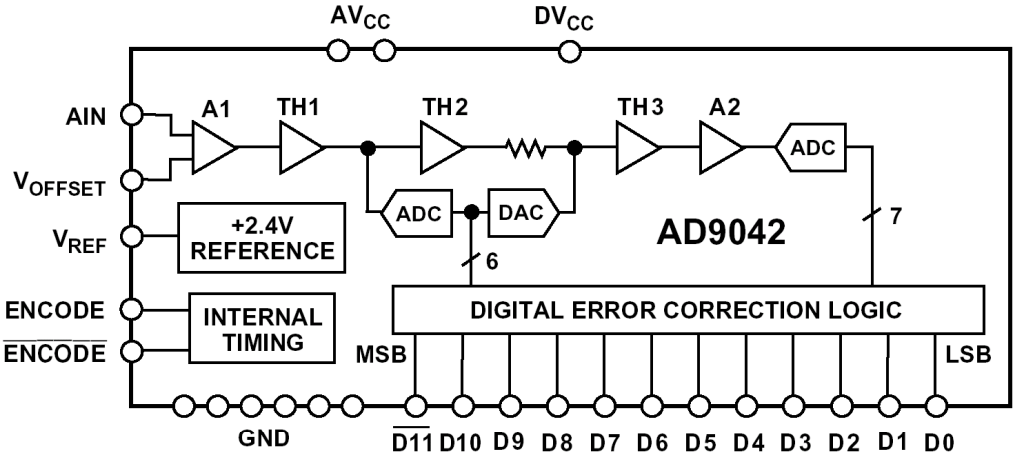

Figure 1.54: *AD9042 12-Bit 41-MSPS XFCB, Sampling ADC,1995*

The concept of a complete data acquisition system on a chip saw fruition in the 1990s with the introduction of the AD789x-series of LC^{2}MOS SAR single-supply (+5 V) ADCs in 1993. These parts offer up to 8 channels of multiplexed inputs and sampling rates of 100 kSPS to 600 kSPS. In order to accommodate the more traditional industry-standard bipolar inputs of ±10 V and ±5 V, the series provides input thin film resistor attenuators/level shifters to match the input range of the internal SAR ADCs.

A significant technology change occurred in the 1990s, when the high-power 8- , 9-, and 10-bit flash converters of the 1980s were gradually replaced by lower power pipelined and folding architectures. This was typified by the introduction of the AD9054 8-bit, 200-MSPS ADC in 1997. The AD9054 utilized a unique architecture consisting of five folding stages followed by a 3-bit parallel flash stage.

CMOS Σ-Δ ADCs became the architecture of choice for measurement, voiceband, and audio ADCs beginning in the early 1990s. The AD7001 was the first GSM baseband converter and was introduced in 1990. Sigma-delta was utilized in many other voiceband and audio converters as well as high-resolution measurement ADCs. The AD771x-family of 24-bit measurement converters was introduced in 1992.

These converters include on-chip multiplexers and PGAs and are designed for direct interfacing to many sensors, such as thermocouples, bridges, RTDs, etc. A significant product in the family is the AD7730, introduced in 1997, which allows a load cell output with a 10-mV fullscale voltage to be digitized to over 80,000 noise-free codes (16.5 bits). A simplified block diagram of the AD7730 is shown in Figure 1.55.

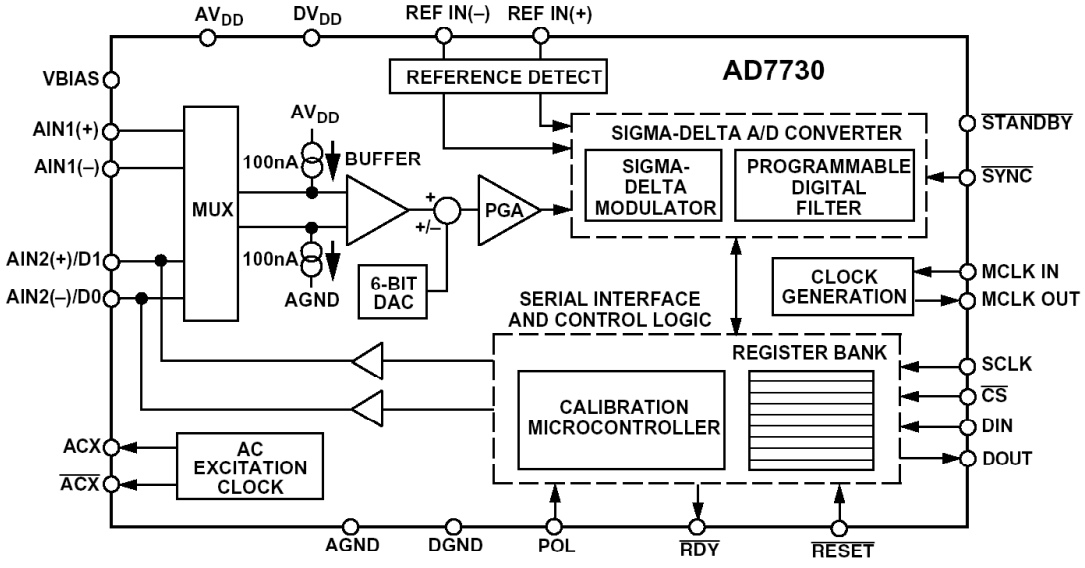

Figure 1.55: *AD7730 24-Bit Signal-Conditioning Σ-Δ ADC, 1997*

Another application of Σ-Δ technology appeared in the late 1990s, with the introduction of the ADE775x-series of energy metering ICs. These parts measure the instantaneous current and voltage of the power mains and calculate power usage, thereby replacing mechanical devices.

A summary of key monolithic ADCs of the 1990s is given in Figure 1.56.

- **AD1674, 12-bit, 100kSPS, sampling ADC, AD574A pin-compatible, 1990**
- **AD7880, 12-bit, 66kSPS LC²MOS sampling ADC, 1990**
- **AD7001, CMOS GSM baseband converter, 1990**
- **AD771x-series 24-bit Σ-Δ measurement ADCs, 1992**
- **AD1671, 12-bit, 1.25MSPS BiCMOS sampling ADC, 1992**
- **AD872, 12-bit, 10MSPS BiCMOS sampling ADC, 1992**
- **AD9220/AD9221/AD9223, 12-bit, 10/1/3 MSPS, CMOS sampling ADCs, 1996**
- **AD9042, 12-bit, 41MSPS sampling ADC, 80dB SFDR, 1995**
- **AD7730, 24-bit bridge transducer measurement ADC, 1997**
- **AD9054, 8-bit, 200MSPS sampling ADC, 1997**
- **ADuC812 MicroConverter® (precision ADCs, DACs, 8051-core, flash memory, 1999**

Figure 1.56: *Summary: Monolithic ADCs of the 1990s*

Because of the ease with which digital functionality can be added to BiCMOS or CMOS ADCs and DACs, there have been an increasing number of highly integrated application-specific integrated circuits during the 1990s and continuing to this day. A few of the important areas served by these chips are listed in Figure 1.57. Most have already been mentioned in this chapter, and are covered throughout this book, especially in Chapter 8.

An important development occurred in 1999 with the introduction of the first Analog Devices' *precision analog microcontroller*, the ADuC812 MicroConverter®. The MicroConverter includes not only precision signal conditioning circuitry (ADCs, DACs, multiplexers, etc.) but also flash memory and an 8051-based microprocessor core. Later MicroConverter products have included higher resolution Σ-Δ ADCs (see Chapter 8 of this book). This level of integration represents an optimum solution for many general-purpose sensor conditioning and signal processing applications.

- **Voiceband codecs**
- **Audio codecs**
- **AC'97 SoundMAX® computer audio codecs**
- **I/O Ports**
- **Mixed signal front ends: modems, communications, CCD imaging, flat panel displays**
- **Transmit and receive signal processors**
- **Direct conversion (Othello® radio) chipsets**
- **Direct digital synthesis**
- **TxDACs® with interpolation, filters, digital quadrature modulation, etc.**
- **Cell phone chipsets**
- **Energy metering**
- **Video RAM-DACs**
- **Video encoders/decoders, codecs**
- **Touchscreen digitizers**
- **MicroConverter products (high performance ADCs, DACs, + 8051 µP core and flash memory)**

Figure 1.57: *Summary: Integrated Functions of the 1990s*

Hybrid and Modular DACs and ADCs of the 1990s

Although monolithic data converter solutions largely replaced the chip-and-wire hybrids and modules of the 1970s and 1980s, there were a few significant introductions early in the 1990s. The AD9014 14-bit, 10-MSPS modular ADC introduced in 1990 represented a major breakthrough in dynamic performance. The part achieved 90-dB SFDR over the Nyquist bandwidth, and utilized a number of proprietary monolithic building blocks which were later used in the fully integrated design of the AD9042 12-bit, 41-MSPS ADC introduced in 1995.

The AD1382 and AD1385 hybrid 16-bit, 500-kSPS sampling ADCs, introduced in 1992, represented state-of-the-art performance at the time, and the AD1385 was one of the first ADCs utilizing autocalibration to maintain its linearity.

Later in the 1990s, multichip module (MCM) technology became an excellent alternative to the expensive modules and chip-and-wire hybrids. Lower-cost packaging techniques allow high performance monolithic ADCs, such as the AD9042, to be packaged as duals along with front-end conditioning circuits. For instance the AD10242 introduced in 1996 (dual 12-bit, 41-MSPS AD9042s) offered an attractive cost-effective solution in applications requiring dual high-performance 12-bit ADCs and more functionality in the analog front end.

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SECTION 1.6: DATA CONVERTERS OF THE 2000s

Walt Kester

The data converter trends started in the 1990s shown in Figures 1.56 and 1.57 have continued into the 2000s. Power dissipation has dropped, and along with it, power supply voltages. Supplies of 5-V, 3.3-V, 2.5-V, and 1.8-V parts have followed as CMOS line spacings shrank to 0.6 µm, 0.35 µm, 0.25µm, and 0.18 µm. Smaller surface mount and chip-scale packages have also emerged as the modern replacement for the nearly obsolete DIP packages of the 1970s and 1980s.

Although the trend toward more highly integrated functions continues, data converter manufacturers are realizing that "smart partitioning" can offer a higher performance and more cost-effective solution than simply always adopting a "system-on-a-chip" philosophy. This topic is explored in much more detail in Chapter 4 of this book, *Data Converter Process Technology*.

The Analog Devices' portfolio of 16- and 18-bit SAR sampling ADCs has grown to over 30 models, including the latest offerings in the breakthrough high-resolution Pulsar® series. For example, the AD7664 16-bit, 570-kSPS ADC was introduced in 2000, the AD7677 16-bit, 1-MSPS ADC in 2001, and the AD7674 18-bit, 800-kSPS ADC in 2003, and the AD7621 18-bit, 3-MSPS ADC in 2003.

In the 2000s, general purpose multiple DAC offerings expanded to include 16-channels (AD5390, AD5391), 32-channels (AD5382, AD5383) and 40-channels (AD5380, AD5381). High speed DACs reached 1-GSPS update rates with the AD9858 10-bit DDS system.

Turning to IF sampling data converters, the AD6645 14-bit 80-/105-MSPS ADC was introduced in 2000, and the AD9430 12-bit, 210-MSPS ADC in 2002. Both converters represent breakthroughs in sampling rate and dynamic range.

Significant multichip module (MCM) introductions were the AD10678 16-bit, 65-/80-/105-MSPS ADC introduced in 2003, and the AD12400 12-bit, 400-MSPS ADC also introduced in 2003. Both devices use high performance IC sampling ADCs as building blocks followed by proprietary digital post processing.

In 2002 and 2003, the ADuC-series of MicroConverter® products was expanded to include 16- and 24-bit on-chip Σ-Δ ADCs. In addition, the SAR-based MicroConverter product line was expanded. Some of the future MicroConverter products to be introduced starting in 2004 will utilize the highly popular ARM7®-microcontroller core.

These data converter highlights of the 2000s are summarized in Figure 1.58.

There are, of course, many other things that could be said about the history of data converters. Many other examples of modern ADCs and DACs are given throughout the remaining chapters of this book. Looking to the future, we can expect many new breakthroughs, not only in sheer performance, but in levels of integration.

- **Continued expansion of Analog Front Ends (AFEs) and Multiplexed Front Ends (MxFEs®)**
- **16-, 18-bit Pulsar® series of switched capacitor SAR sampling ADCs**
  - **AD7674, 18-bit, 800kSPS ADC, 2003**
  - **AD7621, 16-bit, 3MSPS ADC, 2003**
- **Multiple DACs: 16-channel (AD5390, AD5391), 32-channel (AD5382/AD5383), 40-channel (AD5380/AD5381)**
- **IF-Sampling ADCs**
  - **AD6645 14-bit, 105MSPS ADC, 2000**
  - **AD9430 12-bit, 210MSPS ADC, 2002**
- **Multichip modules (MCMs):**
  - **AD12400, 12-bit, 400MSPS ADC, 2003**
  - **AD10678, 16-bit, 65/80/105 MSPS ADC, 2003**
- **AD9858 10-bit, 1GSPS DDS system, 2003**
- **16-/24-bit Σ-Δ MicroConverter products, 2002, 2003**
- **ARM7-based MicroConverter products, 2004**

Figure 1.58: *Data Converter Highlights of the 2000s*