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Nathaniel E Frank-White
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EXHIBIT A

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BEVAN M. BAAS ASSOCIATE PROFESSOR

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EDUCATION

Ph.D. in Electrical Engineering, Stanford University, Stanford, CA, 1999

M.S. in Electrical Engineering, Stanford University, Stanford, CA, 1990

B.S. in Electronic Engineering, California Polytechnic State University, San Luis Obispo, CA, 1987

PROFESSIONAL EXPERIENCE

Associate Professor, University of California, Davis, Electrical & Computer Engineering, 2008-present

Assistant Professor, University of California, Davis, Electrical & Computer Engineering, 2002-2008

Visiting Professor, Circuit Research Lab, Intel Corporation, 2006

Digital Designer, Atheros Communications, Sunnyvale, CA, 1999-2001

AFFILIATION

Electrical and Computer Engineering Graduate Group

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RESEARCH INTERESTS

Algorithms, architectures, circuits, and VLSI design for high-performance, energy-efficient, and area-efficient computation with strong consideration of the challenges and opportunities of future fabrication technologies.

RESEARCH ACTIVITIES

Dr. Baas' research activities involve the development and implementation of efficient and novel computational hardware with a focus on digital signal processing (DSP) workloads, which are becoming increasingly important in high-growth application areas from portable electronics to data-centers.

Active projects involve both programmable and dedicated-purpose processors. Recent projects include the AsAP (Asynchronous Array of simple Processors) programmable array processor chip, applications, compiler and mapping tools; Low Density Parity Check (LDPC) decoders; Fast Fourier Transform (FFT) processors; Viterbi decoders; and H.264 video encoders and decoders.

The 0.18 m CMOS AsAP chip contains 36 programmable processors, operates at over 610 MHz at 2.0 V, and is believed to be the highest clock rate processor designed in any university. The second generation AsAP2 processing platform contains 167 processors and has been implemented in 65 nm CMOS. It contains numerous architectural and circuit innovations and operates at over 1 GHz.

DISTINCTIONS

Bevan Baas was a National Science Foundation Fellow from 1990-93 and a NASA Graduate Student Researcher Fellow from 1993-96. He received the National Science Foundation CAREER award in 2006, and the Most Promising Engineer/Scientist Award by AISES in 2006.

SELECTED PUBLICATIONS

Dean Truong, Wayne Cheng, Tinoosh Mohsenin, Zhiyi Yu, Toney Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Paul Mejia, Anh Tran, Jeremy Webb, Eric Work, Zhibin Xiao, Bevan Baas, "A 167-processor

65 nm Computational Platform with Per-Processor Dynamic Supply Voltage and Dynamic Clock Frequency Scaling," Symposium on VLSI Circuits, June 2008.

Zhiyi Yu and Bevan Baas, "High Performance, Energy Efficiency, and Scalability with GALS Chip Multiprocessors," IEEE Transactions of Very Large Scale Integration Systems (TVLSI), in press.

Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Dean Truong, Tinoosh Mohsenin, Bevan Baas, "AsAP: An Asynchronous Array of Simple Processors," IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 3, pp. 695-705, March 2008.

Ryan Apperson, Zhiyi Yu, Michael Meeuwsen, Tinoosh Mohsenin, Bevan Baas, "A Scalable Dual-Clock FIFO for Data Transfers between Arbitrary and Haltable Clock Domains," IEEE Transactions of Very Large Scale Integration Systems (TVLSI), vol. 15, no. 10, pp. 1125-1134, October 2007.

Tinoosh Mohsenin, Bevan M. Baas, "High-Throughput LDPC Decoders Using A Multiple Split-Row Method," In Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP '07), April 2007.

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Dell Technology White Paper

Performance Analysis of Intel®Pentium® M and Pentium 4 Processors

July 2005

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This white paper is available in PDF; a synopsis follows.

The increased demand for portable computers with longer battery life, coupled with the growing power budget required for desktop processors, have made it impractical to use desktop processors in mobile platforms. The Intel Pentium M is the first Intel processor designed specifically for mobile platforms. Since its introduction in 2003, it has largely displaced the Mobile Pentium 4 and Pentium 4 processors in portable computers.

This white paper compares the architecture and performance of the Pentium M to higher-frequency Pentium 4 processors. This study highlights the fact that, when evaluating mobile platform performance, factors other than processor frequency are becoming more important.

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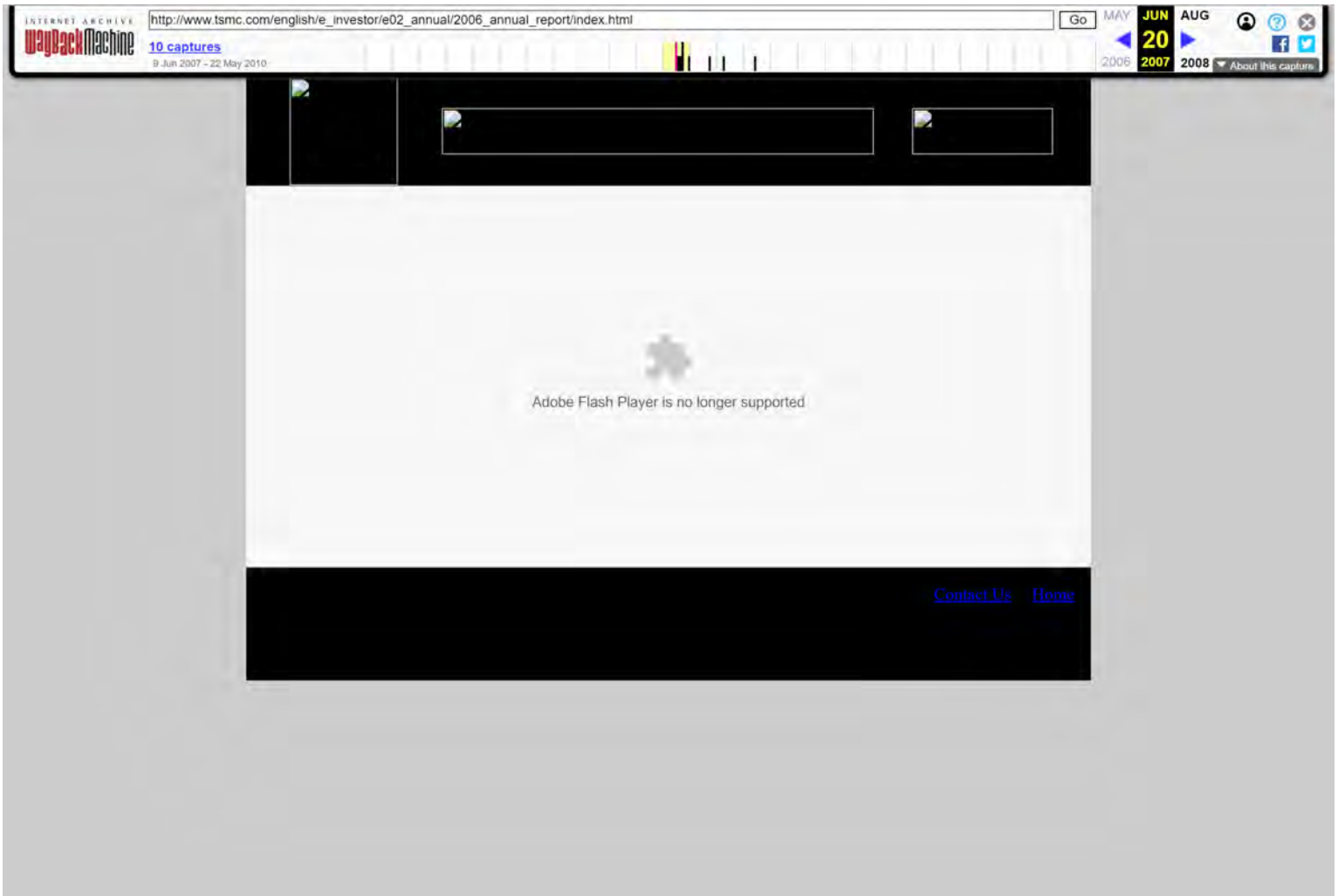
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TSMC Unveils Nexsys 65nm Process Technology Plans

Company Gears its Industry-Leading Fabs for First Customer Products by End of 2005

Issued by: Taiwan Semiconductor Manufacturing Company

Issued on: 2005/04/27

Hsinchu, Taiwan, R.O.C. -- April 27, 2005 -- Taiwan Semiconductor Manufacturing Company (TSE: 2330, NYSE: TSM), unveiled its newest semiconductor manufacturing process today at a Technology Symposium attended by over 400 of the industry's leading IC companies. First wafers are expected in December 2005.

The new 65nm Nexsys Technology for SoC Design allows designers to build logic devices with double the density of the company's industry leading 90nm technology. This massive integration -- the equivalent of more than 750 billion transistors on a single 12-inch wafer -- enables significant cost savings to market movers across the IC industry.

Benefits of TSMC's new process technology include a standard cell gate density twice that of TSMC's 90nm Nexsys process; a 6T SRAM cell size of less than 0.5um² (half that of its 90nm counterpart); and a 1T memory cell size that is a 65 percent smaller than the 90nm memory cell.

The 65nm Nexsys technology features an aggressive gate oxide thickness to further enhance transistor performance.

From a power and performance perspective, the 65nm Nexsys technology leads the industry with a 50 percent speed gain (TSMC's 65nm General Purpose process versus its 90nm General Purpose process); and a 20 percent standby power reduction. High-speed 65nm versions are expected to lead the industry in power/performance tradeoffs.

In a novel development born of an earlier process collaboration, an electrical fuse technology has been added to facilitate identification and configuration of devices.

"TSMC is already the foundry leader in 0.13-micron-and-below manufacturing technologies, with volumes and revenues that are multiples ahead of our nearest competitors," said Kenneth Kin, senior vice president, worldwide sales and service at TSMC. "The new 65nm Nexsys technology represents yet another leadership point from which the industry can rapidly accelerate the pace of innovation."

In response to customer demand, TSMC's first 65nm Nexsys technology, which will enter first production in December 2005, is optimized for low power. A high-speed version will be available in 2006, followed later in the year by a general-purpose 65nm process. A version employing SOI technology and an ultra-high-speed version will be introduced in 2007. Logic and mixed-signal options are slated for all versions, with embedded memory available in each.

TSMC's first 65nm silicon was a fully functional SRAM that featured more than 100 million transistors and was validated in April 2004. Since then, some customers including Altera Corp. and others, have taped out and received functional prototypes of their own designs, including logic and memory, for initial validation and benchmarking. Engineers at multiple companies are designing to the process, and tapeouts of production devices are expected to reach TSMC in the second half of 2005.

Early design rules and SPICE models for the new technology have been developed. TSMC libraries will be available in the fourth quarter of 2005, and third party library and IP developers are fast at work developing additional offerings. TSMC's 65nm Nexsys process is supported by Reference Flow 5.0 and will receive additional support as future iterations of the industry-leading design flow are developed. Process and design tools available to engineers are outlined in power and leakage management and design for manufacturing (DFM) guidelines.

The new technology features a minimum number of process changes, such as strained silicon and a new nickel silicide, to shorten time to volume. The 65nm Nexsys technology is the third-generation TSMC process to employ low-k dielectrics and the fourth generation to use copper interconnects.

The 65nm process may be the first-generation process to use immersion lithography techniques, developed in partnership between TSMC and ASM Lithography. A leading proponent of immersion techniques, TSMC took delivery of the first production-worthy 193nm immersion lithography system in 2004. Capable of 132nm wavelengths, the 193nm immersion system also provides a greater than 200 percent depth-of-field improvement versus dry lithography systems. The new 65nm process will be implemented in TSMC's industry-leading 300mm manufacturing facilities, Fab 12 and Fab 14.

About TSMC

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry industry's largest portfolio of process-proven library, IP, design tools and reference flows. The company operates two advanced twelve-inch wafer fabs, five eight-inch fabs and one six-inch wafer fab. TSMC also has substantial capacity commitments at its wholly-owned subsidiary, WaferTech and TSMC (Shanghai), and its joint venture fab, SSMC. In early 2001, TSMC became the first IC manufacturer to announce a 90-nm technology alignment program with its customers. TSMC's corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please see <http://www.tsmc.com>.

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TSMC Offers Industry's First Commercially Available True 0.18-micron Process Technology; Announces Product Has Shipped Advanced Process Provides 100 Percent Density Improvement, 30 Percent Speed Improvement, One-Third the Power Dissipation of 0.25-micron

Issued by: Taiwan Semiconductor Manufacturing Company Ltd.
Issued on: 1999/05/17

HSIN-CHU, Taiwan, May 17, 1999- Taiwan Semiconductor Manufacturing Company ("TSMC")(NYSE:TSM) Taiwan Semiconductor Manufacturing Company (NYSE: TSM), the world's leading dedicated foundry, today announced the immediate production availability of its true 0.18-micron CMOS process technology. Called CL018, this single-poly, six-metal layer process, with low-k dielectric is the industry's first commercially available 0.18-micron process. TSMC is already shipping products based on CL018 to customers.

"TSMC has consistently maintained a focus on delivering the industry's most advanced technology within an aggressive time table," said F.C. Tseng, president of TSMC. "With our 0.18-micron process we are on the leading edge of the SIA roadmap, providing our customers with a true process generation advance. In addition to current deliveries to customers, we will receive six additional customer tape outs this quarter, and we see over 30 more tape outs planned for the second half of 1999."

TSMC also unveiled its aggressive design rules, which allow densities of over 100,000 gates/mm² and an SRAM cell size of only 4.65 square microns. The performance of the process allows logic speeds over 400 MHz and on-chip memory speeds over 500 MHz. Power gate dissipation, with a 1.8V supply, is less than 30 nW/MHz.

The process technology has been designed to offer the optimal combination of density, speed and power to serve a broad range of computing, communications, and consumer applications. Early applications include high-performance 3D graphics chips for PCs, next-generation digital set-top boxes, high-capacity programmable logic devices, and chips for advanced wireless products.

TSMC's CL018 is a process technology platform for system-on-chip products. Building on the 1.8V logic foundation, customers can add 2.5V and 3.3V transistors for mixed-signal cores and I/O; precision capacitors and resistors for high-performance mixed-signal functions; and high-quality inductors, varactors, and diodes for RF functions. In 2000, TSMC will add Embedded DRAM and Embedded Flash Memory modules to the process.

TSMC defines "true" 0.18-micron process technology as not only CMOS FET transistor gates with a drawn dimension of 0.18 micron, but also layout and interconnect design rules appropriate to the new generation. TSMC's 0.18-micron process boasts the industry's tightest metal pitches with 0.46-micron on contacted metal-1, 0.56-micron on contacted metal 2-5, and 0.90-micron on metal 6. These pitches translate into high gate density, more die per wafer, and lower cost per chip.

"The market demand for 0.18-micron technology is quickly heating up, and TSMC has again established market leadership with its aggressive engineering schedule and its ability to meet customer time-to-market demands," said Tseng. "We have planned capacity to more than meet the expected demand of 34,000 wafers in 1999 and over 600,000 wafers in 2000."

Process Technology Details

TSMC CL018 Technology Summary First Production- 2Q, 1999 Core supply voltage- 1.8V I/O voltages- 2.5V and 3.3V Physical gate length- 0.16 micron Gate dielectric- Dual oxide 32/70 angstroms for 1.8/3.3V or 32/50 angstroms for 1.8/2.5V Poly Half-pitch- 0.215 micron Cobalt silicide gates and diffusion Metal layers- 6 Al/ 4Al+2Cu Contacted M1 pitch- 0.46 micron Contacted M2-5 pitch- 0.56 micron Top metal pitch- 0.90 micron Intermetal dielectric- Low-k FSG Vias- Tungsten with CMP Mixed-signal/RF modules- resistors, capacitors, high Q inductors, varactors, diodes Ring oscillator delay- 28ps SRAM cell size- 4.65 square microns Gate density - >100,000 raw gates/mm² Gate power- 30nW/gate MHz typical

In Q3 of 1999, TSMC will offer customers the option of copper for the top two metal layers to reduce circuit delays by a

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Date: February 11th, 2009
Topic: CPU & Chipset
Manufacturer: Intel
Author: Anand Lal Shimpi

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Seven billion dollars.

That's the amount that Intel is going to spend in the US alone on bringing up its 32nm manufacturing process in 2009 and 2010.

These are the fabs Intel is converting to 32nm:

32nm Manufacturing Fabs



D1D Oregon - Now



D1C Oregon - 4Q 2009



Fab 32 Arizona - 2010



Fab 11X New Mexico - 2010

In Oregon Intel has the D1D fab which is already producing 32nm parts, and D1C which is scheduled to start 32nm production at the end of this year. Then two fabs in Arizona: Fab 32 and Fab 11X. Both of them come on line in 2010.

By the end of next year the total investment just to enable 32nm production in the US will be approximately eight billion dollars. In a time where all we hear about are bailouts, cutbacks and recession, this is welcome news.

If anything, Intel should have a renewed focus on competition given that its chief competitor finally woke up. That focus is there. The show must go on. 32nm will happen this year. Let's talk about how.

The Manufacturing Roadmap

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62 Comments - Last by Oyvind, 46 days ago

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Poor AMD by ucsdmike, 110 days ago

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AMD's staff will be hitting the bar tomorrow.

This is amazing news from Intel. It is an exciting move.

Looking forward to cooler and longer running laptops in the near future.

RE: Poor AMD by Bezado11, 109 days ago

I wouldn't be surprised if the opposite was true. I'm really sick of all the hype on shrinking creates less heat. Look at the gpu industry, ever since they started shrinking things got hotter and hotter, and now it seems with i7 even though it's not a die shrink and we are use to 45nm by now, the new hardware to support minor changes in architecture of the cpu seem to make things run hotter.

i7 is way to hot. The newest GPU's run way to hot.

RE: Poor AMD by V3ctorPT, 109 days ago

The GPU's run hotter, because they pack double the transistors with a new shrink, than their previous HW... Reduction of the manufacturing process enables that we can have so much more transistors in the same place, of course it gets hot...

RE: Poor AMD by Targon, 109 days ago

For the CPU market, the problem is the ever growing amount of cache memory. Intel processors are designed with the large cache being their solution to improvements that AMD brings to the table.

I suspect that Intel will have more trouble after this move to the new fab process because the difficulty in moving to a new process node grows at an exponential rate. We saw Intel hit a wall with the Pentium 3 line because they were not ready for a new process shrink at that point, so the P4 came out. When Intel got their process technology on track, the people at Intel could go back to the Pentium 3 design(with improvements) to release the Core and Core 2 Duo.

There will come a time when an all new design will be needed in order to hold on to their lead, and that is when AMD will probably catch back up, if AMD can survive until then.

RE: Poor AMD by JonnyDough, 109 days ago

Well said, I concur.

RE: Poor AMD by PrinceGaz, 109 days ago

Even though my last three CPUs were all from AMD (they made sense at the time- K6-III/400, Athlon XP 1700+, Athlon 64 X2 4400+), I have to disagree with your comment about the improvements (presumably the integrated memory controller) which AMD brings to the table.

With Core i7, Intel has effectively removed the one last technological advantage AMD had- faster memory access. The fact that Intel chips still tend to have larger L3 caches is quite simply because they can afford to give it to them, as they are ahead of AMD on the fab-process. For a high-end desktop chip where there is die-space to spare, you could add some more cores which will probably sit idle (keeping four busy is hard enough, especially with HT), but adding more L3 cache (so long as the latency of it is not adversely affected) is a very cheap and easy way to use up the space and provide a bit of a speedup in almost everything.

AMD is currently fighting a losing game. The Phenom II (bug-fixed Phenom) cannot compete with Core i7 with AMD's current fabs, and unlike Intel who have the tick-tock steady new-process, then new-design with large teams working on each step; AMD seem to have one team working on a new design, which has to be made to work with whichever process looks like the best option at the time.

We need AMD to survive for the x86 (or x64, who came up with that :p) CPU market to be competitive, but I think the head of AMD is going to have to get into bed with the head of IBM, else they are doomed to fall ever further behind Intel in chip-design. The K10 is promising, but a long way off still, and AMD hasn't exactly been raking in the billions of dollars of profits recently to do that R&D. VIA have found an x86 CPU niche they can compete in, I fear that unless AMD pull an elephant out the hat with the K10, they'll have to slot in between VIA and Intel in providing CPUs specialising in a particular performance-sector, with Intel being the undisputed leader.

RE: Poor AMD by BSMonitor, 108 days ago

What an utter load of BS. Thanks fanboy.

You get all that from wiki?

RE: Poor AMD by JonnyDough, 109 days ago

I think you need to re-read the manufacturing roadmap page. It details the leakage gain (heat).

RE: Poor AMD by Mr Perfect, 108 days ago

That's because every time they shrink the chips they pack in new features and push the clock speed to the bleeding edge. If all they did was die shrink the old tech, we'd all be running something like an Atom CPU right now. Atoms closely resemble Pentium 3s, but on modern manufacturing only draw what? 5 watts?

RE: Poor AMD by Lighnix, 108 days ago

But you're making an unfair comparison - for example, the current latest GPUs have only been

produced on the newest nodes, ever. Now, if we take for example, a Radeon 3870 vs. a Radeon 2900 XT, the former draws far less power and will overclock better on air, almost directly as a result of them shrinking from a 80nm to a 55nm process, despite them performing exactly the same. Another example is the Core 2 E8000 series and E6000 series. Despite the increase in cache size, the E8000 dissipates little enough heat that they can provide them with a very tiny heatsink compared to the earlier 65nm cores, and objectively they draw much less power at the same clock speed because they run at lower volts.

You can see this sort of thing again and again throughout the technology industry. Coppermine (180nm) -> Tualatin(130nm), GeForce 7800 -> 7900, G80 -> G92, etc., etc.

If you were to compare say, a GTX280 to a 8800 GTX and say the former draws much more power than the 8800 GTX, AND it's produced on a smaller process - well, yes, but that's because they've clocked it higher and there are far more transistors (twice as many, in fact).

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The world's fastest processor gets faster. The new Core i7-975 runs at 3.33GHz but will hit 3.60GHz when only one core is active. The end result is the fastest CPU regardless of how many threads you're running.

June 3, 2009, [43 comments](#)

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Intel Unveils Next-Generation Atom Details

The next netbook/nettop Atom platform is closer than you think. It's called Pine Trail and it brings both the memory controller and graphics core on-die. Expect lower power, longer battery life and better performance in Q4 2009 from netbooks.

May 19, 2009, [22 comments](#)

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The Core 2 Quad Q8400: Intel's \$183 Phenom II 940 Competitor

AMD and Intel have quietly been fighting a quad-core price war. AMD started by introducing a very competitive Phenom II X4 940 priced similarly to Intel's Core 2 Quad Q8400. A couple of price cuts later Intel is trying a new strategy. The Q8400 is Intel's highest clocked quad-core CPU with only 4MB of L2 cache. Is that enough to compete with the Phenom II 940? And does AMD have much bigger things to worry about than whether or not it can outperform Intel at \$183?

Phenom II 940
May 19, 2009, [57 comments](#)

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Intel Announces Intent to Manufacture Atom SoCs at TSMC

What could have been a universe imploding sort of announcement amounted to something that just made sense: Intel will be making Atom SoCs at TSMC in addition to at its own fabs. I'll take you though why.

March 2, 2009, [9 comments](#)

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Intel's 32nm Update: The Follow-on to Core i7 and More

And you thought Core i7 was fast, how about a 6-core, 32nm version due out early next year? It's not all high performance though, Intel will be delivering its first 32nm Westmere CPUs for desktops and notebooks this year. If you're planning out your computer purchases for the next 12 - 18 months, help is on the way. Here's a hint: the notebook you want will be out by Q1 2010. You just have to make do until then.

February 11, 2009, [62 comments](#)

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Intel Core 2 Quad Q9550S: A New 65W Quad-Core

Intel joins the 65W quad-core bandwagon with its new S-series of chips. Now officially the most expensive Penryn based LGA-775 CPU you can buy we run the Q9550S through a series of performance, power and efficiency tests to figure out if it's worth it. It turns out that despite the 65W TDP, the Q9550S is best saved for OEMs while Intel offers enthusiasts a much more power efficient CPU for those who care: Nehalem.

January 27, 2009, [62 comments](#)

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Overclocking Core i7: A Tale of Two Retail Processors...

We provide some insight into our i7 overclocking experiences and realize a good IMC is your best friend.

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Nehalem Part 3: The Cache Debate, LGA-1156 and the 32nm Future

Want to understand why Intel went with such a small L2 cache on Nehalem? We sat down with Nehalem's chief architect and got a much better understanding of the world's fastest microprocessor. We

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E7300 and what to expect

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also uncover the on-chip PCIe controller in the mainstream Nehalem derivatives due out in 2009 and talk about its 32nm successors in 2009/2010.

November 19, 2008, [33 comments](#)

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[Nehalem: The Unwritten Chapters](#)

Nehalem can be much more power efficient than Penryn and it can overclock quite well. What follows are some of the side quests that we didn't get to complete for this week's launch of Intel's Core i7.

November 7, 2008, [23 comments](#)

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[Nehalem - Everything You Need to Know about Intel's New Architecture](#)

It's called the Core i7, but we knew it as Nehalem. We go through the entire micro-architecture and explain the new developments from IDF.

November 3, 2008, [36 comments](#)

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[The Dark Knight: Intel's Core i7](#)

Intel reinvented itself with Conroe two years ago, could the sequel possibly live up to expectations? Later this month Intel's Core i7 processors will be shipping and you'll find that they'll offer anywhere between 0 - 40% better performance compared to Penryn. An unexpected side effect? The i7 is Intel's most energy efficient Core microprocessor yet.

November 3, 2008, [74 comments](#)

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[Intel's SoC Update: 1B Transistors Embedded in 5 Years](#)

Intel revealed a bit about its upcoming embedded and SoC plans. Aside from Larrabee, these are brand new areas for Intel's x86 architectures. Intel has 15 chip designs in the works and is using similar rhetoric to what we've heard when the first dual-core chips were in production. Does this mean that Intel embedded and SoC designs will be as pervasive in a few years as dual and quad core CPUs are today?

July 26, 2008, [14 comments](#)

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[The Nehalem Preview: Intel Does It Again](#)

Two years ago we previewed Intel's Conroe core and to our surprise it blew away its closest competitor by 20 - 30% easily. Today, Intel is without competition at the high end but that hasn't stopped it from topping its performance by 20 - 50% with its brand new architecture. Intel's Nehalem processor is due out at the end of this year but we previewed its performance today and were very impressed; if you thought Penryn was fast, just wait until you see Nehalem.

June 5, 2008, [110 comments](#)

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[Intel Launches Low-Power 65nm 4 Series Chipsets for the Desktop](#)

With the release of their X48 Express performance chipset just a few short months back, many are asking why Intel is releasing another round of new chipsets so soon. We've got our ideas behind what's pushing them out the door so quickly and once we explain why you make look at the Intel P45 Express chipset in a whole new light.

June 5, 2008, [15 comments](#)

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[Intel's Atom Architecture: The Journey Begins](#)

When we reviewed the first Centrino CPU we claimed that it would revolutionize the mobile world, and it has. Intel's Atom processor has even more ambitious goals and we're able to have a look at its architecture to find out how it plans on achieving them.

April 2, 2008, [47 comments](#)

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[Opening the Kimono: Intel Details Nehalem and Tempts with Larrabee](#)

Intel gave us a few morsels of information on its future microprocessor plans, including details on the architectural enhancements to its first desktop CPU with an integrated memory controller: Nehalem.

March 17, 2008, [53 comments](#)

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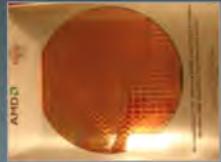
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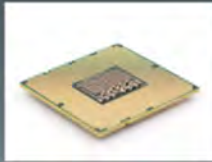
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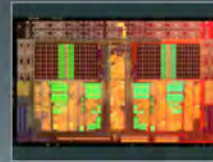
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blog post by Gary Key

Computex 2009 - Intel ULV Processor Updates

Intel is introducing new Ultra-Low Voltage (ULV) processors, Core 2 Duo processors, a speed bumped Standard Voltage (SV) processor, and finally a value based chipset (Mobile Intel GS40 Express) not based on the 945 chipset technology. These products join the recently released Intel ULV Core 2 Duo and Core 2 Solo processors based on...

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AMD's Six-Core Opteron 2435

AMD added 2 cores to the improved AMD quad-core "Shanghai". Which applications can take advantage of these extra cores? The answer is more interesting than you might think at first. ...

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ASUS sent us their W90Vp-A1 monster notebook, the current pinnacle of mobile ATI graphics solutions. There's plenty to like in this desktop replacement system, as well as a few problem areas. Join us for testing of one of the largest notebooks we've ever encountered...

May 29, 2009, 25 comments

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blog post by Anand Lal Shimpi

Lab Update: SSDs, Nehalem Mac Pro, Nehalem EX, Bench and More

I had an epiphany the other day. Long time AnandTech readers will know that I used to do a far better job of keeping you guys apprised of what it was that I was working on. Somewhere along the way that got lost so today I'm going to try something...old, I guess. Here's an update of what's been going on. The WePC Update've been working on a side...

May 27, 2009, 64 comments

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blog post by Anand Lal Shimpi

The Final Update: Flash Video Performance on Ion

It must be because this thing is so darn tiny that I don't mind testing it all the time, but today's short update marks the third follow up to our original Zotac Ion review. The original article crowned the Zotac Ion as the best Atom based mini-ITX board I'd ever encountered. It wasn't a hard feat to accomplish, after all, there are...

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blog post by Anand Lal Shimpi

[Zotac Ion: No Support for Wake on USB](#)

In response to our first article on the first mini-ITX motherboard based on NVIDIA's Ion platform, many of you asked enough questions that warranted a follow up. In said follow up I mentioned that wake-on-USB did not seem to work reliably on Zotac's Ion motherboard. Today I've got confirmation, said feature does not work. Zotac says that...

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We provide a first look at MSI's impressive \$169 X58 motherboard based on the uATX form factor. Does MSI have a winner here? We think so. ...

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[Real-world virtualization benchmarking: the best server CPUs compared](#)

We proudly present our newest virtualization benchmarking effort: vApus Mark I. The results are quite surprising on the latest server CPUs as it paints a very different picture than VMmark. Get a second opinion on how strong or weak the different CPUs are when they are running heavy-duty virtualized applications on ESX 3.5 Update 4....

May 21, 2009, [68 comments](#)

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blog post by Anand Lal Shimpi

[Intel's Atom Processor Compared to 68 CPUs in Bench](#)

A few months ago I launched something we quickly titled "Bench". The idea behind AnandTech Bench is that it's a publicly accessible version of the database of benchmarks we've run internally. You can currently compare 34 AMD CPUs and 36 Intel CPUs in the engine across 18 benchmarks. I'm working on adding power data as well. You can...

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[Intel Unveils Next-Generation Atom Details](#)

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[Zotac's Ion: The Follow Up](#)

At your request I dove deeper into wake on USB issues, overclocking, Flash video performance and power consumption with Zotac's Ion....

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[Digital Storm Core i7-965](#)

Our first look at Digital Storm systems, with impressive, raw performance....

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blog post by Matt Campbell

[BFG Phobos Q&A:](#)

We had an opportunity to chat with John Malley, BFG's Senior Director of Marketing, concerning their plans in the computer industry. They recently announced their intention to begin selling complete systems with the Phobos line, and we wanted to get more details on their goals and approach to the pre-built system market. Below are the questions and...

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Intel Core 2 Extreme QX9650 - Penryn Ticks Ahead



Date: October 29th, 2007

Topic: CPU & Chipset

Manufacturer: Intel

Author: Anand Lal Shimoi

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Intel Core™2 Duo E6550, 2.33 GHz

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We've never seen Intel with such a strong roadmap before, the company is truly firing on all cylinders and executing with amazing precision. Server, mobile, desktop and even new areas like ultra mobility and graphics all have absolutely wonderful roadmaps to look forward to. The biggest complaint we've had about Intel these days is that they kind of botched the X38 launch. Think back to a couple of years ago, what was our chief complaint then? Probably leaving us with power hungry, under performing processors for about 5 years. Today we're looking at a damn good Intel.

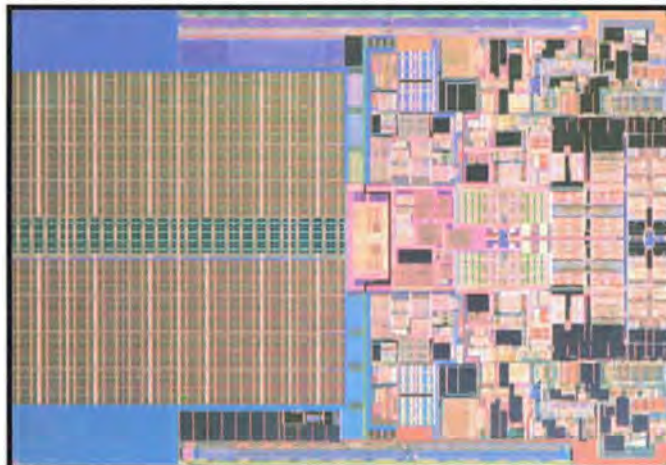
Recap: What's a Penryn?

Core, it's the architecture that shook an industry and today Intel is officially doing its first update to it. Prior to Intel's Core architecture, there wasn't much to get excited about when it came to Intel on the desktop.

At the same time, with Penryn Intel is very much the victim of its own success. How do you follow up such a tremendous splash with anything but equal greatness? AMD is close but still has yet to produce a response to Core 2, much less Penryn, and thus Intel's biggest competition today is itself.

In January 2007 Intel first showed off its 45nm High K + metal gate transistors, a dramatic departure from Intel's current 65nm transistors not only in size/switching speed but actual composition. If you remember back to the days of the original P6 processors, with a smaller transistor we saw tremendous improvements in die size, power consumption and performance. These days, such dramatic improvements are much harder to come by given that we're already dealing with such small transistor feature sizes. Gone are the days of the free lunch with each die shrink.

We've gone over [the technical details of Intel's high-K + metal gate enhancements](#), but the end result is that at the same clock speed you can expect dramatic reductions in power. Alternatively, at the same power levels, you can achieve much higher switching rates and thus higher clock speeds.



The core architecture of Penryn remains unchanged from Conroe; with the smaller transistors Intel's able to fit in a few new features and more cache on the chip while still maintaining a smaller die size. Where each dual-core Conroe die measured 143 mm², Penryn is merely 107 mm² despite having 50% more cache (6MB vs. 4MB). Obviously the quad core chips double overall area but you get the point.

Intel also uses a lot more of these new 45nm transistors than before; while a dual-core Conroe was made up of 291 million transistors, the comparable Penryn weighs in at 410 million (582M vs. 820M for quad-core variants). You're getting 40% more transistors and 50% more cache in a 25% smaller package; the latter is obviously most important to Intel as it helps reduce costs and drive profits up. So while it may seem generous, the move is purely self motivated on Intel's part.

The larger cache is a bit different than what we've seen in Conroe. While Conroe's cache is a 4MB 16-way set-associative L2, the 6MB Penryn cache is 24-way set-associative, designed to improve hit rates and keep latency manageable in an already large cache. Intel hasn't revealed whether Penryn's prefetchers have been adjusted to help populate its larger cache any better. As we saw in [our original Penryn preview](#), Penryn's cache performance remains unchanged; latencies in our final stepping are identical to Conroe.

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The cache enhancements are by far the biggest consumer of those extra transistors in Penryn, but believe it or not, they aren't responsible for the biggest performance boost. Intel has been fairly steady in adding new instructions to the x86 ISA and Penryn continues the trend with the addition of SSE4. Penryn gets 47 new instructions that make up the first implementation of SSE4; more will come with Nehalem at the end of 2008. We'll talk about SSE4 performance later on in this article, but here are the instructions you get with Penryn:

Sub Group	Instructions	Description	Expected Application Benefits
Packed DWORD Multiplies	PMULDQ, PMULBQ	New support for four signed or unsigned 32x32 bit multiplies per instruction, as well as signed forms of 32x32-bit multiplication	Broadly useful for improved automated complex vectorization of data processing written in high-level languages (like C and Fortran)
Floating Point Dot Product	DPBS, DPBSQ	Improved performance for AOS (Array of Structures) data processing through support for single and double precision dot products	3-D content creation, gaming, and support for languages like C++ and HLSL
Packed Blending	BLENDPS, BLENDQ, BLENDVPS, BLENDVQ, BLENDVB, BLENDVDB	Blending conditionally copies one field in the source onto the same field in the destination. These new instructions improve the performance of blending operations for most field sizes through packing multiple operations in a single instruction	Broadly useful for automated complex vectorization of data processing written in high-level languages (like C and Fortran) and applications such as image processing, video processing, multimedia, and gaming
Packed Integer Min and Max	PMINQB, PMAXQB, PMINLW, PMAXLW, PMINLQ, PMAXLQ, PMINSD, PMAXSD	Compares packed signed/unsigned byte/word/dword integers in the destination operand and the source operand, and returns the minimum or maximum as per the instruction type for each packed operand in the destination operand	Broadly useful for automated complex vectorization of data processing written in high-level languages (like C and Fortran) and applications such as image processing, video processing, multimedia, and gaming
Floating Point Round	ROUNDPS, ROUNDSS, ROUNDQ, ROUNDDQ	Efficiently rounds the scalar and packed single- and double-precision operands to integers, with enhanced support for Fortran, Java and C99 language requirements	Image processing, graphics, video processing, 2-D/3-D applications, multimedia, and gaming
Register Insertion/Extraction	PSORTPS, PSORQB, PSORQ, PEXTRQ, PEXTRB, PEXTRD, PEXTRW, PEXTRQ	These new instructions simplify data insertion and extraction between GPR (or memory) and XMM registers	Broadly useful for automated complex vectorization of data processing written in high-level languages (like C and Fortran) and applications such as image processing, video processing, multimedia, and gaming
Packed Format Conversion	PMOVSQB, PMOVQB, PMOVSQ, PMOVQ, PMOVSQB, PMOVQB, PMOVSQB, PMOVQB, PMOVSQB, PMOVQB, PMOVSQB, PMOVQB	Converts from a packed integer (from XMM register or memory) to a zero- or sign-extended integer with wider type	Broadly useful for automated complex vectorization of data processing written in high-level languages (like C and Fortran) and applications such as image processing, video processing, multimedia, and gaming
Packed Test and Set	PTSET	Facilitates branching from SIMD decisions to support conditionally vectorized code	Useful for improved automated complex vectorization of data processing, image and video processing, 3-D content creation, multimedia, and gaming
Packed Compare for Equal	PCMPEQB, PCMPQ	Performs SIMD compare for equality of the packed QWORDS in the destination and the source operand	Broadly useful for automated complex vectorization of data processing written in high-level languages (like C and Fortran) and applications such as image processing, video processing, multimedia, and gaming
Pack (DWORD) to Unsigned WORD	PACKUSDW	Converts packed signed DWORDs into packed unsigned WORDs using unsigned saturation to handle overflow condition. This new instruction completes the set of other instructions in this type	Broadly useful for automated complex vectorization of data processing written in high-level languages (like C and Fortran) and applications such as image processing, video processing, multimedia, and gaming

Penryn also implements a new divider that impacts both integer and floating point divides using a radix-16 algorithm. The algorithm computes more bits of the result of a divide each pass (four bits per iteration vs. two bits in Conroe), decreasing divide latency.



The faster divider is a very specific enhancement that should manifest itself as a performance boost in 3D and imaging applications.

Super Shuffle Engine

- Shuffle operations required for SSE data formatting operations
 - Unpacking
 - Packing
 - Align concatenated sources
 - Wide shifts
 - Insertion and extraction
 - Setup for horizontal arithmetic functions
- Key enabling capability for SSE4
- Penryn super shuffle engine performs 128 bit operations in a single cycle
- No software changes required

2X Faster SSE Shuffle Instruction Execution

Operation	Penryn Family	Merom Family
Shuffle byte	~1.5	~3.0
Insert	~1.5	~3.0
Extract	~1.5	~3.0
Qword shifts	~1.5	~3.0
Contact alignment	~1.5	~3.0
Unpack integer	~1.5	~3.0
Pack	~1.5	~3.0

Penryn's Super Shuffle Engine should also improve SSE2, SSE3 and SSE4 applications that use a lot of shuffle operations. Cache performance is also improved slightly for misaligned stores, which should improve performance, once again, in 3D and imaging applications. Finally, there are some power enhancements made to Penryn, but these are mobile-specific and thus don't apply to any of the desktop variants.

What do we have here today? Yorkfield

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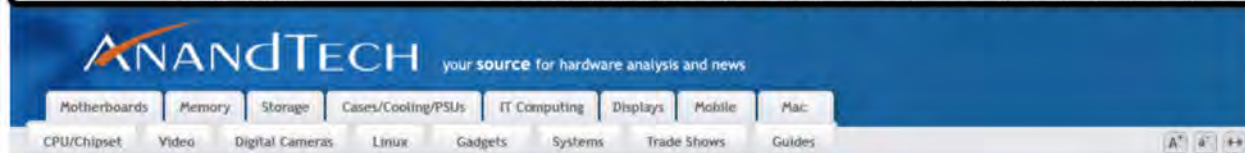
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Transcripts:

Day 1: Paul Otellini - Building a Continuum of Computing (PDF 132KB)
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Day 1: Bob Baker - Silicon Leadership—Delivering Innovation (PDF 110KB)

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Until We Meet Again

by Charlene Zvolanek
Fri Sep 17 2010 23:15:05 GMT+0000 (Coordinated Universal Time)

SUMMARY: The last day of IDF is always a mad rush to see all the things I haven't quite had time for. I spent some time at the poster chats, talking to researchers working on projects ranging from helping people...

How Is Energy Like a PC?

by Charlene Zvolanek
Fri Sep 17 2010 22:25:51 GMT+0000 (Coordinated Universal Time)

SUMMARY: Some of my pet projects were represented today, with personal energy management at the top of the list. The session "Personal Energy Systems: Doing for the Grid What Intel Did for Computing!" covered personal energy management systems, the shift...

Contextual Continuity Across the Continuum

by Charlene Zvolanek
Thu Sep 16 2010 21:49:14 GMT+0000 (Coordinated Universal Time)
SUMMARY: The final day of IDF looks toward the future in the morning keynote with Intel VP, Director of Intel Labs, and CTO Justin Rattner. This is a future shaped by consumer behavior, where technology companies gain insight and identify...

Jasper Forest:

Tech bulletin: Future Family of Low-Power Integrated Intel® Xeon® Embedded Processors for Communications and Storage (PDF 108KB)

Presentation: Innovating and Integrating for Embedded, Communications and Storage (PDF 2MB)

Video: Watch "Jasper Forest" OEM Testimonials



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Download a die shot of the Nehalem-EP based processor codenamed "Jasper Forest" (EPS/JPG 2.9MB)

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retweet **Communication-Assisted Platform Power Management**

February 23, 2010

Intel's energy efficiency research is showing how we're reducing overall platform power demands while maintaining high performance. Intel research is taking a holistic approach to power management from the network to the platform for extended battery life. This communications-based technology creates idle durations by aligning Tx, Rx and I/O break events allowing the CPU and platform to get into a low power state faster and stay there longer. This synergistic approach to power management is resulting in up to 30% CPU power savings for various workloads. See [video for more](#).

retweet **Small Objects, Big Worlds**

February 17, 2010

Intel Labs China is showcasing how photography can be used to allow amateurs to create rich visual content including 3D objects mirror worlds, environments that model buildings and other large structures in the real world. One prototype can help users to create a 3D model from real-life images without prior known camera parameters and without any calibration reference. The other can help users to create and navigate a mirror world by using the ever-increasing volume of user-generated and geo-tagged multimedia data.

retweet **Seamless Classroom Transitions Enabled by Intel**

February 9, 2010

Sustained technology use in classrooms is hampered by difficult moments of transitions, which take time and distract from the core activity of learning. These transitions happen between lessons, individuals, study groups, and classroom-wide activities. Intel's efforts in device composition through our Carry Small, Live Large research initiative enables mobile devices such as the Intel-powered classmate PC to dynamically share their clipboard and storage for collaborative learning, and then seamlessly transition to front-of-the-class presentations using wireless display technology. See [video for more](#) information.

retweet **Collaborative Visual Analytics in Virtual Worlds**

February 2, 2010

Virtual worlds are powerful tools for connecting groups of people. Intel and Qwaq, Inc. are working together on enterprise collaboration combining Intel's Miramar 3D desktop and Qwaq Forums into a new virtual collaboration environment, enabling groups of people to connect with groups of documents. Recently, Intel and Qwaq brought 3D visualizations into the mix, enabling visual analytics usage models within a collaborative work environment. This connects groups of people with large amounts of complex information for collaborative sense-making and understanding. See [Video for more](#).

retweet **Enhancing Computer Vision with Parallel Programming Tool**

January 26, 2010

Creating applications that take advantage of multi-core hardware requires new approaches in parallel programming. Innovative tools from Intel such as Intel® Concurrent Collections and Intel's Ct Technology can aid the development of these applications, such as computer vision. Concurrent Collections for C++ is now

applications, such as computer vision. Concurrent Collections for C++ is a new language, [now available](#), that helps create robust parallel applications, and Ct was born as an Intel research effort to extend C/C++ for data-parallel programming. See [video for more](#).

retweet **Computer Vision Accelerator**

January 19, 2010

As video cameras are integrated into more devices from laptops to phones, computer vision capabilities have become increasingly attractive to enable applications such as gesture-based user interfaces and augmented reality. Intel has demonstrated a functional, reconfigurable hardware accelerator to enable advanced vision capabilities on mobile devices. This research from Intel Labs, St. Petersburg explores the automated design of reconfigurable accelerators based on tools-aided application analysis targeting computationally-intensive media workloads such as the SURF object recognition algorithm. [See video for more information](#).

retweet **Everyday Sensing and Perception**

January 12, 2010

The ability to perceive user context, such as their location, activity and social interaction, is an essential ingredient for future mobile devices. Such devices could remind you to take your medication before a meal, step you through jump-starting your car or help you put a name that you've forgotten to a face. However, understanding detailed context accurately over most of a user's day is beyond the capability of today's devices. "Everyday Sensing and Perception," developed by Intel Labs researchers and demonstrated at [Research@Intel Day](#), integrates a novel wearable sensor-augmented video camera with state-of the art perception algorithms into one of the first systems that can parse much of daily life at a useful level. See "Everyday Sensing & Perception" video.

retweet **Don't Worry, Be Happy: Resilient Circuits**

January 5, 2010

Intel recently demonstrated research on a low voltage resilient processor that automatically adapts its power-performance point to achieve the best throughput at minimum energy. The distributed sensors and error detectors on the die enable automatic reissue of instructions or automatic adaptation of the operating conditions to achieve error-free performance beyond typical dynamic guardbands set by voltage, temperature and aging over lifetime of the product. See [blog and video demonstration](#) for more.

retweet **32nm. Not Just For Logic Chips Any More**

December 14, 2009

While Intel has been introducing a new logic process generation every two years, it has recently been developing a [System-on-a-Chip \(SoC\)](#) process alongside each logic process. With the 32nm generation, Intel's SoC process technology is the most advanced of any reported 32nm or 28nm process in the industry. Intel's 32nm [high-k/metal gate](#) transistor technology has been optimized for SoC platform applications that span a wide range of power, performance, and features. This technology has been developed to be modular, offering mix-and-match transistors, interconnects, RF/analog passive elements, embedded memory, and noise mitigation options. The low gate leakage of the high-k gate dielectric enables the triple transistor architecture to support ultra low power, high performance, and high voltage tolerant I/O devices concurrently. Embedded memories include high density and low voltage SRAMs. Analog/RF SoC features include high precision and high quality passives (resistors, capacitors and inductors) and noise isolation. Details were presented last week at the [International Electron Devices Meeting \(IEDM\)](#).

retweet **Moore's Law Marches On**

December 11, 2009

At the [International Electron Devices Meeting \(IEDM\)](#) this week, Intel disclosed new details of its latest process technology, with 32nm feature sizes. It includes Intel's 2nd generation [high-k/metal gate](#) transistors, for even better performance than that reported a year ago. By one measure, known as drive current, transistor performance has been boosted by 5% and 13% for NMOS and PMOS, respectively over results reported at the same conference a year ago. Intel showed that the 32nm technology continues the trend of 0.7x reduction in gate length variation and that the magnitude of both systematic and random within-wafer variation does not increase for the 32nm technology from the 45nm technology. Intel also showed that SRAM array density, which includes memory cells, sense amps and control circuitry, at 4.2 Mbit/mm², is the highest reported array density for a 32nm or 28nm technology. Intel is in high volume production of 32nm Westmere processors; units are now available to OEMs ahead of planned Q1 2010 introduction.

retweet **Intel Turbo-Charging Transistors**

December 10, 2009

Intel has reached a milestone in its quest to make transistors switch ever faster while using less energy, by integrating a high-k gate with a compound semiconductor transistor. Details were presented this week at the [International Electron Devices Meeting \(IEDM\)](#). Intel has been researching the possibility of replacing the silicon channel of the transistor by a compound semiconductor material such as Indium gallium arsenide (InGaAs). Up until recently, such transistors used a [Schottky](#) gate

with no gate dielectric, and were subjected to large gate leakage. Intel has now identified and integrated a high-k gate dielectric to reduce leakage with these so-called QWFETs (quantum well field effect transistors). The prototype device was fabricated on a silicon wafer substrate, pointing towards eventual process synergy with the existing silicon infrastructure. By using a high-k dielectric, gate leakage for short channel devices was reduced by 1000x compared with a Schottky gate, while the electrical oxide thickness was reduced by 33%, leading to higher switching speeds, which in turn leads to improved chip performance. More details are [available in a blog](#) by Mike Mayberry.

retweet **Organic Photovoltaics**

December 7, 2009

Future generation organic photovoltaic (OPV) technology holds the promise of ultra low-cost renewable energy because of its potential for high-speed manufacturing in roll-to-roll printing production. OPV's are also light-weight, thin, and flexible for ubiquitous use. However, current capabilities are limited to < 1 cm² sizes due to the critical dependence on nanoscale morphology of the organic material. Researchers at [Intel Labs Seattle](#) are investigating how to solve the manufacturability problem by introducing hard templates into the OPV device structure to scaffold the organic inks. The templates can be produced in high-volume and work well as a mold for the organic ink solutions. [Learn more about this research project.](#)

retweet **Sleep Talking PCs**

November 30, 2009

Emerging "anytime" device usages pose a difficult choice for consumers: either having a fully powered-on system that is energy inefficient and costly; or, shutdown their systems to conserve power, but prohibit "anytime" services access. Intel researchers have developed technology that allows devices to enter standby (S3) sleep state while maintaining full network presence, so the system can wake up on network service requests. Energy savings estimates are more than 40 TWhr over 100 million devices. [See blog](#) for more information.

retweet **ACM Symposium "Best Paper" Award**

November 23, 2009

At the recent ACM Symposium on Operating Systems Principles, Intel Labs researchers were awarded a "Best Paper" award for their report on "[FAWN: A Fast Array of Wimpy Nodes](#) (PDF)." The team of researchers, from Carnegie Mellon University and [Intel Labs Pittsburgh](#), combined low-power, embedded processors typically used in netbooks with flash memory to create a server architecture that is fast, but far more energy efficient for data-intensive applications than systems now used by major Internet services. A next-generation FAWN cluster is being built with nodes that include the Intel® Atom™ processor. For more information, see [article in ScienceDaily](#).

Safer & Smarter Roads

November 16, 2009

A number of traffic accidents are caused by worn down car tires. Intel along with industry players, [Kontron](#) and [ProContour](#) have developed tire-tread monitoring embedded technology that is making roads smarter. Kontron, a member of the [Intel® Embedded and Communications Alliance](#) has developed a camera with an Intel® Core™2 Duo processor that captures tire tread depth as a tire passes over a specialized grate. This technology can alert drivers when their tires need replacement to avoid potentially dangerous driving situations. [Learn more about embedded solutions for safer roads.](#)



Delivering 1 Million IOPs Using Seven PCI Express Prototype SSDs!

November 9, 2009

Recently Intel showcased more than 1 million IOPs (input/output operations per second) supported by a single mainstream server using 7 PCIe solid state drive (SSD) prototypes. With this proof of concept, Intel is identifying platform bottlenecks and working on engineering improvements for future storage products. To get this kind of performance from conventional hard drives, you would need many storage racks, filled with ~4,000 hard drives - an expensive, space-consuming and power-hungry proposition. Intel used one dual socket server with an expansion box and consumed only ~400 watts (more than 100x lower power than a hard drive configuration would have). We used a challenging workload for a single 1U server: 4Kbyte transfers with a 2:1 read/write ratio. Meanwhile, the CPUs were only about 50% utilized, leaving plenty of power left for applications. This could enable an online retailer to host an unprecedented number of website transactions while containing costs or a game developer could bring products to market faster. For more info, see Senior VP & GM, Bob Baker's Intel Developer Forum Keynote "[Silicon Leadership - Delivering Innovation](#)" and [recent press](#).





Amazing performance from this small setup



1 million 4K two-to-one read/write IOPs as measured by the IOMeter tool

On-chip Highways: 2D Interconnect for Tera-scale Processors

October 28, 2009

The ability to integrate hundreds of Intel Architecture cores into future microprocessors will help deliver the power of [Moore's Law](#) to new user interfaces and visually compelling experiences. A high performance, resilient, core-to-core interconnect will be as important for these tera-scale microprocessors as a well-designed highway grid is to moving goods and services across a country. Recently Intel demonstrated a next generation 2D interconnect prototype that provides high data bandwidth and low latencies between cores, memory and I/O. The demo also featured our -MCEMU FPGA-based many-core emulation platform developed at [Intel Labs, in Braunschweig, Germany](#), and a 3D visual interface developed with [UC Irvine](#). For more information see a [webcast of the demo](#) from the recent Intel Developer Forum in San Francisco.

Medical Imaging with Many-Core

October 16, 2009

Physicians today are collecting more complex imagery on their patients than ever before. Combined with the need to accurately diagnose disease and develop treatment strategies in a minimally-invasive manner, new imaging modes, methods, and hardware are needed. In collaboration with the [Mayo Clinic](#), Intel is presenting a paper at the [IEEE VisWeek09 Conference](#) today titled "Mapping High-Fidelity Volume Rendering for Medical Imaging to CPU, GPU and Many-Core Architectures," outlining how medical imaging benefits from the parallel processing architecture in the Intel microarchitecture, code-named Nehalem. Medical volumetric imaging requires high fidelity, high performance rendering algorithms. We've now achieved more than an order of magnitude performance improvement on a number of large 3D medical datasets.

Fast Food Made Faster, Smarter

October 12, 2009

Quick Service Restaurants (QSRs), known for making a science of fast food preparation and customer service, are getting a boost with embedded technology. [WAND Corporation's Digital Restaurant](#), powered by Intel processing technology, gives QSRs the ability to immediately alter images, prices and display configurations on digital menu boards and point-of-sale terminals, as well as track the success of marketing programs through sales transactions. The remote management capabilities available through [Intel® Active Management Technology](#) gives QSRs the flexibility to respond quickly to customer trends, inventory outages and competitor price drops. Learn more about Intel solutions for [digital signage](#) and [retail](#).



Robots Among Us

October 5, 2009

Take a closer look the next time you visit a hospital, factory or store - there may be a robot that is monitoring radiation levels, carrying heavy loads or promoting new products. Robots powered by Intel processors and based on [MobileRobots' Motivity](#) can accommodate environments and alter behavior to suit current conditions, including navigating around people and objects, and "learning" the surrounding layout. This is one example of the [15 billion devices](#) expected to be connected to the Internet by 2015. Learn more about [Intel's work with intelligent robots](#).



Shaping the Mobile PC's Future

September 23, 2009

Intel Rock Star Ajay Bhatt today at the [Intel Developer Forum](#) presented how mobile processor power/performance continues to improve with every generation of process technology and how the revolution in the mobile platform enables thinner, lighter notebook PCs with longer battery life that are indispensable in our day-to-day lives. [Download session materials](#) to learn more about enhancements to come to Intel® Architecture mobile platforms. (Locate course number: MPTS001 in the content catalog).



Intel Supply Chain Improvements Lead to Satisfied Customers

September 23, 2009

Intel has made significant improvements in its supply chain, as Intel Senior Vice President [Bob Baker](#) outlined in his keynote this week at the [Intel Developer Forum](#).

President [Bob Baker](#) outlined in his keynote this week at the Intel Developer Forum, Intel's 'Just Say Yes' Initiative has led to significant improvements in customer fulfillment. Manufacturing cycle times have been reduced by 62 percent. Our ability to respond to customer change orders - both positively and quickly - has improved 300 percent. Our turnaround time from customer order placement to delivery has improved 25 percent just in the past 12 months. Our delivery performance to committed dock date has improved significantly. Each of these supply chain improvements has led to more satisfied customers. See [Bob Baker's keynote materials](#) for more info on how Intel is improving its supply chain.

Ultimate Multi-Tasking Concept PC

September 23, 2009

Today at IDF, Intel showcased the world's first multi-screen, multi-touch concept mobile PC made possible using Intel's standard voltage CPU and Intel Graphics. This concept was developed as an inspiration for next generation notebooks.



Without compromising on the activity on your main screen, it allows you to organize and enjoy information your way, in snack-able bits, using the multiple auxiliary screens strategically located just above the keyboard.

Composition and the Collaborative Office

September 15, 2009

Today's conference room equipment is often inefficient and cumbersome, between initiating conference calls and passing projector cables from one presenter to the next. Using wireless display and mobile device-to-speakerphone dialing demonstrated recently at [Research@Intel Day](#), users can have more effective meetings by seamlessly switching between presenters and more easily establishing conference calls. For more information, see the "[Carry Small, Live Large](#)" Research Program.



New Entertainment Experiences in the WiMAX Connected Vehicle

September 9, 2009

Today's personal and in-vehicle entertainment devices are highly incompatible with each other outside of a simple wired connection that enables only rudimentary interactions. In the [new mobile world](#), Mobile Internet Devices (MIDs) used with Intel® Atom™-powered, WiMAX-enabled automobiles, can deliver a personalized, enhanced in-vehicle entertainment experience, as demonstrated recently at [Research@Intel Day](#). Personal preferences contained in MIDs can customize the in-car entertainment experience while WiMAX-based wireless Internet services link drivers with the world around them to enable exciting new safety, entertainment and communication experiences for tomorrow's automobiles.



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Intel Expands Intel® Atom™ Processor-Based Platform to Home, Small Office Storage Device >

CEBIT, HANNOVER, Germany, March 4, 2010 – Intel Corporation today launched its first Intel® Atom™ processor-based platform optimized for networked home and small office/home office (SOHO) storage devices.

Intel Honors 10 Companies with Supplier Continuous Quality Improvement Award >

SANTA CLARA, Calif., March 3, 2010 -- Intel Corporation honored 10 companies today with its Supplier Continuous Quality Improvement (SCQI) award for 2009.

Intel Honors 16 Companies with Preferred Quality Supplier Award >

SANTA CLARA, Calif., March 3, 2010 – Intel Corporation today bestowed 16 companies with its Preferred Quality Supplier (PQS) award.

Intel® Makes Oscar® Debut >

SANTA CLARA, Calif., March 1, 2010 – On the heels of its return as an individual Super Bowl advertiser after a dozen years, Intel Corporation has announced it will be an Oscars® telecast advertiser for the first time.

Intel's Sean Maloney to Take Medical Leave >

SANTA CLARA, Calif., March 1, 2010 – Intel Corporation said today that Sean Maloney, executive vice president and general manager, Intel Architecture Group, is taking a medical leave of absence after suffering a stroke at his home.

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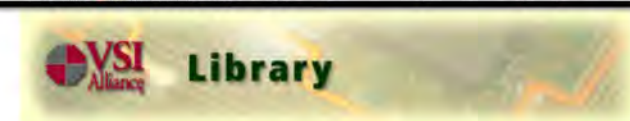
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Technical Documents & Specifications

[Obtaining VSIA Specs/Standards & Documents](#)

Specifications

- [Analog/Mixed-Signal Extension Version 2 \(AMS 1 2.x\)](#)
- [On-Chip Bus Attributes Version 1 \(OCB 1 2.x\)](#)
- [Soft and Hard VC Structural, Performance and Physical Modeling Version 2 \(I/V 1 2.x\)](#)
- [Test Data Interchange Formats and Guidelines for VC Providers Version 1 \(TST 1 1.x\)](#)
- [Virtual Component Transfer Version 2 \(VCT 1 2.x\)](#)

Standards

- [System-Level Interface Behavioral Documentation Standard Version 1 \(SLD 1 1.x\)](#)
- [Test Access Architecture Standard Version 1 \(TST 2 1.x\)](#)
- [Virtual Component Attributes \(VCA\) With Formats for Profiling, Selection and Transfer Standard Version 2 \(VCT 2 2.x\)](#)
- [Virtual Component Identification Physical Tagging Standard \(VCID\) Version 1 \(IPP 1 1.x\)](#)
- [Virtual Component Interface Standard Version 2 \(OCB 2 2.x\)](#)

Other Documents

- [Architecture Document](#)
- [Data Sheets](#)
- [Deliverables Document](#)
- [Document Definitions](#)
- [IP Protection White Paper \(IPPWP 1\)](#)
- [System Level Design Model Taxonomy \(SLD 2 20\)](#)
- [Taxonomy of Functional Verification for Virtual Component Development and Integration \(VER 1 1.x\)](#)
- [Specs under Review & Pre-Release Specs](#)

How to Obtain Specifications, Standards and Documents

- Specifications are available to members, as downloads, after executing a free "click-through" copyright license - located under the description of the documents below.
- Non-members must sign a copyright license and pay an annual fee of \$950 per specification (includes updates). The member and non-member licenses are accessed through the appropriate links in the following table.
- Non Members can buy a Single Copy of any Specification or Standard with this [fax-back form](#).
- VC Vendors can claim "VSIA Compliance" if they meet the requirements of the VSIA Compliance Policy. Click [here](#) for more info!

Specifications

[Analog/Mixed-Signal Extension](#) [On-Chip Bus Attributes](#) [Soft and Hard VC Structural, Performance and Physical Modeling](#) [Test Data Interchange Formats and Guidelines for VC Providers](#) [Virtual Component Transfer](#)

Analog/Mixed-Signal VSI Extension Specification Version 2.2

Analog/Mixed-Signal DWG

(AMS 1 2.2) Revision Date: February 2001

Released November 1999

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This document specifies the exchange of Analog/Mixed-Signal virtual components (VCs) by defining the deliverables, their associated design guidelines, and data formats to facilitate the test, exchange, and integration of process-specific ("hard") mixed-signal virtual components targeting digital system-chip applications, such as A/D, D/A converters and PLLs.

On-Chip Bus Attributes Specification Version 1

On-Chip Bus DWG

(OCB 1 2.0) - Revision Date: September 2001

Released August 1998

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This specification provides a detailed description of the requirements for on-chip bus documentation, physical deliverables, and technical bus attributes. It also defines a minimum set of attributes for system integrators, virtual component (VC) developers, and bus developers to choose from while using or developing system or peripheral on-chip buses. A set of on-chip bus design guidelines and a glossary of common bus terminology are provided as well.

Soft and Hard VC Structural, Performance and Physical Modeling Specification Version 2.1

Implementation/Verification DWG

(I/V 1 2.1) Revision Date: January 2001

Released May 1999

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In this specification, the VSI Alliance Implementation/Verification DWG defines the data formats and the list of deliverables that should be used for structural, performance and physical modeling of both soft and hard VCs. The I/V specification includes the RTL source and performance model formats needed for both hard and soft VCs, summary of the design constraints requirements, endorsement of the OVI Design Constraints Working Group (DC-WG) for the development of the design constraints standard, and the endorsement of the Open Library (OLA) standard for the performance modeling standard. The specification includes the data formats that should be used for the structural netlist and a number of physical data types associated with hard VCs.

Test Data Interchange Formats and Guidelines for VC Providers Specification Version 1

Manufacturing Related Test DWG

(TST 1 1.1) - Revision Date: January 2001

Released June 1999

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This specification covers Test Data Interchange formats and Design-For-Test (DFT) guidelines for VC Providers. Its purpose is to define the nature and format of the information transferred between the VC Provider and the VC Integrator. Guidelines for VC Providers are also presented, to insure successful incorporation of Virtual Components (VCs) into a system chip design using the VSIA (Virtual Socket Interface Alliance) methodology. All test-related information from the VSIA Architecture document (including Section 1.5) and test guidelines from Section 3 are covered. Subsequent revisions of this document will cover the transfer of similar information between the VC Integrator and the manufacturing Test Engineering function.

Virtual Component Transfer Specification Version 2

Virtual Component Transfer DWG

(VCT 1 2.1) - Revision Date: January 2001

Released October 1999

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The VCT 1 2.X Specification defines all the itemized documentation requirements that need to be transferred from the VC providers to the VC users along with the VC design data. VCT 1 2.X clarifies what documentation is needed by the VC integrators and is required to be provided by the VC providers. Adequate documentation is absolutely essential if the mix and match of diverse VCs is to succeed. VC providers benefit from knowing exactly what is needed, and VC integrators can use this specification as acceptance criteria when they are about to obtain a VC from a VC provider.

Standards

 [System-Level Interface Behavioral Documentation Standard \(SLIF\)](#)  [VC Attributes \(VCA\)](#)  [VC Identification Physical Tagging Standard \(VCID\)](#)  [VC Interface Standard \(VCI\)](#)

System-Level Interface Behavioral Documentation Standard Version 1

System-Level Design DWG

(SLD 1 1.0) - Revision Date: March 24, 2000

Released March 2000

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This System-Level Interface (SLIF) Standard provides a mechanism for ensuring the complete description of VC communication at various levels of abstraction. It enables the clean separation of a VC's behavior from its communication protocols, thereby easing the reuse of the same behavioral block with different interfaces. This standard also helps to ease the hand-off of system-level VC models between vendors and integrators, and provides a foundation to guide the import of VC models into different simulation and design environments. The SLIF standard will improve comprehension of VC interface behaviors at system level, support block reuse through improved model generation, and link VC models at multi-levels of interface abstractions. The SLIF standard provides a structure to describe: · A core set of interface layer abstractions which must be delivered with a VC, · The method for specifying the interface layering principle adopted by the provider, (flexible), · The structure for the description of each interface layer, and the definition of a behavioral syntax, · The link between the interface and the VC implementations or models, and · A rigorous technique for specifying the hierarchical relationship between interface abstractions.

Test Access Architecture Standard Version 1

Manufacturing-Related Test DWG

(TST 2 1.0) - Revision Date: September 2001

Released September 2001

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This document describes a standard for manufacturing test access to individual virtual components (VCs) embedded in a System-on-a-Chip (SoC). Test access refers to the ability to apply test stimuli to an individual VC and to monitor the response of the individual VC as a result of the applied test stimuli. Without a standard for test access, SoC designers and users may have difficulty accessing the individual VCs that are integrated with other application circuitry on an SoC. This makes it difficult to test the interconnect and user-defined logic between the VCs, as well as the VCs themselves. This standard was conceived to support the use and reuse of previously generated test vectors for individual VCs. The necessary logical structures needed to support the reuse of previously generated test vectors for individual VCs are introduced and defined in this document.

Virtual Component Attributes (VCA) with Formats for Profiling, Selection and Transfer Standard Version 2

Virtual Component Transfer DWG

(VCT 2.2.2) - Revision Date: March 2001

Released March 2001

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This document defines a set of attributes for the high-level profiling and characterization of virtual components (VCs). These attributes cover subjects, such as function, performance claims, process compatibility, system and logic description, physical description, operating conditions, integration requirements, third-party support, and much more. Attribute definitions include detailed data type information and have a consistent structure. They are designed to facilitate the rapid and easy identification of desired VCs from catalogs and databases containing a large number and variety of VCs. Users depend on such catalog data when they search and select appropriate VCs for their applications. While it is neither practical nor sensible to standardize the formats and contents of proprietary catalog databases, the efficient and unambiguous exchange of catalog data requires definition and compliance with an industry accepted common format. VCT 2.2.x achieves this objective by establishing a standard classification scheme for VC characteristics, and it imposes no requirements on the formats and structure used within any specific database. In order to meet the VCT 2.2.x Standard, VC catalog providers need merely parse their proprietary formats into this common exchange format and include the documents and design data specified in Table 1 of the VSIA Deliverables Document.

Virtual Component Identification Physical Tagging Standard Version 1

Intellectual Property Protection DWG

(IPP 1.1.0) - Revision Date: June 19, 2000

Released June 2000

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The VCID provides semiconductor foundries and providers of virtual components (VCs) with an automated and succinct means to track the use of VCs into the fabrication processes. This is accomplished by the use of tracking information embedded by VC providers or users into the Graphical Design System II-Stream (GDSII-Stream) file. This approach was based on a development from Artisan Components. This standard addresses only the tracking of VCs into the mask-making portion of the fabrication processes. It does not address protection of the Intellectual Property (IP) as a VC. The specified tracking mechanism is not secure. It is susceptible to tampering and is intended only to facilitate the passing, use and sharing of information among honest VC users and VC providers; it provides a ready means for surrounding infrastructure to be built.

Virtual Component Interface Standard Version 2

On-Chip Bus DWG

(OCB 2.2.0) - Revision Date: April 2001

Released March 2000

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This standard begins with defining the basic characteristics of the Virtual Component Interface (VCI). Then, the different complexity interfaces are described in detail, starting with the simplest one, the Peripheral Virtual Component Interface (PVCi). The PVCi and Basic Virtual Component Interface (BVCI) chapters are designed so that they can be read independently. The Advanced Virtual Component Interface (AVCI) contains a set of optional features that can be added to the BVCI. Only the differences from the BVCI are explained in the AVCI chapter. After the interface descriptions, some design guidelines are given. The VCI Transaction Language section is included as Appendix A.

Documents

[VSIA Architecture Document](#)

March, 1997

Available to Public

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This document presents the original baseline architecture for the VSIA proposed set of specifications. It is being updated and replaced by the VSIA Overview Document and the VSIA Deliverables Document. The Deliverables Document is now available. The Overview Document is in the final stages of editing. This document is owned and copyrighted by the VSI Alliance Inc. You may download and print out a copy for your personal use. All other rights are reserved by the VSI Alliance Inc.

VSIA Deliverables Document

[Version 2.5.0](#) - Revision January 2002

[Version 2.4](#) - Revision February 2001

[Version 2.3](#) - Revision October 2000

[Version 2.2](#) - Revision November 1999

[Version 2.1](#) - Revision October 1999

[Version 2.0](#) - Revision August 1999

Available to Public

Virtual Component Vendors wishing to make statements of VSIA Compliance please click [here](#) for instructions.

This document summarizes VSIA specified deliverables, which are explained in detail in the individual specifications. The summary information is expressed in a Table "VSIA Deliverables Summary." Appendix D. contains the VSIA Compliance Policy, which the means for vendors to claim and show compliance to VSIA specifications for their products. This document is updated each time a VSIA specification is updated, and is therefore the central document indicating the current status of all released VSIA specifications. Those using the VSIA summary information need to study the VSIA specifications to understand the full meaning of the data.

 [Intellectual Property Protection White Paper: Schemes, Alternatives and Discussion Version 1](#)

Intellectual Property Protection DWG

(IPPWP 1 1.1) - Revision Date: January 8, 2001

Released August 2000

 [Download](#) - Revision 01/08/01

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 [VSIA System Level Design Model Taxonomy Document Version 2](#)

(SLD 2 2.0)

System Level Design DWG

Released July 2001

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 [Taxonomy of Functional Verification for Virtual Component Development and Integration Standard Version 1](#)

(VER 1 1.1)

Functional Verification DWG

Released January 2001

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VSIA Forum at DesignCon 2002 - Can VSIA address the real SoC Reuse Issues?

Join us for an important Forum on Embedded Software Reuse at DesignCon, January 28, 2002. Hosted by the VSIA, the Forum will explore the need for software reuse in the next generation of SoC designs. The meeting will feature a VSIA Update, Keynote Speech, and a Panel Discussion on embedded software reuse solutions.

Click [here](#) for more info!

Event: VSIA Forum
at DesignCon

Place: Santa Clara

Convention Center

Date: January 28,
2002

Time 4:00 - 6:00 pm

Reception to Follow



VSIA's recent Member Meeting produced a number of well thought-out presentations and proposals on how to deal with the Embedded Software Issue -- as an industry and as the VSIA. Members and non-members are welcome to participate in these discussions via a new [Audio Visual Slideshow](#) of that important meeting.



The VSIA has released the Signal Integrity VSI Extension, Version 1.0 for a 60 day member review. VSIA Members, click [here](#) for more info!

VSIA Includes VCI in OCB VCA Spec Version 2.0. View the Press Release [here!](#) Download the new Specification [here!](#)

Motorola Supports VSIA in Promoting IP Reuse [Standards for System-on-Chip Design](#)

VSIA's Implementation/Verification DWG, has released the Firm VC White Paper for member review. Members, click [here](#) to download and review this new document.

Adoption and use of VSIA specifications is growing at many SoC businesses, including systems houses, EDA companies, IP providers, semiconductor companies (both with fabs and fabless), foundries and test equipment firms. Click [here](#) to view Slide Presentations from VSIA Members on their Adoption developments.

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Radeon HD 5870 Review

By: Hilbert Hagedoorn | Edited by Ian R. Barling & John A. Johnsen | Published: September 23, 2009

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ATI Radeon HD 5870 1024MB

I'm the King of the world

Ah good gawd man... it has been a while since we had something really new to report from that big graphics arena we all like so much. Yeah, it's probably no secret that AMD ATI today launches their Radeon series 5000 cards today as well... every technical detail was leaked like two weeks ago.

None the less, for true facts and no fiction, you know where you need to be. With the press being briefed two weeks in advance we can tell you we are eager to bring you a nice lengthy article with all the ins and outs of the AMD ATI product lineup. Here's what is being announced today:

ATI Radeon Series 5800:

- Radeon HD 5850 (299 USD)
- Radeon HD 5870 (399 USD)

So before I start off, let me state that our focus today will be the Radeon HD 5870, the Radeon HD 5850 samples have not been distributed just yet and will likely arrive in two weeks' time. The Radeon HD 5870... it's a beast, it's dark, really a little evil and it's just so much freaking fun. You have no idea. Why am I making silly euphemisms you ask? Well, I always tend to do that when I am excited about a product. Face it, we have had a dull year when it comes to graphics cards. DirectX 11 is now around the corner and as such both ATI and NVIDIA have been preparing themselves to show off their latest and greatest. Today, AMD's graphics subdivision ATI.

ATI has been focusing on three primary features and key selling points for the series 5000 products. First off, the new graphics adapters are of course DirectX 11 ready. With Windows 7 and Vista being DX11 ready all we need are some games to take advantage of DirectCompute, multi-threading, Hardware Tessellation and new shader 5.0 extensions. DX11 is going to be good. More on that later on in this article of course.

Another big feature of the product that you already learned about is of course Eyefinity, the ability to connect one to up-to six monitors (depending on AIC/AIB choices in outputs) to your videocard and use it in a desktop environment, or to create an incredible wide monitor resolution to play games in. It's nice, it is niche and yes... certainly not an option many of you will use... but really it is breathtaking as well. We'll explain this in a separate chapter though.

The third big and prominent feature is of course performance. Often in the past we have seen a new OS released with a new class of DirectX. Typically manufacturers like ATI and NVIDIA kept performance low and product costs low, barely allowing new titles to be played well with the new graphics cards. ATI has changed the rules today as the Radeon HD 5870 now has 1600 stream processors (shader processors). ATI literally doubled up everything inside that GPU and as such we spot a GPU die with 2.15 billion transistors. That's 2150 million transistors you guys. In comparison, the Radeon HD 4890 has 956 million.

So quite a lot in the architecture of this GPU has changed with one important task in mind, creating the absolute fastest single-GPU based graphics card on the market. The Radeon HD 5870 to date will be the world's most powerful GPU pushing more than 2.7 TFLOPS of computing power; it's the first DX11 GPU on the market and, as this article will show, also comes with a revolutionary energy design as this card's peak wattage is only 188 Watts.

So without further ado, have a peek at the Radeon HD 5870 1024MB, then head on over to the next page where we'll startup a nice in-depth review. Guru style... what else?

Radeon HD 5870

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Radeon HD 5750 review (Crossfire)

By: Hilbert Hagedoorn | Edited by John A. Johnsen | Published: October 21, 2009

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ATI Radeon HD 5750 1024MB

Single GPU and CrossfireX

Ever since ATI released their DX11 class graphics cards the Guru3D.com homepage has been plastered red with all the articles and spin-off articles based on series 5000 products. It's only been a few days since we released the Radeon HD 5770 reference article. In that article we originally also planned the results for the Radeon HD 5750. There was a small shipping mixup though, causing our 5750 board to arrive a little late here in the lab. That said, we received two cards and this article is obviously going to cover them. The article will be similar to the reference Radeon HD 5770 article with minor tweaks here and there, and obviously all Radeon HD 5750 results (CrossfireX as well) now included.

The recently released Radeon HD 5870 and 5850 products are segmented in the high-end range and as such do come with a fairly spicy price tag making all the new features out of reach for a lot of people. ATI is going to address that with the releases of series 5700 graphics cards. Two products will be releases in the mid-range segment. However, they will be stacked and loaded with exactly the same features as the 5800 series, yet it's performance is cut-down and obviously in return, the pricing is much more attractive as well.

In collaboration with ATI we will test the Radeon HD 5750 in single and a CrossfireX (Multi-GPU) setup. It's a product that performance wise positions itself close to the Radeon HD 4850 and GeForce GTS 250 yet now with superior features at an attractive price.

So what's the buzz for series 5000? Well, ATI has been focusing on three primary features and key selling points for the series 5000 products. First off, the new graphics adapters are of course DirectX 11 ready. With Windows 7 and Vista being DX11 ready all we need are some games to take advantage of DirectCompute, multi-threading, Hardware Tessellation and new shader 5.0 extensions. DX11 is going to be good. More on that later on in this article of course.

Another big feature of the product that you already learned about is of course Eyefinity, the ability to connect one to up-to six monitors (depending on AIC/AIB choices in outputs) to your videocard and use it in a desktop environment, or to create an incredible wide monitor resolution to play games in. It's nice, it is niche and yes... certainly not an option many of you will use... but really it is breathtaking as well. We'll explain this in a separate chapter.

The third big and prominent feature is of course performance for money. It's new, it's affordable, it has AMD written all over it ... head on over to the next page where we'll meet and greet Juniper aka Radeon HD series 5700.



Radeon HD 5750

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Gigabyte P55 UD5 motherboard - The UD5 features Gigabyte's UD3 suite of features, which include 2oz of copper throughout the PCB, Japanese solid capacitors, low RDS MOSFETs, high-quality ferrite core chokes, and more.
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Radeon HD 5750 - It is time to review the Radeon HD 5750, ATI's most budget DX11 card available at this time.
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Windows 7 vs Vista VGA game performance - With Windows 7 already released on MSDN as Final, Guru3D figured now would be a good time to look at ATI, NVIDIA, Single- and Multi-GPU game performance in-between Windows Vista and Windows 7.
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Blizzconn 2009 - The place is packed across 4 halls and here you see a mob waiting to try out the latest class for Diablo III, the Monk. Some of the latest hardware was on display; Oh and this year of course there was Ozzy.
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Guru3D PC Buyers Guide Summer 2009 - Guru3D offers you their annual PC Buyers Guide, this is the 2009 summer edition. This article brings you a set of recommendations of products we feel are great components to build yourself a nice gaming rig.
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Anno 1404 VGA graphics performance - So then, 1404's levels are set on a series of islands. Some of them are already inhabited, while others are virgin territory, ripe for conquest. The 3D engine is smooth, beautifully detailed, so how will the game perform with a selection of 15 graphics cards?
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Guru3D photo contest winners - From the 135 photo's you guys have been able to see we made a cut to 15 photo's we figured could end up as finalist. The 15 photo's have been submitted through a panel of judges. Check out the contest top 5 winners as well.

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Radeon HD 5850 review - We'll test and review the Radeon HD 5850, we'll check both the single GPU performance but also will check it out in CrossfireX multi-GPU mode.

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ATI Eyefinity review - Eyefinity in short is having the ability to connect multiple monitors to your graphics card and create an extreme native resolution.

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Radeon HD 5870 Crossfire (HIS) - As the dust settles from yesterdays Radeon series 5800 graphics cards release today we'll look into Radeon HD 5870 CrossfireX performance and scaling in a dedicated article covering a large benchmark test suite

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Radeon HD 5870 review - It's time for the article you've all been waiting on. Today ATI will launch their series 5800 graphics cards, the Radeon HD 5850 and 5870. Our twenty-seven page article today will cover all the ins and outs of this new DirectX 11 class graphics card series.

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AMD Athlon II X4 620 Quad Core - AMD releases their Athlon II X4 620 and 630. That first one, the 620 will be priced at sub 100 USD prices, meaning you get to enjoy and reap the benefits of multi-core processing for 100 USD. These are the cheapest quad-core processors to date.

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Cooler Master Sentinel Advance mouse - Cooler Master have launched their Sentinel Advance mouse, yeah the one with the cute little OLED screen inside. It's funky, it's new, it's refreshing.

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Core i5 750 - Core i7 860 and 870 - Today Intel is introducing the P55 motherboard chipset and no less than three new Nehalem based Lynnfield processors, with many more to follow in the upcoming months. Today's product releases are targeted at the higher segment of the mainstream market.

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Intel P55 chipset - MSI P55-GD80 - In this article we'll introduce you to the p55 chipset and present to you a very nice overclocking experience. MSI's P55-GD80 motherboard will be the flagship P55 motherboard, it oozes with features and performance and stands out alright.

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ASUS MARS dual GTX 285 - You take two GeForce GTX 285 graphics cards, stick 4 GB of memory on there (2GB per GPU), sandwich them, SLI them up, market it as MARS, slap a limited edition label on there and make only a 1000 units. That in a nutshell is the product we'll be testing today.

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Corsair X128 SSD - Corsair just launched the X series with the X for extreme, and you guessed it already, it's an Indilinx controller based product. Armed with Samsung NAND flash memory and a nice 64MB cache to make your operating system run smooth and stutter free.

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MSI N275GTX Lightning - Check out some of the N275GTX Lightning features: Custom design PCB, high-quality chokes and capacitors, Twin Frozr II cooling solution, voltage monitoring points, 10 power phase design, doubled up memory at 1792MB.

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BFG GTX 295 H2OC LE - BFG released two products based on CoolIT's cooling; here at Guru3D we will test and review the BFG GeForce GTX 295 H2OC (limited edition), a self-contained easy to install liquid cooling solution preinstalled onto the GeForce GTX 295 filled with coolant and everything.

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OCZ Vertex TURBO SSD - The Vertex Turbo Series has an increased host clock-speed and the SDR DRAM Cache clock frequency are now running steady and gentle at 180MHz. Yes, the end results is a Solid State Disk that now reaches ultra-fast 270/200 MBps read and write speed

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Phenom II X4 965 BE processor - AMD today launches their fastest quad-core processor to date, the 3400 MHz Phenom II X4 965 Black Edition. Head on over to the link below where we'll start up our in-depth review.

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OCZ Agility SSD review - The OCZ Agility series SSD is an accumulation of all the latest breakthroughs in SSD technology, including controller design, spiffy read/write speeds, and 64MB of onboard cache, yet with this series, it is available at a somewhat better price.

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Gigabyte Nan-Ping Factory Tour - Guru3D visited Gigabyte's Nan-Ping production factory in Taiwan. We followed the design and productions stages of both a motherboard and VGA card.

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Guru3D Rig of the Month - We just adore hardware. And sometimes some you guys really make a PC that really stands out. We ask you to answer a few simple questions and send in photo's of your rig. Each month we'll have a look at the entries and perhaps pick you and post your PC with photo's and everything here at Guru3D.com, each month we add a new addition - join now!

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Guru3D VGA Charts - The VGA charts is simply put a selection of games in which we will show you performance numbers (measured by average framerate). The distinct difference review results and these charts is two-fold, in our reviews we can only show you 5 maybe 6 comparative graphics card results due to limitation. In the VGA chart you can see all the reference cards we have tested in an orderly and easy to comprehend manner.

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Guru3D PC Buyer's Guide - Time to build that dream PC before you head off for school! Surely don't take our advice for granted, but at the very least let us help you a little.

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Interview ATI Dave Baumann - AMD recently launched a new high-end graphics card. In that spirit we interviewed Dave Baumann.

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CeBIT 2009 coverage - Guru3D was at CeBIT 2009 in Germany this year. In this 23 page encounting article Guru3D will show you what was hot and what was not. Loads of photo's on the latest gear, and even some prototype product you have never seen will be on display.

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NVISION 08 Coverage - Guru3D flew across the globe to San Jose to attend the NVISION 08 conference as organized by NVIDIA. We'll be attending a couple of workshops and obviously follow some of the better key-note speeches. Next to that we brought the big ol' camera with us to show you the facility, the people and thus cover the event with regular news-updates.

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Games Convention Leipzig - We just arrived in bumble-frickin nowhere, Leipzig. The cultural rich Leipzig where this years GC - Game Convention will take place. Guru3D is there pretty much to meet up with some of the hardware vendors. We'll tell you all about the gaming hardware & show you well .. a lot of booth babes.

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PhysX by NVIDIA - A review - NVIDIA will introduce a new set of GeForce drivers, PhysX driver and a PhysX pack. All GeForce series 8 and newer cards will get full PhysX support with a little help of the guys from Agela and NVIDIA's CUDA team. We take a peek at what is released next week, what can you expect, what combo's are possible and obviously our opinion on the entire PhysX experience.

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Guide to MKV x.264 GPU acceleration - How would you like to learn to playback MKV / x.264 content 98% accelerated by your Radeon of GeForce graphics card? And we'll even go a step further, optimize image quality with the help of your graphics card shader processors?

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GeForce GTX 285 review | 3-way SLI - The new GTX 285 is a respin product based off the GeForce GTX 280 yet now fabricated on a smaller 55nm fabrication node. Next to an in-depth performance review we'll also show SLI and 3-way

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AMD 785G chipset review - AMD today releases the new AMD 785G chipset. The board supports socket AM3 and thus DDR3 memory allowing the latest Phenom II processors. More importantly, incorporated into the chipset is ATI's Radeon HD 4200 IGP.

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Cooler Master LAB test bench v1.0 review

By Hilbert Hagedoorn, October 26, 2009 - 8:03 PM - 0 Comments

Cooler Master designed the Cooler Master LAB Test Bench v1.0. It's what has been missing here at the lab alright, a nice looking, easy to use chassis where we can pop on and off hardware components, it makes motherboard, cooler and RAM testing really easy. And as simple as this product is, we really like it. And rest assured we'll be using it with pretty much any future motherboard review. It's not a suitable product for everybody, but if it applies to you we can wholeheartedly recommend it.

[Read the Guru3D review](#)

 [Cooler Master LAB Test Bench PC Chassis v1.0](#)



Windows 7 USB - DVD Download Tool

By Hilbert Hagedoorn, October 26, 2009 - 11:26 PM - 0 Comments

When you purchase Windows 7 from Microsoft Store, you have the option to download an ISO file or compressed files. The Windows 7 USB/DVD Download tool allows you to create a copy of your Windows 7 ISO file on a USB flash drive or a DVD. To create a bootable DVD or USB flash drive, download the ISO file and then run the Windows 7 USB/DVD Download tool. Once this is done, you can install Windows 7 directly from the USB flash drive or DVD.

The ISO file contains all the Windows 7 installation files combined into a single uncompressed file. When you download the ISO file, you need to copy it to some medium in order to install Windows 7. This tool allows you to create a copy of the ISO file to a USB flash drive or a DVD. To install Windows 7 from your USB flash drive or DVD, all you need to do is insert the USB flash drive into your USB port or insert your DVD into your DVD drive and run Setup.exe from the root folder on the drive.

Note: You cannot install Windows 7 from the ISO file until you copy it to a USB flash drive or DVD with the Windows 7 USB/DVD Download tool and install from there.

To install the Windows 7 USB/DVD Download tool:

1. Download the Windows 7 USB/DVD Download tool installation file.
2. When you are prompted to either save the file to disk or run it, choose **Run**.
3. Follow the steps in the setup dialogs. You'll have the option to specify where to install the Windows 7 USB/DVD Download tool and whether to create shortcuts on your Start Menu or Windows Desktop.

System Requirements

- Windows XP SP2, Windows Vista, or Windows 7 (32-bit or 64-bit)
- Pentium 233-megahertz (MHz) processor or faster (300 MHz is recommended)
- 50MB of free space on your hard drive
- DVD-R drive or 4GB removable USB flash drive

Download - [click here](#)

S3 Graphics launches 5400E GPGPU

By Hilbert Hagedoorn, October 26, 2009 - 9:12 PM - 0 Comments

S3 Graphics announced the latest addition to its power-efficient embedded graphics processor family, with the unveiling of the OpenCL 1.0 capable Chrome 5400E GPGPU processor. The S3 Graphics 5400E will be unveiled at the Electronic Manufacturer Exposition (eMEX), October 22nd - 25th, in Suzhou, China at the Suzhou International Expo Center, Hall 4A, Booth No. 4K08.

OpenCL is an open, cross-platform standard used to harness the power of a GPU's internal shaders to accelerate parallel computations in applications ranging from scientific, medical, and other high performance computing (HPC) markets. The native OpenCL engine in the 5400E GPU enables our partners to go beyond graphics and video, and penetrate these diverse HPC markets.

"S3 Graphics continues to empower key embedded technology providers, helping extend their market offerings based on our growing portfolio of feature-rich products, incorporating next-generation technologies like General Purpose GPU computing, as well as the latest 3D graphics architectures, HD video decode and encode, and the latest HDMI and Display Port display interfaces," said Dr. Ken Weng, GM for S3 Graphics. "Our new Chrome 5400E truly bridges the gap between PC and embedded device design, giving customers true GPU versatility."

Native support of OpenCL with the industry's best GFLOPS per watt rating including a DirectX 10.1 / OpenGL 3.1 graphics engine, ChromotionHD video core for HD video decode including Blu-ray, H.264, and VC-1, a video encode engine, and OpenVG 1.1 engine in the 5400E creates the most versatile GPU for embedded applications requiring longevity, customization, performance, features, and low power.

DirectX 10.1 and OpenGL 3.1 applications on Microsoft Windows and Linux platforms can be effectively run using the Chrome 5400E programmable shader cores to speed up 3D simulations, 3D rendering applications, and other visual processing functions. OpenVG 1.1 support boosts 2D based vector graphics for scalable graphics and video vector based applications.

Driver support of Microsoft operating systems includes Windows 7 Aero, Vista Aero, XP, and CE. Linux kernel 2.6.xx with support for RedHat, SuSE, Ubuntu, Fedora Core, Debian, along with other Linux distributions are supported by the 5400E drivers. For more information, visit the [product page](#).



ASUS P7P55D-E Premium with SATA 6.0/USB 3.0 pixelized

By Hilbert Hagedoorn, October 26, 2009 - 9:06 PM - 0 Comments

ASUS is very soon introducing a motherboard with support for SATA 6 Gbps and USB 3.0 under product name P7P55D-E Premium. According to ASUS, this P55 board expects to show up in late October. The motherboard follows P7P55D Deluxe design and features except for enhanced SATA 3.0 and USB 3.0. P7P55D-E Premium is available soon.



Windows 7 fails on Japanese TV

By Hilbert Hagedoorn, October 26, 2009 - 8:59 PM - 0 Comments

Whoops ! Blue screen of death, errors, and more errors, yes, you are welcome to the world of Windows. As seen in the video a TV anchor demonstrates Windows 7 on live TV. He tries to zoom in on the Fuji TV studio, but nothing happens. At the end of the failed test, he concludes that Windows 7 is indeed faster than Windows Vista.



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Magnetic HDDs still cheapest in 2020

By Hilbert Hagedoorn, October 26, 2009 - 8:58 PM - 0 Comments

According to a new study, if HDDs continue to progress at their current pace, then in 2020 a two-disk, 2.5-inch disk drive will be capable of storing more than 14 TB and will cost about \$40 (today, a typical 500 GB hard drive costs about \$100). Although flash memories have also become popular - with advantages such as lower power consumption, faster read access time, and better mechanical reliability than HDDs - the cost per GB for flash memories is nearly 10 times that of HDDs. In addition, flash memory technology will reach technical limits that will prevent its continued scaling before 2020, keeping them from replacing HDDs.

In a study published in a recent issue of IEEE Transactions on Magnetics, Professor Mark Kryder and PhD student Chang Soo Kim of Carnegie Mellon University have investigated 13 up-and-coming NVM technologies to see whether one of them might outperform HDDs on a cost-per-TB basis in 2020. Their results showed that most technologies will probably not be competitive with HDDs or flash memories at that time, except for two potential candidates: phase change random access memory (PCRAM) and spin transfer torque random access memory (STTRAM).

As Kryder and Kim explained, PCRAM is based on the phase change properties of chalcogenide glass. With the application of heat, the glass can switch between two different states (amorphous and crystalline) to be used as a memory. With their small cell size and ability to store multiple bits per cell, PCRAMs have the potential to offer high densities and be cost-competitive with HDDs, but their biggest drawback is that they require somewhat higher power than most other technologies. PCRAMs are already beginning to be marketed by Numonyx Inc., an Intel-ST Microelectronics joint venture, and so are closer to practical realization than STTRAM.

STTRAM, which is similar to magnetic RAM, uses a spin polarized current to write data by reorienting the states of a magnetic tunnel junction between parallel and anti-parallel orientations. In their evaluation, Kryder and Kim found that STTRAMs appear to potentially offer superior power efficiency, among other advantages. If STTRAMs could be improved to store multiple bits per cell, the researchers predict that STTRAMs' density could make them candidates for replacing flash memory and possibly HDDs [via physorg].



Radeon HD 5870 QuadFire User Video

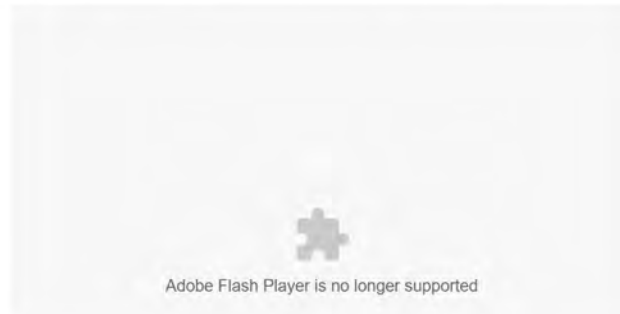
By Hilbert Hagedoorn, October 25, 2009 - 9:26 PM - 5 Comments

One of the bigger fans and aficionado's of graphics technology is Bodar -- Bodar is active in our forums a lot and he spends a lot of money on his gear. He recently built a fantastic PC -- totally overclocked and pimped up with no less than four Radeon HD 5870 1024MB card. This weekend he made a nice little video about his new setup and takes you through a good number of benchmarks and user experiences.

His configuration:

- Radeon HD 5870 1024Mb (x4)
- Xeon 3580 @ 4.72 GHz
- 120GB OCZ Vertex Turbo SSD
- 6GB Corsair Dominator
- 1500 Watt PSU
- Windows 7

If you are bored on a Sunday morning, go check out his video and if you like to comment him, please do so in [this thread](#). Nice job Bodar !



Akasa Freedom Tower CPU cooler

By Hilbert Hagedoorn, October 24, 2009 - 9:56 PM - 0 Comments

Akasa has introduced the Freedom Tower, a new processor cooler for the most recent processors from Intel and AMD. The cooler features a tower heatsink with four nickel plated direct-touch heatpipes, aluminum fins and a 120mm PWM fan with a max airflow of 57.32CFM at a noise level of 27.2dBA. Akasa Freedom Series is designed to unleash the performance of your system. Freedom Tower is a multi platform CPU cooler utilizing four nickel plated copper heatpipes with direct contact technology. The extreme cooling capabilities give you freedom to overclock and white LED 12cm fan with PWM provides ultra quiet performance and subtle illumination. Freedom to overclock is yours.

- Quality materials, classic design and killer looks
- Four nickel plated heatpipes with direct contact technology
- High grade aluminium fins for rapid heat dissipation
- Ultra quiet PWM 12cm white LED fan



Sapphire shows Vapor-X HD 5750

By Hilbert Hagedoorn, October 24, 2009 - 9:53 PM - 0 Comments

Sapphire is developing a Radeon HD 5750 with Vapor-X cooler. The HD 5750 Vapor-X includes a uniquely designed cooler utilizing Sapphire's "Vapor Chamber Technology" and improved heatsink design for superior airflow and much cooler operating temperatures. While exact specs are still unclear, we suspect it will be stock clocked like most Vapor-X models, including 1GB of GDDR5 memory and a core speed of 700MHz with memory at 1150MHz.

With its small size and 16W idle low power consumption, the card is perfect for media centres. It includes dual DVI, as well as HDMI and Display port on the rear. The Vapor-X edition is scheduled for November 3rd at a price of roughly 120 EUR.

The company also demonstrated a Vapor-X 5870 version recently .. which has yet to be found in retail.



Unigine Heaven DirectX 11 benchmark

By Hilbert Hagedoorn, October 23, 2009 - 10:51 PM - 1 Comments

Unigine Corp [announced](#) its release of the first DirectX 11 benchmark "Heaven" that is based on its proprietary Unigine engine. The company has already made a name among the overclockers and gaming enthusiasts for uncovering the realm of true GPU capabilities with previously released "Sanctuary" and "Tropics" demos. Their benchmarking capabilities are coupled with striking visual integrity of the refined graphic art.

"Heaven" benchmark excels at providing the following key features:

- Native support of OpenGL, DirectX 9, DirectX 10 and DirectX 11
- Comprehensive use of tessellation technology
- Advanced SSAO (screen-space ambient occlusion)
- Volumetric cumulonimbus clouds generated by a physically accurate algorithm
- Dynamic simulation of changing environment with high physical fidelity
- Interactive experience with fly/walk-through modes
- ATI Eyefinity support

Hardware requirements:

- The Tessellation feature REQUIRES a GPU with DirectX 11 support!
- ATI Radeon HD 2xxx and higher or NVIDIA GeForce 7xxx and higher (recommended: NVIDIA 8800 / AMD 4800 series)
- 256 Mb of video memory

Earlier this month the company has announced full support of DirectX 11 features in its top-notch 3D middleware. Updated Unigine engine supports Windows 7 and has successfully incorporated the groundbreaking DirectX 11 capabilities, including the following core features:

- Hardware tessellation
- DirectCompute
- Shader Model 5.0

Download the benchmark -- [click here](#) (135MB).

Or you can watch the YouTube video. We also have a discussion [thread open here](#).



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VLSI Computation LAB

The VLSI Computation Laboratory (VCL) is part of the ECE Department at the University of California at Davis. Our goal is to discover and develop novel contributions in **high-performance and energy-efficient VLSI computation**, with an emphasis on **digital signal processing (DSP)** workloads.

People of the VCL

Faculty



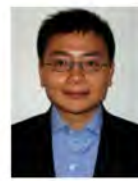
[Professor Bevan Baas](#)

Graduate students



[Dean Truong](#)
Ph.D. Candidate

- Power grid integrity
- DVFS algorithm implementation
- Multi-Vdd design flow



[Zhibin Xiao](#)
Ph.D. Candidate

- Architectures
- Video and multimedia applications
- Memory system design



[Anh Tran](#)
Ph.D. Candidate

- On-chip interconnects
- Multi-core architectures
- VLSI DSP implementation



[Bin Liu](#)
Ph.D. Candidate

- DVFS circuits and algorithms
- Processor architecture
- AES encryption



[Aaron Stillmaker](#)
Ph.D. Student

- Processor architecture
- Database record processing
- Algorithm mapping



[Jon Pimentel](#)
Ph.D. Student

- SAR image processing
- Processor architecture
- Biomedical imaging



[Jeremy Webb](#)
Ph.D. Student

- High-speed board design
- Many-core VLSI
- System interfacing



[Brent Bohnenstiehl](#)
Ph.D. Student

- Processor architectures
- LTE baseband processing
- VLSI Design



[Emmanuel Adeagbo](#)
Ph.D. Student

- Circuit design
- VLSI Design
- Many-core tools



[Houshmand Shirani Mehr](#)
MS Student

- Low Density Parity Check (LDPC) Decoders
- LDPC Algorithms
- Digital signal processing hardware



[Michael Braly](#)
MS Student

- Many-core processor tools
- Processor architectures
- DSP applications



[Samir Kagadkar](#)
MS Student

- VLSI design



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MS Student

- Hardware design



- Processor architectures
- Digital circuits



- DSP applications
- Software tools



Christine Watnik
MS Student

- Viterbi accelerator
- AsAP code scheduler
- DSP C compiler backend

Undergraduate Researchers



Victoria Harvey

- Many-core simulation
- Application development

Alumni



[Prof. Zhiyi Yu](#)
[Ph.D. ECE](#), Oct. 2007
Associate Professor
Fudan University

- Network on chip
- GALS clocking
- AsAP 1.0 physical design



[Prof. Tinoosh Mohsenin](#)
[Ph.D. ECE](#), Nov. 2010
Assistant Professor
University of Maryland, Baltimore County

- LDPC algorithms
- LDPC architectures and processor design
- Many-core processor arrays



Ryan Apperson
MS ECE, Sept. 2004
Senior Electrical Engineer
Physio-Control R&D

- Asynchronous data interfacing circuits
- SRAM design
- Full-custom CMOS layout



Omar Sattari
MS ECE, Sept. 2004
Software Engineer
CornerTurn
Instructor
Allied American University

- Address generation and branching
- Programming assembler, config
- FFT algorithm mapping



Mike Lai
MS ECE, Sept. 2004
Design Engineer
Altera

- High-speed pipelined signed multiplier
- High-speed modular signed adder
- Full-custom CMOS layout



Mike Meeuwsen
MS ECE, April 2005
Hardware Engineer
Intel, Digital Enterprise Group

- 802.11a algorithm mapping
- Architectural enhancements
- Instruction set design



[Toney Jacobson](#)
MS ECE, July 2007
Patent Associate
Fenwick & West LLP

- Fast Fourier Transform (FFT) architectures
- Digital system design
- High-speed FPGA design



[Eric Work](#)
MS ECE, Sept. 2007
Software Engineer
S-Machines

- Arbitrary task to 2D mesh mapping
- Software tool flow
- CAD tools



[Wayne Cheng](#)
MS ECE, January 2008
ASIC Design Engineer
Uniquify

- Dynamic voltage supply circuits
- Dynamic voltage and frequency circuits
- Transistor-level power simulations



Gouri Landge
[MS ECE](#), December 2009
Intel, Digital Home Group

- Video motion estimation architectures
- VLSI 65 nm motion estimation accelerator
- Programmable video processing hardware



Stephen Le
[MS ECE](#), March 2010
Component Design Engineer
Architecture Simulation
Intel, Visual Computing Group



Lucas Stillmaker
[MS ECE](#), September 2011
Graphics Hardware Engineer
Intel, Visual and Parallel Computing Group (VPG)
Intel Architecture Group (IAG)



- Parallel H.264 application development
- High-speed parallel simulator
- Tool integration



- Parallel application development
- Parallel database sorting algorithms
- Digital system design



Trevin Murakami
[MS ECE](#), December 2011
 Product Engineer
 Intel, NAND Solutions Group (NSG)

- Many-core simulator
- Processor architectures
- Digital signal processing hardware

Undergraduate Researchers

- William Au Yeung, BS ECE, June 2005
- Tomoko Tsuruta, BS ECE, June 2005
- Jason Cheung, BS CS, June 2005
- Leo Chan, BS ECE, June 2006
- Bassem Saad, BS ECE, June 2006
- Daniel Gurman, BS ECE, June 2006
- Sam Lee, BS ECE, June 2006
- Chi Chen, BS ECE, June 2006
- Kyle Piper, BS ECE, June 2007



Henna Huang
 BS ECE, June 2009
 Ph.D. Student
 MIT

- Parallel H.264 application development
- Multi-processor characterization
- Tool development



Gary Chung
 BS ECE, August 2009
 Apple Computer

- Embedded processor code development
- File system design and implementation
- Config design of 334-processor system



Brian Zimmer
 BS ECE, June 2010
 Ph.D. Student
 UC Berkeley

- MP3 decoder reference design
- MP3 decoder implementation



Layne Miao
 BS ECE, June 2011
 Analog Design Engineer
 Intel Corporation

- AsAP2 board bring up
- System characterization

Current Research

Asynchronous Array of simple Processors (AsAP)



Many members of the VCL are participating in work on the circuits, functional units, architecture, interconnection network, algorithms, and applications for a high-performance and energy-efficient processing system targeting computationally-demanding multi-algorithm DSP system applications. The single-chip processing system is comprised of a large number of fine-grain asynchronously-operating programmable processors connected by a reconfigurable 2-dimensional mesh network.

AsAP 1. The 0.18 μm AsAP 1 chip contains 36 programmable processors, operates at over 610 MHz at 2.0 V, and is believed to be the second highest clock rate processor designed in any university. Details of the chip were presented in the *Technology and Architecture Directions* session at ISSCC in Feb. 2006. See the paper below.

EETIMES



Also see the EE Times article "[Asynchronous array of processors chip presented at ISSCC 2006](#)," February 9, 2006.

AsAP 2. A second generation 65 nm CMOS design contains 167 processors with dedicated FFT, Viterbi, and video motion estimation processors; 16 KB shared memories; and long-distance inter-processor interconnect. The programmable processors can individually and dynamically change their supply voltage and clock frequency. The chip is fully-functional. Processors operate up to 1.2 GHz at 1.3 V which is believed to be the highest clock rate fabricated processor designed in any university. At 1.2 V, they operate at 1.07 GHz and 47 mW when 100% active. At 0.675 V, they operate at 66 MHz and 608 μW when 100% active. This operating point enables 1 trillion MAC or ALU ops/sec with a power dissipation of only 9.2 Watts. Due to its MIMD architecture and fine-grain clock oscillator stalling, this energy efficiency per operation is almost perfectly constant across widely varying workloads--which is not the case for many architectures.

Low Density Parity Check (LDPC) Decoders

We are working on LDPC algorithms, architectures, and circuits targeting several regimes, with a continual emphasis on high energy efficiency:

- Very high rate decoders
- Efficient decoding algorithms useful at many throughput rates

Special Purpose Processors

We are working on algorithms, architectures, and circuits for a number of dedicated purpose processing engines. Several active projects include:

- Fast Fourier Transform (FFT)
- Viterbi decoder
- H.264 video encoding and decoding
- other accelerator architectures

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 • CCF Grant [No. 0430090](#)
 • CCF Grant [No. 0903549](#)
 • CCF Grant [No. 1018972](#)
 • REU Grant 2005
 • REU Grant 2010



SRC, Semiconductor Research Corporation
 • [GRC](#) Grant 1598.001
 • [CSR](#) Grant 1659.001
 • [GRC](#) Grant 1971.001



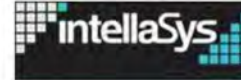
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Miscellaneous

[Computing resources](#) within the VLSI Computation Lab

Publications

Publications in review are provided to sponsors but not yet listed here.

2012

- Zhibin Xiao and Bevan Baas,
 "Processor Shapes and Topologies for Dense On-chip Networks,"
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2011

- Bin Liu and Bevan Baas,
 "Parallel AES Encryption Engines for Many-Core Processor Arrays,"
 To appear in the *IEEE Transactions on Computers*.
- Aaron Stillmaker, Zhibin Xiao and Bevan M. Baas,
 "Toward More Accurate Scaling Estimates of CMOS Circuits from 180 nm to 22 nm,"
 Technical Report ECE-VCL-2011-4, VLSI Computation Laboratory, ECE Department, University of California, Davis, December 2011.
- Trevin Murakami,
 "A SystemC Single-Cycle Simulator,"
 Masters Thesis, Technical Report ECE-VCL-2011-3, VLSI Computation Laboratory, ECE Department, University of California, Davis, December 2011.
- Bin Liu and Bevan Baas,
 "A High-Performance Area-Efficient AES Cipher on a Many-Core Platform,"
IEEE Asilomar Conference on Signals, Systems and Computers (ACSSC), Pacific Grove, CA, November 2011.
Nominated for Best Student Paper.
- Houshmand Shirani-Mehr, Tinoosh Mohsenin and Bevan Baas,
 "A Reduced Routing Network Architecture for Partial Parallel LDPC Decoders,"
IEEE Asilomar Conference on Signals, Systems and Computers (ACSSC), Pacific Grove, CA, November 2011.
- Zhibin Xiao, Stephen Le and Bevan Baas,
 "A Fine-Grained Parallel Implementation of a H.264/AVC Encoder on a 167-processor Computational Platform,"
IEEE Asilomar Conference on Signals, Systems and Computers (ACSSC), Pacific Grove, CA, November 2011.
- Ash Tean and Bevan Baas,

- Anh Tran and Bevan Baas,
["RoShaQ: High-Performance On-Chip Router with Shared Queues."](#)
IEEE International Conference on Computer Design (ICCD), Amherst, MA, October 2011, pp. 232-238.
Best Paper Award.
- Lucas Stillmaker,
["SAISort: An Energy Efficient Sorting Algorithm Many-Core Systems."](#)
 Masters Thesis, Technical Report ECE-VCL-2011-2, VLSI Computation Laboratory, ECE Department, University of California, Davis, September 2011.
- Anh Tran and Bevan Baas,
["Design of Bufferless On-Chip Routers Providing In-Order Packet Delivery."](#)
SRC Technology and Talent for the 21st Century (TECHCON), Austin, TX, USA, Sep. 2011, S14.3.
- Zhibin Xiao and Bevan Baas,
["A 1080p H.264/AVC Baseline Residual Encoder for a Fine-grained Many-core System."](#)
IEEE Transactions on Circuits and Systems for Video Technology, vol. 21, no. 7, pp. 890-902, July 2011.
- Bevan M. Baas,
 "A case for fine-grained many-core processor arrays,"
Parallel Algorithms, Programming, Architectures Workshop at the 48th ACM/IEEE Design Automation Conference (DAC), San Diego, CA, June 5, 2011.
Invited.
- Tinoosh Mohsenin, Houshmand Shirani-Mehr and Bevan Baas,
["Low Power LDPC Decoder with Efficient Stopping Scheme for Undecodable Blocks."](#)
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Invited.
- Jeremy W. Webb,
["A High Performance Baseband Instrument."](#)
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2010

- Tinoosh Mohsenin,
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- Dean Truong and Bevan Baas,
["Massively Parallel Processor Array for Mid-/Back-end Ultrasound Signal Processing."](#)
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Nominated for Best Student Paper.
- Anh Tran and Bevan Baas,
["DLABS: a Dual-Lane Buffer-Sharing Router Architecture for Networks on Chip."](#)
 In Proceedings of the *IEEE Workshop on Signal Processing Systems (SiPS)*, Cupertino, CA, Oct. 2010, pp. 331-336.
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- Anh Tran and Bevan Baas,
["Design of an Energy-Efficient 32-bit Adder Operating at Subthreshold Voltages in 45-nm CMOS"](#),
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- Anh Tran, Dean Truong and Bevan Baas,
["A Reconfigurable Source-Synchronous On-Chip Network for GALS Many-Core Platforms."](#)
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- Dean Truong and Bevan Baas,
["Circuit Modeling for Practical Many-core Architecture Design Exploration."](#)
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["A Split-Decoding Message Passing Algorithm for Low Density Parity Check Decoders."](#)
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2009

- Gouri Landge,
["A Configurable Motion Estimation Accelerator For Video Compression."](#)
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- Tinoosh Mohsenin and Bevan Baas,
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- Tinoosh Mohsenin and Bevan Baas,
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- Tinoosh Mohsenin, Dean Truong and Bevan Baas,
"An Improved Split-Row Thresholding Decoding Algorithm for LDPC Codes."
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- Tinoosh Mohsenin, Dean Truong and Bevan Baas,
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- Anthony Jacobson, Dean Truong and Bevan Baas,
"The Design of a Reconfigurable Continuous-Flow Mixed-Radix FFT Processor."
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- Dean Truong, Wayne Cheng, Tinoosh Mohsenin, Zhiyi Yu, Anthony Jacobson, Gouri Landge, Michael Meeuwsen, Christine Watnik, Anh Tran, Zhibin Xiao, Eric Work, Jeremy Webb, Paul Mejia, Bevan Baas,
"A 167-Processor Computational Platform in 65 nm CMOS."
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"A High-Performance Parallel CAVLC Encoder on a Fine-Grained Many-core System."
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"A 167-processor Computational Array for Highly-Efficient DSP and Embedded Application Processing."
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"An 18 Gbps 2048-bit 10GBASE-T Ethernet LDPC Decoder."
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- Wayne H. Cheng,
"Approaches and Designs of Dynamic Voltage and Frequency Scaling."
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- Zhiyi Yu,
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- Ryan Apperson, Zhiyi Yu, Michael Meeuwsen, Tinoosh Mohsenin, Bevan Baas,
["A Scalable Dual-Clock FIFO for Data Transfers between Arbitrary and Halttable Clock Domains."](#)
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- Eric W. Work,
["Algorithms and Software Tools for Mapping Arbitrarily Connected Tasks onto an Asynchronous Array of Simple Processors."](#)
 Masters Thesis, Technical Report ECE-CE-2007-4, Computer Engineering Research Laboratory, ECE Department, University of California, Davis, 2007.
- Anthony T. Jacobson,
["A Continuous-Flow Mixed-Radix Dynamically-Configurable FFT Processor."](#)
 Masters Thesis, Technical Report ECE-CE-2007-3, Computer Engineering Research Laboratory, ECE Department, University of California, Davis, 2007.
- Michael Meeuwsen, Zhiyi Yu, and Bevan Baas,
["A Shared Memory Module for Asynchronous Arrays of Processors."](#)
EURASIP Journal on Embedded Systems, vol. 2007, Article ID 86273, 13 pages, 2007.
- Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, Tinoosh Mohsenin, Dean Truong, Jason Cheung,
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- Tinoosh Mohsenin and Bevan M. Baas,
["High-Throughput LDPC Decoders Using A Multiple Split-Row Method."](#)
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- Zhiyi Yu and Bevan M. Baas,
["Implementing Tile-based Chip Multiprocessors with GALS Clocking Styles."](#)
 In Proceedings of the *IEEE International Conference on Computer Design (ICCD '06)*, October 2006, pp. 174-179.
- Tinoosh Mohsenin and Bevan M. Baas,
["Split-row: A reduced complexity, high throughput LDPC decoder architecture."](#)
 In Proceedings of the *IEEE International Conference on Computer Design (ICCD '06)*, October 2006, pp. 320-325.
- Bevan Baas, Zhiyi Yu, Michael Meeuwsen, Omar Sattari, Ryan Apperson, Eric Work, Jeremy Webb, Michael Lai, Daniel Gurman, Chi Chen, Jason Cheung, Dean Truong, Tinoosh Mohsenin,
["Hardware and Applications of AsAP: An Asynchronous Array of Simple Processors."](#)
 In Proceedings of the *IEEE HotChips Symposium on High-Performance Chips (HotChips 2006)*, August 2006.
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["Performance and Power Analysis of Globally Asynchronous Locally Synchronous Multi-Processor Systems."](#)
 In Proceedings of the *IEEE Computer Society Annual Symposium on VLSI (ISVLSI '06)*, March 2006, pp. 378-384.
- Zhiyi Yu, Michael Meeuwsen, Ryan Apperson, Omar Sattari, Michael Lai, Jeremy Webb, Eric Work, Tinoosh Mohsenin, Mandeep Singh, Bevan M. Baas,
["An Asynchronous Array of Simple Processors for DSP Applications."](#)
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2005 and prior

- Michael J. Meeuwsen,
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- Bevan M. Baas,
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 In Proceedings of the *IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP) 2005*, March 2005, pp. V-89-92.
- Michael J. Meeuwsen, Omar Sattari, and Bevan M. Baas,
["A Full-Rate Software Implementation of an IEEE 802.11a Compliant Digital Baseband Transmitter."](#)
 In Proceedings of the *IEEE Workshop on Signal Processing Systems (SIPS '04)*, Oct. 2004.
- Ryan W. Apperson,
["A Dual-Clock FIFO for the Reliable Transfer of High-Throughput Data Between Unrelated Clock Domains."](#)
 Masters Thesis, Technical Report ECE-CE-2004-5, Computer Engineering Research Laboratory, ECE Department, University of California, Davis, 2004.
- Michael A. Lai,
["Arithmetic Units for a High Performance Digital Signal Processor."](#)
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- Omar Sattari,
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- Bevan M. Baas,
["A Parallel Programmable Energy-Efficient Architecture For Computationally-Intensive DSP Systems."](#)
 In Proceedings of the *IEEE Asilomar Conference on Signals, Systems and Computers*, 37th, November 2003.
- Howard CheHao Chang and Bevan M. Baas,
["Mapping an FIR Filter to a 2-Dimensional Mesh of Processors."](#)
 Technical Report ECE-CE-2003-1, Computer Engineering Research Laboratory, ECE Department, University of California, Davis, 2003.

In The News

- New 167 processor chip is super fast, ultra energy efficient

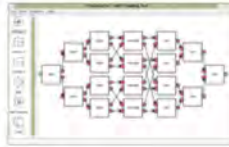
- New 10/7 processor chip is super-fast, and energy-efficient
 - [EurekAlert](#) news service operated by AAAS
 - [TechRadar](#)
 - [UC Davis News Service](#)

Projects for Interested Graduate Students

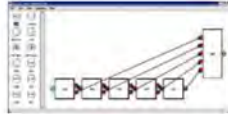
- Arbitrary graph mapping algorithms and tools
- Dynamic supply voltage and clock frequency circuits and algorithms
- Programmable DSP processor design
- Parallel DSP algorithms
- Reconfigurable inter-processor networks for various network traffic styles
- Functional unit and circuit design
- Processor simulation, emulation, and CAD design flow
- Shorter-term projects (possibly for undergraduate students)
 - Enhancements to our C compiler
 - Measurement and characterization of our multi-core chips (longer term)
 - Writing various FFTs on AsAP array
 - Chip design CAD tool projects
- [A note to interested prospective students](#)

Downloadable Tools Developed in the VCL

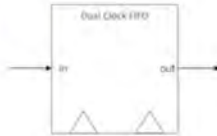
- [Arbitrary Graph to 2D Mesh Mapping Tool](#)



- [Low overhead parallel-task linux based simulator](#)



- [Dual-clock FIFO](#)



VCL-Specific Material



- [Directions to the VCL lab](#)
- [Some VCL Guidelines](#) for students in the VCL lab (good computer etiquette, writing papers, responding to reviewers)
- [VLSI & Sig. Processing conferences](#), [Micro Sys News Calendar](#)
- [Unix command notes](#), [Unix tutorials](#), [latex notes](#)
- [Information on the FPGA boards](#) used in the lab
- [Getting started in the VCL lab](#)

Other CAD Tools We Use

- Some [tools installed locally](#)
- [Cadence](#)
 - [Tool notes](#)
 - [NC verilog](#)
 - SoC Encounter
 - [Virtuoso](#)
- [Synopsys](#)
 - Design Compiler
 - [HSpice](#)
 - [NanoSim](#)
- [Mentor Graphics](#)
 - Calibre
 - Expedition
- Magic layout tool
 - [Magic web site](#)
- Tutorial web pages
 - [Cadence](#), [NCSU](#), and various tutorials

Other Useful Links

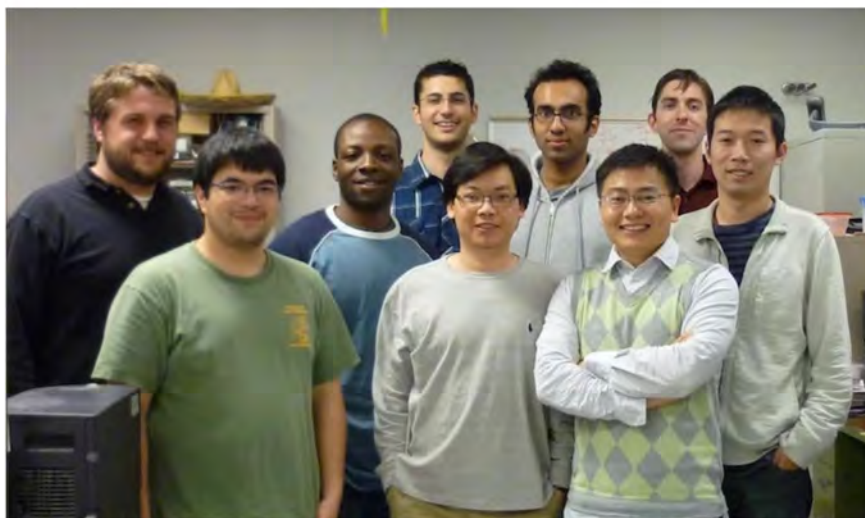
- [IEEE papers](#)
 - [JSSC](#)
 - [TVLSI](#)
 - [TCAS I](#): Regular papers; [Publication statistics](#)
 - [TCAS II](#): Express briefs
- [Microprocessors through the ages](#)
- [Intl. Tech. Roadmap for Semiconductors \(ITRS\)](#)
- [MOSIS web site](#)
- Future technology envisions from UCR's Predictive Technology Model

- [future technology space access](#) from GDS II future technology model
- [Accurel](#) for FIBing, packaging,....
- [AsAP Wikipedia page](#)
- [gds2pov](#), a 3D GDSII visualization tool

Informative References

- LaTeX: [Formulas](#).
- Deep chip's [CAD tool review](#) from CAD '04

A few group pictures



Aaron, Michael, Emmanuel, Jon, Ahn, Samir, Zhibin, Brent, and Bin in the office-lab; April 4, 2012.



Group dinner celebrating Jeremy, Lucas, and Trevin's graduations as well as Ahn's best paper award and Bin's best paper nomination; January 25, 2012.



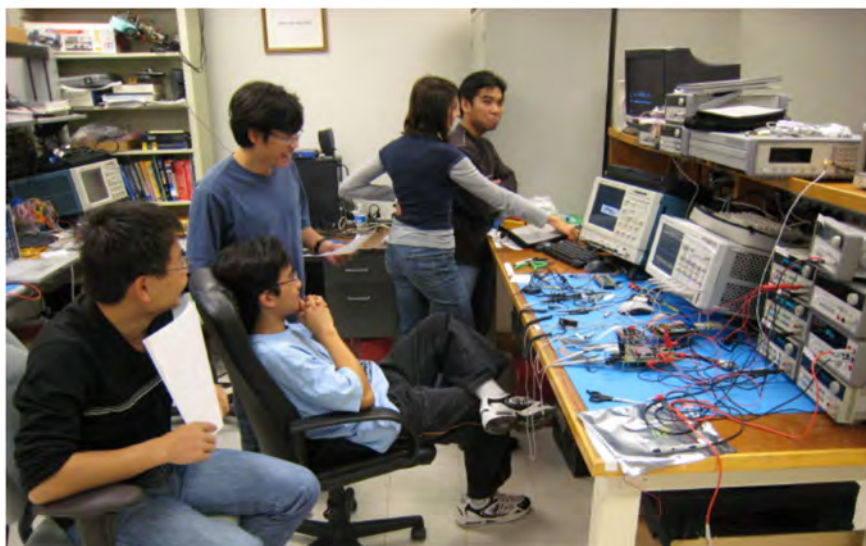
Group lunch celebrating end of Spring quarter; June 10, 2009



Dean and Anh in office-lab; January 25, 2009.

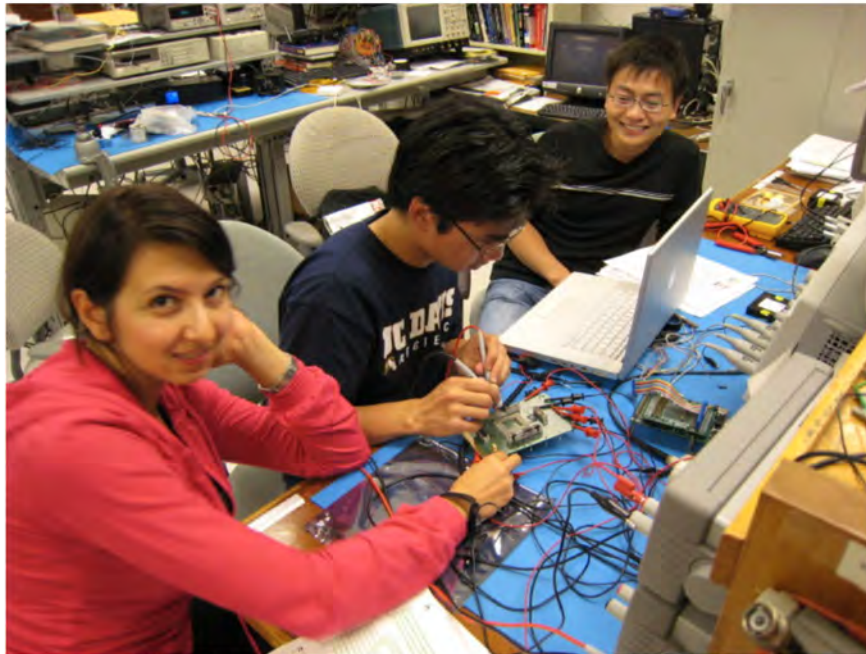


Dean, Zhibin and Paul in office-lab; March 27, 2008.





Zhibin, Dean, Anh, Tinoosh, and Paul working on AsAP2 bringup; October 12, 2007.



Tinoosh, Dean, and Zhibin working on AsAP2 bringup; October 11, 2007.



Dean, Zhibin, Anh, Tinoosh, Paul, and Bevan at ECE Grad Student BBQ in Kemper courtyard; October 4, 2007.

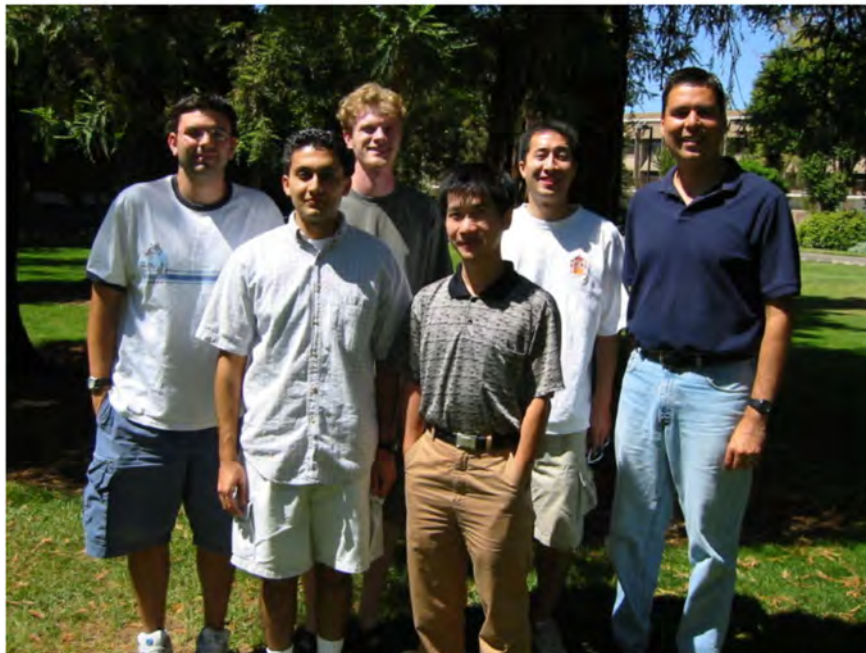




Toney, Wayne, Zhibin, Anh, Zhiyi, Tinoosh, Paul, Dean, and Bevan celebrating Toney's and Wayne's graduations at Woodstock's; August 29, 2007.



Tinoosh, Dean, Christine, Wayne, and Zhiyi in Kemper 2211; November 8, 2006.



Ryan, Omar, Mike M., Zhiyi, Mike L., and Bevan near the quad after lunch; August 26, 2004.

Bevan Baas



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Teaching

Quarter		Course
Spring 2012	-	Family "new Dad" leave :-)
Winter 2012	EECS 281	VLSI Digital Signal Processing
Fall 2011	-	Sabbatical
Spring 2011	ENG 6	Engineering Problem Solving
Winter 2011	EECS 281	VLSI Digital Signal Processing
Fall 2010	EECS 116	VLSI Design

Final Project [winners and results](#)

Office hours

Spring quarter by appointment.

Bio

Bevan Baas received a B.S. in electronic engineering from California Polytechnic State University in 1987, and M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1990 and 1999 respectively.

From 1987-89, he served as a new product engineer working on the processor for a high-end minicomputer in Hewlett Packard's Computer Systems Division, Cupertino, CA. In 1999, he joined Atheros Communications as the second full-time employee after the founders and served as a core member of the team which developed the first IEEE 802.11a (54 Mbps, 5 GHz) Wi-Fi wireless LAN solution. The chipset has been shipping in volume since September of 2001 and for one and a half years was the only shipping 802.11a chipset [[ISSCC 2002](#)]. Atheros became a publicly-held company in Feb. of 2004 and was purchased by Qualcomm in 2011.

In 2003, Dr. Baas joined the Department of Electrical and Computer Engineering at the University of California, Davis as an Assistant Professor, where he currently supervises research for 13 graduate students. In 2008, he became an Associate Professor.

Dr. Baas' research interests are in the algorithms, architectures, circuits, and VLSI design for high-performance, energy-efficient, and area-efficient computation with strong consideration of the challenges and opportunities of future fabrication technologies. He is interested in both programmable and special-purpose processors with an emphasis on DSP workloads. Recent projects include the [AsAP](#) (Asynchronous Array of simple Processors) programmable array processor chip, applications, and tools [[ISSCC 2006](#)]; Low Density Parity Check (LDPC) decoders; FFT processors; viterbi decoders; and H.264 video codecs. The 0.18 μm AsAP 1 chip contains 36 programmable processors, operates at over 610 MHz at 2.0 V, and is believed to be the second highest clock rate processor designed in any university. His research group recently completed the design and fabrication of a second generation processing platform with 167 1.2 GHz processors in 65 nm CMOS [[VLSI Symp 2008](#)] which is believed to be the highest clock rate processor designed in any university. The chip contains 164 programmable processors that can each independently control their supply voltage and clock frequency; three highly-configurable special-purpose processors: Fast Fourier transform (FFT), H.264 video motion estimation, and Viterbi decoder; and three 1.3 GHz 16 KB shared memories.



Dr. Baas was an NSF Fellow from 1990-93 and a NASA Graduate Student Researcher Fellow from 1993-96. He received the National Science Foundation [CAREER award](#) in 2006, the Best Paper Award at the IEEE International Conference on Computer Design in 2011, and the Most Promising Engineer/Scientist Award by AISES in 2006. During the summer of 2006 he was a Visiting Professor in Intel's Circuit Research Lab. Since 2007 he has been an [Associate Editor](#) for the *IEEE Journal of Solid-State Circuits*. He has served and is serving as: Program Committee Co-Chair of the IEEE HotChips Symposium on High-Performance Chips in 2011 and Program Committee member in 2009-10; Parallel Architecture Co-Chair of the 2011 Design Automation Conference (DAC) Workshop on Parallel Algorithms, Programming, and Architectures; Technical Program Committee member of the International Conference on Computer Design (ICCD) in 2004-05, 2007-09; Technical Program Committee member of the IEEE International Symposium on Asynchronous Circuits and Systems in 2010; International Solid-State Circuits Conference (ISSCC) Student Research Preview Committee member in 2012; Guest Editor of the March 2012 IEEE Micro Special Issue; and the Technical Advisory Board of an early stage technology company. He is a member of Tau Beta Pi, Phi Kappa Phi, Eta Kappa Nu, AISES, and a Senior Member of the IEEE.

A [short bio](#), and a [slightly longer bio](#) which is not kept up to date.

[My department web page](#)

Research & Students



[VLSI Computation Lab](#) (VCL) home page

Research opening

I currently have an opening for a Ph.D. student with an outstanding academic record. Strong grades are a requirement. A completed MS, research experience, and publications are big pluses. Domestic US status is another big plus. Please contact me if you qualify and are interested. [A few student project examples](#). [A note to interested prospective students](#).

Undergraduate Research

I often have research projects available for UC Davis undergraduate students. I have found a strong GPA is the best predictor of research success so that is fairly important. Please contact me if you are interested.

Research Interests

- Overall: Novel contributions in high-performance and energy-efficient VLSI computation, with an emphasis on digital signal processing workloads
- Processor architectures
- Digital circuits
- Algorithms which map well to hardware (both programmable and special-purpose)
 - Software-defined radios
 - H.264 video encoders and decoders
 - [Fast Fourier Transform processors](#), algorithms, and architectures
 - Turbo decoders
 - Low Density Parity Check (LDPC) decoders
 - Viterbi decoders
- Processor interconnection networks
- Mapping scientific workloads onto single-chip many-core architectures
- VLSI design
- Algorithms and tools for mapping application graphs onto arrays of processors

Misc Items

- [Some hopefully-useful links for graduate students](#)
- [ECE Grad Student Assoc](#)
- [UC Davis AISES](#)
- [Patent 7113559, Oral defense](#)
- [Mind-numbing protests meet pepper spray, April 13, 2012](#)

Other Work

- Design of the baseband transmitter, parts of the receiver, and some system-level blocks in an 802.11a wireless LAN (54 Mbps, 5 GHz) at [Atheros Communications](#)



- [SPIFFEE](#): an energy-efficient single-chip 1024-point FFT processor.



- Other chips:
 - [Spiffee1](#): the first fabricated SPIFFEE processor.
 - Srambb: a 128 x 36bit low-power SRAM. [A few slides](#) (596KB compressed ps) [[die photo](#)]
 - ULP Accumulator 1: a low-voltage memory/adder test chip. [Chip plot](#) (55KB compressed ps)
 - ULP Accumulator 2: a low-voltage memory/adder test chip. [A few slides](#) (586KB compressed ps) [[die photo](#)]
 - Multbb: a 20bit pipelined full-array multiplier. [[die photo](#)]
 - MTC: MCM Test Chip.
- *This work has been supported by [NSF](#), [NASA-GSRP](#) and [AISES-GE](#) fellowships.*

[VLSI & Sig. Processing conferences](#), [MIT Comp Arch list](#)

Recent and Upcoming Presentations

- November 15, 2011; EEC 1 guest lecture, "From Transistors to Processor Architectures: How High-speed Processors are Designed and Built"
- November 9, 2011; ICCAD panel speaker, "Manycore, Heterogeneous, or Neither: Which one is the way to go for EDA?", San Jose, CA.
- October 21, 2011; Tsinghua University, Beijing, China
- October 18, 2011; Zhejiang University, Hangzhou, China
- October 12, 2011; Shanghai Jiao Tong University, Shanghai, China
- October 7, 2011; Fudan University, Shanghai, China
- October 5, 2011; C2S2 Annual Review, CMU, Pittsburgh, PA
- August 11, 2011; Global Foundries Research, Milpitas, CA
- July 1, 2011; Intel Circuit Research Lab
- June 30, 2011; Advanced Micro Devices Research Meeting.
- June 27, 2011; SRC GRC Executive Technical Advisory Board Summer Study, Seattle, WA
- June 5, 2011; "A case for fine-grained many-core processor arrays," Design Automation Conference, Parallel Algorithms Programming, Architectures Workshop.
- June 3, 2011; Corporate Research Seminar.
- April 22, 2011; Native American Admitted Student Reception.
- December 3, 2010; DARPA Workshop, Arlington, VA.
- November 13, 2010; "From Transistors to Processor Architectures: How High-speed Processors are Designed and Built", American Indian Science and Engineering Society (AISES)

- National Conference, Albuquerque, NM.
- November 11, 2010; Corporate Research Seminar.
- October 16, 2010; Northern California Forum for Graduate Diversity, Panel speaker, Sacramento State University, Sacramento, CA.
- October 4, 2010; C2S2 Annual Review, Georgia Tech, Atlanta, GA.
- August 19, 2010; C2S2 Enterprise Systems Review, IBM T.J. Watson Laboratory, Yorktown Heights, NY.
- April 27-29, 2010; SRC Annual Review, Carnegie Mellon University, Pittsburgh, PA.
- October 28, 2009; Intel CRL Circuits Research Lab Seminar, Hillsboro, Oregon.
- October 31, 2009; AISES National Conference; Portland, OR.
- May 15, 2009; Corporate Research Seminar.
- April 15, 2009; NACD Professionals Panel Member, Davis, CA.
- March 25, 2009; Corporate Research Seminar.
- November 8, 2008; Northern California Forum for Graduate Diversity, Panel speaker, Berkeley, CA.
- November 5, 2008; Harvey Mudd College, Claremont, CA.
- October 31-Nov. 1, 2008; AISES National Conference; Anaheim, CA.
- October 30, 2008; UC Riverside, CA.
- October 29, 2008; Westmont College, Santa Barbara, CA.
- October 28, 2008; UC Santa Barbara, CA.
- October 27, 2008; Cal Poly, San Luis Obispo, CA.
- September 25, 2008; Cambridge University, Cambridge, UK.
- September 10-12, 2008; Semiconductor Research Corporation (SRC) annual review meeting, Corvallis, OR.
- September 9, 2008; Intel CRL Circuits Research Lab, Hillsboro, Oregon.
- August 28, 2008; Sun Labs, Menlo Park, CA.
- August 27, 2008; Intelliasys, Cupertino, CA.
- July 11-12, 2008; SRC/NSF/ITRS Forum on 2020 Computing: Virtual Immersion Architectures, Santa Cruz, CA.
- March 21, 2008; Agilent Labs, Santa Clara, CA.
- March 20, 2008; Intelliasys, Cupertino, CA.
- March 14, 2008; Prospective Graduate Student Visit Day, Davis, CA.
- February 20, 2008; Multi-core seminar, Davis, CA.
- November 3, 2007; AISES National Conference; Phoenix, AZ.
- October 29, 2007; [EECS IC Seminar, UC Berkeley](#).
- October 26, 2007; IBM T.J. Watson, Yorktown Heights, NY.
- October 24, 2007; [ECE Graduate Seminar, U Mass, Amherst](#).
- October 24, 2007; Semiconductor Research Corporation (SRC) annual review meeting, Amherst, MA.
- October 8, 2007; Hewlett-Packard Laboratories, Palo Alto, CA.
- May 7, 2007; Distinguished Alumni Scholars Day speaker; Stanford University, Stanford, CA.
- April 27, 2007; Intel CRL Circuits Research Symposium; Invited speaker; Hillsboro, Oregon.
- January 26-27, 2007; Panel member; UC Berkeley Academic Edge Retreat, Bodega Bay, California.
- November 4, 2006; "From Transistors to Processor Architectures: How High-speed Processors are Designed and Built", American Indian Science and Engineering Society (AISES) National Conference, Detroit, Michigan.
- October 24, 2006; "An Asynchronous Array of Simple Processors for DSP Applications", [EE Seminar, University of Washington](#).
- August 21, 2006; "Hardware and Applications of AsAP: An Asynchronous Array of Simple Processors", IEEE HotChips Symposium on High-Performance Chips.
- March 24, 2005; "Algorithms, Architecture, and Circuits for the Efficient Computation of Complex DSP Workloads", [ECE Seminar, Carnegie Mellon University](#).

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Faculty

Departmental Faculty

- [Khaled Abdel-Ghaffar, Professor](#)
- [Venkatesh Akella, Professor and Vice Chair for Graduate Studies](#)
- [Hussain Al-Asaad, Associate Professor](#)
- [Rajeevan Amirtharajah, Associate Professor](#)
- [Bevan M. Baas, Associate Professor](#)
- [G. Rick Branner, Professor](#)
- [Tsu-Shuan Chang, Professor](#)
- [Chen-Nee Chuah, Professor](#)
- [Zhi Ding, Professor](#)
- [Soheil Ghiasi, Associate Professor](#)
- [A. Nazli Gündes, Professor](#)
- [Joshua Hihath, Assistant Professor](#)
- [Charles E. Hunt, Professor](#)
- [Paul J. Hurst, Professor](#)
- [M. Saif Islam, Professor and Vice Chair for Undergraduate Studies](#)

 [Faculty Contact Sheet](#)



- [Linda P. B. Katehi, Professor](#)
- [Richard A. Kiehl, Professor and Chair](#)
- [André Knoesen, Professor](#)
- [Brian H. Kolner, Professor](#)
- [Bernard C. Levy, Professor](#)
- [Stephen H. Lewis, Professor](#)
- [Xiaoguang "Leo" Liu, Assistant Professor](#)
- [N.C. Luhmann, Jr., Professor](#)
- [Omeed Momeni, Assistant Professor](#)
- [Stephen D. O'Driscoll, Assistant Professor](#)
- [John D. Owens, Associate Professor](#)
- [Anh-Vu Pham, Professor](#)
- [Anna Scaglione, Professor](#)
- [Erkin Seker, Assistant Professor](#)
- [Kent Wilken, Professor](#)
- [S.J. Ben Yoo, Professor](#)
- [Qing Zhao, Professor](#)

Adjunct Faculty

- [Ivor Brodie, Adjunct Professor](#)
- [Shu Lin, Adjunct Professor](#)
- [Katsunari Okamoto, Adjunct Professor](#)
- [Diego R. Yankelevich, Adjunct Associate Professor](#)

Emeritus Faculty

- [V. Ralph Algazi](#)
- [Robert W. Bower](#)
- [John N. Churchill](#)
- [Jean-Pierre Colinge](#)
- [K. Wayne Current](#)
- [Andrew Dienes](#)
- [Richard C. Dorf](#)
- [Herman Fink](#)
- [Gary E. Ford](#)
- [William A. Gardner](#)
- [Mohammed S. Ghausi](#)
- [Stephen B. Haley](#)
- [Jonathan P. Heritagge](#)
- [Tien C. "Steve" Hsia](#)
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- [G. Robert Redinbo](#)
- [Ronald A. Soolhoo](#)
- [Richard R. Spencer](#)
- [Shih-Ho Wang](#)

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ELECTRICAL & COMPUTER ENGINEERING





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The revolution in Information Technology has led to laptop computers, wireless communication networks and the Internet. At UC Davis, we believe there is much more to come! Our campus is uniquely positioned to undertake the challenges of the 21st Century. We benefit from our proximity to Silicon Valley, which supplies a wealth of collaborations with the world-leading electronics industry and opens tremendous career opportunities for our graduates. In addition, UC Davis's renowned strength in the Biological Sciences provides a rich environment for studies in bioelectronics, which will allow us to play an important role in the new revolution in biology. In addition to its academic focus, the community of Davis is immersed in natural beauty — with Napa Valley, pristine national parks and dramatic mountains less than an hour away. We hope you will explore this site and contact us to learn more.

News

Afton Geil wins NSF Graduate Research Fellowship

April 16, 2012

Student [Afton Geil](#) mentored by [Professor John Owens](#), wins highly competitive NSF Graduate Research Fellowship.

Dr. Kegin Liu Wins the 2012 Zuhair A. Munir Award

April 12, 2012

The winner of the 2012 Zuhair A. Munir Award for Best Doctoral Dissertation is [Dr. Kegin Liu](#) for his research entitled "On Multi-Armed Bandit in Dynamic Systems". Dr. Liu received his Ph.D. in June 2010. His research was completed under the mentorship of [Professor Qing Zhao](#) in the Department of Electrical and Computer Engineering.

Professor Jerry Woodall, National Medal of Technology Laureate, to Join ECE

March 9, 2012

[Jerry Woodall](#) will join ECE as Distinguished Professor effective July 1, 2012. Woodall is well known for his prolific and seminal contributions to compound semiconductor materials and devices for high-speed circuits and photovoltaic applications. He is also engaged in work on "green" energy storage using bulk aluminum alloys. Woodall, who has co-authored over 350 publications and holds over 60 patents, will add a wealth of industrial and academic experience to the department.

Professor Brian Kolner Elevated to IEEE Fellow

November 29, 2011

Professor [Brian Kolner](#) has been selected for elevation to IEEE Fellow for "contributions to optical waveform analysis and mode locked lasers". IEEE Fellow is conferred upon a person with an "extraordinary record of accomplishments" and is recognized by the technical community as a prestigious honor and an important career achievement. The total number selected in any one year does not exceed 0.1% of the voting membership.

Four New Faculty Join ECE!!!!

November 16, 2011

The UC Davis ECE Department is pleased to announce that four new members will join its faculty this year. Professors [Joshua Hihath](#) and [Erkin Seker](#), who began fall quarter, do research in physical electronics with an emphasis on biology: Hihath from the molecular transport side and Seker from a materials interface perspective. Professors [Xiaoquan "Leo" Liu](#) and [Omeed Momeni](#), who will join this winter and summer, respectively, do research in microwave/mmWave/THz electronics: Liu focuses on micro/nano-electromechanical systems while Momeni studies high-performance circuits and systems.

Graduate Student Anh Tran and Professor Baas Receive Best Paper Award

October 31, 2011

Graduate student Anh Tran and Professor Bevan Baas receive the Best Paper Award at the IEEE International Conference on Computer Design (ICCD), October 2011. Their paper was entitled "RoShaQ: High-Performance On-Chip Router with Shared Queues."

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FACULTY OPENINGS

ELECTRICAL & COMPUTER ENGINEERING P L Y H E R E

SEMINAR SERIES

ABET

Professor Yoo Receives Dean's Faculty Award

September 27, 2011

[Professor Ben Yoo](#) will receive this year's "Outstanding Senior Research Faculty Award" for the College of Engineering. This award will be presented along with others honoring the achievements of outstanding faculty at a reception on November 3rd, 5:00-7:00 pm in the lobby of Kemper Hall.

Professor Stephen O'Driscoll wins the 2011 ASUCD Excellence in Education Award for the College of Engineering

May 26, 2011

[Professor Stephen O'Driscoll](#) was awarded the 2011 ASUCD Excellence in Education Award for the College of Engineering. These teaching awards are completely student-funded, student-nominated, and student-chosen. One award is presented to an outstanding instructor from each college (except for Letters & Science, which has one award for each of its three divisions).

Professor John Owens leads Graphics Systems theme in Center for Visual Computing

April 26, 2011

[Intel's Science and Technology Center](#) for Visual Computing, a \$2.5M/5-year collaboration between Intel and eight universities, includes Associate Professor [John Owens](#) who leads UC Davis's involvement as theme leader in "Graphics Systems" theme within the center. ([ISTC home](#), [Press Release](#))

Dr. Nicolas K. Fontaine Wins the 2011 Zuhair A. Munir Award

April 13, 2011

[Fontaine's](#) Ph.D. research on "[Optical Arbitrary Waveform Generation and Measurement](#)" was completed in June 2010 under the mentorship of ECE [Professor S. J. Ben Yoo](#).

2011 Industrial Affiliates Conference

The Annual Industrial Affiliates Conference will be held on Friday, April 15, 2011. [Click here](#) for more information and registration.

Professor Brian Kolner elected to Fellow of the Optical Society of America

March 11, 2011

[Professor Kolner](#) has been elected to Fellow of the Optical Society of America for "conceiving and developing the optical time lens and for contributions to the understanding of low-frequency noise properties of femtosecond solid state lasers." The OSA Fellow Member designation is awarded to select OSA members who have made significant contributions to the advancement of optics.

Professor Qing Zhao receives Best Paper Award

February 2, 2011

[Professor Qing Zhao](#) was awarded the [2010 IEEE Signal Processing Magazine Best Paper Award](#) for her paper co-authored with Brian M. Sadler of ARL entitled "A Survey of Dynamic Spectrum Access", published in the Vol. 24, No. 3, May 2007 issue. The IEEE Signal Processing Magazine Best Paper Award honors the authors of a paper of exceptional merit and broad interest on a subject related to the Signal Processing Society's technical scope and appearing in the Society's magazine. The award will be presented at the Society's Awards Ceremonies at ICASSP to be held in Prague, Czech Republic, in May, 2011.

Professor Anna Scaglione Elevated to IEEE Fellow

December 16, 2010

[Professor Scaglione](#) has been selected for elevation to IEEE Fellow for "contributions to filterbank precoding for wireless transmission and signal processing for cooperative sensor networks". IEEE Fellow is conferred upon a person with an "extraordinary record of accomplishments" and is recognized by the technical community as a prestigious honor and an important career achievement. The total number selected in any one year does not exceed 0.1% of the voting membership.

Professor Qing Zhao Is Named a 2010-11 Chancellor's Fellow

October 15, 2010

Professor Qing Zhao has been selected as a 2010-11 Chancellor's Fellow. The Chancellor's Fellows Program is supported in part by funds from the Davis Chancellor's Club and the Annual Fund of the University of California, Davis. The Program was established in 2000 to honor the achievements of outstanding faculty members early in their careers. It includes a one-time award of \$25,000 to be used for support of research, teaching, and service activities, together with the designated title Chancellor's Fellow.

ECE Graduate Student Wins Prestigious

NSF Fellowship

April 27, 2010

[Integrated Nanodevices and Nanosystems Lab \(Inano\)](#) masters student Heim Kirin Grewal won the highly competitive and prestigious [National Science Foundation \(NSF\)](#) sponsored Sandia Fellowship 2010. Only twelve fellowships were awarded in the nation. Dr. Jack L. Skinner will be Heim Kirin Grewal's Sandia research supervisor whose work involves plasmonics and nanofabrication; the integration of nano- and microscale devices.

ECE Architecture Course Featured on iTunes U

April 27, 2010

Associate Professor [John Owens's Graphics Architecture](#) class (EEC 277) is now [featured on iTunes U](#).

Professor Islam Receives 2010 Academic Senate Distinguished Teaching Award

April 18, 2010

Professor Saif Islam is one of 3 recipients of this year's Academic Senate Distinguished Teaching Award for undergraduate teaching. The award will be presented at a ceremony in conjunction with other Academic Senate and Academic Federation awards on Tuesday, May 11, 2010 5:30 p.m. in ARC Ballroom A.

[News Archive](#)

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 - Soils & Biogeochemistry
- Landscape Architecture Program
 - Center for Design Research (CDR)
- Law, School of
- Letters and Science (see individual department listings in this list)
- The University Library
- Linguistics

Departments: A-C | D-L | **M-Q** | R-Z

- Management, Graduate School of
- Mathematics
- Mechanical and Aeronautical Engineering
 - Advanced Highway Maintenance and Construction Technology Center
- Medical Pathology
- Medicine, School of
 - Anesthesiology
 - Biochemistry and Molecular Medicine
 - Cardiovascular Medicine
 - Cell Biology and Human Anatomy
 - Dermatology
 - Emergency Medicine
 - Family and Community Medicine
 - Physiology and Membrane Biology
 - Infectious Diseases
 - Internal Medicine
 - Medical Microbiology & Immunology
 - Neurological Surgery
 - Neurology
 - Obstetrics and Gynecology
 - Ophthalmology
 - Pathology
 - Pediatrics
 - Cleft and Craniofacial Reconstruction
 - Pharmacology
 - Physical Medicine and Rehabilitation
 - Psychiatry
 - Public Health Sciences
 - Surgery
 - Urology
- Medieval Studies
- Microbiology
- Military Science
- Molecular and Cellular Biology
- Music
- Native American Studies
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- Neuroscience, Center for
- Nursing, Betty Irene Moore School of
- Nutrition
- Philosophy
- Physics
- Plant Biology
- Plant Pathology
- Plant Sciences
- Political Science
- Population Biology, Graduate Group in
- Psychiatry
- Psychology

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- Religious Studies
- Russian
- School of Law
- School of Medicine
 - See Medicine, School of (above) for full department listing
- School of Nursing (Betty Irene Moore)
- Sociology
- Spanish
- Statistics
- Division of Textiles and Clothing
- Theatre and Dance

- [Veterinary Medicine, School of](#)
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ACADEMICS



Colleges

Undergraduate and graduate reap the benefits of UC Davis interdisciplinary strengths. The university offers the most graduate programs in the University of California system.

- College of Agricultural and Environmental Sciences
- College of Biological Sciences
- College of Engineering
- College of Letters and Science



Schools

Professional students receive a rich education at UC Davis, which has the highest number of professional schools in the University of California system.

- The Betty Irene Moore School of Nursing
- Graduate School of Management
- School of Education
- School of Law
- School of Medicine
- School of Veterinary Medicine



Majors, departments and programs

Academics at UC Davis challenge, stimulate and inspire. We offer more than 100 undergraduate majors and the largest variety of graduate programs — more than 90 — of any University of California campus. Check out our programs on campus and across the world.

- Majors
- Graduate programs of study
- Academic departments
- Special programs
- Summer sessions



International programs

UC Davis attracts more than 5,000 of the brightest international students and scholars from more than 100 countries. In addition, 1,200 of our students study or work abroad each year, building a global academic network.

- Academic centers, institutes and programs
- Study and intern abroad
- International students and scholars
- International partnerships and visitors
- Funding opportunities
- International travel and safety
- Office of the Vice Provost

Classes, schedules, calendar

Use our General Catalog to find the classes you want to take, and then find more details from the class schedule.

- Class search tool
- General Catalog
- Class schedule

- [Academic calendar](#)



Library and collections

From books to bugs, UC Davis' libraries and collections are a treasure trove. The general library alone contains more than 3.9 million volumes and has access to more than 50,000 electronic journals and databases.

- [Libraries](#)



Academic resources

A number of academic resources are available to students, including offices for undergraduate studies and graduate education.

- [Office of the Vice Provost – Undergraduate Studies](#)
- [Graduate Studies](#)
- [Advising and tutoring](#)
- [Veterans' Affairs Office](#)
- [Student Disability Center](#)

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[School of Education 4 pm, June 13](#)

News



- [Hand with sand shovel in virtual sand box with purple stream](#)

Cancer Center earns 'comprehensive' status

UC Davis' newly named Comprehensive Cancer Center is now among the nation's elite for cancer care, research and education.

- [Katehi, student leader urge public support for higher ed \(Sacramento Bee op-ed\)](#)
- [Search begins to replace Vice Chancellor Fred Wood](#)
- [Meteor hunt: Public asked to give to science](#)
- [Washington Post: In time for Memorial Day weekend, UC Davis film expert Scott Simmon on restored WWII film](#)
- [Professor receives \\$5.6M for gratitude research](#)

[more news](#)

Happenings

- [Pitcher throwing ball](#)

May 25-27

Aggies host Irvine over Memorial Day weekend

Baseball fans, don't forget to wear Aggie Blue; 2:30 p.m. Friday, 1 p.m. Saturday and Sunday; Dobbins Stadium, UC Davis

- May 29, June 4 and 7

[Public forums set for candidates for director of athletics](#)

2:30-3:45 p.m., Tercero South's Wall Hall, and ballrooms at Activities and and Recreation Center and Conference Center (see schedule for specific sites), UC Davis

- Wednesday, May 30

['Bats, Birds and Bellflowers: The Evolution of Specialized Pollination in the Neotropics'](#)

12:10-1 p.m., 122 Briggs Hall, UC Davis



- Wed., May 30

[Farm to College dinner](#)

Straight from local farms to the university, 4:30 to 7:30 p.m., central lawn in the Segundo housing area, UC Davis

- Through June 7

[M.F.A. design exhibitions: Dockable Shelter, Soucraft Clothing](#)

Noon-4 p.m. Monday-Friday, 2-4 p.m. Sunday, Design Museum, Cruess Hall, UC Davis

[more happenings](#)



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Admission decisions are in for transfer students

Transfers, don't forget to [submit your Statement of Intent to Register](#) by June 1.

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