

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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GOOGLE LLC,  
Petitioner,

v.

SINGULAR COMPUTING LLC,  
Patent Owner.

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Case No. IPR2023-00394  
Patent No. 10,754,616

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**DECLARATION OF PAUL FRANZON, PHD.**

|                                           |
|-------------------------------------------|
| Google Exhibit 1003<br>Google v. Singular |
|-------------------------------------------|

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I, Paul Franzon, declare:

1. I have been retained by Wolf, Greenfield & Sacks, P.C., counsel for Petitioner Google LLC, to assess claims 1-5, 7-14 and 16-22 and 24 (the “challenged claims”) of U.S. Patent No. 10,754,616 (“the ’616 patent”). I am being compensated for my time at my standard rate of \$500.00 per hour, plus actual expenses. My compensation is not dependent in any way upon the outcome of the *inter partes* review of the ’616 patent.

**I. PERSONAL AND PROFESSIONAL BACKGROUND**

2. I completed my Ph.D. in Electrical and Electronic Engineering in 1989 from the University of Adelaide in Australia. I obtained two additional degrees from the University of Adelaide: a Bachelor of Engineering in Electrical and Electronic Engineering in 1984 and a Bachelor of Science in Physics and Mathematics in 1983.

3. I am currently the Cirrus Logic Distinguished Professor and Director of Graduate Programs in the Department of Electrical and Computer Engineering at North Carolina State University (“NCSU”) in Raleigh, North Carolina. I have been affiliated with NCSU in various roles since 1989.

4. I am a Fellow of the IEEE. I have over 30 years’ experience designing computing devices including microprocessors, array processors,

programmable logic devices, computer interfaces and peripherals. I also have over 30 years of experience in the design and fabrication of processors.

5. From 1985 to 1989, I was doing the research for my PhD at the University of Adelaide and AT&T Bell Laboratories. The title of my PhD thesis was “Fault Tolerance in VLSI”. My thesis discussed 3-D chip technologies, including a flip-chip device comprised of a hybrid wafer scale integration (or HWSI). At the University, I contributed to the design of a programmable parallel signal processing chip, the “Transform and Filter Brick” and analyzed the design for defect tolerance through reconfigurability. While I was a consultant at AT&T Bell Laboratories I designed a reconfigurable array processor of signal processing filter elements. Several publications arose in whole or in part from my PhD. In my PhD thesis I addressed multiple integration issues and technologies, including 3D integration using through silicon vias, and reviewed multiple processor types being designed by other groups leveraging wafer scale integration and 3D technologies.

6. I joined North Carolina State University in 1989. From 1989 to 1994 I taught the graduate course “ECE 521 Computer Design and Technology. This covered the architecture and design of microprocessors, including pipelined designs and cache designs. In 1995, I taught ECE 218, Computer Organization and Microprocessors, which covered the architecture and programming of the M68000 microprocessor. From 1996 to 2011 I taught “Design of Complex Digital

Systems.” That was an undergraduate course (renumbered several times) covering the design of non-pipelined microprocessors, including arithmetic and logic units. Since 1997 I have been teaching ASIC design. This course covers advanced digital design techniques using Verilog RTL and synthesis tools. It includes teaching modules on arithmetic design including adders and multipliers.

7. Over 1990 – 2000 I was the Principal Investigator of several projects investigating the design of processors and led or contributed to the design of several processors, many of which were built. These included a disaggregated superscalar CPU, a heterogeneous multiprocessor, a video processor, an encryption engine, a network processor, and the “Dynamically Programmable Cache.”

8. Over (roughly) 1993 to 1997 I was the principle investigator in a DARPA funded project entitled “Methodology, Tools and Demonstration of MCM System Optimization”. As part of that project, we designed a disaggregated superscalar RISC processor. We also designed and built an encryption processor. In 1995 and 1996 I was a consultant at DCT Inc. was responsible for designing video processors that were compatible with various standards including H.261 and H.263

9. Over (roughly) 1997 to 1999 I had a joint project with HRL Labs entitled “Dynamically Programmable Cache” (DPC). In this project we designed a hybrid FPGA/cache. In the DPC we merged cache with FPGA, placing a row of

FPGA elements between multiple rows of cache memory and repeating. Together with the CPU that the cash served it functioned as a heterogeneous multiprocessor.

10. Since 2000, I have been heavily involved in the design and fabrication of 3D processors integrated using through silicon vias and other technologies.

These included a synthetic aperture radar processor, a 3D memory, a heterogeneous microprocessor stack, that included a cache hierarchy. Recently, my group designed and fabricated a multiprocessor chiplet set intended for integration on top of a silicon interposer substrate. In that microprocessor chip chiplet set, we redesigned a RISC V core so that extension instructions could be defined and run on other chiplets. Some work also continued on the DPC.

11. Over (roughly) 2001 to 2003 I was the NCSU PI of a project entitled “network processor design for just-in-time our optical networking protocols”. As part of that project, we built a network processor using FPGAs. Part of this project continued from 2003 to 2005, under DARPA sponsorship, and with a focus on network security.

12. Over (roughly) 2011 to 2017 I was the PI of an Intel funded project entitled “modular, testable, tightly coupled 3D implementation of a heterogeneous processor”. As part of that project we built a two course stack of heterogeneous micro processes using advanced 3D integration technologies. This project included the design investigation of the 3D x86 heterogeneous course stack.

13. Over (roughly) 2011 to 2016 I was the PI of the DARPA project entitled “3G enabled customized embedded computer”. As part of that project we designed and built a SIMD processor aimed at supporting a wide range of applications with a focus on low power consumption.

14. Since 2017 I led other projects focused on 2.5 D and 3D processor design. As part of the DARPA funded project entitled “2.5 D extendable processor” my team designed and built a disaggregated multiple chip processor that included a RISC-V CPU tightly coupled with instruction-controlled array co-processors aimed at accelerating machine learning tasks. We also designed a 3D programmable processor aimed at machine learning acceleration using an array of the SIMD processes designed in an earlier project.

15. Over my career I have built and tested many integrated circuits ranging using processes from at least the following semiconductor processing nodes: 5  $\mu\text{m}$ , 3  $\mu\text{m}$ , 250 nm, 180 nm, 130 nm, 55 nm, 45 nm, 32 nm, and 28 nm. I have used public domain 45 nm and 15 nm processing kits in my classes

16. I have authored numerous peer reviewed publications relating to processor design. I have also supervised graduate students performing work relating to processor design. I am also the named inventor on numerous patents and patent applications, a number of which relate to the design and fabrication of

computing devices. My CV, which is EX1004, contains a complete list of my publications and patents.

## **II. MATERIALS REVIEWED AND CONSIDERED**

17. My findings, as explained below, are based on my years of education, research, experience, and background in the field of computer processor and co-processor design and implementation, as well as my investigation and study of relevant materials for this declaration. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth in Section IV below. In forming my opinions, I have studied and considered the materials identified in the list below.

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                                                                                                             |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1001           | U.S. Patent No. 10,754,616                                                                                                                                                                                                                                                                     |
| 1002           | Prosecution History of U.S. Patent No. 10,754,616                                                                                                                                                                                                                                              |
| 1005           | Declaration of Dr. Mary K. Bolin                                                                                                                                                                                                                                                               |
| 1006           | PCT Publication WO2005/037326A2 (“Stuttard”)                                                                                                                                                                                                                                                   |
| 1007           | Schmidt et al., “KPROC - An Instruction Systolic Architecture for Parallel Prefix Applications,” <i>Parallel and Distributed Computing Practices</i> Vol. 3, No. 2, pp. 163–178 (2000) (“Schmidt-2000”)                                                                                        |
| 1008           | Schimmler et al., “A bit-serial floating-point unit for a massively parallel system on a chip,” in <i>Parallel Algorithms and Applications</i> , 19:2-3, 79-95 (2004)                                                                                                                          |
| 1009           | Schmidt et al., “A Parallel Accelerator Architecture for Multimedia Video Compression,” in <i>Euro-Par’99, Lecture Notes in Computer Science</i> 1685, Springer Verlag, 1999, pp. 950–960 (“Schmidt-1999”)                                                                                     |
| 1010           | Schimmler et al., “The Instruction Systolic Array – Implementation of a Low-Cost Parallel Architecture as Add-On Board for Personal Computers,” <i>High Performance Computing and Networking, Lecture Notes in Computer Science</i> 797, Springer Verlag, 1994, pp. 487–488 (“Schimmler-1994”) |

| Exhibit | Description                                                                                                                                                                                                              |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1011    | Schimmmler et al., “The Instruction Systolic Array in Image Processing Applications,” Vision Systems: Sensors, Sensor systems, and Components, Europto 96, pp. 136–144 (“Schimmmler-1996”)                               |
| 1012    | Yeh et al., “Parallax: An architecture for real-time physics,” the 34th International Symposium on Computer Architecture (ISCA), 2007, pp. 232-243 (“Yeh-ISCA07”)                                                        |
| 1013    | Yeh et al., “The Art of Deception: Adaptive Precision Reduction for Area Efficient Physics Acceleration,” 40th IEEE/ACM International Symposium on Microarchitecture (MICRO’07), 2007, pp. 394-406 (“Yeh-Micro07”)       |
| 1014    | Yeh et al., “Fool me twice: Exploring and exploiting error tolerance in physics-based animation” (2007)                                                                                                                  |
| 1015    | U.S. Patent No. 5,355,508 (“Kan”)                                                                                                                                                                                        |
| 1016    | G.E. Moore, “Cramming More Components onto Integrated Circuits,” Proceedings of the IEEE, Vol. 86, No. 1 (January 1998)                                                                                                  |
| 1017    | IEEE SSCS Newsletter 36-37 (reprinting Moore, “Progress in Digital Integrated Electronics,” International Electron Devices Meeting, IEEE, 1975, pp. 11-13).                                                              |
| 1018    | <i>Microprocessor Report</i> , “Mendocino Improves Celeron,” Volume 12, Number 11, August 24, 1998                                                                                                                       |
| 1019    | Sim et. al, “MIMD-SIMD hybrid system—towards a new low cost parallel system,” Parallel Computing 29 (2003) pp. 21-36 (“Sim”)                                                                                             |
| 1020    | Taveniku et. al. “The VEGA Moderately Parallel MIMD, Moderately Parallel SIMD, Architecture for High Performance Array Signal Processing,” Proceedings of IPPS/SPDP’98 (IEEE Computer Society), pp 226-232 (“Taveniku”). |
| 1021    | The National Technology Roadmap for Semiconductors, 1997 Edition (“NTRS-1997”)                                                                                                                                           |
| 1022    | International Technology Roadmap for Semiconductor, 1999 Edition (“ITRS-1999”)                                                                                                                                           |
| 1023    | International Technology Roadmap for Semiconductors, 2000 Update (“ITRS-2000”) (from Exhibit B, Folders 1-2 of the Declaration of Nathaniel E Frank-White, EX1029)                                                       |
| 1024    | International Technology Roadmap for Semiconductor, 2002 Update (“ITRS-2002”) (from Exhibit B, Folders 3-7 of the Declaration of Nathaniel E Frank-White, EX1029)                                                        |

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                                                                                                  |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1025           | International Technology Roadmap for Semiconductors, 2004 Update (“ITRS-2004”) (from Folders 8-11 of the Declaration of Nathaniel E Frank-White, EX1029)                                                                                                                            |
| 1026           | International Technology Roadmap for Semiconductors, 2007 Edition (“ITRS-2007”) (from Folders 12-13 of the Declaration of Nathaniel E Frank-White, EX1029)                                                                                                                          |
| 1027           | International Technology Roadmap for Semiconductors, 2009 Edition (“ITRS-2009”) (from Folders 14-15 of the Declaration of Nathaniel E Frank-White, EX1029)                                                                                                                          |
| 1028           | International Technology Roadmap for Semiconductors, 2010 Update (“ITRS-2010”) (from Folder 16 of the Declaration of Nathaniel E Frank-White, EX1029)                                                                                                                               |
| 1029           | Declaration of Nathaniel E Frank-White (November 30, 2022)                                                                                                                                                                                                                          |
| 1030           | International Technology Roadmap for Semiconductor, 2001 Edition (“ITRS-2001”)                                                                                                                                                                                                      |
| 1031           | Declaration of Nathaniel E Frank-White (November 30, 2022)                                                                                                                                                                                                                          |
| 1032           | Declaration of Nathaniel E Frank-White (November 30, 2022)                                                                                                                                                                                                                          |
| 1033           | Gargini, “The International Technology Roadmap for Semiconductors (ITRS): Past, present and future,” GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuits Symposium. 22nd Annual Technical Digest 2000                                                                      |
| 1034           | Tong et al., “Reducing Power by Optimizing the Necessary Precision/Range of Floating-Point Arithmetic,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 3, June 2000 (“Tong”) (from pages 6-19 of the Declaration of Gerard P. Grenier, EX1035)       |
| 1035           | Declaration of Gerard P. Grenier regarding Tong et al., Reducing Power by Optimizing the Necessary Precision/Range of Floating-Point Arithmetic, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 3, June 2000                                         |
| 1036           | Shirazi et al., “Quantitative Analysis of Floating Point Arithmetic on FPGA Based Custom Computing Machines,” Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, April 19-21, 1995 (“Shirazi”) (from pages 6-13 of Declaration of Gordon MacPherson, EX1037) |
| 1037           | Declaration of Gordon MacPherson regarding Shirazi et al., Quantitative Analysis of Floating Point Arithmetic on FPGA Based Custom Computing Machines, Proceedings of the IEEE Symposium                                                                                            |

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                                                             |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | on FPGAs for Custom Computing Machines, April 19-21, 1995                                                                                                                                                                                      |
| 1038           | Altera Product Catalog (2008) (from pages 82-153 of Declaration of Nathaniel E Frank-White, EX1047)                                                                                                                                            |
| 1039           | Stackhouse et al., “A 65 nm 2-Billion Transistor Quad-Core Itanium Processor,” in IEEE Journal of Solid-State Circuits, vol. 44, no. 1, pp. 18-31, Jan. 2009 (“Intel-Itanium”)                                                                 |
| 1040           | Dell White Paper, “Performance Analysis of Intel® Pentium® M and Pentium 4 Processors,” July 2005. (“Pentium-4”) (from pages 61-65 of Declaration of Nathaniel E Frank-White, EX1047)                                                          |
| 1041           | The Guru of 3D Report on Radeon HD Series 5700 (“Radeon-5700”) (from pages 10-11 of Declaration of Nathaniel E Frank-White, EX1047)                                                                                                            |
| 1042           | “Intel Core 2 Extreme QX9650 – Penryn Ticks Ahead,” Anandtech.com (Oct. 29, 2007) (from pages 30-40 of Declaration of Nathaniel E Frank-White, EX1047)                                                                                         |
| 1043           | TSMC Report (2008), “TSMC Ramps Most Advanced Available Process Technology to Volume Production” (pr.tsmc.com/english/news/1526) (“TSMC-40nm”)                                                                                                 |
| 1044           | “Updated CPU Cheatsheet – Seven Years of Covert CPU Operations,” Anandtech.com (Aug. 28, 2004) (from pages 42-49 of Declaration of Nathaniel E Frank-White, EX1047)                                                                            |
| 1045           | Natarajan et al., “A 32nm logic technology featuring 2nd-generation high-k + metal-gate transistors, enhanced channel strain and 0.171µm <sup>2</sup> SRAM cell size in a 291Mb array,” 2008 IEEE International Electron Devices Meeting, 2008 |
| 1047           | Declaration of Nathaniel E Frank-White (December 10, 2022) (742000)                                                                                                                                                                            |
| 1048           | Declaration of Nathaniel E Frank-White (December 12, 2022) (744136)                                                                                                                                                                            |
| 1049           | PCT Publication WO2002/065700A2                                                                                                                                                                                                                |
| 1050           | UK Patent Appl. Publ. No. GB 2,415,561                                                                                                                                                                                                         |
| 1051           | UK Patent Appl. Publ. No. GB 2,390,506                                                                                                                                                                                                         |
| 1052           | “Intel’s 32nm Update: The Follow-on to Core i7 and More,” Anandtech.com (Feb. 11, 2009) (from pages 21-28 of Declaration of Nathaniel E Frank-White, EX1047)                                                                                   |
| 1053           | “AMD Evergreen: 40nm DirectX 11 GPU Silicon Arrives,” Anandtech.com (June 3, 2009) (from pages 16-19 of Declaration of Nathaniel E Frank-White, EX1047)                                                                                        |
| 1054           | U.S. Patent Appl. Publ. No. 2007/0258641A1                                                                                                                                                                                                     |
| 1055           | U.S. Provisional Application No. 61/218691                                                                                                                                                                                                     |
| 1058           | U.S. Patent Appl. Publ. No. 2003/0033509A1                                                                                                                                                                                                     |

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                                                         |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1059           | U.S. Patent Appl. Publ. No. 2008/0288823A1                                                                                                                                                                                                 |
| 1063           | U.S. Patent Appl. Publ. No. 2009/0148068A1                                                                                                                                                                                                 |
| 1066           | U.S. Patent Appl. Publ. No. 2009/0114952A1                                                                                                                                                                                                 |
| 1067           | U.S. Patent Appl. Publ. No. 2006/0088958A1                                                                                                                                                                                                 |
| 1068           | U.S. Patent Appl. Publ. No. 2008/0023700A1                                                                                                                                                                                                 |
| 1069           | U.S. Patent Appl. Publ. No. 2009/0150112A1                                                                                                                                                                                                 |
| 1070           | U.S. Patent Appl. Publ. No. 2005/0237327A1                                                                                                                                                                                                 |
| 1075           | U.S. Patent No. 5,226,142                                                                                                                                                                                                                  |
| 1076           | U.S. Patent No. 6,681,059                                                                                                                                                                                                                  |
| 1077           | U.S. Patent No. 7,243,165 (“Kravec”)                                                                                                                                                                                                       |
| 1078           | U.S. Patent No. 7,072,872 (“Caid”)                                                                                                                                                                                                         |
| 1080           | U.S. Patent No. 6,963,891                                                                                                                                                                                                                  |
| 1081           | U.S. Patent No. 6,825,857                                                                                                                                                                                                                  |
| 1082           | U.S. Patent No. 6,353,867                                                                                                                                                                                                                  |
| 1083           | U.S. Patent No. 6,477,610                                                                                                                                                                                                                  |
| 1084           | U.S. Patent No. 5,581,773                                                                                                                                                                                                                  |
| 1087           | U.S. Patent No. 6,700,142                                                                                                                                                                                                                  |
| 1088           | VSI Alliance™: Virtual Component Interface Standard Version 2 (OCB 2 2.0) (April 2001)                                                                                                                                                     |
| 1089           | “Port,” in Microsoft Computer Dictionary, p. 412 (5th. ed. 2002)                                                                                                                                                                           |
| 1092           | Aty et al., “High-Speed, Area-Efficient FPGA-Based Floating-Point Multiplier,” Proceedings of the 12 IEEE International Conference on Fuzzy Systems, December 11, 2003 (“Aty”) (from p. 14-17 of Declaration of Gordon MacPherson, EX1093) |
| 1093           | Declaration of Gordon MacPherson regarding Aty et al., High-Speed, Area-Efficient FPGA-Based Floating-Point Multiplier, Proceedings of the 12 IEEE International Conference on Fuzzy Systems, December 11, 2003                            |
| 1094           | Chen et al., “A cost effective 32nm high-K/ metal gate CMOS technology for low power applications with single-metal/gate-first process,” 2008 Symposium on VLSI Technology, 2008, pp. 67-68                                                |
| 1095           | Prosecution History of PCT/GB2004004377                                                                                                                                                                                                    |
| 1096           | U.S. Patent No. 4,450,402                                                                                                                                                                                                                  |
| 1097           | Schiml et al., “A 0.13 /spl mu/m CMOS platform with Cu/low-k interconnects for system on chip applications,” 2001 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.01 CH37184), 2001, pp. 101-102                    |
| 1098           | Sudha et al., “An Efficient Digital Architecture for Principal                                                                                                                                                                             |

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                                                                 |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | Component Neural Network and its FPGA Implementation,” IETE Journal of Research, Vol. 53, No. 5, September-October 2007, ISSN 0377-2063, pp. 425-431 (“Sudha”)                                                                                     |
| 1100           | Oh et al., “A fully pipelined single-precision floating-point unit in the synergistic processor element of a CELL processor,” in IEEE Journal of Solid-State Circuits, vol. 41, no. 4, pp. 759-771, April 2006,                                    |
| 1103           | Prabhu, “SOMGPU: An unsupervised pattern classifier on Graphical Processing Unit,” 2008 IEEE Congress on Evolutionary Computation (IEEE World Congress on Computational Intelligence), 2008, pp. 1011-1018                                         |
| 1104           | Poli et al., “Processing Neocognitron of Face Recognition on High Performance Environment Based on GPU with CUDA Architecture,” 2008 20th International Symposium on Computer Architecture and High Performance Computing, 2008, pp. 81-88         |
| 1105           | Ligon et al., “A re-evaluation of the practicality of floating-point operations on FPGAs,” Proceedings. IEEE Symposium on FPGAs for Custom Computing Machines (Cat. No.98TB100251), 1998, pp. 206-215                                              |
| 1106           | Held, “From a Few Cores to Many: A Tera-scale Computing Research Overview,” white paper, Intel, 2006 (from pages 67-78 of Declaration of Nathaniel E Frank-White, EX1047)                                                                          |
| 1107           | Reddaway et al., “Ultra-high performance, low-power, data parallel radar implementations,” IEEE International Radar Conference, 2005., 2005, pp. 822-826                                                                                           |
| 1108           | Lokhmotov et al., “Revisiting SIMD Programming,” Languages and Compilers for Parallel Computing: 20th International Workshop, LCPC 2007, Urbana, IL, USA, October 11-13, 2007, Revised Selected Papers. Springer-Verlag, Berlin, Heidelberg, 32–46 |
| 1109           | U.S. Patent No. 4,534,010                                                                                                                                                                                                                          |
| 1110           | Shahbahrami et al., “Optimization of Content-Based Image Retrieval Functions,” 2008 Tenth IEEE International Symposium on Multimedia, 2008, pp. 607-612                                                                                            |
| 1111           | Noumsi et al., “Acceleration of a content-based image-retrieval application on the RDISK cluster,” Proceedings 20th IEEE International Parallel & Distributed Processing Symposium, 2006                                                           |
| 1112           | Proceedings 20th IEEE International Parallel & Distributed Processing Symposium, 2006 (TOC)                                                                                                                                                        |

| Exhibit | Description                                                                                                                                                                                                                                               |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1113    | Pengdong et al., “Performance Comparison between Color and Spatial Segmentation for Image Retrieval and Its Parallel System Implementation,” 2008 International Symposium on Computer Science and Computational Technology, 2008, pp. 539-543             |
| 1114    | Bradley et al., “Exploiting Loop-Level Parallelism for SIMD Arrays Using OpenMP,” 89-100 (2007) (attachment 13c to Declaration of Dr. Mary K. Bolin, EX1005)                                                                                              |
| 1115    | Haran et al., “22 nm technology compatible fully functional 0.1 $\mu\text{m}^2$ 6T-SRAM cell,” 2008 IEEE International Electron Devices Meeting, 2008, pp. 1-4                                                                                            |
| 1116    | Tong et al., Sean & Hahn, Scott. (2008). Operating System Support for Shared-ISA Asymmetric Multi-core Architectures.                                                                                                                                     |
| 1117    | Borkar, “Thousand Core Chips A Technology Perspective,” Proceedings of the 44th ACM/IEEE Design Automation Conference, pp. 746-749 (2007) (attachment 11b to Declaration of Dr. Mary K. Bolin, EX1005)                                                    |
| 1118    | “ClearSpeed kicks it up a notch,” Arstechnica.com (Oct. 11, 2004) (from pages 5-6 of Declaration of Nathaniel E Frank-White, EX1123)                                                                                                                      |
| 1119    | U.S. Patent No. 7,447,873                                                                                                                                                                                                                                 |
| 1120    | Manocha, “General-purpose computations using graphics processors,” in Computer, vol. 38, no. 8, pp. 85-88, Aug. 2005                                                                                                                                      |
| 1122    | U.S. Patent Appl. Publ. No. 2009/0183167A1                                                                                                                                                                                                                |
| 1123    | Declaration of Nathaniel E Frank-White (December 12, 2022)                                                                                                                                                                                                |
| 1124    | Burger et al., “Composable Multicore Chips,” in Multicore Processors and Systems. Integrated Circuits and Systems (Springer 2009)                                                                                                                         |
| 1125    | Roma et al., “In the development and evaluation of specialized processors for computing high-order 2-D image moments in real-time,” in Proceedings Fifth IEEE International Workshop on Computer Architectures for Machine Perception, pp. 170-179 (2000) |
| 1126    | “Intel Developer Forum 22nm News Facts,” Intel Corporation (Sept. 22, 2009) (from page 80 of Declaration of Nathaniel E Frank-White, EX1047)                                                                                                              |
| 1127    | Declaration of Gordon MacPherson regarding EX1013                                                                                                                                                                                                         |
| 1128    | Declaration of Gordon MacPherson regarding EX1039                                                                                                                                                                                                         |
| 1129    | Declaration of Gordon MacPherson regarding EX1045                                                                                                                                                                                                         |
| 1130    | Declaration of Gordon MacPherson regarding EX1094                                                                                                                                                                                                         |
| 1131    | Declaration of Gordon MacPherson regarding EX1097                                                                                                                                                                                                         |
| 1133    | Declaration of Gordon MacPherson regarding EX1100                                                                                                                                                                                                         |
| 1134    | Declaration of Gordon MacPherson regarding EX1110                                                                                                                                                                                                         |

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                                                                            |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1135           | Declaration of Gordon MacPherson regarding EX1115                                                                                                                                                                                                             |
| 1136           | Declaration of Gordon MacPherson regarding EX1125                                                                                                                                                                                                             |
| 1137           | TSMC Press Release, “TSMC Ramps 40nm Volume Production to Promote Innovation as Foundries Assume a Larger Role for \$300 Billion Industry” (Nov. 17, 2008)                                                                                                    |
| 1138           | Thornton et al., “Tradeoff analysis of integer multiplier circuits implemented in FPGAs,” in 1999 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing (PACRIM 1999). Conference Proceedings (Cat. No.99CH36368), 1999, pp. 301-304 |

### **III. MY UNDERSTANDING OF PATENT LAW**

18. In developing my opinions, I discussed various relevant legal principles with Petitioner’s attorneys. Though I do not purport to have prior knowledge of such principles, I understood them when they were explained to me and have relied upon such legal principles, as explained to me, in the course of forming the opinions set forth in this declaration. My understanding in this respect is as follows:

19. I understand that “*inter partes* review” (IPR) is a proceeding before the United States Patent & Trademark Office for evaluating the patentability of an issued patent’s claims based on prior-art patents and printed publications.

20. I understand that, in this proceeding, Petitioner has the burden of proving that the challenged claims of the ’616 patent are unpatentable by a preponderance of the evidence. I understand that “preponderance of the evidence” means that a fact or conclusion is more likely true than not true.

21. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a person of ordinary skill in the art (“POSA”) in the context of the entire patent and the prosecution history pertaining to the patent. If the specification provides a special definition for a claim term that differs from the meaning the term would otherwise possess, the specification’s special definition controls. If a claim element is expressed as a “means” for performing a specified function, I understand that it covers the corresponding structure described in the specification and equivalents of the described structure. I have applied these standards in preparing the opinions in this declaration.

22. I understand that determining whether a particular patent or printed publication constitutes prior art to a challenged patent claim can require determining the effective filing date (also known as the priority date) to which the challenged claim is entitled. I understand that for a patent claim to be entitled to the benefit of the filing date of an earlier application to which the patent claims priority, the earlier application must have described the claimed invention in sufficient detail to convey with reasonable clarity to the POSA that the inventor had possession of the claimed invention as of the earlier application’s filing date. I understand that a disclosure that merely renders the claimed invention obvious is

not sufficient written description for the claim to be entitled to the benefit of the filing date of the application containing that disclosure.

23. I understand that for an invention claimed in a patent to be patentable, it must be, among other things, new (novel—*i.e.*, not anticipated) and not obvious from the prior art. My understanding of these two legal standards is set forth below.

**A. Anticipation**

24. I understand that, for a patent claim to be “anticipated” by the prior art (and therefore not novel), each and every limitation of the claim must be found, expressly or inherently, in a single prior-art reference. I understand that a claim limitation is disclosed for the purpose of anticipation if a POSA would have understood the reference to disclose the limitation based on inferences that a POSA would reasonably be expected to draw from the explicit teachings in the reference when read in light of the POSA’s knowledge and experience.

25. I understand that a claim limitation is inherent in a prior art reference if that limitation is necessarily present when practicing the teachings of the reference, regardless of whether a person of ordinary skill recognized the presence of that limitation in the prior art.

## **B. Obviousness**

26. I understand that a patent claim may be unpatentable if it would have been obvious in view of a single prior-art reference or a combination of prior-art references.

27. I understand that a patent claim is obvious if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the relevant field at the time the invention was made. Specifically, I understand that the obviousness question involves a consideration of:

- the scope and content of the prior art;
- the differences between the prior art and the claims at issue;
- the knowledge of a person of ordinary skill in the pertinent art; and
- if present, objective factors indicative of non-obviousness, sometimes referred to as “secondary considerations.”

28. I understand that such secondary considerations include: (a) commercial success of a product due to the merits of the claimed invention; (b) a long-felt, but unmet need for the invention; (c) failure of others to find the solution provided by the claimed invention; (d) deliberate copying of the invention by others; (e) unexpected results achieved by the invention; (f) praise of the invention by others skilled in the art; (g) the taking of licenses under the patent by others; and (h) evidence that the patentee proceeded contrary to the accepted wisdom of

the prior art. I understand that secondary considerations are relevant where there is a connection, or nexus, between them and the claimed invention. I have reviewed Section XVI of the Petition regarding the alleged secondary considerations in the patent owner's prior IPRs involving related patents. I have relied on the Petition's analysis that the patent owner's alleged evidence of secondary considerations was too speculative and failed to establish the required nexus with any challenged claim, and therefore I have not considered the alleged secondary considerations in forming my opinions regarding obviousness of the '616 patent's claims.

29. I understand that in order for a claimed invention to be considered obvious, a POSA must have had a reason for combining teachings from multiple prior-art references (or for altering a single prior-art reference, in the case of obviousness in view of a single reference) in the fashion proposed.

30. I further understand that in determining whether a prior-art reference would have been combined with other prior art or with other information within the knowledge of a POSA, the following are examples of approaches and rationales that may be considered:

- combining prior-art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of a known technique to improve similar devices in the same way;

- applying a known technique to a known device ready for improvement to yield predictable results;
- applying a technique or approach that would have been “obvious to try,” *i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success.
- known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior-art reference or to combine prior-art reference teachings to arrive at the claimed invention. I understand that this teaching, suggestion or motivation may come from a prior-art reference or from the knowledge or common sense of one of ordinary skill in the art.

31. I understand that for a single reference or a combination of references to render the claimed invention obvious, a POSA must have been able to arrive at the claimed invention by altering or combining the applied references.

#### **IV. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)**

32. I have been informed and understand that for purposes of assessing whether prior-art references disclose every element of a patent claim (thus “anticipating” the claim) and/or would have rendered the claim obvious, the patent and the prior-art references must be assessed from the perspective of a person having ordinary skill in the art (“POSA”) to which the patent is related, based on the understanding of that person at the time of the patent claim’s priority date. I

have been informed and understand that a POSA is presumed to be aware of all pertinent prior art and the conventional wisdom in the art, and is a person of ordinary creativity. I have applied this standard throughout my declaration.

33. The '616 patent involves technology in the field of computing. I have been asked to provide my opinions as to the state of the art in this field by 2009. I use this timeframe because the face of the '616 patent indicates an earliest claimed priority date of the June 19, 2009 filing date of a provisional application. EX1001, (60). Unless I specify otherwise, whenever I offer an opinion in this declaration about the knowledge of a POSA, the manner in which a POSA would have understood the claims of the '616 patent or its description, the manner in which a POSA would have understood the prior art, or what a POSA would have been led to do based on the prior art, I am referencing the 2009 timeframe, even if I do not say so specifically in each case.

34. I understand that the Patent Owner may attempt to prove that the alleged invention recited in the challenged claims was conceived at some time prior to the earliest claimed priority date on the face of the patent (June 19, 2009). At the time of this declaration, I am unaware of the Patent Owner having alleged any earlier conception date or produced any evidence to establish any earlier conception date.

35. In my opinion, a POSA in 2009 or 2010 would have had at least a bachelor's degree in Electrical Engineering, Computer Engineering, Applied Mathematics or the equivalent, and at least two years of academic or industry experience in computer architecture. More education could substitute for experience, and vice versa. This person would have been capable of understanding and applying the teachings of the prior-art references discussed in this declaration, and the teachings of the '616 patent to the extent of the written description and enablement it provides.

36. By 2009, I held a Ph.D. in Electrical Engineering, and I had 20+ years of experience in computer architecture, including the design of microprocessors and parallel processing systems. Therefore, I was a person of more than ordinary skill in the art during the relevant timeframe. However, I worked with many people who fit the characteristics of the POSA, and I am familiar with their level of skill. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth above.

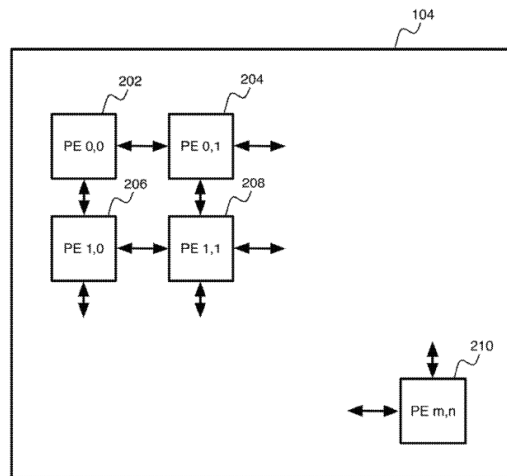
## **V. THE '616 PATENT**

### **A. Specification of the '616 Patent**

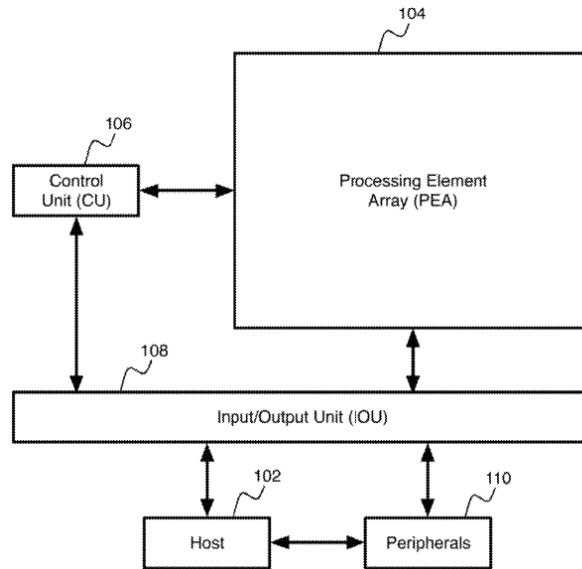
37. The '616 patent describes a decades-old architecture that was well-known for facilitating parallel computations: an array of interconnected processing elements (PE's) each having a local memory and an arithmetic unit configured to

perform desired arithmetic operations. The '616 patent itself acknowledges and discusses many such examples, including single-instruction multiple-data (SIMD) arrays, multiple-instruction multiple-data (MIMD) arrays and massively-parallel computing systems that used such architectures dating back to the 1980s and 1990s (and before). '616 patent, 3:20-5:36.

38. The '616 patent describes the use of low-precision high-dynamic range (LPHDR) PEs using this well-known architecture of interconnecting PEs into an array of processors to perform parallel computations, as illustrated in Fig. 2 of the '616 patent reproduced below. '616 patent, 9:39-56.



39. The '616 patent utilizes this PE array in a conventional computer system with a host computer that utilizes the PE array for parallel processing, as illustrated in FIG. 1 of the '616 patent reproduced below. '616 patent, 8:12-9:38.



40. Contrary to the '616 specification's allegation that it was "commonly believed" among persons of ordinary skill in the art that LPHDR was either "not practical" or "not useful," ('616 patent, 6:57-66), low precision processing elements with high dynamic range were well-known as were the benefits of LPHDR arithmetic in minimizing resource consumption—including reduced area and power consumption as discussed in §V.D below in connection with the challenged independent claims and further in my analysis of the grounds of unpatentability of the challenged claims in §VII.

41. The bulk of the '616 specification describes logarithmic and analog embodiments of LPHDR processing elements in the above architecture (11:57-24:61), which the inventor's use of simulation on a conventional computer to show that example applications could tolerate low precision computations was not implemented at the time. '616 patent, 17:41-23:42. As discussed in further detail

below, the claims of the '616 patent are not directed to these techniques, but are instead drawn to processing elements with floating-point multipliers the '616 patent mentions once to compare the relatively large size of such multipliers with logarithmic and analog implementations.

42. In particular, '616 patent's specification has one isolated statement that "[i]f [some LPHDR] values were represented and manipulated using the methods of floating point arithmetic, they would have binary mantissas of no more than 10 bits plus a sign bit and binary exponents of at least 5 bits plus a sign bit. However, the circuits to multiply and divide these floating point values would be relatively large." '616 patent, 5:66-6:6. The specification thus criticizes this option and spends the remainder of the specification describing the logarithmic and analog embodiments.

## **B. Prosecution History of the '616 Patent**

43. I have reviewed the prosecution history of the '616 patent (EX1002). The examiner allowed the claims of the '616 patent without substantively discussing any prior art. Based on my review of the file history and the patent, the examiner allowed the claims of the '616 patent as originally filed, providing only a brief summary of three prior art patents the examiner indicated were "not relied upon" but "considered pertinent to the applicant's disclosure" without any analysis

of how they pertain to the claims. See EX1002, 137-152 (originally-filed claims), 9-19 (Notice of Allowance and brief summary of prior art patents not relied upon).

44. The '616 patent claims priority through a chain of “continuation” applications. I understand from counsel that in the file histories of the applications to which the '616 patent claims priority, the examiner also allowed the claims in those patents without substantively discussing any prior art. I understand from counsel that in some cases, the examiner issued “double patenting” rejections over claims in previous patents in the priority chain, which the applicant overcame by filing terminal disclaimers or filing a new set of claims.

### **C. Priority Dates**

45. The '616 patent claims priority to a 2009 provisional application, Provisional Application No. 61/218,619 (EX1055) (the “'619 Provisional”). See '616 patent, code (60). In my opinion, the '619 Provisional does not describe at least claims 7-15, which recite “*no less than 5000*” processing elements.

46. The '619 Provisional disclosed only that in “certain embodiments” the number of “LPHDR arithmetic elements...significantly exceeds (e.g., by at least 20 more than three times) the number of arithmetic elements” of “traditional precision,” which discloses neither a number of LPHDR elements, nor what number of traditional-precision elements the number of LPHDR elements “significantly exceeds.” EX1055, 8. In my opinion, this disclosure is not a full,

clear, concise and exact description of an array of processing elements numbering “no less than 5000,” which I understand from counsel would be required to satisfy the written description requirement. In my opinion, a POSA reading the ’619 Provisional would not immediately discern that the “no less than 5000 limitation” was described in the provisional.

47. Although it would have been obvious to a POSA to integrate as many processing elements as semiconductor processing permitted (as I discuss in §IX.A below), I understand from counsel that obviousness does not satisfy the written description requirement.

48. Thus, in my opinion, independent claim 7 and its respective dependent claims (8-15) are not described in the ’619 Provisional and so, I understand from counsel, the ’616 patent is not entitled to claim priority to the provisional application’s 2009 filing date. I understand that the next-earliest application to which the ’616 patent claims priority was filed June 15, 2010. See ’616 patent, code (63). I have been informed by counsel that continuation applications share the same specification so that the ’616 patent would have the same disclosure as the June 2010 application and therefore would have contained the first mention 5000 processing elements.

#### **D. The Challenged Claims**

49. Challenged independent claims 1, 7 and 16 each recite a decades-old processing element (PE) array architecture that was well-known for facilitating parallel computations as discussed above. Further limitations recite conventional computer system components including a “*computing chip*” for the PE array, a “*host computer*,” an “*input-output unit*,” and a “*host connection*,” as also discussed above.

50. The recited PEs include respective multiplier circuits adapted to receive floating-point values having a “*binary mantissa of width no more than 11 bits*” and a “*binary exponent of width at least 6 bits.*” Such floating-point formats (in which a binary number can be represented as a fractional “mantissa” (greater than 1 and less than 2) scaled by a power of two (the power being the “exponent”)) were also decades old. The number of mantissa bits in a floating-point value determines the “precision” of the value. Precision relates to the ability to represent numbers that differ from each other by small amounts—*e.g.*, fractional values. For example, in a decimal (base-10) representation, the number 2.13 (represented using two fractional digits) is more precise than if rounded to 2.1 (using just one fractional digit), which is more precise than if rounded to 2 (using no fractional digits).

51. The number of exponent bits in a floating-point number relates to the dynamic range of the number. A simple example of a floating-point representation of a decimal number using base ten would represent the number 3,046,000 as  $3.046 \times 10^6$ . In a typical binary (base-2) floating-point representation, one bit is allocated to indicate the number's sign (positive or negative), some bits are allocated to specify the "exponent" (the number's order of magnitude in base two), and other bits are allocated to specify the mantissa. See, e.g., EX1013 ("Yeh-Micro07"), 395-396 ("The IEEE standard single precision FP representation has a single sign bit (S), eight exponent bits (E), and 23 mantissa bits (M).... Precision reduction, as used in this study, refers to the removal of less significant bits from the mantissa...."); Tong (EX1034), 274 ("There are two different IEEE standards for FP computation. IEEE 754 is a binary standard that requires the implied radix (base) to be two. IEEE 854 allows either radix 2 or radix 10 representation. By far, IEEE 754 is more popular and most desktop microprocessors support the IEEE 754 standard.").

52. It was well known that using reduced-precision floating-point formats (e.g., formats in which the bitwidth of the mantissa is reduced below the standard single precision format) had benefits. Tong (EX1034) demonstrated that for a variety of image and signal processing applications there was "no noticeable degradation in accuracy" (Tong, 278) when the mantissa of floating-point operands

was reduced to 11 bits, with multiple applications (including floating discrete cosine transform (DCT) tolerating even further reduction in the bit-width of the mantissa (e.g., down to as low as 5 bits), but that the exponent bits could not be reduced significantly from 8-bits. Tong, 273, 278-279 (“we can reduce, but not reduce dramatically, the number of exponent bits but the fine precision of the 23-bit mantissa is not essential”).

53. Claim 7 recites that there are “no less than 5000” PEs in the array. The ’616 patent describes no implementation of 5000 processors integrated on a single chip. The ’616 patent only references 5000 PEs once (’616 patent, 28:46-51), among a generalized, boilerplate description of “certain embodiments,” all but one of which have significantly fewer than 5000 PEs (*id.*, 28:13-51) and fewer than 1024 processors integrated on the KPROC-chip. Furthermore, the ’616 patent does not describe any number of PEs as being critical, nor does the ’616 patent disclose that qualitatively different functionality could be performed or that integrating 5000 PEs on a chip produced any new or unexpected results, only the expected result of increasing computational performance.

## **VI. PRIOR-ART REFERENCES**

### **A. Public Accessibility of Non-patent Prior Art Exhibits**

54. My opinions regarding public accessibility of the following exhibits are discussed in my Appendix attached hereto in the sections of my Appendix summarized in the table below:

| <b>Exhibit</b> | <b>Appendix Section</b> |
|----------------|-------------------------|
| <b>1007</b>    | §II.A.1                 |
| <b>1009</b>    | §II.A.2                 |
| <b>1010</b>    | §II.A.3                 |
| <b>1011</b>    | §II.A.4                 |
| <b>1012</b>    | §II.C.1                 |
| <b>1013</b>    | §II.C.2                 |
| <b>1014</b>    | §II.C.3                 |
| <b>1016</b>    | §II.C.4                 |
| <b>1017</b>    | §II.C.5                 |
| <b>1018</b>    | §II.C.6                 |
| <b>1019</b>    | §II.C.7                 |
| <b>1020</b>    | §II.C.8                 |
| <b>1021</b>    | §II.B.1                 |
| <b>1022</b>    | §II.B.2                 |
| <b>1023</b>    | §II.B.3                 |
| <b>1024</b>    | §II.B.5                 |
| <b>1025</b>    | §II.B.6                 |
| <b>1026</b>    | §II.B.7                 |
| <b>1027</b>    | §II.B.8                 |
| <b>1030</b>    | §II.B.4                 |
| <b>1034</b>    | §II.C.43                |

|             |          |
|-------------|----------|
| <b>1036</b> | §II.C.44 |
| <b>1038</b> | §II.C.9  |
| <b>1039</b> | §II.C.10 |
| <b>1040</b> | §II.C.11 |
| <b>1041</b> | §II.C.12 |
| <b>1042</b> | §II.C.13 |
| <b>1043</b> | §II.C.14 |
| <b>1044</b> | §II.C.15 |
| <b>1045</b> | §II.C.16 |
| <b>1088</b> | §II.C.19 |
| <b>1092</b> | §II.C.45 |
| <b>1094</b> | §II.C.20 |
| <b>1097</b> | §II.C.21 |
| <b>1098</b> | §II.C.22 |
| <b>1100</b> | §II.C.23 |
| <b>1103</b> | §II.C.24 |
| <b>1104</b> | §II.C.25 |
| <b>1105</b> | §II.C.26 |
| <b>1106</b> | §II.C.27 |
| <b>1107</b> | §II.C.28 |
| <b>1108</b> | §II.C.29 |
| <b>1110</b> | §II.C.30 |
| <b>1111</b> | §II.C.31 |
| <b>1113</b> | §II.C.32 |
| <b>1114</b> | §II.C.33 |
| <b>1115</b> | §II.C.34 |
| <b>1116</b> | §II.C.35 |
| <b>1117</b> | §II.C.36 |
| <b>1118</b> | §II.C.37 |

|             |          |
|-------------|----------|
| <b>1120</b> | §II.C.38 |
| <b>1124</b> | §II.C.39 |
| <b>1125</b> | §II.C.40 |
| <b>1126</b> | §II.C.41 |
| <b>1137</b> | §II.C.42 |
| <b>1138</b> | §II.C.46 |

## **VII. THE CHALLENGED CLAIMS ARE UNPATENTABLE IN LIGHT OF THE PRIOR ART IDENTIFIED IN THE PETITION**

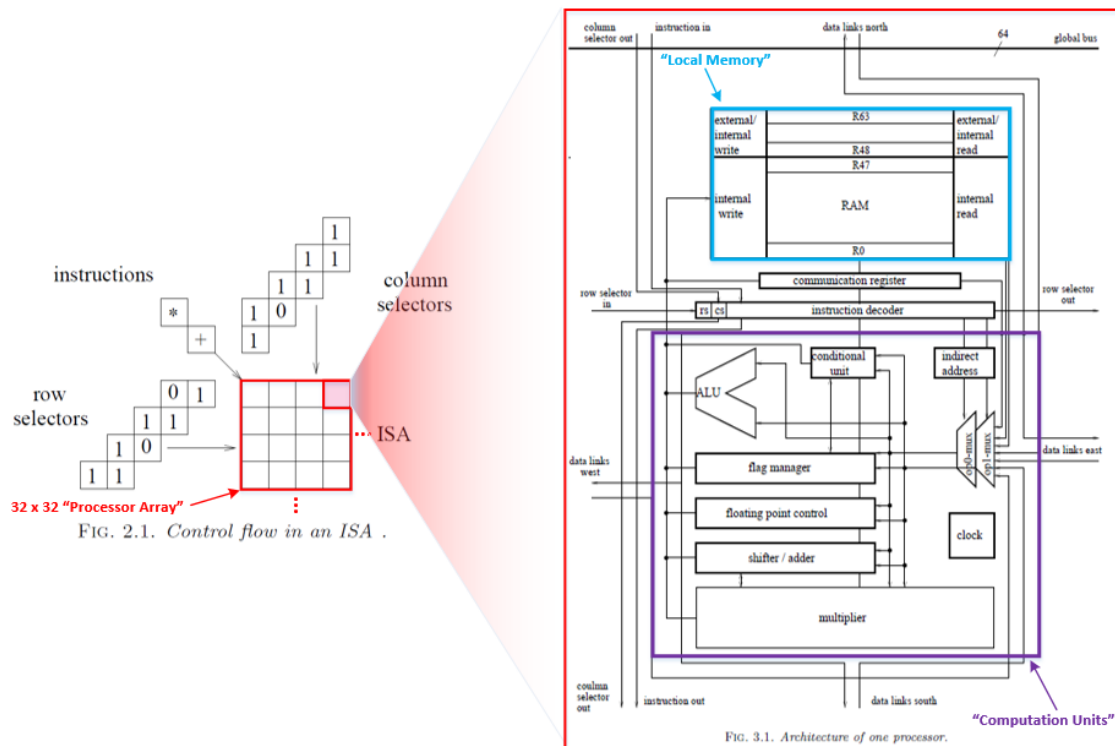
55. I have been asked to provide my opinion concerning whether claims 1-5, 7-14 and 16-22 and 24 of the '616 patent are anticipated or would have been obvious to a POSA in light of the prior-art references identified in the Petition. For the reasons explained below, it is my opinion that each of claims 1-5, 7-14 and 16-22 and 24 would have been obvious to a POSA.

## **VIII. GROUND 1A: CLAIMS 1, 4-5 ARE OBVIOUS OVER SCHMIDT-2000**

### **A. Schmidt-2000 (EX1007)**

56. Schmidt-2000 discloses “a parallel computer with 1024 floating-point processors on a single chip,” called the “KPROC-chip” (for KiloPROCessor). Schmidt-2000, 163. The KPROC-chip is utilized by a “host computer” as a “coprocessor” to speed up computationally intensive tasks. Schmidt-2000, 163, 168-175. The KPROC-chip includes an instruction systolic array (ISA) arranging the 1024 processors in a 32x32 “array of identical processors, each connected to its

four direct neighbors,” a portion of which is illustrated in Fig. 2.1 (annotated below left). Schmidt-2000, 163-165, 178. See Appendix, §II.A.1 discussing my opinions on the public accessibility of EX1007.



57. Fig. 3.1 (annotated above right) shows that each processor in the array has 64 general-purpose registers of “local memory” (blue) implemented as random access memory (RAM) that are independently addressable for read/write operations (R0-R47 by the processor and internal computing units and R48-R63 additionally by the host computer), and a communication register (red). Schmidt-2000, 163-164. Each processor further comprises “computing units” (in purple box above) including a 16-bit integer adder, a 16-bit integer multiplier, and a

floating-point unit that uses the integer multiplier for multiplying mantissas (up to 16 bits wide) and the integer adder for adding exponents (up to 16 bits wide) when multiplying floating-point operands. Schmidt-2000, 166-167.

58. Schmidt discloses a “parallel-serial design” in which each processor has a 16-bit architecture: 16-bit registers and computing units that perform computations on 16-bit operands. Schmidt, 163-164; 166-167. Higher bit-width computations are performed by partitioning operands into 16-bit words and performing operations 16 bits at a time—i.e., the computing units are each configured to receive 16-bit operands per instruction. The floating-point unit, which uses the 16-bit integer multiplier used to perform mantissa multiplies and the 16-bit adder used to perform exponent addition is configured to receive 16-bit operands and performs higher bit-width computations iteratively, 16-bits at a time. Schmidt-2000, 166-167.

### **1. Modification to 8-bit Architecture**

59. POSAs would have had motivation and reasonable expectation of success in implementing an 8-bit architecture for Schmidt-2000’s KPROC-array to provide a high-performance coprocessor optimized for image-processing applications. Schmidt-2000, 163-165.

60. As discussed above in the description of Schmidt-2000, the KPROC-chip used a 16-bit architecture in which each processor has 16-bit registers and

computing units that operate on 16-bit operands one bit per clock cycle. Schmidt-2000, 163-164. Operands of more than 16 bits are partitioned into multiple 16-bit operands such that operations are performed iteratively, 16 bits at a time. Schmidt-2000, 166. As also discussed above in the description of Schmidt-2000, the float-point unit of each processes uses its 16-bit integer multiplier to multiply the mantissas and its 16-bit integer adder to add the exponents and performs higher-bitwidth multiplication (i.e., more than 16-bits) are likewise performed iteratively, 16 bits at time, on partitioned 16-bit operands. Schmidt-2000, 166-167. In this way, Schmidt-2000's processors can perform floating-point multiplication of higher-precision numbers (e.g., 32-bit, 64-bit, etc.) by partitioning them into 16-bit operands and performing a sequence of 16-bit sub-operations. Schmidt-2000, 166-167.

61. Schmidt-2000 explains that the 16-bit architecture was chosen as a “compromise between the requirements of different application areas,” recognizing that the optimal bitwidth choice would be different for systems intended for different applications. As examples, Schmidt-2000 explains that an 8-bit architecture would be preferable for image processing and a 64-bit architecture for numeric applications. Schmidt-2000, 164-165 (“The wordlength...was chosen to 16 bits as a compromise between the requirements of different application areas like image processing (favourable 8 bits) and numeric (64 bits).”).

62. A POSA would have understood that because longer bitwidth operands can be multiplied via iteration, the selection of the processor architecture's native bitwidth—including the bitwidth of the processor's registers and computing units that determines the bitwidth of the inputs received by the multiplier after longer-bitwidth operands are partitioned—was merely a design choice to optimize the trade-off between computation speed and the chip area and power needed for each processor, for whichever applications the chip is designed to primarily perform.

63. POSAs would have understood that Schmidt-2000's 16-bit architecture is larger in size (e.g., chip area) than an 8-bit architecture. As described below in the section describing process scaling (§IX.A.2.b), POSAs understood that an 8-bit KPROC ISA would have had about a factor of 0.6 reduction in area over the 16-bit KPROC ISA disclosed in Schmidt-2000 (i.e., a 16-bit architecture would have been approximately 1.7 time larger in area) based on the 8-bit architecture implemented in Schmidt-1999 (EX1009). Additionally, with the "parallel-serial design" (Schmidt-2000, 166) of the computing units, Schmidt-2000's 16-bit architecture requires significantly more clock cycles and consumes more power when performing computations on operands with less than 16 bits than would an 8-bit architecture optimized for image processing. Specifically, Schmidt-2000's computing unit operate bit-serially, each instruction

taking 16 clock cycles (referred to as an instruction cycle) such that instruction performed on 8-bit data still take 16 clock cycles to perform, consuming the same amount of power for computations on 8-bit operands as for computations on 16-bit operands. Schmidt-2000, 163-164, 166. As described below in the section describing process scaling (§IX.A.2.b), POSAs understood that an 8-bit KPROC ISA would have consumed significantly less (up to a half) the power of the 16-bit KPROC ISA disclosed in Schmidt-2000 based on the 8-bit architecture implemented in Schmidt-1999. See Appendix, §II.A.2 for my opinion on the public accessibility of EX1009.

64. A POSA would have recognized the desirability of an 8-bit architecture for Schmidt-2000's processors in implementing a KPROC-chip optimized for image processing in which a substantial percentage of the operands are contemplated to have fewer than 16 bits (circumstances in which Schmidt-2000 explains 8-bits would be favorable) with the capability of performing higher-bitwidth operations via iterative computations on 8-bit operands, for example, a KPROC-chip optimized to perform the example computations that Schmidt-2000 teaches the disclosed ISA is particularly well-suited (matrix multiplication, convolution, FFT, motion estimation, histogram and filtered back-projection for tomographic image reconstruction, etc.). Schmidt-2000, 169-176.

65. In such circumstances, such as when optimizing the KPROC-chip for image processing, a POSA would have understood that the speed-up of the disclosed 16-bit architecture for computations performed on higher bit-width operands may not merit the significant increase in size and power consumption relative to an 8-bit architecture for such implementations intended to primarily perform applications where operations are skewed towards 8-bit operands (like image processing and many digital signal processing and multimedia applications), but that also may need higher-bitwidth computations as well but less frequently.

66. Reduced-bitwidth floating-point formats' suitability for a broad range of applications was known, as were benefits of reducing power and conserving chip area resulting from their use. EX1034, 278-279; EX1125, 172-174. As discussed above in §V.D above in connection with the challenged claims, the area reduction and reduced power consumption of reduced-precision floating-point formats were well known, and were suitable for a wide-range of image and digital signal processing applications, including multiple applications at 8-bits (and lower) such as floating-point digital cosine transform (DCT) operations frequently used in imaging processing. EX1034, 273-274, 277-280; see also EX1125, 172-174 (describing the use of reduce-precision floating-point formats for image processing). Thus, an 8-bit architecture would also reduce power consumption for floating-point operations in image processing while retaining the higher-bitwidth

floating-point capabilities where needed. See Appendix, §II.C.40 and II.C.43 for my opinions on the public accessibility of EX1125 and EX1034.

67. That a POSA would have understood Schmidt-2000's teachings, coupled with the POSA's background knowledge, to suggest implementing the KPROC-chip with an 8-bit architecture for an image-processing-optimized implementation is further corroborated by the fact that Schmidt-2000's authors chose an 8-bit architecture when implementing a video accelerator (an application involving computations that occasionally required 24-bit capability, but were predominantly 8-bit) using the same general ISA architecture described in Schmidt-2000 that performed higher bit-width operations via iteration, corroborating the POSA's knowledge that the choice of architecture bit-width is a matter of design choice for a given application or application area. EX1009 ("Schmidt-1999"), 953-956. See Appendix, §II.A.2 for my opinions on the public accessibility of EX1009.

68. Thus, POSAs would have been motivated to implement an 8-bit architecture for a Schmidt-2000 coprocessor optimized for image processing. The suitability of reduced bit-width floating-point formats for a broad range of applications was known, as were the benefits of reducing power and conserving chip area that resulted from their use. EX104, 273-274, 277-280.

69. This 8-bit KROC-chip would substantially reduce the size of each processor (allowing for integrating even higher numbers of processors on a single chip), reduce the power consumption of both integer and floating-point operations, and increase the performance for many image processing applications by halving the number of clock cycles it takes to perform computations on operands of 8-bits (or less), while retaining the ability to perform computations on higher bit-width operands via iteration as needed. POSAs would thus have been motivated to implement an 8-bit KROC-chip.

## **2. Implementing the 8-bit KPROC-chip**

70. A POSA seeking to implement an 8-bit KPROC-chip would have known how to do so and would have had a reasonable expectation of success. For example, an 8-bit architecture could be implemented using 8-bit general-purpose and communication registers (either physically or logically) in place of the 16-bit registers and reducing the native hardware for the computing units to 8-bit widths.

71. Because Schmidt-2000's processors perform operations using a parallel-serial design, the bit-serial connections between registers and computing units require little or no change and the control circuitry would be modified in known ways to execute 8-clock instruction cycles. As discussed above, Schmidt-2000's authors in fact chose an 8-bit architecture for a video accelerator and demonstrated this implementation by 1999. Schmidt-1999, 953-956.

## **B. Claim 1**

72. The obvious 8-bit implementation of Schmidt-2000's system I discussed above in §§VIII.A.1-VIII.A.2 meets all limitations of claim 1 as demonstrated limitation-by-limitation below.

### **1. [1PRE]: "A computing system, comprising:"**

73. Schmidt-2000 discloses "a parallel computer with 1024 floating-point processors on a single chip"—the "KPROC-chip"—that is utilized by a "host computer" as a "coprocessor" to speed up computationally intensive tasks. Schmidt-2000, 163. The host computer together with the 8-bit KPROC-chip (§§VIII.A.1-VIII.A.2) as a coprocessor meet the "*computing system*" recited in [1PRE].

### **2. [1A]: "a host computer;"**

74. Schmidt-2000's "host computer" that utilizes the 8-bit KPROC-chip as a "coprocessor" meets [1A]. Schmidt-2000, 163.

### **3. [1B]: "a computing chip comprising:"**

75. Schmidt-2000 discloses that the "KPROC is an ISA with 1024 processors *integrated on a single chip*" called a "KPROC-chip" to implement a "parallel *computer*" Schmidt-2000, 163 (The KPROC-chip "consists of 1024 of these processors *integrated on one die* using a 0.25-micron digital CMOS process."). The 8-bit KPROC-chip uses this same 1024-processor chip but with an 8-bit architecture and therefore meets the "*computing chip*" recited in [1B].

4. [1C] **“a processing element array comprising” “first” and “second” “edge processing element[s] positioned at a first edge of the processing element array” and “first” and “second” “interior processing element[s] positioned at [first and second] location[s] in the interior of the processing element array”**

76. Schmidt-2000 discloses a “processor array” (Schmidt-2000, 164) with 1024 processors arranged as a “32×32 ISA” with each processor connected to adjacent processors to form a “mesh connected processor grid.” Schmidt-2000, 163-164, 176 (Table 6.1 caption). The ’616 patent “call[s] each unit[] which pairs memory with arithmetic[] a Processing Element.” ’616 patent, 16:65-67, 8:7-11 (““processing elements’...should be understood more generally as any kind of execution unit”).

77. Each processor executes instructions using the computing units including an adder, multiplier and a floating-point unit that operate on operands store in 64 general-purpose registers and a communication register—i.e., each Schmidt-2000 processor is an execution unit that pairs memory with arithmetic. Schmidt-2000, 164-167. Thus, these processors are processing elements and the mesh-connected “processor array” disclosed in Schmidt-2000 meets the claimed “*processing element array*.”

78. In the “processor array” (Schmidt-2000, 164) disclosed in Schmidt-2000, each processor is connected to adjacent processors in a “mesh connected processor grid,” meeting the claimed “*processing element array*.” Schmidt-2000,

163-164, 176 (Table 6.1 caption). A portion of this “KPROC array” (Schmidt-2000, 169) is illustrated in Fig. 2.1, reproduced below with processors positioned at an edge of the array outlined in **red** and processors positioned in the array’s interior (i.e., not on an edge) outlined in **blue**.

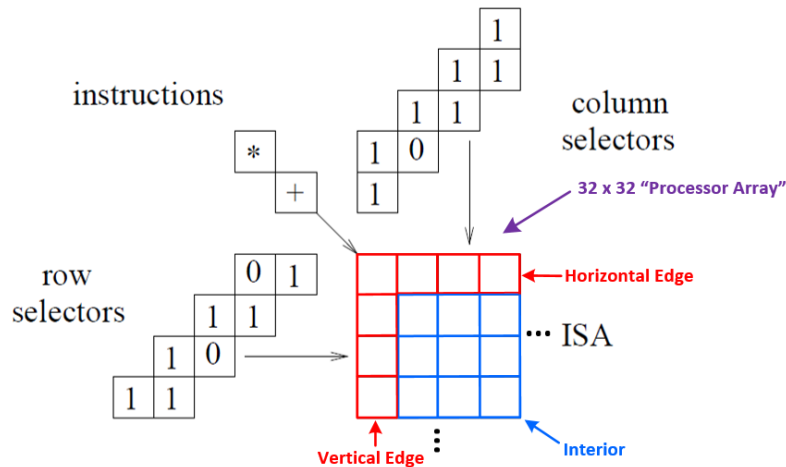


FIG. 2.1. Control flow in an ISA .

79. With the exception of the top-left corner processor (which is not connected to an interior processor), any of the processors in the first row and first column (or in the last row and last column not shown in the drawing unless it’s a corner processor) are “*edge processing elements*” positioned at an “*edge of the processing element array,*” as recited in [1C]. Annotated Fig. 2.1 of Schmidt-2000 below shows example first and second “*edge processing elements*” positioned at an example “*first edge*” (top row) are shaded **red** below, and example first and a second interior processing elements are shaded **blue**, showing that they are “*positioned at [first and second] location[s] in the interior of the processing element array*” as claimed.

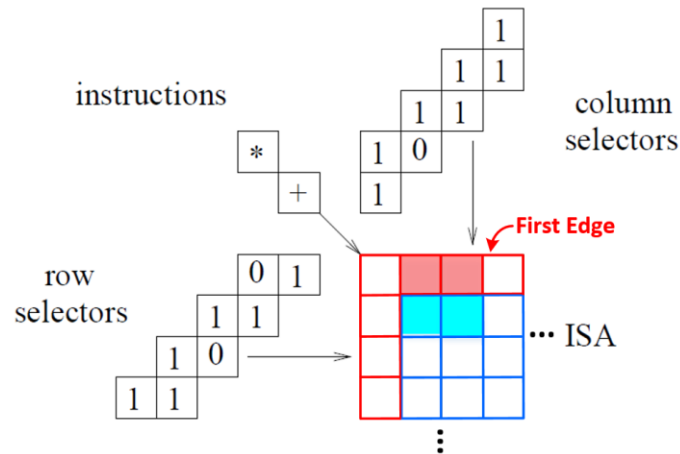


FIG. 2.1. Control flow in an ISA .

80. As discussed in §§VIII.A.1-VIII.A.2 above, the 8-bit KPROC-chip uses this same mesh-connected “processor array” and therefore the processor array with the above-labeled processors meets [1C].

5. **[1D]: “a first processing element connection connecting the first edge processing element with the first interior processing element; a second processing element connection connecting the second edge processing element with the second interior processing element”**

81. Schmidt-2000 discloses that the KPROC processor array is “a mesh connected processor grid” in which “[c]ommunication among adjacent processors occurs via designated communication registers.” Schmidt-2000, 163-164 (“Every processor has read write access to its own memory [and]...has a designated communication register that can also be read by the four neighbour processors.”).

82. Data exchange between adjacent processors via communication registers is performed bit-serially such that each processor is connected to each of its four neighbors with a pair of wires, one in each direction for reading the

respective adjacent register. Schmidt-2000, 163 (“each processor is connected to its four direct neighbours by two unidirectional data wires”), 164 (“Two adjacent processors can exchange data by writing on their own communication register and afterwards reading the communication register of the other in two subsequent clock phases.”).

83. The four pairs of wires connecting the communication register of each processor to its four adjacent neighbors are shown as north, south, east and west data links (highlighted in purple) in Fig. 3.1 (“Architecture of one processor”) reproduced below. As annotated in Fig. 2.1 and 3.1 of Schmidt-2000 below.

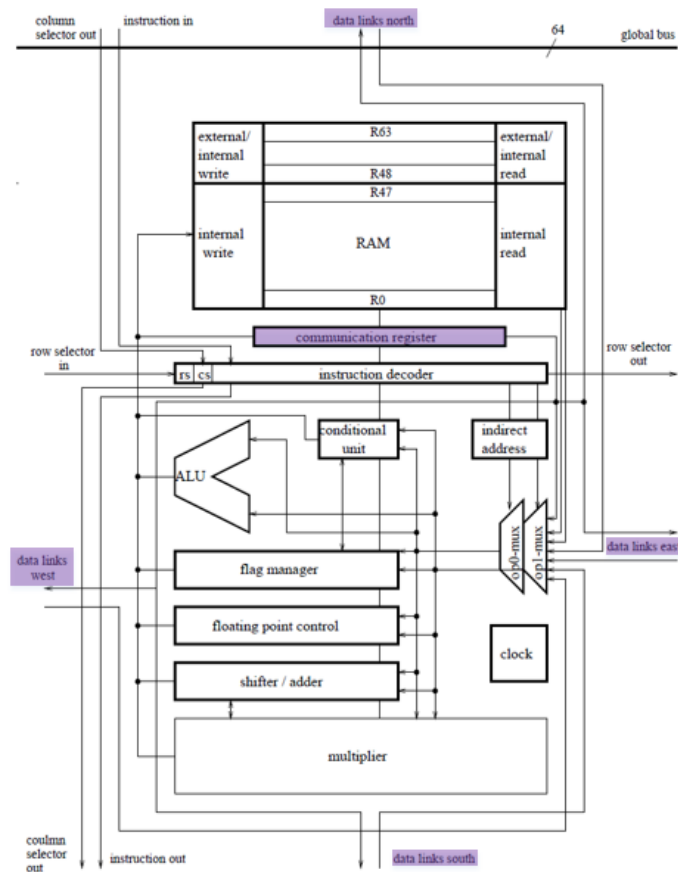
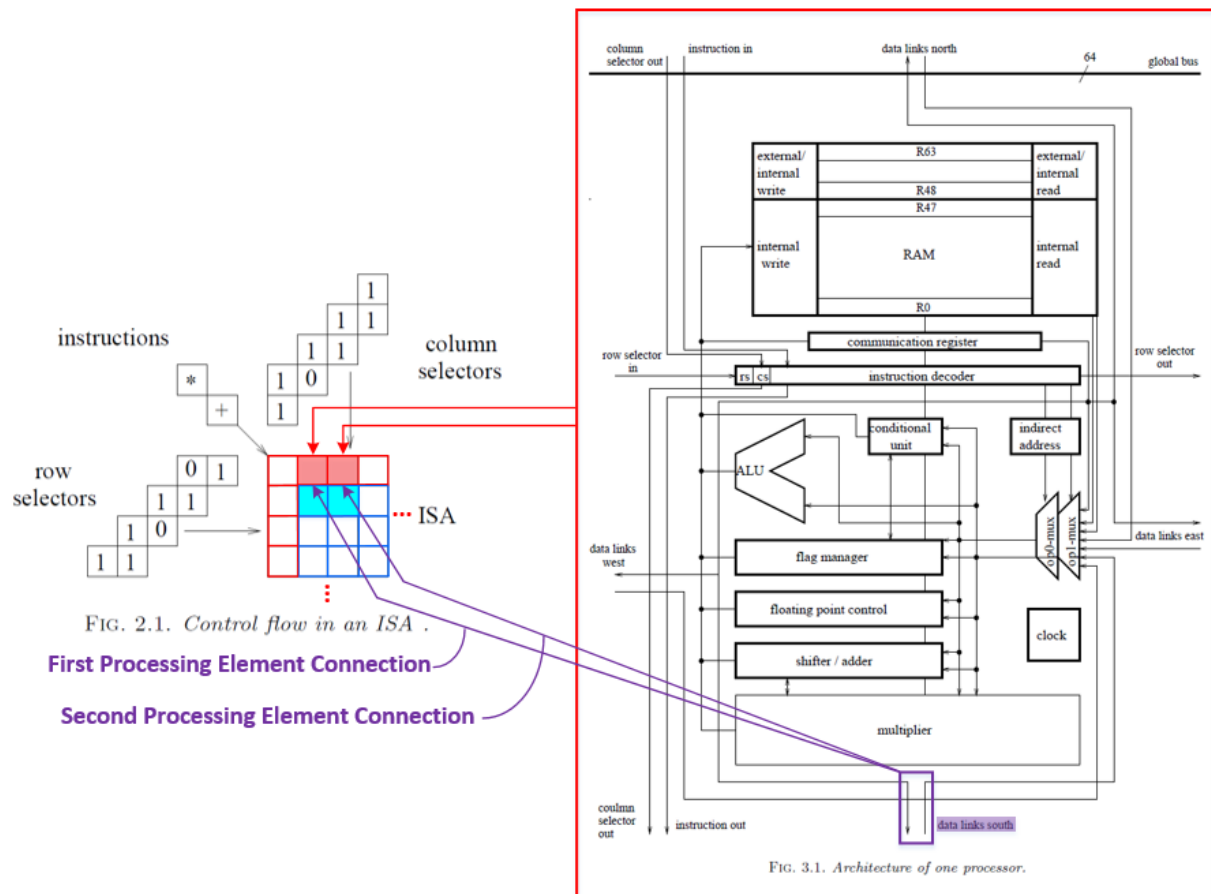


FIG. 3.1. Architecture of one processor.

84. The “data links south” provide the connections between the communication registers of the above-described example first edge processing element and the first interior processing element and the communication register of the second edge processing element and the second interior processing element as illustrated in annotated Fig. 3.1 of Schmidt-2000 below.



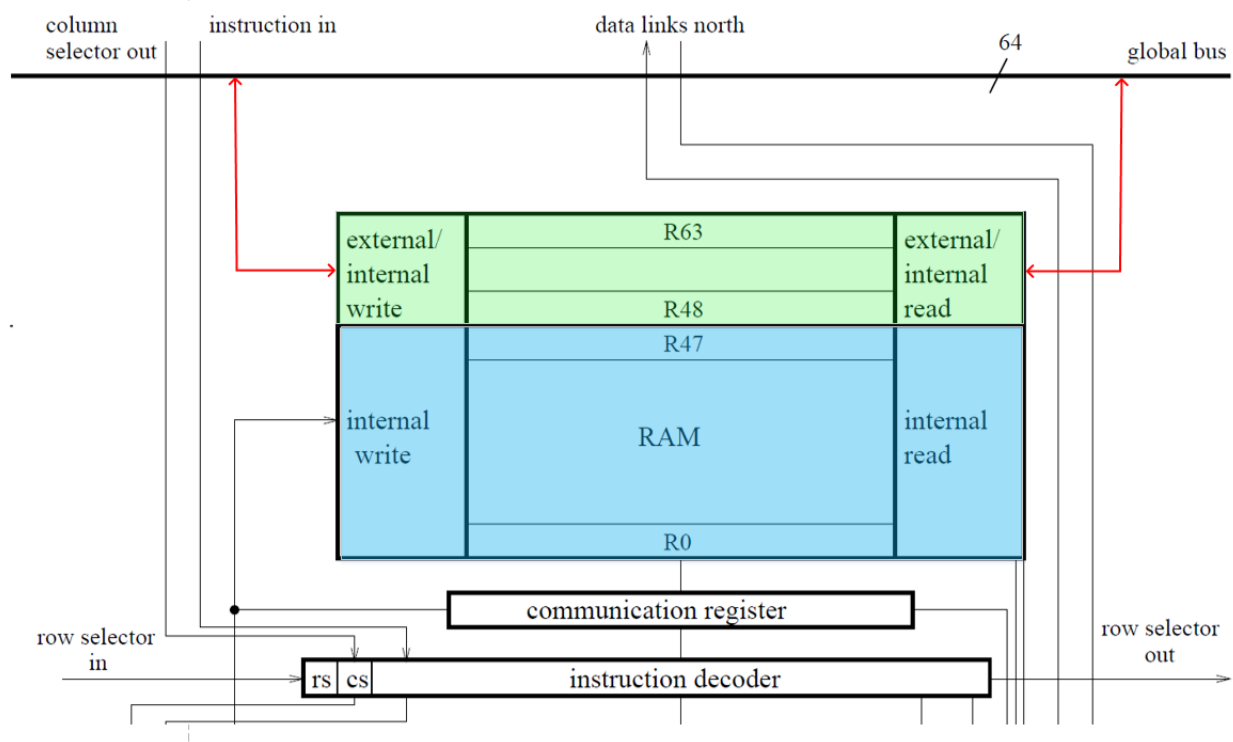
85. The 8-bit N-KPROC-chip implements 8-bit communication registers but does not modify the connection between the communication registers that connects each processor to its four direct neighbors. Thus, the data links south

(either individually or as pairs) meet the processing element connections recited [1D].

**6. [1E]: “an input-output unit connected to the first edge processing element and the second edge processing element;”**

86. Schmidt-2000 discloses that the “array allows off-chip communication with a data rate of 800 Mbytes per second between host computer and the KPROC-chip.” Schmidt-2000, 163. To implement this communication, Schmidt-2000 discloses that “every processor has two memory banks, from which one is connected to the outside, while the other serves as local storage,” the contents of which are “switched with a special instruction.” Schmidt-2000, 168. This arrangement “allow[s] random access data exchange with the external memory.” *Id.*

87. The two memory banks at each processor are shown in Figure 3.1 of Schmidt-2000 annotated below with **blue** and **green** shading for the respective “memory banks.” Specifically, each processor includes addressable “64 general-purpose registers” of “local memory” (Schmidt-2000, 164) labeled R0-R63 in Fig. 3.1. Forty-eight registers (R0-R47) have only “internal write” and “internal read” access with connections to the computation units of the processor and, sixteen registers (R48-R63 shaded in **green**) that include “external/internal write” and “external/internal read” access as labeled in Fig. 3.1.



88. POSAs understood that registers R48-R63 are “connected to the outside” for “data exchange with the external memory” (Schmidt-2000, 168) of the host computer by input-output connections that allow the “off-chip communication...between the host computer and the KPROC-chip” (Schmidt-2000, 163). Those input-output connections are not illustrated in Fig. 3.1, but POSAs understood that R48-R63’s “external” read/write is what “connect[s] to the outside” by connecting to the off-chip host computer’s “external memory” via the 64-bit “global data bus” illustrated in Fig. 3.1 above, as illustrated by the red arrows annotated above.

89. Schmidt-2000 offers no other structure that would allow “random access data exchange with external memory” or would connect registers R48-R63

“to the outside” as Schmidt-2000 discloses and POSAs understood the obvious way to implement the functionality described in Schmidt-2000 would have been to couple R47-R63 to the global data bus. For example, Schmidt-2000 discloses that “random access data exchange with the external memory is possible, because KPROC has not interface processors at all,” but instead implemented the above-described “two-memory banks” I/O architecture where one of the memory banks (register R48-R63) are “connected to the outside.” Schmidt, 168.

90. The “interface processors” that Schmidt-2000 removes in the KPROC architecture to allow for random access data exchange with the host computer’s external memory are described in Schimmler-1996 (EX1011), which is bibliography reference [14] in Schmidt-2000 (and shares a co-author). Schimmler-1996 implemented a 1024-processor ISA on an “add-on board” containing “a 4 x 4 array of processor chips. Each chip contains 64 Processors, arranged as an 8 x 8 square. This provides 1024 processors on the board.” Schimmler-1996, 138. One of the chips is illustrated in Fig. 2 of Schimmler-1996 (page 138) reproduced below. See Appendix, §II.A.4 for my opinions on the public accessibility of EX1011.

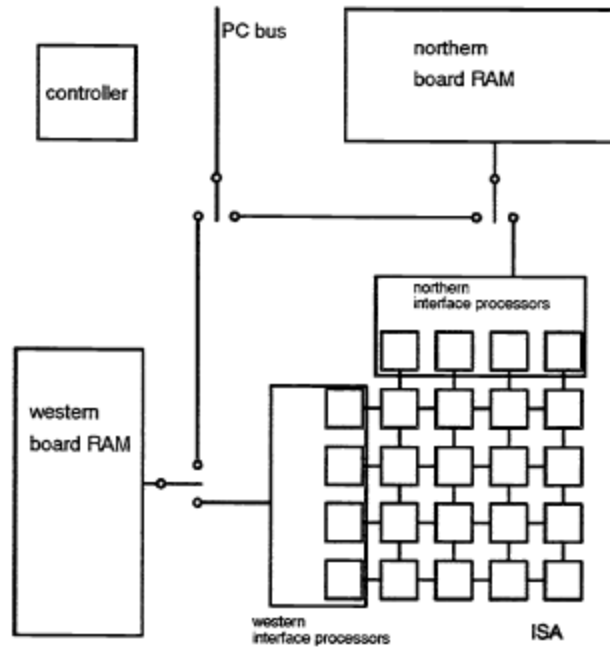


Fig. 2: Data paths in the parallel computer

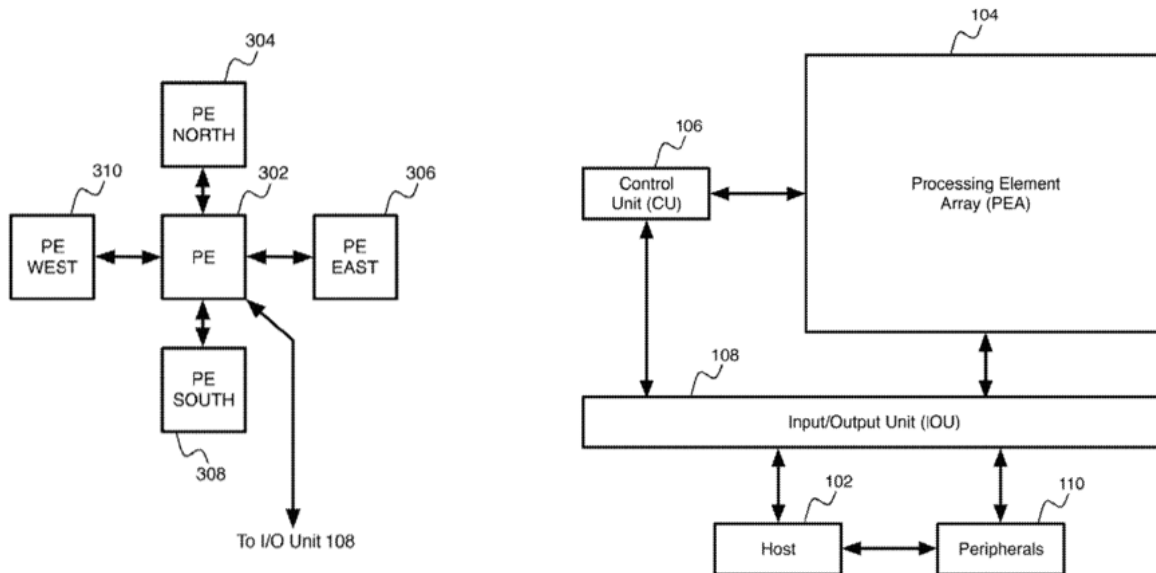
91. Schimmler-1996 implemented I/O with the off-chip PC (i.e., the host computer) using “interface processors,” which are “intelligent memory units” connected to processors on edges of the ISA “by a single wire for data transfer in each direction.” Schimmler-1996, 138. These interface processors exchanged data between the ISA and the off-chip PC via the PC bus as shown in Fig. 2 above. Schimmler-1996, 139. Since the interface processors are connected only to corresponding edge processors such that data for interior processing elements are routed processor-by-processor through the ISA, random access data exchange with the external memory is not possible.

92. As discussed above, Schmidt-2000 eliminated these interface processors in favor of externally connected registers R47-63 to allow for random

access data exchange between the host computer and each processor in the KPROC array. The obvious implementation of coupling registers R47-R63 to the “global bus” in Fig. 3.1 of Schmidt for off-chip data exchange is corroborated by the use of the PC bus to exchange data with the off-chip PC via using an on-chip RAM as an I/O buffer that Schmidt-2000 also removed in favor of using R47-R63 for this purpose, which was a known and conventional way of implementing I/O between on-chip and off-chip component. Schimmler-1996, 139.

93. Thus, registers R48-R63 of each processor and the global data bus implement “off-chip communication [] between the host computer and the KPROC-chip” (Schmidt-2000, 163) and is therefore (each individually or both together) meet “*an input-output unit*” as claimed. Each set of registers R48-R63 can also be internally read/written via “switching” the content with internal registers R0-R47, and therefore the input-output unit is “*connected to the first edge processing element and the second edge processing element,*” via their respective registers R48-R63.

94. The '616 patent illustrates a similar configuration in Fig. 3 (below left) where the PE “includes a data connection to the IOU 108.” EX1001, 9:57-58.



95. Furthermore, the '616 patent does not describe what the I/O unit comprises (or even that it is on-chip), but rather illustrates the I/O unit as a box in the block diagram of Figure 1 (above right) and discloses that “to get data into and out of the CU 106 and PEA 104, the I/O unit 108 may interface the CU 106 and PEA 104 with the Host 102” and that “I/O could be routed through the CU 106” (which the '616 patent discloses is optional) or “through a separate I/O unit 108.” EX1001, 9:7-9, 20-30. Schmidt-2000’s above-described input-output unit interfaces with the KPROC array and the host computer to get data into and out of the KPROC array and meets [1E] for at least the same reasons the '616 patent’s I/O unit 108 would.

96. The 8-bit KPROC-chip does not alter how the KPROC-chips performs I/O and therefore meets [1E] whether implemented with or without an on-chip cache as discussed below in §XI.B (Schmidt combination).

7. [1F]: Each Processing Element of Limitation [1C] Has a “memory local to” It

97. Schmidt-2000 discloses that “[e]very processor has read and write *access to its own memory.*” Schmidt-2000, 164. Each processor’s “local memory” was limited to 64 general-purpose registers plus one communication register.” *Id.* The sixty-four addressable registers of local memory are shaded in blue in Fig. 3.1 below.

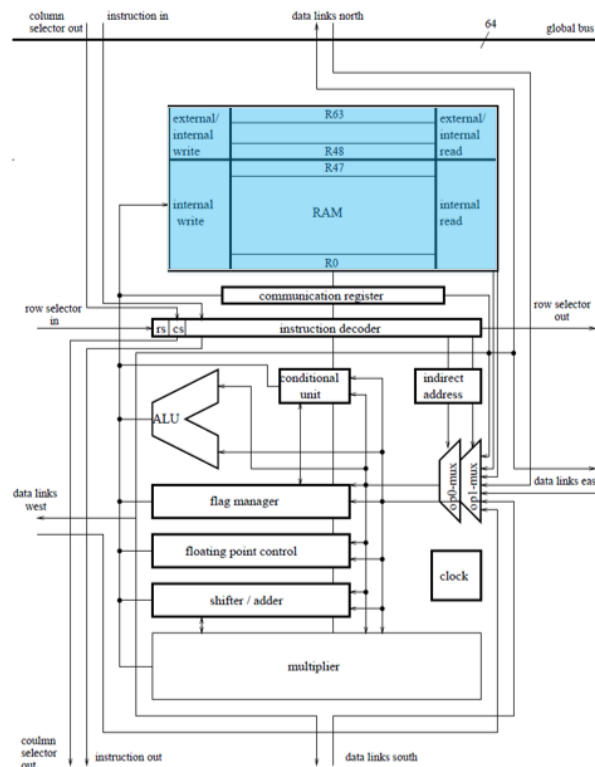


FIG. 3.1. Architecture of one processor.

98. As discussed for [1E] above, the 64 registers include registers R0-R47 with internal read/write access and R48-R3 with internal/external access, both “memory banks” of which are local to the respective processor and therefor meet [1F]. Registers R0-R47 themselves also meet [1F]. The 8-bit KPROC-chip uses

this same memory structure, but with 8-bit registers. Therefore, each processor's "own" set of 64 "local" general-purpose registers or internal registers R0-47 of the 8-bit KPROC-chip meets [1F] for the same reason.

## 8. [1G]: Each Processing Element of Limitation [1C] Comprises an "arithmetic unit"

99. Schmidt-2000 discloses that each processor in the KPROC processor array includes a number of "computation units" that perform the arithmetic operations for the processor. Schmidt-2000, 166-167. These computation units are illustrated within the purple box shaded yellow in annotated in Fig. 3.1 reproduced below.

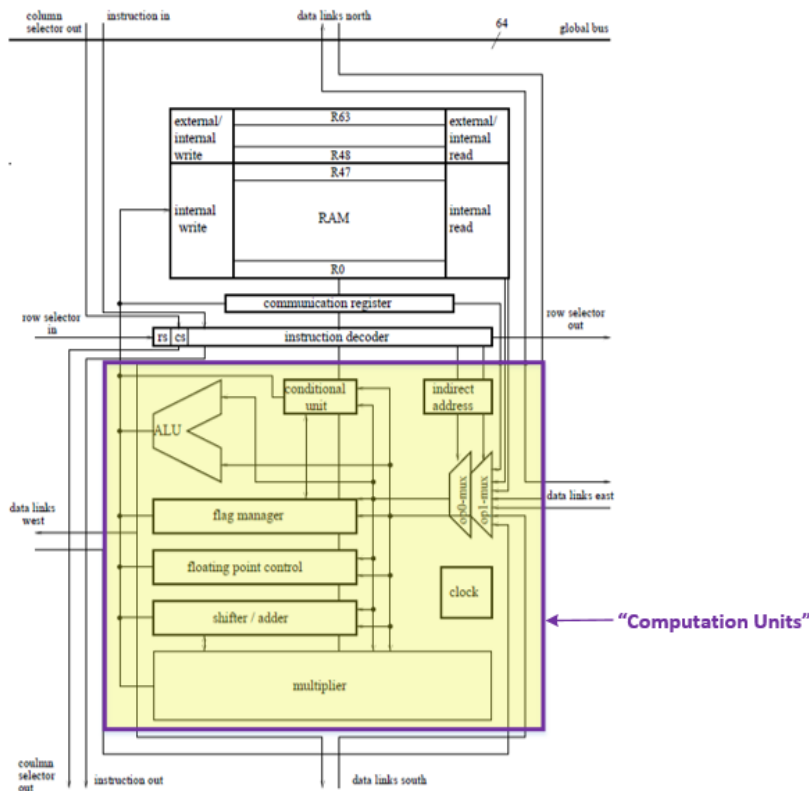


FIG. 3.1. Architecture of one processor.

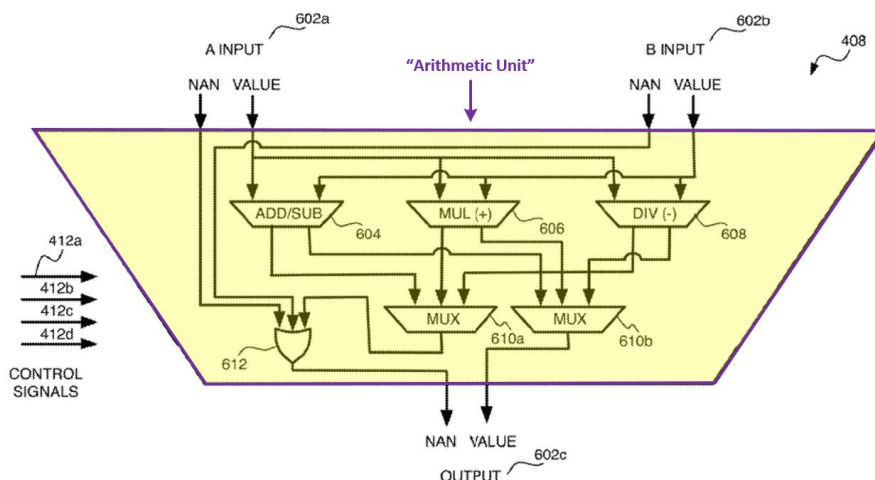
100. The computation units disclosed in Schmidt-2000 include “a unit for integer arithmetic and logical operations” consisting of “a full adder with feedback of the carry output to one of the inputs and a collection of logic gates for implementing AND, OR, NAND, NOR, XOR, EQV and arithmetical and logical shift operations,” which Schmidt-2000 refers to as a “standard ALU.” Schmidt-2000, 166.

101. Each processor’s computation units also include an integer multiplier and a “floating-point unit” (Schmidt-2000, 167) that utilizes the integer multiplier and the integer adder in conjunction with the “floating point control” and “shift/adder” to perform floating point operations. Schmidt-2000, 164-167.

102. A POSA would have understood that the collection of computation units that perform integer and floating-point operations is an “*arithmetic unit*” recited in [1G] for each of the processing elements recited in [1C], which is consistent with the specification of the ’616 patent that likewise describes the arithmetic unit as including multiple different computing units. EX1001, 12:54-13-5, FIG. 6.

103. As illustrated in Figure 6 of the ’616 patent annotated below, “arithmetic unit 408” boxed purple and shaded yellow includes adder/subtractor (“ADD/SUB”), a multiplier (“MUL”), a divider (“DIV”), logic circuits and multiplexer (’616 patent, 12:54-13:5, FIG. 6 (annotated below)), like the above-

described arithmetic unit of Schmidt-2000 comprises multiple computing units including “full adder” (as part of the ALU), a “multiplier” and a “floating point unit” that utilizes both. Schmidt-2000, 166-167.



104. As shown by the “architecture of one processor” illustrated in Fig. 3.1 of Schmidt-2000 above, the arithmetic unit (i.e., the collection of “computation units”) is part of and within the corresponding processor. Each processor of the 8-bit KPROC-chip includes this same set of computation units but with an 8-bit architecture (see §§VIII.A.1-VIII.A.2) and therefore each of the processing elements recited in [1C] comprises a respective “*arithmetic unit*,” as recited in [1G].

**9. [1H]: “a host connection at least partially connecting the input-output unit with the host computer;”**

105. In Schmidt-2000, “off-chip communication” (Schmidt-2000, 163) with the host computer occurs via the I/O pins of the KPROC-chip, which POSAs understood provides the “*host connection*” to the KPROC-chip—i.e., the host

computer connects to the KPROC-chip's I/O pins which are the chips connection to the "outside." Schmidt-2000, 163 (describing the bandwidth of "off-chip communication...between the host computer and the KPROC-chip"), 168 , 176 (describing that the "I/O bandwidth" is limited by the "pin limitation" of the chip).

106. The '616 patent does not use the term "host connection" and describes only that "the I/O unit may interface...with the Host 102." '616 patent, 9:7-9. Thus, the I/O pins that allow "off-chip communication...between the host computer and the KPROC-chip" provides a means for the host computer to interface with the KPROC-chip. As discussed in §VIII.B.6 above ([1E]), registers R48-63 "connected to the outside" provide external read/write access and are at least part of the claimed "*input-output unit*." The I/O pins provide the interface between the host computer and the input-output unit and are connected to both to allow off-chip data exchange. Schmidt-2000, 163, 168, 176. The I/O pins therefore "*connect[] the input-output unit with the host computer,*" as recited in [1H].

10. [1I] “wherein the first, second, third and fourth arithmetic units each comprises a corresponding multiplier circuit adapted to receive as a first input to the corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits”

107. As discussed in §VIII.B.8 ([1G]) above, each processor includes a number of “computation units” illustrated within the purple box (shaded yellow) annotated in Fig. 3.1 below that meet the claimed “*arithmetic units*,” including a “floating-point unit” that utilizes the integer adder for adding exponents and the integer multiplier for multiplying mantissas for floating point multiplication. Schmidt-2000, 166-167. That is, the “floating-point unit” in Schmidt-2000 performs floating-point multiplication by using the integer adder to add the exponents and the integer multiplier to multiply the mantissas of two floating-point operands. Schmidt-2000, 166-167 (“Floating point multiplication is performed in the usual way: Exponents are added and mantissas are multiplied using the integer units discussed above.”)

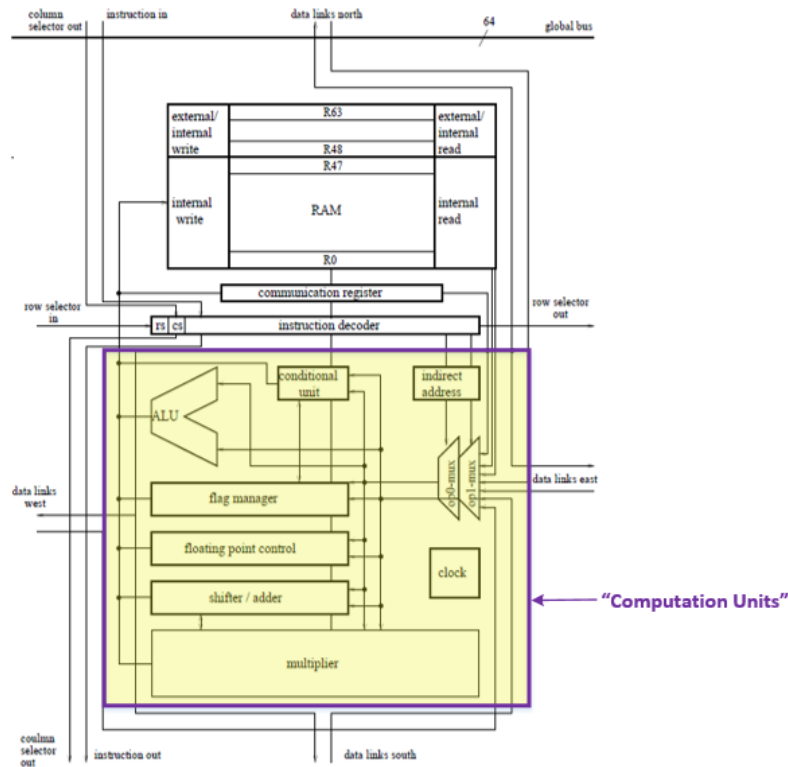


FIG. 3.1. Architecture of one processor.

108. Thus, a POSA would have understood that the “*multiplier circuit*” adapted to receive a first and second “*floating point value*” in the Schmidt-2000 processor would include the integer adder and the integer multiplier, as well as the “floating point control” and “shift/add” units that are used to perform floating-point multiplication.

109. Schmidt-2000’s processors have a 16-bit architecture and when not modified to an 8-bit architecture have a 16-bit architecture with 16-bit registers providing 16-bit operands to computing units that operate on 16-bit operands on each instruction cycle. Schmidt-2000, 163-164, 166. To perform computations on operands of more than 16-bits, the operands are partitioned into multiple 16-bit

words for storage in the 16-bit registers, and the computing units receive and each operate on 16-bit operands at a time.

110. As discussed above, the processor multiplies two floating-point numbers by adding their exponents in the 16-bit adder and multiplying their mantissas in the 16-bit multiplier. If the mantissas have more than 16 bits, the processor multiplies them by first loading 16 bits of each mantissa into the multiplier, multiplying those 16-bit mantissas, and then subsequently loading the remaining mantissa bits to perform “the same procedure...more than one times,...add[ing] the intermediate results” to arrive at the full product. Schmidt-2000, 166 (description of “Multiplier”). In the 16-bit architecture, the multiplier circuit in each processor is thus adapted to receive as first and second inputs two floating-point values, each having an exponent of up to 16 bits (added by the 16-bit adder) and a mantissa of up to 16 bits (the first mantissa partition multiplied by the 16-bit multiplier) and subsequently the multiplier circuit can receive further mantissa bits as inputs for multiplication.

111. Schmidt-2000 discloses performing single-precision and double-precision floating-point operations, which include 8-bit and 11-bit exponents, respectively. Schmidt, 167. Thus, the floating-point unit’s multiplier circuit is adapted to receive inputs with 8 or more exponent bits.

112. As discussed in §§VIII.A.1-VIII.A.2 above, the 8-bit KPROC-chip modifies the 16-bit architecture disclosed as a “compromise” and uses an 8-bit architecture and therefore has computing units configured to receive 8-bit operands and no more. Thus, in the 8-bit KPROC-chip, the floating-point multiplier circuit of each processing element’s arithmetic unit is adapted to receive as first and second inputs two floating-point values, each having an 8-bit exponent (added by the 8-bit adder) and a mantissa of up to 8 bits (the first mantissa partition multiplied by the 8-bit multiplier), meeting [1I].

113. As demonstrated in the foregoing, the 8-bit KPROC-Chip meets each limitation of claim 1 and therefore it is my opinion that claim 1 is unpatentable.

**C. Claim 4: “said host computer is programmed to provide instructions to said computing chip that, when executed, cause said processing element array to perform an operation whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.”**

114. POSAs would have readily understood that image pattern matching, such as image database search, is precisely the type of “computationally intensive task[]” in image processing that the KPROC array is ideally suited due to the highly parallelizable nature of the processing—i.e., large-scale repetitions of the same computations on different data, for example, as explained in Kravec (EX1077), 7:6-12 and Caid (EX1078), 3:15-24, 13:28-52.

115. For example, Kravec corroborates the POSA's knowledge that many pattern matching problems require an input pattern to be compared with numerous reference patterns (e.g., an input fingerprint to a library of fingerprints, an input image to a database of images) to find the closest match (1:55-60, 7:6-12) and that sequential matching of patterns (e.g., on a conventional CPU) cannot achieve the desired high performance for these computations (3:58-60).

116. POSAs knew that in image matching, the pattern to be matched is typically a characteristic or feature vector derived from salient features or characteristics patterns of the corresponding image (*see, e.g.*, Caid, 5:6-8:4; 4:33-56;13:1-15), and image matching was typically performed by computing a distance between two feature vectors, such as a dot-product (*see, e.g.*, Caid, Abstract, 2:19-21, 3:15-24, 4:33-56; 13:28-38), Euclidean distance (*see, e.g.*, Kravec, 10:35-53), Manhattan distance (*id.*), etc.

117. A POSA would have understood that such distance computations (i.e., repeated multiplication and addition operations) are of the type of computations that the KPROC array is specifically designed for. Both the matrix multiplication and the convolution operations described in Schmidt-2000 are composed of the same repeated multiplication and addition operations involved in computing the distance between an input pattern and massive numbers of reference patterns. Schmidt-2000, 169-170. Thus, a POSA seeking to accelerate image database

search and retrieval operations (e.g., as described in background art such as Kravec and Caid) would have implemented the distance computations in the same general manner described in Schmidt-2000 for matrix multiplication and convolution.

118. In particular, the KPROC processor's multiply and add capabilities allow the elements of the patterns (e.g., feature vectors) to be matched in a highly parallel manner using the KPROC systolic architecture. Schmidt-2000, 166. Specifically, by providing each of a set of KPROC processors with successive elements of an input pattern and a sequence pattern, a multiply-and-add instruction can be propagated through the array such that each processor performs a multiplication (e.g., for a dot-product) between the two elements stored in its local memory and adds the product to the accumulated sum of those products received via the communication register of the adjacent processor (e.g., to the west) such that the multiply and add operation performed by the last processor in the set computes the distance between the input and the reference vector—i.e., by adding the accumulated products of the preceding processors in the set. Numerous other implementations such as instructing each processor in the array to perform the sequence of instructions that compute the distance between a target and reference pattern could be programmed to compute thousands of distance computations in parallel. Furthermore, POSAs understood that the 8-bit KPROC array is well suited to find the smallest distance computation from those computed on the array.

119. This obvious use of the 8-bit KPROC-chip system to perform known image-matching applications on a parallel processor array (as corroborated in Caid and Kravec) on the Schmidt-2000's KPROC-array renders obvious claim 4. Specifically, the obvious implementation described above programs the host computer *“to provide instructions to said computing chip that, when executed, cause said processing element array to perform an operation”* (e.g., desired distance computations between query vector obtained from a query image and respective feature vectors of images stored in a database) *“whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image”* (e.g., the distance computation output by the processor array that determines the closest images in the database, determines the smallest distance value computed, etc.), as recited in claim 4.

**D. Claim 5: “the width of each [first/second] binary mantissa is no more than 10 bits plus a [first/second] sign bit.”**

120. As discussed in §VIII.B.10 ([11]) above, the floating-point multiplier circuit of each 8-bit processor of the 8-bit KPROC-chip is configured to receive first and second inputs having up to 8-bit mantissas (i.e., mantissas of less than 10 bits plus a sign bit). Specifically the width of each mantissa (i.e., 8-bits) is less than the width of 10-bits plus a sign bit (i.e., 10-bits plus 1-bit = 11 bits).

**IX. GROUND 1B: CLAIMS 7, 9 AND 14 ARE OBVIOUS IN VIEW OF SCHMIDT-2000 AND A POSA’S KNOWLEDGE OF SEMICONDUCTOR PROCESS ADVANCES**

121. Claim 7 recites substantially the same computing system recited in claim 1—*i.e.*, a host computer and a computing chip comprising a plurality of interconnected processing elements with reduced-bitwidth multipliers—but recites that there be “*no less than 5000*” ([7D]) processing elements on the computing chip. The ’616 patent describes no implementation of 5000 processors integrated on a single chip. The ’616 patent only references 5000 PEs once (’616 patent, 28:46-51), among a generalized, boilerplate description of “certain embodiments,” all but one of which have significantly fewer than 5000 PEs (*id.*, 28:13-51) and fewer than 1024 processors integrated on the KPROC-chip. Furthermore, the ’616 patent does not describe any number of PEs as being critical, nor does the ’616 patent disclose that qualitatively different functionality could be performed or that integrating 5000 PEs on a chip produce any new or unexpected results.

**A. Obviousness of Process Scaling the KPROC-Chip**

**1. Motivation**

122. Schmidt-2000 disclosed that the KPROC was the “first implementation of a parallel computer with 1024 floating-point processors on a single chip.” Schmidt-2000, 163 (Abstract). Schmidt-2000 discloses “building large arrays of many KPROC chips or speeding up small machines with a single KPROC as a coprocessor,” thus recognizing the performance benefit of using

larger numbers of processors to accelerate computationally intensive tasks beyond what could be integrated on a single chip in 2000. Schmidt-2000, 163 (Abstract).

123. Thus, Schmidt-2000 reflects the POSA's understanding of the computational performance benefit of using very large number of processors, and POSAs would have been motivated to increase the number of processors integrated on a single chip as advances in semiconductor technology permitted increasing levels of integration. In fact, Schmidt-2000 cites Schimmler-1996 (EX1011), authored by Schmidt-2000's co-author Schimmler, where a 1024-processor array was obtained by assembling sixteen 64-processor chips on a circuit board. Schimmler-1996, 136-139; see also EX1010 ("Schimmler-1994"), 487 (also describing an add-on board implementation where "[t]here are 16 ISA chips on the board, each comprising 64 processors."). See Appendix, §II.A.3 for my opinion on the public accessibility of EX1010.

124. POSAs would have been similarly motivated to integrate multiple KPROC arrays on a single chip (an "N-KPROC-chip") as later advances in semiconductor processing allowed higher levels of within-chip integration. For example, integrating a 3x3 or a 4x4 tiling of KPROC arrays on single chip—i.e., a 9-KPROC-chip (including  $9 \times 1024 = 9,216$  processors) or a 16-KPROC-chip (including  $16 \times 1024 = 16,384$  processors)—are two examples of obvious and desirable implementations to "build[] large arrays" (Schmidt-2000, 163) on a

single chip in which a POSA would have had a reasonable expectation of success using semiconductor processes available before June 2009. Scaling the 32x32 KPROC array up to a 72x72 array—i.e., a 5-KPROC-chip (including 5184 processors)--is another example of an obvious and desirable implementation.

## **2. Reasonable Expectation of Success**

125. A POSA would have had a reasonable expectation of success of implementing an N-KPROC-chip using semiconductor processes available in the 2009-2010 timeframe. In particular, Schmidt-2000 disclosed integrating 1024 floating-point processors on a 1.2-cm<sup>2</sup> (120-mm<sup>2</sup>) chip using a 250-nm CMOS process nearly a decade earlier. Schmidt-2000, 163-164.

### **a. Moore's Law**

126. It was well-known that advances in semiconductor process technology allowed for increasing levels of single-chip integration that kept pace with (and often exceeded) the prediction known as “Moore’s Law” that the integration capacity of a single chip doubles approximately every two years based on predictions from Gordon Moore. *See e.g.*, EX1026 (“ITRS-2007”), 1, 86. Moore’s original prediction in 1965 was that single-chip integration capacity would double *annually*. EX1016, 83-84 (original Gordon Moore prediction). *See* Appendix, §§II.B.7 and II.C.4 for my opinion on the public accessibility of EX1026 and EX1016, respectively.

127. At the 1975 IEEE International Electron Devices Meeting (IEDM), Moore revised his forecast rate, predicting semiconductor complexity would continue to double annually until about 1980, after which it would decrease to a rate of doubling approximately every *two years* (and sometimes formulated as every 18 months)—becoming “Moore’s Law” that has since been the guiding principle of semiconductor advancement. Ex. 1017, 36-37, Figure 5. The ‘616 patent also acknowledges that Moore’s Law “has proved valid for over thirty years and looks likely to continue in some form.” , 1:28-30, 6:30-32. See Appendix, §II.C.5 for my opinion on the public accessibility of EX1017.

128. By application of the well-corroborated Moore’s Law starting from Schmidt-2000’s disclosure in 2000, POSAs would have understood the increase in the number Schmidt-processors implementable on a single chip (of the same size as Schmidt-2000 disclosed) to have been on the order of thirty-two (i.e.,  $32 \times 1024 = 32,768$  processors) by 2009, and would have understood that 8192 Schmidt-processors (well over 5000) was achievable at least by 2006, simply based on the time elapsed following Schmidt-2000’s disclosure date in 2000.

129. Moreover, the 250-nm process used by Schmidt-2000 was a legacy process node even by 2000. EX1022 (“ITRS-1999”), 1 (“Note that products built with the 180-nm node are shipping in 1999, fulfilling the forecast of a 2-year technology-node cycle from the 250-nm node in 1997”); EX1030 (“ITRS-2001”),

31 (“250 nm node in 1997, 180 nm node in 1999”); EX1018, 1 (reporting on the release of Intel’s Celeron processor). Thus, POSAs would have understood that the 1024-processor KPROC-chip disclose in Schmidt-2000 would have been achievable in the 1997-1998 timeframe when the 250-nm process node was available and commercialized. See Appendix, §§II.B.2, II.B.4 and II.C.6 for my opinion on the public accessibility of EX1022, EX1030 and EX1018, respectively.

130. Applying Moore’s Law to the 250-nm process technology used by Schmidt-2000, POSAs would have understood that up to a factor-of-sixty-four increase in the number of Schmidt-processors (i.e., 65,536 processors) was achievable by 2009, and that a factor-of-eight increase (i.e., 8192 processors) was achievable at least by 2004. Moore’s Law is corroborated by actual transistor-density increases achieved by commercial products fabricated at successively smaller process nodes available in the years up to June 2009, discussed below.

#### **b. Process Node Scaling**

131. Moore’s Law has accurately predicted semiconductor process technology advancement over decades in part thanks to the ITRS, a well-known collaboration of leading companies and research institutions that established performance targets for the semiconductor industry with the stated goal of keeping pace with Moore’s Law. EX1027 (“ITRS-2009”), 3 (“As indicated in the overview, the Roadmap has been put together in the spirit of defining what

technical capabilities the industry needs to develop in order to stay on Moore's Law and the other trends, and when. So the ITRS is not so much a forecasting exercise as a way to indicate where research should focus to continue Moore's law."); EX1026, 1-3, 87; 1022, 1-2; EX1021, 1 ("The Roadmap continues to call for reduction in geometric dimensions in accordance with Moore's Law"), 9 ("With the relentless decrease in feature size required for the productivity increases necessary to follow Moore's Law"). See Appendix, §§II.B.8 and II.B.1 for my opinions on the public accessibility of EX1027 and EX1021, respectively.

132. These performance targets defined metrics called "process nodes" that the semiconductor industry designed in developing next-generation products, meeting (and often exceeding) those targets. EX1022, 1. A process node historically referred to the minimum DRAM feature size (minimum metal half-pitch) and specified in nanometers. See *e.g.*, EX1022, 2. It was recognized as early as 1999 that the direct connection to that metric became of diminishing value, but the nomenclature was (and still is) retained to describe a set of technology metrics including a number of feature sizes (*e.g.*, minimum feature size, interconnect half-pitch size, and transistor logic size), power requirements, clock speeds, etc., needed to keep pace with Moore's Law that the ITRS continued to target.

133. The National Technology Roadmap for Semiconductors (NTRS) was created by the U.S. Semiconductor Industry to provide the semiconductor industry

with a common vision of the future technology needs and published its first performance targets in 1991 and released its final NTRS report in 1997 (EX1021 (“NTRS 1997 Edition”) before being joined by an international group of semiconductor experts and leading industry organizations to become the International Technology Roadmap for Semiconductors (ITRS) that published its own reports on odd years, and updates on even years from 1998 to 2013. See e.g., EX1022-1028.

134. The ITRS established process node forecasts that were used extensively by semiconductor companies as a set of targets that needed to be achieved ahead of schedule to maintain industry leadership. ITRS-1999, 1. As a result, the industry often exceeded ITRS forecasts so that ITRS reports also included updates reflecting the actual state of the industry and the corresponding process node. The ITRS reports provided both prospective and retrospective dates for the leading-edge (“at introduction”) and high-volume (“at production”) dates for products at corresponding process node. See *e.g.*, ITRS-1999, 2.

135. From the 250-nm process used by Schmidt-2000, semiconductor processing technology advanced through numerous successively smaller process nodes (180-nm, 130-nm, 90-nm, 65-nm, 45-nm, 40-nm, 32 nm nodes) that POSAs knew were available in 2009. As shown below, POSAs would have understood that (at least) the 90-nm node (available and commercialized by 2004) and all

smaller nodes would have allowed more than 5000 Schmidt-2000 processors (i.e., a factor-of-five increase) to be integrated on the KPROC-chip without even changing the chip's size.

136. POSAs understood that commercially demonstrated process nodes would have allowed more than 50 times as many Schmidt-2000 processors to be integrated on the same size chip (e.g., using a 40-nm process node) according to the transistor-density (i.e., the number of transistors integrated on a chip divided by the area of the chip) increases achieved by commercial products released before June 2009.

137. **250-nm:** Intel's Celeron processor ("Mendocino"), released in 1998, integrated 19 million transistors on a 154-mm<sup>2</sup> die using a 250-nm process—a transistor density of 123,377 transistors/mm<sup>2</sup>. EX1018, 3, Fig. 3. See Appendix, §II.C.6 for my opinion on the public accessibility of EX1018.

138. **90-nm:** Intel's 90-nm Pentium 4 processor ("Prescott"), released in 2004, integrated 112 million transistors on a 112-mm<sup>2</sup> die—a transistor density of 1.1 million transistors/mm<sup>2</sup>—demonstrating a transistor-density increase by a factor of 9.4 or, rounding to the nearest integer, a factor-of-9 increase in transistor density over 250-nm Mendocino. EX1040, 1, Table 1. See Appendix, §II.C.11 for my opinion on the public accessibility of EX1040.

139. **65-nm:** The 65-nm process node was available in 2005 with commercial products released in 2006. EX1039, 1. Intel’s 65-nm Itanium processor integrated 2.05 billion transistors on a 698.75 mm<sup>2</sup> die—a transistor density of 2.93 million transistors/mm<sup>2</sup>—demonstrating a transistor-density increase by a factor of 23.7 or, rounding to the nearest integer, a factor-of-24 increase in transistor density over 250-nm Mendocino. EX1039, 18. See Appendix, §II.C.10 for my opinion on the public accessibility of EX1039.

140. **45-nm:** Intel’s first 45-nm Penryn product, released in 2007, integrated 410 million transistors on a 107-mm<sup>2</sup> die—a transistor density of 3.8 million transistors/mm<sup>2</sup>—demonstrating a transistor-density increase by a factor of 31.1 or, rounding to the nearest integer, a factor-of-31 increase in transistor density over the 250-nm Mendocino processor. EX1042, 1. See Appendix, §II.C.13 for my opinion on the public accessibility of EX1042.

141. **40-nm:** TSMC, a leading (and largest) semiconductor foundry, departed from the standard ITRS node progression after 65-nm and developed a 40-nm process that it announced at volume production in 2008. EX1043, 1-2; EX1137, 1-2; *see also* EX1038, 3 (noting Altera’s commercial “40-nm devices” (e.g., “FPGAs and ASICs”) using TSMC’s 40-nm node were introduced at publication). AMD’s 40-nm Radeon HD 5870 integrated 2.15 billion transistors on a 334-mm<sup>2</sup> die—a transistor density of 6.44 million transistors/mm<sup>2</sup>—

demonstrating a transistor-density increase by a factor of 52.2 or, rounding down to the nearest integer, a factor-of-52 increase in transistor density over the 250-nm Mendocino processor. EX1041, 1-2. See Appendix, §§II.C.14, II.C.9, II.C.42 and II.C.12 for my opinion on the public accessibility of EX1043, EX1038, EX1137 and EX1041, respectively.

142. A similar (but even larger) scale factor at 40-nm is demonstrated by the “2.35 times density improvement compared to devices built on 65nm process technology,” the latter of which was TSMC’s predecessor process node to 40-nm. *See e.g.*, EX1038, 3, 71; EX1043, 1-2; EX1137, 1-2. Using the factor of 2.35 factor density improvement over the 65-nm Itanium processor discussed above yields a transistor density of 6.88 transistors/mm<sup>2</sup> (i.e., a 2.35-factor increase over the Itanium processor’s transistor density of 2.93 million transistors/mm<sup>2</sup> from above), which is a factor-of-56 increase over 250-nm Mendocino, corroborating the factor of 52 increase using commercial product data and POSAs understanding that the 40-nm process node would have provided over a factor-of-50 increase in transistor density. EX1039, 18.

143. **32-nm:** By mid-2009, POSAs would have also been aware that they could have achieved even more transistors on a single chip using the 32-nm process node. EX1045 demonstrated a 32nm chip (an “SRAM test vehicle”) that achieved an SRAM “0.171μm<sup>2</sup> cell size.” EX1045, 1. EX1038 (at 71) noted that

TSMC's 40-nm process had an "SRAM cell size at  $0.242 \mu\text{m}^2$ ." Thus, the 32-nm node process disclosed in EX1045 would have allowed for an additional 1.4x scaling over TSMC's 40nm SRAM cell size ( $0.242 \mu\text{m}^2 / 0.171 \mu\text{m}^2$ ). EX1094 demonstrated a "32nm" process achieving "functional high-density SRAM with a cell size of  $0.157 \mu\text{m}^2$ . EX1094, 67. As noted above, TSMC's 40-nm process node had an "SRAM cell size at  $0.242 \mu\text{m}^2$ ." EX1038, 71. Thus, the 32-nm process node disclosed in EX1094 would have allowed for an additional 1.5x scaling over TSMC's 40-nm process node based on their respective SRAM cell sizes ( $0.242 \mu\text{m}^2 / 0.157 \mu\text{m}^2$ ). See Appendix, §§II.C.16 and II.C.20 for my opinion on the public accessibility of EX1045 and EX1094, respectively.

144. POSAs understood that the factor increases in transistor density between process nodes shown above provide an approximation of the factor increase in the number of Schmidt-2000 processors implementable on a single chip without increasing the chip size between those nodes. Table A-1 below shows these transistor-scale factors for the above-discussed process nodes that were available before June 2009, and the number of Schmidt-2000 processors on the KPROC-chip that would have resulted from each scaling factor.

| <b>Process Node</b> | <b>Transistor-Density<br/>Scale Factor</b> | <b>#Schmidt-2000<br/>Processors</b> |
|---------------------|--------------------------------------------|-------------------------------------|
| 250-nm              | 1                                          | 1024                                |
| 90-nm               | 9                                          | 9256                                |
| 65-nm               | 24                                         | 24,576                              |
| 45-nm               | 31                                         | 31,744                              |
| 40-nm               | 52                                         | 53,248                              |

**Table A-1**

145. Thus, POSAs would have understood from the transistor-density increases achieved by commercial products between the 250-nm process node at which the Schmidt-2000 KPROC-chip was implemented and the 40-nm process node available by 2009 that there would have been a reasonable expectation of success in implementing well over 5000 Schmidt-2000 processors on the KPROC-chip by the practice of ordinary skill in using process technology available in semiconductor foundries before 2009.

### **3. Implementing the 8-bit N-KPROC-chip**

146. A POSA seeking to implement an 8-bit N-KPROC-chip (e.g., 8-bit 9-KPROC-chip or 8-bit 16-KPROC-chip) would have known how to do so and would have had a reasonable expectation of success as it requires nothing more than making use of the well-known semiconductor process technology available in semiconductor foundries by 2009. POSAs would have known how to and would have had a reasonable expectation of success in scaling-up the design of the 8-bit

KPROC ISA discussed above to include a larger KPROC array (N-KPROC array) totaling well over 5000 processors.

147. Examples of obvious and desirable 8-bit N-KPROC-chip (i.e., multiple (N) 1-K processor-ISAs on a single chip as discussed above in the motivation section) implementations to increase computational performance include scaling-up the KPROC ISA to include a 72x72 (5-KPROC), a 96x96 (9-KPROC) or a 128x128 (16-KPROC) array. Based on the above-discussed scale factors, the Table A-2 below shows the chip area occupied by each of the 5-KPROC, 9-KPROC and 16-KPROC processor arrays at 65-nm, 45-nm and 40-nm nodes using the scale factors demonstrated by the commercial products above, as well as how each area compares with the 102.4-mm<sup>2</sup> area occupied by Schmidt-2000's original processor array in the year 2000, as a percentage (in parentheses) of the original Schmidt-2000 array area. Specifically, Schmidt-2000 discloses that with the pad frame and clock distribution on a 1.2-cm<sup>2</sup> chip, the area for one processor was limited to about .1-mm<sup>2</sup>—i.e., the 1024-processor KPROC array occupied an area of approximately 102.4-mm<sup>2</sup>. Schmidt-2000, 164.

| Process Node | Scale Factor | Per-Processor Area    | 5-KPROC Area<br>(72 x 72)<br>(% <u>KPROC</u> Chip) | 9-KPROC Area<br>(96 x 96)<br>(% <u>KPROC</u> Chip) | 16-KPROC Area<br>(128 x 128)<br>(% <u>KPROC</u> Chip) |
|--------------|--------------|-----------------------|----------------------------------------------------|----------------------------------------------------|-------------------------------------------------------|
| 250-nm       | 1            | .1 mm <sup>2</sup>    |                                                    |                                                    |                                                       |
| 65-nm        | 24           | .0042 mm <sup>2</sup> | 21.3 mm <sup>2</sup> (21%)                         | 38.4 mm <sup>2</sup> (38%)                         | 68.3 mm <sup>2</sup> (67%)                            |
| 45-nm        | 31           | .0032 mm <sup>2</sup> | 16.5 mm <sup>2</sup> (16%)                         | 29.7 mm <sup>2</sup> (29%)                         | 52.9 mm <sup>2</sup> (52%)                            |
| 40-nm        | 52           | .0019 mm <sup>2</sup> | 9.8 mm <sup>2</sup> (10%)                          | 17.7 mm <sup>2</sup> (17%)                         | 31.5 mm <sup>2</sup> (31%)                            |

**Table A-2: Area of N-KPROC Arrays**

148. The above areas for the N-KPROC ISA do not account for the reduction in processor size of using an 8-bit architecture (or scaling the pad frame and clock generation). As discussed above in §§VIII.A.1-VIII.A.2 in connection with the 8-bit KPROC ISA, each processor in an 8-bit architecture would include 8-bit registers and 8-bit computing units. POSAs understood that a significant portion of the size of the .1 mm<sup>2</sup> Schmidt-2000 processor (see Schmidt, 164) would have been consumed by the 64 registers because in the bit-serial operation of the “parallel-serial design” of the computing units (Schmidt-2000, 166) resulted in a small relative size for the computing units—which is the very reason Schmidt-2000 chose this architecture. Schmidt-2000, 164 (“Due to the limited area the processor had to be very compact. In fact, this was the reason for the choice of a bit serial data organization”).

149. Therefore, the “size of the of the local memory was limited to 64 (16-bit) general-purpose registers plus one communication register” (Schmidt-2000, 163-164). Thus, POSAs would have understood that reducing the size of this local

memory to 8-bits would have significantly reduced the area of each Schmidt-2000 and the reduction of the computing units to 8-bit computing unit could have reduced the overall area of the Schmidt-2000 processor by as much as a half or close thereto. This is corroborated by the area of the 8-bit processor disclosed in Schmidt-1999 (955, Tables 1 and 2).

150. In particular, Schmidt-1999 implemented 8-bit processors for the ISA, each with 32 (8-bit) general-purpose registers and two communication registers and 8-bit computing units (arithmetic, logic and multiplier computing units) as illustrated in Fig. 3 reproduced below (left). Schmidt-1999, 953-955. Tables 2 illustrates the total area of the 96-processor ISA (“12x8 ISA of the described processors,” Schmidt-1999, 954) was 3.7 mm<sup>2</sup> for a per-processor area of .038 mm<sup>2</sup> (shown in Table 1) compared to the .1 mm<sup>2</sup> Schmidt-2000 processor (Schmidt-2000, 164).

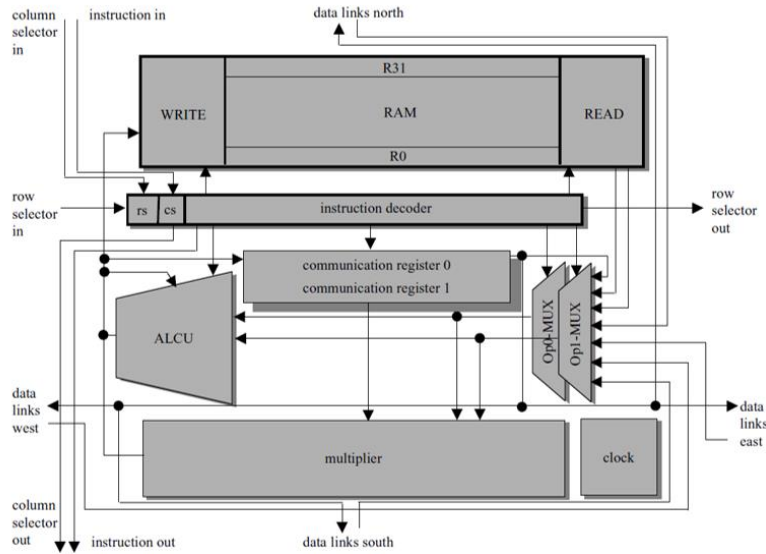


Fig. 3: Architecture of the array processor

Table 1: Area of the individual processor.

|                      |                                          |
|----------------------|------------------------------------------|
| RAM                  | 12.144 $\mu\text{m}^2$                   |
| Multiplier           | 6.398 $\mu\text{m}^2$                    |
| Read-write-logic     | 2.874 $\mu\text{m}^2$                    |
| ALCU                 | 5.125 $\mu\text{m}^2$                    |
| Instruction decoder  | 4.011 $\mu\text{m}^2$                    |
| Addressing           | 1.190 $\mu\text{m}^2$                    |
| Routing              | 1.674 $\mu\text{m}^2$                    |
| Operand multiplexers | 2.133 $\mu\text{m}^2$                    |
| Clock                | 2.613 $\mu\text{m}^2$                    |
| <b>Sum</b>           | <b>38.135 <math>\mu\text{m}^2</math></b> |

Table 2: Area of the accelerator.

|              |                                     |
|--------------|-------------------------------------|
| ISA          | 3.7 $\text{mm}^2$                   |
| Controller   | 1.1 $\text{mm}^2$                   |
| Internal RAM | 3.3 $\text{mm}^2$                   |
| <b>Sum</b>   | <b>8.1 <math>\text{mm}^2</math></b> |

151. Schmidt-1999 implemented 32 registers (plus two communication registers) compared to the 64 registers (plus one communication register) of the Schmidt-2000. Doubling the size of the registers (RAM in Schmidt-1999's Table 1 above) would have resulted in a .05  $\text{mm}^2$  Schmidt-1999 processor, approximately half the area of the 16-bit Schmidt-2000 processor. The Schmidt-1999 ISA does not include floating-point support and therefore does not include floating-point control logic or the shift/add logic for the multiply-add. But because Schmidt-2000's floating-point unit uses the multiplier and adder for floating-point operations, POSAs understood the additional control and shift/add logic would require relatively small additional area and that .05  $\text{mm}^2$  is therefore a reasonable estimate of the area of an 8-bit Schmidt-2000 processor.

152. As an overly conservative estimate of an 8-bit Schmidt-2000 processor, even providing for a 20% increase in area (which would be an increase in size larger than whole multiplier in Table 1 of Schmidt-1999, the largest computing unit in the Schmidt-1999 processor) to account for the control and logic that Schmidt-2000 implemented to support floating-point operations, the resulting 8-bit Schmidt-2000 processor would have an area of approximately .06 mm<sup>2</sup>—60% the size of the Schmidt-2000’s 16-bit processor. The area of an 8-bit 5-KPROC, 9-KPROC and 16-KPROC ISAs (.06 mm<sup>2</sup> processor per above) is illustrated below in Table A-3.

| Process Node | 8-bit 5-KPROC ISA<br>(% <u>KPROC ISA</u> ) | 8-bit 9-KPROC ISA<br>(% <u>KPROC ISA</u> ) | 8-bit 16-KPROC ISA<br>(% <u>KPROC ISA</u> ) |
|--------------|--------------------------------------------|--------------------------------------------|---------------------------------------------|
| 65-nm        | 12.8 mm <sup>2</sup> (13%)                 | 23 mm <sup>2</sup> (23%)                   | 40.96 mm <sup>2</sup> (40%)                 |
| 45-nm        | 9.9 mm <sup>2</sup> (10%)                  | 17.8 mm <sup>2</sup> (17%)                 | 31.7 mm <sup>2</sup> (13%)                  |
| 40-nm        | 5.9 mm <sup>2</sup> (6%)                   | 10.6 mm <sup>2</sup> (10%)                 | 18.9 mm <sup>2</sup> (18%)                  |

**Table A-3**

153. Schmidt-1999 also demonstrates the significant power reduction of using an 8-bit architecture discussed in §§VIII.A.1-VIII.A.2 above in connection with implementing the 8-bit KPROC-chip. In particular, Schmidt-1999 disclosed that at a clock frequency of 300 MHz, the estimated power consumption of the 96-processor ISA is 120mW (.120W)—i.e., 1.25mW per processor. Schmidt-1999, 954. Compare this to the per-processor power dissipation of “slightly above 4mW” of the Schmidt-2000 processor with a 16-bit architecture at a clock rate of 400

MHz. Even a proportional scale of power consumption to clock rate (1.25), the expected power consumption of an 8-bit Schmidt-2000 would be approximately 1.67mW (1.25mW time 1.25 clock rate scale factor) and the power dissipation of an 8-bit KPROC ISA would have expected to be below 2W and as low as approximately 1.7W, significantly less than the 5W that Schmidt-2000 disclosed the KPROC ISA “should dissipate,” demonstrating the significant power reduction of using an 8-bit architecture.

154. In addition, POSAs understood that process scaling also reduced power consumption as advances in semiconductor processing provided reduced power supplies as transistor gate voltages decreased. The smaller transistor sizes required less power and more energy efficient designs were continually developed.

155. Thus, each of these obvious implementations that substantially increase the computational performance of the KPROC-chip would have occupied only a fraction of the area of the original KPROC-chip and at reduced power consumption and POSAs would have had a reasonable expectation of success in arriving at them, even within the constraints that Schmidt-2000 imposed on its KPROC chip, which POSAs understood were not technological limitation but design choice. For example, Schmidt-2000 disclosed that the “chip area should not exceed 1.2 cm<sup>2</sup>” but, in fact, proposed adding an on-chip cache to address I/O bandwidth limitations and therefore contemplated a larger chip design

demonstrating that the 1.2 cm<sup>2</sup> (120 mm cm<sup>2</sup>) chip used by Schmidt-2000 was a design choice and not a limitation on available chip sizes that a POSA would have understood were available even in the timeframe in which the KPROC-chip was designed, let alone taking into account the larger chip-sizes available and routinely used before June 2009.

156. As estimate of the size of an on-chip cache for the KPROC ISA can be approximated from the size of the on-chip RAM implemented in Schmidt-1999 discussed above in §§VIII.A.1-VIII.A.2 in connection with the 8-bit architecture. In particular, Schmidt-1999 discloses that 8KB of on-chip-cache RAM for a 96-processor ISA occupied an area of 3.3 mm<sup>2</sup> at a 250-nm process, as illustrated in Fig. 4 and Table 2 of Schmidt-1999 reproduced below.

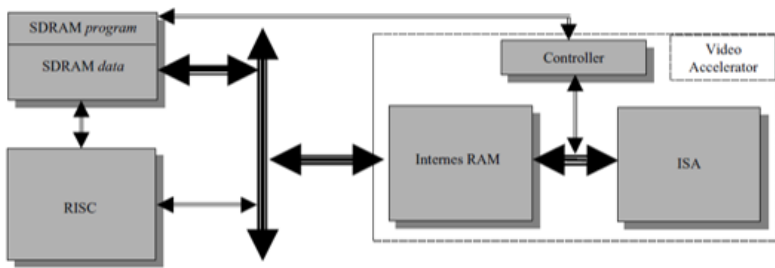


**Table 2:** Area of the accelerator.

|              |                           |
|--------------|---------------------------|
| ISA          | 3.7 mm <sup>2</sup>       |
| Controller   | 1.1 mm <sup>2</sup>       |
| Internal RAM | 3.3 mm <sup>2</sup>       |
| <b>Sum</b>   | <b>8.1 mm<sup>2</sup></b> |

**Fig. 4:** Video accelerator architecture and data paths to the environment.

157. To estimate the size of the on-chip cache for the KPROC ISA, the same ratio of on-chip RAM per processor (i.e., 8KB/96 of RAM per processor) is preserved in scaling-up the on-chip cache. The size of the on-chip cache for Schmidt-2000's KPROC ISA was thus estimated by multiplying the per-processor

size of memory by 3.3 mm<sup>2</sup> (size at 250-nm) and by the 1024 (the number of processors on the KPROC ISA also at 250-nm), resulting in an area of 35.2 mm<sup>2</sup> at 250-nm, which would have required 137.7 mm<sup>2</sup> of area for the 1024-processor KPROC ISA disclosed in Schmidt-2000. Thus, to implement the on-chip cache proposed by Schmidt-2000 would have required an increase in chip area that POSAs would have understood were available even in 2000 (see e.g., Intel's 250-nm Mendocino chip at 154-mm<sup>2</sup> discussed above).

**B. Claim 7**

158. The obvious implementation of the system disclosed in Schmidt-2000 (i.e., a host processor using the KPROC chip as a coprocessor) with an 8-bit N-KPROC chip meets all limitations of claim 7 as demonstrated below.

**1. [7PRE]: “A computing system, comprising:”**

159. Schmidt-2000's “host computer” (Schmidt-2000, 163) together with the 8-bit N-KPROC chip described above as a coprocessor meet the “*computing system*” recited in [7PRE].

**2. [7A]: “a host computer;”**

160. Schmidt-2000's “host computer” utilizes a KPROC-chip as a “coprocessor” and meets [7A]. Schmidt-2000, 163.

**3. [7B]: “a computing chip comprising:”**

161. Schmidt-2000's “KPROC is an ISA with 1024 processors *integrated on a single chip*” called a “KPROC-chip.” Schmidt-2000, 163 (The KPROC-chip

“consists of 1024 of these processors *integrated on one die* using a 0.25-micron digital CMOS process.”). The 8-bit N-KPROC-chip discussed above (§§VIII.A.1-VIII.A.2) is implemented on the same chip disclosed in Schmidt-2000, but includes a larger number of processors on the same chip and therefore meets the “*computing chip*” recited in [7B].

4. [7C] “a processing element array comprising a plurality of first processing elements, wherein the plurality of first processing elements is no less than 5000 in number, wherein each of a first subset of the plurality of first processing elements is positioned at a first edge of the processing element array, and wherein each of a second subset of the plurality of first processing elements is positioned in the interior of the processing element array;”

162. As discussed in §§VIII.A.1-VIII.A.2 above, the 8-bit N-KPROC-chip uses the mesh-connected “processor array” disclosed in Schmidt-2000 (163-164, 169, 176), but with higher numbers of processors—i.e., the claimed “*plurality of first processing elements*”—in the array integrated on the chip, and therefore meets “*a processing element array comprising a plurality of first processing elements*” for the same reasons discussed in §VIII.B.4 above in connection with limitation [1C] of claim 1.

163. As discussed in §IX.A.3 above, an 8-bit 5-KPROC-chip (5,184 processors), 9-KPROC-chip (9,216 processors), and 16-KPROC-chip (16,384 processors) would each have been obvious and desirable scaled-up implementations of Schmidt-2000’s system by June 2009 (as would be numerous

other implementations), and each implements well over 5000 processors (i.e., the claimed “*first processing elements*” on a single chip. See also §VIII.B.4 above in connection with [1C] of claim 1.

164. As discussed in §VIII.B.4 ([1C]) above any of the processors in the top row or left-most column (or bottom row or right-most column) outlined in **red** in annotated Fig. 2.1 below is a processing element positioned at an “*edge of the processing element array,*” and any of the processors outlined in **blue** is “*positioned in the interior of the processing element array.*”

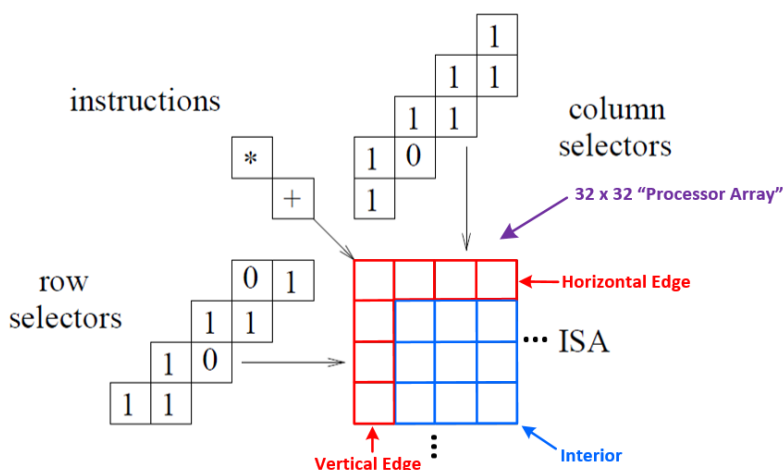


FIG. 2.1. Control flow in an ISA .

165. As an example meeting [7C], the processors in the top row (or alternatively those in the left-most column) outlined in **red** above meet “*a first subset of the plurality of first processing elements*” each of which is “*positioned at a first edge of the processing element array,*” and processors highlighted in **blue** above meet “*a second subset of the plurality of first processing elements*” each of which is “*positioned in the interior of the processing element array,*” as claimed.

5. **[7D]: “an input-output unit connected to each of the first subset of the plurality of first processing elements;”**

166. The 8-bit *N*-KPROC-chip does not alter how the KPROC-chip performs input/output (I/O) and therefore meets [7D] for the same reasons discussed in §VIII.B.6 in connection with limitation [1E] of claim 1.

6. **[7E]: “a plurality of processing element connections, each processing element connection connecting one of the plurality of first processing elements with another of the plurality of first processing elements, wherein each of the plurality of first processing elements is connected to at least one other of the plurality of first processing elements by at least one of the plurality of processing element connections;”**

167. As discussed in §VIII.B.5 in connection with [1D] in claim 1, Schmidt-2000 discloses that “[c]ommunication among adjacent processors occurs via designated communication registers” that can be “read by the four neighbour processors.” Schmidt-2000, 163-164. The four pairs of wires connecting the communication register of each processor to its four adjacent neighbors are shown as north, south, east and west data links (highlighted in red) in Fig. 3.1 (“Architecture of one processor”) reproduced below.

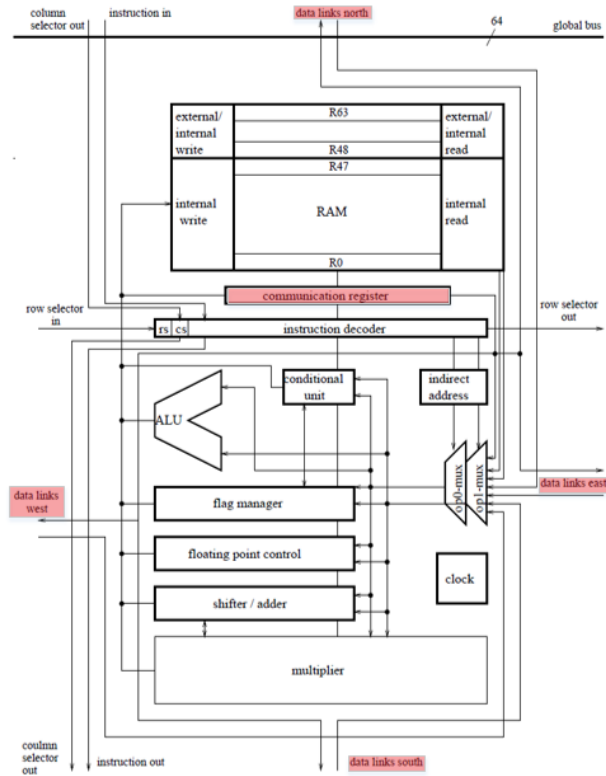


FIG. 3.1. Architecture of one processor.

168. The 8-bit N-KPROC-chip implements 8-bit communication registers but does not modify the wire connections between the communication registers that connect each processor to its four direct neighbors (see §§VIII.A.1-VIII.A.2 above) and therefore the data links connecting the communication registers of each processor in the 8-bit N-KPROC-chip meet the “*plurality of processing element connections*” connected to the “*the plurality of first processing elements*” in the same manner as recited in claim [7E].

7. [7F]: “a plurality of memory units, wherein each of the plurality of first processing elements is associated with a corresponding one of the plurality of memory units, and

**wherein each of the plurality of memory units is local to its associated one of the plurality of first processing elements”**

169. As discussed in §VIII.B.7 above in connection with [1F] of claim 1, Schmidt-2000 discloses every processor has its “own” 64 general-purpose registers of addressable “local memory” shaded in blue in Fig. 3.1 below. Schmidt-2000, 164. The 8-bit N-KPROC-chip uses this same memory structure, but with 8-bit registers (see the discussion of the 8-bit architecture in §§VIII.A.1-VIII.A.2 above), and therefore each processor’s 64 registers (or alternatively, just registers R0-R47) of the 8-bit N-KPROC-chip meets one of the “*plurality of memory units*” and therefore the memory unit of the numerous processors on the 8-bit N-KPROC-chip meet [7F].

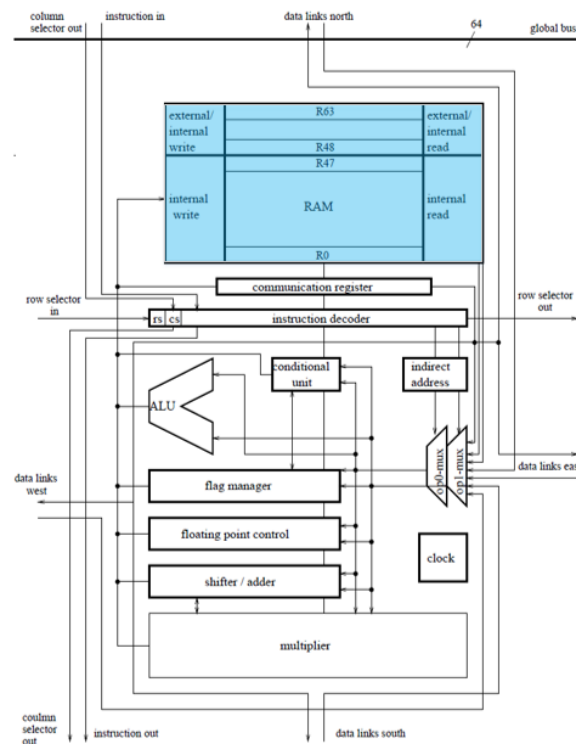


FIG. 3.1. Architecture of one processor.



*elements has positioned therein at least one of the plurality of arithmetic units,” as recited in [7G].*

**9. [7H]: “a host connection at least partially connecting the input-output unit with the host computer”**

172. The 8-bit N-KPROC-chip does not change the ways in which Schmidt-2000 discloses performing “off-chip communication...between the host computer and the KPROC-chip and therefore the I/O pins of the 8-bit N-KPROC-chip meet [7H] for the same reasons discussed in §VIII.B.9 in connection with [1H] of claim 1.

**10. [7I]: “wherein the plurality of arithmetic units each comprises a first corresponding multiplier circuit adapted to receive as a first input to the first corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the first corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits”**

173. As discussed above in §VIII.B.10 ([1I]), the 8-bit N-KPROC-chip uses the 8-bit architecture for the KPROC ISA described in §§VIII.A.1-VIII.A.2 (but uses higher numbers of Schmidt-2000 processors) and therefore meets [7I] for the same reasons Schmidt-2000’s computing units meet limitation [1I] of claim 1 as discussed in §VIII.B.10 above in connection with limitation [1I] of claim 1.

**C. Claim 9: “the plurality of memory units each comprises a corresponding register”**

174. As discussed above in §IX.B.7, each processor’s “local memory” are addressable “general purpose registers” (Schmidt-2000, 164) that meet the claimed “*memory units.*” The 8-bit N-KPROC-chip also utilizes this register file but with 8-bit registers and therefore each of “*the plurality of memory units each comprises a corresponding register,*” because each register file comprises multiple registers, any one of which is “*a corresponding register*” as claimed in claim 9.

**D. Claim 14: “the width of each [first/second] binary mantissa is no more than 10 bits plus a [first/second] sign bit”**

175. As discussed supra §IX.B.10, the floating-point multiplier circuit of each 8-bit processor of the 8-bit N-KPROC-chip is adapted to receive first and second inputs having up to 8-bit mantissas (i.e., whose widths are less than 10 bits plus a sign bit).

**X. GROUND 2: CLAIMS 2-3 ARE OBVIOUS OVER SCHMIDT-2000 IN VIEW OF SCHMIDT-1999**

**A. Schmidt Combination**

176. Schmidt-2000 discloses that instructions executed on the KPROC ISA are “input in the upper left corner of the processor array” as are the row/column selectors (Schmidt-2000, 164), but does not describe the component that issues these instructions and selectors to the ISA. The obvious and conventional way in which instructions were issued to a parallel array was via a controller like the

controller disclosed in Schmidt-1999. Schmidt-1999, 955-956. As discussed above in §VIII.A.1, the authors of Schmidt-2000 disclosed an 8-bit-architecture implementation of a similar ISA for a video accelerator, as illustrated in Fig. 1 (below left) and Fig. 3 (below right). Schmidt-1999, 951-955. Schmidt-1999 uses substantially the same architectural features as Schmidt-2000 but optimized for integer operations (i.e., floating-point support was not implemented).

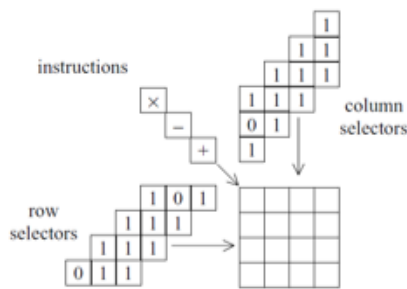


**Fig. 1: Control flow in an ISA**

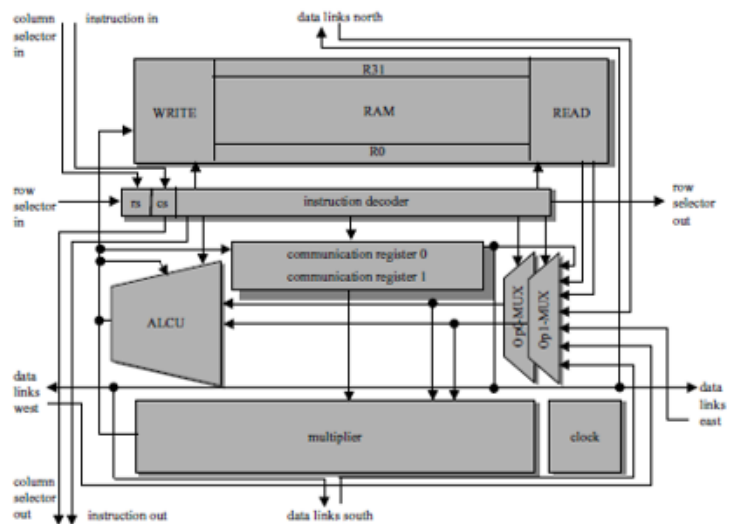


**Fig. 3: Architecture of the array processor**

177. As illustrated in Fig. 4 of Schmidt-1999 below, an on-chip controller is provided that “supplies the processor array with instructions and selectors as illustrated in Figure 4 of Schmidt-1999 above. Schmidt-1999, 955-956. It would have would have been obvious to use an on-chip controller to issue instructions and selectors to the 8-bit KPROC ISA, the obvious and desirability of which does

change in view of differences between the two processors (i.e., with or without floating-point support).

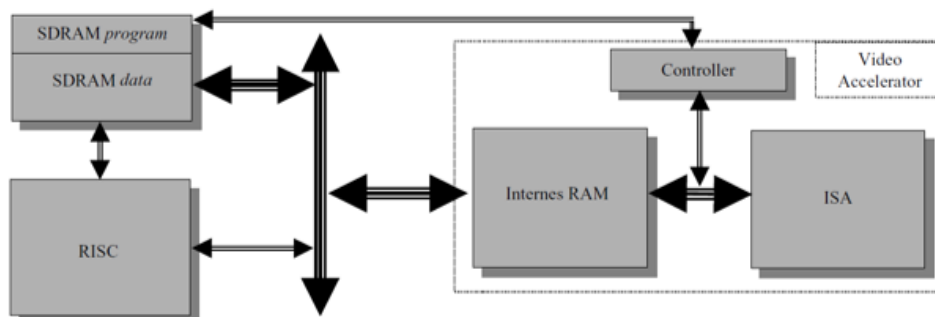


**Fig. 4:** Video accelerator architecture and data paths to the environment.

178. To reduce the number of off-chip input/output operations, Schmidt-2000 proposed introducing a “memory hierarchy” using a cache “integrated onto the KPROC-chip.” Schmidt-2000, 176. Schmidt-1999 also adopted a “cascaded memory” organization “implemented on-chip” using the same switched memory bank configuration as Schmidt-2000 and disclosed coupling the first memory bank to an on-chip RAM via a “fast data channel” (Schmidt-1999, 954-955, Fig. 4 reproduced above), like the on-chip cache that Schmidt-2000 proposed implementing to reduce the number of off-chip I/O operations that needed to be performed. Schmidt-2000, 176.

179. Thus, in view of these teachings by the same authors on very similar architectures, an obvious and desirable implementation of the 8-bit KPROC-chip described above in §§VIII.A.1-VIII.A.2 (the discussion of the 8-bit KPROC-chip) in view of Schmidt-1999 (“Schmidt combination”) would have been to implement

an on-chip cache as Schmidt-2000 proposed and to include a controller (as disclosed in Schmidt-1999) to issue instructions and selectors to the KPROC array and to control the data transfer between the on-chip cache and registers R48-R63 of Schmidt-2000's processors (see Fig. 3.1 of Schmidt-2000 and §VIII.B.6 above describing the claimed "*input-output unit*") as disclosed in the Schmidt-1999 system. Schmidt-1999, 955 (disclosing that the "data transfer between ISA [via the "interface registers"] and internal RAM" is "controlled by [the] on-chip controller" via the "fast data channel").

180. Schmidt-2000 discloses that the on-chip cache "must be global, i.e., every processor can access the cache for data exchange." Schmidt-2000, 176. Thus, the obvious way to implement the on-chip cache would have been to couple the on-chip cache and the 64-bit global bus to make the on-chip cache accessible by every processor (as Schmidt-2000 says it "must" be), as well as allowing the cache to access and store the data received from external memory (like Schmidt-1999's on-chip RAM communicates "bidirectionally with the external SRAM"—Schmidt-1999, 955). Schmidt-2000, 176. In this manner, the processors can access data from the cache and avoid repeating off-chip communication via the "limited I/O bandwidth" of the I/O pins, thereby "gain[ing] performance by reuse of data," as disclosed in Schmidt-2000. Schmidt-2000, 176.

181. In Schmidt-2000's KPROC architecture, data is exchanged with external memory by either writing data from external memory to the corresponding processor's registers R48-R63 shown in Fig. 3.1 of Schmidt) or reading data from those registers to external memory by first using a "special instruction" to write data from registers R0-R67 to R48-R63, the latter of which are "connected to the outside." Schmidt-2000, 168. Reads and writes to the external memory are both supported—e.g., "[r]andom access data exchange with external memory is possible." Schmidt-2000, 168. A conventional and obvious way to implement the "special instruction" in the Schmidt-2000 Combination would have been to use conventional load and store instructions that are performed by the on-chip controller.

182. For a load instruction (i.e., to load data operands into a processor's registers), the on-chip controller would transfer the data needed by each processor from the cache to registers R48-R63 (or if the data is not already in the cache, to first retrieve the data from the external memory and store it in the cache) and instruct the processors to switch the content of the memory banks so that the data on which each processor is to operate is loaded into the processor's internal registers R0-47. Schmidt-2000, 168.

183. For a store instruction (i.e., to read output results from the processors), the on-chip controller would be configured to first instruct each processor to switch

memory banks and then read the contents of the external registers and store that data in the cache. In this way, the on-chip cache also can operate as an I/O buffer for data exchange with the host computer, similar to Schmidt-1999's on-chip RAM with the off-chip RISC control and external SRAM. Schmidt-1999, 955-957.

184. The Schmidt combination meets each of the limitations recited in claim 1 for the same reasons the 8-bit KPROC-chip meets each of claim 1's limitations as discussed above in §VIII.B (limitation-by-limitation analysis of claim 1). Further, in the Schmidt combination, the global data bus coupled to registers R47-63 of each processor and with their corresponding I/O circuitry (together or individually) are an “*input-output unit*” as claimed as discussed above in §VIII.B.6 in connection with the claimed “*input-output unit* in claim 1. Alternatively, those components together with the on-chip cache also are “*an input-output unit*” as recited in [1E] as also discussed above in §VIII.B.6—i.e., these components provide an interface with the host computer to “get data into and out of” ('616 patent, 9:7-9) of the processor array.

185. Schimmler-1996 (described in further detail in §XY below and discussed above in §XII also describes this “cascaded memory” (Schimmler-1996, 138) structure using with on-chip RAM and on-chip controller to issue instructions to a 16-bit ISA, like disclosed in Schmidt-2000, and to control the data transfer between the on-chip RAM, the ISA and the external host (Schimmler-1996, 138-

139), demonstrating the obviousness of the above-described conventional I/O structure for the KPROC ISA disclosed in Schmidt-2000. It would have been obvious to use this I/O and instruction control scheme for the KPROC-chip for the same reasons.

**B. Claim 2: “the computing chip further comprises a control unit connected to the processing element array, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the processing element array to cause the processing element array to operate according to the at least one instruction.”**

186. In the Schmidt combination, the on-chip controller meets the limitations of claim 2 because the on-chip controller—i.e., the claimed “*control unit*”—is adapted to decode load/store instructions provided in the instruction stream from the host computer via the input-output unit (including the global bus) to load operands into or read results from the registers of each processor, and configured to thereafter issue the special instruction (i.e., “*control signals*” as claimed that tell the processor how to operate) to the corresponding processor in the array to read/write data between the two register files as instructed. Furthermore, for a load instruction, the subsequent instructions and row/column selectors issued to the array that instruct the processor to operate on that data are also “control signals” that cause the array to operate in accordance with the load/store instructions.

- C. **Claim 3: “the computing chip” of Claim 2 “further comprises an instruction memory adapted to store the at least one instruction received from the host computer via the input-output unit, wherein the control unit is further adapted to retrieve the at least one instruction from the instruction memory.”**

187. An obvious way to implement the on-chip controller in the Schmidt combination would have been to provide an on-chip instruction queue to buffer the instruction stream provided by the host computer so that the on-chip controller can synchronize the execution of instructions with the “global clock” of the ISA and can operate asynchronously with the host computer. Schmidt-2000, 163 (“The array is synchronised by a global clock”). This on-chip instruction queue meets the “*instruction memory*” recited in claim 3. In fact, Schimmler-1996 discloses the use of an on-chip instruction queue for the on-chip controller corroborating the obviousness of using this well-known architecture. Schimmler-1996, 138-139. This on-chip instruction queue, from which the on-chip controller (i.e., the claimed “*control unit*”) is adapted to retrieve the instructions, meets claim 3’s “*instruction memory*.”

**XI. GROUND 3: CLAIMS 8, 10-13 ARE OBVIOUS OVER SCHMIDT-2000 IN VIEW SCHMIDT-1999 AND KAN**

188. Schmidt-2000 that an instruction systolic array, like the KPROC ISA, provides “high performance hardware for *specific* computation intensive applications” and is typically used by a sequential host as a coprocessor that

“solves **only** the computationally intensive tasks within a **global application**.”

Indeed, single-instruction multiple-data (SIMD) architectures (of which ISAs are one particular type) were known to provide high performance for a limited class of computations—large-scale repetition of the same simple computations on different data. Schmidt-2000, 309; Kan, 2:14-17; EX1019, 24; EX1020, 226. See Appendix, II.C.7 and II.C.8 for my opinion on the public accessibility of EX1019, EX1020, respectively.

189. However, many application areas such as image processing and multimedia applications also include other levels of parallelism or types of processing, such as task-level parallelism, irregular computations or process flow, or complex data dependency for which SIMD-type architectures are not well suited. Kan, 1:50-2:49. Thus, for many image processing applications, acceleration is limited to portions of the global application when relying solely on SIMD-type architectures to increase performance.

**A. Kan (EX1015)**

190. Kan recognized that SIMD and MIMD (multiple-instruction multiple-data) had respective advantages and disadvantages that made one well-suited to some application areas and not others (and vice versa). Kan, 1:50-68. Moreover, SIMD and MIMD architectures had respective advantages/disadvantages with

respect to different types of processing within a single application field. Kan, 2:7-49.

191. Kan discloses a parallel processing system combining both SIMD-type and MIMD-type units to take advantage of each architecture, while each compensates for the respective drawbacks of the other, thereby providing an improved parallel processing system and optimized for the different types of processing within a given application field, such as image processing. Kan, 2:45-56. FIG. 1 of Kan reproduced below illustrates an example of a hybrid parallel processing system combining a SIMD-type unit and a MIMD-type unit.

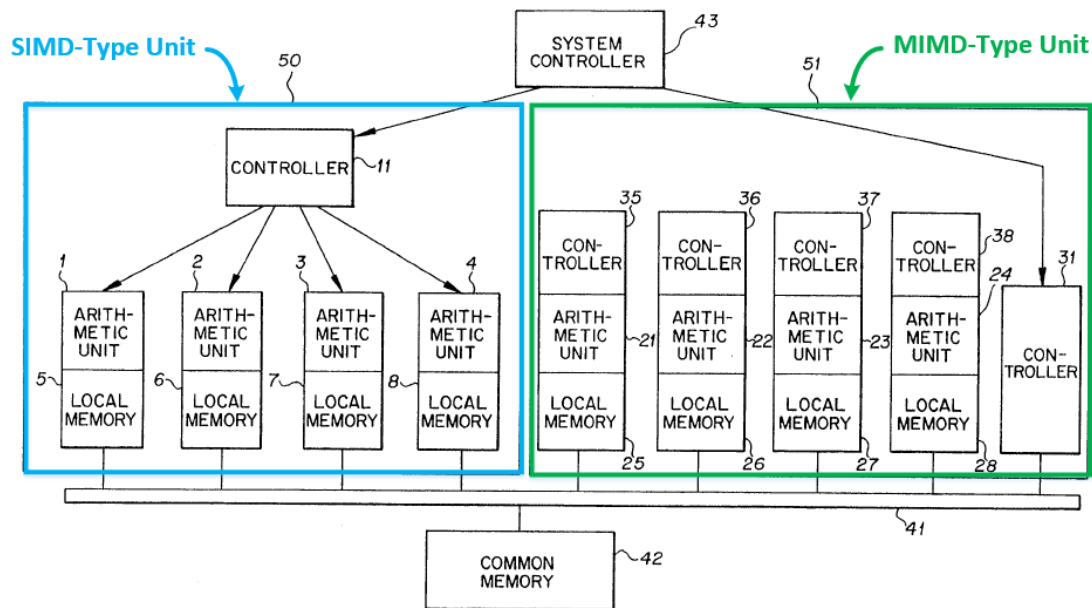


FIG. 1

192. The above-illustrated hybrid system comprises a “**SIMD type**” parallel data processing unit 50 and a “**MIMD type**” parallel data processing system 51, both of which are coupled to a system controller 43 that allocates

processing of programs to each parallel-processing unit depending on which unit is more suitable for that type of processing. Kan, 4:10-32. The system controller 43 can utilize the SIMD-type unit 50 and MIMD-type unit 51 to execute separate programs operating on different data, execute portions of a program that operates on the same data (including data computed by the other unit) and/or to execute the same program independently and the results compared. Kan, 4:24-5:4, 7:1-8:18.

## **B. Schmidt-Kan Combination**

### **1. Motivation**

193. Given the known limitations of accelerating processing using a single type of parallel processing architecture, a POSA would have been motivated to integrate aspects of Kan's hybrid parallel data processing system on the same chip as the 8-bit N-KPROC ISA to provide a more flexible single-chip coprocessor capable of accelerating a wider array of computations and more types of processing within a given application area, such as image processing for which the 8-bit N-KPROC ISA is optimized as discussed above in §§VIII.A.1-VIII.A.2 discussing the 8-bit architecture. Kan, 1:24-3:55, 9:31-10:16.

194. In particular, a POSA would have been motivated to integrate a MIMD-type unit like Kan's MIMD unit 51 on the 8-bit N-KPROC-chip to provide a hybrid single-chip coprocessor (Schmidt-Kan coprocessor) that benefits from the acceleration of not only large-scale parallelism via the N-KPROC array, but

processing tasks for which the N-KPROC array is not well-suited but for which Kan's MIMD-type unit is optimized, such as course-grain parallelism, task parallelism (e.g., repetition of routines with substantial sequential or irregular computations), or complex data processing (e.g., complex data flow, frequent branch conditions or data dependency), etc., that are present in image processing applications. Kan, Abstract, 1:50-2:56, 4:22-32.

195. Schmidt-2000 discloses that the KPROC was the "first implementation of a parallel computer with 1024 floating-point processors on a single chip" using a 250-nm process and that the KPROC processors were specifically designed with the "the goal of integration of 1024 processors on a single chip." Schmidt-2000, 163, 166. Thus, Schmidt-2000 recognized the desirability of integrating as much processing power on a single chip as the available semiconductor processes would allow.

196. Indeed, Schmidt-2000 cites Schimmler-1996 (EX1011), authored by Schmidt-2000's co-author Schimmler, where a 1024-processor array was obtained by assembling sixteen 64-processor chips on a circuit board, corroborating the desirability of increased levels of single-chip integration as advance in semiconductor technology permitted. Schimmler-1996, 136-139; see also EX1010 ("Schimmler-1994"), 487 (also describing an add-on board implementation where "[t]here are 16 ISA chips on the board, each comprising 64 processors.").

197. By extension, POSA would have likewise been motivated to implement the Schmidt-Kan coprocessor as a single-chip solution to take advantage of the known benefits of integrating desired functionality on a single-chip. Increasing single-chip functionality is the fundamental principle underlying Moore's Law and that drove (and still drives) the semiconductor industry to continually (and rapidly) develop smaller semiconductor components.

## **2. Implementing the Schmidt-Kan Coprocessor**

198. As discussed above in §XI.B (Schmidt Combination), an obvious and desirable implementation of the KPROC-chip would have to been to implement an on-chip controller and cache coupled to the 8-bit KPROC ISA and POSAs would have been motivated to implement a Schmidt-Kan coprocessor with or without an on-chip controller and on-chip cache.

199. A POSA seeking to provide a hybrid coprocessor that takes advantage of both types of parallelism for which the KPROC ISA and a MIMD-type unit like Kan's are respectively well-suited would have been motivated to integrate a MIMD-type unit on the same chip as the 8-bit N-KPROC ISA to provide a single-chip solution that can be utilized as a coprocessor by a host computer. An obvious implementation of a Schmidt-Kan coprocessor would have been to integrate a "MIMD type" parallel data processing system 51 like Kan's (annotated in **green** in Kan's FIG. 1 above) on the 8-bit N-KPROC-chip in association with the N-

KPROC ISA with or without the on-chip controller and cache discussed in §XI.B (Schmidt combination) are shown in Figures A-1 and A-2 below (using Kan's **MIMD-type unit** from FIG. 1 of Kan).

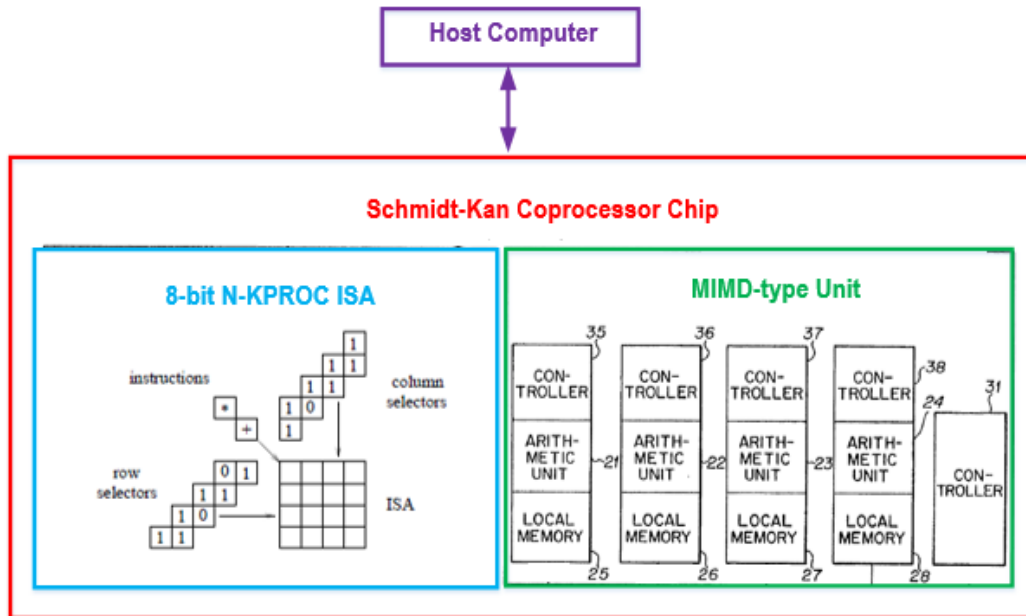


**Figure A-1: First Exemplary Schmidt-Kan Coprocessor Chip**

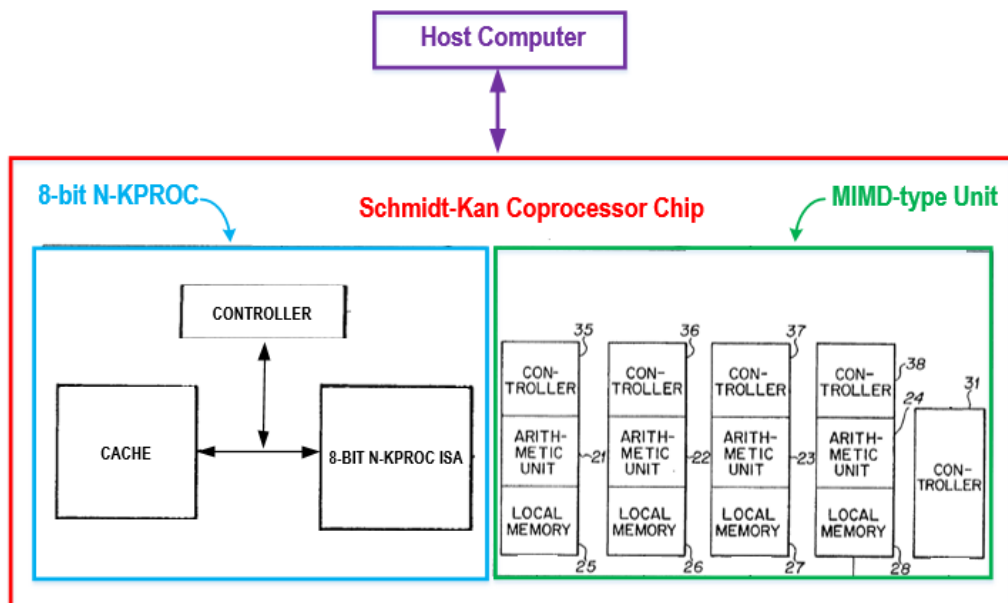


**Figure A-2: Second Exemplary Schmidt-Kan Coprocessor Chip with  
On-chip Controller and Cache**

200. POSAs would have understood that Kan’s system controller 43—which comprises “a data processor 90, a memory 91, a bus connector 92, a disk unit 93 and an internal bus 106” that processes “user programs...stored in the memory 91,” transfers data “stored in the disk unit 93...to the common memory 42,” and selects “either one of the parallel data processing units 50 and 51” to execute user programs—operates as a host computer (annotated above in Fig. A). Kan, 6:13-23. See also EX1001, 8:29-30, FIG. 1 (“The Host 102 is responsible for overall control of the computing system 100.”).

201. Thus, POSAs understood that the “host computer” or “sequential host” configured to execute programs that utilize the KPROC ISA to accelerate specialized tasks would likewise be configured to control the execution of user programs in the hybrid system combining Schmidt-2000 and Kan, referred to hereinafter as the Schmidt-Kan Coprocessor. It would have been obvious to POSAs to connect the integrated MIMD-unit to the Schmidt-2000’s “global bus” to perform off-chip communication with the host computer’s external memory (e.g., by connecting the controller 35 of each MIMD-processing element 109 to the global bus) like the KPROC ISA performs I/O (and similar to manner in which Kan’s SIMD and MIMD units were connected to a shared bus 41 to access common non-local memory 42 shown in FIG. 1 of Kan above). Kan, 5:39-6:12

### 3. Reasonable Expectation of Success

202. POSAs would have reasonably expected success implementing the above-described Schmidt-Kan coprocessor on a single chip of the same size as Schmidt-2000's KPROC-chip because it merely involves the ordinary skill of using the available semiconductor process technology in 2009.

#### a. Process Node Scaling

203. As discussed in §IX.A.2.b on process scaling and illustrated in Table B-1 reproduced below, numerous obvious implementations of an N-KPROC ISA could have been implemented on a fraction of the area of the KPROC-chip disclosed in Schmidt-2000 using process nodes available before June 2009.

| Process Node | Scale Factor | Per-Processor Area    | 5-KPROC Area<br>(72 x 72)<br>(% <u>KPROC ISA</u> ) | 9-KPROC Area<br>(96 x 96)<br>(% <u>KPROC ISA</u> ) | 16-KPROC Area<br>(128 x 128)<br>(% <u>KPROC ISA</u> ) |
|--------------|--------------|-----------------------|----------------------------------------------------|----------------------------------------------------|-------------------------------------------------------|
| 250-nm       | 1            | .1 mm <sup>2</sup>    |                                                    |                                                    |                                                       |
| 65-nm        | 24           | .0042 mm <sup>2</sup> | 21.3 mm <sup>2</sup> (21%)                         | 38.4 mm <sup>2</sup> (38%)                         | 68.3 mm <sup>2</sup> (67%)                            |
| 45-nm        | 31           | .0032 mm <sup>2</sup> | 16.5 mm <sup>2</sup> (16%)                         | 29.7 mm <sup>2</sup> (29%)                         | 52.9 mm <sup>2</sup> (52%)                            |
| 40-nm        | 52           | .0019 mm <sup>2</sup> | 9.8 mm <sup>2</sup> (10%)                          | 17.7 mm <sup>2</sup> (17%)                         | 31.5 mm <sup>2</sup> (31%)                            |

**Table B-1: Area of N-KPROC Arrays**

204. As discussed above, it would have been obvious and desirable to implement a Schmidt-Kan coprocessor with or without an on-chip controller and cache for the 8-bit N-KPROC ISA (as in the Schmidt combination discussed above). To demonstrate that POSAs would have had a reasonable expectation of success in arriving at either implementation, the estimated areas discussed below

are computed using the larger area of a Schmidt-Kan coprocessor implemented with an on-chip controller and cache. POSAs would have had a reasonable success in arriving at the smaller Schmidt-Kan coprocessor implementation without an on-chip controller and cache for the same reasons.

205. The sizes of 5-, 9- and 16-KPROC ISAs with on-chip controller and cache are shown in the table below can be computed from Schmidt-1999, 955, Table 2. In particular, Schmidt-1999 discloses that 8KB of on-chip-cache RAM for a 96-processor ISA occupied an area of 3.3 mm<sup>2</sup> at a 250-nm process, as illustrated in Fig. 4 and Table 2 of Schmidt-1999 reproduced below.

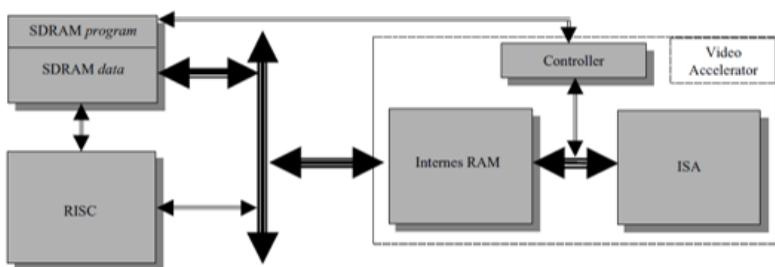


**Table 2:** Area of the accelerator.

|              |                           |
|--------------|---------------------------|
| ISA          | 3.7 mm <sup>2</sup>       |
| Controller   | 1.1 mm <sup>2</sup>       |
| Internal RAM | 3.3 mm <sup>2</sup>       |
| <b>Sum</b>   | <b>8.1 mm<sup>2</sup></b> |

**Fig. 4:** Video accelerator architecture and data paths to the environment.

206. To estimate the size of the on-chip cache for the N-KPROC ISA, the same ratio of on-chip RAM per processor (i.e., 8KB/96 of RAM per processor) was preserved in scaling-up the on-chip cache. The size of the on-chip cache for an N-KPROC ISA was thus estimated by multiplying the per-processor size of memory by 3.3 mm<sup>2</sup> (size at 250-nm) and by the number of processors and dividing by the scale factors illustrated in Table B-1 above. The size of the on-chip

cache for each of the example N-KPROC ISAs in Table B-1 above is illustrated in Table B-2 below.

| Process Node | Scale Factor | 8KB RAM              | 427KB RAM<br>(5-KPROC ISA) | 768KB RAM<br>(9-KPROC ISA) | 1.4MB RAM<br>(16-KPROC ISA) |
|--------------|--------------|----------------------|----------------------------|----------------------------|-----------------------------|
| 250-nm       | 1            | 3.3 mm <sup>2</sup>  |                            |                            |                             |
| 65-nm        | 24           | .138 mm <sup>2</sup> | 7.3 mm <sup>2</sup>        | 13.2 mm <sup>2</sup>       | 23.5 mm <sup>2</sup>        |
| 45-nm        | 31           | .106 mm <sup>2</sup> | 5.7 mm <sup>2</sup>        | 10.2 mm <sup>2</sup>       | 18.2 mm <sup>2</sup>        |
| 40-nm        | 52           | .063mm <sup>2</sup>  | 3.4 mm <sup>2</sup>        | 6.1 mm <sup>2</sup>        | 10.8 mm <sup>2</sup>        |

**Table B-2: Area of On-chip Cache for N-KPROC ISA**

207. The total area of each N-KPROC ISA with an on-chip cache of the size from Table B-2 and a (scaled) 1.1-mm<sup>2</sup> controller (per Table 2 of Schmidt-1999) is illustrated in Table B-3 below.

| Process Node | 5-KPROC ISA          | 9-KPROC ISA<br>(Cache + Controller) | 16-KPROC ISA<br>(Cache + Controller) |
|--------------|----------------------|-------------------------------------|--------------------------------------|
| 65-nm        | 28.7 mm <sup>2</sup> | 51.6 mm <sup>2</sup>                | 91.7 mm <sup>2</sup>                 |
| 45-nm        | 22.2 mm <sup>2</sup> | 39.9 mm <sup>2</sup>                | 71 mm <sup>2</sup>                   |
| 40-nm        | 13.2 mm <sup>2</sup> | 23.8 mm <sup>2</sup>                | 42.3 mm <sup>2</sup>                 |

**Table B-3: Area of N-KPROC ISA with On-chip Cache and Controller**

208. Kan does not disclose the area of the eight processing elements 109 used for MIMD-type unit 51 (Kan, 6:52-54: “MIMD type parallel data processing unit 51 consists of [] eight processing elements 109”), but POSAs knew a wide variety of processors were suitable for use as processing elements 109 and knew that eight such processors could have been integrated on the 8-bit N-KPROC chip using available processing nodes before June 2009. For example, Yeh-ISCA07

(EX1012) and Yeh-Micro07 (EX1013) disclose using processors based on GPU shader cores (hereafter, “Yeh-processor”) in a parallel processor array for a physics-based animation accelerator. Yeh-ISCA07, 233-235, 238-241; Yeh-Micro07, 396, 400-403. Each Yeh-processor in the array independently executes its own instructions on its own data stored in its own local memory—i.e., the array performs multiple-instruction multiple-data (MIMD) parallel processing. Yeh-ISCA07, 233-235, 238-241; Yeh-Micro07, 396, 400-403.

209. As illustrated in Table 6 of Yeh-Micro07, each Yeh-processor includes a controller (shaded yellow), arithmetic unit (green) and local memory (blue) analogous to controller 35, arithmetic unit 21 and local memory 25 of Kan’s processing elements 109. Yeh-Micro07, 401. POSAs understood that this Yeh-processor would have been suitable to implement the processing elements 109 in Kan’s MIMD-type unit 51. Kan, 6:52-68.

|                    |                                      |
|--------------------|--------------------------------------|
| Processor Pipeline | 1-wide, 5-stages, in-order execution |
| Functional Units   | 1 int, 1 fp, 1 ld/st                 |
| Window/Scheduler   | 8,4                                  |
| Branch Predictor   | 384B YAGS + 4-entry RAS              |
| Local Inst Memory  | 4KB, 1-cycle                         |
| Local Data Memory  | 4KB, 1-cycle                         |
| Technology         | 90 nm                                |
| Clock Frequency    | 1GHz                                 |
| FP Latencies       | fpALU (4) fpMult (4) fpDiv (20)      |
| INT Latencies      | iALU (1) iMult (6) iDiv (40)         |

**Table 6. Fine-grain shader core design**

210. Yeh-Micro07 describes techniques for using reduced-precision floating-point-units (FPUs) using the sizes for three different full 32-bit FPUs. Yeh-Micro07, 400-401. Using the largest of the 32-bit floating-point-units (FPUs) disclosed in Yeh-Micro07 to compute the size of a Yeh-processor, the size of an Yeh-processor with 32-bit functional units (including the largest size 32-bit FPU) is  $3.5 \text{ mm}^2$  at a 90-nm process node. Yeh-Micro07, 400 (“We use simple, in-order shader-class cores with the parameters shown in Table 6” with a core area excluding the floating-point unit (FPU) of  $2 \text{ mm}^2$  in 90nm technology.”); 401 (“we explore four FPU designs with varying area requirements:  $1.5 \text{ mm}^2$ ,  $1.0 \text{ mm}^2$ ,  $0.75 \text{ mm}^2$ , and  $0.375 \text{ mm}^2$ .”).

211. Yeh-ISCA07 also discloses using a GPU shader core as the basis for its parallel array of processors based on the Nvidia G80 core processor that POSAs understood would have understood would have been suitable processing elements for use in a MIMD-type array—i.e., both the Yeh-ISCA07 and Yeh-Micro07 processors are pipelined processors used in GPUs capable of independently executing a stream of instructions and include the full range of 32-bit functional units including 32-bit FPUs and branch predictors. Yeh-ISCA07 discloses that 150 shader cores would have an area of  $591 \text{ mm}^2$  at 90-nm—i.e.,  $3.94 \text{ mm}^2$  per processor, slightly larger than the Yeh-Micro07 processor with the largest FPU design due to the larger pipeline, etc. Yeh-ISCA07, 241.

212. As discussed above in §IX.A.2.b above in connection with process scaling, the 90-nm Pentium 4 processor achieved a transistor density of 1.1 million transistors/mm<sup>2</sup>. The transistor scale factors for the 65-nm, 45-nm and 40-nm process nodes from the 90-nm process node computed in the same way the transistor density factors were computed from the 250-nm node illustrated in Table A-1 in the process node scaling section above are illustrated in Table B-4 below. Also shown in Table B-4 below are sizes of an 8-processor MIMD array using the larger of the sizes of the Yeh-processors (i.e, 3.94 mm<sup>2</sup>) at 90-nm at the 65-nm, 45-nm and 40-nm process nodes.

| Process Node | Scale Factor | Yeh-Processor Area   | 8-Processor Array   |
|--------------|--------------|----------------------|---------------------|
| 90-nm        | 1            | 3.94 mm <sup>2</sup> |                     |
| 65-nm        | 2.62         | 1.5 mm <sup>2</sup>  | 12 mm <sup>2</sup>  |
| 45 nm        | 3.43         | 1.15 mm <sup>2</sup> | 9.2 mm <sup>2</sup> |
| 40 nm        | 5.77         | 0.68 mm <sup>2</sup> | 5.5 mm <sup>2</sup> |

**Table B-4: Area for 8-Processor Array**

213. Kan discloses that each of the processing elements 109 in MIMD-type unit 51 includes a 1MB local memory, whereas an 8KB local memory was chosen for the Yeh-processors. Yeh-ISCA07, 240-241. To determine the size of an array of 8 processors including an additional 1MB of local memory, the size of the 8KB RAM in Schmidt-1999 (955, Table 2) was used to compute the size of 1MB of local memory and the total size of an 8MB local memory (i.e., 1MB for each of the

8 processing elements in Kan's MIMD-type unit 51), as illustrated in Table B-5 below for the 65-nm, 45-nm and 40-nm process nodes.

| Process Node | Scale Factor | 8KB RAM              | 1MB RAM               | 8MB RAM               | 8-Processor Array (+8MB Memory) |
|--------------|--------------|----------------------|-----------------------|-----------------------|---------------------------------|
| 250-nm       | 1            | 3.3 mm <sup>2</sup>  |                       |                       |                                 |
| 65-nm        | 24           | .087 mm <sup>2</sup> | 17.85 mm <sup>2</sup> | 137 mm <sup>2</sup>   | 149.5 mm <sup>2</sup>           |
| 45-nm        | 31           | .087 mm <sup>2</sup> | 13.3 mm <sup>2</sup>  | 106.5 mm <sup>2</sup> | 115.6 mm <sup>2</sup>           |
| 40-nm        | 52           | .065mm <sup>2</sup>  | 7.9 mm <sup>2</sup>   | 63.5 mm <sup>2</sup>  | 69 mm <sup>2</sup>              |

**Table B-5**

214. Also illustrated in Table B-5 above is the total size of an 8-processor array MIMD-type unit with each processor including an additional 1MB of local memory by adding the size of 8MB of memory to the size of the 8-processor array from Table B-4. Thus, the size of a Schmidt-Kan Coprocessor using 5-KPROC, 9-KPROC and 16-KPROC ISAs (with controller and on-chip cache) and an 8-processor MIMD-type unit (each with an additional 1MB of local memory) is illustrated below in Table B-6. As shown, both the 5-KPROC and 9-KPROC implementations of the Schmidt-Kan Coprocessor would have been available as a single-chip solution without increasing the size of the KPROC-chip and without accounting for the reduction in size of using an 8-bit architecture.

| Process Node | Schmidt-Kan Coprocessor<br>(5-KPROC ISA) | Schmidt-Kan Coprocessor<br>(9-KPROC ISA) | Schmidt-Kan Coprocessor<br>(16-KPROC ISA) |
|--------------|------------------------------------------|------------------------------------------|-------------------------------------------|
| 65-nm        | 178.2                                    | 229.8 mm <sup>2</sup>                    | 321.5 mm <sup>2</sup>                     |
| 45-nm        | 137.8 mm <sup>2</sup>                    | 155.6 mm <sup>2</sup>                    | 186.7 mm <sup>2</sup>                     |
| 40-nm        | 82.2 mm <sup>2</sup>                     | 92.7 mm <sup>2</sup>                     | 111.3 mm <sup>2</sup>                     |

**Table B-6**

215. As shown in the table above, both the 5-KPROC and 9-KPROC implementations of the Schmidt-Kan coprocessor (highlighted yellow) would have been available as single-chip solutions without increasing the size of the KPROC-chip and without even accounting for the processor-size reduction of using an 8-bit architecture (and without accounting for process scaling of Schmidt-2000's pad frame and clock generation).

216. As discussed above in §§VIII.A.1-VIII.A.2 in connection with the 8-bit KPROC-chip and in §IX.A.2.b in connection with process scaling, an 8-bit Schmidt-2000 processor would occupy approximately 0.6 the area of a 16-bit Schmidt-2000. The area of a Schmidt-Kan Coprocessor with 8-bit 5-KPROC, 9-KPROC and 16-KPROC ISAs (.06 mm<sup>2</sup> processor per above) is illustrated below in Table B-7, demonstrating that an 8-bit 16-KPROC ISA would also have fit on the KPROC-chip without increasing its size. Given that the pad frame and clock generation that occupied 17.6 mm<sup>2</sup> of area on the KPROC-chip would also have scaled, meaningfully more of Schmidt-2000's 120 mm<sup>2</sup> chip area (Schmidt-2000, 164) would have been available.

| <b>Process Node</b> | <b>Schmidt-Kan Coprocessor<br/>(8-bit 5-KPROC ISA)</b> | <b>Schmidt-Kan Coprocessor<br/>(8-bit 9-KPROC ISA)</b> | <b>Schmidt-Kan Coprocessor<br/>(8-bit 16-KPROC ISA)</b> |
|---------------------|--------------------------------------------------------|--------------------------------------------------------|---------------------------------------------------------|
| 65 nm               | 169.7 mm <sup>2</sup>                                  | 185.8 mm <sup>2</sup>                                  | 214 mm <sup>2</sup>                                     |
| 45 nm               | 131.2 mm <sup>2</sup>                                  | 143.7 mm <sup>2</sup>                                  | 165.5 mm <sup>2</sup>                                   |
| 40 nm               | 78.2 mm <sup>2</sup>                                   | 85.7 mm <sup>2</sup>                                   | 98.65 mm <sup>2</sup>                                   |

**Table B-7**

217. Additionally, as shown in Table B-5 above, a significant portion of the area of the above-described Schmidt-Kan coprocessor implementations is contributed by the large 1MB local memory assumed for each processing element 109 of the MIMD-type unit (over 80%, 70% and 60% of the area for the 8-bit 5-KPROC, 9-KPROC and 16KPROC Schmidt-Kan coprocessors described above), and POSAs would have understood that many more single-chip Schmidt-Kan coprocessors could have been implemented without increasing the chip size by reducing the size of the 1MB local memory which POSAs understood was large compared to other MIMD array processors, such as the Yeh-processors discussed above.

**b. Chip-Size**

218. As discussed above in §IX.A.2.b in connection with process scaling, Schmidt-2000 disclosed that the “chip area should not exceed 1.2 cm<sup>2</sup>” but, in fact, proposed adding an on-chip cache to address I/O bandwidth limitations and therefore contemplated a larger chip design (e.g., an on-chip cache using the per-processor on-chip RAM used by Schmidt-1999 would have included approximately 85KB of RAM having an area of 35.2 mm<sup>2</sup> at 250-nm, requiring 137.7 mm<sup>2</sup> of area for a 1024-processor array) demonstrating that the 1.2 cm<sup>2</sup> (120 mm cm<sup>2</sup>) chip used by Schmidt-2000 was a design choice and not a limitation on

available chip sizes that a POSA would have understood were available even in the timeframe in which the KPROC-chip was implemented (e.g., the 154 mm<sup>2</sup> chip of Intel's 250-nm Celeron processor discussed above in §IX.A.2.b on process scaling), let alone taking into account the larger chip-sizes routinely used before June 2009 as demonstrated by the example commercial products discussed in the process node scaling section above.

219. It was the routine and common practice among chip designers to increase the size of the chip to accommodate the desired functionality and, for this reason, chip-size increased by about 12% a year, doubling every six years. Ex. 1022, 7 (chip area has “continued to double every six years (an increase of about 12%/year)”; Ex. 1021 and 1027, 73 (same). Chip-sizes available before June 2009 could have accommodated any of the above-described example Schmidt-Kan coprocessor implementations that POSAs would have had a reasonable expectation of success in implementing thereon using the routine and ordinary practice of using an appropriate chip size.

220. Moreover, POSAs would have understood that any combination of process node and chip-size scaling would have made available sufficient chip-area to implement a wide variety of obvious and desirable Schmidt-Kan coprocessors implementations (including any of the above-described example Schmidt-Kan coprocessor implementations), including increasing (or decreasing) the ratio of

SIMD-type processing elements to MIMD-type processing elements 109 that Kan discloses can be chosen based on processor performance and the nature of the application (Kan chose a  $4096/8 = 512$  ratio for image processing applications, similar to the 5-KPROC implementation). Kan, 5:13-16, 6:23-26, 52-55, 9:31-59.

221. The Schmidt-Kan coprocessor includes the 8-bit N-KPROC ISA discussed above in §§VIII.A.1-VIII.A.2 (8-bit architecture) and §IX.A (scaling-up the KPROC-chip) and therefore meets each of the limitations in claim 7 for the same reasons as the 8-bit N-KPROC-chip discussed above in the limitation-by-limitation analysis of claim 7 in demonstrated supra §IX.B. Any of these obvious implementations of a Schmidt-Kan Coprocessor also meets the limitations of claim 8.

### C. Claim 8

1. **[8A]: “the computing chip further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;”**

222. As discussed in §XI.B.2, the Schmidt-Kan coprocessor includes a MIMD-type unit having eight processing elements. Each of the eight processing elements comprises a “32-bit arithmetic unit 21” (Kan, 6:52-56) for “floating point calculations” (Kan, 9:41-44) on “32-bit real number data” (Kan, 9:46-59)—i.e., a 32-bit floating-point multiplier circuit adapted to receive as inputs two floating-

point values each of width at least 32 bits, to be multiplied). These eight MIMD processing elements thus meet [8A]’s “*plurality of second processing elements.*”.

2. **[8B]: “wherein, other than the plurality of second processing elements, the computing chip has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and”**

223. As discussed above in §VIII.B.10 (limitation [1I] in claim 1) and §IX.B.10 (limitation [7I] in claim 7), the 8-bit *N*-KPROC array implemented on the Schmidt-Kan Coprocessor is composed of processors having an 8-bit architecture and, as such, each comprise a floating-point multiplier configured to receive 8-bit operands and no more and, as such, are not adapted to receive 32-bit floating-point values as inputs. Accordingly, the eight MIMD processing elements are the chip’s only processing elements comprising multiplier circuits “*adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits,*” as recited in [8B].

3. **[8C]: “wherein the plurality of first processing elements is greater in number, by at least 100, than the plurality of second processing elements.”**

224. As discussed in above in §XI.B.2 in connection with the example Schmidt-Kan coprocessor implementations, each of the obvious and desirable 5-KPROC, 9-KPROC and 16-KPROC arrays includes multiple thousands of 8-bit Schmidt-2000 processors, which are thus “*greater in number, by at least 100,*

*than*” than the eight MIMD processing elements of the exemplary Schmidt-Kan coprocessor illustrated above, and therefore meets [8C].

**D. Claim 10**

225. Claim 10 depends from claim 8 and recites the same additional limitations as claim 4 that are met by the obvious use of the KPROC ISA to perform the massive amounts of distance computations involved in comparing a target image with a database of images to identify matches as discussed above in §VIII.C in connection with claim 4. The Schmidt-Kan coprocessor, which likewise utilizes the KPROC ISA but increases the number of processors meets claim 10 for the same reasons demonstrated in the above-identified section for claim 4. In the Schmidt-Kan coprocessor system, the host computer is programmed via processing a “user program” (Kan, 6:13-23) and allocating the distance-computation processing to the N-KPROC ISA—i.e., the host computer (like Kan’s system controller 43) provides the instruction stream corresponding to distance computations (via the on-chip controller) to the N-KPROC ISA for execution.

**E. Claim 11: “an aggregate maximum bandwidth of the plurality of processing element connections exceeds a maximum bandwidth of the host connection.”**

226. Schmidt-2000 discloses that the KPROC array “allows off-chip communication with a data rate of 800 Mbytes per second between host computer and the KPROC-chip” over the pins of the KPROC-chip (Schmidt-2000, 163)—

i.e., the “*host connection*” (see §IX.B.9 above)—and that this “I/O bandwidth” is “limited” relative to the “remarkable processing power” of the KPROC array that achieves “up to 24 giga instructions per second (with respect to 16 bit operations).” Schmidt-2000, 176.

227. Schmidt-2000 discloses that each processor can read from an adjacent processor’s 16-bit (two bytes) communication register via the “*processing element connection*” (see §IX.B.6 above in connection with limitation [7E] of claim 7) and write to its own communication register on each instruction cycle. Schmidt-2000, 164. Therefore, the 1024-processor KPROC array can, in aggregate, transfer 2 Kbytes of information between the array’s communication registers on each instruction cycle (i.e., over the plurality of processing element connections) at a rate of “24 giga instructions per second”—a bandwidth of 48 terabytes per second, substantially more than the 800 Mbytes per second of the host connection.

228. In an 8-bit architecture, twice as many instructions can be performed per second, but the communication registers are half the size, so the aggregate bandwidth of the communication registers of an 8-bit KPROC array is the same as Schmidt-2000’s 16-bit implementation. As an N-KPROC array (with multiple times more than 1024 processors) would only increase the aggregate bandwidth of the plurality of processing element connections by increasing the number of

communication registers that can be read/written on each instruction cycle, the 8-bit N-KPROC array of the Schmidt-Kan coprocessor meets claim 11.

**F. Claim 12: “the computing chip further comprises a control unit connected to the processing element array, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the processing element array to cause the processing element array to operate according to the at least one instruction.”**

229. Claim 12 recites the same limitations as claim 2. As discussed above in §XI.B.2, an obvious implementation of the Schmidt-Kan coprocessor includes the 8-bit KPROC-chip with on-chip controller and cache discussed in §X.A in connection with the Schmidt combination (but with larger numbers of processors). The Schmidt-Kan coprocessor therefore meets each of the limitations of claim 12 for the same reasons the Schmidt combination meets claim 2 (see §X.B above).

**G. Claim 13: “the computing chip further comprises an instruction memory adapted to store the at least one instruction received from the host computer via the input-output unit, wherein the control unit is further adapted to retrieve the at least one instruction from the instruction memory.”**

230. Claim 13 recites the same limitations as claim 3. For the same reasons discussed in above in §XI.F (i.e., obvious Schmidt-Kan coprocessor implementations with on-chip controller and cache), the Schmidt-Kan coprocessor meets claim 13 for the same reasons the Schmidt combination meets claim 3 (see §XI.G above).

## **XII. GROUND 4: CLAIMS 16-17 ARE OBVIOUS OVER SCHMIDT-2000 IN VIEW OF SCHIMMLER-1996**

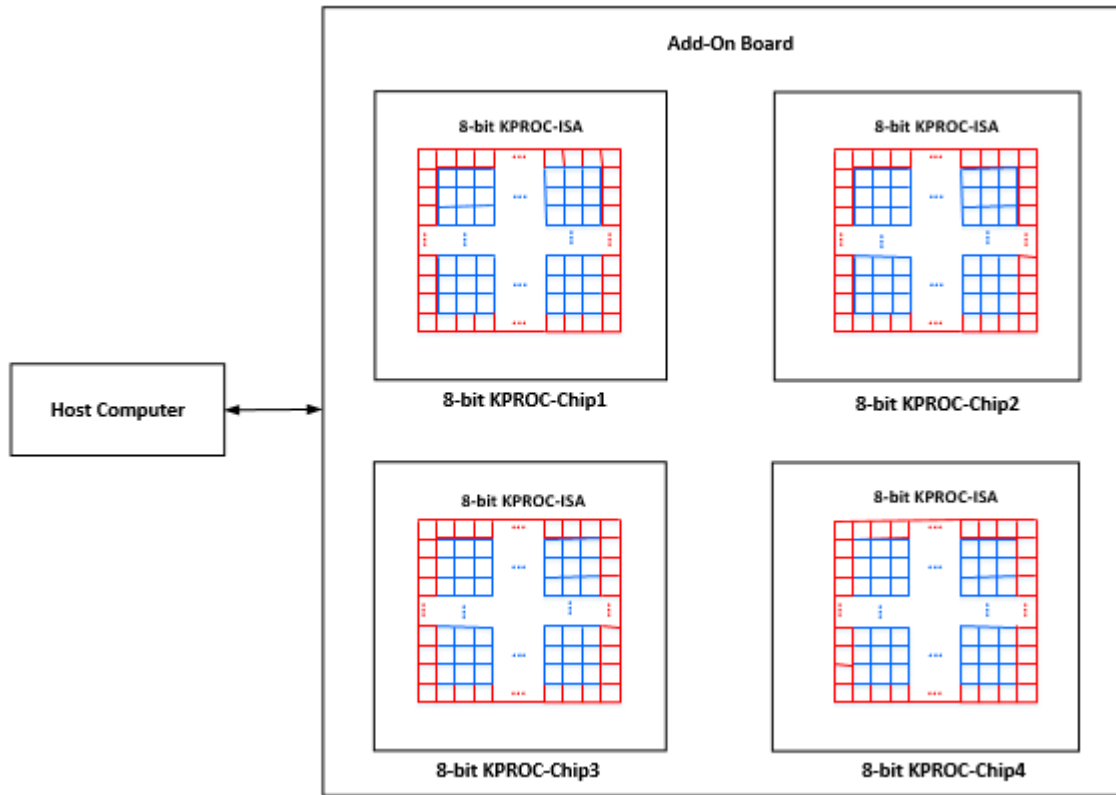
231. Schmidt-2000 discloses that the KPROC-chip integrates 1024 processors arranged in a 32x32 array and that the KPROC architecture's "modular organization" allows for "building *large arrays of many KPROC chips.*" The conventional and obvious way to build a large arrays from multiple KPROC chips would have been to tile and interconnect multiple KPROC-chips on a circuit board in a manner similar to the add-on board solution proposed in Schimmler-1996 (cited in Schmidt-2000 and authored by Schmidt-2000's co-author Schimmler) to obtain a 1024-processor array by assembling sixteen 64-processor chips on a circuit board. Schimmler-1996, 136-139. This add-on board configuration is also disclosed in Schimmler-1994 (EX1010). See Appendix, §II.A.3 for my opinion on the public accessibility of EX1010.

232. It would have been obvious to a POSA to similarly build large arrays from multiple KPROC-chips for use by the host computer as a coprocessor as disclosed in Schmidt-2000 by arranging and interconnecting the chips on circuit board in the conventional way disclosed in Schimmler-1996.

### **A. Add-On Board Implementation of Schmidt**

233. While any number of KPROC-chips may be used for a Schmidt Add-On Board, an example of an obvious and desirable implementation of a host computer using a Schmidt Add-On Board of four 8-bit KPROC-chips as a

coprocessor is illustrated below (see the discussion off the 8-bit KPROC-chip in §§VIII.A.1-VIII.A.2 above).



234. To perform I/O between the host processor and the 8-bit KPROC-chips, it would have been conventional, obvious, and desirable to connect the host computer to the board using conventional I/O interconnect technology and route I/O via circuitry printed on the circuit board to the I/O pins of each 8-bit KPROC-chip. Similarly, to implement inter-chip communication between array processors, it would have been conventional, obvious, and desirable to use each 8-bit KPROC-chip's I/O unit that handles other data exchange with other external components—

e.g., the I/O unit that routes “off-chip communication [] between the host computer and the KPROC chip” (Schmidt-2000, 163).

235. As discussed in above in connection with limitation [1E] of claim 1 (“*input-output unit*”), the registers R47-R63 of each processor and its external connections (e.g., the obvious use of the global data bus) handle I/O between the host computer and the processors of the KPROC array. It would have been obvious and desirable to use this I/O unit to implement inter-chip communication between processor arrays on different 8-bit KPROC-chips to “build large arrays” as Schmidt-2000 discloses. Schmidt-2000, 163.

236. Another way to implement inter-chip communication is to wire edge-processors together via the I/O pins as disclosed in Schimmler-1994 that describes a similar add-on board having the same configuration as Schimmler-1996. Schimmler-1994, 488 (“The parallel unit is laid out as a 4x4 square of ISA chips comprising an 8x8 array of processors each. Inter-chip communication is again done across short wires between physically adjacent pins, thus keeping the restriction of local communication only.”).

237. However, with a larger array integrated on each KPROC chip (i.e., an array that is sixteen-time bigger than the 64-processor chips disclosed in Schimmler-94 and Schimmler-96, a POSA would have understood that implementing “interchip communication” by connecting processors on the edges of

the array via small wires connecting corresponding pins would exacerbate the “pin limitation” identified in Schmidt-2000. Schmidt, 176.

238. Thus, it would have been obvious and desirable to implement data exchange between the communication registers of corresponding edge processors on adjacent 8-bit KPROC-chips, and a POSA would have had a reasonable expectation of success. In particular, each processor’s communication register is connected to internal registers R0-47 which exchange data with registers R48-R63 that in turn connect to the global bus that routes I/O off-chip. Schmidt-2000, 164-165, Fig. 3.1. In this way, POSAs would have understood that inter-chip I/O between edge processors can be routed through the existing I/O framework component without having to dedicate limited I/O pins to direct links between inter-chip communication registers.

**B. Claim 16**

239. Claim 16 recites substantially the same computing system recited in claim 1—*i.e.*, a host computer and a computing chip comprising a plurality of interconnected processing elements with reduced-bitwidth multipliers. A first 8-bit KPROC-chip 1 on the Schmidt Add-On Board meets those limitation for the same reasons the 8-bit KPROC-chip meets the corresponding limitations as discussed above in the limitation-by-limitation analysis of claim 1.

240. Claim 16 further recites “*an external edge processing element external to the computing chip*” that comprises the same components as the processing elements on the “*computing chip*.” This “*external edge processing element*” is connected to an on-chip edge processing element via the on-chip “*input-output unit*” and an “*external input-output unit external to the computing chip*.”

241. As demonstrated below, the Schmidt Add-On Board meets these limitations for the reasons discussed below. The '616 patent does not disclose any of subject-matter of claim 16 pertaining to “external” components—it neither discloses an external processing element connected to an on-chip processing element, nor does it disclose an external input-output unit connected to an on-chip input-output unit (let alone an external processing element connected to an on-chip processing element via external and on-chip input-output units)—but merely discloses the well-known concept that “the physical implementation of the PEA 104 (e.g., a chip) could be replicated (e.g., tiled on a circuit board) to produce a larger PEA” disclosed in Schmidt-2000 and Schimmler-1996 a decade before. EX1001, 10:32-34; Schmidt-2000, 163; Schimmler-1996, 136-139; Schimmler-1994, 487-488.

## 1. [16PRE], [16A]-[16B]

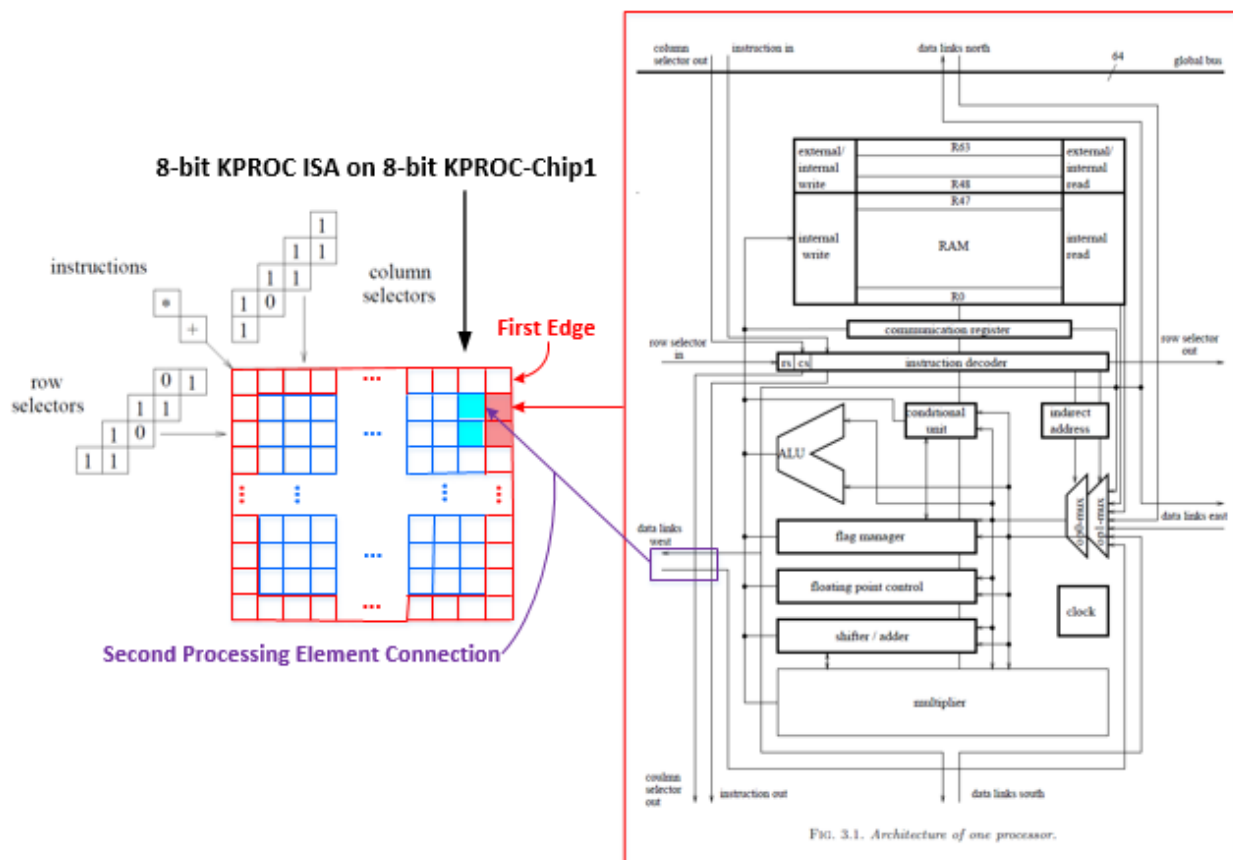
242. The preamble [16PRE] and the “*host computer*” and “*computing chip*” limitations [16A] and [16B] recite the identical subject matter as claim 1’s preamble [1PRE] and limitations [1A]-[1B]. The “host computer” (Schmidt-2000, 163) that utilizes the Schmidt-Add-On Board as a coprocessor meets [16A], a first 8-bit KPROC-chip on the board meets [16B], and all together meet the “*computing system*” of [16PRE] for the reasons discussed above in connection with these same limitations for claim 1.

## 2. [16C]-[16D]

243. The processing element array comprising edge and interior processing elements recited in [16C] and the processing element connections recited in [16D] recite the same language as [1C] and [1D] in claim 1. As discussed in above in §VIII.B.4 ([1C]), any of the processors in the first or last row or first or first or last column are edge processing elements positioned on at an edge of the array.

244. Fig. 2.1 of Schmidt-2000 (below left) is modified and annotated to show the right-most column of the 8-bit KPROC ISA—i.e., the “*processing element array*”—of the first 8-bit KPROC-chip that meets the “*first edge of the processing element array*” recited in [16C]. The processors shaded in **red** meet the claimed first and second “*edge processing element[s]*” the processors shaded in **blue** meet the claimed first and second “*interior processing element[s]*” meet

[16C], and the pair of wires shown in **purple** in annotated Fig. 3.1 below right, connecting the communication registers of the first red processor and the first blue processor, and the same connection for the second red processor and the second blue processor meet [16D] for the reasons discussed above in connection with limitations [1C] and [1D] in claim 1 for a different pair of edge and interior processors.



### 3. [16E], [16F] and [16G]

245. Limitations [16E]-[16G] of claim 16 recite the same limitations as [1E]-[1G] of claim 1 and the first 8-bit KPROC-chip on the Schmidt-Add-On

Board meets [16E]-[16G] for the same reason the 8-bit KPROC-chip meets [1E]-[1G] as discussed above in connection with these limitation for claim 1.

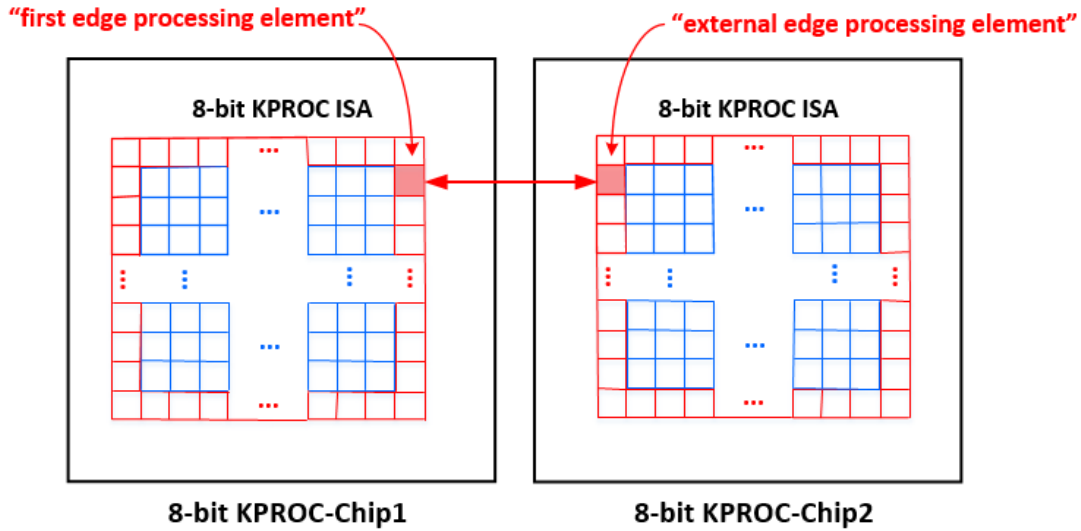
**4. [16H]: “a host connection at least partially connecting the input-output unit with the host computer”**

246. As discussed in above in connection with limitation [1H] (“*host connection*”) of claim 1, the host computer connects to the Schmidt-Add-On Board via the circuit board terminals, which route via the circuitry printed on the circuit board to the I/O pins of each 8-bit KPROC-Chip, which are in turn connected to the I/O unit on the respective chip. Thus, either the terminals on the circuit board or alternatively the I/O pins on the first 8-bit KPROC-chip meet [16H] because both at least partially connect the host computer with the I/O unit on the first 8-bit KPROC-chip.

**5. [16I], [16K]-[16M]: “an external edge processing element external to the computing chip” comprising “a fifth arithmetic unit” comprising a “multiplier circuit adapted to receive” limited-bitwidth inputs; and “a fifth memory local to the external edge processing element”**

247. In the Schmidt-Add-On Board discussed above, any edge processor on a second KPROC-chip meets [16I] because the edge processors on the second chip are external to the first chip (the claimed “*computing chip*”). In the drawing below, the processor on the 8-bit KPROC-Chip2 (shaded **red**) connected inter-chip to the edge processor of the 8-bit KPROC-Chip1 (also shaded red)—the “first edge

processing element”—via the respective I/O units of the above-described Schmidt-Add-On Board is such an “*external edge processing element*” that meets [16I].



248. This external edge processing element comprises the same components and has the same 8-bit architecture as the each of the other Schmidt-2000 processors in the KPROC array on each of the chips in the array. Thus, the external edge processing element has a “*fifth memory*” local to it [16K] and “*comprises a fifth arithmetic unit*” [16L] having a “*corresponding multiplier circuit*” adapted to receive as inputs two floating point values having “*mantissa[s] of width no more than 11 bits*” and “*exponent[s] of width at least 6 bits*” [16M] for the same reasons the discussed above in connection with limitations [1F]-[1G] and [1I] of claim 1 for the recited first-through-fourth processing elements.

**6. [16J] “an external input-output unit external to the computing chip;”**

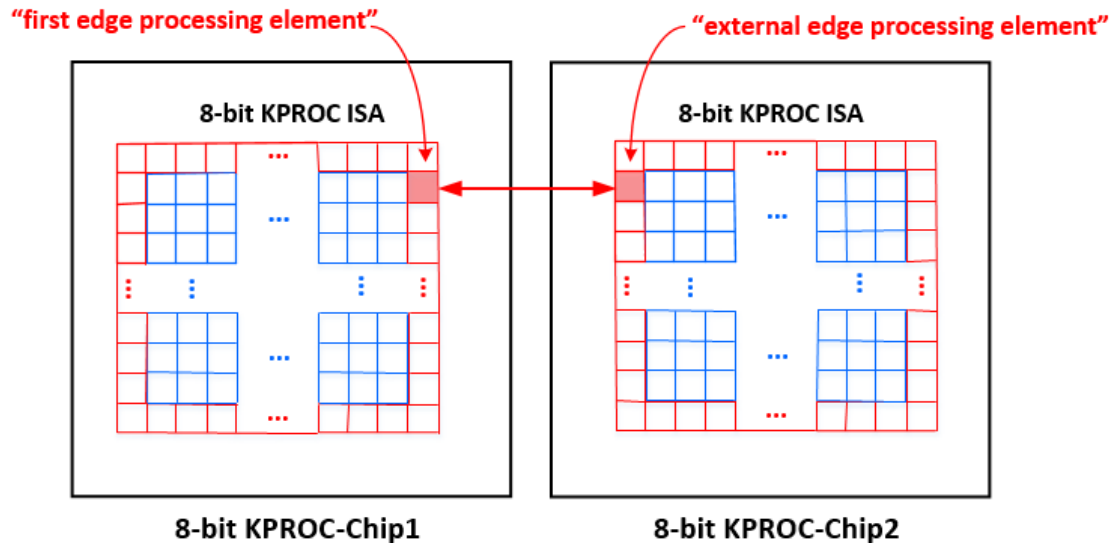
249. As discussed in above in the section describing the Schmidt-Add-On Board, it would have been obvious to use each KPROC-chip’s I/O unit (discussed above in §VIII.B.6 in connection with the “*input-output unit*” limitation [1E]) that routes other types of off-chip communication to also route inter-chip communication between the communication registers on corresponding edge processors of different KPROC-chips. Thus, this I/O unit on, for example, the 8-bit KPROC-chip2 meets [16J] because it is external to the 8-bit KPROC-chip1 illustrated in the drawing above.

**7. [16N] “wherein the first edge processing element is connected with the external edge processing element through the input-output unit and the external input-output unit.”**

250. As also discussed above in the section describing the Schmidt-Add-On Board, the I/O unit on each KPROC-chip routes inter-chip communication between corresponding edge processors on adjacent KPROC-chips, and therefore any edge processor on a KPROC-chip is connected to a corresponding edge processor on an adjacent KPROC-chip via its own I/O unit and the I/O unit on the adjacent chip, and therefore meets [16K].

251. As illustrated in the above-drawing (reproduced below), the edge processor on the 8-bit KPROC-Chip2 shaded **red** connects inter-chip to the edge

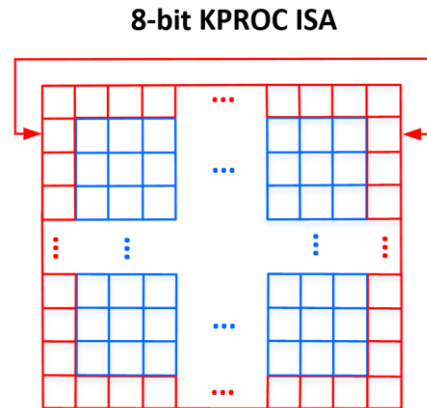
processor on the 8-bit KPROC-Chip1 (also shaded **red**)—i.e., the “*first edge processing element*” discussed in connection with limitations [16C]-[16D]—via the connection between the I/O unit on the 8-bit KPROC-Chip2 and the I/O on the 8-bit KPROC-Chip1, and therefore meets [16K].



**C. Claim 17: “the first edge processing element is connected with the external edge processing element using a torus interconnect.”**

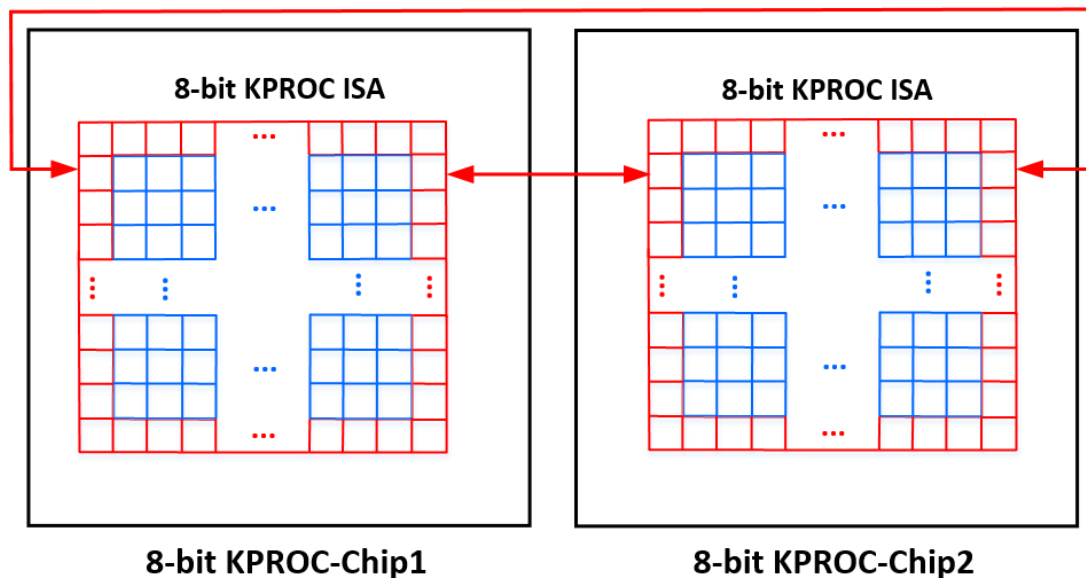
252. As the ’616 patent itself discloses, a torus interconnect was “well studied” connection scheme that connects “the outside edges” of an array of processing elements and the desirability of such an interconnect to allow communication between the first and last processors in a row were known. EX1001, 10:22-29. In Schmidt-2000’s design, a horizontal torus interconnect would be achieved by connecting the communication registers of the first and last

processors in a row, an example of which is illustrated below for the 8-bit KPROC ISA.

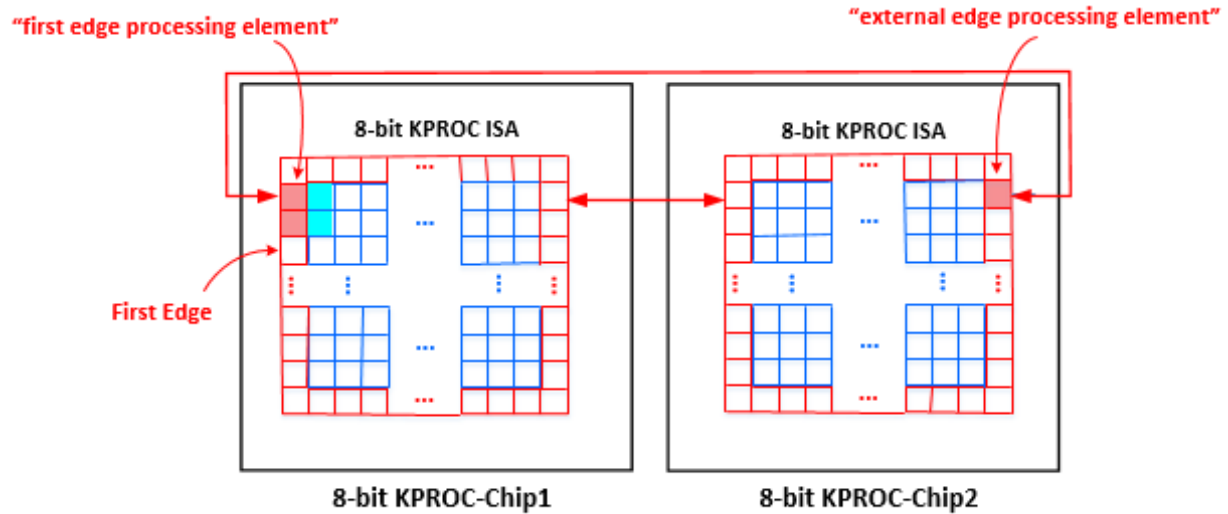


253. A POSA would have had good reason to connect the communication register of the first and last processor in each row of the KPROC ISA for the known benefits of providing this additional connection. Furthermore, for the specific design of the KPROC ISA, Schmidt-2000 discloses broadcast and ring-shift operations, and teaches that while only one instruction is needed to propagate a data item from left to right along a row of processors,  $2n$  instructions are required to send a data item from right to left, which operations should be avoided if possible. Schmidt-2000, 169. POSAs knew that by implementing a torus interconnect in the manner discussed above, sending a data item from right to left can be achieved by performing left-to-right shifts via the torus interconnect, reducing the number of instructions needed to propagate a data item from right to left.

254. In the Schmidt-Add-On Board discussed above, such an obvious and desirable torus interconnect would be formed by inter-chip connections between the last edge processor in each row in the eastern-most KPROC-chips in the chip array (e.g., 8-bit KPROC-chip2) to the first edge processor in each row of the western-most KPROC-chips in the chip array (e.g., 8-bit KPROC-chip1), as illustrated in the below drawing.



255. As discussed above in connection with limitation [1C] of claim 1 and limitation [16J], any Schmidt-2000 processor on an edge (other than corner-processors) and adjacent processor in the interior meet the recited edge/interior processing elements processing and any Schmidt-2000 edge processor on a different chip meets the claimed “external edge processing element.” Another example of such processing elements that meet each of the limitations in claim 16 are shown in the drawing below.



256. As shown above, the obvious and desirable use of a “torus interconnect” connects the “first edge processing element” and the “external edge processing element” via their respective I/O units discussed in connection with the Schmidt Add-On Board implementation above, and therefore meets each of the limitations in claim 17.

### **XIII. GROUND 5: CLAIMS 18-22 AND 24 ARE OBVIOUS OVER SCHMIDT-2000 IN VIEW OF SCHIMMLER-1996 AND KAN**

257. For the reasons discussed above in §X.A (Schmidt combination), §XI.B.2 (Schmidt-Kan coprocessor), it would have been obvious to integrate on-chip controller, cache, and MIMD-type unit on each 8-bit KPROC-chip on the Schmidt-Add-On Board described *supra* §VIII.A. This is true whether or not each chip is scaled to over 5000 PEs (which is not recited in claims 16-25).

258. This Schmidt-Kan Add-On Board meets claims 18-22 and 24 for the same reasons each Schmidt-Kan coprocessor meets the corresponding limitations

in other claims as in table below, wherein [18A]’s “*first additional processing elements*” are 8-bit Schmidt-2000 processors in the N-KPROC ISA, and [18C]’s “*second additional processing elements*” are Kan MIMD PEs.

| <b>Claim/Limitations:</b> | <b>Corresponding Claim/Limitations:</b> | <b>Addressed in Above Section:</b> |
|---------------------------|-----------------------------------------|------------------------------------|
| [18PRE], [18A]            | [7C], [7G]                              | §IX.B.4, §IX.B.8                   |
| [18B]                     | [7I]                                    | §IX.B.10                           |
| [18C], [18D], [18E]       | claim 8                                 | §XI.C                              |
| 19                        | 4, 10                                   | §VIII.C, XI.D                      |
| 20                        | 2, 12                                   | §X.B, XI.F                         |
| 21                        | 3, 13                                   | §X.C, XI.G                         |
| 22                        | 5                                       | §VIII.D                            |
| 24                        | 14                                      | §IX.D                              |

259. I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

260. I declare under penalty of perjury that the foregoing is true and correct.

Dated: 12/22/2022

A handwritten signature in black ink, appearing to be "A. O. M.", is written above a horizontal line.

## XIV. CLAIM LISTING

The following claim listing assigns element labels (e.g., [1PRE], [1A], etc.) to certain claims for convenience of reference.

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Claim 1</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| <b>[1PRE]</b> A computing system, comprising:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>[1A]</b> a host computer;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>[1B]</b> a computing chip comprising:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>[1C]</b> a processing element array comprising a first edge processing element positioned at a first edge of the processing element array, a second edge processing element positioned at the first edge of the processing element array, a first interior processing element positioned at a first location in an interior of the processing element array, and a second interior processing element positioned at a second location in the interior of the processing element array;                                                                                          |
| <b>[1D]</b> a first processing element connection connecting the first edge processing element with the first interior processing element; a second processing element connection connecting the second edge processing element with the second interior processing element;                                                                                                                                                                                                                                                                                                       |
| <b>[1E]</b> an input-output unit connected to the first edge processing element and the second edge processing element;                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>[1F]</b> a first memory local to the first edge processing element; a second memory local to the second edge processing element; a third memory local to the first interior processing element; and, a fourth memory local to the second interior processing element;                                                                                                                                                                                                                                                                                                           |
| <b>[1G]</b> wherein the first edge processing element comprises a first arithmetic unit; wherein the second edge processing element comprises a second arithmetic unit; wherein the first interior processing element comprises a third arithmetic unit; and wherein the second interior processing element comprises a fourth arithmetic unit; and,                                                                                                                                                                                                                               |
| <b>[1H]</b> a host connection at least partially connecting the input-output unit with the host computer;                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>[1I]</b> wherein the first, second, third and fourth arithmetic units each comprises a corresponding multiplier circuit adapted to receive as a first input to the corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits. |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Claim 2</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| The computing system of claim 1, wherein the computing chip further comprises a control unit connected to the processing element array, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the processing element array to cause the processing element array to operate according to the at least one instruction.                     |
| <b>Claim 3</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| The computing system of claim 2, wherein the computing chip further comprises an instruction memory adapted to store the at least one instruction received from the host computer via the input-output unit, wherein the control unit is further adapted to retrieve the at least one instruction from the instruction memory.                                                                                                                                              |
| <b>Claim 4</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| The computing system of claim 1, wherein said host computer is programmed to provide instructions to said computing chip that, when executed, cause said processing element array to perform an operation whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.                                                                                                                      |
| <b>Claim 5</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| The computing system of claim 1, wherein the width of each first binary mantissa is no more than 10 bits plus a first sign bit, and wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit.                                                                                                                                                                                                                                        |
| <b>Claim 6</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| The computing system of claim 5, wherein the width of each first binary exponent is at least 5 bits plus a third sign bit and wherein the width of each second binary exponent is at least 5 bits plus a fourth sign bit.                                                                                                                                                                                                                                                   |
| <b>Claim 7</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <b>[7PRE]</b> A computing system, comprising:                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <b>[7A]</b> a host computer;                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>[7B]</b> a computing chip comprising:                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>[7C]</b> a processing element array comprising a plurality of first processing elements, wherein the plurality of first processing elements is no less than 5000 in number, wherein each of a first subset of the plurality of first processing elements is positioned at a first edge of the processing element array, and wherein each of a second subset of the plurality of first processing elements is positioned in the interior of the processing element array; |
| <b>[7D]</b> an input-output unit connected to each of the first subset of the plurality of first processing elements;                                                                                                                                                                                                                                                                                                                                                       |

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| <b>[7E]</b> a plurality of processing element connections, each processing element connection connecting one of the plurality of first processing elements with another of the plurality of first processing elements, wherein each of the plurality of first processing elements is connected to at least one other of the plurality of first processing elements by at least one of the plurality of processing element connections;                                                                                                                                            |
| <b>[7F]</b> a plurality of memory units, wherein each of the plurality of first processing elements is associated with a corresponding one of the plurality of memory units, and wherein each of the plurality of memory units is local to its associated one of the plurality of first processing elements; and,                                                                                                                                                                                                                                                                 |
| <b>[7G]</b> a plurality of arithmetic units, wherein each of the plurality of first processing elements has positioned therein at least one of the plurality of arithmetic units; and,                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>[7H]</b> a host connection at least partially connecting the input-output unit with the host computer;                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>[7I]</b> wherein the plurality of arithmetic units each comprises a first corresponding multiplier circuit adapted to receive as a first input to the first corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the first corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits. |
| <b>Claim 8</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>[8PRE]</b> The computing system of claim 7,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <b>[8A]</b> wherein the computing chip further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;                                                                                                                                                                                                                            |
| <b>[8B]</b> wherein, other than the plurality of second processing elements, the computing chip has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and                                                                                                                                                                                                                                                                                          |
| <b>[8C]</b> wherein the plurality of first processing elements is greater in number, by at least 100, than the plurality of second processing elements.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Claim 9</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| The computing system of claim 7, wherein the plurality of memory units each comprises a corresponding register.                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

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| <b>Claim 10</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 8, wherein said host computer is programmed to provide instructions to said computing chip that, when executed, cause said processing element array to perform an operation whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.                                                                                                   |
| <b>Claim 11</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 8, wherein an aggregate maximum bandwidth of the plurality of processing element connections exceeds a maximum bandwidth of the host connection.                                                                                                                                                                                                                                                                           |
| <b>Claim 12</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 11, wherein the computing chip further comprises a control unit connected to the processing element array, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the processing element array to cause the processing element array to operate according to the at least one instruction. |
| <b>Claim 13</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 12, wherein the computing chip further comprises an instruction memory adapted to store the at least one instruction received from the host computer via the input-output unit, wherein the control unit is further adapted to retrieve the at least one instruction from the instruction memory.                                                                                                                          |
| <b>Claim 14</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 7, wherein the width of each first binary mantissa is no more than 10 bits plus a first sign bit, and wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit.                                                                                                                                                                                                                     |
| <b>Claim 15</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 14, wherein the width of each first binary exponent is at least 5 bits plus a third sign bit and wherein the width of each second binary exponent is at least 5 bits plus a fourth sign bit.                                                                                                                                                                                                                               |
| <b>Claim 16</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>[16PRE]</b> A computing system, comprising:                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>[16A]</b> a host computer;                                                                                                                                                                                                                                                                                                                                                                                                                            |
| <b>[16B]</b> a computing chip comprising:                                                                                                                                                                                                                                                                                                                                                                                                                |

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| <b>[16C]</b> a processing element array comprising a first edge processing element positioned at a first edge of the processing element array, a second edge processing element positioned at the first edge of the processing element array, a first interior processing element positioned at a first location in the interior of the processing element array, and a second interior processing element positioned at a second location in the interior of the processing element array;                                                                                                                       |
| <b>[16D]</b> a first processing element connection connecting the first edge processing element with the first interior processing element; a second processing element connection connecting the second edge processing element with the second interior processing element;                                                                                                                                                                                                                                                                                                                                     |
| <b>[16E]</b> an input-output unit connected to the first edge processing element and the second edge processing element;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <b>[16F]</b> a first memory local to the first edge processing element; a second memory local to the second edge processing element; a third memory local to the first interior processing element; and a fourth memory local to the second interior processing element;                                                                                                                                                                                                                                                                                                                                          |
| <b>[16G]</b> wherein the first edge processing element comprises a first arithmetic unit; wherein the second edge processing element comprises a second arithmetic unit; wherein the first interior processing element comprises a third arithmetic unit; and wherein the second interior processing element comprises a fourth arithmetic unit;                                                                                                                                                                                                                                                                  |
| <b>[16H]</b> a host connection at least partially connecting the input-output unit with the host computer;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>[16I]</b> an external edge processing element external to the computing chip;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <b>[16J]</b> an external input-output unit external to the computing chip; and,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <b>[16K]</b> a fifth memory local to the external edge processing element;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>[16L]</b> wherein the external edge processing element comprises a fifth arithmetic unit;                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <b>[16M]</b> wherein the first, second, third, fourth, and fifth arithmetic units each comprises a first corresponding multiplier circuit adapted to receive as a first input to the first corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the first corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits; and |
| <b>[16N]</b> wherein the first edge processing element is connected with the external edge processing element through the input-output unit and the external input-output unit.                                                                                                                                                                                                                                                                                                                                                                                                                                   |

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| <b>Claim 17</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| The computing system of claim 16, wherein the first edge processing element is connected with the external edge processing element using a torus interconnect.                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>Claim 18</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>[18PRE]</b> The computing system of claim 16,                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <b>[18A]</b> wherein the processing element array further comprises a plurality of first additional processing elements and a plurality of first additional arithmetic units, each of the plurality of first additional processing elements having positioned therein at least one of the plurality of first additional arithmetic units;                                                                                                                                                                                                                                                              |
| <b>[18B]</b> wherein the plurality of first additional arithmetic units each comprises a second corresponding multiplier circuit adapted to receive as a third input to the second corresponding multiplier circuit a third floating point value having a third binary mantissa of width no more than 11 bits and a third binary exponent of width at least 6 bits, and to receive as a fourth input to the second corresponding multiplier circuit a fourth floating point value having a fourth binary mantissa of width no more than 11 bits and a fourth binary exponent of width at least 6 bits; |
| <b>[18C]</b> wherein the computing chip further comprises a plurality of second additional processing elements, wherein the plurality of second additional processing elements each comprises a third corresponding multiplier circuit adapted to receive as inputs to the third corresponding multiplier circuit two floating point values each of width at least 32 bits;                                                                                                                                                                                                                            |
| <b>[18D]</b> wherein other than the second additional processing elements the computing chip has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and,                                                                                                                                                                                                                                                                                                                 |
| <b>[18E]</b> wherein the plurality of first additional processing elements is greater in number, by at least 100, than the plurality of second additional processing elements.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>Claim 19</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| The computing system of claim 18, wherein said host computer is programmed to provide instructions to said computing chip that, when executed, cause said processing element array to perform an operation whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.                                                                                                                                                                                                                                                |

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| <b>Claim 20</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 18, wherein the computing chip further comprises a control unit connected to the processing element array, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the processing element array to cause the processing element array to operate according to the at least one instruction. |
| <b>Claim 21</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 20, wherein the computing chip further comprises an instruction memory adapted to store the at least one instruction received from the host computer via the input-output unit, wherein the control unit is further adapted to retrieve the at least one instruction from the instruction memory.                                                                                                                          |
| <b>Claim 22</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 16, wherein the width of each first binary mantissa is no more than 10 bits plus a first sign bit, and wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit.                                                                                                                                                                                                                    |
| <b>Claim 23</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 22, wherein the width of each first binary exponent is at least 5 bits plus a third sign bit and wherein the width of each second binary exponent is at least 5 bits plus a fourth sign bit.                                                                                                                                                                                                                               |
| <b>Claim 24</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 18, wherein the width of each first binary mantissa is no more than 10 bits plus a first sign bit, wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit, wherein the width of each third binary mantissa is no more than 10 bits plus a third sign bit, and wherein the width of each fourth binary mantissa is no more than 10 bits plus a fourth sign bit.                    |
| <b>Claim 25</b>                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| The computing system of claim 24, wherein the width of each first binary exponent is at least 5 bits plus a fifth sign bit, wherein the width of each second binary exponent is at least 5 bits plus a sixth sign bit, wherein the width of each third binary exponent is at least 5 bits plus a seventh sign bit, and wherein the width of each fourth binary exponent is at least 5 bits plus an eighth sign bit.                                      |

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1. I understand from counsel that a printed publication qualifies as publicly accessible as of the date it was disseminated or otherwise made available such that any member of the public interested in the subject matter could locate it through the exercise of reasonable diligence.

2. While I understand that the determination of public accessibility under the foregoing standard rests on a case-by-case analysis of the facts particular to an individual publication, I also understand that a printed publication is rendered “publicly accessible” if it is cataloged and indexed by a library such that a member of the public interested in the subject matter a could locate it exercising reasonable diligence (i.e., I understand that cataloging and indexing by a library in a manner that permits a member of the public interested in the subject matter to locate the publication is sufficient, though there are other ways that a printed publication may qualify as publicly accessible, such as being indexed and catalogued in an online database). One manner of sufficient indexing is indexing according to subject matter category. I understand that the cataloging and indexing by a single library of a single instance of a particular printed publication is sufficient, even if the single library is in a foreign country. I also understand that the cataloging and indexing of information that would guide a person interested in the relevant subject matter to the printed publication, such as the cataloging and indexing of an abstract

for the printed publication, is sufficient to render the printed publication publicly accessible.

3. I understand that a document may also be publicly accessible if it is catalogued and indexed in an online digital database such that a person interested in the relevant subject matter could locate the document in the database exercising reasonable diligence. For example, as Dr. Bolin discussed in paragraphs 17-18 of her declaration, the ACM Digital Library and IEEE Xplore are examples of digital databases that are well-regarded among the academic community and considered to be accurate and trustworthy sources of information regarding the scientific and academic publications catalogued in those databases. As discuss in §§I.B-I.C below, I have personally used these databases and, in my opinion, POSAs would have been aware of these databases and would have used them to search for and retrieve publications in the art of computing and related fields at the time of the alleged invention.

4. I understand that routine business practices, such as general library cataloging and indexing practices, can be used to establish an approximate date on which a printed publication became publicly accessible. I further understand that the date on which digital databases, like IEEE Xplore and ACM Digital Library, indicate a document was published and/or added to the database can be used to establish a date on which the document became publicly accessible.

5. I agree with Dr. Bolin that POSAs would have been engaged in research, learning through study and practice in their field, and possibly through formal instruction, the bibliographic resources relevant to their research. *See* Bolin, ¶25. I also agree with Dr. Bolin that in the late-2000s POSAs would have had access to a vast array of long-established print and online resources providing indexing information, abstracts, and full-text services for publications in the field of computing. Bolin, ¶25.

6. I agree with Dr. Bolin that POSAs would have been able to locate the material discussed in Dr. Bolin's declaration as well as any additional documents I discuss in the sections below on their own or with the assistance of a research librarian, with relative ease using the tools and resources described in Dr. Bolin's declaration and in the sections below. *See* Bolin, ¶26.

## **I. OVERVIEW OF SEVERAL RESOURCES**

### **A. Internet Archive**

7. Exhibits 1029, 1031-1032, 1047-1048, and 1123 were provided by Nathaniel E Frank-White, the Records Request Processor at the Internet Archive, regarding various websites and files that were captured by the Internet Archive at the indicated dates and made browsable by the Internet Archive's Wayback Machine. The Internet Archive's Wayback Machine is well known to researchers and the general public as a service that provides archives of webpages as they

existed on dates in the past. I am personally familiar with the Internet Archive and its Wayback Machine from my own use of the service in my work and research. It is well known that the Internet Archive collects and archives captures of webpages using web crawlers, which are software programs that surf the Web, visiting websites and automatically storing copies of the webpages and other files represented by the URLs that the crawler visits. Crawlers are also used by Internet search engines (e.g., Google, Bing, etc.) to access webpages to be provided as search results, as is also well known to researchers and the general public. When the Internet Archive's crawlers visit a URL on a particular date, they store a copy of that webpage or file at the URL as it existed on that date. Users of the Wayback Machine can later access that archived capture of the URL to view and interact with the webpage or retrieve a file as it existed on that past date.

8. It is well known to users of the Internet Archive's Wayback Machine, and I am personally aware from my own use of the Wayback Machine, that the date on which an archived webpage was captured by the Internet Archive's crawlers can be observed in the URL that the Internet Archive assigns to the archived capture (what the Internet Archive calls an "extended URL"). When an archived capture of a webpage is viewed through the Wayback Machine on the Internet Archive's website (<http://web.archive.org>), the URL of the archived capture is <http://web.archive.org/web>, followed by numbers indicating the year,

month, day, and time at which the webpage was captured by the Internet Archive's crawlers, followed by the original URL of the archived webpage. For example, a Wayback Machine URL of <http://web.archive.org/web/20111231171057/http://www.uspto.gov:80/> is the Internet Archive's archived capture of the USPTO's homepage (<http://www.uspto.gov:80/>) captured on December 31, 2011 (2011/12/31), at 17:10:57 (5:10 p.m. and 57 seconds). This general practice of the Internet Archive for assigning URLs indicating the date and time of capture of an archived URL is well known to the Wayback Machine's users (including myself), and is also confirmed by the Frank-White declarations (*e.g.*, EX1029, ¶5).

## **B. IEEE and IEEE Xplore**

9. The Institute of Electrical and Electronics Engineers (IEEE) "is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity."<sup>1</sup> According to the IEEE official homepage, there are more than 409,000 IEEE members in more than 160 countries. The IEEE's website includes a digital database (currently called IEEE Xplore) for searching and retrieving copies of publications of the IEEE. The IEEE Xplore digital library currently has more than 5 million documents and more than 15

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<sup>1</sup> <https://www.ieee.org/about/at-a-glance.html> (last visited Dec. 19, 2022)

million downloads each month. I have personally used the IEEE Xplore digital database (and the IEEE's predecessor digital database) to retrieve copies of articles or presentations published by the IEEE and in my opinion POSA at the time of the alleged invention would have been aware of IEEE publications and could have retrieved an article or presentation published by the IEEE by exercising reasonable diligence (e.g., by obtaining a copy of an article from a library, by being a member of or subscriber of the IEEE publication, or by navigating to the IEEE's digital database).<sup>2</sup> *See also* Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”).

### **C. ACM and ACM Digital Library**

10. The Association for Computing Machinery (ACM) is “the world's largest educational and scientific computing society, delivers resources that advance computing as a science and a profession.”<sup>3</sup> According to the ACM's

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<sup>2</sup> *See, e.g.*, August 9, 2008 Wayback Machine archive of IEEE Xplore, at <https://web.archive.org/web/20080809051147/http://ieeexplore.ieee.org:80/Xplore/guesthome.jsp>

<sup>3</sup> <https://www.acm.org/about-acm> (last visited Dec. 19, 2022)

official homepage, there are “more than 100,000 members” of the ACM.<sup>4</sup> The ACM’s website links to a digital database (currently called the ACM Digital Library), which is “the world’s most comprehensive database of full-text articles and bibliographic literature covering computing and information technology. This renowned repository includes the complete collection of ACM publications plus an extended bibliographic database of core works in computing from scholarly publishers.”<sup>5</sup> I have personally used the ACM Digital Library to retrieve copies of articles or presentations published in journals in the field of computing and information technology and in my opinion POSA at the time of the alleged invention would have been aware of the ACM and the ACM Digital Library and could have retrieved an article or presentation published by the ACM or publishers indexed by the ACM Digital Library by exercising reasonable diligence (e.g., by obtaining a copy of an article from a library, by being a member of or subscriber of

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<sup>4</sup> <https://www.acm.org/about-acm/about-the-acm-organization> (last visited Dec. 19, 2022)

<sup>5</sup> <https://www.acm.org/publications/digital-library> (last visited Dec. 19, 2022); *see also* <https://dl.acm.org/> (last visited Dec. 19, 2022)

the publication, or by navigating to the ACM Digital Library).<sup>6</sup> *See also* Bolin, ¶17 (identifying ACM Digital Library as “a well-known and widely used resource for researchers, educators, and professionals in the field of computer science and related disciplines”).

## **II. OPINIONS REGARDING PUBLIC ACCESSIBILITY**

### **A. Public Accessibility of the Schmidt Articles (EX1007, EX1009-EX1011)**

#### **1. Public Accessibility of Schmidt-2000 (EX1007)**

11. EX1007 (which I refer to herein as “Schmidt-2000”) is titled “KPROC – An Instruction Systolic Architecture for Parallel Prefix Applications.” Based on the evidence I discuss below, it is my opinion that Schmidt-2000 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence.

12. According to the face of EX1007, Schmidt was published in the June 2000 issue of *Parallel and Distributed Computing Practices* (PDCP) by Nova Science Publishers, Inc. (Huntington, NY 2000). Page 163 of Schmidt-2000

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<sup>6</sup> *See, e.g.*, June 24, 2006 Wayback Machine archive of the ACM Digital Library, at <https://web.archive.org/web/20060624020808/http://portal.acm.org:80/dl.cfm>

similarly bears the text “© 2000 Nova Science Publishers, Inc.” indicating it was copyrighted and thus publicly accessible by the year 2000. According to Dr. Bolin, the PDCP journal has a creation date of December 9, 1997 in the OCLC MARC database and the University of Hong Kong has the PDCP journal in its collection and online catalog. *See* Bolin, ¶¶28-30; *see also id.* ¶¶7-15 (discussing MARC records). EX1007 is the copy of Schmidt-2000 that Dr. Bolin obtained from the University of Hong Kong Library. Bolin, ¶¶28-29. Based on this evidence, Dr. Bolin concluded that Schmidt-2000 was indexed, searchable and publicly accessible no later than early 2001. Bolin, ¶¶31-38. Based on the above evidence, I too conclude that Schmidt-2000 would have also been publicly accessible to a POSA exercising reasonable diligence at least by early 2001.

13. As I discuss below, a copy of Schmidt-2000 also appears to have been publicly accessible from a Schmidt-2000 author’s websites more than one year before the earliest possible priority date of the Asserted Patent. I understand from counsel that a POSA may use other publicly accessible information as “research aids” as a roadmap to locating additional prior art in the same or related field. Various publications publicly available before the earliest possible priority date of the Asserted Patent would have directed a POSA to Schmidt-2000. For example, one of Schmidt-2000’s authors – Dr. Bertil Schmidt – co-authored several articles published by Springer-Verlag and the IEEE with subject matter relating to the field

of the Asserted Patent, which would have directed a POSA exercising reasonable diligence to Schmidt-2000. *See also* §I.B above (discussing a POSA’s knowledge of the IEEE as a reputable compiler and publisher of scientific and technical books and journals); Bolin, ¶51 (identifying Springer-Verlag as “a well-known and respected publisher (founded in 1842) of academic journals and books”). Several of Dr. Schmidt’s IEEE- and Springer-published articles indicated that he was employed at the Nanyang Technological University (NTU) in Singapore at that time of their publication. *See, e.g.,*

<https://ieeexplore.ieee.org/document/1016589/authors#authors>;

<https://ieeexplore.ieee.org/document/1556805/authors#authors>;

<https://ieeexplore.ieee.org/document/1524318/authors#authors>. POSAs in the field of the challenged patent would have had reason to navigate to the website of an author of an article in a field relevant to the challenged patent, to find additional information about publications or, in some cases, copies of publications relating to that author’s teaching, research and research groups, projects and other academics and graduate students in the same and related academic department.

14. Page 33 of EX1031 is the Internet Archive’s archived capture of NTU’s homepage, <http://www.ntu.edu.sg/publicportal/>, as it existed on November 6, 2006, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20061106005508/http://www.ntu.edu.sg/publicportal>.

See EX1031, ¶¶5-6, p. 32. At the top of the NTU's homepage, there is a dropdown box for "Quick Links," one of which is to an "A-Z Website Directory." Selecting "A-Z Website Directory" from the dropdown box navigates to NTU's "Website Directory Service" webpage at

[https://wis.ntu.edu.sg/webexe88/owa/wdr\\_search.index\\_search](https://wis.ntu.edu.sg/webexe88/owa/wdr_search.index_search). Page 35 of

EX1031 is the Internet Archive's archived capture of that webpage as it existed on October 6, 2006, as reflected in the Internet Archive's extended URL:

[https://web.archive.org/web/20061006171248/https://wis.ntu.edu.sg/webexe88/owa/wdr\\_search.index\\_search](https://web.archive.org/web/20061006171248/https://wis.ntu.edu.sg/webexe88/owa/wdr_search.index_search). See EX1031, p. 34.

15. As shown on Page 35 of EX1031, NTU's Website Directory included hyperlinks to a list of NTU Staff, reachable by clicking on the letter that matched the first letter of the Staff's name. Clicking on "B" in the Staff row navigates to [https://wis.ntu.edu.sg/pls/webexe88/wdr\\_search.index\\_search?P\\_category=SF&P\\_index=B](https://wis.ntu.edu.sg/pls/webexe88/wdr_search.index_search?P_category=SF&P_index=B), which provides a list of "Staff websites [that] begin with letter B." Page 37 of EX1031 is the Internet Archive's archived capture of that webpage as it existed on October 6, 2006, as reflected in the Internet Archive's extended URL:

[https://web.archive.org/web/20061006173813/https://wis.ntu.edu.sg/pls/webexe88/wdr\\_search.index\\_search?P\\_category=SF&P\\_index=B](https://web.archive.org/web/20061006173813/https://wis.ntu.edu.sg/pls/webexe88/wdr_search.index_search?P_category=SF&P_index=B). See EX1031, p. 36.

16. As shown on Page 37 of EX1031, there was a hyperlink to the website of "Bertil Schmidt." Clicking on "Bertil Schmidt" navigates to

<http://www.ntu.edu.sg/home/asbschmidt/>, which was Dr. Schmidt's homepage hosted on NTU's website. Page 39 of EX1031 is the Internet Archive's archived capture of that webpage as it existed on October 9, 2006, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20061009222645/http://www.ntu.edu.sg/home/asbschmidt/>. See EX1031, p. 38.

17. As shown on Page 39 of EX1031, Dr. Schmidt's homepage included a link at the top of homepage to "Publications." Clicking on "Publications" navigates to a webpage listing various Books, Journal Papers, and Conferences Papers authored by Dr. Schmidt. Pages 56-58 of EX1031 contain the Internet Archive's archived capture of that webpage as it existed on September 24, 2006, as reflected in the Internet Archive's extended URL:

[https://web.archive.org/web/20060924015515fw\\_/http://www.ntu.edu.sg/home/asbschmidt/publications.htm](https://web.archive.org/web/20060924015515fw_/http://www.ntu.edu.sg/home/asbschmidt/publications.htm). See EX1031, p. 55.

18. As shown on Page 56 of EX1031, item number "17" is identified as "B. Schmidt, M. Schimmler, KPROC - An Instruction Systolic Architecture for Parallel Prefix Applications, Parallel and Distributed Computing Practices, Vol. 3, No. 2, 2000," which is the title and journal listed on the face of Schmidt-2000.

Clicking on the hyperlink for item number "17" navigates to

<http://www.ntu.edu.sg/home/asbschmidt/paper/PDCP00.htm>, which is a webpage

that includes a “Title,” “Abstract,” and “Reference” citation that matches what is shown on the face of Schmidt-2000 (EX1007). Page 45 of EX1031 is the Internet Archive’s archived capture of that webpage as it existed on October 26, 2004, as reflected in the Internet Archive’s extended URL:

[https://web.archive.org/web/20041026062341fw\\_/http://www.ntu.edu.sg/home/asbschmidt/paper/PDCP00.htm](https://web.archive.org/web/20041026062341fw_/http://www.ntu.edu.sg/home/asbschmidt/paper/PDCP00.htm). *See* EX1031, p. 44.

19. As shown on Page 45 of EX1031, there was a hyperlink to “File download” a pdf at the Internet Archive’s extended URL [https://web.archive.org/web/20041026062341fw\\_/http://www.ntu.edu.sg/home/asbschmidt/paper/KPROC2.pdf](https://web.archive.org/web/20041026062341fw_/http://www.ntu.edu.sg/home/asbschmidt/paper/KPROC2.pdf). This extended URL suggests that this webpage provided a link to download a PDF copy of Schmidt-2000 that the Internet Archive had archived on October 26, 2004. This extended URL, however, does not presently link to a PDF copy of Schmidt-2000 and instead navigates to a recent archive of NTU’s website, which indicates that the Internet Archive’s extended hyperlink to the Schmidt-2000 PDF is no longer valid. However, as discussed below, several other articles listed on the archived version of Dr. Schmidt’s webpage of “Journal Articles” are still archived by the Internet Archive from August 2007, which indicates to me that Schmidt-2000 likely would have also been available to download from Dr. Schmidt’s website, likely by October 26,

2004, or at least by August 2007, consistent with the Internet Archive's archived copies of other Schmidt-authored articles from Dr. Schmidt's website.

20. But even if Dr. Schmidt's hyperlink to download Schmidt-2000 had never been active, a POSA exercising reasonable diligence would have been able to obtain a copy of Schmidt-2000, or information about how to obtain a copy of Schmidt-2000, by contacting Dr. Schmidt directly. As shown on Page 39 of EX1031, Dr. Schmidt's homepage (archived on October 9, 2006) included an "Address," "Tel[ephone]" number, "Fax" number, and "E-mail" for contacting Dr. Schmidt. Thus, Dr. Schmidt's website provided a POSA several methods by which to contact Dr. Schmidt to ask for a copy of the Schmidt-2000 article, which I know from personal experience would have been a common courtesy of professors and researchers in this field. If Dr. Schmidt had been unable (or unwilling) to provide a copy of the Schmidt-2000 article, it reasonable to assume that Dr. Schmidt would have at least provided information about where to obtain a copy of Schmidt-2000 from the journal that published Schmidt (the PDCP) and/or the PDCP's publisher (Nova Science).

21. Based on the above evidence, I too conclude that Schmidt-2000 would have also been publicly accessible, via Dr. Schmidt's website, to a POSA exercising reasonable diligence by October 26, 2004, or at least by August 2007.

22. As I noted above in this section and discussed in §I.A, the Internet Archive maintains active archived links to copies of another paper co-authored by Dr. Schmidt, which indicates to me that the Schmidt-2000 article also would have been available for download at around the same time, consistent with the “File download” hyperlink I discussed above.

## **2. Public Accessibility of Schmidt-1999 (EX1009)**

23. EX1009 (which I refer to herein as “Schmidt-1999”) is titled “A Parallel Accelerator Architecture for Multimedia Video Compression.” Based on the evidence I discuss below, it is my opinion that Schmidt-1999 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence.

24. According to the face of EX1009, Schmidt-1999 was published in connection with the August/September 1999 5th International Euro-Par Conference in Toulouse, France by the publisher Springer-Verlag. Page 3 of Schmidt-1999 similarly bears the text “© Springer-Verlag Berlin Heidelberg 1999,” indicating it was copyrighted and thus publicly accessible by the year 1999. According to Dr. Bolin, the publisher Springer-Verlag “was and is a well-known and respected publisher (founded in 1842) of academic journals and books ...

[and] provides an online search tool (‘SpringerLink’)[ ] for providing researchers with access to millions of academic publications.” Bolin, ¶16.

25. According to Dr. Bolin, the proceedings of the Euro-Par’99 conference have a creation date of August 6, 1999 in the OCLC MARC database and the University of Wisconsin at Madison has a copy of Schmidt-1999. Bolin, ¶¶13-15; *see also* Bolin, ¶¶7-15 (discussing MARC records). EX1009 is the copy of Schmidt-1999 that Dr. Bolin obtained from the University of Wisconsin. Bolin, ¶12. Attachment 3c to Dr. Bolin’s declaration is a copy of Schmidt-1999 that Dr. Bolin obtained from the SpringerLink online database, which indicated a “first online” date for the article of January 1, 1999 and an online publication date of August 6, 1999. Bolin, ¶17. Based on this evidence, Dr. Bolin concluded that Schmidt-1999 was indexed, searchable and publicly accessible no later than early the end of 1999. Bolin, ¶18. Based on the above evidence, I too conclude that Schmidt-1999 would have been publicly accessible to a POSA exercising reasonable diligence at least by the end of 1999.

### **3. Public Accessibility of Schimmler-1994 (EX1010)**

26. EX1010 (which I refer to herein as “Schimmler-1994”) is titled “The Instruction Systolic Array – Implementation of a Low-Cost Parallel Architecture as Add-On Board for Personal Computers.” Based on the evidence I discuss below, it is my opinion that Schimmler-1994 is prior art to the challenged patent because it

was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence.

27. According to the face of EX1010, Schimmler-1994 was published in connection with the April 1994 High-Performance Computing and Networking (HPCN) conference in Munich, Germany by the publisher Springer-Verlag. Page 3 of Schimmler-1994 similarly bears the text “© Springer-Verlag Berlin Heidelberg 1994,” indicating it was copyrighted and thus publicly accessible by the year 1994. According to Dr. Bolin, the publisher Springer-Verlag “was and is a well-known and respected publisher (founded in 1842) of academic journals and books ... [and] provides an online search tool (‘SpringerLink’)[ ] for providing researchers with access to millions of academic publications.” Bolin, ¶16.

28. According to Dr. Bolin, the proceedings of the 1994 HPCN conference have a creation date of June 30, 1994 in the OCLC MARC database and the University of Wisconsin at Madison has a copy of Schimmler-1994. Bolin, ¶¶21-23; *see also* Bolin, ¶¶7-15 (discussing MARC records). EX1010 is the copy of Schimmler-1994 that Dr. Bolin obtained from the University of Wisconsin. Bolin, ¶20. According to Dr. Bolin, the Springer Link online database indicates that Schimmler-1994 has a “first online” date for the article of January 1, 2005 and an online publication date of May 26, 2005. Bolin, ¶25. Based on this evidence,

Dr. Bolin concluded that Schimmler-1994 was indexed, searchable and publicly accessible by May 26, 2005. Bolin, ¶18.

29. Based on the above evidence, I too conclude that Schimmler-1994 would have been publicly accessible to a POSA exercising reasonable diligence at least by May 26, 2005.

#### **4. Public Accessibility of Schimmler-1996 (EX1011)**

30. EX1011 (which I refer to herein as “Schimmler-1996”) is titled “The Instruction Systolic Array in Image Processing Applications.” Based on the evidence I discuss below, it is my opinion that Schimmler-1996 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence.

31. According to the face of EX1011, Schimmler-1996 was published in connection with the June 10-12, 1996 Vision Systems: Sensors, Sensor Systems, and Components conference in Besancon, France by the publisher SPIE—The International Society for Optical Engineering, which is a well-known international technical society and respected publisher of engineering and scientific journals and proceedings. Bolin, ¶30. Page 3 of Schimmler-1996 similarly bears the text “Copyright © 1996, The Society of Photo-Optical Instrumentation Engineers,” indicating it was copyrighted and thus publicly accessible by the year 1996.

32. According to Dr. Bolin, the proceedings of the 1996 Vision Systems: Sensors, Sensor Systems, and Components conference have a creation date of May 16, 1996 in the OCLC MARC database and the University of Wisconsin at Madison has a copy of Schimmler-1996. Bolin, ¶¶28-30; *see also* Bolin, ¶¶7-15 (discussing MARC records). EX1011 is the copy of Schimmler-1996 that Dr. Bolin obtained from the University of Wisconsin. Bolin, ¶27. According to Dr. Bolin, the SPIE Digital Library indicates that Schimmler-1996 has a publication date of August 21, 1996. Bolin, ¶31. Based on this evidence, Dr. Bolin concluded that Schimmler-1996 was published at least by September 17, 1996. Bolin, ¶31.

33. Based on the above evidence, I too conclude that Schimmler-1996 would have been publicly accessible to a POSA exercising reasonable diligence at least by September 17, 1996.

**B. Public Accessibility of NTRS/ITRS Reports (EX1021-EX1027, EX1030)**

34. The International Technology Roadmap for Semiconductors (ITRS) is a document that outlines the expected future development of the semiconductor industry and incorporates the latest information and insights from the semiconductor industry when the roadmap is being updated. The ITRS was established to determine research needs for the semiconductor industry. Several times a year, teams of semiconductor professionals get together and establish capabilities and forecast research problems that needed addressing. Before the

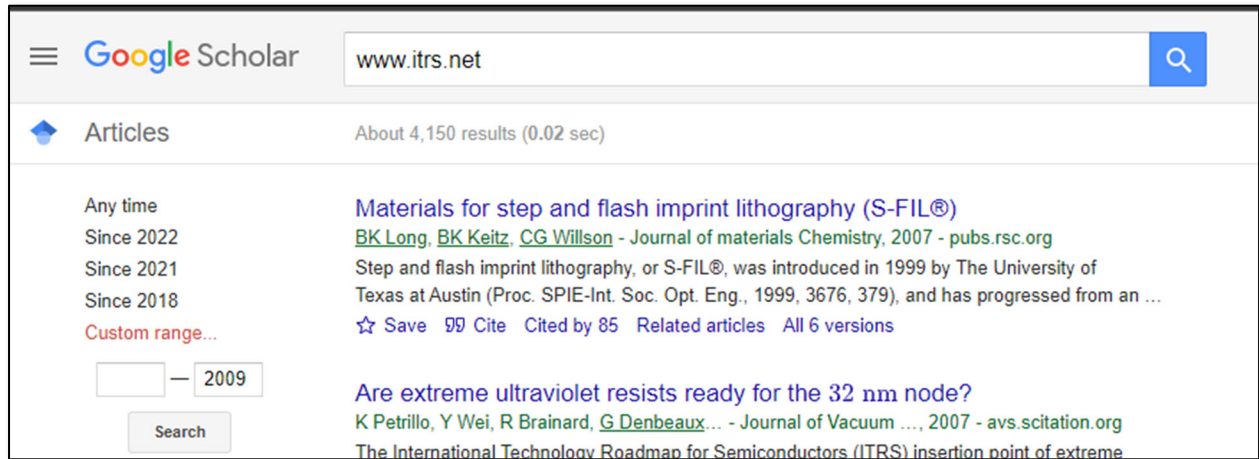
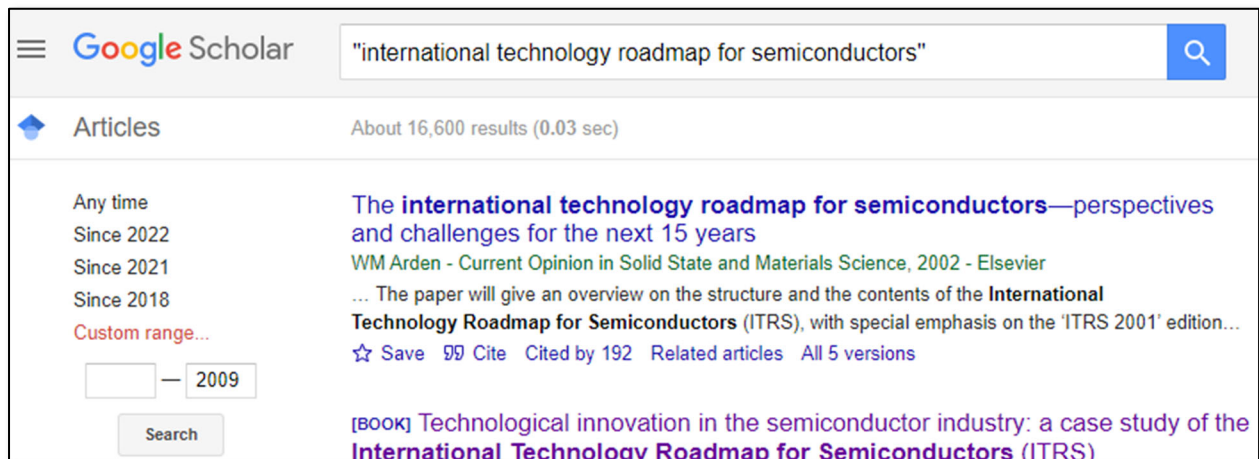
ITRS there was the National Technology Roadmap for Semiconductors (NTRS), which was initiated by the Semiconductor Industry Association (SIA), an association for the semiconductor industry, whose members include and have included leading companies in the semiconductor industry, such as Broadcom, IBM, Intel, Micron, Qualcomm, ARM, Samsung, TSMC, and others. In 1998, the NTRS evolved into the ITRS after the SIA invited semiconductor industry associations from around the world to contribute to and sponsor the roadmap moving forward. *See* EX1029, p. 94 (Foreward).

35. The ITRS roadmap has been updated every two years by a consortium of semiconductor industry organizations from around the world, like the SIA, European Semiconductor Industry Association, Korean Semiconductor Industry Association, Taiwan Semiconductor Industry Association, and Japan Electronics and Information Technology Industries Association. Though the ITRS roadmap has been published every two years, there have often been yearly updates. Each roadmap and update provides a long-term view of the key technologies and trends that are expected to drive the growth of the semiconductor industry, including areas such as device scaling, materials and processes, manufacturing, and design and architecture. The ITRS is an important tool for companies and researchers in the semiconductor industry, as it helps them to plan and prioritize their technology development efforts.

36. I personally served on the ITRS for several years in the mid-2010s, and was aware of and relied on the roadmaps throughout the 2000s. In my opinion, POSAs would have been aware of the NTRS and ITRS roadmaps that were published in the late-1990s through the 2000s and into the 2010s. The roadmaps would have been relied upon by POSAs at the time of the alleged invention for reliable data about both logic chip and memory chip development, which POSAs would have used to estimate the chip area and transistor density for the design of semiconductor devices like computing chips, for example. The roadmaps were published and widely distributed to POSAs throughout the world at no charge, and, as I discuss below, were available for download directly from the ITRS website, which POSAs would have been aware of and been able to locate with reasonable diligence.

37. For example, as shown below, a recent search of Google Scholar returned 4,150 articles from 2009 and earlier that included the ITRS's website – [www.itrs.net](http://www.itrs.net) – and 16,600 articles that included the text “international technology roadmap for semiconductors,” corroborating my opinion that POSAs would have

been well-aware of the ITRS website and roadmaps.<sup>7</sup> *See also* Bolin, ¶6 (identifying Google Scholar as a reliable repository of scholarly and research data).



<sup>7</sup> [https://scholar.google.com/schhp?hl=en&as\\_sdt=0,22](https://scholar.google.com/schhp?hl=en&as_sdt=0,22) (search for “[www.itrs.net](http://www.itrs.net)”; from filter tool select “Custom range...”; enter “2009” into right field for date range; click “Search”); *id.*, (same search pathway for “international technology roadmap for semiconductors”).

The ITRS roadmap is also referenced and/or cited in numerous U.S. patent application publications and issued patents from before the time of the alleged invention. Several specifically identify the ITRS's website as a source for retrieving copies of the roadmaps. *See, e.g.*, U.S. Patent Appl. Publ. No. 2003/0219157A1, [0184] (“Data of the chip areas and the technologies is referred from ITRS 2000[ ]Update Road Map (Reference: ‘ITRS 2000 Update: The International Technology Roadmap for Semiconductors 2000 Update’, [URL http://public.itrs.net/\(2000\)](http://public.itrs.net/(2000))).”); U.S. Patent Appl. Publ. No. US2003/0040130A1 [0041] (“As used herein, the term ““technology node”” is in accordance with the definition for Technology node provided in The International Technology Roadmap for Semiconductors (2000 Update), **published by the Semiconductor Industry Association (SIA), San Jose Calif.**; <http://public.itrs.net/>”).

38. Further corroborating my opinion that the roadmaps would have been widely distributed to POSAs, ITRS chairman Paolo Gargini, wrote in a 2000 IEEE publication, that “**It is the purpose of the 1999 ITRS, of the 2000 ITRS Update, and of future ITRS documents, to provide a set of up-to-date reference documents** of requirements, potential solutions, and their timing for the semiconductor industry. **These documents have already provided a common reference for international forums that have initiated discussions on cooperation among the leading silicon semiconductor manufacturers** and the

leading suppliers of equipment, materials, and software, **as well as researchers from university and government laboratories.**” EX1033, 4. Thus, it is my opinion that at the time of the alleged invention, POSAs would have been aware of and had reason to be familiar with the NTRS/ITRS roadmaps and would have been able to obtain any roadmap by exercising reasonable diligence, such as by navigating to the ITRS’s website.

39. A “Technology Node” in the roadmap “was defined as the achievement of an approximate 0.7x reduction per node.” EX1023 (ITRS 2000), 5. The node name generally tracks the DRAM minimum metal half-pitch or polysilicon half pitch. EX1023 (ITRS 2000), 31. The ITRS roadmaps typically also included information about the area required to fabricate a 4-transistor logic gate. *See, e.g.*, EX1028 (ITRS 2010 Executive Summary), 67. A POSA would understand that many useful gates require four transistors, such as NAND and NOR gates, and so the area required to fabricate a conventional 4-transistor logic gate would have been a useful metric for estimating the transistor density achievable with a particular technology node.

#### **1. Public Accessibility of NTRS 1997 (EX1021: “NTRS-1997”)**

40. The first page of EX1021 (which I refer to herein as “NTRS-1997”) is titled “The National Technology Roadmap for Semiconductors Technology Needs 1997 Edition,” by the Semiconductor Industry Association (SIA). As I discussed

in §II.B above, POSAs would have been aware of and had reason to be familiar with the NTRS/ITRS roadmaps and would have been able to obtain any roadmap by exercising reasonable diligence, such as by navigating to the ITRS's website.

41. Page 3 of EX1021 bears a copyright "© 1997 Semiconductor Industry Association," which indicates it was published in 1997. As discussed in §§II.B.2-II.B.7 below, the Internet Archive has various archived captures of the ITRS's website from before the year 2009. *See, e.g.*, EX1029, 6, 10. As I will discuss (§II.B.3 below), the Internet Archive captured the ITRS's "ITRS Edition Reports and Ordering" webpage as it existed on April 1, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080401032429/http://www.itrs.net:80/reports.html>.

*See also* EX1029, ¶¶5-7, p. 11. Page 12 of EX1029 is the Internet Archive's archived capture of that webpage. As shown at the bottom of that webpage, the ITRS disclosed that "[a] limited number of hard copy books are available for the 2005 ITRS **and previous roadmaps** (1994, **1997**, 1999, 2001, 2003)." As I discussed above (§II.B), I have personal knowledge that POSAs with a background or interest in the semiconductor industry, were familiar with the ITRS by the 2009-2010 timeframe. Such POSAs would have been interested in the ITRS roadmaps, which were accessible via the ITRS's website as demonstrated by the above-discussed archived webpage captures. In other words, a skilled artisan would have

known to navigate to the ITRS homepage and browsing the ITRS website would have known to navigate to the page of a particular roadmap or roadmap update, to retrieve documents on that page regarding a particular roadmap or roadmap update. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the semiconductor industry or interested in the roadmaps, could have located NTRS-1997 by searching the Web for keywords of interest such as “NTRS” or “National Technology Roadmap for Semiconductor,” which would be terms of interest to a POSA interested in the semiconductor industry and/or the roadmaps and updates. Based on the evidence I discussed above, NTRS-1997 was published and publicly accessible and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence by (at least) April 1, 2008.

## **2. Public Accessibility of ITRS 1999 (EX1022: “ITRS-1999”)**

42. The first page of EX1022 (which I refer to herein as “ITRS-1999”) is titled “International Technology Roadmap for Semiconductors 1999 Edition,” “Overall Roadmap Technology Characteristics & Glossary.” As I discussed in §II.B above, POSAs would have been aware of and had reason to be familiar with

the NTRS/ITRS roadmaps and would have been able to obtain any roadmap by exercising reasonable diligence, such as by navigating to the ITRS's website.

43. The Internet Archive has an archived capture of the ITRS's website, <http://public.itrs.net/>, as it existed on February 1, 2001, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20010201085500/http://public.itrs.net/>. As shown on the left side of that webpage is the text "Reports," which navigates to,

<http://public.itrs.net/Reports.htm>. The Internet Archive has an archived capture of that webpage as it existed on February 6, 2001, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20010206133820/http://public.itrs.net/Reports.htm>. As shown on that page, there is a hyperlink to "1999 Edition," which navigates to [http://public.itrs.net/files/1999\\_SIA\\_Roadmap/Home.htm](http://public.itrs.net/files/1999_SIA_Roadmap/Home.htm). The Internet Archive has an archived capture of that webpage as it existed on February 6, 2001, as reflected in the Internet Archive's extended URL:

[https://web.archive.org/web/20010206135413/http://public.itrs.net/files/1999\\_SIA\\_Roadmap/Home.htm](https://web.archive.org/web/20010206135413/http://public.itrs.net/files/1999_SIA_Roadmap/Home.htm). As shown on that page, there is a hyperlink to "Overall Technology Roadmap Characteristics and Glossary" (ORTC), which navigates to a PDF of the 1999 roadmap's ORTC, as it existed on June 4, 2001, as reflected in the Internet Archive's extended URL:

[https://web.archive.org/web/20010604100132/http://public.itrs.net/files/1999\\_SIA\\_Roadmap/ORTC.pdf](https://web.archive.org/web/20010604100132/http://public.itrs.net/files/1999_SIA_Roadmap/ORTC.pdf). That PDF is EX1022.

44. As I discussed above (§I above), I have personal knowledge that POSAs with a background or interest in the semiconductor industry, were familiar with the ITRS by the 2009-2010 timeframe. Such POSAs would have been interested in the ITRS roadmaps, which were accessible via the ITRS's website as demonstrated by the above-discussed archived webpage captures. In other words, a skilled artisan would have known to navigate to the ITRS homepage and browsing the ITRS website would have known to navigate to the page of a particular roadmap or roadmap update, to retrieve documents on that page regarding a particular roadmap or roadmap update. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I above), such that a POSA interested in the semiconductor industry or interested in the roadmaps, could have located ITRS-1999 by searching the Web for keywords of interest such as "ITRS" or "International Technology Roadmap for Semiconductor," which would be terms of interest to a POSA interested in the semiconductor industry and/or the roadmaps and updates. Based on the evidence I discussed above, ITRS-1999 (EX1022) was published and publicly accessible and

could have been located by any member of the public interested in the subject matter by exercising reasonable diligence by (at least) February 6, 2001.

**3. Public Accessibility of ITRS 2000 Update (EX1023: “ITRS-2000”)**

45. The first page of EX1023 (which I refer to herein as “ITRS-2000”) is titled “International Technology Roadmap for Semiconductors 2000 Update: Overall Roadmap Technology Characteristics.” As I discussed in §II.B above, POSAs would have been aware of and had reason to be familiar with the NTRS/ITRS roadmaps and would have been able to obtain any roadmap by exercising reasonable diligence, such as by navigating to the ITRS’s website.

46. Page 10 of EX1029 is the Internet Archive’s archived capture of the ITRS’s homepage, <http://www.itrs.net/home.html/>, as it existed on April 1, 2008. This is reflected in the Wayback Machine URL on page 9 of EX1029:

<https://web.archive.org/web/20080401032723/http://www.itrs.net/home.html>.

47. As shown on the left side of Page 10 of EX1029, the ITRS home page included a link to “ITRS Edition Reports and Ordering,” which navigates to <http://www.itrs.net/reports.html>. Page 12 of EX1029 is the Internet Archive’s archived capture of that webpage as it existed on April 1, 2008, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20080401032429/http://www.itrs.net:80/reports.html>.

*See also* EX1029, ¶¶5-7, p. 11.

48. As shown on the middle of Page 12 of EX1029, the ITRS home page included a link to the “2000 Update,” which navigates to <http://www.itrs.net/Links/2000UpdateFinal/2kUdFinal.html>. Page 14 of EX1029 is the Internet Archive’s archived capture of that webpage as it existed on April 20, 2008, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20080420120224/http://www.itrs.net/Links/2000UpdateFinal/2kUdFinal.html>. See also EX1029, ¶¶5-7, p. 13. EX1023 combines the portions of the 2000 Update retrievable from the hyperlinks respectively labeled (1) “Overall Roadmap Technology Characteristics (ORTC)” and (2) “PIDS” (i.e., Process Integration, Devices and Structures), as they existed on July 13, 2007, as reflected in their respective Internet Archive’s extended URLs: *e.g.*, <https://web.archive.org/web/20070713160806/http://www.itrs.net/Links/2000UpdateFinal/ORTC2000final.pdf>. See EX1029, ¶7, pp. 29-92 (Folders 1-2).

49. As I discussed above (§I above), I have personal knowledge that POSAs with a background or interest in the semiconductor industry, were familiar with the ITRS by the 2009-2010 timeframe. Such POSAs would have been interested in the ITRS roadmaps, which were accessible via the ITRS’s website as demonstrated by the above-discussed archived webpage captures. In other words, a skilled artisan would have known to navigate to the ITRS homepage and browsing the ITRS website would have known to navigate to the page of a particular

roadmap or roadmap update, to retrieve documents on that page regarding a particular roadmap or roadmap update. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I above), such that a POSA interested in the semiconductor industry or interested in the roadmaps, could have located ITRS-2000 by searching the Web for keywords of interest such as “ITRS” or “International Technology Roadmap for Semiconductor,” which would be terms of interest to a POSA interested in the semiconductor industry and/or the roadmaps and updates. Based on the evidence I discussed above, ITRS-2000 was published and publicly accessible and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence by (at least) April 20, 2008.

#### **4. Public Accessibility of ITRS 2001 (EX1030: “ITRS-2001”)**

50. The first page of EX1030 (which I refer to herein as “ITRS-2001”) is titled “International Technology Roadmap for Semiconductors 2001 Edition: Executive Summary.” As I discussed in §II.B above, POSAs would have been aware of and had reason to be familiar with the NTRS/ITRS roadmaps and would have been able to obtain any roadmap by exercising reasonable diligence, such as by navigating to the ITRS’s website.

51. As discussed (§II.B.3 above), the Internet Archive captured the ITRS's "ITRS Edition Reports and Ordering" webpage as it existed on April 1, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080401032429/http://www.itrs.net:80/reports.html>.

*See also* EX1029, ¶¶5-7, p. 11. Page 12 of EX1029 is the Internet Archive's archived capture of that webpage.

52. As shown on the middle of Page 12 of EX1029, the ITRS home page included a link to the "2001 Edition," which navigates to

<http://www.itrs.net/Links/2001ITRS/Home.htm>. The Internet Archive archived a

capture of that webpage as it existed on December 22, 2007, as reflected in the

Internet Archive's extended URL:

<https://web.archive.org/web/20071222013746/http://www.itrs.net/Links/2001ITRS>

[/Home.htm](http://www.itrs.net/Links/2001ITRS/Home.htm). *See also* EX1029, ¶¶5-7. As shown on that page, there is a hyperlink

to "Executive Summary," which navigates to a PDF of the 2001 roadmap's

Executive Summary, as it existed on July 11, 2007, as reflected in the Internet

Archive's extended URL:

<https://web.archive.org/web/20070711213510/http://www.itrs.net/Links/2001ITRS>

[/ExecSum.pdf](http://www.itrs.net/Links/2001ITRS/ExecSum.pdf). That PDF is EX1030.

53. As I discussed above (§II.B), I have personal knowledge that POSAs with a background or interest in the semiconductor industry, were familiar with the

ITRS by the 2009-2010 timeframe. Such POSAs would have been interested in the ITRS roadmaps, which were accessible via the ITRS's website as demonstrated by the above-discussed archived webpage captures. In other words, a skilled artisan would have known to navigate to the ITRS homepage and browsing the ITRS website would have known to navigate to the page of a particular roadmap or roadmap update, to retrieve documents on that page regarding a particular roadmap or roadmap update. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the semiconductor industry or interested in the roadmaps, could have located ITRS-2001 by searching the Web for keywords of interest such as "ITRS" or "International Technology Roadmap for Semiconductor," which would be terms of interest to a POSA interested in the semiconductor industry and/or the roadmaps and updates. Based on the evidence I discussed above, ITRS-2001 was published and publicly accessible and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence by (at least) July 11, 2007.

**5. Public Accessibility of ITRS 2002 Update (EX1024: "ITRS-2002")**

54. The first page of EX1024 (which I refer to herein as "ITRS-2002") is the "Foreward" to the "International Technology Roadmap for Semiconductors:

2002 Update.” As I discussed in §II.B above, POSAs would have been aware of and had reason to be familiar with the NTRS/ITRS roadmaps and would have been able to obtain any roadmap by exercising reasonable diligence, such as by navigating to the ITRS’s website.

55. Page 10 of EX1029 is the Internet Archive’s archived capture of the ITRS’s homepage, <http://www.itrs.net/home.html/>, as it existed on April 1, 2008. This is reflected in the Internet Archive’s extended URL on page 9 of EX1029: <https://web.archive.org/web/20080401032723/http://www.itrs.net/home.html>.

56. As shown on the left side of Page 10 of EX1029, the ITRS home page included a link to “ITRS Edition Reports and Ordering,” which navigates to <http://www.itrs.net/reports.html>. Page 12 of EX1029 is the Internet Archive’s archived capture of that webpage as it existed on April 1, 2008, as reflected in the Internet Archive’s extended URL. *See also* EX1029, ¶¶5-7, p. 11.

57. As shown on the middle of Page 12 of EX1029, the ITRS home page included a link to the “2002 Update,” which navigates to <http://www.itrs.net/Links/2002Update/Home.htm>. Page 16 of EX1029 is the Internet Archive’s archived capture of that webpage as it existed on January 26, 2008, as reflected in the Internet Archive’s extended URL. *See also* EX1029, ¶¶5-7, p. 15. EX1024 combines the portions of the 2002 Update retrievable from the hyperlinks respectively labeled (1) “Foreward,” (2) “Table of Contents,”

(3) “Overall Roadmap Technology Characteristics (ORTC),” and (4) “Process Integration, Devices & Structures (includes Emerging Research Devices),” as they existed on July 12, 2007, as reflected in their respective Internet Archive’s extended URLs. *See* EX1029, ¶7, pp. 94-154 (Folders 3-7)

58. As I discussed above (§I above), I have personal knowledge that POSAs with a background or interest in the semiconductor industry, were familiar with the ITRS by the 2009-2010 timeframe. Such POSAs would have been interested in the ITRS roadmaps, which were accessible via the ITRS’s website as demonstrated by the above-discussed archived webpage captures. In other words, a skilled artisan would have known to navigate to the ITRS homepage and browsing the ITRS website would have known to navigate to the page of a particular roadmap or roadmap update, to retrieve documents on that page regarding a particular roadmap or roadmap update. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I above), such that a POSA interested in the semiconductor industry or interested in the roadmaps, could have located ITRS-2002 by searching the Web for keywords of interest such as “ITRS” or “International Technology Roadmap for Semiconductor,” which would be terms of interest to a POSA interested in the semiconductor industry and/or the roadmaps and updates. Based on the evidence I

discussed above, ITRS-2002 was published and publicly accessible and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence by (at least) April 20, 2008.

**6. Public Accessibility of ITRS 2004 Update (EX1025: “ITRS-2004”)**

59. The first page of EX1025 (which I refer to herein as “ITRS-2004”) is titled “International Technology Roadmap for Semiconductors 2004 Update: Overview and Summaries.” As I discussed in §II.B above, POSAs would have been aware of and had reason to be familiar with the NTRS/ITRS roadmaps and would have been able to obtain any roadmap by exercising reasonable diligence, such as by navigating to the ITRS’s website.

60. Page 6 of EX1029 is the Internet Archive’s archived capture of the ITRS’s homepage, <http://public.itrs.net/>, as it existed on March 21, 2005. This is reflected in the Wayback Machine extended URL on page 5 of EX1029.

61. As shown on Page 6 of EX1029, the ITRS homepage included the following text – “The 2004 Update is now available here” – which ended in a hyperlink (“here”) that navigates to <http://www.itrs.net/Common/2004Update/2004Update.htm>. Page 8 of EX1029 is the Internet Archive’s archived capture of that webpage as it existed on April 3, 2005, as reflected in the Internet Archive’s extended URL. *See also* EX1029, ¶¶5-7.

62. As shown on Page 8 of EX1029, the ITRS “2004 Update Tables” included hyperlinks to download the 2004 Update to the 2003 roadmap. Page 8 of EX1029 is the Internet Archive’s archived capture of that webpage as it existed on April 3, 2005, as reflected in the Internet Archive’s extended URL. *See* EX1029, ¶¶5-6, p. 7. EX1025 combines the portions of the 2004 Update retrievable from the hyperlinks respectively labeled (1) Overview and Summaries, (2) Overall Roadmap Technology Characteristics (ORTC), (3) Design, and (4) Process Integration, Devices & Structures, as they existed on May 4, 2005, as reflected in their respective Internet Archive’s extended URLs. *See* EX1029, ¶7, pp. 156-320 (Folders 8-11).

63. As I discussed above (§II.B), I have personal knowledge that POSAs with a background or interest in the semiconductor industry, were familiar with the ITRS by the 2009-2010 timeframe. Such POSAs would have been interested in the ITRS roadmaps, which were accessible via the ITRS’s website as demonstrated by the above-discussed archived webpage captures. In other words, a skilled artisan would have known to navigate to the ITRS homepage and browsing the ITRS website would have known to navigate to the page of a particular roadmap or roadmap update, to retrieve documents on that page regarding a particular roadmap or roadmap update. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler

software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the semiconductor industry or interested in the roadmaps, could have located ITRS-2004 by searching the Web for keywords of interest such as “ITRS” or “International Technology Roadmap for Semiconductor,” which would be terms of interest to a POSA interested in the semiconductor industry and/or the roadmaps and updates. Based on the evidence I discussed above, ITRS-2004 was published and publicly accessible and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence by (at least) May 4, 2005.

## **7. Public Accessibility of ITRS 2007 (EX1026: “ITRS-2007”)**

64. The first page of EX1026 (which I refer to herein as “ITRS-2007”) is titled “International Technology Roadmap for Semiconductors 2007 Edition: Executive Summary.” As I discussed in §II.B above, POSAs would have been aware of and had reason to be familiar with the NTRS/ITRS roadmaps and would have been able to obtain any roadmap by exercising reasonable diligence, such as by navigating to the ITRS’s website.

65. Page 10 of EX1029 is the Internet Archive’s archived capture of the ITRS’s homepage, <http://www.itrs.net/home.html/>, as it existed on April 1, 2008. This is reflected in the Wayback Machine extended URL on page 9 of EX1029.

66. As shown on the left side of Page 10 of EX1029, the ITRS home page included a link to “ITRS Edition Reports and Ordering,” which navigates to <http://www.itrs.net/reports.html>. Page 12 of EX1029 is the Internet Archive’s archived capture of that webpage as it existed on April 1, 2008, as reflected in the Internet Archive’s extended URL. *See also* EX1029, ¶¶5-7, p.11.

67. As shown on the middle of Page 12 of EX1029, the ITRS home page included a link to the “2007 Edition,” which navigates to <http://www.itrs.net/Links/2007ITRS/Home2007.htm>. Page 18 of EX1029 is the Internet Archive’s archived capture of that webpage as it existed on April 22, 2008, as reflected in the Internet Archive’s extended URL. *See also* EX1029, ¶¶5-7, p.

17. EX1026 combines the portions of the 2007 Roadmap retrievable from the hyperlinks respectively labeled (1) “Executive Summary” (as it existed on November 23, 2009) and (2) “Process Integration, Devices & Structures” (as it existed on March 6, 2009), as reflected in their respective Internet Archive’s extended URLs. *See* EX1029, ¶7, pp. 322-487 (Folders 12-13).

68. As I discussed above (§II.B), I have personal knowledge that POSAs with a background or interest in the semiconductor industry, were familiar with the ITRS by the 2009-2010 timeframe. Such POSAs would have been interested in the ITRS roadmaps, which were accessible via the ITRS’s website as demonstrated by the above-discussed archived webpage captures. In other words, a skilled

artisan would have known to navigate to the ITRS homepage and browsing the ITRS website would have known to navigate to the page of a particular roadmap or roadmap update, to retrieve documents on that page regarding a particular roadmap or roadmap update. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.Aabove), such that a POSA interested in the semiconductor industry or interested in the roadmaps, could have located ITRS-2007 by searching the Web for keywords of interest such as “ITRS” or “International Technology Roadmap for Semiconductor,” which would be terms of interest to a POSA interested in the semiconductor industry and/or the roadmaps and updates. Based on the evidence I discussed above, ITRS-2007 was published and publicly accessible and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence by (at least) April 22, 2008.

#### **8. Public Accessibility of ITRS 2009 (EX1027: “ITRS-2009”)**

69. The first page of EX1027 (which I refer to herein as “ITRS-2009”) is titled “International Technology Roadmap for Semiconductors 2009 Edition: Executive Summary.” As I discussed in §II.B above, POSAs would have been aware of and had reason to be familiar with the NTRS/ITRS roadmaps and would

have been able to obtain any roadmap by exercising reasonable diligence, such as by navigating to the ITRS's website.

70. Page 20 of EX1029 is the Internet Archive's archived capture of the ITRS's homepage, <http://www.itrs.net/home.html>, as it existed on April 13, 2010. This is reflected in the Wayback Machine URL on page 19 of EX1029.

71. As shown on the middle of Page 20 of EX1029, the ITRS home page included a link to "The NEW **ITRS 2009 Edition** is now released!," which navigates to <http://www.itrs.net/Links/2009ITRS/Home2009.htm>. Page 22 of EX1029 is the Internet Archive's archived capture of that webpage as it existed on April 7, 2010, as reflected in the Internet Archive's extended URL. *See also* EX1029, ¶¶5-7, p. 21. EX1027 combines the portions of the 2009 Roadmap retrievable from the hyperlinks respectively labeled (1) "Executive Summary" and (2) "Process Integration, Devices & Structures," as they existed on March 31, 2010, as reflected in their respective Internet Archive's extended URLs. *See* EX1029, ¶7, pp. 489-611 (Folders 14-15)

72. As I discussed above (§II.B), I have personal knowledge that POSAs with a background or interest in the semiconductor industry, were familiar with the ITRS by the 2009-2010 timeframe. Such POSAs would have been interested in the ITRS roadmaps, which were accessible via the ITRS's website as demonstrated by the above-discussed archived webpage captures. In other words, a skilled

artisan would have known to navigate to the ITRS homepage and browsing the ITRS website would have known to navigate to the page of a particular roadmap or roadmap update, to retrieve documents on that page regarding a particular roadmap or roadmap update. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the semiconductor industry or interested in the roadmaps, could have located ITRS-2009 by searching the Web for keywords of interest such as “ITRS” or “International Technology Roadmap for Semiconductor,” which would be terms of interest to a POSA interested in the semiconductor industry and/or the roadmaps and updates. Based on the evidence I discussed above, ITRS-2009 was published and publicly accessible and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence by (at least) April 7, 2010.

**C. Public Accessibility of Additional Prior Art**

**1. Public Accessibility of EX1012 (“Yeh-ISCA07”)**

73. EX1012 (which I refer to herein as “Yeh-ISCA07”) is titled “ParallAX: An Architecture for Real-Time Physics.” Based on the evidence I discuss below, it is my opinion that Yeh-ISCA07 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date

for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence.

74. According to the face of EX1012, Yeh-ISCA07 was “[p]ublished by the Association for Computing Machinery” (ACM) in the May 2007 issue of Computer Architecture News, in connection with the Proceedings of the 34<sup>th</sup> International Symposium on Computer Architecture (ISCA’07). *See also* §I.C above (discussing a POSA’s knowledge of the ACM as a reputable compiler and publisher of scientific and technical books and journals). I am personally familiar with ISCA conferences, which are and have been since before the alleged invention date one of the premier conferences on computer architecture. Page 232 of EX1012 similarly bears the text “Copyright 2007 ACM,” indicating it was copyrighted and thus publicly accessible in the year 2007. According to Dr. Bolin, the ACM Digital Library database indicates Yeh-ISCA07 was published on June 9, 2007. Based on this evidence, Dr. Bolin concluded that Yeh-ISCA07 was indexed, searchable and publicly accessible no later than June 2007. Bolin, ¶¶68-73. Based on the above evidence, I too conclude that Yeh-ISCA07 would have been publicly accessible to a POSA exercising reasonable diligence by June 2007.

75. As I discuss below, a copy of Yeh-ISCA07 was also publicly accessible from one of the author’s websites more than one year before the earliest possible priority date of the Asserted Patent. I understand from counsel that a

POSA may use other publicly accessible prior art as “research aids” that provide a roadmap to locating additional prior art in the same or related field. Before 2008, I was personally aware of Dr. Glenn Reinman – a Yeh-ISCA07 co-author – as a well-known, reputable researcher in the field of parallel computing architectures. In my opinion, a POSA would have also been aware of Dr. Reinman and his research group at UCLA and thus would have had reason to go UCLA’s homepage and navigate to the homepages of professors and graduate students associated with Dr. Reinman’s research. *See* Yeh-ISCA07, p. 232 (identifying three of the four authors as being associated with the “Computer Science Department, UCLA” with “@cs.ucla.edu” email addresses).

76. Page 5 of EX1032 is the Internet Archive’s archived capture of UCLA’s homepage, <http://www.ucla.edu/>, as it existed on February 1, 2008, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20080201003048/http://www.ucla.edu/>. *See* EX1032, ¶¶5-6, p. 4. At the top of UCLA’s homepage, there is a hyperlink to “ACADEMICS,” which navigates to UCLA’s “ACADEMICS” webpage at <http://www.ucla.edu/academics.html>. Page 7 of EX1032 is the Internet Archive’s archived capture of that webpage as it existed on February 8, 2008, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20080208230223/http://www.ucla.edu/academics.html>

. See EX1032, ¶¶5-6, p. 6.

77. As shown on Page 7 of EX1032, UCLA's Academics webpage included hyperlinks to various "Professional Schools," including the "Henry Samueli School of Engineering and Applied Science," which navigates to <http://www.engineer.ucla.edu/>, which is the landing page for UCLA's School of Engineering. Page 9 of EX1032 is the Internet Archive's archived capture of that webpage as it existed on February 6, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080206081155/http://www.engineer.ucla.edu/>. See EX1032, ¶¶5-6, p. 8.

78. As shown on Page 9 of EX1032, UCLA's Engineering school webpage included a hyperlink "DEPARTMENTS," which navigates to [www.engineer.ucla.edu/departments/index.html](http://www.engineer.ucla.edu/departments/index.html). Page 11 of EX1032 is the Internet Archive's archived capture of that webpage as it existed on February 11, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080211124057/http://www.engineer.ucla.edu/departments/index.html>. See EX1032, ¶¶5-6, p. 10.

79. As shown on Page 11 of EX1032, the "Departments in the School" included a hyperlink to the "Computer Science" department, which navigates to

<http://www.cs.ucla.edu/>. Page 13 of EX1032 is the Internet Archive's archived capture of that webpage as it existed on February 8, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080208153715/http://www.cs.ucla.edu/>. See EX1032, ¶¶5-6, p. 12.

80. As shown on Page 13 of EX1032, the Computer Science Department included a hyperlink to “people” in the department, which navigates to <http://www.cs.ucla.edu/csd/people/index.html>. Page 15 of EX1032 is the Internet Archive's archived capture of that webpage as it existed on February 6, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080206005807/http://www.cs.ucla.edu/csd/people/index.html>. See EX1032, ¶¶5-6, p. 14.

81. As shown on Page 15 of EX1032, the “CSD People Pages” included a hyperlink to “Faculty” in the department, which navigates to <http://www.cs.ucla.edu/csd/people/faculty.html>. Pages 18-25 of EX1032 is the Internet Archive's archived capture of that webpage as it existed on February 14, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080214085121/http://www.cs.ucla.edu/csd/people/faculty.html>. See EX1032, ¶¶5-6, p. 17.

82. As shown on Page 20 of EX1032, the list of “Faculty” included a hyperlink for “Petros Faloutsos” – one of Yeh-ISCA07’s authors – which navigates to <http://www.cs.ucla.edu/~pfal/>. Page 17 of EX1032 is the Internet Archive’s archived capture of Dr. Faloutsos’s epage hosted at UCLA.edu as it existed on February 20, 2008, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20080220222723/http://www.cs.ucla.edu/~pfal/>. See EX1032, ¶¶5-6, p. 26.

83. As shown on Page 27 of EX1032, Dr. Faloutsos’ webpage included a hyperlink to “Publications,” which navigates to <http://www.cs.ucla.edu/~pfal/papers.html>. Page 29 of EX1032 is the Internet Archive’s archived capture of that webpage as it existed on February 22, 2008, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20080222132652/http://www.cs.ucla.edu/~pfal/papers.html>. See EX1032, ¶¶5-6, p. 28.

84. As shown on Page 29 of EX1032, item number “8” under “*Refereed Conferences*” is identified as ““ParallAX: An Architecture for Real-Time Physics’, Tom Yeh, Petros Faloutsos, Sanjay Patel, Glenn Reinman, in 34th Annual International Symposium on Computer Architecture, pp. 232-243, June 2007,” which is the title and conference identified on the face of Yeh-ISCA07. At the end of item number “8” is a hyperlink to a “pdf.” Clicking on that hyperlink

downloads a PDF of Yeh-ISCA07 (EX1012) that is identical to Yeh-ISCA07 at EX1012. Pages 60-71 of EX1032 which is substantively identical to EX1012, is the Internet Archive's archived capture of the PDF as it existed on February 21, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080221202312/http://www.cs.ucla.edu/~pfal/papers/ISCA-07-ParallAX.pdf>. See EX1032, ¶¶5-6, p. 59.

85. Based on the above evidence, I too conclude that Yeh-ISCA07 would have also been publicly accessible, via Dr. Faloutsos' website, to a POSA exercising reasonable diligence by February 21, 2008.

## **2. Public Accessibility of EX1013 ("Yeh-Micro07")**

86. EX1013 is titled "The Art of Deception: Adaptive Precision Reduction for Area Efficient Physics Acceleration." Based on the evidence I discuss below, it is my opinion that Yeh-Micro07 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence.

87. According to the face of EX1013, Yeh-Micro07 was published by the "IEEE Computer Society" in connection with "The 40<sup>th</sup> Annual IEEE/ACM International Symposium on Microarchitecture" on December 1-5, 2007 in Chicago, Illinois, USA. See also §I.B above (discussing a POSA's knowledge of

the IEEE as a reputable compiler and publisher of scientific and technical books and journals). Page 2 of Yeh-Micro07 similarly bears the text “© 2007 IEEE,” indicating it was copyrighted and thus publicly accessible in the year 2007.

According to Dr. Bolin, the IEEE Xplore database indicates Yeh-Micro07 was added December 26, 2007. Based on this evidence, Dr. Bolin concluded that Yeh-Micro07 was indexed, searchable and publicly accessible no later than December 2007. Bolin, ¶¶75-80. Testimony from an IEEE representative demonstrates public accessibility of EX1013 no later than December 5, 2007. *See* EX1127, ¶¶6-11. Based on the above evidence, I too conclude that Yeh-Micro07 would have been publicly accessible to a POSA exercising reasonable diligence in December 2007.

88. My opinion that Yeh-Micro07 would have been publicly accessible to a POSA exercising ordinary is further corroborated by the fact that a copy of Yeh-Micro07 was available from Dr. Faloutsos’ website by at least early 2008, as I discuss below. As I discussed (§II.C.1 above), a POSA exercising reasonable diligence had reason to and could have navigated to Dr. Faloutsos’ homepage hosted on the UCLA website, as demonstrated by the Internet Archives archived captures on Pages 4-31 of EX1032.

89. As shown on Page 29 of EX1032, item number “2” under Dr. Faloutsos’ list of “*Refereed Conferences*” is identified as “The Art of Deception:

Adaptive Precision Reduction for Area Efficient Physics Acceleration’, Tom Yeh, Petros Faloutsos, Sanjay Patel, Milos Ercegovac, and Glenn Reinman, The 40th Annual International Symposium on Microarchitecture (MICRO), Dec 2007, to appear,” which is the title and conference identified on the face of Yeh-Micro07.

At the end of item number “2” is a hyperlink to a “pdf.” Clicking on that hyperlink downloads a PDF of Yeh-Micro07 (EX1013) that is identical to Yeh-Micro07 at EX1013. Pages 46-58 of EX1032, which is substantively identical to EX1013, is the Internet Archive’s archived capture of the PDF as it existed on February 21, 2008, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20080222132652/http://www.cs.ucla.edu/~pfal/papers/MICRO-07-art.pdf>.

90. Based on the above evidence, I too conclude that Yeh-Micro07 would have also been publicly accessible, via Dr. Faloutsos’ website, to a POSA exercising reasonable diligence by February 21, 2008.

### **3. Public Accessibility of EX1014 (“Yeh Fool Me Twice”)**

91. EX1014 is an article titled “Fool Me Twice: Exploring and Exploiting Error Tolerance in Physics-Based Animation.” Based on the evidence I discuss below, it is my opinion that EX1014 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged

patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence.

92. As discussed (§II.C.2 above), Yeh-Micro07 (EX1013) was published by the IEEE in 2007 and was also publicly accessible from Dr. Faloutsos' website by February 21, 2008. Reference [34] in Yeh-Micro07 is identified as an article by, among others, Dr. Faloutsos titled "Fool me twice: Exploring and exploiting error tolerance in physics-based animation," which is the title of EX1014. *See* Yeh-Micro07, p. 406. Yeh-Micro07's reference also indicates that a copy of the article was accessible from a webpage hosted at [www.cs.ucla.edu](http://www.cs.ucla.edu) (i.e., UCLA's Computer Science Department). Thus, a POSA interested in Yeh-Micro07 – published in the IEEE – and exercising reasonable diligence would have navigated to the website for UCLA's computer science department to retrieve a copy of EX1014 from the URL indicated in Yeh-Micro07 and, if not there, via the homepage of one of the other author's identified in Yeh-Micro07.

93. A copy of EX1014 was available from Dr. Faloutsos' website by at least early 2008. As I discussed (§II.C.1 above), a POSA exercising reasonable diligence had reason to and could have navigated to Dr. Faloutsos' homepage hosted on the UCLA website, as demonstrated by the Internet Archives archived captures on Pages 4-31 of EX1032. As shown on Page 29 of EX1032, item number "1" under "*Refereed Journals*" is identified as "Fool Me Twice:

Exploring and Exploiting Error Tolerance in Physics-Based Animation’, Tom Yeh, Sanjay Patel, Petros Faloutsos, Glenn Reinman, ACM Transactions on Graphics, accepted with revisions, 2007,” which is the title and journal identified on the face of EX1014. At the end of item number “1” is a hyperlink to a “pdf.” Clicking on that hyperlink downloads a PDF of the journal paper that is identical to EX1014. Pages 34-44 of EX1032, which has been excerpted as EX1014, is the Internet Archive’s archived capture of the PDF as it existed on February 21, 2008, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20080222132652/http://www.cs.ucla.edu/~pfal/papers/TOG-08-Fool.pdf>. Based on the above evidence, I too conclude that EX1014 was publicly accessible, via Dr. Faloutsos’ website, to a POSA exercising reasonable diligence by February 21, 2008.

#### **4. Public Accessibility of EX1016 (“Moore 1965”)**

94. EX1016 is titled “Cramming More Components onto Integrated Circuits.” As seen on the face of the document, EX1016 was published in the January 1998 edition of the Proceedings of the IEEE. *See also* EX1016, p. 3 (indicating this as Vol. 86, No. 1 of the proceedings of the IEEE “published monthly”). As I discussed above (§I.B), the IEEE is a well-known, reputable and widely used resources for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines. As shown on

Page 5 of EX1016, the article “Cramming More Components onto Integrated Circuits” by Gordon Moore (of Moore’s Law fame), was originally published on April 19, 1965 in the journal “Electronics.” IEEE Xplore indicates that Vol. 86, Issue 1 of the Proceedings of the IEEE, which republished Moore 1965, had a “Date of Publication” of “January 1998.”<sup>8</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”).

95. Based on the evidence above, it is my opinion that EX1017 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by January 1998.

#### **5. Public Accessibility of EX1017 (“Moore 1975”)**

96. EX1017 is titled “Progress in Digital Integrated Electronics.” As seen on the face of the document, EX1017 was printed in the September 2006 edition of the IEEE SSCS (Solid-State Circuits Society) Newsletter. EX1017 bears a “Copyright 1975 IEEE” based on the article’s original publication in the Technical

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<sup>8</sup> <https://ieeexplore.ieee.org/document/658762>

Digest, International Electron Devices Meeting. IEEE Xplore indicates that Vol. 11, Issue 3 of the IEEE Solid-State Circuits Society Newsletter, which republished Moore 1975, had a “Date of Publication” of “September 2006.”<sup>9</sup> *See* Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Based on the evidence above, it is my opinion that EX1017 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by September 2006.

#### **6. Public Accessibility of EX1018 (“Mendocino”)**

97. EX1018 is titled “Mendocino Improves Celeron.” According to the face of the document, EX1018 was published in Volume 12, No. 11 of Microprocessor Report (“MPR”) on August 24, 1998. I am personally familiar with MPR as a well-known, reputable newsletter in the microprocessor industry and in my opinion POSAs would have also been aware of MPR at the time of the alleged invention and would have considered MPR to be reputable source of information in the microprocessor industry. In the 2000s, MPR was widely

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<sup>9</sup> <https://ieeexplore.ieee.org/document/4804410>

distributed to POSAs interested in the microprocessor industry on or around the dates indicated on the face of an article published by Microprocessor Report.

98. The Internet Archive's Wayback Machine has several archives of the MPR's website from the 2000s. For example, the Internet Archive has an archive of that website as it existed on April 2, 2001, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20010402030508/http://mpronline.com/>. The MPR's main webpage had a search box in the upper lefthand, which would have allowed a user to keyword search the entire contents of the MPR website, including all articles published by MPR. As shown at the bottom of the April 2, 2001 archive of the MPR's website, there is a link to "Subscribe," which navigates to the "About Microprocessor Report" page as it existed on February 5, 2004, as reflected in the Internet Archive's extended URL:

[https://web.archive.org/web/20040205074721/http://www.mpronline.com/mpr\\_public/about.html](https://web.archive.org/web/20040205074721/http://www.mpronline.com/mpr_public/about.html). As shown on that page, any interested member of the public could subscribe to MPR to "access current articles and **an eight-year archive** at [www.MPRonline.com](http://www.MPRonline.com)."

99. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I

above), such that a POSA interested in the semiconductor industry or interested in the roadmaps, could have located EX1018 by searching the Web for keywords of interest such as “Microprocessor Report” or “Mendocino,” which would be terms of interest to a POSA interested in the semiconductor industry generally and/or information about Intel’s Mendocino processor specifically.

100. Based on the evidence I discussed above, it is my opinion that EX1018 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence by (at least) the 1999-2001 timeframe, but certainly no later than the 2004 timeframe from when archives of articles in Microprocessor Report could be obtained from MPRonline.com, as I discussed above.

## **7. Public Accessibility of EX1019 (“Sim”)**

101. EX1019 (which I refer to herein as “Sim”) is titled “MIMD–SIMD hybrid system—towards a new low cost parallel system.” As indicated on the face of EX1019, Sim was published in Volume 29 of the journal “Parallel Computing” in 2003. Parallel Computing “is an international journal presenting the practical use of parallel computer systems, including high performance architecture, system

software, programming systems and tools, and applications.”<sup>10</sup> I am personally aware of Parallel Computing as a widely distributed, reputable journal in the field of computing and thus, in my opinion, journal that POSAs interested in the field of computing in the 2000 timeframe had reason to review articles published in Parallel Computing.

102. The face of EX1019 bears “© 2002 Elsevier Science B.V.,” indicating it was published by Elsevier Science in 2002. Elsevier is “a Dutch academic publishing company specializing in scientific, technical, and medical content. Its products include journals such as The Lancet, Cell, the ScienceDirect collection of electronic journals.”<sup>11</sup> “Elsevier published more than 600,000 articles annually in over 2,700 journals; as of 2018 its archives contained over 17 million documents and 40,000 e-books, with over one billion annual downloads.”<sup>12</sup> Sim was also “Available online” from [www.sciencedirect.com](http://www.sciencedirect.com) on December 4, 2002, which also indicates Sim was published on pages 21-36 of Issue 1, Volume 29 of Parallel Computing.<sup>13</sup> ScienceDirect, which “launched in March 1997,” is “a website which

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<sup>10</sup> <https://www.sciencedirect.com/journal/parallel-computing>

<sup>11</sup> <https://en.wikipedia.org/wiki/Elsevier> (last visited Dec. 19, 2022)

<sup>12</sup> *Id.*

<sup>13</sup> <https://www.sciencedirect.com/science/article/abs/pii/S0167819102001825>

provides access to a large bibliographic database of scientific and medical publications of the Dutch publisher Elsevier. It hosts over 18 million pieces of content from more than 4,000 academic journals and 30,000 e-books of this publisher.”<sup>14</sup> I was personally aware of [www.sciencedirect.com](http://www.sciencedirect.com) in the 2000 timeframe as a reputable digital database for publications in the field of computing and, in my opinion, POSAs in the 2000 timeframe would have been aware of [www.sciencedirect.com](http://www.sciencedirect.com) as indexed, searchable, and publicly accessible source of publications in the field of computing.

103. Based on the evidence above and my understanding of the Parallel Computing journal and Science Direct website, it is my opinion that Sim is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence by December 4, 2002 (from ScienceDirect.com), but not later than 2003 (from Volume 29, Issue 1 of the journal “Parallel Computing”).

## **8. Public Accessibility of EX1020 (“Taveniku”)**

104. EX1020 (which I refer to herein as “Taveniku”) is titled “The VEGA Moderately Parallel MIMD, Moderately Parallel SIMD, Architecture for High

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<sup>14</sup> <https://en.wikipedia.org/wiki/ScienceDirect> (last visited Dec. 19, 2022)

Performance Array Signal Processing.” Page 226 of Taveniku bears a copyright “© 1998 IEEE,” which indicates it was published in 1998 by the IEEE. IEEE Xplore indicates that Taveniku was published by the IEEE in connection with a conference held on March 30, 1998 – April 3, 1998, and had a “Date Added to IEEE Xplore” of August 6, 2002 and had a “Print ISBN” number and “Print ISSN” number.<sup>15</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”).

105. Based on the above evidence and my understanding of the IEEE and IEEE Xplore, it is my opinion that EX1020 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by August 2002.

#### **9. Public Accessibility of EX1038 (“Altera Product Catalog”)**

106. EX1038 is titled “Altera Product Catalog” from Altera, which “was a manufacturer of programmable logic devices (PLDs) headquartered in San Jose, California” that “was founded in 1983 and acquired by Intel in 2015.”<sup>16</sup> As

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<sup>15</sup> <https://ieeexplore.ieee.org/document/669915>

<sup>16</sup> <https://en.wikipedia.org/wiki/Altera> (last visited Dec. 14, 2002)

corroborated by Intel's acquisition of Altera, Altera was one of the leading manufacturers of PLDs at the time of the alleged invention. For example, a recent search of Google Patents for US patents or patent applications filed before June 19, 2009 with the words "Altera" and "FPGA" returned 2,834 results:

The screenshot shows the Google Patents search interface. The search bar contains the query: ("Altera") ("FPGA") country:US before:filing:2009-06-19. The search results show approximately 2,834 results. The search terms are listed as "Altera" and "FPGA", both with options to remove or add synonyms. The search fields include Date (Filing), Inventor, Assignee, Patent Office (US), Language, Status, Type, and Litigation. The results list includes patent entries such as "Digital camera system f" (WO EP US • US9565419B2) and "Methods and apparatus" (US • US7454732B2).

Google Patents

("Altera") ("FPGA") country:US before:filing:2009-06-19

SEARCH TERMS ⓘ

"Altera" × or + Synonym

"FPGA" × or + Synonym

+ Synonym

SEARCH FIELDS

📅 Date · Filing ▾

YYYY-MM-DD — 2009-06-19

👤 + Inventor

🏢 + Assignee

Patent Office · US ▾ Language ▾

Status ▾ Type ▾

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× About 2,834 results

Sort by · Relevance ▾ Group by ▾

Results / page · 10 ▾

Digital camera system f

WO EP US • [US9565419B2](#) • Ari M

Priority 2007-04-13 • Filed 2008-0

32 is connected to the MEN F17

daughter card, which contains AI

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from the camera module 152

Methods and apparatus

...

US • [US7454732B2](#)

Priority 1999-05-17

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Programmable logic dev

WO US AU • [US773](#)

Priority 2002-07-12

Thus, POSAs interested in the field of computing exercising reasonable diligence had reason to navigate to Altera's website to review the information and documentation available there, such as white papers and press releases, available from Altera's website regarding Altera's products, research, and development.

107. Page 72 of EX1038 bears a "Copyright © 2008 Altera Corporation," which indicates it was published in 2008. The very bottom of page 72 states "June 2008," which is consistent with a 2008 Copyright date.

108. Page 112 of EX1048 is the Internet Archive's archived capture of Altera's homepage, <http://www.altera.com/>, as it existed on June 2, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080602092253/http://www.altera.com/>. *See*

EX1048, ¶¶5-6, p. 111. At the top of the Altera's homepage there is the text

"Products," which navigates to Altera's products webpage at

<http://www.altera.com/products/prd-index.html>. Page 110 of EX1048 is the

Internet Archive's archived capture of that webpage as it existed on June 2, 2008,

as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080602092611/http://www.altera.com/products/prd-index.html>. *See* EX1048, p. 109.

109. As shown on Page 110 of EX1048, there is the text "View All" next to the heading for Altera's "Devices," which navigates to Altera Devices webpage

at <http://www.altera.com/products/devices/dev-index.jsp>. Page 108 of EX1048 is the Internet Archive's archived capture of that webpage as it existed on May 29, 2008, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20080529214527/http://www.altera.com/products/devices/dev-index.jsp>. See EX1048, p. 107.

110. Near the bottom right of that page is a hyperlink with the text “***Product Catalog (PDF)***,” which I right clicked on to save the document at the link, which downloaded a PDF that was at the URL

<http://www.altera.com/literature/sg/product-catalog.pdf>. Pages 82-153 of EX1047 (which is EX1038) is the Internet Archive's capture of that PDF from December 20, 2008, as reflected in the Internet Archive's extended URL:  
<https://web.archive.org/web/20081220145857/http://www.altera.com:80/literature/sg/product-catalog.pdf>. See EX1047, p. 81.

## **10. Public Accessibility of EX1039 (“Intel-Itanium”)**

111. EX1039 (which I refer to herein as “Intel-Itanium”) is titled “A 65 nm 2-Billion Transistor Quad-Core Itanium Processor.” As indicated on the face of EX1039, Intel-Itanium was published by the IEEE in the IEEE Journal of Solid-State Circuits (Volume: 44, Issue: 1, January 2009). I have reviewed EX1039, which appears to be a library scan of a physical copy of the issue of the IEEE Journal of Solid-State Circuits that contained Stackhouse, which is listed in the

TOC on page 3 of EX1039. Page 2 of EX1039 bears a “Copyright © 2009 by The Institute of Electrical and Electronics Engineers, Inc.” and an “ISSN” number.

Pages 1 and 3 of EX1039 bear a stamp from the “Linda Hall Library.” Page 5 of Intel-Itanium bears a Copyright “© 2008 IEEE,” which indicates it was published in 2008. IEEE Xplore indicates that Intel-Itanium had a “Date of Publication” of December 30, 2008.<sup>17</sup> *See* Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Testimony from an IEEE representative demonstrates public accessibility of EX1039 no later than December 31, 2008. *See* EX1128, ¶¶6-11.

112. Based on the above evidence and my review of the indicia appearing on the Intel-Itanium document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Intel-Itanium is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by January 2009. *See also* Bolin, ¶¶101-105 (concluding that attachment 12b to her declaration, an IEEE conference paper about the Itanium Processor by several authors indicated on the

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<sup>17</sup> <https://ieeexplore.ieee.org/document/4735536>

face of EX1039, “was publicly accessible at least as of January 9, 2009 and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence, on their own or with the assistance of a research librarian”).

## **11. Public Accessibility of EX1040 (“Janakiraman”)**

113. EX1040 (which I refer to herein as “Janakiraman”) is titled “Performance Analysis of Intel® Pentium® M and Pentium 4 Processors.” As indicated on the face of EX1040, Janakiraman is a white paper by Dell System Performance Analysis and bears the date “July 2005.” Page 5 of EX1040 bears a copyright “© 2005 Dell Inc.,” indicating it was published in 2005. Dell was and still is a large developer and seller of computing devices, like personal computers and servers. In the mid-2000s, Dell had an active research and development group that produced various white papers in the field of computing that POSAs exercising reasonable diligence would have been aware of to learn about developments in the industry. *See, e.g.*, Page 12 of EX1048 (showing the Internet Archive’s archived capture of the “Innovation @ Dell” webpage under the Dell.com domain as it existed on February 3, 2007, as reflected in the Internet Archives extended URL:  
<https://web.archive.org/web/20070203155947/http://www.dell.com/content/topics/global.aspx/innovation/en/index?c=us&l=en&s=corp>).

114. Page 8 of EX1048 is the Internet Archive's archived capture of a web page under the Dell.com domain summarizing Janakiraman, [http://www.dell.com/content/topics/global.aspx/vectors/en/2005\\_p4\\_pentiumm?c=us&l=en&s=corp](http://www.dell.com/content/topics/global.aspx/vectors/en/2005_p4_pentiumm?c=us&l=en&s=corp), as it existed on September 6, 2007, as reflected in the Internet Archive's extended URL: [https://web.archive.org/web/20070906020846/http://www.dell.com/content/topics/global.aspx/vectors/en/2005\\_p4\\_pentiumm?c=us&l=en&s=corp](https://web.archive.org/web/20070906020846/http://www.dell.com/content/topics/global.aspx/vectors/en/2005_p4_pentiumm?c=us&l=en&s=corp). See EX1048, ¶¶5-6, p. 7. See also EX1048, pp. 9-16 (showing the Internet Archive's captures of Dell.com's homepage and webpages from which POSAs could navigate to EX1048, as they existed in February 2007, as reflected in the Internet Archive's extended URLs). On the right of the Dell.com webpage summarizing Janakiraman there is a hyperlink to "Download PDF," that the Internet Archived captured on February 5, 2007, as reflected in the Internet Archive's extended URL: [https://web.archive.org/web/20070205153105/http://www.dell.com/downloads/global/vectors/2005\\_p4\\_pentiumm.pdf](https://web.archive.org/web/20070205153105/http://www.dell.com/downloads/global/vectors/2005_p4_pentiumm.pdf). That PDF is EX1048. See EX1047, ¶¶5-6, pp. 60-65. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (see §I.A above), such that a POSA interested in the computing industry, could have located EX1048 by searching the Web for keywords of interest such as "Pentium 4," die size," and

”transistor process,” which are terms that appear in EX1048 and would be terms of interest to a POSA interested in the computing industry.

115. Based on the above evidence and my review of the indicia appearing on EX1048, it is my opinion that EX1048 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by February 2007.

## **12. Public Accessibility of EX1041 (“Radeon-5700”)**

116. EX1041 (which I refer to herein as the “Radeon-5700 article”) is an article from guru3d.com titled “Radeon HD Series 5700 features.” According to the face of EX1041, EX1041 was published on October 21, 2009 on the website guru3d.com, a website which has “well over 15 million pageviews monthly” and “is one of World’s leading Interactive Entertainment and PC Hardware fan sites.”<sup>18</sup> The site “provides up-to-date news on latest developments in the interactive entertainment industry and in-depth reviews and articles targeted at the PC enthusiast and gamer” and “covers the hottest hardware such as video cards, [and] mainboards.”<sup>19</sup> An article that published on December 1, 2008 in the “ACM

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<sup>18</sup> <https://www.guru3d.com/content-page/contact-us.html>

<sup>19</sup> *Id.*

Transactions on Graphics” regarding algorithm to exploit “the fine-grained parallelism of GPUs” cited an article from guru3d.com as a reference, demonstrating that guru3d.com was a reliable source of information in the computing industry that POSAs would have been aware of by the mid-2000s timeframe.<sup>20</sup> *See also* §I.C above (discussing ACM and ACM Digital Library).

117. Pages 120-127 of EX1048 is the Internet Archive’s archived capture of The Guru of 3D’s homepage, <https://www.guru3d.com>, as it existed on October 26, 2009, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20091026163855/https://www.guru3d.com/>. *See* EX1048, ¶¶5-6, p. 119. At the right of the guru3d.com homepage, there is the text “Quick article links,” which includes hyperlinked text that says “Radeon HD 5750 review (Crossfire)”, which navigates to guru3d.com’s review of the ATI Radeon HD 5750 GPU webpage at <http://www.guru3d.com/article/radeon-hd-5750-review-crossfire/>. Pages 117-118 of EX1048 is the Internet Archive’s archived capture of that webpage as it existed on October 25, 2009, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20091025050805/http://www.guru3d.com/article/rade>

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<sup>20</sup> <https://dl.acm.org/doi/abs/10.1145/1409060.1409079> (citing a product review hosted on Guru3D.com for a device in the computing industry)

[on-hd-5750-review-crossfire/](http://www.guru3d.com/article/radeon-hd-5750-review-crossfire/). See EX1048, p. 116. As shown near the top of that page there is a drop-down box to navigate to different portions of the review. Selecting the text “Radeon HD Series 5700 features” from the drop down list navigates to the webpage at <http://www.guru3d.com/article/radeon-hd-5750-review-crossfire/3>. Pages 13-14 of EX1047 (which are EX1041) is the Internet Archive’s archived capture of that webpage as it existed on September 26, 2009, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20090926023317/http://www.guru3d.com/article/radeon-hd-5870-review-test/3>. See EX1047, ¶¶5-6, p. 12.

118. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the computing industry and data about commercial GPUs, could have located EX1041 by searching the Web for keywords of interest such as “processing elements” and “GPU,” “process,” “transistors,” and “die size,” which are terms that appear in EX1041 and would be terms of interest to a POSA interested in the computing industry.

119. Based on the above evidence and my review of the indicia appearing on EX1041, it is my opinion that EX1041 was publicly accessible before the June 15, 2010 filing date for U.S. Appl. No. 12/816,201 (challenged patent, code (63))

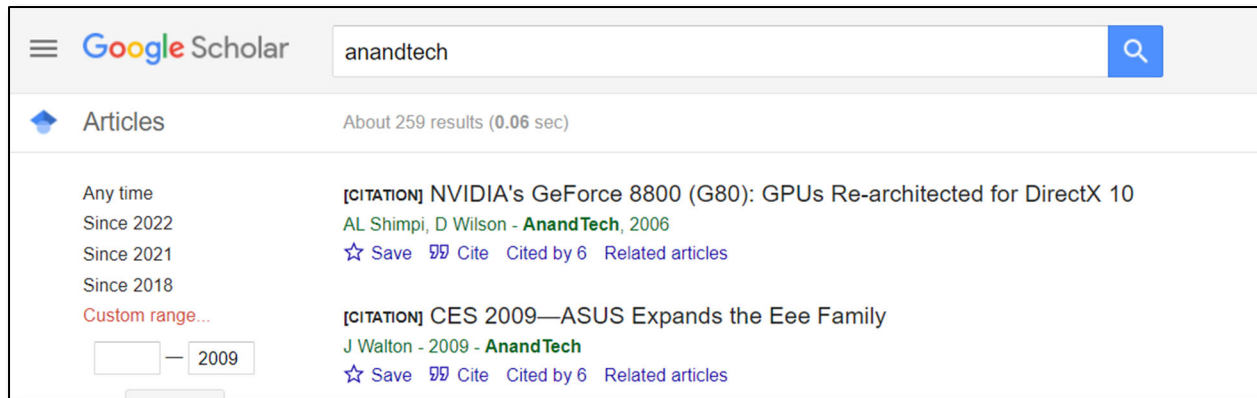
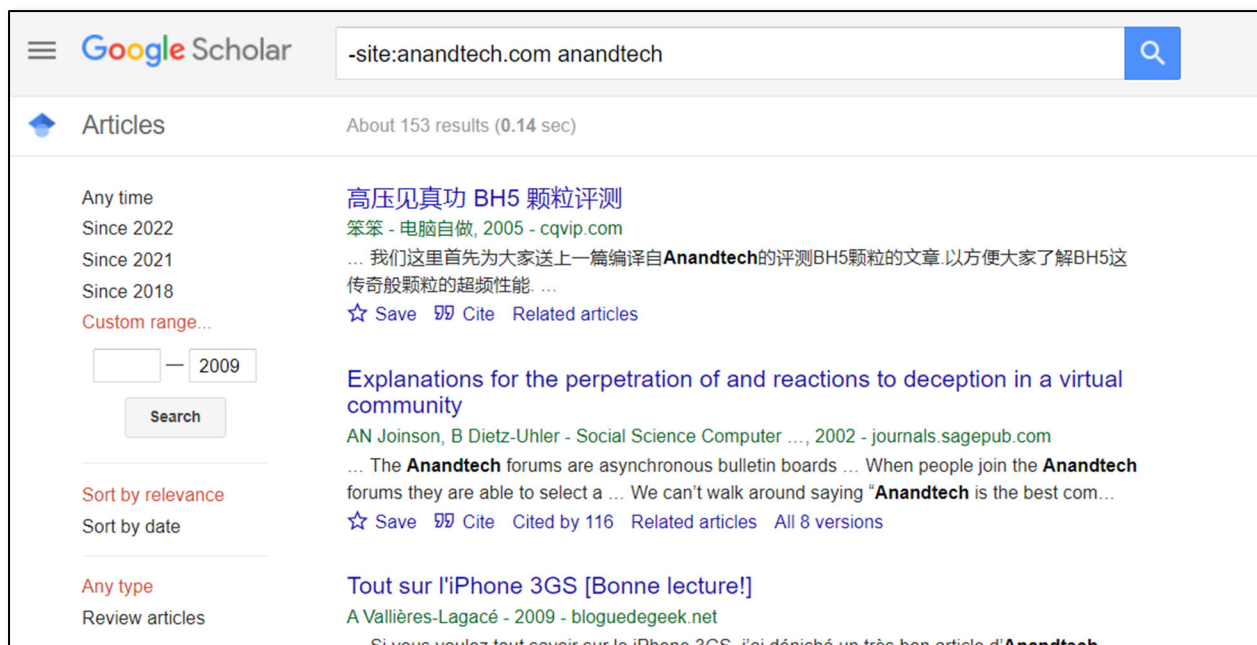
by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by October 26, 2009.

### **13. Public Accessibility of EX1042 (“Penryn”)**

120. EX1042 (which I refer to as “Penryn”) is an article from AnandTech.com titled “Intel Core 2 Extreme QX9650 - Penryn Ticks Ahead.” The face of EX1042 is dated “Oct[ober] 29, 2007,” indicating it was publicly accessible from AnandTech.com by that date. AnandTech is website that reviews computing products like GPUs and microprocessors that began in 1997 (though under different domain).<sup>21</sup> A recent search of Google Scholar returned 259 articles from 2009 and earlier that included “anandtech” and 153 articles hosted on sites that were not under the anandtech.com domain name, demonstrating that AnandTech was a well-known website for those interested in technology, such as the technology of computing devices. *See also* Bolin, ¶6 (identifying Google Scholar as a reliable repository of scholarly and research data).

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<sup>21</sup> <https://www.anandtech.com/home/about/>



121. Articles from AnandTech have also been cited in various publications from the ACM and IEEE, demonstrating that AnandTech was a reliable source of information in the computing industry that POSAs would have been aware of by

the mid-2000s timeframe.<sup>22</sup> *See also* U.S. Patent Publication Application 2008/0094427A1 (filed October 28, 2005), at [0055] (citing article from anandtech.com regarding a graphics control).

122. Pages 70-71 of EX1048 is the Internet Archive's archived capture of AnandTech's homepage, <https://www.anandtech.com>, as it existed on October 29, 2007, as reflected in the Internet Archive's extended URL:

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<sup>22</sup> *See, e.g.,*

<https://ieeexplore.ieee.org/abstract/document/1412184/references#references>

(articled added to IEEE Xplore on April 4, 2005; reference no. 15 from anandtech.com);

<https://ieeexplore.ieee.org/abstract/document/4523358/references#references>

(articled published by the IEEE on May 16, 2008; reference no. 15 from anandtech.com). *See, e.g.,*

<https://ieeexplore.ieee.org/abstract/document/1412184/references#references>

(articled added to IEEE Xplore on April 4, 2005; reference no. 15 from anandtech.com);

<https://ieeexplore.ieee.org/abstract/document/4523358/references#references>

(articled published by the IEEE on May 16, 2008; reference no. 15 from anandtech.com).

<https://web.archive.org/web/20071029173916/https://www.anandtech.com/>. *See*

EX1048, ¶¶5-6, p. 69. In the middle of AnandTech.com’s homepage there is hyperlinked text “Intel Core 2 Extreme QX9650 – Penryn Ticks Ahead,” which navigates to AnandTech’s review of Intel’s Penryn chip at

<http://www.anandtech.com/cpuchipsets/intel/showdoc.aspx?i=3137>. Pages 30-40

of EX1047 (which is EX1042) is the Internet Archive’s archived capture of that webpage as it existed on October 31, 2007, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20080602092611/http://www.altera.com/products/prd-index.html>.

<https://web.archive.org/web/20071031095146/http://www.anandtech.com/printarticle.aspx?i=3137>. *See* EX1047, p. 29.

123. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the computing industry and data about commercial GPUs and microprocessors, could have located EX1042 by searching the Web for keywords of interest such as “Intel” and “45nm,” “65nm,” “Intel,” “AMD,” and “transistors,” which are terms that appear in EX1042 and would be terms of interest to a POSA interested in the computing industry.

124. Based on the above evidence and my review of the indicia appearing on EX1041, it is my opinion that EX1041 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by October 2007.

**14. Public Accessibility of EX1043 (“TSMC 40nm Press Release 1”)**

125. EX1043 is a press release by TSMC titled “TSMC Ramps Most Advanced Available Process Technology to Volume Production” and appears to be a press release “Issued by: TSMC.” EX1043, 1. The face of EX1043 includes the date “November 17, 2008,” which indicates it was published by TSMC on November 17, 2008. I retrieved EX1043 from TSMC’s website at the URL <https://pr.tsmc.com/english/news/1526>. Because TSMC is one of the leading semiconductor manufacturers in the world and a publicly traded company, in my opinion the date identified on the face of a TSMC press release is a reliable indication of when the press release would have been publicly available from TSMC’s website. Based on the above evidence and my review of the indicia appearing on the face of EX1043, it is my opinion that EX1043 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or

otherwise made available to POSAs exercising reasonable diligence at least by November 17, 2008.

### **15. Public Accessibility of EX1044 (“CPU Cheatsheet”)**

126. EX1044 (which I refer to as “CPU Cheatsheet”) is an article from AnandTech.com titled “Updated CPU Cheatsheet - Seven Years of Covert CPU Operations.” The face of EX1044 is dated “Aug[ust] 28, 2004,” indicating it was publicly accessible from AnandTech.com by that date. As I discussed above (§II.C.13) Anandtech.com is a source of information for commercial GPUs and microprocessors that POSAs interested in the field of computing would have been aware of considered a reliable source of information regarding commercial chips.

127. Pages 73-74 of EX1048 is the Internet Archive’s archived capture of AnandTech’s homepage, <https://www.anandtech.com>, as it existed on August 29, 2004, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20040829013031/http://anandtech.com/>. See EX1048, ¶¶5-6, p. 72. Near the top of that webpage there is hyperlinked text “Updated CPU Cheatsheet - Seven Years of Covert CPU Operations,” which navigates to <http://www.anandtech.com/cpuchipsets/showdoc.aspx?i=2178>. Pages 51-52 of EX1047 is the Internet Archive’s archived capture of that page as it existed on September 9, 2004, as reflected in the Internet Archives extended URL:

<https://web.archive.org/web/20040909115936/http://www.anandtech.com/cpuchips/ets/showdoc.aspx?i=2178>.

128. Towards the bottom of page there is the text “Print this article.” Clicking on that navigates to a webpage containing the entire “Updated CPU Cheatsheet - Seven Years of Covert CPU Operations” article. Pages 42-49 of EX1047 (which is EX1044) is the Internet Archive’s archived capture of the entire article as it existed on January 22, 2005, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20050122063415/http://www.anandtech.com/printarticle.aspx?i=2178>. See EX1047, p. 41.

129. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the computing industry and data about commercial GPUs and microprocessors, could have located EX1042 by searching the Web for keywords of interest such as “Intel,” “AMD,” “die size,” and “transistor count,” which are terms that appear in EX1044 and would be terms of interest to a POSA interested in the computing industry.

130. Based on the above evidence and my review of the indicia appearing on EX1044, it is my opinion that EX1044 is prior art to the challenged patent

because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by January 2005.

## **16. Public Accessibility of EX1045 (“Natarajan”)**

131. EX1045 (which I refer to herein as “Natarajan”) is titled “A 32nm logic technology featuring 2nd-generation high-k + metal-gate transistors, enhanced channel strain and 0.171 $\mu$ m<sup>2</sup> SRAM cell size in a 291Mb array.” IEEE Xplore indicates that Natarajan was “Published in: 2008 IEEE International Electron Devices Meetings” by the IEEE in connection with a conference held on December 15-17, 2008, and had a “Date Added to IEEE Xplore” of February 27, 2009 and had an “ISBN” number and “Print ISSN” number.<sup>23</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Testimony from an IEEE representative demonstrates public accessibility of EX1045 no later than December 17, 2008. See EX1129, ¶¶6-11. Based on the above evidence and my understanding of the IEEE and IEEE Xplore, it is my opinion that Natarajan is prior art to the challenged patent because it was publicly accessible before the

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<sup>23</sup> <https://ieeexplore.ieee.org/document/4796777>

earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence by December 17, 2008, or at least no later than February 27, 2009.

#### **17. Public Accessibility of EX1052 (“Intel’s 32nm Update”)**

132. EX1052 is an article from AnandTech.com titled “Intel’s 32nm Update: The Follow-on to Core i7 and More.” The face of EX1052 is dated “Feb[ruary] 11, 2009,” indicating it was publicly accessible from AnandTech.com by that date. As I discussed above (§II.C.13) Anandtech.com is a source of information for commercial GPUs and microprocessors that POSAs interested in the field of computing would have been aware of considered a reliable source of information regarding commercial chips.

133. Pages 63-64 of EX1048 is the Internet Archive’s archived capture of AnandTech’s homepage, <https://www.anandtech.com>, as it existed on June 3, 2009 as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20090603130817/https://www.anandtech.com/>. *See*

EX1048, ¶¶5-6, p. 62. Near the top of that page there is a tab with the text “CPU/Chipset.” Clicking on that text navigates to AnandTech’s “CPU & Chipset Section” at <http://www.anandtech.com/cpuchipsets/>. The Internet Archive captured that page as it existed on May 31, 2009, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20090531115149/http://www.anandtech.com/cpuchipsets/>. See EX1048, ¶¶5-6; see also EX1048, pp. 56-59 (Internet Archives capture of that same webpage as it existed on June 17, 2009, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20090617064007/http://www.anandtech.com/cpuchipsets/default.aspx?manu=77&topicid=101>).

134. Towards the middle of the CPU & Chipset Section webpage there is hyperlinked text “Intel's 32nm Update: The Follow-on to Core i7 and More,” which navigates to <http://www.anandtech.com/cpuchipsets/showdoc.aspx?i=3513>. Pages 53-54 of EX1048 is the Internet Archive’s archived capture of that page as it existed on June 1, 2009, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20090601070325/http://www.anandtech.com/cpuchipsets/showdoc.aspx?i=3513>. See EX1048, ¶¶5-6, p. 52.

135. Towards the bottom of page there is the text “Print this article.” Clicking on that navigates to a webpage containing the entire “Intel’s 32nm Update: The Follow-on to Core i7 and More” article. Pages 21-28 of EX1047 (which is EX1052) is the Internet Archive’s archived capture of the entire article as it existed on December 31, 2009, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20091231063002/http://anandtech.com/printarticle.aspx?i=3513>. See EX1047, ¶¶5-6, p. 20.

136. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the computing industry and data about commercial GPUs and microprocessors, could have located EX1052 by searching the Web for keywords of interest such as “Intel,” “32nm process,” “CPUs,” and “dual-core,” which are terms that appear in EX1052 and would be terms of interest to a POSA interested in the computing industry.

137. Based on the above evidence and my review of the indicia appearing on EX1052, it is my opinion that EX1052 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by June 17, 2009 (as reflected in the Internet Archive’s extended URL for the main page of the “Intel’s 32nm Update: The Follow-on to Core i7 and More,” as discussed above). At the very latest, EX1052 was publicly accessible by December 31, 2009 (as reflected in the Internet Archive’s extended URL for printing the entire article, as discussed above).

## **18. Public Accessibility of EX1053 (“AMD Evergreen”)**

138. EX1053 (which I refer to herein as “AMD Evergreen”) is an article from AnandTech.com titled “AMD Evergreen: 40nm DirectX 11 GPU Silicon Arrives.” The face of EX1053 is dated “June 3, 2009,” indicating it was publicly accessible from AnandTech.com by that date. As I discussed above (§II.C.13) Anandtech.com is a source of information for commercial GPUs and microprocessors that POSAs interested in the field of computing would have been aware of considered a reliable source of information regarding commercial chips.

139. Pages 63-64 of EX1048 is the Internet Archive’s archived capture of AnandTech’s homepage, <https://www.anandtech.com>, as it existed on June 3, 2009 as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20090603130817/https://www.anandtech.com/>. *See*

EX1048, ¶¶5-6, p. 62. Near the top of that page is hyperlinked text that reads

“AMD Evergreen: 40nm DirectX 11 GPU Silicon Arrives,” which navigates to

<http://www.anandtech.com/video/showdoc.aspx?i=3573>. Pages 16-19 of EX1047

(which is EX1053) is the Internet Archive’s archived capture of that page as it existed on June 6, 2009, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20090606053120/http://www.anandtech.com/video/showdoc.aspx?i=3573>. *See* EX1047, ¶¶5-6, p. 15.

140. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the computing industry and data about commercial GPUs and microprocessors, could have located EX1053 by searching the Web for keywords of interest such as “AMD,” “GPU,” “transistors,” and “die” which are terms that appear in EX1053 and would be terms of interest to a POSA interested in the computing industry.

141. Based on the above evidence and my review of the indicia appearing on EX1053, it is my opinion that EX1053 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by June 6, 2009.

#### **19. Public Accessibility of EX1088 (“VSI Standard”)**

142. EX1088 (which I refer to herein as the “VSI Standard”) is titled “VSI Alliance™ Virtual Component Interface Standard Version 2 (OCB 2 2.0) On-Chip Bus Development Working Group April 2001.” Stuttard (EX1006) refers to the “Virtual Component Interface Standard by the VSI Alliance” (Stuttard, 13:7-9), which indicates that the VSI Alliance’s Virtual Component Interface Standard was publicly accessible to POSAs interested in its subject matter. Thus, POSAs

interested in Stuttard's teachings would have had reason to obtain standard documents published by the VSI Alliance, such as by navigating to the VSI Alliance's website as it was (and still is) conventional for standards bodies and alliances to provide copies of their standards and publications for members and other interested persons on their websites. As shown below, a recent search of Google Scholar returned 465 articles from 2009 and earlier that included the VSI Alliance's website – [www.vsi.org](http://www.vsi.org) –including IEEE publications, corroborating my opinion that POSAs would have been well-aware of the VSI Alliance's website and standards. *See also* Bolin, ¶6 (identifying Google Scholar as a reliable repository of scholarly and research data).



143. Pages 105-106 of EX1048 is the Internet Archive's archived capture of the VSI Alliance's homepage, <https://vsi.org/>, as it existed on January 22, 2002, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20020122030423/https://vsi.org>. See EX1048, ¶¶5-6, p. 104. At the left of the VSI's homepage, there is the text "members list," which navigates to the VSI Alliance's Member List webpage at <http://www.vsi.org/members.htm>. Pages 7-8 of EX1047 is the Internet Archive's archived capture of that webpage as it existed on February 10, 2002, as reflected in the Internet Archive's extended URL:

<https://web.archive.org/web/20020210130046/http://www.vsi.org/members.htm>.

See EX1047, p. 6. As shown on Pages 7-8 of EX1047, the VSI Alliance's Members included many of the largest and well-known corporations in the semiconductor and related industries, like Analog Devices, ARM, Hewlett-Packard, IBM, Motorola, Samsung, and TSMC.

144. At the top of the VSI's homepage (EX1048, 105), there is the text "VSIA Specifications," which navigates to the VSI Alliance's Technical Documents & Specifications webpage at

<http://www.vsi.org/library/specs/summary.htm>. Pages 101-103 of EX1048 is the Internet Archive's archived capture of that webpage as it existed on February 15, 2002, as reflected in the Internet Archive's extended URL: <https://web.archive.org/web/20020215225401/http://www.vsi.org/library/specs/summary.htm>. See EX1048, p. 100.

145. As shown on Pages 101-103 of EX1048, the VSI Alliance's Technical Documents & Specifications webpage included links to retrieve various publications of the VSI Alliance, one of which include the "Virtual Component Interface Standard Version 2," which is the name of the document on the face of EX1088. The VSI's Alliance's Technical Documents & Specifications webpage also notes that this is the OCB 2 2.0 – Revision Date: April 2001, consistent with the face of EX1088 which includes the text "OCT 2 2.0" and the date "April 2001." As shown on Page 103 of EX1048, the Alliance's Technical Documents & Specifications webpage included hyperlinks for a "Member Download" and a "Non Member Buy a Single Copy here." Based on the above evidence, I conclude that EX1088 would have been publicly accessible to a POSA exercising reasonable diligence at least by the year 2002.

## **20. Public Accessibility of EX1094 ("Chen")**

146. EX1094 (which I refer to herein as "Chen") is titled "A cost effective 32nm high-K/ metal gate CMOS technology for low power applications with single-metal/gate-first process." EX1094 appears to be a scan of a print copy of the cover matter of the journal in which the Chen article was published along with the table of contents for the publication and a copy of the Chen article. The face of EX1094 indicates that it was published by the IEEE in connection with the 2008 Symposium on VLSI Technology held on June 17-19, 2008 and provides an

“ISBN 13” number. Page 3 of EX1094 includes what appears to be a stamp from the SUNY Institute of Technology at Utica/Rome – Library. Page 4 of EX1094 includes a “Copyright © 2008 by The Institute of Electrical and Electronics Engineers, Inc.,” which indicates it was published by the IEEE in 2008. Page 67 of the Chen article similarly includes a copyright “©2008 IEEE.” IEEE Xplore indicates that Chen was “Published in: 2008 Symposium on VLSI” by the IEEE in connection with a conference held on June 17-19, 2008, and had a “Date Added to IEEE Xplore” of August 5, 2008 and had an “ISBN” number and “Print ISSN” number.<sup>24</sup> *See* Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Testimony from an IEEE representative demonstrates public accessibility of EX1094 no later than June 19, 2008. *See* EX1130, ¶¶6-11. Based on the above evidence and my understanding of the IEEE and IEEE Xplore, it is my opinion that Chen is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence by June 19, 2008, or at least by August 5, 2008.

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<sup>24</sup> <https://ieeexplore.ieee.org/document/4588573>

## 21. Public Accessibility of EX1097 (“Schiml”)

147. EX1097 (which I refer to herein as “Schiml”) is titled “A 0.13 $\mu$ m CMOS platform with Cu/low-k interconnects for system on chip applications.” As indicated on the face of EX1097, Schiml was published in connection with the 2001 Symposium on VLSI Technology Digest of Technical Papers. IEEE Xplore indicates that Schiml was published by the IEEE in connection with a June 12-14, 2001 conference and had a “Date Added to IEEE Xplore” of August 7, 2002 and had a “Print ISBN” number.<sup>25</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Testimony from an IEEE representative demonstrates public accessibility of EX1097 no later than June 14, 2001. See EX1131, ¶¶6-11. Based on the above evidence and my review of the indicia appearing on the Schiml document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Schiml is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence by June 14, 2001, or at least by August 2002.

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<sup>25</sup> <https://ieeexplore.ieee.org/document/934969>

## **22. Public Accessibility of EX1098 (“Sudha”)**

148. EX1098 (which I refer to herein as “Sudha”) is titled “An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation.” As indicated on the face of EX1098, Sudha was published in Volume 53, No. 5, September-October 2007 issue of the IETE Journal of Research. I have reviewed EX1098, the first page of which appears to be a library scan of the front page of a physical copy of the issue of the IETE Journal of Research in which the Sudha article was published. I am aware from my past work experience that the IETE, or Institute of Electronics and Telecommunication Engineers, is an Indian organization that is often considered to be the IEEE of India. Sudha, p. 1. As the official website for the IETE states, the IETE is “is India’s leading recognized professional society devoted to the advancement of Science and Technology of Electronics, Telecommunication & IT” and has “more than 1,25,000 members.”<sup>26</sup> The cover page of Sudha bears the label “Volume 53, No. 5, September-October 2007” and an “ISSN” number of 0377-2063. In addition, the cover page of Sudha bears a stamp from the “Linda Hall Library” dated December 28, 2007. Page 425 of Sudha bears a “Copyright © 2007 by the IETE,” which indicates that the document was published in the year 2007. Based

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<sup>26</sup> <https://www.iete.org/aboutiete.html>

on my review of the indicia appearing on the Sudha document and my understanding of the IETE, it is my opinion that Sudha is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by the end of 2007.

### **23. Public Accessibility of EX1100 (“Oh”)**

149. EX1100 (which I refer to herein as “Oh”) is titled “A fully pipelined single-precision floating-point unit in the synergistic processor element of a CELL processor.” As indicated on the face of EX1100, Oh was published by the IEEE in Volume 41, Number 4 of the IEEE Journal of Solid-State Circuits (April 2006). I have reviewed Oh, which appears to be a library scan of a physical copy of the issue of the journal that contained Oh. The cover page of Oh bears an “ISSN” number of 0018-9200 and a stamp from the “Linda Hall Library” dated April 10, 2006. Page 759 of Oh bears a Copyright “© 2006 IEEE,” which indicates it was published in 2006. IEEE Xplore indicates that Oh had a “Date of Publication” of March 27, 2006.<sup>27</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of

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<sup>27</sup> <https://ieeexplore.ieee.org/document/1610620>

electrical engineering, computer science, and related disciplines”). Testimony from an IEEE representative demonstrates public accessibility of EX1100 no later than March 31, 2006. *See* EX1133, ¶¶6-11. Based on the above evidence and my review of the indicia appearing on the Oh document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Oh is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by the end of 2006. *See also* Bolin, ¶¶91-95 (concluding that the Oh article “was publicly accessible by July 2005 and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence, on their own or with the assistance of a research librarian”).

#### **24. Public Accessibility of EX1103 (“Prabhu”)**

150. EX1103 (which I refer to herein as “Prabhu”) is titled “SOMGPU: An Unsupervised Pattern Classifier on Graphical Processing Unit.” As indicated on the face of EX1103, Prabhu was published by the IEEE in connection with the 2008 IEEE Congress on Evolutionary Computation (IEEE World Congress on Computational Intelligence). Page 1101 of Prabhu bears a Copyright “© 2008 IEEE,” which indicates it was published by the IEEE in 2008. IEEE Xplore

indicates that Prabhu had a “Date Added to IEEE *Xplore*” of September 23, 2008.<sup>28</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Based on the above evidence and my review of the indicia appearing on the Prabhu document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Prabhu is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by September 23, 2008.

## **25. Public Accessibility of EX1104 (“Poli”)**

151. EX1104 (which I refer to herein as “Poli”) is titled “Processing Neocognitron of Face Recognition on High Performance Environment Based on GPU with CUDA Architecture.” As indicated on the face of EX1104, Poli was published by the IEEE in connection with the 2008 20<sup>th</sup> International Symposium on Computer Architecture and High Performance Computing. I have reviewed Poli, which appears to be a library scan of a physical copy of the issue of the journal that contained Poli. Page 2 of EX1104 bears a “Copyright © 2008 by The

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<sup>28</sup> <https://ieeexplore.ieee.org/abstract/document/4630920>

Institute of Electrical and Electronics Engineers, Inc.” an “ISBN” number and an “ISSN” number. Page 4 of EX1104 bears a stamp from the “Linda Hall Library.” Page 7 of Poli bears a Copyright “© 2008 IEEE,” which indicates it was published in 2008. IEEE Xplore indicates that Poli had a “Date Added to IEEE *Xplore*” of November 21, 2008.<sup>29</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Based on the above evidence and my review of the indicia appearing on the Poli document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Poli is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by November 21, 2008.

## **26. Public Accessibility of EX1105 (“Ligon”)**

152. EX1105 (which I refer to herein as “Ligon”) is titled “A re-evaluation of the practicality of floating-point operations on FPGAs.” As indicated on the face of EX1105, Ligon was published by the IEEE in connection with the IEEE Symposium on FPGAs for Custom Computing Machines (Cat. No.98TB100251)

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<sup>29</sup> <https://ieeexplore.ieee.org/document/4685731>

April 17, 1998. I have reviewed Ligon, which appears to be a library scan of a physical copy of the issue of the journal that contained Ligon. Page 3 of EX1105 bears a “Copyright © 2008 by The Institute of Electrical and Electronics Engineers, Inc.” an “ISBN” number and an “ISSN” number. Page 3 of EX1105 also bears a stamp from the “University of Wisconsin-Madison.” Page 206 of Ligon bears a Copyright “© 1998 IEEE,” which indicates it was published in 1998. IEEE Xplore indicates that Ligon had a “Date Added to IEEE *Xplore*” of August 6, 2002.<sup>30</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Based on the above evidence and my review of the indicia appearing on the Ligon document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Ligon is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by August 6, 2002.

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<sup>30</sup> <https://ieeexplore.ieee.org/document/707898>

## **27. Public Accessibility of EX1106 (“Held”)**

153. EX1106 (which I refer to herein as “Held”) is titled “From a Few Cores to Many: A Tera-scale Computing Research Overview.” As shown on the face of EX1106, Held is a “White Paper” from Intel, one of the leading semiconductor manufacturers and designers of microprocessors in the world. POSAs interested in the field of computing exercising reasonable diligence had reason to navigate to Intel’s website to review the information and documentation available there, such as white papers and press releases, available from Intel’s website regarding Intel’s products, research, and development.

154. Page 82 of EX1048 is the Internet Archive’s archived capture of Intel’s homepage, <http://www.intel.com/>, as it existed on December 6, 2006, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20061206101550/http://www.intel.com/>. *See*

EX1048, ¶¶5-6, p. 81. At the top of Intel’s homepage, there is the text

“Technology & Research,” which navigates to

[http://www.intel.com/technology/index.htm?iid=homepage+hdr\\_nav1\\_technology](http://www.intel.com/technology/index.htm?iid=homepage+hdr_nav1_technology).

Page 80 of EX1048 is the Internet Archive’s archived capture of that webpage as it existed on December 6, 2006, as reflected in the Internet Archive’s extended URL:

[https://web.archive.org/web/20061206013632/http://www.intel.com/technology/index.htm?iid=homepage+hdr\\_nav1\\_technology](https://web.archive.org/web/20061206013632/http://www.intel.com/technology/index.htm?iid=homepage+hdr_nav1_technology). *See* EX1048, p. 79.

155. On the left of that webpage, there is the text “Intel® multi-core,” which navigates to <http://www.intel.com/multi-core/index.htm>. Page 78 of EX1048 is the Internet Archive’s archived capture of that webpage as it existed on December 2, 2006, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20061202183758/http://www.intel.com/multi-core/index.htm>. *See* EX1048, p. 77.

156. On the bottom right of that webpage, there is the text “Tera-scale Research,” which navigates to <http://www.intel.com/technology/techresearch/terascale/index.htm>. Page 76 of EX1048 is the Internet Archive’s archived capture of that webpage as it existed on November 28, 2006, as reflected in the Internet Archive’s extended URL: <https://web.archive.org/web/20061128200422/http://www.intel.com/technology/techresearch/terascale/index.htm>. *See* EX1048, p. 75.

157. On the bottom of that webpage there is the text “A whitepaper detailing our tera-scale computing research vision,” which provides a hyperlink to a PDF that the Internet Archived captured on July 3, 2007, as reflected in the Internet Archive’s extended URL: [https://web.archive.org/web/20070703180231/http://download.intel.com/research/platform/terascale/terascale\\_overview\\_paper.pdf](https://web.archive.org/web/20070703180231/http://download.intel.com/research/platform/terascale/terascale_overview_paper.pdf). That PDF is EX1106. *See* EX1047, ¶¶5-6, pp. 66-78.

158. Based on the above evidence, it is my opinion that EX1106 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least in the year 2007.

## **28. Public Accessibility of EX1107 (“Reddaway”)**

159. EX1107 (which I refer to herein as “Reddaway”) is titled “Ultra-high performance, low-power, data parallel radar implementations.” As indicated on the face of EX1107, Reddaway was published by the IEEE in connection with the IEEE International Radar Conference. I have reviewed Reddaway, which appears to be a library scan of a physical copy of the issue of the journal that contained Reddaway. Page 4 of EX1107 bears a “Copyright © 2005 by The Institute of Electrical and Electronics Engineers, Inc.” an “ISBN” number and an “ISSN” number. Page 5 of EX1107 bears a stamp from the “Library of Congress Copyright Office” dated July 29, 2005. Page 822 of Reddaway bears a Copyright “© 2005 IEEE,” which indicates it was published in 2005. IEEE Xplore indicates that Reddaway had a “Date Added to IEEE Xplore” of June 6, 2005.<sup>31</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for

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<sup>31</sup> <https://ieeexplore.ieee.org/document/1435940>

researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Based on the above evidence and my review of the indicia appearing on the Reddaway document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Reddaway is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least in the year 2005.

## **29. Public Accessibility of EX1108 (“Lokhmotov”)**

160. EX1108 (which I refer to herein as “Lokhmotov”) is titled “Revisiting SIMD Programming.” As indicated on the face of EX1108, Lokhmotov was published by the publisher Springer in connection with the 20<sup>th</sup> International Workshop of Languages and Compilers for Parallel Computing (LPCP) in Urbana, IL, USA, October 11-13, 2007. According to Dr. Bolin, the publisher Springer-Verlag “was and is a well-known and respected publisher (founded in 1842) of academic journals and books ... [and] provides an online search tool (‘SpringerLink’)[<sup>1</sup>] for providing researchers with access to millions of academic publications.” Bolin, ¶16. According to Dr. Bolin, the book containing the Lokhmotov article has a creation date of August 12, 2008 in the OCLC MARC database. *See* Bolin, ¶119; *id.* ¶¶7-15 (discussing MARC records). As shown in

Attachment 15b to Dr. Bolin’s declaration, the Springer Link database indicates a copyright of “© 2008 Springer-Verlag Berlin Heidelberg,” consistent with the face of EX1108. Bolin, ¶120. Attachment 15c to Dr. Bolin’s declaration includes an electronic copy of the Lokhmotov article, which is identical to EX1108, that Dr. Bolin retrieved from the Springer Link database along with cover matter for the book that contained the Lokhmotov article. Bolin, ¶121. Based on this evidence and the other evidence Dr. Bolin reviewed, Dr. Bolin concluded that the Lokhmotov article was indexed, searchable and publicly accessible by August 12, 2008. Bolin, ¶¶119-123.

161. I have also reviewed Lokhmotov, which appears to be a library scan of a physical copy of the issue of the journal that contained Lokhmotov. Page 2 of EX1107 bears a Copyright “© Springer-Verlag Berlin Heidelberg 2008” and an “ISBN-10” number, “ISBN-13” number, and an “ISSN” number. Page 2 of EX1108 also bears a stamp from the “Cornell University Libraries.” Page 6 of Lokhmotov bears a Copyright “© Springer-Verlag Berlin Heidelberg 2008,” which indicates it was published in 2008. The ACM Digital Library indicates that the Lokhmotov article was published October 1, 2007.<sup>32</sup> See Bolin, ¶17 (identifying

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<sup>32</sup> [https://dl.acm.org/doi/10.1007/978-3-540-85261-2\\_3](https://dl.acm.org/doi/10.1007/978-3-540-85261-2_3); see also

[https://link.springer.com/chapter/10.1007/978-3-540-85261-2\\_3#Abs1](https://link.springer.com/chapter/10.1007/978-3-540-85261-2_3#Abs1)

the ACM Digital Library as “a well-known and widely used resource for researchers, educators, and professionals in the field of computer science and related disciplines”). Based on the above evidence and my review of the indicia appearing on the Lokhmotov document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Lokhmotov is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by August 12, 2008.

### **30. Public Accessibility of EX1110 (“Shahbahrami”)**

162. EX1110 (which I refer to herein as “Shahbahrami”) is titled “Tradeoff analysis of integer multiplier circuits implemented in FPGAs.” As indicated on the face of EX1110, Shahbahrami was published by the IEEE in connection with the 2008 Tenth IEEE International Symposium on Multimedia. I have reviewed Shahbahrami, which appears to be an electronic copy from the issue of the journal that contained Shahbahrami. Page 4 of EX1110 bears a “Copyright © 2008 by The Institute of Electrical and Electronics Engineers, Inc.,” which indicates it was

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(SpringerLink database to retrieve digital copy of the Lokhmotov article); Bolin, ¶16 (identifying Springer-Verlag as a “well-known and respected published (founded in 1842) of academic journals and books”).

published by the IEEE in 2008, and an “ISBN” number. Page 607 of Shahbahrami bears a Copyright “© 2008 IEEE,” which indicates it was published in 2008. IEEE Xplore indicates that Shahbahrami had a “Date Added to IEEE Xplore” of January 9, 2009.<sup>33</sup> *See* Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Testimony from an IEEE representative demonstrates public accessibility of EX1110 no later than December 17, 2008. *See* EX1134, ¶¶6-11. Based on the above evidence and my review of the indicia appearing on the Shahbahrami document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Shahbahrami is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence by December 17, 2008, or at least by January 9, 2009.

### **31. Public Accessibility of EX1111 (“Noumsi”)**

163. EX1111 (which I refer to herein as “Noumsi”) is titled “Acceleration of a content-based image-retrieval application on the RDISK cluster.” I have reviewed EX1112, which appears to be a scan of the face and table of contents of

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<sup>33</sup> <https://ieeexplore.ieee.org/document/4741235>

the journal of a bound collection of abstracts of papers published in connection with the 20<sup>th</sup> IEEE International Parallel & Distributed Processing Symposium. Page 3 of EX1112 indicates that this publication included “Abstracts and CD-ROM,” of the articles listed therein, which suggests that the CD-ROM that accompanied this document included electronic copies of the articles listed in the table of contents starting on 7 of EX1112. Page 3 of EX1112 bears a stamp from the “Library of Congress Copyright Office,” dated June 2, 2006. Page 4 of EX1112 bears a “Copyright © 2006 by The Institute of Electrical and Electronics Engineers, Inc.,” an “ISBN” number and an “ISSN” number. Page 13 of EX1112 identifies an article titled “Acceleration of a content-based image-retrieval application on the RDISK cluster,” by the authors “A. Noumsi, S. Derrien, and P. Quinton,” which is the title and authors listed on the face of the Noumsi article in EX1111. Page 38 of EX1112 includes a copy of the abstract of the Noumsi article that matches the abstract on the face of EX1111. IEEE Xplore indicates that Noumsi had a “Date Added to IEEE Xplore” of June 26, 2006.<sup>34</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Based on the above evidence and my

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<sup>34</sup> <https://ieeexplore.ieee.org/document/1639346>

review of the indicia appearing on the Noumsi document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Noumsi is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least in the year 2006.

### **32. Public Accessibility of EX1113 (“Pengdong”)**

164. EX1113 (which I refer to herein as “Pengdong”) is titled “Performance Comparison between Color and Spatial Segmentation for Image Retrieval and Its Parallel System Implementation.” As indicated on the face of EX1113, Pengdong was published by the IEEE in connection with the 2008 International Symposium on Computer Science and Computational Technology. I have reviewed Pengdong, which appears to be a library scan of a physical copy of the issue of the journal that contained Pengdong. Page 2 of EX1113 bears a “Copyright © 2008 by The Institute of Electrical and Electronics Engineers, Inc.” and an “ISBN-13” number. Page 4 of EX1113 bears a stamp from the “Linda Hall Library.” Page 14 of Pengdong bears a Copyright “© 2008 IEEE,” which indicates it was published in 2008. IEEE Xplore indicates that Pengdong had a “Date Added

to IEEE *Xplore*” of December 30, 2008.<sup>35</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Based on the above evidence and my review of the indicia appearing on the Pengdong document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Pengdong is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by December 30, 2008.

### **33. Public Accessibility of EX1114 (“Bradley”)**

165. EX1114 (which I refer to herein as “Bradley”) is titled “Exploiting Loop-Level Parallelism for SIMD Arrays Using *OpenMP*.” Based on the evidence I discuss below, it is my opinion that Bradley is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by November 11, 2008.

166. The face of EX114 bears a copyright “© Springer-Verlag Berlin Heidelberg 2008,” which indicates it was published in 2008. According to Dr.

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<sup>35</sup> <https://ieeexplore.ieee.org/document/4731486>

Bolin, the publisher Springer-Verlag “was and is a well-known and respected publisher (founded in 1842) of academic journals and books ... [and] provides an online search tool (‘SpringerLink’)[ ] for providing researchers with access to millions of academic publications.” Bolin, ¶16. According to Dr. Bolin, the book containing the Bradley article has a creation date of November 11, 2008 in the OCLC MARC database, which was published in connection with the Proceedings of the 3<sup>rd</sup> International Workshop on OpenMP, IWOMP 2007, Beijing China, June 3-7, 2007. *See* Bolin, ¶1078; *id.* ¶¶7-15 (discussing MARC records). EX1114 is the copy of the Bradley article that Dr. Bolin obtained from the Springer Link database. Bolin, ¶108. As shown in Attachment 13b to Dr. Bolin’s declaration, the Springer Link database indicates a copyright of “© 2008,” consistent with the face of EX1114. Attachment 13c to Dr. Bolin’s declaration, which is EX1114, is an electronic copy of the Bradley article that Dr. Bolin retrieved from the Springer Link database. Bolin, ¶109. Based on this evidence, Dr. Bolin concluded that the Bradley article was indexed, searchable and publicly accessible by at least November 11, 2008. Bolin, ¶¶107-112. Based on the above evidence, I too conclude that Schmidt-2000 would have also been publicly accessible to a POSA exercising reasonable diligence at least by November 11, 2008.

### 34. Public Accessibility of EX1115 (“Haran”)

167. EX1115 (which I refer to herein as “Haran”) is titled “22 nm technology compatible fully functional 0.1  $\mu\text{m}^2$  6T-SRAM cell.” I have reviewed EX1115, which appears to be a digital copy of an article retrieved from IEEE Xplore (see footer of page 1). IEEE Xplore indicates that Haran was published by the IEEE and “Published in: 2008 IEEE International Electron Devices Meeting,” for a conference held on December 15-17, 2008, and had a “Date Added to IEEE Xplore” of February 27, 2009, and had a “Print ISBN” number and “Print ISSN” number.<sup>36</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Testimony from an IEEE representative demonstrates public accessibility of EX1115 no later than December 17, 2008. See EX1135, ¶¶6-11. Based on the above evidence and my understanding of the IEEE and IEEE Xplore, it is my opinion that EX1115 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence by December 17, 2008, or at least by February 27, 2009.

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<sup>36</sup> <https://ieeexplore.ieee.org/document/4796769>

### 35. Public Accessibility of EX1116 (“Li”)

168. EX1116 (which I refer to herein as “Li”) is titled “Operating System Support for Shared-ISA Asymmetric Multi-core Architectures.” The Semantic Scholar database indicates that Li was published in 2008.<sup>37</sup> The ACM Digital Library indicates that Li was cited in a paper published on April 21, 2009 that concerned multicore processors, which indicates that Li was publicly accessible to POSAs in the art exercising reasonable diligence at least by the April 2009.<sup>38</sup> *See* Bolin, ¶17 (identifying ACM Digital Library as a “well-known and widely used resource for researchers, educators, and professionals in the field of computer science and related disciplines”). Based on the above evidence and my understanding of the ACM and ACM Digital Library, it is my opinion that Li is

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<sup>37</sup> <https://www.semanticscholar.org/paper/Operating-System-Support-for-Shared-ISA-Asymmetric-Li-Brett/c835d52e0c8ac9c861f1a5ca215dbdc7d48aeff9>; <https://www.semanticscholar.org/about> (“Semantic Scholar provides free, AI-driven search and discovery tools, and open resources for the global research community. We index over 200 million academic papers sourced from publisher partnerships, data providers, and web crawls.”).

<sup>38</sup> <https://dl.acm.org/doi/10.1145/1531793.1531801> (identifying Li as cited Reference 22).

prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by April 21, 2009.

### **36. Public Accessibility of EX1117 (“Borkar”)**

169. EX1117 (which I refer to herein as “Borkar”) is titled “Thousand Core Chips—A Technology Perspective.” According to Dr. Bolin, the ACM Digital Library indicates that the Borkar article was published on June 4, 2007 in connection with a 2007 conference. Bolin, ¶97; §I.C above (discussing the ACM and ACM Digital Library). Attachment 11b to Dr. Bolin’s declaration, which is EX1117, is the copy of Borkar that Dr. Bolin retrieved from the ACM Digital Library. Bolin, ¶98. As Dr. Bolin noted, the first page of EX1117 includes a “Copyright 2007 ACM.” Based on this evidence, Dr. Bolin concluded that the Borkar article was indexed, searchable and publicly accessible no later than early June 2007, which is consistent with evidence I have reviewed. Bolin, ¶100 (concluding that the Borkar article “was publicly accessible by June 2007 and could have been located by any member of the public interested in the subject matter by exercising reasonable diligence, on their own or with the assistance of a research librarian”). Based on the above evidence, I too conclude that Borkar

would have also been publicly accessible to a POSA exercising reasonable diligence by June 2007. *See also* Bolin, ¶¶96-100.

### **37. Public Accessibility of EX1118 (“Hannibal”)**

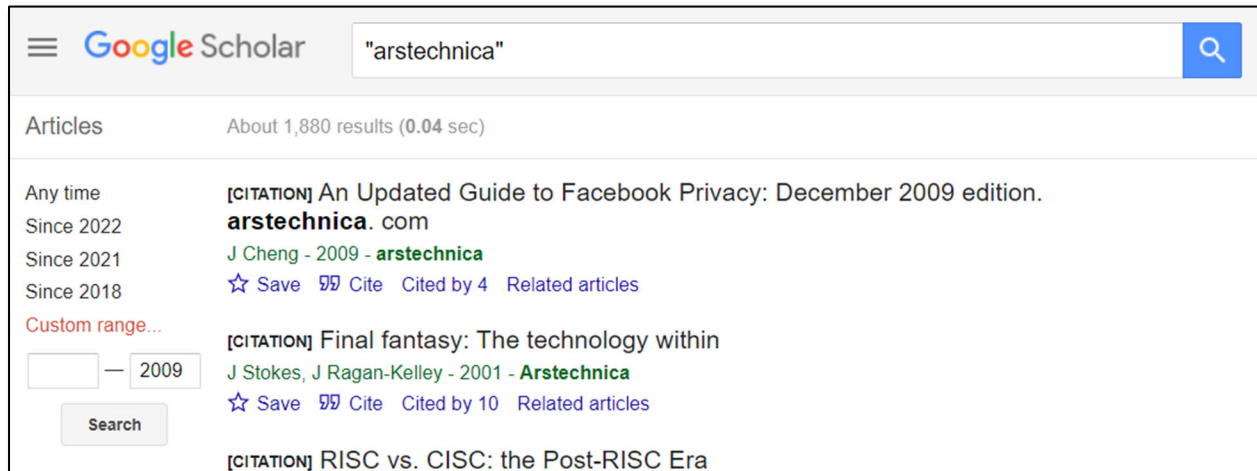
170. EX1118 (which I refer to herein as “Hannibal”) is an article from Arstechnica.com titled “ClearSpeed kicks it up a notch.” Based on the evidence I discuss below, it is my opinion that EX1118 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by October 13, 2004.

171. According to the face of EX1118, EX1118 was published on October 11, 2004 on the website arstechnica.com. According to Arstechnica’s website, Ars Technica “was founded in 1998” as a “a publication devoted to technology” and “[i]n 2001, Ars launched a digital subscription service” and in 2008 it was acquired by “the parent company of Condé Nast,” a well-known and reputable publisher of magazines, such as Wired and The New Yorker.<sup>39</sup> For example, as shown below, a recent search of Google Scholar returned 1,880 articles from 2009 and earlier that included “arstechnica” and 770 articles hosted on sites that were not under the

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<sup>39</sup> <https://arstechnica.com/about-us/>; <https://www.condenast.com/brands-and-markets/brands>

arstechnica.com domain name, demonstrating that Ars Technica was a well-known website for those interested in technology, such as the technology of computing devices.<sup>40,41</sup> *See also* Bolin, ¶6 (identifying Google Scholar as a reliable repository of scholarly and research data).

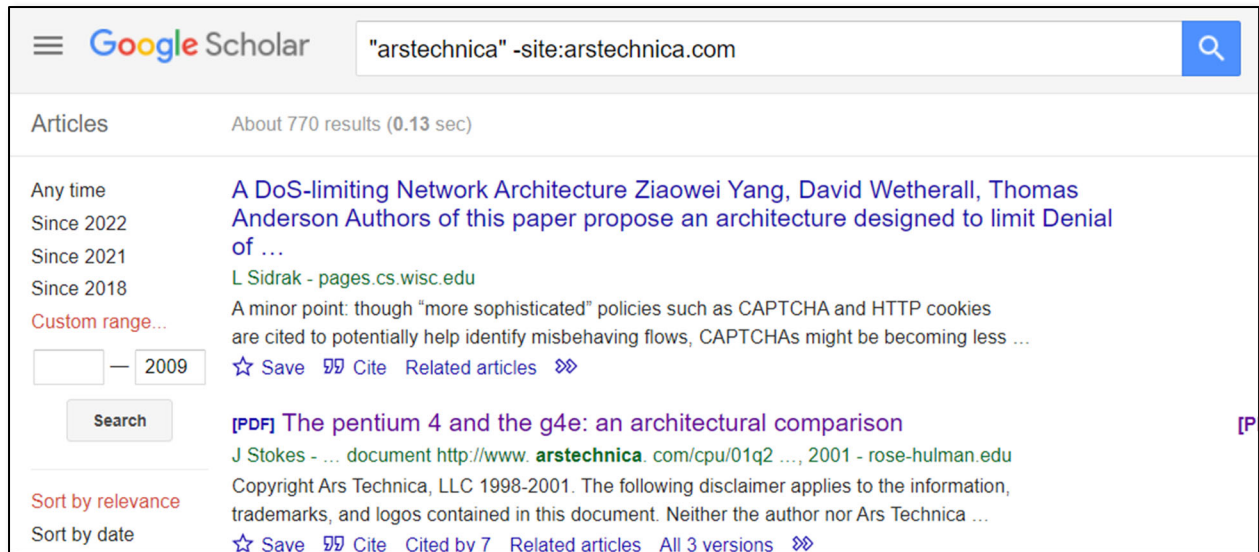


<sup>40</sup> [https://scholar.google.com/scholar?q=%22...](https://scholar.google.com/scholar?q=%22arstechnica%22&hl=en&as_sdt=0%2C33&as_ylo=&as_yhi=2009)

[arstechnica%22&hl=en&as\\_sdt=0%2C33&as\\_ylo=&as\\_yhi=2009](https://scholar.google.com/scholar?q=%22arstechnica%22&hl=en&as_sdt=0%2C33&as_ylo=&as_yhi=2009)

<sup>41</sup> [https://scholar.google.com/scholar?hl=en&as\\_sdt=0%2C33&as\\_yhi=2009...](https://scholar.google.com/scholar?hl=en&as_sdt=0%2C33&as_yhi=2009...)

[&q=%22arstechnica%22+-site%3Aarstechnica.com&btnG=](https://scholar.google.com/scholar?hl=en&as_sdt=0%2C33&as_yhi=2009...&q=%22arstechnica%22+-site%3Aarstechnica.com&btnG=)



172. Page 8 of EX1123 is the Internet Archive’s archived capture of Arstechnica.com’s homepage, <http://arstechnica.com/index.ars>, as it existed on October 13, 2004, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20041013014107/http://arstechnica.com/index.ars>.

See EX1123, ¶¶5-6, p. 7. On the left, towards the bottom of Arstechnica’s homepage, there is a hyperlink to the “Full Story” for an article titled “ClearSpeed kicks it up a notch,” which navigates to the article in EX1118. Page 5-6 of EX1123, which is EX1118, is the Internet Archive’s archived capture of that webpage as it existed on October 13, 2004, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20041013015215/http://arstechnica.com/news.ars/post/20041011-4293.html>. See EX1123, p. 4. Additionally, Internet search engines

(e.g., Google, Yahoo, etc.) would have had access to the same webpages using the

same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the computing industry, could have located EX1118 by searching the Web for keywords of interest such as “processing elements” and “FPU” and “floating-point,” which are terms that appear in EX1118 and would be terms of interest to a POSA interested in the computing industry. Based on the above evidence and my review of the indicia appearing on EX1118, it is my opinion that EX1118 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by October 13, 2004.

### **38. Public Accessibility of EX1120 (“Manocha”)**

173. EX1120 (which I refer to herein as “Manocha”) is titled “A cost effective 32nm high-K/ metal gate CMOS technology for low power applications with single-metal/gate-first process.” As indicated on the face of EX1120, Manocha was published by the IEEE in Volume 38, Issue 8 of the magazine Computer. I have reviewed Manocha, which appears to be a library scan of a physical copy of the issue of the issue of Computer that contained Manocha. Page 1 of EX1120 bears a library stamp date August 8, 2005. Page 2 of EX1120 bears a “Copyright © 2005 by The Institute of Electrical and Electronics Engineers, Inc.”

and page 5 bears “ISSN” number. Page 85 of Manocha states that it was “Published by the IEEE Computer Society” and the date “August 2005.” IEEE Xplore indicates that Manocha had a “Date of Publication” of August 8, 2005.<sup>42</sup> See Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Based on the above evidence and my review of the indicia appearing on the Manocha document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Manocha is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by August 8, 2005.

### **39. Public Accessibility of EX1124 (“Burger”)**

174. EX1124 (which I refer to herein as “Burger”) is titled “Composable Multicore Chips.” As indicated on page 2 of EX1124, Burger was published in a book titled “Multicore Processors and Systems” by the publisher Springer. According to Dr. Bolin, the publisher Springer-Verlag “was and is a well-known and respected publisher (founded in 1842) of academic journals and books ...

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<sup>42</sup> <https://ieeexplore.ieee.org/document/1492276>

[and] provides an online search tool (‘SpringerLink’)[ ] for providing researchers with access to millions of academic publications.” Bolin, ¶16. According to Dr. Bolin, the book containing the Burger article has a creation date of June 18, 2009 in the OCLC MARC database. *See* Bolin, ¶82; *id.* ¶¶7-15 (discussing MARC records). As shown in Attachment 8c to Dr. Bolin’s declaration, the Springer Link database indicates the book containing the Burger article was “First Online: 01 January 2009” and had a copyright of “© 2009 Springer-Verlag US,” consistent with page 3 of EX1124. Bolin, ¶83. Attachment 8d to Dr. Bolin’s declaration, which is EX1124 includes an electronic copy of the Burger article that Dr. Bolin retrieved from the Springer Link database along with cover matter for the book that contained the Burger article. Bolin, ¶184. Based on this evidence and the other evidence Dr. Bolin reviewed, Dr. Bolin concluded that the Burger article was indexed, searchable and publicly accessible by January 1, 2009, which is consistent with evidence I have reviewed. Bolin, ¶¶81-85. Based on the above evidence, I too conclude that Burger would have also been publicly accessible to a POSA exercising reasonable diligence by January 1, 2009.

#### **40. Public Accessibility of EX1125 (“Roma”)**

175. EX1125 (which I refer to herein as “Roma”) is titled “In the Development and Evaluation of Specialized Processors for Computing High-Order 2-D Image Moments in Real-Time.” As indicated on page 170 of EX1125, Roma

was published by the IEEE and bears a copyright “© 2000 IEEE,” which indicates it was published in the year 2000. As shown in attachment 14b to Dr. Bolin’s declaration, IEEE Xplore indicates that the Roma article was added to IEEE Xplore on August 6, 2002. Bolin, ¶114. Testimony from an IEEE representative demonstrates public accessibility of EX1125 no later than September 13, 2000. *See* EX1136, ¶¶6-11. Based on this evidence and the other evidence Dr. Bolin reviewed, Dr. Bolin concluded that the Roma article was indexed, searchable and publicly accessible by August 6, 2002, but at least no later than March 1, 2004, which is consistent with evidence I have reviewed. Bolin, ¶¶113-117. Based on the above evidence, I conclude that Roma would have been publicly accessible to a POSA exercising reasonable diligence by 2004.

#### **41. Public Accessibility of EX1126 (“Intel 22nm”)**

176. As shown on its face, EX1126 is a “News Fact Sheet” from Intel titled “Intel Developer Forum 22nm News Facts” dated September 22, 2009. EX1126 states that “Intel Corporation is holding its Intel Developer Forum in San Francisco from Sept. 22-24” and “Paul Otellini, Intel president and CEO, **today** [i.e., September 22, 2009] displayed the world’s first working chips built on 22nm process technology.” In my opinion, POSAs interested in the field of computing would have been familiar with the technological developments announced by Intel at its developer forums and would have been the type of people that attended

Intel's developer forums, which were "a biannual gathering of technologists to discuss Intel products and products based on Intel products."<sup>43</sup> POSAs that did not personally attend the Intel developer's forum had reason to navigate to Intel's website to find information about the technologies discussed at the forum, such as through Intel press releases and white papers posted to and/or retrievable from Intel's website.

177. Page 98 of EX1048 is the Internet Archive's archived capture of Intel's homepage, <http://www.intel.com/index.htm/>, as it existed on October 19, 2009, as reflected in the Internet Archive's extended URL:

[https://web.archive.org/web/20091019172712/http://www.intel.com/index.htm/#/en\\_US\\_01](https://web.archive.org/web/20091019172712/http://www.intel.com/index.htm/#/en_US_01). See EX1048, ¶¶5-6, p. 97. In the middle of Intel's homepage, there is the text "About Intel" which opens a drop-down box that includes the text "Press," which navigates to

[http://www.intel.com/pressroom/index.htm?iid=gg\\_about+intel\\_pressroom](http://www.intel.com/pressroom/index.htm?iid=gg_about+intel_pressroom). Page 96 of EX1048 is the Internet Archive's archived capture of that webpage as it existed March 6, 2010, as reflected in the Internet Archive's extended URL:

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<sup>43</sup> Wikipedia, Intel Developer Forum,

[https://en.wikipedia.org/wiki/Intel\\_Developer\\_Forum](https://en.wikipedia.org/wiki/Intel_Developer_Forum) (last visited Dec. 20, 2022)

[https://web.archive.org/web/20100306035503/http://www.intel.com/pressroom/index.htm?iid=gg\\_about+intel\\_pressroom](https://web.archive.org/web/20100306035503/http://www.intel.com/pressroom/index.htm?iid=gg_about+intel_pressroom). See EX1048, ¶¶5-6, p. 95.

178. At the left of Intel’s press room webpage there is the text “Innovation@Intel,” which navigates to [http://www.intel.com/pressroom/innovation/innovation.htm?iid=pr1\\_ln\\_innovation](http://www.intel.com/pressroom/innovation/innovation.htm?iid=pr1_ln_innovation). Pages 90-94 of EX1048 is the Internet Archive’s archived capture of that webpage as it existed February 27, 2010, as reflected in the Internet Archive’s extended URL:

[https://web.archive.org/web/20100227023739/http://www.intel.com/pressroom/innovation/innovation.htm?iid=pr1\\_ln\\_innovation](https://web.archive.org/web/20100227023739/http://www.intel.com/pressroom/innovation/innovation.htm?iid=pr1_ln_innovation). See EX1048, ¶¶5-6, p. 89.

179. On the left of that webpage there is the text “Press Kits,” which navigates to <http://lz1.intel.com/appzone/pressroom/PressReleases.asp?ReleaseType=VPK>. Pages 87-88 of EX1048 is the Internet Archive’s archived capture of that webpage as it existed March 9, 2010, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20100309202006/http://lz1.intel.com/appzone/pressroom/PressReleases.asp?ReleaseType=VPK>. See EX1048, ¶¶5-6, p. 86.

180. Under the heading “Services” of that webpage there is a hyperlink with the text “PRESS KIT - Intel Developer Forum (IDF) San Francisco 2009” which navigates to

[http://www.intel.com/pressroom/kits/events/idffall\\_2009/index.htm](http://www.intel.com/pressroom/kits/events/idffall_2009/index.htm). Pages 84-85 of EX1048 is the Internet Archive's archived capture of that webpage as it existed September 23, 2009, as reflected in the Internet Archive's extended URL: [https://web.archive.org/web/20090923235718/http://www.intel.com/pressroom/kits/events/idffall\\_2009/index.htm](https://web.archive.org/web/20090923235718/http://www.intel.com/pressroom/kits/events/idffall_2009/index.htm). See EX1048, ¶¶5-6, p. 83.

181. Towards the bottom left of that page under the heading "Press Materials" there is a hyperlink with the text "Intel Developer Forum 22nm News Facts (PDF 70KB)," which navigates to a PDF of a document that the Internet Archive captured on October 7, 2009, as reflected in the Internet Archive's extended URL:

[https://web.archive.org/web/20091007000925/http://download.intel.com/pressroom/kits/events/idffall\\_2009/pdfs/22nm\\_factsheet.pdf](https://web.archive.org/web/20091007000925/http://download.intel.com/pressroom/kits/events/idffall_2009/pdfs/22nm_factsheet.pdf). That PDF, which is on page 80 of EX1047, is EX1126. See also EX1047, ¶¶5-6, p. 79.

182. Based on the above evidence, it is my opinion that EX1126 was publicly accessible before the June 15, 2010 filing date for U.S. Appl. No. 12/816,201 (challenged patent, code (63)) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by October 7, 2009.

**42. Public Accessibility of EX1137 (“TSMC 40nm Press Release 2”)**

183. EX1137 is a press release by TSMC titled “TSMC Ramps 40nm Volume Production to Promote Innovation as Foundries Assume a Larger Role for \$300 Billion Industry.” The face of EX1137, states that it was “Issued by: TSMC” and “Issue on: 2008/11/17,” which indicates it was published by TSMC on November 17, 2008. I retrieved EX1137 from the Internet Archive’s Wayback Machine at the following extended URL, which indicates EX1137, is a copy of the press release as it existed on March 18, 2009, as reflected in the Internet Archive’s extended URL:

<https://web.archive.org/web/20090318021909/http://www.tsmc.com/tsmcdotcom/PRListingNewsArchivesAction.do?action=detail&newsid=3222&language=E>. *See, e.g.,* EX1029, ¶5. Additionally, Internet search engines (e.g., Google, Yahoo, etc.) would have had access to the same webpages using the same type of crawler software that the Internet Archive used to capture the archived pages (*see* §I.A above), such that a POSA interested in the computing industry, could have located EX1137 by searching the Web for keywords of interest such as “TSMC,” “semiconductor foundry,” and “40nm process,” which are terms that appear in EX1137 and would be terms of interest to a POSA interested in the computing industry.

184. Based on the above evidence and my review of the indicia appearing on the face of EX1137, it is my opinion that EX1137 is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by March 18, 2009.

**43. Public Accessibility of EX1034 (“Tong”)**

185. EX1034 (which I refer to herein as “Tong”) is titled “Reducing Power by Optimizing the Necessary Precision/Range of Floating-Point Arithmetic.” As indicated on page 273 of EX1034, Tong was published by the IEEE and bears a copyright “© 2000 IEEE,” which indicates it was published in the year 2000. Testimony from an IEEE representative demonstrates public accessibility of EX1034 no later than the last date of June 2000. *See* EX1035, ¶¶6-11; *see* EX1035, Exhibit A (showing IEEE Xplore information for this exhibit). Based on the above evidence, I conclude that Tong would have been publicly accessible to a POSA exercising reasonable diligence in 2000.

**44. Public Accessibility of EX1036 (“Shirazi”)**

186. EX1036 (which I refer to herein as “Shirazi”) is titled “Quantitative Analysis of Floating Point Arithmetic on FPGA Based Custom Computing Machines.” As indicated on page 155 of EX1036, Shirazi was published by the IEEE and bears a copyright “© 1995 IEEE,” which indicates it was published in

the year 1995. Testimony from an IEEE representative demonstrates public accessibility of EX1036 no later than April 21, 1995. *See* EX1037, ¶¶6-11; *see* EX1037, Exhibit A (showing IEEE Xplore information for this exhibit). Based on the above evidence, I conclude that Shirazi would have been publicly accessible to a POSA exercising reasonable diligence in 1995.

**45. Public Accessibility of EX1092 (“Aty”)**

187. EX1092 (which I refer to herein as “Aty”) is titled “High-Speed, Area-Efficient FPGA-Based Floating-Point Multiplier.” As indicated on page 274 of EX1092, Aty was published in connection with the ICM 2003 conference on December 9-11 in Cairo, Egypt, indicating it was publicly available in the year 2003. Testimony from an IEEE representative demonstrates public accessibility of EX1092 no later than December 11, 2003. *See* EX1093, ¶¶6-11; *see* EX1093, Exhibit A (showing IEEE Xplore information for this exhibit). Based on the above evidence, I conclude that Aty would have been publicly accessible to a POSA exercising reasonable diligence in 2003.

**46. Public Accessibility of EX1138 (“Thornton”)**

188. EX1138 (which I refer to herein as “Thornton”) is titled “Tradeoff analysis of integer multiplier circuits implemented in FPGAs.” As indicated on the face of EX1138, Thornton was published by the IEEE in connection with the 1999 IEEE Pacific Rim Conference on Communications, Computers and Signal

Processing (PACRIM 1999). I have reviewed Thornton, which appears to be a library scan of a physical copy of the issue of the journal that contained Thornton. Page 2 of EX1138 bears a “Copyright © 1999 by The Institute of Electrical and Electronics Engineers, Inc.” an “ISBN” number a stamp from the University of Wisconsin - Madison. Page 301 of Thornton bears a Copyright “© 1999 IEEE,” which indicates it was published in 1999. IEEE Xplore indicates that Thornton had a “Date Added to IEEE Xplore” of August 6, 2002.<sup>44</sup> *See* Bolin, ¶18 (identifying IEEE Xplore as “a well-known and widely used resource for researchers, educators, and professionals in the fields of electrical engineering, computer science, and related disciplines”). Based on the above evidence and my review of the indicia appearing on the Thornton document and my understanding of the IEEE and IEEE Xplore, it is my opinion that Thornton is prior art to the challenged patent because it was publicly accessible before the earliest possible priority date for the challenged patent (June 19, 2009) by being disseminated or otherwise made available to POSAs exercising reasonable diligence at least by August 6, 2002. *See also* Bolin, ¶¶86-90 (concluding that the Thornton article “was publicly accessible by August 2002 and could have been located by any

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<sup>44</sup> <https://ieeexplore.ieee.org/document/799536>

member of the public interested in the subject matter by exercising reasonable diligence, on their own or with the assistance of a research librarian”).