

Paper No. ____

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC,
Petitioner,

v.

SINGULAR COMPUTING LLC,
Patent Owner.

Case No. IPR2023-00395
Patent No. 10,754,616

JOINT MOTION TO TERMINATE PROCEEDING

LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 10,754,616
1002	Prosecution History of U.S. Patent No. 10,754,616
1003	Declaration of Paul Franzon, PhD.
1004	Curriculum Vitae of Paul Franzon, PhD.
1005	Declaration of Dr. Mary K. Bolin
1006	PCT Publication WO2005/037326A2 (“Stuttard”)
1007	Schmidt et al., “KPROC - An Instruction Systolic Architecture for Parallel Prefix Applications,” Parallel and Distributed Computing Practices Vol. 3, No. 2, pp. 163–178 (2000) (“Schmidt-2000”)
1008	Schimmler et al., “A bit-serial floating-point unit for a massively parallel system on a chip,” in Parallel Algorithms and Applications, 19:2-3, 79-95 (2004)
1009	Schmidt et al., “A Parallel Accelerator Architecture for Multimedia Video Compression,” in Euro-Par’99, Lecture Notes in Computer Science 1685, Springer Verlag, 1999, pp. 950–960 (“Schmidt-1999”)
1010	Schimmler et al., “The Instruction Systolic Array – Implementation of a Low-Cost Parallel Architecture as Add-On Board for Personal Computers,” High Performance Computing and Networking, Lecture Notes in Computer Science 797, Springer Verlag, 1994, pp. 487–488 (“Schimmler-1994”)
1011	Schimmler et al., “The Instruction Systolic Array in Image Processing Applications,” Vision Systems: Sensors, Sensor systems, and Components, Europto 96, pp. 136–144 (“Schimmler-1996”)
1012	Yeh et al., “Parallax: An architecture for real-time physics,” the 34th International Symposium on Computer Architecture (ISCA), 2007, pp. 232-243 (“Yeh-ISCA07”)
1013	Yeh et al., “The Art of Deception: Adaptive Precision Reduction for Area Efficient Physics Acceleration,” 40th IEEE/ACM International Symposium on Microarchitecture (MICRO’07), 2007, pp. 394-406 (“Yeh-Micro07”)
1014	Yeh et al., “Fool me twice: Exploring and exploiting error tolerance in physics-based animation” (2007)
1015	U.S. Patent No. 5,355,508 (“Kan”)
1016	G.E. Moore, “Cramming More Components onto Integrated Circuits,” Proceedings of the IEEE, Vol. 86, No. 1 (January 1998)

Exhibit	Description
1017	IEEE SSCS Newsletter 36-37 (reprinting Moore, “Progress in Digital Integrated Electronics,” International Electron Devices Meeting, IEEE, 1975, pp. 11-13).
1018	<i>Microprocessor Report</i> , “Mendocino Improves Celeron,” Volume 12, Number 11, August 24, 1998
1019	Sim et. al, “MIMD-SIMD hybrid system—towards a new low cost parallel system,” <i>Parallel Computing</i> 29 (2003) pp. 21-36 (“Sim”)
1020	Taveniku et. al. “The VEGA Moderately Parallel MIMD, Moderately Parallel SIMD, Architecture for High Performance Array Signal Processing,” <i>Proceedings of IPPS/SPDP’98</i> (IEEE Computer Society), pp 226-232 (“Taveniku”).
1021	The National Technology Roadmap for Semiconductors, 1997 Edition (“NTRS-1997”)
1022	International Technology Roadmap for Semiconductor, 1999 Edition (“ITRS-1999”)
1023	International Technology Roadmap for Semiconductors, 2000 Update (“ITRS-2000”) (from Exhibit B, Folders 1-2 of the Declaration of Nathaniel E Frank-White, EX1029)
1024	International Technology Roadmap for Semiconductor, 2002 Update (“ITRS-2002”) (from Exhibit B, Folders 3-7 of the Declaration of Nathaniel E Frank-White, EX1029)
1025	International Technology Roadmap for Semiconductors, 2004 Update (“ITRS-2004”) (from Folders 8-11 of the Declaration of Nathaniel E Frank-White, EX1029)
1026	International Technology Roadmap for Semiconductors, 2007 Edition (“ITRS-2007”) (from Folders 12-13 of the Declaration of Nathaniel E Frank-White, EX1029)
1027	International Technology Roadmap for Semiconductors, 2009 Edition (“ITRS-2009”) (from Folders 14-15 of the Declaration of Nathaniel E Frank-White, EX1029)
1028	International Technology Roadmap for Semiconductors, 2010 Update (“ITRS-2010”) (from Folder 16 of the Declaration of Nathaniel E Frank-White, EX1029)
1029	Declaration of Nathaniel E Frank-White (November 30, 2022) (ITRS)
1030	International Technology Roadmap for Semiconductor, 2001 Edition (“ITRS-2001”)
1031	Declaration of Nathaniel E Frank-White (November 30, 2022) (Schmidt)

Exhibit	Description
1032	Declaration of Nathaniel E Frank-White (November 30, 2022) (Yeh)
1033	Gargini, “The International Technology Roadmap for Semiconductors (ITRS): Past, present and future,” GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuits Symposium. 22nd Annual Technical Digest 2000
1034	Tong et al., “Reducing Power by Optimizing the Necessary Precision/Range of Floating-Point Arithmetic,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 3, June 2000 (“Tong”) (from pages 6-19 of the Declaration of Gerard P. Grenier, EX1035)
1035	Declaration of Gerard P. Grenier regarding Tong et al., Reducing Power by Optimizing the Necessary Precision/Range of Floating-Point Arithmetic, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 3, June 2000
1036	Shirazi et al., “Quantitative Analysis of Floating Point Arithmetic on FPGA Based Custom Computing Machines,” Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, April 19-21, 1995 (“Shirazi”) (from pages 6-13 of Declaration of Gordon MacPherson, EX1037)
1037	Declaration of Gordon MacPherson regarding Shirazi et al., Quantitative Analysis of Floating Point Arithmetic on FPGA Based Custom Computing Machines, Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, April 19-21, 1995
1038	Altera Product Catalog (2008) (from pages 82-153 of Declaration of Nathaniel E Frank-White, EX1047)
1039	Stackhouse et al., “A 65 nm 2-Billion Transistor Quad-Core Itanium Processor,” in IEEE Journal of Solid-State Circuits, vol. 44, no. 1, pp. 18-31, Jan. 2009 (“Intel-Itanium”)
1040	Dell White Paper, “Performance Analysis of Intel® Pentium® M and Pentium 4 Processors,” July 2005. (“Pentium-4”) (from pages 61-65 of Declaration of Nathaniel E Frank-White, EX1047)
1041	The Guru of 3D Report on Radeon HD Series 5700 (“Radeon-5700”) (from pages 10-11 of Declaration of Nathaniel E Frank-White, EX1047)
1042	“Intel Core 2 Extreme QX9650 – Penryn Ticks Ahead,” Anandtech.com (Oct. 29, 2007) (from pages 30-40 of Declaration of Nathaniel E Frank-White, EX1047)

Exhibit	Description
1043	TSMC Report (2008), “TSMC Ramps Most Advanced Available Process Technology to Volume Production” (pr.tsmc.com/english/news/1526) (“TSMC-40nm”)
1044	“Updated CPU Cheatsheet – Seven Years of Covert CPU Operations,” Anandtech.com (Aug. 28, 2004) (from pages 42-49 of Declaration of Nathaniel E Frank-White, EX1047)
1045	Natarajan et al., “A 32nm logic technology featuring 2nd-generation high-k + metal-gate transistors, enhanced channel strain and 0.171 μ m ² SRAM cell size in a 291Mb array,” 2008 IEEE International Electron Devices Meeting, 2008
1046	RESERVED – NOT USED
1047	Declaration of Nathaniel E Frank-White (December 10, 2022) (742000)
1048	Declaration of Nathaniel E Frank-White (December 12, 2022) (744136)
1049	PCT Publication WO2002/065700A2
1050	UK Patent Appl. Publ. No. GB 2,415,561
1051	UK Patent Appl. Publ. No. GB 2,390,506
1052	“Intel’s 32nm Update: The Follow-on to Core i7 and More,” Anandtech.com (Feb. 11, 2009) (from pages 21-28 of Declaration of Nathaniel E Frank-White, EX1047)
1053	“AMD Evergreen: 40nm DirectX 11 GPU Silicon Arrives,” Anandtech.com (June 3, 2009) (from pages 16-19 of Declaration of Nathaniel E Frank-White, EX1047)
1054	U.S. Patent Appl. Publ. No. 2007/0258641A1
1055	U.S. Provisional Application No. 61/218691
1056	RESERVED – NOT USED
1057	RESERVED – NOT USED
1058	U.S. Patent Appl. Publ. No. 2003/0033509A1
1059	U.S. Patent Appl. Publ. No. 2008/0288823A1
1060	RESERVED – NOT USED
1061	RESERVED – NOT USED
1062	RESERVED – NOT USED
1063	U.S. Patent Appl. Publ. No. 2009/0148068A1
1064	RESERVED – NOT USED
1065	RESERVED – NOT USED
1066	U.S. Patent Appl. Publ. No. 2009/0114952A1
1067	U.S. Patent Appl. Publ. No. 2006/0088958A1
1068	U.S. Patent Appl. Publ. No. 2008/0023700A1
1069	U.S. Patent Appl. Publ. No. 2009/0150112A1

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1070	U.S. Patent Appl. Publ. No. 2005/0237327A1
1071	RESERVED – NOT USED
1072	RESERVED – NOT USED
1073	RESERVED – NOT USED
1074	RESERVED – NOT USED
1075	U.S. Patent No. 5,226,142
1076	U.S. Patent No. 6,681,059
1077	U.S. Patent No. 7,243,165 (“Kravec”)
1078	U.S. Patent No. 7,072,872 (“Caid”)
1079	RESERVED – NOT USED
1080	U.S. Patent No. 6,963,891
1081	U.S. Patent No. 6,825,857
1082	U.S. Patent No. 6,353,867
1083	U.S. Patent No. 6,477,610
1084	U.S. Patent No. 5,581,773
1085	RESERVED – NOT USED
1086	RESERVED – NOT USED
1087	RESERVED – NOT USED
1088	VSI Alliance™: Virtual Component Interface Standard Version 2 (OCB 2 2.0) (April 2001)
1089	“Port,” in Microsoft Computer Dictionary, p. 412 (5th. ed. 2002)
1090	RESERVED – NOT USED
1091	RESERVED – NOT USED
1092	Aty et al., “High-Speed, Area-Efficient FPGA-Based Floating-Point Multiplier,” Proceedings of the 12 IEEE International Conference on Fuzzy Systems, December 11, 2003 (“Aty”) (from p. 14-17 of Declaration of Gordon MacPherson, EX1093)
1093	Declaration of Gordon MacPherson regarding Aty et al., High-Speed, Area-Efficient FPGA-Based Floating-Point Multiplier, Proceedings of the 12 IEEE International Conference on Fuzzy Systems, December 11, 2003
1094	Chen et al., “A cost effective 32nm high-K/ metal gate CMOS technology for low power applications with single-metal/gate-first process,” 2008 Symposium on VLSI Technology, 2008, pp. 67-68
1095	Prosecution History of PCT/GB2004004377
1096	U.S. Patent No. 4,450,402
1097	Schiml et al., “A 0.13 μm CMOS platform with Cu/low-k interconnects for system on chip applications,” 2001 Symposium on

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	VLSI Technology. Digest of Technical Papers (IEEE Cat. No.01 CH37184), 2001, pp. 101-102
1098	Sudha et al., “An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation,” IETE Journal of Research, Vol. 53, No. 5, September-October 2007, ISSN 0377-2063, pp. 425-431 (“Sudha”)
1099	RESERVED – NOT USED
1100	Oh et al., “A fully pipelined single-precision floating-point unit in the synergistic processor element of a CELL processor,” in IEEE Journal of Solid-State Circuits, vol. 41, no. 4, pp. 759-771, April 2006,
1101	RESERVED – NOT USED
1102	RESERVED – NOT USED
1103	Prabhu, “SOMGPU: An unsupervised pattern classifier on Graphical Processing Unit,” 2008 IEEE Congress on Evolutionary Computation (IEEE World Congress on Computational Intelligence), 2008, pp. 1011-1018
1104	Poli et al., “Processing Neocognitron of Face Recognition on High Performance Environment Based on GPU with CUDA Architecture,” 2008 20th International Symposium on Computer Architecture and High Performance Computing, 2008, pp. 81-88
1105	Ligon et al., “A re-evaluation of the practicality of floating-point operations on FPGAs,” Proceedings. IEEE Symposium on FPGAs for Custom Computing Machines (Cat. No.98TB100251), 1998, pp. 206-215
1106	Held, “From a Few Cores to Many: A Tera-scale Computing Research Overview,” white paper, Intel, 2006 (from pages 67-78 of Declaration of Nathaniel E Frank-White, EX1047)
1107	Reddaway et al., “Ultra-high performance, low-power, data parallel radar implementations,” IEEE International Radar Conference, 2005., 2005, pp. 822-826
1108	Lokhmotov et al., “Revisiting SIMD Programming,” Languages and Compilers for Parallel Computing: 20th International Workshop, LCPC 2007, Urbana, IL, USA, October 11-13, 2007, Revised Selected Papers. Springer-Verlag, Berlin, Heidelberg, 32–46
1109	U.S. Patent No. 4,534,010
1110	Shahbahrami et al., “Optimization of Content-Based Image Retrieval Functions,” 2008 Tenth IEEE International Symposium on Multimedia, 2008, pp. 607-612

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1111	Noumsi et al., “Acceleration of a content-based image-retrieval application on the RDISK cluster,” Proceedings 20th IEEE International Parallel & Distributed Processing Symposium, 2006
1112	Proceedings 20th IEEE International Parallel & Distributed Processing Symposium, 2006 (TOC)
1113	Pengdong et al., “Performance Comparison between Color and Spatial Segmentation for Image Retrieval and Its Parallel System Implementation,” 2008 International Symposium on Computer Science and Computational Technology, 2008, pp. 539-543
1114	Bradley et al., “Exploiting Loop-Level Parallelism for SIMD Arrays Using OpenMP,” 89-100 (2007) (attachment 13c to Declaration of Dr. Mary K. Bolin, EX1005)
1115	Haran et al., “22 nm technology compatible fully functional 0.1 μm^2 6T-SRAM cell,” 2008 IEEE International Electron Devices Meeting, 2008, pp. 1-4
1116	Tong et al., Sean & Hahn, Scott. (2008). Operating System Support for Shared-ISA Asymmetric Multi-core Architectures.
1117	Borkar, “Thousand Core Chips A Technology Perspective,” Proceedings of the 44th ACM/IEEE Design Automation Conference, pp. 746-749 (2007) (attachment 11b to Declaration of Dr. Mary K. Bolin, EX1005)
1118	“ClearSpeed kicks it up a notch,” Arstechnica.com (Oct. 11, 2004) (from pages 5-6 of Declaration of Nathaniel E Frank-White, EX1123)
1119	U.S. Patent No. 7,447,873
1120	Manocha, “General-purpose computations using graphics processors,” in Computer, vol. 38, no. 8, pp. 85-88, Aug. 2005
1121	RESERVED – NOT USED
1122	U.S. Patent Appl. Publ. No. 2009/0183167A1
1123	Declaration of Nathaniel E Frank-White (December 12, 2022)
1124	Burger et al., “Composable Multicore Chips,” in Multicore Processors and Systems. Integrated Circuits and Systems (Springer 2009)
1125	Roma et al., “In the development and evaluation of specialized processors for computing high-order 2-D image moments in real-time,” in Proceedings Fifth IEEE International Workshop on Computer Architectures for Machine Perception, pp. 170-179 (2000)
1126	“Intel Developer Forum 22nm News Facts,” Intel Corporation (Sept. 22, 2009) (from page 80 of Declaration of Nathaniel E Frank-White, EX1047)
1127	Declaration of Gordon MacPherson regarding EX1013

Exhibit	Description
1128	Declaration of Gordon MacPherson regarding EX1039
1129	Declaration of Gordon MacPherson regarding EX1045
1130	Declaration of Gordon MacPherson regarding EX1094
1131	Declaration of Gordon MacPherson regarding EX1097
1132	RESERVED – NOT USED
1133	Declaration of Gordon MacPherson regarding EX1100
1134	Declaration of Gordon MacPherson regarding EX1110
1135	Declaration of Gordon MacPherson regarding EX1115
1136	Declaration of Gordon MacPherson regarding EX1125
1137	TSMC Press Release, “TSMC Ramps 40nm Volume Production to Promote Innovation as Foundries Assume a Larger Role for \$300 Billion Industry” (Nov. 17, 2008)
1138	Thornton et al., “Tradeoff analysis of integer multiplier circuits implemented in FPGAs,” in 1999 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing (PACRIM 1999). Conference Proceedings (Cat. No.99CH36368), 1999, pp. 301-304
1139	Amended Complaint for Patent Infringement, <i>Singular Computing LLC v. Google LLC</i> , 1:21-cv-12110 (D. Mass. Mar. 10, 2022)
1140	Settlement Agreement [CONFIDENTIAL]

Pursuant to 35 U.S.C. § 317, 37 C.F.R § 42.74, and the authorization provided by the Board on March 1, 2024, Petitioner Google LLC (“Petitioner”) and Patent Owner Singular Computing LLC (“Patent Owner”) jointly request termination of this proceeding, IPR2023-00395, directed to U.S. Patent No. 10,754,616 (“the ’616 patent”).

Petitioner and Patent Owner have settled their dispute regarding the ’616 patent, including both this proceeding and Patent Owner’s assertion of the ’616 patent in the related district court litigation, Civil Action No. 1:19-cv-12551 FDS (D. Mass.). The parties do not anticipate further litigation between them concerning the ’616 patent.

Good cause exists to terminate this proceeding because the parties have settled their dispute regarding the ’616 patent and the proceeding is still at an early stage. Terminating the proceeding now would thus serve the interests of judicial economy as well as the mutual interest of the parties.

A true and correct copy of the parties’ settlement agreement in writing is being filed as Exhibit 1140, along with a joint motion to treat the settlement agreement as business confidential information.

Respectfully submitted,

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March 7, 2024

CERTIFICATE OF SERVICE UNDER 37 C.F.R. § 42.6 (E)(4)

I certify that on March 7, 2024, I will cause a copy of the foregoing document, including any exhibits filed therewith, to be served via electronic mail, as previously consented to by Patent Owner, upon the following:

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