AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Massachusetts on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
1:21-cv-12110	12/22/2021	Massachusetts

PLAINTIFF	DEFENDANT
Singular Computing LLC	Google LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	10,754,616	8/25/2020	Joseph Bates
2	11,169,775	11/9/2021	Joseph Bates
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

Google Exhibit 1002
Google v. Singular

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	11/09/2021	11169775	SNG.1001C9	3296

144359 7590 10/20/2021

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Joseph Bates, Newton, MA;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Singular Computing LLC, Newton, MA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :C46167

Sale Accounting Date:09/30/2021

Sale Item Reference Number	Effective Date
16882694	09/29/2021

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20219T812371715	1501	UTILITY APPL ISSUE FEE	$1,000.00	Salea
I20219T812371715	1501	UTILITY APPL ISSUE FEE	$200.00	Deposit Account

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

144359 7590 09/27/2021

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Cambridge, MA 02142

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Kim Hauser	(Typed or printed name)
/Kim Hauser/	(Signature)
September 29, 2021	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

TITLE OF INVENTION: PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$1000.00	$200	12/27/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
YAARY, MICHAEL D	2182	708-524000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 BLUESHIFT IP LLC
2 ROBERT PLOTKIN
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SINGULAR COMPUTING LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): NEWTON, MASSACHUSETTS

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ☒ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 60/1293

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
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NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Robert Plotkin/ Date September 29, 2021

Typed or printed name Robert Plotkin Registration No. 43861

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

ATTORNEY'S DOCKET NO: SNG.1001C9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	16/882,694
Confirmation No.:	3296
Title:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Inventor:	Bates, Joseph
Filing Date:	05/25/2020
Examiner:	MICHAEL D YAARY
Art Unit:	2182

REQUEST TO APPLY PREVIOUSLY-PAID FUNDS

In response to the Notice of Allowance mailed September 27, 2021, Applicant respectfully requests the Office apply previously-paid funds to complete the $1,200 issue fee payment requirement for the above-mentioned application.

Itemization of fees previously paid by the Applicant are shown on the table below:

Date of Payment	Fee Code	Fee Amount	Amount Paid	Method of Payment
07-16-2021	1501	$200.00	$200.00	Method of Payment: Deposit Account DA601293
07-16-2021	1501	$1,000.00	$1,000.00	Method of Payment: Deposit Account DA601293

CONCLUSIONS

If this Request is deficient in any way, Applicant hereby authorizes the Office to charge any fees or make any credits, to Deposit Account No. 60/1293.

Respectfully submitted,

/Robert Plotkin/ September 29, 2021

Robert Plotkin, Esq.
Reg. No. 43861

Blueshift IP LLC,
1 Broadway, 14th Floor,
Cambridge, MA 02142
Tel: (617) 207-6141
Fax: (617) 207-6215

Date

Electronic Acknowledgement Receipt

EFS ID:	43904168
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	29-SEP-2021
Filing Date:	25-MAY-2020
Time Stamp:	16:42:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	SNG-1001C9_Issue_Fee_Transmittal.pdf	147244 180abcebaddc0b125fb73262a0bd6dfc85ab2742	no	1

Warnings:

Information:					
2	Fee Worksheet (SB06)	SNG-1001C9_Request_to_Apply_Funds.pdf	85540 c6fb3e25f2a0ac43df30e050ceaafecb702d97a6	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	232784	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Best Available Copy

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
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144359 7590 09/27/2021
Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142



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Kim Hauser	(Typed or printed name)
/Kim Hauser/	(Signature)
September 29, 2021	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

TITLE OF INVENTION: PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$1000.00	$200	12/27/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
YAARY, MICHAEL D	2182	708-524000

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1 BLUESHIFT IP LLC
2 ROBERT PLOTKIN
3

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4a. Fees submitted: ☒ Issue Fee ☒ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

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5. **Change in Entity Status** (from status indicated above)

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Authorized Signature /Robert Plotkin/ Date September 29, 2021

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PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

144359 7590 09/27/2021

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

EXAMINER	
YAARY, MICHAEL D	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/27/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

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nonprovisional	UNDISCOUNTED	$1200	$0.00	$1000.00	$200	12/27/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

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Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Google Ex. 1002 - Page 11

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
YAARY, MICHAEL D	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 09/27/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/882,694	Applicant(s) Bates, Joseph	
	Examiner MICHAEL D YAARY	Art Unit 2182	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 08/10/2021.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-24 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 08/10/2021 and 09/14/2021.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MICHAEL D. YAARY/
Primary Examiner, Art Unit 2182

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	Art Unit
	MICHAEL D YAARY	2182

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	Art Unit
	MICHAEL D YAARY	2182

Search Notes		
Search Notes	**Date**	**Examiner**
EAST search with keywords	07/23/2020	MY
NPL search	07/23/2020	MY
Inventor name search	07/23/2020	MY
EAST search with keywords in combination with CPC classes	08/18/2020	MY
IPR2021-00154 Reviewed Inter Partes Review of U.S. Patent No. 10,416,961	07/06/2021	MY
IPR2021-00155 Reviewed Inter Partes Review of U.S. Patent No. 10,416,961 on 07/06/2021	07/06/2021	MY
IPR2021-00164 Reviewed Inter Partes Review of U.S. Patent No. 9,218,156 on 07/06/2021	07/06/2021	MY
IPR2021-00165 Reviewed Inter Partes Review of U.S. Patent No. 9,218,156 on 07/06/2021	07/06/2021	MY
IPR2021-00178 Reviewed Inter Partes Review of U.S. Patent No. 8,407,273 on 07/06/2021	07/06/2021	MY
IPR2021-00179 Reviewed Inter Partes Review of U.S. Patent No. 8,407,273 on 07/06/2021	07/06/2021	MY
IDS filed 08/10/2021 and 09/14/2021 considered	09/20/2021	MY

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
G06F	7/483	08/18/2020	MY

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/23/2020	08/18/2020	07/06/2021	09/20/2021					
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4	4	✓	=	=	=					
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6	6	✓	=	=	=					
7	7	✓	=	=	=					
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23	23	✓	=	=	=					
24	24	✓	=	=	=					

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

CPC							
Symbol						**Type**	**Version**
G06F	/	7	/	483		F	2013-01-01
G06F	/	7	/	38		I	2013-01-01
H03K	/	19	/	17728		I	2013-01-01
G06F	/	7	/	5235		I	2013-01-01
G06F	/	7	/	4833		I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	24	
/MICHAEL D. YAARY/ Primary Examiner, Art Unit 2182	20 September 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20210920

Google Ex. 1002 - Page 18

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	Art Unit
	MICHAEL D YAARY	2182

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G06F7/483	/	7	/	483
G06F7/38	/	7	/	38
H03K19/17728	/	19	/	17728
G06F7/523	/	7	/	523

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 24	
/MICHAEL D. YAARY/ Primary Examiner, Art Unit 2182 (Primary Examiner)	20 September 2021 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

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Google Ex. 1002 - Page 19

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	Art Unit
	MICHAEL D YAARY	2182

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10	19	19										
2	2	11	11	20	20										
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4	4	13	13	22	22										
5	5	14	14	23	23										
6	6	15	15	24	24										
7	7	16	16												
8	8	17	17												
9	9	18	18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	24	
/MICHAEL D. YAARY/ Primary Examiner, Art Unit 2182	20 September 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

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PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16882694
Filing Date	2020-05-25
First Named Inventor	Joseph Bates
Art Unit	2182
Examiner Name	MICHAEL D YAARY
Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/MY/	1	10754616		2020-08-25	JOSEPH BATES	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

/MY/	1	MAKINO et al., 'An 8.8-ns 54><54-Bit Multiplier with High Speed Redundant Binary Architecture", IEEE Journal of Solid State Circuits, Vol. 31, No. 6, June 1996, pp. 773-783.
/MY/	2	MCCALLUM, IAN D., "Intel QuickAssist Technology: FSB-FPGA Accelerator Architecture", QATS0002, Intel Developer Forum, Copyright 2007 Intel Corporation, 27 pages.
/MY/	3	STRZODKA et al., "Pipelined Mixed Precision Algorithms on FPGAs for Fast and Accurate PDE Solvers from Low Precision Components", Extended technical report, Original in IEEE Proceedings on Field-Programmable Custom Computing Machines, 2006,13 pages.

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EXAMINER SIGNATURE

Examiner Signature	/MICHAEL D. YAARY/	Date Considered	09/20/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature		Date (YYYY-MM-DD)	
Name/Print	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1					

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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	Attorney Docket Number	SNG.1001C9

/MY/	1	HAMMERSTROM, D., "Neural networks at work," IEEE Spectrum, pp. 26-32, June 1993, obtained from IEEE Xplore on April 9, 2020, 7 pages.	
/MY/	2	HAMMERSTROM, D., "Working with neural networks," IEEE Spectrum, pp. 46-53, July 1993, obtained from IEEE Xplore on April 9, 2020, 8 pages.	
/MY/	3	KINSER, J. and LINDBLAD, T., "Implementation of Pulse-Coupled Neural Networks in a CNAPS Environment," IEEE Transactions on Neural Networks, Vol. 10, No. 3, pp. 584-590, June 1999.	
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	Attorney Docket Number	SNG.1001C9

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	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

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First Named Inventor/Applicant Name:	Joseph Bates
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53	Non Patent Literature	SNG-1001C9-A-NPL-046.pdf	2453068 7b761f12f475a573b1474360cc87e280dd87c3c8	no	11
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55	Non Patent Literature	SNG-1001C9-A-NPL-048.pdf	1412346 025443052b51ee04017f3657a1a8cbdd09a9e332	no	8
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57	Non Patent Literature	SNG-1001C9-A-NPL-038-pages-001-154.pdf	18159364 4c4d98b5459903b7a5f65dad8cc0b9123094beaa	no	154
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58	Non Patent Literature	SNG-1001C9-A-NPL-038-pages-155-308.pdf	16777536 c748af5d7cac15565cb689890d0f634907aeaa4a	no	154
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(Not for submission under 37 CFR 1.99)

Application Number	16882694
Filing Date	2020-05-25
First Named Inventor	Joseph Bates
Art Unit	2182
Examiner Name	MICHAEL D YAARY
Attorney Docket Number	SNG.1001C9

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	12	WAWRZYNEK et al., "SPERT-II: A Vector Microprocessor System and its Application to Large Problems in Backpropogation Training," Computer, Vol. 29, No. 3, pp. 79-86, March 1996.	
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	First Named Inventor	Joseph Bates
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	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

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	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2021-09-14
Name/Print	Robert Plotkin	Registration Number	43861

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Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	14-SEP-2021
Filing Date:	25-MAY-2020
Time Stamp:	12:28:34
Application Type:	Utility under 35 USC 111(a)

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(Not for submission under 37 CFR 1.99)

Application Number	16882694
Filing Date	2020-05-25
First Named Inventor	Joseph Bates
Art Unit	2182
Examiner Name	MICHAEL D YAARY
Attorney Docket Number	SNG.1001C9

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	4	5689677		1997-11-18	MACMILLAN DAVID C	
	5	5892962		1999-04-06	CLOUTIER	
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	1	20030204750		2003-10-30	NG JOSEPH S	
	2	20030204760		2003-10-30	YOUNGS LYNN R	
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OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2021-08-10
Name/Print	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	43469571
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	10-AUG-2021
Filing Date:	25-MAY-2020
Time Stamp:	12:43:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	SNG-1001C9_6th_Supp_IDS.pdf	1053554 fb350460d4d5633e1c8be7e1684b798dee0008f8	no	4

Warnings:

Information:					
2	Non Patent Literature	SNG-1001C9-NPL-001.pdf	2638111 a2b44e7e6414a69876b449d769a6e55769c498b5	no	11
Warnings:					
Information:					
3	Non Patent Literature	SNG-1001C9-NPL-003.pdf	454440 febadc3e171639ee337c34ec1a75cc42ff9bb568	no	13
Warnings:					
Information:					
4	Non Patent Literature	SNG-1001C9-NPL-002-.pdf	1312672 86a2a7208e6c7dfbaf4f51fb8d0042a330cf2a3f	no	27
Warnings:					
Information:					
		Total Files Size (in bytes):	5458777		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16/882,694	Filing Date	2020-05-25	Docket Number (if applicable)	SNG.1001C9	Art Unit	2182
First Named Inventor	Joseph Bates			Examiner Name	MICHAEL D YAARY		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☒ Other PETITION TO WITHDRAW AN APPLICATION FROM ISSUE AFTER PAYMENT OF THE ISSUE FEE UNDER 37 CFR 1.313(c)

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 601293

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2021-08-10
Name	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	10754616		2020-08-25	JOSEPH BATES	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	1	MAKINO et al., 'An 8.8-ns 54><54-Bit Multiplier with High Speed Redundant Binary Architecture", IEEE Journal of Solid State Circuits, Vol. 31, No. 6, June 1996, pp. 773-783.
	2	MCCALLUM, IAN D., "Intel QuickAssist Technology: FSB-FPGA Accelerator Architecture", QATS0002, Intel Developer Forum, Copyright 2007 Intel Corporation, 27 pages.
	3	STRZODKA et al., "Pipelined Mixed Precision Algorithms on FPGAs for Fast and Accurate PDE Solvers from Low Precision Components", Extended technical report, Original in IEEE Proceedings on Field-Programmable Custom Computing Machines, 2006,13 pages.

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature		Date (YYYY-MM-DD)	
Name/Print	Robert Plotkin	Registration Number	43861

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc Code: PET.AUTO Document Description: Petition automatically granted by EFS-Web	PTO/SB/140 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**PETITION TO WITHDRAW AN APPLICATION FROM ISSUE AFTER PAYMENT OF THE ISSUE FEE UNDER 37 CFR 1.313(c)**
Application Number	16882694
Filing Date	25-May-2020
First Named Inventor	Joseph Bates
Art Unit	2182
Examiner Name	
Attorney Docket Number	SNG.1001C9
Title	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

An application may be withdrawn from issue for further action upon petition by the applicant. To request that the Office withdraw an application from issue, applicant must file a petition under this section including the fee set forth in § 1.17(h) and a showing of good and sufficient reasons why withdrawal of the application from issue is necessary.

APPLICANT HEREBY PETITIONS TO WITHDRAW THIS APPLICATION FROM ISSUE UNDER 37 CFR 1.313(c).

A grantable petition requires the following items:
(1) Petition fee; and
(2) One of the following reasons:
(a) Unpatentability of one or more claims, which must be accompanied by an unequivocal statement that one or more claims are unpatentable, an amendment to such claim or claims, and an explanation as to how the amendment causes such claim or claims to be patentable;
(b) Consideration of a request for continued examination in compliance with § 1.114 (for a utility or plant application only); or
(c) Express abandonment of the application. Such express abandonment may be in favor of a continuing application, but not a CPA under 37 CFR 1.53(d).

Petition Fee

◯	Small Entity
◯	Micro Entity
◉	Regular Undiscounted

Reason for withdrawal from issue

◯ One or more claims are unpatentable ◉ Consideration of a request for continued examination (RCE) (List of Required Documents and Fees) ◯ Applicant hereby expressly abandons the instant application (any attorney/agent signing for this reason must have power of attorney pursuant to 37 CFR 1.32(b)).
RCE request,submission, and fee. ☐ I certify, in accordance with 37 CFR 1.4(d)(4) that : The RCE request ,submission, and fee have already been filed in the above-identified application on ☒ Are attached.
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ◉ An attorney or agent registered to practice before the Patent and Trademark Office who has been given power of attorney in this application. ◯ An attorney or agent registered to practice before the Patent and Trademark Office, acting in a representative capacity. ◯ A sole inventor ◯ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ◯ A joint inventor; all of whom are signing this e-petition

Signature	/Robert Plotkin/
Name	Robert Plotkin
Registration Number	43861

Electronic Patent Application Fee Transmittal

Application Number:	16882694
Filing Date:	25-May-2020
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Filer:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
PETITION FEE- 37 CFR 1.17(H) (GROUP III)	1464	1	140	140
RCE- 2ND AND SUBSEQUENT REQUEST	1820	1	2000	2000
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2140**

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Decision Date : August 10, 2021

In re Application of :

Joseph Bates

DECISION ON PETITION

UNDER CFR 1.313(c)(2)

Application No : 16882694

Filed : 25-May-2020

Attorney Docket No : SNG.1001C9

This is an electronic decision on the petition under 37 CFR 1.313(c)(2), filed August 10, 2021 , to withdraw the above-identified application from issue after payment of the issue fee.

The petition is **GRANTED.**

The above-identified application is withdrawn from issue for consideration of a submission under 37 CFR 1.114 (request for continued examination). See 37 CFR 1.313(c)(2).

Petitioner is advised that the issue fee paid in this application cannot be refunded. If, however, this application is again allowed, petitioner may request that it be applied towards the issue fee required by the new Notice of Allowance.

Telephone inquiries concerning this decision should be directed to the Patent Electronic Business Center (EBC) at 866-217-9197.

This application file is being referred to Technology Center AU 2182 for processing of the request for continuing examination under 37 CFR 1.114 .

Office of Petitions

Electronic Acknowledgement Receipt	
EFS ID:	43468882
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin
Filer Authorized By:	
Attorney Docket Number:	SNG.1001C9
Receipt Date:	10-AUG-2021
Filing Date:	25-MAY-2020
Time Stamp:	12:22:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$2140
RAM confirmation Number	E202180C21554219
Deposit Account	601293
Authorized User	Robert Plotkin
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	SNG-1001C9_2nd_RCE--.pdf	1350045 0b057392cc0082e9591850c8a7c5bafce09409df	no	3
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	SNG-1001C9_6th_Supp_IDS.pdf	1053512 964880fdbe92bcaa182e9c7e77abc5e7faa84dde	no	4
Warnings:					
Information:					
3	ePetition Request Form	petition-request.pdf	39844 d5f62e608f71e2a5141801004 3f8292594e92329	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	40515 9356bd203b79b6bcd51af3fe93ffb1efa9264fb8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2483916		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/882,694	Filing Date 05/25/2020	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	08/10/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 24	Minus	** 24	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/LAVINIA D JOHNSON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :C46472

Sale Accounting Date:07/16/2021

Sale Item Reference Number	Effective Date
16882694	07/15/2021

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20217F946500710	1501	UTILITY APPL ISSUE FEE	$1,000.00	Salea
I20217F946500710	1501	UTILITY APPL ISSUE FEE	$200.00	Deposit Account

Doc Code: MFEE.C.AD PTO/SB/47-EFS

Document Description: Maintenance Fee Address Change

FEE ADDRESS INDICATION FORM			
Application Number	16882694	Art Unit	2182
Filing Date	25-May-2020	Examiner Name	MICHAEL YAARY
First Name Inventor	Joseph Bates	Attorney Doc. Number	SNG.1001C9

INSTRUCTIONS: In order for the fee address identified on this form to be effective, the issue fee must have been paid for the application listed on this form. Only an address represented by a customer number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. For more information on customer numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

Please recognize as the Fee Address under the provisions of 37 CFR 1.363 the address associated with:

Customer Number:	144359 Blueshift IP LLC 1 Broadway, 14th Floor Cambridge MA 02142 UNITED STATES 617-207-6141 mail@blueshiftip.com

Signature :

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application.

Signature	/Robert Plotkin/	**Date**	07-15-2021
Name	Robert Plotkin	**Registration Number**	43861

Electronic Acknowledgement Receipt

EFS ID:	43260036
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin
Filer Authorized By:	
Attorney Docket Number:	SNG.1001C9
Receipt Date:	15-JUL-2021
Filing Date:	25-MAY-2020
Time Stamp:	15:51:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Web85b.pdf	46282 a52f02edeec744d208d1516fed56e8bd13a1731e	no	2

Warnings:

Information:					
2	Maintenance Fee Address Change	web85feeaddress.pdf	32752 31eec136c2014c3bc9d9175b021eb2328b86136c	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	79034	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
16882694	25-May-2020	Joseph Bates	SNG.1001C9	3296

TITLE OF INVENTION :

PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Regular Undiscounted	Utility under 35 USC 111(a)	2182	524000	MICHAEL YAARY

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$1200	$0	$1200	15-Oct-2021	$1000

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
144359 Blueshift IP LLC 1 Broadway, 14th Floor Cambridge MA 02142 UNITED STATES 617-207-6141 docketing@blueshiftip.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☒ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

○ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

◉ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☐ Issue Fee	☐ I authorize USPTO to apply my previously paid issue fee to the current fees due
☐ Publication Fee	☒ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number 601293
☐ Advance Order - # of copies _____	☒ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency, or credit any overpayment, to Deposit Account Number 601293 . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. BLUESHIFT IP, LLC
2. ROBERT PLOTKIN
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
Singular Computing LLC	Newton	MASSACHUSETTS	united states	corporation

6.Signature

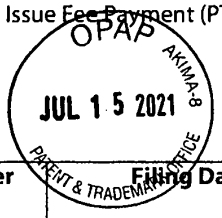
I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Robert Plotkin/	**Date**	07-15-2021
Name	Robert Plotkin	**Registration Number**	43861

WEB IFEE 1.0

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)



Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
16882694	25-May-2020	Joseph Bates	SNG.1001C9	3296

TITLE OF INVENTION :

PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Regular Undiscounted	Utility under 35 USC 111(a)	2182	524000	MICHAEL YAARY

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$1200	$0	$1200	15-Oct-2021	$1000

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
144359 Blueshift IP LLC 1 Broadway, 14th Floor Cambridge MA 02142 UNITED STATES 617-207-6141 docketing@blueshiftip.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☒ Fee Address indication requested, system generated SB/47-EFS form attached

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Change in Entity Status

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○ Applicant asserting small entity status. See 37 CFR 1.27.
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Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

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☐ Issue Fee	☐ I authorize USPTO to apply my previously paid issue fee to the current fees due
☐ Publication Fee	☒ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number 601293
☐ Advance Order - # of copies _____	☒ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency or credit any overpayment, to Deposit Account Number 601293. The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

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For printing on the patent front page, list to be displayed as entered

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3.

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Name	City	State	Country	Category
Singular Computing LLC	Newton	MASSACHUSETTS	united states	corporation

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Robert Plotkin/	**Date**	07-15-2021
Name	Robert Plotkin	**Registration Number**	43861

WEB IFEE 1.0

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

144359 7590 07/15/2021

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

EXAMINER
YAARY, MICHAEL D

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/15/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

TITLE OF INVENTION: PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$1000.00	$200	10/15/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

144359 7590 07/15/2021
Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

TITLE OF INVENTION: PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$1000.00	$200	10/15/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
YAARY, MICHAEL D	2182	708-524000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Google Ex. 1002 - Page 108

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

144359 7590 07/15/2021

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

EXAMINER	
YAARY, MICHAEL D	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/15/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	**Application No.** 16/882,694	**Applicant(s)** Bates, Joseph	
	Examiner MICHAEL D YAARY	**Art Unit** 2182	**AIA (FITF) Status** Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 11/11/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☐ The allowed claim(s) is/are _____ . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MICHAEL D. YAARY/
Primary Examiner, Art Unit 2182

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 11/11/2020;01/21/2021;02/23/2021;and05/25/2021

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

CPC						
Symbol					**Type**	**Version**
G06F	/	7	/	483	F	2013-01-01
G06F	/	7	/	38	I	2013-01-01
H03K	/	19	/	17728	I	2013-01-01
G06F	/	7	/	5235	I	2013-01-01
G06F	/	7	/	4833	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	24	
/MICHAEL D. YAARY/ Primary Examiner, Art Unit 2182	06 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20210706

Google Ex. 1002 - Page 113

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G06F7/483	/	7	/	483
G06F7/38	/	7	/	38
H03K19/17728	/	19	/	17728
G06F7/523	/	7	/	523

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	24	
/MICHAEL D. YAARY/ Primary Examiner, Art Unit 2182	06 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20210706

Google Ex. 1002 - Page 114

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10	19	19										
2	2	11	11	20	20										
3	3	12	12	21	21										
4	4	13	13	22	22										
5	5	14	14	23	23										
6	6	15	15	24	24										
7	7	16	16												
8	8	17	17												
9	9	18	18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	24	
/MICHAEL D. YAARY/ Primary Examiner, Art Unit 2182	06 July 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20210706

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/23/2020	08/18/2020	07/06/2021						
1	1	✓	=	=						
2	2	✓	=	=						
3	3	✓	=	=						
4	4	✓	=	=						
5	5	✓	=	=						
6	6	✓	=	=						
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21	21	✓	=	=						
22	22	✓	=	=						
23	23	✓	=	=						
24	24	✓	=	=						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	Art Unit
	MICHAEL D YAARY	2182

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	Art Unit
	MICHAEL D YAARY	2182

Search Notes		
Search Notes	**Date**	**Examiner**
EAST search with keywords	07/23/2020	MY
NPL search	07/23/2020	MY
Inventor name search	07/23/2020	MY
EAST search with keywords in combination with CPC classes	08/18/2020	MY
IPR2021-00154 Reviewed Inter Partes Review of U.S. Patent No. 10,416,961	07/06/2021	MY
IPR2021-00155 Reviewed Inter Partes Review of U.S. Patent No. 10,416,961 on 07/06/2021	07/06/2021	MY
IPR2021-00164 Reviewed Inter Partes Review of U.S. Patent No. 9,218,156 on 07/06/2021	07/06/2021	MY
IPR2021-00165 Reviewed Inter Partes Review of U.S. Patent No. 9,218,156 on 07/06/2021	07/06/2021	MY
IPR2021-00178 Reviewed Inter Partes Review of U.S. Patent No. 8,407,273 on 07/06/2021	07/06/2021	MY
IPR2021-00179 Reviewed Inter Partes Review of U.S. Patent No. 8,407,273 on 07/06/2021	07/06/2021	MY

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
G06F	7/483	08/18/2020	MY

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16882694
Filing Date	2020-05-25
First Named Inventor	Joseph Bates
Art Unit	2182
Examiner Name	MICHAEL D YAARY
Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/MY/	1	20210048981	A1	2021-02-18	Bates	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	1		

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/MICHAEL D. YAARY/	Date Considered	07/06/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2021-02-23
Name/Print	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /MY/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

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Filing Date	2020-05-25
First Named Inventor	Joseph Bates
Art Unit	2182
Examiner Name	MICHAEL D YAARY
Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/MY/	1	10838694		2020-11-17	BATES JOSEPH	
/MY/	2	5689677		1997-11-18	MACMILLAN DAVID C	
/MY/	3	6065209		2000-05-23	GONDOUIN MICHAEL	
/MY/	4	5375084		1994-12-20	BEGUN RALPH M	
/MY/	5	4933895		1990-06-12	GRINBERG JAN	
/MY/	6	5442577		1995-08-15	COHEN EARL T	
/MY/	7	5790834		1998-08-04	DREYER ROBERT S	
/MY/	8	5666071		1997-09-09	HAWKINS KEITH G	

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	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

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/MY/	13	8407273		2013-03-26	BATES JOSEPH	
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/MY/	15	7301436		2007-11-27	HOPPER PETER J	
/MY/	16	7349939		2008-03-25	PAASIO ARI	
/MY/	17	7346643		2008-03-18	HO YING-WAI	
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/MY/	21	6292586		2001-09-18	KAWAKAMI SUSUMU	
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/MY/	11	20050235070		2005-10-20	YOUNG JOSHUA	
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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/MY/	1	Prosecution History of U.S. Patent No. 10,416,961, identified as Exhibit 1002, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 288 pages.	
/MY/	2	Declaration of Richard Goodin, identified as Exhibit 1003, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 325 pages.	
/MY/	3	Curriculum Vitae of Richard Goodin, identified as Exhibit 1004, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 9 pages.	
/MY/	4	U.S. Patent Appl. 12/816, 201, identified as Exhibit 1005, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 64 pages.	
/MY/	5	Tong et. al, Reducing Power by Optimizing the Necessary Precision/Range of Floating-Point Arithmetic, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 3, June 2000 ("Tong") (from pages 6-19 of the Declaration of Gerard P. Grenier, Ex. 1025), identified as Exhibit 1008, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 14 pages.	
/MY/	6	Gaffar et. al, "Unifying Bit-width Optimization for Fixed-Point and Floating-Point Designs," 12th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, April 20-23, 2004 ("Gaffar") (from pages 22-31 of the Declaration of Gerard P. Grenier, Ex. 1028), identified as Exhibit 1012, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 10 pages.	

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/MY/	15	Docket Report for Singular Computing LLC v. Google, LLC, 1-19-cv-12551 (D. Mass.), identified as Exhibit 1033, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 15 pages.	
/MY/	16	Memorandum in Support of Motion to Dismiss for Failure to State a Claim (Dkt. No. 41), identified as Exhibit 1034, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 30 pages.	
/MY/	17	Plaintiff's Opposition to Defendant's Rule 12(b)(6) Motion to Dismiss for Lack of Patentable Subject Matter, Singular Computing LLC v. Google, LLC, 1-19-cv-12251 (D. Mass.), Dkt. No. 44, identified as Exhibit 1035, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 116 pages.	

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	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

/MY/	18	Memorandum and Order on Defendant's Motion to Dismiss (Dkt. No. 51), identified as Exhibit 1036, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 16 pages.	
/MY/	19	Plaintiffs' Preliminary Patent-Related Disclosures Pursuant to Patent L.R. 16.6(d)(1)(A), identified as Exhibit 1037, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 46 pages.	
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/MY/	23	Letter Re Reservation of Rights, identified as Exhibit 1041, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 2 pages.	
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/MY/	36	PETITION FOR INTER PARTES REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq, AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 92 pages.	
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	Attorney Docket Number	SNG.1001C9

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Examiner Signature	/MICHAEL D. YAARY/	Date Considered	07/06/2021

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2021-05-25
Name/Print	Robert Plotkin	Registration Number	43861

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

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	Application Number	16882694
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	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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/MY/	1	20080155004		2008-06-26	ANDO HISASHIGE	
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	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

/MY/	1	Hearing Notice mailed January 16, 2021, in Indian patent application number 98/MUMNP/2012, 3 pages.	

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EXAMINER SIGNATURE

Examiner Signature	/MICHAEL D. YAARY/	Date Considered	07/06/2021

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Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2021-01-21
Name/Print	Robert Plotkin	Registration Number	43861

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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	Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6650327	B1	2003-11-18	Airey et al.	

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
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	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	1	Communication pursuant to Article 94(3) EPC mailed April 21, 2021 in European patent application number 18177602.2, 8 pages.	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application Number	16/882,694
	Filing Date	05/25/2020
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Client Number	SNG
Page 1 of 1	**Matter Number**	1001C9

GENERAL

Pursuant to 37 C.F.R. 1.97 and 1.98 and to the duty of disclosure set forth in 37 C.F.R. 1.56, the Examiner in charge of the above-identified application is requested to consider and make of record the references listed herewith. A copy of each listed reference, other than U.S. patents/applications and references cited in a parent application, is enclosed.

Although the information submitted herewith may be "material" to the Examiner's consideration of the subject application, this submission is not intended to constitute an admission that such information is "prior art" as to the claimed invention.

In accordance with 37 C.F.R. 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made.

TIMING

In accordance with 37 CFR 1.97(b), this Information Disclosure Statement is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits; or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

CERTIFICATION STATEMENT

No certification statement is required. This Information Disclosure Statement is being filed in accordance with 37 CFR 1.97(b).

FEE

No fee is required. This Information Disclosure Statement is being filed in accordance with 37 CFR 1.97(b).

If necessary, the Director is hereby authorized to charge or credit Deposit Account No. 60/1293 for any additional fees, or any underpayment or credit for overpayment in connection herewith. Please reference attorney docket number SNG-1001C9 for any such charge or credit.

ADDITIONAL COMMENTS

SIGNATURE

Signature	/Robert Plotkin/	**Date**	2021-05-25
Name	Robert Plotkin	**Registration Number**	43861

SyncIDS.com

Electronic Acknowledgement Receipt

EFS ID:	42813445
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	25-MAY-2021
Filing Date:	25-MAY-2020
Time Stamp:	13:42:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	SNG-1001C9_5th_Supp_IDS-Form.pdf	1053249 fb70bb9b33dad5f767de0e1f25d2e6cacb50a44b	no	4

Warnings:

Information:					
2	Transmittal Letter	SNG-1001C9_5th_Supp_IDS-Transmittal-Letter.pdf	514500 2054eeedfe7477e4275b6428405051fe52474e08	no	1
Warnings:					
Information:					
3	Non Patent Literature	SNG-1001C9-NPL-001.pdf	331770 6591ae1d756a72e9a43f77df50b53b63f54024d2	no	8
Warnings:					
Information:					
		Total Files Size (in bytes):	1899519		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20210048981	A1	2021-02-18	Bates	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	1	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2021-02-23
Name/Print	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application Number	16/882,694
	Filing Date	05/25/2020
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Client Number	SNG
Page 1 of 1	**Matter Number**	1001C9

GENERAL

Pursuant to 37 C.F.R. 1.97 and 1.98 and to the duty of disclosure set forth in 37 C.F.R. 1.56, the Examiner in charge of the above-identified application is requested to consider and make of record the references listed herewith. A copy of each listed reference, other than U.S. patents/applications and references cited in a parent application, is enclosed.

Although the information submitted herewith may be "material" to the Examiner's consideration of the subject application, this submission is not intended to constitute an admission that such information is "prior art" as to the claimed invention.

In accordance with 37 C.F.R. 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made.

TIMING

In accordance with 37 CFR 1.97(b), this Information Disclosure Statement is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits; or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

CERTIFICATION STATEMENT

No certification statement is required. This Information Disclosure Statement is being filed in accordance with 37 CFR 1.97(b).

FEE

No fee is required. This Information Disclosure Statement is being filed in accordance with 37 CFR 1.97(b).

If necessary, the Director is hereby authorized to charge or credit Deposit Account No. 60/1293 for any additional fees, or any underpayment or credit for overpayment in connection herewith. Please reference attorney docket number SNG-1001C9 for any such charge or credit.

ADDITIONAL COMMENTS

SIGNATURE

Signature	/Robert Plotkin/	**Date**	2021-02-23
Name	Robert Plotkin	**Registration Number**	43861

SyncIDS.com

Electronic Acknowledgement Receipt

EFS ID:	42002867
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	23-FEB-2021
Filing Date:	25-MAY-2020
Time Stamp:	19:35:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	SNG-1001C9_PTO_IDS-Form_4th_Supp.pdf	1053142 c90660c82a33425653071069bed499c0837e5b9c	no	4

Warnings:

Information:					
2	Transmittal Letter	SNG-1001C9_Transmittal-Letter_4th_Supp.pdf	503391 85a5d8af914e1bc54aa0f270b68e051dccc40517	no	1
Warnings:					
Information:					
			Total Files Size (in bytes):	1556533	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20080155004		2008-06-26	ANDO HISASHIGE	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	1	Hearing Notice mailed January 16, 2021, in Indian patent application number 98/MUMNP/2012, 3 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2021-01-21
Name/Print	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application Number	16/882,694
	Filing Date	05/25/2020
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Client Number	SNG
Page 1 of 1	**Matter Number**	1001C9

GENERAL

Pursuant to 37 C.F.R. 1.97 and 1.98 and to the duty of disclosure set forth in 37 C.F.R. 1.56, the Examiner in charge of the above-identified application is requested to consider and make of record the references listed herewith. A copy of each listed reference, other than U.S. patents/applications and references cited in a parent application, is enclosed.

Although the information submitted herewith may be "material" to the Examiner's consideration of the subject application, this submission is not intended to constitute an admission that such information is "prior art" as to the claimed invention.

In accordance with 37 C.F.R. 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made.

TIMING

In accordance with 37 CFR 1.97(b), this Information Disclosure Statement is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits; or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

CERTIFICATION STATEMENT

No certification statement is required. This Information Disclosure Statement is being filed in accordance with 37 CFR 1.97(b).

FEE

No fee is required. This Information Disclosure Statement is being filed in accordance with 37 CFR 1.97(b).

If necessary, the Director is hereby authorized to charge or credit Deposit Account No. 60/1293 for any additional fees, or any underpayment or credit for overpayment in connection herewith. Please reference attorney docket number SNG-1001C9 for any such charge or credit.

ADDITIONAL COMMENTS

SIGNATURE

Signature	/Robert Plotkin/	**Date**	01/21/2021
Name	Robert Plotkin	**Registration Number**	43861

SyncIDS.com

Electronic Acknowledgement Receipt

EFS ID:	41708582
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	21-JAN-2021
Filing Date:	25-MAY-2020
Time Stamp:	15:57:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	SNG-1001C9_PTO_IDS-Form_3rd_Supp.pdf	1053210 0c5fc4e5f91f67044670766059988ca27f31317	no	4

Warnings:

Information:					
2	Transmittal Letter	SNG-1001C9_Transmittal-Letter.pdf	514498 584d516c7b775c5e494cdc9c77c76d48b7b7e1d8	no	1
Warnings:					
Information:					
3	Non Patent Literature	SNG-1001C9-NPL-001.pdf	141360 e94b81ff1b0fc14368bcc9ce5879d2fd670c8046	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	1709068		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PET.AUTO Document Description: Petition automatically granted by EFS-Web	PTO/SB/140 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**PETITION TO WITHDRAW AN APPLICATION FROM ISSUE AFTER PAYMENT OF THE ISSUE FEE UNDER 37 CFR 1.313(c)**
Application Number	16882694
Filing Date	25-May-2020
First Named Inventor	Joseph Bates
Art Unit	2182
Examiner Name	MICHAEL YAARY
Attorney Docket Number	SNG.1001C9
Title	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

An application may be withdrawn from issue for further action upon petition by the applicant. To request that the Office withdraw an application from issue, applicant must file a petition under this section including the fee set forth in § 1.17(h) and a showing of good and sufficient reasons why withdrawal of the application from issue is necessary.

APPLICANT HEREBY PETITIONS TO WITHDRAW THIS APPLICATION FROM ISSUE UNDER 37 CFR 1.313(c).

A grantable petition requires the following items:
(1) Petition fee; and
(2) One of the following reasons:
(a) Unpatentability of one or more claims, which must be accompanied by an unequivocal statement that one or more claims are unpatentable, an amendment to such claim or claims, and an explanation as to how the amendment causes such claim or claims to be patentable;
(b) Consideration of a request for continued examination in compliance with § 1.114 (for a utility or plant application only); or
(c) Express abandonment of the application. Such express abandonment may be in favor of a continuing application, but not a CPA under 37 CFR 1.53(d).

Petition Fee

- ◯ Small Entity
- ◯ Micro Entity
- ◉ Regular Undiscounted

Reason for withdrawal from issue

◯ One or more claims are unpatentable ◉ Consideration of a request for continued examination (RCE) (List of Required Documents and Fees) ◯ Applicant hereby expressly abandons the instant application (any attorney/agent signing for this reason must have power of attorney pursuant to 37 CFR 1.32(b)).
RCE request,submission, and fee. ☒ I certify, in accordance with 37 CFR 1.4(d)(4) that : The RCE request ,submission, and fee have already been filed in the above-identified application on 2020.11.12 ☐ Are attached.
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ◉ An attorney or agent registered to practice before the Patent and Trademark Office who has been given power of attorney in this application. ◯ An attorney or agent registered to practice before the Patent and Trademark Office, acting in a representative capacity. ◯ A sole inventor ◯ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ◯ A joint inventor; all of whom are signing this e-petition

Signature	/Robert Plotkin/
Name	Robert Plotkin
Registration Number	43861

Electronic Patent Application Fee Transmittal

Application Number:	16882694
Filing Date:	25-May-2020
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Filer:	Robert Plotkin/Kimberly Hauser
Attorney Docket Number:	SNG.1001C9

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
PETITION FEE- 37 CFR 1.17(H) (GROUP III)	1464	1	140	140
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**140**

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Decision Date : November 11, 2020

In re Application of :

Joseph Bates

DECISION ON PETITION

UNDER CFR 1.313(c)(2)

Application No : 16882694

Filed : 25-May-2020

Attorney Docket No : SNG.1001C9

This is an electronic decision on the petition under 37 CFR 1.313(c)(2), filed November 11, 2020 to withdraw the above-identified application from issue after payment of the issue fee.

The petition is **GRANTED.**

The above-identified application is withdrawn from issue for consideration of a submission under 37 CFR 1.114 (request for continued examination). See 37 CFR 1.313(c)(2).

Petitioner is advised that the issue fee paid in this application cannot be refunded. If, however, this application is again allowed, petitioner may request that it be applied towards the issue fee required by the new Notice of Allowance.

Telephone inquiries concerning this decision should be directed to the Patent Electronic Business Center (EBC) at 866-217-9197.

This application file is being referred to Technology Center AU 2182 for processing of the request for continuing examination under 37 CFR 1.114 .

Office of Petitions

Electronic Acknowledgement Receipt	
EFS ID:	41072491
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	11-NOV-2020
Filing Date:	25-MAY-2020
Time Stamp:	20:41:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$140
RAM confirmation Number	E2020AAK40590921
Deposit Account	601293
Authorized User	Kimberly Hauser
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges) 37 CFR 1.20 (Post Issuance fees)	

37 CFR 1.17 (Patent application and reexamination processing fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition automatically granted by EFS	petition-request.pdf	31628 3f8f0f7fd4f33c92f4d3c550a601c2b425d5cbdb	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30823 e01c1a730b1a44d319dd809ce0bf46d1b06607b8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	62451		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16882694
Filing Date	2020-05-25
First Named Inventor	Joseph Bates
Art Unit	2182
Examiner Name	MICHAEL D YAARY
Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	10838694		2020-11-17	BATES JOSEPH	
	2	5689677		1997-11-18	MACMILLAN DAVID C	
	3	6065209		2000-05-23	GONDOUIN MICHAEL	
	4	5375084		1994-12-20	BEGUN RALPH M	
	5	4933895		1990-06-12	GRINBERG JAN	
	6	5442577		1995-08-15	COHEN EARL T	
	7	5790834		1998-08-04	DREYER ROBERT S	
	8	5666071		1997-09-09	HAWKINS KEITH G	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	9	6311282		2001-10-30	NELSON PHILLIP D	
	10	4583222		1986-04-15	FOSSUM TRYGGVE	
	11	5623616		1997-04-22	VITALE PHILIP L	
	12	8150902		2012-04-03	BATES JOSEPH	
	13	8407273		2013-03-26	BATES JOSEPH	
	14	6622135		2003-09-16	IMBERT DE TREMIOLLES GISLAIN	
	15	7301436		2007-11-27	HOPPER PETER J	
	16	7349939		2008-03-25	PAASIO ARI	
	17	7346643		2008-03-18	HO YING-WAI	
	18	7209867		2007-04-24	VIGODA BENJAMIN	
	19	6941334		2005-09-06	ROGENMOSER ROBERT	

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	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	20	6742007		2004-05-25	OSHIAMA HIROYASU	
	21	6292586		2001-09-18	KAWAKAMI SUSUMU	
	22	6282559		2001-08-28	HELFENSTEIN MARKUS	
	23	5581485		1996-12-03	VAN AKEN PHILIP A	
	24	5293558		1994-03-08	NARITA MASAHISA	

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20200334011		2020-10-22	BATES JOSEPH	
	2	20100325186		2010-12-23	BATES JOSEPH	
	3	20070203967		2007-08-30	DOCKSER KENNETH A	
	4	20070266071		2007-11-15	DOCKSER KENNETH A	

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	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	5	20030028759		2003-02-06	PRABHU J ARJUN	
	6	20090066164		2009-03-12	FLYNN DAVID WALTER	
	7	20070033572		2007-02-08	DONOVAN ROBERT J	
	8	20060270110		2006-11-30	STEFFEN FRANCIS	
	9	20090188705		2009-07-30	KACKER KARAN	
	10	20070050566		2007-03-01	LANG CHRISTIAN A	
	11	20050235070		2005-10-20	YOUNG JOSHUA	
	12	20030204760		2003-10-30	YOUNGS LYNN R	
	13	20080183791		2008-07-31	HO YING-WAI	
	14	20050160129		2005-07-21	ENDO YUKIO	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
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	Attorney Docket Number	SNG.1001C9

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	0632369A1	EP		1995-01-04	STICHTING TECH WETENSCHAPP		
	2	H0877282A	JP		1996-03-22	RADIC KK		X

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Prosecution History of U.S. Patent No. 10,416,961, identified as Exhibit 1002, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 288 pages.	
	2	Declaration of Richard Goodin, identified as Exhibit 1003, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 325 pages.	
	3	Curriculum Vitae of Richard Goodin, identified as Exhibit 1004, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 9 pages.	
	4	U.S. Patent Appl. 12/816, 201, identified as Exhibit 1005, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 64 pages.	
	5	Tong et. al, Reducing Power by Optimizing the Necessary Precision/Range of Floating-Point Arithmetic, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 3, June 2000 ("Tong") (from pages 6-19 of the Declaration of Gerard P. Grenier, Ex. 1025), identified as Exhibit 1008, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 14 pages.	
	6	Gaffar et. al, "Unifying Bit-width Optimization for Fixed-Point and Floating-Point Designs," 12th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, April 20-23, 2004 ("Gaffar") (from pages 22-31 of the Declaration of Gerard P. Grenier, Ex. 1028), identified as Exhibit 1012, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 10 pages.	

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	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	7	A Matter of Size: Triennial Review of the National Nanotechnology Initiative (National Academies Press 2006), pages 15-44, 99-109, identified as Exhibit 1021, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 46 pages.
	8	Transcript of YouTube video on Practical Approximate Computing at University of California, Berkeley, March 2016 ("Bates transcript"), video available at https://www.youtube.com/watch?v=aHkWX3QctkM (last accessed Sep. 16, 2020), identified as Exhibit 1022, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 35 pages.
	9	Declaration of Gerard P. Grenier regarding Tong et. al, Reducing Power by Optimizing the Necessary Precision/Range of Floating-Point Arithmetic, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8, No. 3, June 2000, identified as Exhibit 1025, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 19 pages.
	10	Moshnyaga, Energy Reduction in Queues and Stacks by Adaptive Bitwidth Compression, Proceedings of the 2001 International Symposium on Low Power Electronics and Design, Aug. 6-7, 2001 ("Moshnyaga"), with IEEE Xplore information appended, identified as Exhibit 1026, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 17 pages.
	11	Simunic, Energy-Efficient Design of Battery-Powered Embedded Systems, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 9, No. 1, Feb. 2001 ("Simunic") , with IEEE Xplore information appended, identified as Exhibit 1027, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 28 pages.
	12	Declaration of Gerard P. Grenier regarding Gaffar et. al, Unifying Bit-width Optimization for Fixed-Point and Floating-Point Designs, 12th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, April 20-23, 2004, identified as Exhibit 1028, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 31 pages.
	13	David A. Patterson and John L. Hennessy, Computer Organization and Design (Morgan Kaufmann 3rd ed. Revised 2007) ("Patterson"), pages 189-217, identified as Exhibit 1031, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 41 pages.
	14	First Amended Complaint in Singular Computing LLC v. Google, LLC, 1-19-cv-12251 (D. Mass.) (Dkt. No. 37), identified as Exhibit 1032, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 80 pages.
	15	Docket Report for Singular Computing LLC v. Google, LLC, 1-19-cv-12551 (D. Mass.), identified as Exhibit 1033, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 15 pages.
	16	Memorandum in Support of Motion to Dismiss for Failure to State a Claim (Dkt. No. 41), identified as Exhibit 1034, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 30 pages.
	17	Plaintiff's Opposition to Defendant's Rule 12(b)(6) Motion to Dismiss for Lack of Patentable Subject Matter, Singular Computing LLC v. Google, LLC, 1-19-cv-12251 (D. Mass.), Dkt. No. 44, identified as Exhibit 1035, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 116 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	18	Memorandum and Order on Defendant's Motion to Dismiss (Dkt. No. 51), identified as Exhibit 1036, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 16 pages.	
	19	Plaintiffs' Preliminary Patent-Related Disclosures Pursuant to Patent L.R. 16.6(d)(1)(A), identified as Exhibit 1037, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 46 pages.	
	20	Scheduling Order for Singular Computing LLC v. Google, LLC, 1-19-cv-12551 (D. Mass.) (Dkt. No. 59), identified as Exhibit 1038, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 5 pages.	
	21	Transcript of Scheduling Conference held on July 24, 2020, identified as Exhibit 1039, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 13 pages.	
	22	General Order 20-21, Second Supplemental Order Concerning Jury Trials and Related Proceedings, In Re: Coronavirus Public Emergency (D. Mass. May 27, 2020), identified as Exhibit 1040, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 2 pages.	
	23	Letter Re Reservation of Rights, identified as Exhibit 1041, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 2 pages.	
	24	Prosecution History of U.S. Patent No. 8,150,902, issued from U.S. Patent Appl. No. 12/816,201, identified as Exhibit 1042, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 196 pages.	
	25	Prosecution History of U.S. Patent No. 8,407,273, identified as Exhibit 1043, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 191 pages.	
	26	Prosecution History of U.S. Patent No. 9,218,156, identified as Exhibit 1044, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 319 pages.	
	27	Prosecution History of U.S. Patent No. 9,792,088, identified as Exhibit 1045, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 302 pages.	
	28	Prosecution History of U.S. Patent No. 10,120,648, identified as Exhibit 1046, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 269 pages.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Attorney Docket Number	SNG.1001C9

	29	Thomas Way et. al, Compiling Mechanical Nanocomputer Components, Global Journal of Computer Science and Technology, Vol. 10, Issue 2 (Ver. 1.0), April 2010, pp. 36-42 ("Way"), identified as Exhibit 1047, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 7 pages.	
	30	David Nield, In a Huge Milestone, Engineers Build a Working Computer Chip out of Carbon Nanotubes, Sciencealert.com, Dec. 7, 2019 (accessed Sep. 9, 2020) ("Nield"), identified as Exhibit 1048, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 4 pages.	
	31	Leah Cannon, What Can DNA-Based Computers Do?, MIT Technology Review, Feb. 4, 2015 (accessed Sep. 8, 2020) ("Cannon"), identified as Exhibit 1049, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 8 pages.	
	32	Katherin Bourzac, The First Carbon Nanotube Computer, MIT Technology Review, Sep. 25, 2013 (accessed Sep. 8, 2020) ("Bourzac"), identified as Exhibit 1050, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 10 pages.	
	33	Joe Touch et. al,, Optical Computing, Nanophotonics 2017 6(3): 503-505 ("Touch"), identified as Exhibit 1051, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 10 pages.	
	34	Robert Allen, Ed., The Penguin Complete English Dictionary, (Penguin 2006) ("Penguin"), page 1411, definition of "supercomputer", identified as Exhibit 1052, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 3 pages.	
	35	A Dictionary of Computing (Oxford 6th ed. 2008) ("Oxford"), page 500, definition of "supercomputer", identified as Exhibit 1053, for AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 3 pages.	
	36	PETITION FOR INTER PARTES REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq, AIA Parties Review proceedings number IPR2021-00155, October 30, 2020, 92 pages.	
	37	PETITION FOR INTER PARTES REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq, AIA Parties Review proceedings number IPR2021-00154, October 30, 2020, 85 pages.	
	38	Pavle Belanovic et al., "A Library of Parameterized Floating-Point Modules and Their Use," M. Glesner, P. Zipf, and M. Renovell (Eds.): FPL 2002, LNCS 2438, pp. 657–666, 2002. Copyright Springer-Verlag Berlin Heidelberg 2002	
	39	Pavle Belanovic, "Library of Parameterized Hardware Modules for Floating-Point Arithmetic with An Example Application," Thesis Presented to Department of Electrical and Computer Engineering in Partial Fulfillment of the Requirements for the Degree of Master of Science for Electrical and Computer Engineering, Northeastern University, Boston, Massachusetts, May 2002, 187 pages.	

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	Attorney Docket Number	SNG.1001C9

	40	GH A. Aty et al., "High-Speed, Area-Efficient FPGA-Based Floating-Point Multiplier," ICM 2003, Dec 9-11, Cairo, Egypt, 4 pages.	
	41	Nabeel Shirazi et al., "Quantitative Analysis of Floating Point Arithmetic on FPGA Based Custom Computing Machines," Presented at the IEEE Symposium on FPGAs for Custom Computing Machines, Napa Valley, California, April 1995, 8 pages.	
	42	David A. Martin et al., "A mixed-signal array processor with early vision applications," IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 33, NO. 3, MARCH 1998, 6 pages,	
	43	Jarmo Takala et al., "Hardware architecture for real-time distance transform," Conference: Acoustics, Speech, and Signal Processing, 1999. ICASSP '99. Proceedings., 1999 IEEE International Conference, Volume: 4, April 1999, 4 pages.	
	44	V. Raghunathan et al., "High-level synthesis with SIMD units," Conference: Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia and South Pacific and the 15th International Conference on VLSI Design. Proceedings. February 2002, 8 pages.	
	45	PETITION FOR INTER PARTES REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq, AIA Parties Review proceedings number IPR2021-00178, November 6, 2020, 90 pages.	
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	47	PETITION FOR INTER PARTES REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq, AIA Parties Review proceedings number IPR2021- 00164, November 5, 2020, 86 pages.	
	48	PETITION FOR INTER PARTES REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq, AIA Parties Review proceedings number IPR2021-00165, November 5, 2020, 92 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2020-11-11
Name/Print	Robert Plotkin	Registration Number	43861

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application Number	16/882,694
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	First Named Inventor	Joseph Bates
	Art Unit	2182
	Client Number	SNG
Page 1 of 1	**Matter Number**	1001C9

GENERAL

Pursuant to 37 C.F.R. 1.97 and 1.98 and to the duty of disclosure set forth in 37 C.F.R. 1.56, the Examiner in charge of the above-identified application is requested to consider and make of record the references listed herewith. A copy of each listed reference, other than U.S. patents/applications and references cited in a parent application, is enclosed.

Although the information submitted herewith may be "material" to the Examiner's consideration of the subject application, this submission is not intended to constitute an admission that such information is "prior art" as to the claimed invention.

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TIMING

In accordance with 37 CFR 1.97(b), this Information Disclosure Statement is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits; or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

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ADDITIONAL COMMENTS

SIGNATURE

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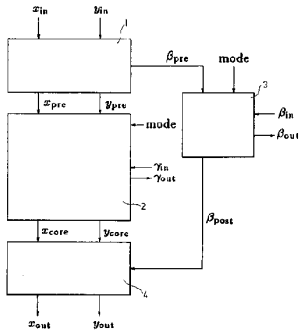
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(54) CORDIC algorithms and architectures.

(57) A CORDIC arrangement to rotate an input vector (x_{in},y_{in}) over an angle α to an output vector (x_{out},y_{out}), the coordinates being represented by floating-point numbers with respective mantissas (m_x,m_y) and respective angle exponents (e_x,e_y) comprising:

- a pre-rotation unit (1) receiving the input vector (x_{in},y_{in}) to rotate the input vector (x_{in},y_{in}) over an angle β_{pre};
- a core (2) connected to the pre-rotation unit 1 and carrying out a vectoring operation or a rotation operation in dependence on a mode signal (mode);
- a post-rotation unit (4) connected to the core (2) to carry out a post-rotation in dependence on the mode signal (mode);
- a rotation handler (3) receiving the mode signal (mode) and connected to both the pre-rotation unit (1) and to the post-rotation unit (3) in order to control their operation.

fig-2



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The present invention relates to CORDIC algorithms and architectures. The CORDIC (COordinate Rotation DIgital Computer) algorithm was presented by Volder, "The CORDIC trigonometric computing technique", IRE Transactions on electronic computers, pages 330-334, September 1959, as an elegant and cost-effective method to perform rotations on vectors in the 2-D plane. Walther, "A unified algorithm for elementary functions", Proceedings of the AFIPS Spring Joint Computer Conference, pages 379-385, 1971, extended the algorithm to rotations in circular, linear and hyperbolic coordinate systems. Since then, many implementations of the CORDIC have been made, both for fixed-point and floating-point with respect to the input.

CORDIC computing techniques are widely used in e.g. navigation where course angles have to be corrected and distance-to-destination relationships in great circle steering have to be solved. However, the magnitude and phase of a complex number may also be approximated by a CORDIC, EP-A-0.365.226. Also, a CORDIC may be an element in a filter arrangement to detect phase differences, EP-A-0.481.543. A digital receiver comprising a CORDIC is described in EP-A-0.486.095. Generally spoken, a CORDIC may be used in any technical field in which an input vector has to be rotated to an output vector.

The main drawback in the computations with floating-point data with the classic CORDIC algorithm lies with the inherent fixed-point resolution of the angle. The accuracy, especially when calculating angles close to or smaller than the angle resolution, becomes unacceptable. Therefore, in applications using a CORDIC there is a need to enhance the accuracy of the output data of the CORDIC in order not to loose any precision by the use of CORDIC's.

The object of the present invention is to provide CORDIC architectures and algorithms that overcome the problems of the prior art.

In accordance with the present invention the object is obtained by a CORDIC arrangement to rotate an input vector (x_{in},y_{in}) over an angle α to an output vector (x_{out}, y_{out}), characterized in that x_{in}, y_{in}, x_{out}, y_{out} are represented by floating-point numbers with respective mantissas (m_x, m_y) and respective angle exponents (e_x, e_y) and the CORDIC arrangement comprises:

(a) a pre-rotation unit receiving the input vector (x_{in}, y_{in}) to rotate the input vector (x_{in}, y_{in}) over an angle β_{pre} to give a vector (x_{pre}, y_{pre});

(b) a core receiving the vector (x_{pre}, y_{pre}) from the pre-rotation unit to rotate the vector (x_{pre}, y_{pre}) over an angle γ to give a vector (x_{core}, y_{core}), where the angle γ, depending on a signal mode supplied by an operator, is either supplied by the operator as γ_{in} or computed and output as γ_{out};

(c) a rotation handler receiving the angle β_{pre} from the prerotation unit and the signal mode supplied by an operator, and a possible angle β_{in} supplied by the operator to compute angles β_{post}, β_{out} in dependence thereon;

(d) a post-rotation unit receiving the vector (x_{core}, y_{core}) from the core and receiving the angle β_{post} from the rotation handler to rotate the vector (x_{core}, y_{core}) over the angle β_{post} to give the output vector (x_{out}, y_{out});

wherein

(a) the floating-point angle α is represented by a tuple (β, γ), β being the sum of β_{pre} and β_{post}, and γ being represented by a tuple (ξ, ζ), of which ξ is an angle exponent and ζ is an angle mantissa;

(b) α equals the sum of β and γ.

By the application of these measures an accuracy in the output vector may be obtained to such precision that the error introduced by the CORDIC computation is smaller than the error which can be accounted to the (in)accuracy of the input data.

In a first preferred embodiment of the CORDIC arrangement defined above it is characterized in that the core comprises:

(a) an exponent handler receiving the exponents $(e_{x,pre}, e_{y,pre})$ of the vector (x_{pre}, y_{pre}) and computing a CORDIC table selector Ξ, and alignment factors $a_{y,pre}$, $a_{x,core}$ and $a_{y,core}$, exponents $(e_{x,core}, e_{y,core})$ of the vector (x_{core}, y_{core}) and, depending on the signal mode, either receiving from the operator an angle exponent ξ_{in} or computing an angle exponent ξ_{out};

(b) an instruction sequencer receiving the cordic table selector Ξ from the exponent handler and producing a sequence of instructions I;

(c) an instruction execution unit receiving the mantissas $(m_{x,pre},m_{y,pre})$ of the vector (x_{pre}, y_{pre}), receiving the alignement factors $a_{y,pre}$, $a_{x,core}$ and $a_{y,core}$ from the exponent handler and receiving the sequence of instructions I supplied by the instruction sequencer and, depending on the signal mode, either receiving an angle mantissa ζ_{in} supplied by the operator or computing an angle mantissa ζ_{out} producing mantissas $(m_{x,core}, m_{y,core})$ of the vector (x_{core}, y_{core}).

Such a CORDIC arrangement has a sequential implementation and therefore saves chip area.

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A similar scheme for floating-point on-line computation of Givens rotations has been presented in M. Ercegovac and T. Lang, "On-line scheme for computing rotation factors", Journal of parallel and distributed Computing, 5:209-227, 1988. However, in this scheme no CORDIC arithmetic was used and the implementation shows up to be very complex.

In a second preferred embodiment the CORDIC arrangement is characterized in that the core comprises:

(a) an exponent handler receiving the exponents ($e_{x,pre}$, $e_{y,pre}$) of the vector (x_{pre}, y_{pre}) and computing a CORDIC table selector Ξ, alignment factors $a_{y,coarse}$, $a_{y,fine}$, $a_{y,fixed}$, $a_{y,fixed}$, exponents ($e_{x,coarse}$, $e_{y,coarse}$) of a vector (x_{coarse}, y_{coarse}) and, depending on the signal mode, either receiving from the operator an angle exponent ξ_{in} or computing an angle exponent ξ_{out};

(b) a coarse core receiving the mantissas ($m_{x,pre}$, $m_{y,pre}$) of the vector (x_{pre}, y_{pre}) and receiving the alignment factor $a_{y,coarse}$ from the exponent handler and, depending on the signal mode, receiving a coarse angle mantissa $\zeta_{in,coarse}$ supplied by the operator, or producing $\zeta_{out,coarse}$, to compute mantissas ($m_{x,coarse}$, $m_{y,coarse}$) of the vector (x_{coarse}, y_{coarse});

(c) a fine core receiving the mantissas ($m_{x,coarse}$, $m_{y,coarse}$) from the coarse core and receiving the alignment factors $a_{y,fine}$,$a_{y,fixed}$ and $a_{y,fixed}$ from the exponent handler and, depending upon the signal mode, receiving a fine angle mantissa $\zeta_{in,fine}$ supplied by the operator, or producing $\zeta_{out,fine}$, to compute the mantissas ($m_{x,core}$, $m_{y,core}$) of the vector (x_{core}, y_{core});

wherein the angle mantissa ζ is represented by a tuple (ζ_{coarse}, ζ_{fine}) and, depending on the signal mode, is either input by the operator as ζ_{in} or computed and output as ζ_{out}.

Such a CORDIC arrangement has an efficient parallel, pipelined implementation.

The invention further relates to a method defined in claims 4, 5, 6.

First, a short summary of the original CORDIC algorithm will be given.

The CORDIC algorithm knows two modes of operation, namely vectoring and rotation which are equivalent to the so-called backward and forward Givens rotations.

In the vectoring mode, the vector $(x,y)_{in}$ is rotated to

$$(x,y)_{out} = ([x^2_{in} + y^2_{in}]^{\frac{1}{2}},0)$$

and thereby computing the angle of inclination α_{out}.

In the rotation mode, the vector $(x,y)_{in}$ is rotated over a given angle α_{in} to $(x,y)_{out}$.

The basic idea behind the CORDIC algorithm is that a rotation is decomposed into a sequence of n so-called unnormalized micro-rotations over the base angles α_i, with $i \in \{0, ..., n-1\}$ and $0 < \alpha_i \leq \pi/2$. These base angles are chosen in such a way that the micro-rotations are easy to execute (implement) in hardware.

The general recursion for the micro-rotations is given by:

$$\begin{aligned} x_{i+1} &= x_i - (\sigma_i \tan \alpha_i)y_i \\ y_{i+1} &= +(\sigma_i \tan \alpha_i)x_i + y_i \end{aligned} \qquad (1)$$

with the input and output to the recursion:

$$x_0 = K^{-1}.x_{in} \qquad x_{out} = x_n$$

and (2)

$$y_0 = K^{-1}.y_{in} \qquad y_{out} = y_n$$

The use of unnormalized micro-rotations in the recursion (1) causes that the vector is lengthened or scaled by a factor $1/\cos\alpha_i$ with every step. Hence the need for a division by K in equation (2), where K is the accumulative scaling factor given by:

$$K = \prod_{i=0}^{n-1} \frac{1}{\cos\alpha_i} \qquad (3)$$

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The σ_i in the recursion (1) indicates the direction of the micro-rotation. These "sigma-bits" σ_i can be either -1 or +1, signifying clockwise resp. counterclockwise rotations.

The relationship between the angle of rotation α and the sequence of sigma bits $\{\sigma_i\}$ is given by the summation:

$$\alpha = + \sum_{i=0}^{n-1} \sigma_i \alpha_i \qquad (4)$$

In order to converge for any angle within a given domain of convergence, the sequence of base angles must form a basis and hence satisfy the conditions:

$$\alpha_i \leq \sum_{k>i}^{n-1} \alpha_k + \alpha_{min};\ \alpha_{min} = \alpha_{n-1} \qquad (5)$$

$$\alpha_i \geq \alpha_{i+1} \qquad (6)$$

We will refer to the sequence of base angles $\{\alpha_i\}$ as the angular basis. The domain of convergence r is given by the sum of the base angles:

$$r = + \sum_{i=0}^{n-1} \alpha_i + \alpha_{min} \qquad (7)$$

For any angle α within the domain of convergence, with $|\alpha| \leq r$, the CORDIC algorithm will converge with the resolution determined by the smallest base angle.

In order to keep the implementation of the micro-rotations simple, we introduce:

$$a_i = \tan \alpha_i \qquad (8)$$

and require that the multiplication by a_i is of low complexity when implemented in hardware. We opt for the approach presented by Bu et al.[1], where

$$a_i = 2^{+S_i} + \eta_i \cdot 2^{+S'_i} \qquad \eta_i \in \{-1,0,1\} \qquad (9)$$

with the shift factors S_i and S'_i being integer numbers. Using this scheme, the micro-rotation in recursion (1) is either a pair on one ($\eta_i = 0$) or two ($\eta_i \neq 0$) shift- and add operations.

A definition of floating-point numbers is given. A floating-point number x is represented by a tuple (e_x,m_x) with:

exponent An N_e-bit exponent e_x. The number of bits N_e determine the dynamic range of the representation.

mantissa An N_m-bit, signed, mantissa m_x. The number of bits N_m, not including the sign bit, determine the precision of the representation. Assuming correct rounding, the mantissa m_x has an inherent accuracy of $\pm \frac{1}{2}$ lsb, where $lsb = 2^{-Nm+1}$ is the weight for the least significant bit.

The corresponding value of x is given by

$$x = m_x 2^{e_x} \qquad (10)$$

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For the sake of discussion, we will assume that the input of the floating-point CORDIC is normalized. This means that the mantissa lies within the range given by:

$$1.00...00_2 \leqq m_x \leqq 1.11...11_2$$
$$1 \leqq m_x \leqq 2 - lsb \quad (11)$$

The IEEE 754 Standard for Binary Floating-Point Arithmetic allows representations for denormalized numbers, zero, infinity and "Not a Number" (NaN). It has to be mentioned here that all of these too can be elegantly handled by the floating-point CORDIC implementation presented in the present patent application. To deal with this in detail, however, is beyond the scope of this patent application.

The invention will be further explained referring to the figures in which some preferred embodiments are shown, by way of example.

Figure 1 shows a part of the (x,y) floating-point domain;

Figure 2 shows a CORDIC-arrangement;

Figure 3 shows a sequential CORDIC-arrangement;

Figure 4 shows a parallel CORDIC-arrangement.

Before the working of the floating-point CORDIC is explained, first, the following observation is made: the floating-point CORDIC works on floating-point vectors (x,y). All the possible values for the vector (x,y) lie in the floating-point domain, as is visualized in figure 1. The boxed areas represent regions in the domain in which the x and y exponents are constant. The points within such a region represent all possible values for the floating-point numbers with normalized mantissa. In the example shown in figure 1, we have taken $N_m = 4$, giving $1{,}000_2 \leqq m_x, m_y \leqq 1{,}111_2$. The large box in the top-right corner of the figure represents the region with $e_x = 2$, $e_y = 2$. The figure only shows a part of the domain and only the first quadrant, for positive vectors. It should be extended by mirroring in the x- and y-axes.

Now, there will be explained how, in accordance with the present invention, a floating-point CORDIC algorithm that can rotate a floating-point vector (x,y) over a floating-point angle α is derived. First, the floating-point CORDIC will be defined and a representation of the angle α in an internal floating-point format will be given.

In the floating-point CORDIC, a floating-point vector $(x,y)_{in}$ is rotated to $(x,y)_{out}$ over the floating-point angle of rotation α. How this angle α is derived depends on whether the mode of operation is vectoring or rotation.

Figure 2 shows a general arrangement of a CORDIC capable of computing output data $(x,y)_{out}$ to such precision that the error introduced by the CORDIC computation is smaller than the error that can be accounted to the (in)accuracy of the input data. The arrangement of figure 2 comprises four elements: a pre-rotation unit 1, a core 2, a post-rotation unit 4, and a rotation handler 3.

The pre-rotation unit 1 has two inputs x_{in}, y_{in} and three outputs x_{pre}, y_{pre}, β_{pre}. The inputs x_{in}, y_{in} are floating-point numbers, as are the outputs x_{pre}, y_{pre}. β_{pre} is represented by a tuple $(\sigma_{\pi/2,pre}, \sigma_{\pi,pre})$ with $\sigma_{\pi/2,pre}$, $\sigma_{\pi,pre} \in \{0,1\}$ and $\beta_{pre} = \sigma_{\pi/2,pre} \cdot \pi/2 + \sigma_{\pi,pre} \cdot \pi$. The function of the pre-rotation unit 1, in combination with the post-rotation unit 4 is to solve the problem of accurately representing angles (of vectors) close to the x- and y-axes. The operation will be explained hereinafter.

The core 2 has four inputs x_{pre}, y_{pre}, γ_{in} and mode and three outputs x_{core}, y_{core} and γ_{out}. The inputs are connected to the outputs x_{pre}, y_{pre}, respectively of the pre-rotation unit 1. The input signal mode denotes whether the mode of operation is vectoring or rotation. The purpose of the core 2 is to compute the output signals x_{core}, y_{core} from the input signals x_{pre}, y_{pre} in accordance with the desired vectoring or rotation mode.

The post-rotation unit 4 has three inputs x_{core}, y_{core}, β_{post} and two outputs x_{out}, y_{out}. The post-rotation unit 4 performs a rotation on the input signals x_{core}, y_{core} present on its inputs, whenever there has been pre-rotations by the pre-rotation unit 1. The post-rotation unit 4 is controlled by the rotation handler 3 through the input β_{post}.

The rotation handler 3 has three inputs β_{pre}, mode, β_{in} and two outputs β_{out}, β_{post}. The inputs β_{pre} and mode are defined above. The input β_{in} receives a tuple $(\sigma_{\pi/2,in}, \sigma_{\pi,in})$. The output β_{out} is represented by a tuple $(\sigma_{\pi/2,out}, \sigma_{\pi,out})$ and β_{post} by a tuple $(\sigma_{\pi/2,post}, \sigma_{\pi,post})$.

The rotation handler 3 computes the angles β_{post}, β_{out} from the input β_{pre}, β_{in} depending on the mode. If the mode is vectoring, then the angle output β_{out} is the same as the angle produced by the pre-rotations β_{pre}; no post rotation is necessary. If the mode is rotation, then the angle that the input vector should be rotated over is given by β_{in}; since the input is already rotated over β_{pre} by the pre-rotations, post-rotations must correct this by rotating over $\beta_{post} = \beta_{in} - \beta_{pre}$.

First, an algorithm allowed to be implemented in the architecture of figure 2 will be described. The floating-point CORDIC consists of three distinctive operations. They are:

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1. A pre-rotation over the angle β_{pre}.
2. A core-rotation over the angle γ.
3. A post-rotation over the angle β_{post}.

In the first step (pre-rotation) the input data, (x_{in}, y_{in}), is rotated to the region of convergence using accuracy-preserving rotations over $+\pi/2$ and $+\pi$ radians. These rotations take effect in changing the signs and exchanging the exponents and mantissas between x and y and therefore do not affect the precision that is present in the data.

The rotation over $+\pi/2$ radians is performed if $|y_{in}| > |x_{in}|$, otherwise no rotation is performed. The result of this rotation is an intermediate vector (x_{int}, y_{int}).

```
if |y_in| > |x_in| then
      σ_π/2,pre = 1
      x_int = -y_in
      y_int = x_in
else                                                    (12)
      σ_π/2,pre = 0
      x_int = x_in
      y_int = y_in
end if
```

The rotation over π radians is performed if the resulting x_{int} is negative. The combination of these rotations brings the input data to the halfplane $x \geq 0$.

```
if x_int < 0 then
      σ_π,pre = 1
      x_pre = -x_int
      y_pre = -y_int
else                                                    (13)
      σ_π,pre = 0
      x_pre = x_int
      y_pre = y_int
end if
```

The following properties now hold for the resulting (x_{pre}, y_{pre}) data:

$$e_{x,pre} \geq e_{y,pre} \quad (14)$$

$$x_{pre} \geq |y_{pre}| \geq 0 \quad (15)$$

The pre-rotations serve two purposes. Firstly, they make it possible to accurately represent angles which are close to the x- and y-axes, rather than just angles close to the positive x-axis. Secondly, the formulas and the calculations in the core 2 can be greatly simplified due to the prior knowledge of condition (14).

The value of the angle β_{pre} is given by

$$\beta_{pre} = \sigma_{\pi,pre} \cdot \pi + \sigma_{\pi/2,pre} \cdot \pi/2 \quad (16)$$

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with $\sigma_{\pi/2,pre}$, $\sigma_{\pi,pre} \in \{0, 1\}$.

Step 2 (core rotation) of the floating-point CORDIC algorithm requires the definition of an angle exponent.

Looking at the floating-point domain in figure 1 we see that when two regions have the same difference in exponents e_x-e_y they share the same domain of convergence and accuracy in angles. This is due to the equivalence:

$$\tan^{-1}\left(\frac{m_y \cdot 2^{e_y}}{m_x \cdot 2^{e_x}}\right) = \tan^{-1}\left(\frac{m_y}{m_x} \cdot 2^{e_y - e_x}\right) \qquad (17)$$

Therefore, in the vectoring mode, an angle exponent ξ is chosen as

$$\xi = e_{y,pre} - e_{x,pre} \qquad (18)$$

In the rotation mode, the angle exponent ξ is taken from the input angle:

$$\xi = \xi_{in} \qquad (19)$$

The angle exponent is an indication of both the maximum value (range) that a floating-point angle α can attain, and of the absolute precision of the angle. The relative precision is, by definition, more or less constant.

Combining this with the property (14) placed upon the exponents of the rotated data, we have that:

$$\xi_{min} \leqq \xi \leqq 0 \qquad (20)$$

where $\xi_{min} = -(2^{Ne}-1)$ is the smallest value that the angle exponent can attain in equation (18).

In the second step (core-rotation), the angle exponent ξ is computed according to formulas (18) and (19), the angle exponent selects the proper base tangent sequence $A_\xi = (a_{0,\xi}, a_{1,\xi},..., a_{n\xi-1,\xi})$ from a set of base tangent sequences $\{A_0, A_{-1},..., A_{\xi min}\}$.

Each of these base tangent sequences is specifically designed to operate on angles with given domain of convergence and accuracy as determined by the region of the floating-point (x, y)-domain. Each A_ξ also defines

1. a base angle sequence $\{\alpha_i\}_\xi$, consisting of the n_ξ angles $\alpha_{0,\xi}, \alpha_{1,\xi},..., \alpha_{n\xi-1,\xi}$,
2. a domain of convergence r_ξ, computed from the base angles in correspondence with formula (7),
3. a scaling factor K_ξ, according to formula (3),
4. an accuracy determined by the minimum angle $\alpha_{min,\xi} = \alpha_{n,\xi-1,\xi}$.

The accuracy condition on the minimum base angle $\alpha_{min,\xi}$ and the feasibility condition on domain of convergence r_ξ are:

$$\alpha_{min,\xi} = \tan^{-1}(2^{\xi - N_m - 1}) \qquad (21)$$

where N_m is the number of bits of the mantissa m_x as defined above and

$$r_\xi \geqq \tan^{-1}(2^\xi) \qquad (22)$$

This base tangent sequence A_ξ is used to perform micro-rotations, where the general recursion (1) is replaced by

$$\begin{aligned} x_{i+1} &= x_i - \sigma_i\, a_{i,\xi}\, y_i \\ y_{i+1} &= y_i + \sigma_i\, a_{i,\xi}\, x_i \end{aligned} \qquad (23)$$

with the input and output to the recursion being:

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$$\begin{aligned} x_0 &= K_\xi^{-1}\, x_{pre} \\ y_0 &= K_\xi^{-1}\, y_{pre} \end{aligned} \qquad \text{and} \qquad \begin{aligned} x_{core} &= x_{n\xi} \\ y_{core} &= y_{n\xi} \end{aligned} \tag{24}$$

In the vectoring mode, the σ_i are chosen according to

$$\sigma_i = \begin{cases} +1 \text{ if } y_i < 0 \\ -1 \text{ if } y_i \geq 0 \end{cases} \tag{25}$$

In the rotation mode, the σ_i are determined by the input angle:

$$\sigma_i = \sigma_{i,in} \tag{26}$$

In both cases, $\sigma_{i,out} = \sigma_i$.

The angle γ is represented by a tuple (ξ, ζ), where ζ is the angle mantissa which is represented by the sequence of σ-bits. $\{\sigma_0, \sigma_1, ..., \sigma_{n\xi-1}\}$

In the third step (post-rotation), the angle β_{post} is computed in the rotation handler 3, according to

$$\begin{aligned} \beta &= \begin{cases} \beta_{pre} \text{ if mode = vectoring} \\ \beta_{in} \text{ if mode = rotating} \end{cases} \\ \beta_{post} &= \beta - \beta_{pre} \\ \beta_{out} &= \beta \end{aligned} \tag{27}$$

The input data, $(x,y)_{core}$, is rotated over the angle β_{post}. The result of the post-rotation is the output vector $(x,y)_{out}$. The post-rotation follows the basic scheme of the pre-rotation. The rotation over $\pi/2$ radians is performed if $\sigma_{\pi/2,post} = 1$, otherwise no rotation is performed. The result of this rotation is an intermediate vector $(x,y)_{temp}$.

$$\begin{aligned} &\text{if } \sigma_{\pi/2,post} = 1 \text{ then} \\ &\quad \begin{cases} x_{temp} = -y_{core} \\ y_{temp} = x_{core} \end{cases} \\ &\text{else} \\ &\quad \begin{cases} x_{temp} = x_{core} \\ y_{temp} = y_{core} \end{cases} \\ &\text{end if} \end{aligned} \tag{28}$$

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The rotation of π radians is performed if $\sigma_{\pi,post} = 1$, otherwise no rotation is performed.

$$\begin{aligned}
&\text{if } \sigma_{\pi,post} = 1 \text{ then} \\
&\quad \begin{cases} x_{out} = -x_{temp} \\ y_{out} = -y_{temp} \end{cases} \\
&\text{else} \\
&\quad \begin{cases} x_{out} = x_{temp} \\ y_{out} = y_{temp} \end{cases}
\end{aligned} \tag{29}$$

The floating-point angle α is represented by the tuple (β,γ). The value of alpha is given by the sum of the two elements:

$$\alpha = \beta + \gamma \tag{30}$$

The angle β is an integer multiple of $\pi/2$, and is, in itself, represented as a tuple $(\sigma_\pi,\sigma_{\pi/2})$. The value of β is given by:

$$\beta = \sigma_\pi \cdot \pi + \sigma_{\pi/2} \cdot \frac{\pi}{2} \tag{31}$$

where $\sigma_\pi, \sigma_{\pi/2} \in \{0,1\}$.

The angle γ, with $|\gamma| \leq \pi/4$, is represented by a tuple (ξ,ζ), where ξ is the angle exponent and ζ is the angle mantissa represented by the sequence $(\sigma_0, \sigma_1, ..., \sigma_{n\xi-1})$; the value of γ is given by

$$\gamma = \sum_{i=0}^{n\xi-1} \sigma_i \alpha_{i,\xi} \tag{32}$$

Within the arrangement according to figure 2 there are basically two approaches to implement the desired CORDIC. The first approach relates to an algorithm coupled to a sequential architecture, whereas the second approach relates to an algorithm coupled to a parallel, pipelined architecture.

The difference between the two approaches is how the rotation over the floating-point angle γ is implemented. This in turn has effect on how the base tangent sequences A_ξ are chosen.

For the sequential floating-point CORDIC, where the micro-rotations and scaling iterations are performed sequentially, we take the least attainable number of operations per A_ξ, and thus achieve a minimum latency in number of clock cycles. This gives rise to a set of base tangent sequences, as shown in table 1 for an example sequential floating-point CORDIC with $N_m = 12$.

For the parallel floating-point CORDIC, where each micro-rotation is assigned to and implemented in a micro-rotation stage, we take the least complexity per micro-rotation, and thus achieve a high throughput and minimal area. The A_ξ are then as shown in table 2 for an example parallel floating-point CORDIC with $N_m = 12$.

The sequential floating-point CORDIC which we explain first follows the main scheme as shown in figure 2 of which the core 2 is now described in detail with reference to figure 3.

Figure 3 shows a preferred embodiment of the core 2 in a sequential floating-point CORDIC arrangement. The core 3 consists of three parts:

(a) an exponent handler 21 receiving the exponents $e_{x,pre}$, $e_{y,pre}$ of the vector x_{pre}, y_{pre} and computing a CORDIC table selector Ξ, and alignment factors $a_{y,pre}$, $a_{x,core}$ and $a_{y,core}$, exponents $e_{x,core}$, $e_{y,core}$ of the vector x_{core}, y_{core} and, depending on the signal mode, either receiving from the operator an angle exponent ξ_{in} or computing an angle exponent ξ_{out};

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(b) an instruction sequencer 22 receiving the cordic table selector Ξ from the exponent handler 21 and producing a sequence of instructions I;

(c) an instruction execution unit 23 receiving the mantissas $m_{x,pre}$, $m_{y,pre}$ of the vector x_{pre}, y_{pre}, receiving the alignment factors $a_{y,pre}$, $a_{x,core}$ and $a_{y,core}$ from the exponent handler 21 and receiving the sequence of instructions I supplied by the instruction sequencer 22 and, depending on the signal mode, either receiving an angle mantissa ζ_{in} supplied by the operator or computing an angle mantissa ζ_{out} producing mantissas $m_{x,core}$, $m_{y,core}$ of the vector x_{core}, y_{core}.

The core rotation over the angle γ in the sequential floating-point CORDIC consists of three steps. They are:

1. computing exponents ($e_{x,core}$, $e_{y,core}$), an angle exponent ξ, a CORDIC table selector Ξ, and alignment factors $a_{y,pre}$, $a_{x,core}$, $a_{y,core}$
2. selection of a sequence of instructions I determined by the CORDIC table selector Ξ, to perform
   i. loading of initial values
   ii. mantissa alignment
   iii. scaling of the mantissas
   iv. performing micro-rotations
3. execution of the sequence of instructions I to carry out a rotation or vectoring operation on the vector (x_{pre}, y_{pre}) over the angle γ to give the vector (x_{core}, y_{core}).

We are placing the (implementation) constraint here that all calculations in the core are done in block floating-point. This means that exponent is fixed throughout the calculation and the mantissa is not re-normalized between consecutive additions. This is to prevent the use of expensive floating-point additions for the micro-rotations.

We do take precautions against the possible overflow of the y-mantissa datapath. We align the mantissa and change its exponent accordingly. To guarantee that the overflow is no more than two bits we take:

$$e_{y,core} - e_{x,core} \geq \xi \qquad (33)$$

Due to the pre-rotation, $e_{y,pre} \leq e_{x,pre}$, and so only the y-mantissa ever needs to be aligned.

We force the scaling factor K_ξ to be such that the multiplication with the inverse K_ξ^{-1} in the prescaling of formula (24) is cheap in hardware. For a base tangent sequence A_ξ, with domain of convergence satisfying condition (22), the scaling factor is given by

$$K_\xi \approx (1-2^{2\xi-1})^{-1} \qquad (34)$$

The scaling factor of (34) is optimal in the sense of combining an easy multiplication of the inverse scaling factor and a minimal number of micro-rotations. The multiplication with the inverse scaling factor then degenerates to a shift and subtract operation, similar to a CORDIC micro-rotation.

The scaling factor quickly approaches 1 as the angle exponent ξ gets smaller. Hence, after a certain limit, we revert to a generic base tangent sequence A_ξ which has a scaling factor of $K_\xi = 1$ to the required precision and defined by

$$a_{i,\xi} = 2^{\xi-i}, \; i \in \{0,1,...,N_m+1\} \qquad (35)$$

This base tangent sequence has the required domain of convergence r_ξ as set in equation (22).

The limiting value L of ξ at which the scaling factor K_ξ becomes 1 to enough precision is given by

$$L = \left\lfloor \frac{-N_m - 1}{2} \right\rfloor \qquad (36)$$

In practice this means that for, say, a 12-bit floating-point CORDIC with L = -7, the 7 base tangent sequences $A_0,...,A_{-6}$ must be implemented.

The accuracy for the core datapath of the Floating-point CORDIC follows general guidelines known to the person skilled in the art. The datapath is extended with guard bits on the left (msb) to prevent overflow and extra bits on the right (lsb) to defy the effect of accumulative round-off errors in the micro-rotations. Simulations have proven these measures to be effective.

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The base tangent sequences A_ξ for a 12-bit floating-point CORDIC are presented in table 1.

Similar tables may be calculated for a 24-bit mantissa, as required by the IEEE 754 std for single precision floating-point numbers.

In step 1 the angle exponent ξ is computed according to formulas (18) en (19); the exponents are computed as follows (taking the overflow condition (33) into account)

$$e_{x,core} = e_{x,pre}$$
$$e_{y,core} = \max (e_{y,pre}, e_{x,pre} + \xi) \quad (37)$$

The alignment factors are computed as

$$a_{y,pre} = (e_{y,pre} - e_{y,core})$$
$$a_{x,core} = (e_{y,core} - e_{x,core})$$
$$a_{y,core} = (e_{x,core} - e_{y,core}) \quad (38)$$

The table selector is taken as

$$\Xi = \max (\xi, L) \quad (39)$$

In step 2, the instructing sequence I_Ξ is selected according to formula (39) and delivered to the execution unit 22 to perform the rotation as determined by the base tangent sequence A_ξ.

In step 3, initial value loading, mantissa alignment and scaling are performed according to

$$m_x[0] = K_\xi^{-1}.m_{x,pre}$$
$$m_y[0] = K_\xi^{-1}.m_{y,pre}.2^{ay,pre} \quad (40)$$

The micro-rotations are performed sequentially according to the recursion

$$m_x[i+1] = m_x[i] - \sigma_i.a_{i\xi}.2^{ax,core}.m_y[i]$$
$$m_y[i+1] = m_y[i] + \sigma_i.a_{i\xi}.2^{ay,core}.m_x[i] \quad (41)$$

In the vectoring mode, the σ_i are determined from

$$\sigma_i = \begin{cases} 1 & \text{if } m_y[i] < 0 \\ -1 & \text{if } m_y[i] \geq 0 \end{cases} \quad (42)$$

In the rotation mode, the σ_i are determined from the input angle:

$$\sigma_i = \sigma_{i,in} \quad (43)$$

The values of the mantissas ($m_{x,core}$, $m_{y,core}$) are given by:

$$m_{x,core} = m_x[n_\xi]$$
$$m_{y,core} = m_y[n_\xi] \quad (44)$$

Having described a sequential floating-point CORDIC, now a parallel/pipelined floating-point CORDIC will be described. It follows the main scheme as shown in figure 2 of which the core 2 is now described in detail with reference to figure 4.

Figure 4 shows a design of a core 2 to be used in such a parallel architecture. In figure 4 the core 2 comprises:

(a) an exponent handler 24 receiving the exponents $e_{x,pre}$, $e_{y,pre}$ of the vector x_{pre}, y_{pre} and computing a CORDIC table selector Ξ, alignment factors $a_{y,coarse}$, $a_{y,fine}$, $a_{y,fixed}$, $a_{y,fixed}$, exponents $e_{x,coarse}$, $e_{y,coarse}$ of a vector x_{coarse}, y_{coarse} and, depending on the signal mode, either receiving from the operator an angle exponent ξ_{in} or computing an angle exponent ξ_{out};

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(b) a coarse core 25 receiving the mantissas $m_{x,pre}$, $m_{y,pre}$ of the vector x_{pre}, y_{pre} and receiving the alignment factor $a_{y,coarse}$ from the exponent handler 24 and, depending on the signal mode, receiving a coarse angle mantissa $\zeta_{in,coarse}$ supplied by the operator, or producing $\zeta_{out,coarse}$, to compute mantissas $m_{x,coarse}$, $m_{y,coarse}$ of the vector x_{coarse}, y_{coarse};

(c) a fine core 26 receiving the mantissas $m_{x,coarse}$, $m_{y,coarse}$ from the coarse core 25 and receiving the alignment factors $a_{y,fine}$, $a_{y,fixed}$ and $a_{y,fixed}$ from the exponent handler 24 and, depending upon the signal mode, receiving a fine angle mantissa $\zeta_{in,fine}$ supplied by the operator, or producing $\zeta_{out,fine}$, to compute the mantissas $m_{x,core}$, $m_{y,core}$ of the vector x_{core}, y_{core};

wherein the angle mantissa ζ is represented by a tuple ζ_{coarse}, ζ_{fine} and, depending on the signal mode, is either input by the operator as ζ_{in} or computed and output as ζ_{out}.

The core-rotation over the angle γ in the parallel floating-point CORDIC consists of three steps. They are:

1. computing exponents ($e_{x,core}$, $e_{y,core}$), an angle exponent ξ, a CORDIC table selector Ξ, and alignment factors $a_{y,coarse}$,$a_{y,fine}$, $a_{x,fixed}$, $a_{y,fixed}$,
2. carrying out alignment and scaling of the mantissas and carrying out coarse micro-rotations,
3. carrying out further alignment of the mantissas and carrying out fine micro-rotations.

The floating-point angle γ is said to be "coarse" if its angle exponent ξ satisfies $0 \leq \xi < L$. Likewise, it is said to be "fine" if $L \leq \xi < \xi_{min}$. The limit L between fine and coarse is given by

$$L = \left\lfloor \frac{-N_m - 2}{2} \right\rfloor \qquad (45)$$

The CORDIC table selector Ξ selects the related base tangent sequence, coarse and fine respectively, as shown in table 2 for a 12-bit parallel floating-point CORDIC. Ξ is given by

$$\Xi = \begin{cases} \text{coarse} & \text{if } \xi > L \\ \text{fine} & \text{if } \xi \leq L \end{cases} \qquad (46)$$

The micro-rotations, both coarse and fine, take place in block floating-point datapaths that compute on mantissas only, and are devoid of floating-point adders. These datapaths can have different exponents, and thus mantissas have to be re-aligned when transferred from one datapath to another. We distinguish four block-floating-point datapaths:

- Two for the coarse micro-rotations, the x and y datapath, with (fixed) exponents $e_{x,coarse}$ and $e_{y,coarse}$. When rotating over a coarse angle with $\xi > L$, these exponents must be equal to each other. Otherwise, for fine angles, the exponent is taken equal to that of the fine y-datapath that follows it.

$$e_{y,coarse} = e_{x,coarse} \text{ if } \xi > L$$
$$e_{y,coarse} = e_{y,fine} \text{ if } \xi \leq L \qquad (47)$$

and

$$e_{x,coarse} = e_{x,pre} \qquad (48)$$

- Two for the fine micro-rotations, the x and y datapath, with (fixed) exponents $e_{x,fine}$ and $e_{y,fine}$. The exponent for the y fine datapath must be chosen such that no overflow occurs during computation and still achieve maximum relative precision. This is guaranteed if

$$e_{y,fine} = \max(e_{x,coarse} + \xi, e_{y,coarse}) \qquad (49)$$

and

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$e_{x,fine} = e_{x,coarse}$ (50)

The coarse base tangent sequence is characterized by:

1. an angular basis $\{\alpha_i\}$, consisting of n + m base angles numbered $\alpha_0, ..., \alpha_{n+m-1}$, where $m = N_m + 2$,
2. a corresponding set of base tangents $\{a_i\}$, such that $a_i = \tan\alpha_i$,
3. a scaling factor K_{coarse}, with

$$K_{coarse} = \prod_{i=0}^{n+m-1} (1+a_i^2)^{1/2} \quad (51)$$

The scaling factor K_{coarse} is chosen, along with the a_i, such that the multiplication with K_{coarse}^{-1} is cheap to implement in hardware.

4. an angle domain of convergence, r_{coarse}, given by

$$r_{coarse} = \sum_{i=0}^{n+m-1} \alpha_i + \alpha_{min} \quad (52)$$

and satisfying $r_{coarse} \geq \pi/4$.

5. an angle resolution α_{min} as determined by the minimum angle $\alpha_{min,coarse} = \alpha_{n+m-1}$.
6. a sufficient datapath width, such that the relative precision is not affected for $|\gamma| > r_{fine}$, where r_{fine} is the domain of convergence of the "fine" CORDIC.

The coarse base tangent sequence is implemented partially by the coarse micro-rotations for i = 0,1,...,n-1, and partially by the fine micro-rotations for i = n,n + 1,...,n + m-1.

The "fine" base tangent sequence is characterised by:

1. a maximum angle domain of convergence r_{fine}
2. an angle resolution α_{min} that varies with the angle exponent, such that the relative precision of the angle is constant and that the precision in the input vector (from which the angle is computed by vectoring) is preserved.
3. $K_{fine} = 1$ to enough precision.
4. a sufficient datapath width, such that the precision of the mantissas is not affected by roundoff errors, and also such that no overflow occurs in computations. The fine base tangent sequence relies on a linearization of the rotation.
5. the base tangents $a_{i,\xi}$ being given by

$$a_{i,\xi} = 2^{\xi-i},\ i \in \{0,1,...,N_m+1\} \quad (53)$$

The fine base tangent sequence is implemented by the fine micro-rotations i = n,n + 1,...,n + m-1.

In step 1, the angle exponent ξ is computed according to formulas (18) and (19); the exponents are computed according to formulas (47) - (50); the table selector Ξ is computed according to formula (46); the alignment factors are computed from the differences in the exponents of the individual datapaths, and given by

$$\begin{cases} a_{y,fine} = e_{y,coarse} - e_{y,fine} \\ a_{x,fixed} = e_{x,coarse} - e_{y,fine} + h \\ a_{y,fixed} = e_{y,coarse} - e_{x,fine} + h \\ a_{y,coarse} = e_{y,pre} - e_{y,coarse} \end{cases} \quad (54)$$

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with

$$h = \begin{cases} L & \text{if } L < \xi \\ \xi & \text{if } L \geq \xi \end{cases} \quad (55)$$
$$= \min(L, \xi)$$

In step 2 the "coarse" micro-rotations are performed in the coarse core 26, which rotate vectors over an angle γ_{coarse}, with enough precision, such that the residue $\gamma_{fine} = \gamma - \gamma_{coarse}$ satisfies $|\gamma_{fine}| \leq r_{fine}$, where r_{fine} is the domain of convergence for the "fine" microrotations. The domain of convergence of the coarse microrotations r_{coarse} satisfies $r_{coarse} \geq \pi/4$ to assure proper continuation from the pre-rotation.

In the case that the angle exponent $\xi \leq L$, the micro-rotations are skipped, the y-mantissa is aligned to the datapath of the fine micro-rotations that follow; the recursion for the micro-rotations is given by:

$$m_{x,coarse}[i+1] = m_{x,coarse}[i]$$
$$m_{y,coarse}[i+1] = m_{y,coarse}[i] \quad (56)$$

for $i = 0 \ldots n-1$ with initialisation

$$m_{x,coarse}[0] = m_{x,pre} \quad (57)$$
$$m_{y,coarse}[0] = m_{y,pre} \cdot 2^{a_{y,coarse}}$$

Otherwise, for $L < \xi$ the recursion for the coarse microrotations is given by:

$$m_{x,coarse}[i+1] = m_{x,coarse}[i] - \sigma_i . a_1 . m_{y,coarse}[i]$$
$$m_{y,coarse}[i+1] = m_{y,coarse}[i] + \sigma_i . a_1 . m_{x,coarse}[i] \quad (58)$$

for $i = 0 \ldots n-1$ with initialisation

$$m_{x,coarse}[0] = K^{-1}_{coarse} \cdot m_{x,pre} \quad (59)$$
$$m_{y,coarse}[0] = K^{-1}_{coarse} \cdot m_{y,pre} \cdot 2^{a_{y,coarse}}$$

In the vectoring mode, the σ_i, are determined from

$$\sigma_i = \begin{cases} 1 & \text{if } m_{y,coarse}[i] < 0 \\ -1 & \text{if } m_{y,coarse}[i] \geq 0 \end{cases} \quad (60)$$

In the rotation mode, the σ_i, are determined from the input angle:

$$\sigma_i = \sigma_{i,in} \quad (61)$$

and the resulting mantissas are given by:

$$m_{x,coarse} = m_{x,coarse}[n]$$
$$m_{y,coarse} = m_{y,coarse}[n] \quad (62)$$

In step 3 the "fine" micro-rotations are performed in the fine core 27. These rotate vectors over the

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remaining γ_{fine}, with $|\gamma_{fine}| \leq r_{fine}$, utilising a linearization of the angle.

The recursion for the fine micro-rotations is given by:

$$m_{x,fine}[i+1] = m_{x,fine}[i] - \sigma_i.2^{-i}.m_{y,fixed}$$
$$m_{y,fine}[i+1] = m_{y,fine}[i] + \sigma_i.2^{-i}.m_{x,fixed} \quad (63)$$

for $i = n,...,n+m-1$ with initialisation

$$\begin{aligned} m_{x,fine}[n] &= m_{x,coarse} \\ m_{y,fine}[n] &= m_{y,coarse}.2^{a_{y,fine}} \\ m_{x,fixed} &= m_{x,coarse}.2^{a_{x,fixed}} \\ m_{y,fixed} &= m_{y,coarse}.2^{a_{y,fixed}} \end{aligned} \quad (64)$$

Like for the coarse micro-rotations, the σ_i are determined in the vectoring mode from

$$\sigma_i = \begin{cases} 1 & \text{if } m_{y,fine}[i] < 0 \\ -1 & \text{if } m_{y,fine}[i] \geq 0 \end{cases} \quad (65)$$

In the rotation mode, the σ_i are determined from the input angle:

$$\sigma_i = \sigma_{i,in} \quad (66)$$

The output vector (x_{core}, y_{core}) is given by

$$m_{x,core} = m_{x,fine}[n+m]$$
$$m_{y,core} = m_{y,fine}[n+m]$$
$$e_{x,core} = e_{x,fine}$$
$$e_{y,core} = e_{y,fine} \quad (67)$$

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Base tangent sequence	$\mathcal{A}_0$	$\mathcal{A}_{-1}$	$\mathcal{A}_{-2}$	$\mathcal{A}_{-3}$	$\mathcal{A}_{-4}$	$\mathcal{A}_{-5}$	$\mathcal{A}_{-6}$	$\mathcal{A}_\xi$
ξ	0	-1	-2	-3	-4	-5	-6	≤ -7
Ξ	0	-1	-2	-3	-4	-5	-6	-7
K_ξ	2	$\frac{8}{7}$	$\frac{32}{31}$	$\frac{128}{127}$	$\frac{512}{511}$	$\frac{2048}{2047}$	$\frac{8192}{8191}$	1
K_ξ^{-1}	$1-2^{-1}$	$1-2^{-3}$	$1-2^{-5}$	$1-2^{-7}$	$1-2^{-9}$	$1-2^{-11}$	$1-2^{-13}$	1
Cordic iteration	$a_{i,\xi}$							$a_{i,\xi}$
1	$2^{-0}+2^{-4}$	2^{-1}	$2^{-3}+2^{-4}$	$2^{-4}+2^{-5}$	$2^{-5}+2^{-7}$	2^{-6}	2^{-6}	$2^{\xi-0}$
2	$2^{-1}+2^{-3}$	2^{-3}	$2^{-3}+2^{-7}$	2^{-4}	2^{-5}	2^{-6}	2^{-7}	$2^{\xi-1}$
3	2^{-1}	2^{-3}	$2^{-4}+2^{-6}$	$2^{-5}+2^{-7}$	2^{-5}	2^{-6}	2^{-8}	$2^{\xi-2}$
4	$2^{-2}-2^{-7}$	2^{-4}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-9}	$2^{\xi-3}$
5	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-10}	$2^{\xi-4}$
6	2^{-4}	2^{-4}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-11}	$2^{\xi-5}$
7	2^{-5}	2^{-5}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-12}	$2^{\xi-6}$
8	2^{-6}	2^{-6}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-13}	$2^{\xi-7}$
9	2^{-7}	2^{-7}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-14}	$2^{\xi-8}$
10	2^{-8}	2^{-8}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-15}	$2^{\xi-9}$
11	2^{-9}	2^{-9}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-16}	$2^{\xi-10}$
12	2^{-10}	2^{-10}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-17}	$2^{\xi-11}$
13	2^{-11}	2^{-11}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-18}	$2^{\xi-12}$
14	2^{-12}	2^{-12}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-19}	$2^{\xi-13}$
15	2^{-13}	2^{-13}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	—	—
16	—	2^{-14}	—	—	—	—	—	—

Table 1: The set of base tangent sequences $\mathcal{A}_\xi$ for the sequential floating-point Cordic

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Base tangent sequence	$\mathcal{A}_0 \ldots \mathcal{A}_{-6}$	$\mathcal{A}_\xi$
ξ	$0 \ldots -6$	≤ -7
Ξ	coarse	fine
K_ξ	2	1
K_ξ^{-1}	2^{-1}	1
coarse micro-rotations	$a_{i,\xi}$	$a_{i,\xi}$
1	$2^{-0} + 2^{-4}$	—
2	$2^{-1} + 2^{-3}$	—
3	2^{-1}	—
4	$2^{-2} - 2^{-7}$	—
5	2^{-3}	—
6	2^{-4}	—
7	2^{-5}	—
8	2^{-6}	—
fine micro-rotations	$a_{i,\xi}$	$a_{i,\xi}$
9	2^{-7}	2^{ξ}
10	2^{-8}	$2^{\xi-1}$
11	2^{-9}	$2^{\xi-2}$
12	2^{-10}	$2^{\xi-3}$
13	2^{-11}	$2^{\xi-4}$
14	2^{-12}	$2^{\xi-5}$
15	2^{-13}	$2^{\xi-6}$
16	2^{-14}	$2^{\xi-7}$
17	2^{-15}	$2^{\xi-8}$
18	2^{-16}	$2^{\xi-9}$
19	2^{-17}	$2^{\xi-10}$
20	2^{-18}	$2^{\xi-11}$
21	2^{-19}	$2^{\xi-12}$
22	2^{-20}	$2^{\xi-13}$

Table 2: The set of base tangent sequences $\mathcal{A}_\xi$ for the parallel floating-point Cordic

Claims

1. A CORDIC arrangement to rotate an input vector (x_{in},y_{in}) over an angle α to an output vector (x_{out}, y_{out}), characterized in that x_{in}, y_{in}, x_{out}, y_{out} are represented by floating-point numbers with respective mantissas (m_x, m_y) and respective angle exponents (e_x, e_y) and the CORDIC arrangement comprises:

   (a) a pre-rotation unit (1) receiving the input vector (x_{in}, y_{in}) to rotate the input vector (x_{in}, y_{in}) over an angle β_{pre} to give a vector (x_{pre}, y_{pre});

   (b) a core (2) receiving the vector (x_{pre}, y_{pre}) from the pre-rotation unit (1) to rotate the vector (x_{pre}, y_{pre}) over an angle γ to give a vector (x_{core}, y_{core}), where the angle γ, depending on a signal mode supplied by an operator, is either supplied by the operator as γ_{in} or computed and output as γ_{out};

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(c) a rotation handler (3) receiving the angle β_{pre} from the pre-rotation unit (1) and the signal mode supplied by an operator, and a possible angle β_{in} supplied by the operator to compute angles β_{post}, β_{out} in dependence thereon;

(d) a post-rotation unit (4) receiving the vector (x_{core}, y_{core}) from the core (2) and receiving the angle β_{post} from the rotation handler (3) to rotate the vector (x_{core}, y_{core}) over the angle β_{post} to give the output vector (x_{out}, y_{out});

wherein

(a) the floating-point angle α is represented by a tuple (β, γ), β being the sum of β_{pre} and β_{post}, and γ being represented by a tuple (ξ, ζ), of which ξ is an angle exponent and ζ is an angle mantissa;

(b) α equals the sum of β and γ.

2. A CORDIC arrangement according to claim 1 characterized in that the core (2) comprises:

(a) an exponent handler (21) receiving the exponents ($e_{x,pre}$,$e_{y,pre}$) of the vector (x_{pre}, y_{pre}) and computing a CORDIC table selector Ξ, and alignment factors $a_{y,pre}$, $a_{x,core}$ and $a_{y,core}$, exponents ($e_{x,core}$, $e_{y,core}$) of the vector (x_{core}, y_{core}) and, depending on the signal mode, either receiving from the operator an angle exponent ξ_{in} or computing an angle exponent ξ_{out};

(b) an instruction sequencer (22) receiving the cordic table selector Ξ from the exponent handler (21) and producing a sequence of instructions I;

(c) an instruction execution unit (23) receiving the mantissas ($m_{x,pre}$, $m_{y,pre}$) of the vector (x_{pre}, y_{pre}), receiving the alignment factors $a_{y,pre}$, $a_{x,core}$ and $a_{y,core}$ from the exponent handler (21) and receiving the sequence of instructions I supplied by the instruction sequencer (22) and, depending on the signal mode, either receiving an angle mantissa ζ_{in} supplied by the operator or computing an angle mantissa ζ_{out} producing mantissas ($m_{x,core}$, $m_{y,core}$) of the vector (x_{core}, y_{core}).

3. A CORDIC arrangement according to claim 1 characterized in that the core (2) comprises:

(a) an exponent handler (24) receiving the exponents ($e_{x,pre}$,$e_{y,pre}$) of the vector (x_{pre}, y_{pre}) and computing a CORDIC table selector Ξ, alignment factors $a_{y,coarse}$, $a_{y,fine}$, $a_{y,fixed}$, $a_{y,fixed}$, exponents ($e_{x,coarse}$, $e_{y,coarse}$) of a vector (x_{coarse},y_{coarse}) and, depending on the signal mode, either receiving from the operator an angle exponent ξ_{in} or computing an angle exponent ξ_{out};

(b) a coarse core (25) receiving the mantissas ($m_{x,pre}$, $m_{y,pre}$) of the vector (x_{pre}, y_{pre}) and receiving the alignment factor $a_{y,coarse}$ from the exponent handler (24) and, depending on the signal mode, receiving a coarse angle mantissa $\zeta_{in,coarse}$ supplied by the operator, or producing $\zeta_{out,coarse}$, to compute mantissas ($m_{x,coarse}$, $m_{y,coarse}$) of the vector (x_{coarse}, y_{coarse});

(c) a fine core (26) receiving the mantissas ($m_{x,coarse}$, $m_{y,coarse}$) from the coarse core (25) and receiving the alignment factors $a_{y,fine}$, $a_{y,fixed}$ and $a_{y,fixed}$ from the exponent handler (24) and, depending upon the signal mode, receiving a fine angle mantissa $\zeta_{in,fine}$ supplied by the operator, or producing $\zeta_{out,fine}$, to compute the mantissas ($m_{x,core}$, $m_{y,core}$) of the vector (x_{core}, y_{core});

wherein the angle mantissa ζ is represented by a tuple (ζ_{coarse}, ζ_{fine}) and, depending on the signal mode, is either input by the operator as ζ_{in} or computed and output as ζ_{out}.

4. A CORDIC method to rotate an input vector (x_{in}, y_{in}) received from an input means over an angle α to an output vector (x_{out}, y_{out}) to be supplied to an output means, characterized in that x_{in}, y_{in}, x_{out}, y_{out} are represented by floating-point numbers with respective mantissas (m_x, m_y) and respective angle exponents (e_x, e_y) comprising:

(a) a pre-rotation of the input vector (x_{in}, y_{in}) over an angle β_{pre} to give a vector (x_{pre}, y_{pre}) in accordance with formulas (12-16);

(b) a core rotation or a vectoring operation by rotating the vector (x_{pre}, y_{pre}) over an angle γ to give a vector (x_{core}, y_{core}), in accordance with formulas (18-26);

(c) calculation of angles β_{post} and β_{out} in accordance with formula (27);

(d) a post-rotation of the vector (x_{core}, y_{core}) over the angle β_{post} to give the output vector (x_{out}, y_{out}) in accordance with formulas (28, 29).

5. A CORDIC method according to claim 4 characterized in that step 4(b) comprises the steps of

(a) computing exponents ($e_{x,core}$, $e_{y,core}$), an angle exponent ξ, a CORDIC table selector Ξ, and alignment factors $a_{y,pre}$, $a_{x,core}$, $a_{y,core}$, in accordance with formulas (18, 19, 37-39);

(b) selection of a sequence of instructions I determined by the CORDIC table selector Ξ, to perform

i. loading of initial values

ii. mantissa alignment

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iii. scaling of the mantissas

iv. performing micro-rotations

(c) execution of the sequence of instructions I to carry out a rotation or vectoring operation on the vector (x_{pre}, y_{pre}) over the angle γ to give the vector (x_{core}, y_{core}) in accordance with formulas (40-44).

6. A CORDIC method according to claim 4 characterized in that step 4(b) comprises the steps of

(a) computing exponents ($e_{x,core}$, $e_{y,core}$), an angle exponent ξ, a CORDIC table selector Ξ, and alignment factors $a_{y,coarse}$,$a_{y,fine}$, $a_{x,fixed}$, $a_{y,fixed}$, in accordance with formulas (18, 19, 46-50, 54, 55);

(b) carrying out alignment and scaling of the mantissas in accordance with formulas (57, 59);

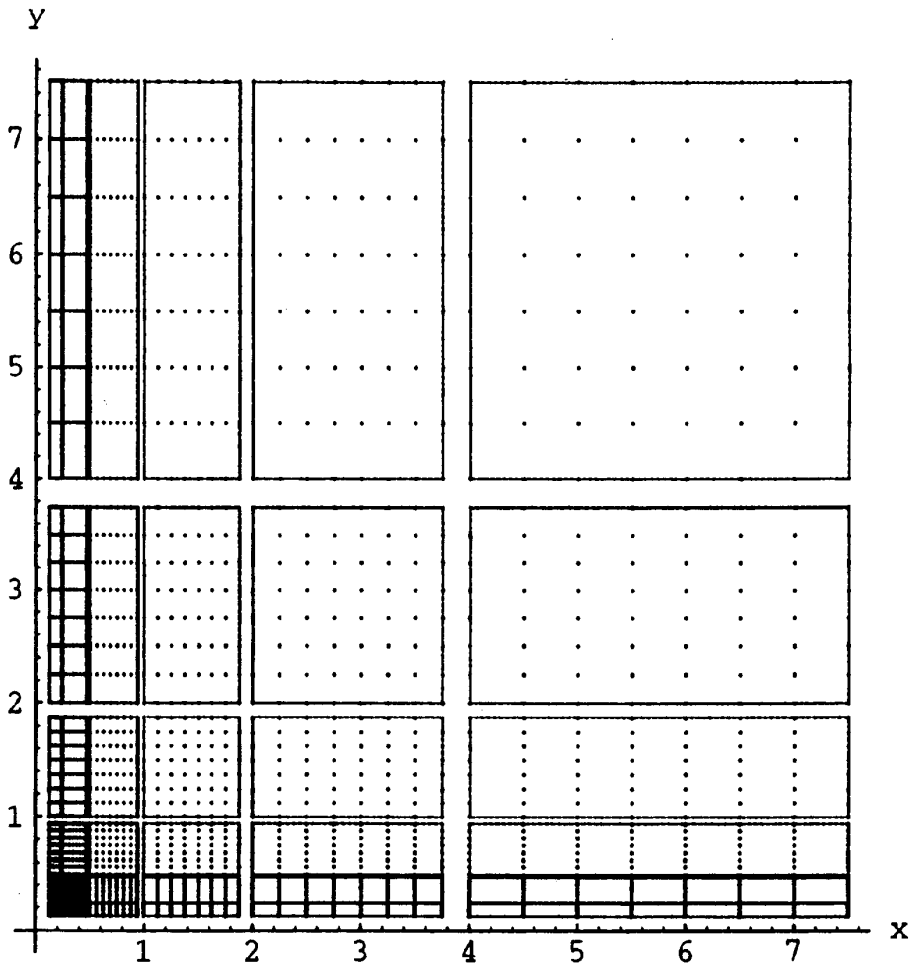
(c) carrying out coarse micro-rotations in accordance with formulas (56-62);

(d) carrying out further alignment of the mantissas in accordance with formula (64);

(e) carrying out fine micro-rotations in accordance with formulas (63-67).

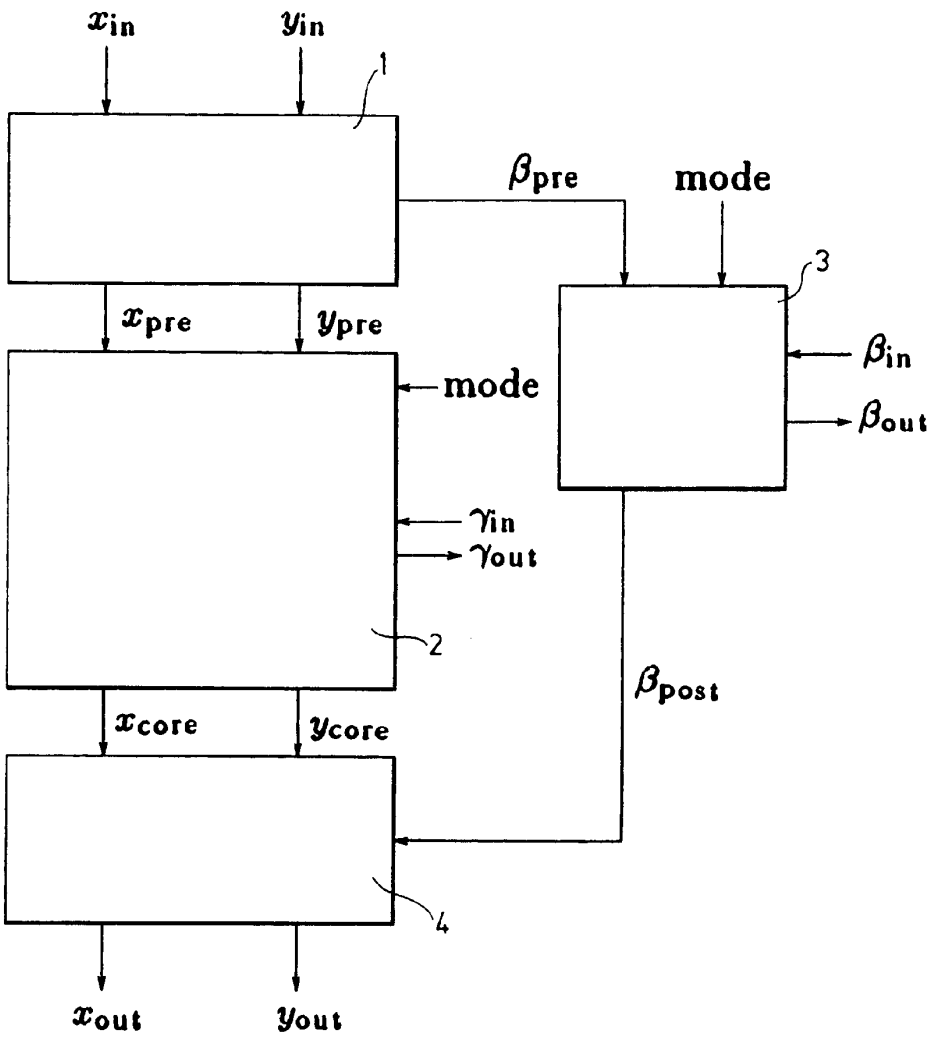
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fig-1



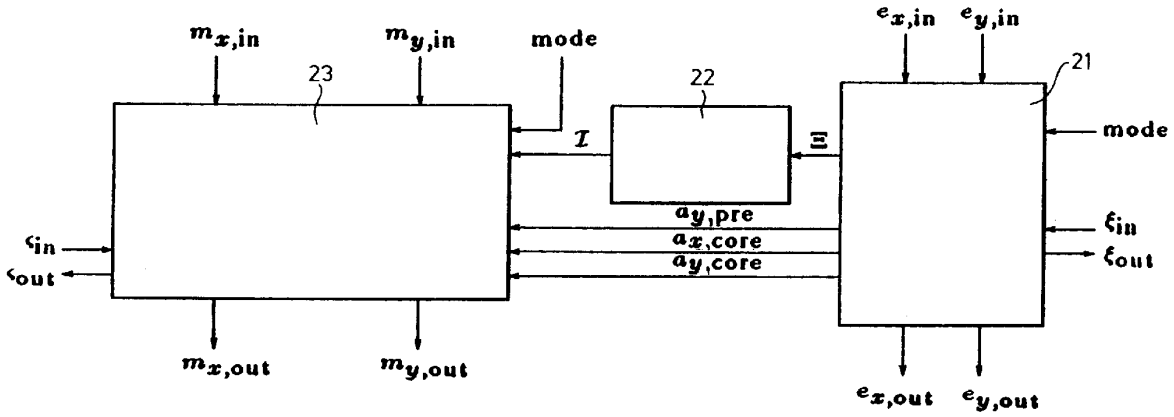
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Fig-2



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Fig - 3



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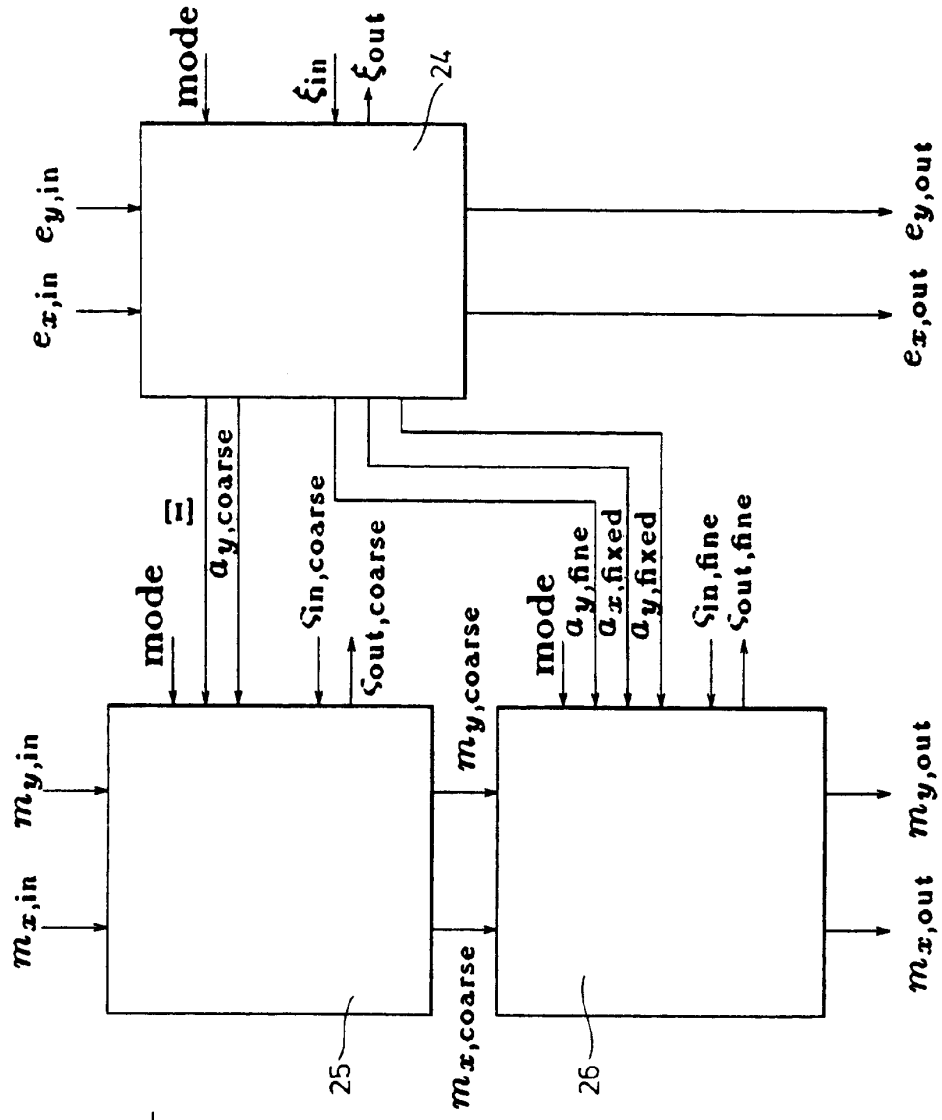


Fig - 4

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EUROPEAN SEARCH REPORT

Application Number
EP 93 20 1892

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PROCEEDINGS OF VLSI AND COMPUTERS. FIRST INTERNATIONAL CONFERENCE ON COMPUTER TECHNOLOGY, SYSTEMS AND APPLICATIONS. COMPEURO 87, HAMBURG, WEST GERMANY, 11-15 MAY 1987. 1987 , IEEE COMPUTER SOCIETY PRESS, WASHINGTON, DC, USA. pages 727 - 730 B. YANG, ET AL. 'Special computers: graphics, robotics' * figures 2,3 * ---	1,3,4,6	G06F7/544
A	PROCEEDINGS OF THE 10TH IEEE SYMPOSIUM ON COMPUTER ARITHMETIC, GRENOBLE, FRANCE, 26-28 JUNE 1991. 1991 , IEEE COMPUTER SOCIETY PRESS, LOS ALAMITOS, CA., USA. pages 272 - 281 A. DE LANGE ET AL. 'Design and Implementation of a Floating-point Quasi-Systolic General Purpose CORDIC Rotator for High-rate Parallel Data and Signal Processing' * sections 4, 5 ; figure 5.1 * ---	1,4	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G06F
A	PROCEEDINGS OF THE 1989 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, ISCAS '89, 8-11 MAY 1989, PORTLAND, OR, USA. vol. 1 , 1989 , IEEE COMPUTER SOCIETY PRESS, LOS ALAMITOS, CA., USA. pages 175 - 178 YU HEN HU ET AL. 'ANGLE RECODING METHOD FOR EFFICIENT IMPLEMENTATION OF THE CORDIC ALGORITHM' * page 177, left column, line 10 - line 12 * -----	1,4	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 November 1993	Verhoof, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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JPH0877282A ANALOG ARITHMETIC CIRCUIT

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ANALOG ARITHMETIC CIRCUIT

Abstract

PURPOSE: To provide the inexpensive, high-performance analog arithmetic circuit which does not require highly precise components. CONSTITUTION: This circuit consists of a 1st 1-bit D/A converter 11 which receives a DC voltage as the denominator of correction arithmetic, a subtracter 12 which receives the output of the 1-bit D/A converter 11 and a reference voltage and performs subtraction, an integrator 13 which receives and integrates the output of the subtracter 12, a comparator 14 which receives the output of the integrator 13 and decides the polarity, and a 2nd 1-bit D/A converter 15 which receives a DC voltage as the numerator of the correction arithmetic; and the output of the comparator 14 is used as a switching signal for the 1st and 2nd 1-bit D/A converters 11 and 15. The output of the 2nd 1-bit D/A converter 15 is used as a correction arithmetic output. Therefore, there is no place to be adjusted, so good precision and superior stability are obtained and neither special components nor severe selecting operation is required.

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審査請求　未請求　請求項の数２　ＯＬ　（全　４　頁）

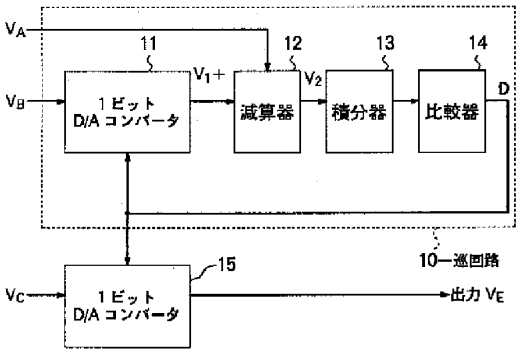
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(54)【発明の名称】　アナログ演算回路

(57)【要約】
【目的】　精度の高い部品を必要としない安価で高性能なアナログ演算回路を提供すること。
【構成】　補正演算の分母となる直流電圧を受ける第１の１ビットＤ／Ａコンバータ１１と、該１ビットＤ／Ａコンバータの出力と基準電圧とを受けて減算を行う減算器１２と、該減算器の出力を受けて積分を行う積分器１３と、該積分器の出力を受けて極性判別を行う比較器１４と、補正演算の分子となる直流電圧を受ける第２の１ビットＤ／Ａコンバータ１５とから成り、前記比較器の出力を前記第１及び第２の１ビットＤ／Ａコンバータの切り換え信号として用いる。前記第２の１ビットＤ／Ａコンバータの出力を補正演算出力として得る。
【効果】　調整を要する箇所が無いため、精度が良く安定性に優れているのみならず、特種な部品または厳格な選定作業を必要としない。



【特許請求の範囲】
【請求項１】　補正演算の分母となる直流電圧を受ける第１の１ビットＤ／Ａコンバータと、該１ビットＤ／Ａコンバータの出力と基準電圧とを受けて減算を行う演算器と、該演算器の出力を受けて積分を行う積分器と、該積分器の出力を受けて極性判別を行う比較器と、補正演算の分子となる直流電圧を受ける第２の１ビットＤ／Ａコンバータとからなり、前記比較器の出力を前記第１及び第２の１ビットＤ／Ａコンバータの切り換え信号として用い、前記第２の１ビットＤ／Ａコンバータの出力を補正演算出力として得ることを特徴とするアナログ演算回路。
【請求項２】　請求項１記載のアナログ演算回路において、前記１ビットＤ／Ａコンバータとしてアナログスイッチを用いることを特徴とするアナログ演算回路。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は差動トランスの検出信号を補正するためのアナログ演算回路に関する。
【０００２】
【従来の技術】差動トランスの信号検出回路は、差動トランスにおけるコアの位置変位を電気信号に変換して取り出す回路であり、その一例を図５を参照して説明する。図５において、差動トランス４０の一次側に発振回路４１を接続し、２次側の両端にはそれぞれ、加算回路４２，減算回路４３を接続している。加算回路４２は、差動トランス４０のコア４１の位置変位に応じて変化する２次側の電圧V_aと電圧V_bとを加算し、減算回路４３は電圧V_aと電圧V_bとの減算を行う。加算回路４２，減算回路４３にはそれぞれ、同期整流回路４４，４５が接続され、これらの和分信号電圧（$V_a + V_b$），差分信号電圧（$V_a - V_b$）がそれぞれ出力される。
【０００３】ところで、この信号検出回路では、差動トランス４０と発振回路４１及び差動トランス４０と加算回路４２、減算回路４３とを接続しているケーブルの長さや、差動トランス内部の抵抗値が温度等により変化した場合に誤差が生ずる。一般に、この誤差要因を補正するため、除算回路により差分の信号電圧（$V_a - V_b$）を和分の信号電圧（$V_a + V_b$）にて除算する方式が用いられている。
【０００４】従来用いられている除算回路の一例を図６に示す。この除算回路４６は、乗算回路５１，減算回路５２，増幅回路５３から成り、半導体の指数関数特性を利用したアナログ演算器を用いるものである。
【０００５】
【発明が解決しようとする課題】しかしながら、上記従来例では半導体のダイオード順方向電流電圧特性が指数関数に近似できる事を利用したアナログ演算器を用いており、素子のばらつきによる特性誤差が大きい。このため、精度の高いものを得ようとすると、厳密な選定を行った高価な部品を使用する必要がある。また、調整要素も多く複雑で、多大な調整時間がかかるという欠点があった。
【０００６】そこで本発明の目的は、前記のような従来のアナログ演算器の持つ問題を解決し、精度の高い部品を必要としない安価で高性能なアナログ演算回路を提供することにある。
【０００７】
【課題を解決するための手段】本発明によれば、補正演算の分母となる直流電圧を受ける第１の１ビットＤ／Ａコンバータと、該１ビットＤ／Ａコンバータの出力と基準電圧を受けて減算を行う演算器と、該演算器の出力を受けて積分を行う積分器と、該積分器の出力を受けて極性判別を行う比較器と、補正演算の分子となる直流電圧を受ける第２の１ビットＤ／Ａコンバータとからなり、前記比較器の出力を前記第１及び第２の１ビットＤ／Ａコンバータの切り換え信号として用い、前記第２の１ビットＤ／Ａコンバータの出力を補正演算出力として得ることを特徴とするアナログ演算回路が得られる。
【０００８】
【作用】本発明回路によるアナログ演算は、内部にデジタル信号を用いながら一巡回路内の積分器の効果により、高精度の乗除算アナログ電圧を得る事ができる。また、アナログの非直線性素子を用いていないため、特性変化要因が少なく時間，温度等に対する安定性に優れた演算が可能である。
【０００９】
【実施例】次に、本発明の実施例を図面を参照して詳細に説明する。図１を参照して、本発明によるアナログ演算回路は、補正演算の分母となる入力信号電圧V_Bを受ける第１の１ビットＤ／Ａコンバータ１１と、この１ビットＤ／Ａコンバータ１１の出力V_1と基準電圧としての入力信号電圧V_Aとを受けて減算を行う減算器１２と、この減算器１２の出力V_2を受けて積分を行う積分器１３と、この積分器１３の出力を受けて極性判別を行う比較器１４とから成る一巡回路１０と、補正演算の分子となる入力信号電圧V_Cを受ける第２の１ビットＤ／Ａコンバータ１５とを有している。なお、入力信号電圧V_A，V_B，V_Cはいずれも直流電圧である。
【００１０】一般に、Ｄ／Ａコンバータの出力は、基準電圧としてのアナログ電圧入力とデジタル入力の積になる事は周知の通りである。図１の回路に、入力信号電圧V_A，V_B，V_Cを加えた場合の各部波形は、図２に示す様になる。すなわち、入力信号電圧V_Bが加わった１ビットＤ／Ａコンバータ１１の出力V_1は、図２（ａ）の比較器１４のデジタル出力Ｄによって入力信号電圧V_Bを正、負に振ることにより、図２（ｂ）の様に時間T_2において符号が反転する。これに負の入力信号電圧V_Aを加えた減算器１２の出力V_2の波形は、図２（ｃ）の様になる。

【００１１】積分器１３により出力V_2の平均電圧は０（Ｖ）となるため、下式を得る。

【００１２】

$(V_B - V_A) \times T_1 - (V_B + V_A) \times T_2 = 0$

変形すると、

$V_B \times (T_1 - T_2) = V_A \times (T_1 + T_2)$

よって、下式を得る。

【００１３】

$V_A = V_B \cdot (T_1 - T_2) / (T_1 + T_2)$

一方、デジタル出力ＤをT_1，T_2を用いて下式のように表現する。

【００１４】$D = (T_1 - T_2) / (T_1 + T_2)$

上記式と式より下式を得る。

【００１５】$V_A = D \times V_B$

変形すると下式となる。

【００１６】$D = V_A / V_B$

入力信号電圧V_Cを１ビットＤ／Ａコンバータ１５に通した出力電圧V_Eは、入力信号電圧V_Cをデジタル出力Ｄによって正、負に振ることにより、$V_E = D \times V_C$で表され、式より次式を得る。このように、比較器１４のデジタル出力Ｄは、１ビットＤ／Ａコンバータ１１、１５の切り換え信号として作用する。

【００１７】$V_E = V_C \cdot V_A / V_B$

つまり、出力電圧V_EはV_AとV_C間を乗算し、これをV_Bで除算した値が得られる。

【００１８】図３に本発明による演算回路を差動トランス信号検出回路に適用した場合の回路を示す。差動トランス信号検出回路１０から出力される和信号である入力信号電圧V_B（$= V_a + V_b$）の極性は常に正であるため、図１の１ビットＤ／Ａコンバータ１１，１５はそれぞれ、アナログスイッチ３１，３５により置き換えが可能である。基準電圧発生器３７からの基準電圧V_Aは負電圧である。また、入力信号電圧V_Cは直流電圧であるが、アナログスイッチ３５により脈流になっているので、このリップル分を除去するために低域通過フィルター３６が用いられている。

【００１９】低域通過フィルター３６の出力V_oは、前出の説明によって、下式となる。

【００２０】

$V_o = K \cdot (V_a - V_b) / (V_a + V_b)$

ここで、Ｋは任意の定数であり、前出の入力信号電圧V_Aに対応する。

【００２１】図１の減算器１２は入力信号電圧V_A，V_B間の極性が反対ならば、加算器３２に置き換えられる。また、１ビットＤ／Ａコンバータ１１、１５は、演算する信号の極性，応答性により各種の方式が使用できることは言うまでもない。すなわち、上記実施例では、入力信号電圧V_B（$= V_a + V_b$）の極性が常に正であるので、１ビットＤ／Ａコンバータ１１、１５をアナログスイッチ３１，３５により置き換えることができたが、極性が負をとるのであれば、図４（ａ）、（ｂ）のような構成にする必要がある。

【００２２】図４（ａ）では、入力信号電圧V_Bとこれを反転増幅器ＩＡ１により反転した電圧とを、比較器３４の出力Ｄによりスイッチ回路Ｓ１で切り換えるようにしている。図４（ｂ）では、入力信号電圧V_BをオペアンプＯＰ１の反転入力端子に入力する。一方、オペアンプＯＰ１の非反転入力端子への入力信号電圧V_Bの入力を、比較器３４の出力Ｄによってオン、オフするスイッチＳ２により切り換えるようにしている。

【００２３】

【発明の効果】以上の説明により明らかなように、本発明によるアナログ演算回路は調整を要する箇所が無いため、精度が良く安定性に優れているのみならず、特種な部品または厳格な選定作業を必要とせず、得られる経済効果は大である。

【図面の簡単な説明】

【図１】本発明による演算回路の実施例の構成を示す図である。

【図２】図１の各部の電圧波形を示す図である。

【図３】本発明による演算回路を差動トランス信号検出回路の補正に適用した例を説明するための図である。

【図４】図１に示された１ビットＤ／Ａコンバータの具体例を示した図である。

【図５】差動トランス信号検出回路の一例を示す図である。

【図６】従来のアナログ演算回路の構成を示す図である。

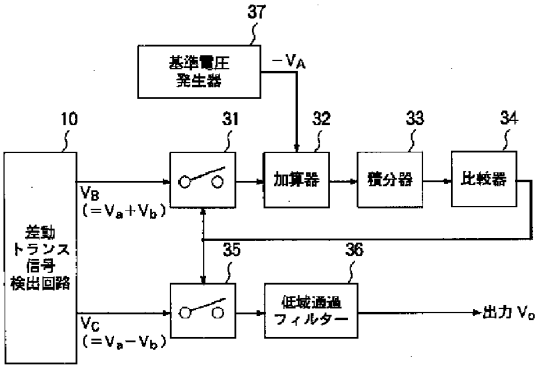
【符号の説明】

３１、３５　　アナログスイッチ

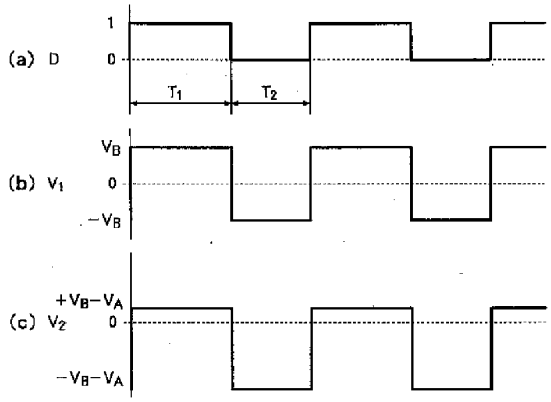
ＩＡ１　　反転増幅器

ＯＰ１　　オペアンプ

【図１】

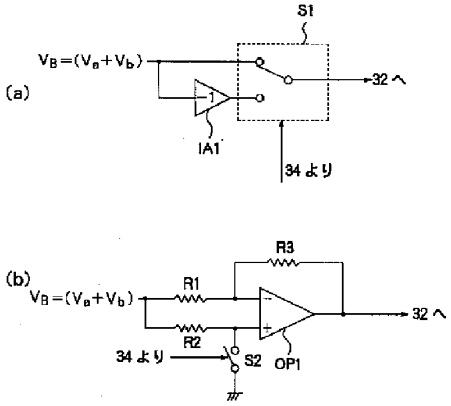


【図２】

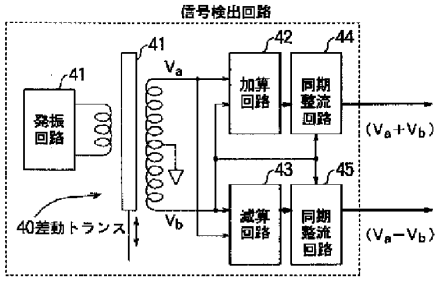


【図３】

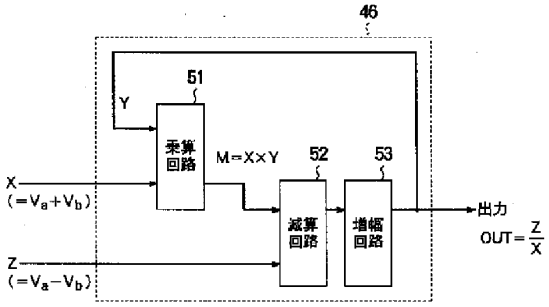
【図４】



【図５】



【図６】



Electronic Patent Application Fee Transmittal

Application Number:	16882694
Filing Date:	25-May-2020
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Filer:	Robert Plotkin/Kimberly Hauser
Attorney Docket Number:	SNG.1001C9

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1360	1360
		Total in USD ($)		**1360**

Electronic Acknowledgement Receipt	
EFS ID:	41099914
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	11-NOV-2020
Filing Date:	25-MAY-2020
Time Stamp:	20:08:39
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1360
RAM confirmation Number	E2020AAK09340752
Deposit Account	601293
Authorized User	Kimberly Hauser
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges) 37 CFR 1.20 (Post Issuance fees)	

37 CFR 1.17 (Patent application and reexamination processing fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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2	Information Disclosure Statement (IDS) Form (SB08)	SNG-1001C9_PTO_IDS-Form_2nd_Supp.pdf	1057906 236761c3bbaa0f38c292932f7f8ef1b8ae306af4	no	12
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		Total Files Size (in bytes):	394181408		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	16/882,694	Filing Date	2020-05-25	Docket Number (if applicable)	SNG.1001C9	Art Unit	2182
First Named Inventor	Joseph Bates			Examiner Name	MICHAEL D YAARY		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☒ Other PETITION TO WITHDRAW AN APPLICATION FROM ISSUE AFTER PAYMENT OF THE ISSUE FEE UNDER 37 CFR 1.313(c)

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 601293

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2020-11-11
Name	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	41099985
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	11-NOV-2020
Filing Date:	25-MAY-2020
Time Stamp:	20:12:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	NPL-017-pages-001-077.pdf	16205641 460ca21d8906151 4a2f7dcede9417d63d05 02b13	no	77
Warnings:					

Information:					
2	Non Patent Literature	NPL-017-pages-078-116.pdf	10573442 580a791a5b5f9fcf605868bc754210295e79bac3	no	39
Warnings:					
Information:					
3	Non Patent Literature	NPL-027-pages-001-169.pdf	21042539 c9285560abebec5cbda4f62ed0ca653403f8e51f	no	169
Warnings:					
Information:					
4	Non Patent Literature	NPL-027-pages-170-302.pdf	20777104 7d830cbb83ab9c09b8166f2525e3b57f52e505f2	no	133
Warnings:					
Information:					
5	Non Patent Literature	NPL-047.pdf	610152 a0a4844ab5122e834a757c2aff9591e9a22f7c10	no	86
Warnings:					
Information:					
6	Non Patent Literature	NPL-048.pdf	1292882 2e2c7328b5d192d4cc376e533ae77f7c2d1e4c8f	no	92
Warnings:					
Information:					
			Total Files Size (in bytes):	70501760	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	11/17/2020	10838694	SNG.1001C9	3296

144359 7590 10/28/2020

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Singular Computing LLC, Newton, MA;
Joseph Bates, Newton, MA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9

CONFIRMATION NO. 3296

144359
Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

PUBLICATION NOTICE

OC000000120834402

Title:PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

Publication No.US-2020-0334011-A1
Publication Date:10/22/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

144359 7590 10/01/2020

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

EXAMINER	
YAARY, MICHAEL D	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
10/01/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@blueshiftip.com
eofficeaction@appcoll.com
mail@blueshiftip.com

Corrected ***Notice of Allowability***	**Application No.** 16/882,694	**Applicant(s)** Bates, Joseph	
	Examiner MICHAEL D YAARY	**Art Unit** 2182	**AIA (FITF) Status** Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 09/17/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-24 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/17/2020.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MICHAEL D. YAARY/
Primary Examiner, Art Unit 2182

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /MY/

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

/MY/	1	G. H. A. Aty, A. I. Hussein, I. S. Ashour and M. Mones, "High-speed, area-efficient FPGA-based floating-point multiplier," Proceedings of the 12th IEEE International Conference on Fuzzy Systems (Cat. No.03CH37442), Cairo, Egypt, 2003, pp. 274-277, doi: 10.1109/ICM.2003.237828.
/MY/	2	Belanović P., Leeser M. (2002) A Library of Parameterized Floating-Point Modules and Their Use. In: Glesner M., Zipf P., Renovell M. (eds) Field-Programmable Logic and Applications: Reconfigurable Computing Is Going Mainstream. FPL 2002. Lecture Notes in Computer Science, vol 2438. Springer, Berlin, Heidelberg. https://doi.org/10.1007/3-540-46117-5_68
/MY/	3	N. Shirazi, A. Walters and P. Athanas, "Quantitative analysis of floating point arithmetic on FPGA based custom computing machines," Proceedings IEEE Symposium on FPGAs for Custom Computing Machines, Napa Valley, CA, USA, 1995, pp. 155-162, doi: 10.1109/FPGA.1995.477421.

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/MICHAEL D. YAARY/	Date Considered	09/28/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2020-09-17
Name/Print	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :66043

Sale Accounting Date:09/21/2020

Sale Item Reference Number	Effective Date
16882694	09/17/2020

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I202091752475066	1806	SUBMISSION- INFORMATION DISCLOSURE STMT	$240.00	Deposit Account

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

144359 7590 09/18/2020

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

EXAMINER	
YAARY, MICHAEL D	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
09/18/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@blueshiftip.com
eofficeaction@appcoll.com
mail@blueshiftip.com

Response to Rule 312 Communication	Application No.	Applicant(s)	
	16/882,694	Bates, Joseph	
	Examiner	Art Unit	AIA (FITF) Status
	MICHAEL D YAARY	2182	Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 03 September 2020 under 37 CFR 1.312 has been considered, and has been:
   a) ☑ entered.
   b) ☐ entered as directed to matters of form not affecting the scope of the invention.
   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
      Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.
   d) ☐ disapproved. See explanation below.
   e) ☐ entered in part. See explanation below.

/MICHAEL D. YAARY/
Primary Examiner, Art Unit 2182

OK TO ENTER: /MY/

ATTORNEY'S DOCKET NO: SNG.1001C9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	16/882,694
Confirmation No.:	3296
Title:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Inventor:	Joseph Bates
Filing Date:	May 25, 2020
Examiner:	MICHAEL D YAARY
Art Unit:	2182

AMENDMENT UNDER 37 C.F.R. § 1.312

Applicant hereby submits the following post-allowance amendments pursuant to 37 C.F.R. § 1.312:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks begin on page 15 of this paper.

Conclusions begin on page 17 of this paper.

Doc Code: QPIDS.REQ
Document Description: QuickPath Information Disclosure Statement

PTO/SB/09 (09-18)

CERTIFICATION AND REQUEST FOR CONSIDERATION OF AN INFORMATION DISCLOSURE STATEMENT FILED AFTER PAYMENT OF THE ISSUE FEE UNDER THE QPIDS PROGRAM

Non-Provisional Application Number: 16/882,694	Filing Date: 25 May 2020
First Named Inventor: Joseph Bates	Title of Invention: PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

THE UNDERSIGNED HEREBY CERTIFIES AND REQUESTS THE FOLLOWING FOR THE ABOVE-IDENTIFIED APPLICATION.

1. Consideration is requested of the information disclosure statement (IDS) submitted herewith, which is being filed after payment of the issue fee.
2. Check the box next to the appropriate selection:

   ☐ Each item of information contained in the IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the IDS. See 37 CFR 1.97(e)(1).

   OR

   ☑ No item of information contained in the IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the IDS was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the IDS. See 37 CFR 1.97(e)(2).

   OR

   ☐ See attached certification statement in compliance with 37 CFR 1.97(e).
3. Please charge the IDS fee set forth in 37 CFR 1.17(p) to Deposit Account No. 60/1293.
4. A Petition to Withdraw from Issue After Payment of the Issue Fee (37 CFR 1.313(c)(2)), including the petition fee set forth in 37 CFR 1.17(h), is submitted herewith as a **Web-based ePetition**. **WARNING:** Do not submit the petition as a follow-on paper via EFS-Web. Submit the petition as a Web-based ePetition by signing on to EFS-Web as a registered user, selecting the radio button next to "Existing application/patent," and then selecting the radio button next to "ePetition (for automatic processing and immediate grant, if all petitions requirements are met)." Failure to use the Web-based ePetition interface will result in automatic entry of the RCE.
5. A request for continued examination (RCE) under 37 CFR 1.114 and the RCE fee under 37 CFR 1.17(e) are submitted herewith.
6. The RCE will be treated as a "conditional" RCE. In the event the examiner determines that any item of information contained in the IDS necessitates the reopening of prosecution in the application, the undersigned understands that (i) the RCE will be processed and treated as an RCE under 37 CFR 1.114 and therefore (ii) the IDS fee under 37 CFR 1.17(p) will be returned in accordance with 37 CFR 1.97(b)(4). In the event that no item of information in the IDS necessitates reopening prosecution, the undersigned understands that the RCE will not be processed and the RCE fee under 37 CFR 1.17(e) will be returned.
7. This certification and request is being filed as a **Web-based ePetition** and is not accompanied by an amendment to the application. Inclusion of an amendment will result in automatic entry of the RCE.

Signature /Robert Plotkin/	Date 2020-09-17
Name (Print/Typed) Robert Plotkin	Practitioner Registration Number (If applicable) 43861

Note: *Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below.**

☑ *Total of 1 forms are submitted.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

	1	G. H. A. Aty, A. I. Hussein, I. S. Ashour and M. Mones, "High-speed, area-efficient FPGA-based floating-point multiplier," Proceedings of the 12th IEEE International Conference on Fuzzy Systems (Cat. No.03CH37442), Cairo, Egypt, 2003, pp. 274-277, doi: 10.1109/ICM.2003.237828.
	2	Belanović P., Leeser M. (2002) A Library of Parameterized Floating-Point Modules and Their Use. In: Glesner M., Zipf P., Renovell M. (eds) Field-Programmable Logic and Applications: Reconfigurable Computing Is Going Mainstream. FPL 2002. Lecture Notes in Computer Science, vol 2438. Springer, Berlin, Heidelberg. https://doi.org/10.1007/3-540-46117-5_68
	3	N. Shirazi, A. Walters and P. Athanas, "Quantitative analysis of floating point arithmetic on FPGA based custom computing machines," Proceedings IEEE Symposium on FPGAs for Custom Computing Machines, Napa Valley, CA, USA, 1995, pp. 155-162, doi: 10.1109/FPGA.1995.477421.

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	2182
	Examiner Name	MICHAEL D YAARY
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2020-09-17
Name/Print	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc Code: PET.AUTO Document Description: Petition automatically granted by EFS-Web	PTO/SB/140 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**PETITION TO WITHDRAW AN APPLICATION FROM ISSUE AFTER PAYMENT OF THE ISSUE FEE UNDER 37 CFR 1.313(c)**
Application Number	16882694
Filing Date	25-May-2020
First Named Inventor	Joseph Bates
Art Unit	2182
Examiner Name	MICHAEL YAARY
Attorney Docket Number	SNG.1001C9
Title	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

An application may be withdrawn from issue for further action upon petition by the applicant. To request that the Office withdraw an application from issue, applicant must file a petition under this section including the fee set forth in § 1.17(h) and a showing of good and sufficient reasons why withdrawal of the application from issue is necessary.

APPLICANT HEREBY PETITIONS TO WITHDRAW THIS APPLICATION FROM ISSUE UNDER 37 CFR 1.313(c).

A grantable petition requires the following items:
(1) Petition fee; and
(2) One of the following reasons:
(a) Unpatentability of one or more claims, which must be accompanied by an unequivocal statement that one or more claims are unpatentable, an amendment to such claim or claims, and an explanation as to how the amendment causes such claim or claims to be patentable;
(b) Consideration of a request for continued examination in compliance with § 1.114 (for a utility or plant application only); or
(c) Express abandonment of the application. Such express abandonment may be in favor of a continuing application, but not a CPA under 37 CFR 1.53(d).

Petition Fee

- ◯ Small Entity
- ◯ Micro Entity
- ◉ Regular Undiscounted

Reason for withdrawal from issue

○ One or more claims are unpatentable ◉ Consideration of a request for continued examination (RCE) (List of Required Documents and Fees) ○ Applicant hereby expressly abandons the instant application (any attorney/agent signing for this reason must have power of attorney pursuant to 37 CFR 1.32(b)).
RCE request,submission, and fee. ☐ I certify, in accordance with 37 CFR 1.4(d)(4) that : The RCE request ,submission, and fee have already been filed in the above-identified application on ☒ Are attached.
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ○ An attorney or agent registered to practice before the Patent and Trademark Office who has been given power of attorney in this application. ◉ An attorney or agent registered to practice before the Patent and Trademark Office, acting in a representative capacity. ○ A sole inventor ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ○ A joint inventor; all of whom are signing this e-petition

Signature	/Robert Plotkin/
Name	Robert Plotkin
Registration Number	43861

Electronic Patent Application Fee Transmittal

Application Number:	16882694
Filing Date:	25-May-2020
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Filer:	Robert Plotkin/Kimberly Hauser
Attorney Docket Number:	SNG.1001C9

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
PETITION FEE- 37 CFR 1.17(H) (GROUP III)	1464	1	140	140
RCE- 1ST REQUEST	1801	1	1300	1300
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1440**

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Decision Date : September 17, 2020

In re Application of :

Joseph Bates

DECISION ON PETITION
UNDER CFR 1.313(c)(2)

Application No : 16882694

Filed : 25-May-2020

Attorney Docket No : SNG.1001C9

This is an electronic decision on the petition under 37 CFR 1.313(c)(2), filed September 17, 2020, to withdraw the above-identified application from issue after payment of the issue fee.

The petition is **GRANTED.**

The above-identified application is withdrawn from issue for consideration of a submission under 37 CFR 1.114 (request for continued examination). See 37 CFR 1.313(c)(2).

Petitioner is advised that the issue fee paid in this application cannot be refunded. If, however, this application is again allowed, petitioner may request that it be applied towards the issue fee required by the new Notice of Allowance.

Telephone inquiries concerning this decision should be directed to the Patent Electronic Business Center (EBC) at 866-217-9197.

This application file is being referred to Technology Center AU 2182 for processing of the request for continuing examination under 37 CFR 1.114 .

Office of Petitions

Electronic Acknowledgement Receipt	
EFS ID:	40589731
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	17-SEP-2020
Filing Date:	25-MAY-2020
Time Stamp:	16:44:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1440
RAM confirmation Number	E20209GG44462275
Deposit Account	601293
Authorized User	Kimberly Hauser
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges) 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Quick Path Information Disclosure Statement	SNG-1001C9_QPIDS_Certification.pdf	186564 7fa9e8cd175050b6e7939d6b3814c3109799c6fc	no	2
Warnings:					
Information:					
2	Request for Continued Examination (RCE)	SNG-1001C9_RCE.pdf	1350059 8482f7c207f3610ebd9c3dd14aa1f20e99198d47	no	3
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	SNG-1001C9_PTO_IDS-Form_1st_Supp.pdf	1053708 704af8b7d8b9e3417f85f4faa11231a09dc0947e	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
4	Non Patent Literature	NPL_Aty.pdf	793863 ab1168e201670dccb78bdfc671586aba98e75c58	no	4
Warnings:					
Information:					
5	Non Patent Literature	NPL_Belanovic.pdf	191996 281f4f72237e1fd76c38593e5d5e0cfc692027c5	no	10
Warnings:					
Information:					

6	Non Patent Literature	NPL_Shirazi.pdf	256051 0eb769be9ea3abf84b1133fc88d2ab11f8dcb703	no	8
Warnings:					
Information:					
7	Petition automatically granted by EFS	petition-request.pdf	31507 04365633f5d00ad2d1e13c0563bd55d4909d6506	no	2
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	32397 1282c47b501d0112f2299b95beb3be5476e112e8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3896145		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
16882694	25-May-2020	Joseph Bates	SNG.1001C9	3296

TITLE OF INVENTION :

PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Regular Undiscounted	Utility under 35 USC 111(a)	2182	524000	MICHAEL YAARY

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$1000	$0	$1000	24-Nov-2020	$0

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
144359 Blueshift IP LLC 1 Broadway, 14th Floor Cambridge MA 02142 UNITED STATES 617-207-6141 docketing@blueshiftip.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☐ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

○ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

◉ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☒ Issue Fee	☐ I authorize USPTO to apply my previously paid issue fee to the current fees due
☐ Publication Fee	☐ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number _____
☐ Advance Order - # of copies _____	☒ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency, or credit any overpayment, to Deposit Account Number 601293 . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. BLUESHIFT IP, LLC
2. ROBERT PLOTKIN
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
Singular Computing LLC	Newton	MASSACHUSETTS	united states	corporation

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Robert Plotkin/	**Date**	09-16-2020
Name	Robert Plotkin	**Registration Number**	43861

WEB IFEE 1.0

Electronic Patent Application Fee Transmittal

Application Number:	16882694
Filing Date:	25-May-2020
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Filer:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt	
EFS ID:	40576399
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin
Filer Authorized By:	
Attorney Docket Number:	SNG.1001C9
Receipt Date:	16-SEP-2020
Filing Date:	25-MAY-2020
Time Stamp:	15:18:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	E20209FF18070643
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Web85b.pdf	46148 384973af7865a03f2e73651a5d5a5deae47e e78b	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31883 497b2a9c01814023941f38ee30a3dc465a9 919fc	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	78031		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

ATTORNEY'S DOCKET NO: SNG.1001C9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	16/882,694
Confirmation No.:	3296
Title:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Inventor:	Joseph Bates
Filing Date:	May 25, 2020
Examiner:	MICHAEL D YAARY
Art Unit:	2182

AMENDMENT UNDER 37 C.F.R. § 1.312

Applicant hereby submits the following post-allowance amendments pursuant to 37 C.F.R. § 1.312:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks begin on page 15 of this paper.

Conclusions begin on page 17 of this paper.

Electronic Acknowledgement Receipt

EFS ID:	40468830
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	03-SEP-2020
Filing Date:	25-MAY-2020
Time Stamp:	16:28:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SNG-1001C9_312_Amendment.pdf	86408 f62758fdf1e002715c092f3cbc54c46eed097dc5	yes	21

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	15	21
	Claims	3	14
	Specification	2	2
	Amendment after Notice of Allowance (Rule 312)	1	1
Warnings:			
Information:			
	Total Files Size (in bytes):	86408	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph [00127] at page 50, with the following replacement paragraph.

[00127] PEs implemented according to certain embodiments of the present invention may be relatively small for PEs that can do arithmetic. This means that there are many PEs per unit of resource (e.g., transistor, area, volume), which in turn means that there is a large amount of arithmetic computational power per unit of resource. This enables larger problems to be solved with a given amount of resource than does traditional computer designs. For instance, a digital embodiment of the present invention built as a large silicon chip fabricated with current state of the art technology might perform tens of thousands of arithmetic operations per cycle, as opposed to hundreds in a conventional GPU or a handful in a conventional multicore CPU. These ratios reflect an architectural advantage of embodiments of the present invention that should persist as fabrication technology continues to improve, even as we reach nanotechnology or other implementations for digital and analog computing.

REMARKS

The present amendments are submitted after the Notice of Allowance in accordance with 37 CFR § 1.312.

Amendments to the Specification

The specification is amended at page 50 to correct for minor typographical errors identified during review of the application. By entry of this amendment, the specification is made consistent with the other papers that are of record in the file wrapper of the present application. Entry of the amendments to the specification is respectfully requested.

Amendments to the Claims

Claim 7 have been amended to provide clarity, consistent use of terminology, and to correct for minor informalities identified during review of the application. Entry of the amendment of claim 7 is respectfully requested.

Remarks in Response to Reasons for Allowance

Examiner's statements of Reasons for Allowance of the above-referenced patent application are acknowledged and it is agreed that the claimed subject matter is patentable. However, no position is taken regarding the Reasons for Allowance presented by the Examiner other than the positions that may have previously been taken during

prosecution. Therefore, the Examiner's Reasons for Allowance should not be attributed as being an indication of the basis for the belief that the claims are patentable. Furthermore, it is respectfully asserted that there may also be additional reasons for patentability of the claimed subject matter not explicitly stated in this record and no waiver of rights are made to such arguments by not further addressing such reasons herein.

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CONCLUSIONS

The amendments made herein introduce no new matter.

If the Examiner wishes to discuss this Amendment, the Examiner is requested to call the Applicant's attorney at the phone number listed below.

No admission is made herein, explicitly or implicitly, that any amendments made herein are made for reasons of patentability.

If this response is not considered timely filed and if a request for extension of time is otherwise absent, Applicant hereby requests any extension of time. Please charge any fees or make any credits, to Deposit Account No. 60/1293.

Respectfully submitted,

/Robert Plotkin/ September 3, 2020

Robert Plotkin, Esq. Date

Reg. No. 43,861

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AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Previously presented) A computing system, comprising:

a host computer;

a computing chip comprising:

a processing element array comprising a first edge processing element positioned at a first edge of the processing element array, a second edge processing element positioned at the first edge of the processing element array, a first interior processing element positioned at a first location in the interior of the processing element array, and a second interior processing element positioned at a second location in the interior of the processing element array;

a first processing element connection connecting the first edge processing element with the first interior processing element;

a second processing element connection connecting the second edge processing element with the second interior processing element;

an input-output unit connected to the first edge processing element and the second edge processing element;

a first memory local to the first edge processing element;

a second memory local to the second edge processing element;

a third memory local to the first interior processing element;

a fourth memory local to the second interior processing element; and,

a fifth arithmetic unit;

wherein the first edge processing element comprises a first arithmetic unit;

wherein the second edge processing element comprises a second arithmetic unit;

wherein the first interior processing element comprises a third arithmetic unit; and

wherein the second interior processing element comprises a fourth arithmetic unit; and,

a host connection at least partially connecting the input-output unit with the host computer;

wherein the first, second, third and fourth arithmetic units each comprises a corresponding multiplier circuit adapted to receive as a first input to the corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the corresponding multiplier

circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits;

wherein the fifth arithmetic unit comprises a corresponding multiplier circuit adapted to receive as inputs to the corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein the multiplier circuit corresponding to the first arithmetic unit comprises a first plurality of transistors and has no other transistors, the multiplier circuit corresponding to the second arithmetic unit comprises a second plurality of transistors and has no other transistors, the multiplier circuit corresponding to the third arithmetic unit comprises a third plurality of transistors and has no other transistors, the multiplier circuit corresponding to the fourth arithmetic unit comprises a fourth plurality of transistors and has no other transistors, and the multiplier circuit corresponding to the fifth arithmetic unit comprises a fifth plurality of transistors; and,

wherein the fifth plurality of transistors exceeds in number each of the first plurality of transistors, the second plurality of transistors, the third plurality of transistors, and the fourth plurality of transistors.

2. (Previously presented) The computing system of claim 1, wherein said host computer is programmed to provide instructions to said computing chip that, when executed, cause said processing element array to perform an operation whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.

3. (Previously presented) The computing system of claim 1, wherein the computing chip further comprises a control unit connected to the processing element array, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the processing element array to cause the processing element array to operate according to the at least one instruction.

4. (Previously presented) The computing system of claim 3, wherein the computing chip further comprises an instruction memory adapted to store the at least one instruction received from the host computer via the input-output unit, wherein the control unit is further adapted to retrieve the at least one instruction from the instruction memory.

5. (Previously presented) The computing system of claim 1, wherein the width of each first binary mantissa is no more than 10 bits plus a first sign bit, and wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit.

6. (Previously presented) The computing system of claim 5, wherein the width of each first binary exponent is at least 5 bits plus a third sign bit and wherein the width of each second binary exponent is at least 5 bits plus a fourth sign bit.

7. (Currently Amended) A computing system, comprising:

a host computer;

a computing chip comprising:

a processing element array comprising a plurality of first processing elements, wherein the ~~the~~ plurality of first processing elements is no less than 5000 in number, wherein each of a first subset of the plurality of first processing elements is positioned at a first edge of the processing element array, and wherein each of a second subset of the plurality of first processing elements is positioned in the interior of the processing element array;

an input-output unit connected to each of the first subset of the plurality of first processing elements;

a plurality of processing element connections, each processing element connection connecting one of the plurality of first processing elements with another of the plurality of first processing elements, wherein each of the plurality of first processing elements is connected to at least one other of the plurality of first processing elements by at least one of the plurality of processing element connections;

a plurality of memory units, wherein each of the plurality of first processing elements is associated with a corresponding one of the plurality of memory units, and wherein each of the plurality of memory units is local to its associated one of the plurality of first processing elements;

a plurality of first arithmetic units, wherein each of the plurality of first processing elements has positioned therein at least one of the plurality of first arithmetic units;

a plurality of second processing elements; and

a plurality of second arithmetic units, wherein each of the plurality of second processing elements has positioned therein at least one of the plurality of second arithmetic units; and

a host connection at least partially connecting the input-output unit with the host computer;

wherein the plurality of first arithmetic units each comprises a first corresponding multiplier circuit adapted to receive as a first input to the first corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the first corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits;

wherein the first multiplier circuits corresponding to the plurality of first arithmetic units each comprises a first respective plurality of transistors and has no other transistors;

wherein the plurality of second arithmetic units each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein the second multiplier circuits corresponding to the plurality of second arithmetic units each comprises a second respective plurality of transistors;

wherein each of the second respective pluralities of transistors of the second multiplier circuits corresponding to the plurality of second arithmetic units exceeds in number each of the

first respective pluralities of transistors of the first multiplier circuits corresponding to the plurality of first arithmetic units.

8. (Previously presented) The computing system of claim 7,

wherein, other than the plurality of second processing elements, the computing chip has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and

wherein the plurality of first processing elements exceeds in number, by at least 100, the plurality of second processing elements.

9. (Previously presented) The computing system of claim 7, wherein the plurality of memory units each comprises a corresponding register.

10. (Previously presented) The computing system of claim 8, wherein said host computer is programmed to provide instructions to said computing chip that, when executed, cause said processing element array to perform an operation whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.

11. (Previously presented) The computing system of claim 8, wherein an aggregate maximum bandwidth of the plurality of processing element connections exceeds a maximum bandwidth of the host connection.

12. (Previously presented) The computing system of claim 11, wherein the computing chip further comprises a control unit connected to the processing element array, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the processing element array to cause the processing element array to operate according to the at least one instruction.

13. (Previously presented) The computing system of claim 12, wherein the computing chip further comprises an instruction memory adapted to store the at least one instruction received from the host computer via the input-output unit, wherein the control unit is further adapted to retrieve the at least one instruction from the instruction memory.

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14. (Previously presented) The computing system of claim 7, wherein the width of each first binary mantissa is no more than 10 bits plus a first sign bit, and wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit.

15. (Previously presented) The computing system of claim 14, wherein the width of each first binary exponent is at least 5 bits plus a third sign bit and wherein the width of each second binary exponent is at least 5 bits plus a fourth sign bit.

16. (Previously presented) A circuit board connected to a host computer, the circuit board comprising:

a plurality of processing element arrays, each comprising:

a plurality of first processing elements, wherein the plurality of first processing elements of said processing element array is no less than 5000 in number, wherein each of a first subset of the plurality of first processing elements of said processing element array is positioned at a first edge of said processing element array, and wherein each of a second subset of the plurality of first processing elements of said processing element array is positioned in the interior of said processing element array;

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a plurality of processing element connections, each processing element connection connecting one of the plurality of first processing elements of said processing element array with another of the plurality of first processing elements of said processing element array, wherein each of the plurality of first processing elements of said processing element array is connected to at least one other of the plurality of first processing elements of said processing element array by at least one of the plurality of processing element connections of said processing element array;

a plurality of memory units, wherein each of the plurality of first processing elements of said processing element array is associated with a corresponding one of the plurality of memory units of said processing element array, and wherein each of the plurality of memory units of said processing element array is local to its associated one of the plurality of first processing elements of said processing element array; and,

a plurality of arithmetic units, wherein each of the plurality of first processing elements of said processing element array has positioned therein at least one of the plurality of arithmetic units of said processing element array;

wherein the plurality of arithmetic units of said processing element array each comprises a first corresponding

multiplier circuit adapted to receive as a first input to the first corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the first corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits; and,

an input-output unit connected to at least one of the plurality of processing element arrays; and,

a host connection at least partially connecting the input-output unit with the host computer.

17. (Previously presented) The circuit board of claim 16,

wherein the circuit board further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein other than the second processing elements, the circuit board has no other processing element that comprises a multiplier

circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and,

wherein a total count of the pluralities of first processing elements of the plurality of processing element arrays exceeds in number, by at least 20 more than three times, the plurality of second processing elements.

18. (Previously presented) The circuit board of claim 16,

wherein the circuit board further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein other than the second processing elements the circuit board has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and,

wherein a total count of the pluralities of first processing elements of the plurality of processing element arrays exceeds in number, by at least 1000 more than five times, the plurality of second processing elements.

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19. (Previously presented) The circuit board of claim 16,

wherein the circuit board further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein other than the second processing elements the circuit board has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and,

wherein a total count of the pluralities of first processing elements of the plurality of processing element arrays exceeds in number, by at least 100 more, the plurality of second processing elements.

20. (Previously presented) The circuit board of claim 18, wherein said circuit board is adapted to receive instructions from the host computer that, when executed, cause at least one of said processing element arrays to perform an operation whose output is

used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.

21. (Previously presented) The circuit board of claim 18, wherein the circuit board further comprises a control unit connected to at least one of the plurality of processing element arrays, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the at least one of the plurality of processing element arrays to cause the at least one of the plurality of processing element arrays to operate according to the at least one instruction.

22. (Previously presented) The circuit board of claim 21,

wherein the circuit board further comprises an instruction memory connected to the control unit, the instruction memory comprising circuitry adapted to store the at least one instruction received from the host computer via the input-output unit, and

wherein the control unit further comprises circuitry adapted to retrieve the at least one instruction from the instruction memory.

23. (Previously presented) The circuit board of claim 16, wherein the width of each first binary mantissa is no more than 10

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bits plus a first sign bit, and wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit.

24. (Previously presented) The circuit board of claim 23, wherein the width of each first binary exponent is at least 5 bits plus a third sign bit and wherein the width of each second binary exponent is at least 5 bits plus a fourth sign bit.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

144359 7590 08/24/2020

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

EXAMINER	
YAARY, MICHAEL D	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 08/24/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

TITLE OF INVENTION: PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	11/24/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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144359 7590 08/24/2020
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(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

TITLE OF INVENTION: PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	11/24/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
YAARY, MICHAEL D	2182	708-524000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
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PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

144359 7590 08/24/2020

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

EXAMINER	
YAARY, MICHAEL D	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 08/24/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/882,694	Applicant(s) Bates, Joseph	
	Examiner MICHAEL D YAARY	Art Unit 2182	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 05/25/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-24 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MICHAEL D. YAARY/
Primary Examiner, Art Unit 2182

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or suggest at least "a processing element array comprising a first edge processing element positioned at a first edge of the processing element array, a second edge processing element positioned at the first edge of the processing element array, a first interior processing element positioned at a first location in the interior of the processing element array, and a second interior processing element positioned at a second location in the interior of the processing element array; a first processing element connection connecting the first edge processing element with the first interior processing element; a second processing element connection connecting the second edge processing element with the second interior processing element; an input-output unit connected to the first edge processing element and the second edge processing element; a first memory local to the first edge processing element; a second memory local to the second edge processing element; a third memory local to the first interior processing element; a fourth memory local to the second interior processing element; and, a fifth arithmetic unit; wherein the first edge processing element comprises a first arithmetic unit; wherein the second edge processing element comprises a second arithmetic unit; wherein the first interior processing element comprises a third arithmetic unit; and wherein the second interior processing element comprises a fourth arithmetic unit; and, a host connection at least partially connecting the input-output unit with the host computer; wherein the first,

second, third and fourth arithmetic units each comprises a corresponding multiplier circuit adapted to receive as a first input to the corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits; wherein the fifth arithmetic unit comprises a corresponding multiplier circuit adapted to receive as inputs to the corresponding multiplier circuit two floating point values each of width at least 32 bits;" as recited in claim 1 and similarly in claims 7 and 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL D YAARY whose telephone number is (571)270-1249. The examiner can normally be reached on Mon-Fri 9-5:30.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on (571)272-3702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL D. YAARY/
Primary Examiner, Art Unit 2182

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

CPC						
Symbol					**Type**	**Version**
G06F	/	7	/	483	F	2013-01-01
G06F	/	7	/	4833	I	2013-01-01
G06F	/	7	/	38	I	2013-01-01
H03K	/	19	/	17728	I	2013-01-01
G06F	/	7	/	5235	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	24	
/MICHAEL D. YAARY/ Primary Examiner, Art Unit 2182	18 August 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20200818

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G06F7/483	/	7	/	483
G06F7/38	/	7	/	38
H03K19/17728	/	19	/	17728
G06F7/523	/	7	/	523

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	24	
/MICHAEL D. YAARY/ Primary Examiner, Art Unit 2182	18 August 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20200818

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10	19	19										
2	2	11	11	20	20										
3	3	12	12	21	21										
4	4	13	13	22	22										
5	5	14	14	23	23										
6	6	15	15	24	24										
7	7	16	16												
8	8	17	17												
9	9	18	18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	24	
/MICHAEL D. YAARY/ Primary Examiner, Art Unit 2182	18 August 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20200818

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/23/2020	08/18/2020							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
5	5	✓	=							
6	6	✓	=							
7	7	✓	=							
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22	22	✓	=							
23	23	✓	=							
24	24	✓	=							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	Art Unit
	MICHAEL D YAARY	2182

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST search with keywords	07/23/2020	MY
NPL search	07/23/2020	MY
Inventor name search	07/23/2020	MY
EAST search with keywords in combination with CPC classes	08/18/2020	MY

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G06F	7/483	08/18/2020	MY

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	63	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or G06F7/$.cpc.) and array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/18 10:55
L2	1,227	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/08/18 10:55
L3	1,548	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/18 10:55
L4	135	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa and exponent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/08/18 10:55
L5	54	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa and exponent and simd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/08/18 10:55
L6	97	(Bates, Joseph).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/08/18 10:55
L7	9	(Bates, Joseph).in. and singular.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/08/18 10:56

S1	666	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/06/29 09:16
S2	249	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 09:20
S3	242	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier and memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 09:25
S4	165	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier and memory and binary	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 09:25
S5	39	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 09:29
S6	97	(Bates, Joseph).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/29 10:46
S7	9	(Bates, Joseph).in. and (Singular Computing LLC).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/29 10:47
S8	39	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 11:41

S9	62	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or G06F7/$.cpc.) and array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 11:42
S10	1	"42271192".FMID.	US-PGPUB; USPAT; FPRS; JPO	OR	OFF	2020/06/29 11:42
S11	1	"42271192".FMID.	US-PGPUB; USPAT; FPRS; JPO	OR	OFF	2020/06/29 11:42
S12	62	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or G06F7/$.cpc.) and array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 12:34
S13	395	array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 13:40
S14	29	array and edge and floating and multiplier and memory and binary and (edge near5 array) and mantissa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 14:32
S15	28	array and edge and floating and multiplier and memory and binary and (edge near5 array) and mantissa and exponent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 14:36
S16	2,125	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/07/23 09:53
S17	1,225	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/07/23 09:54

S18	140	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/07/23 09:54
S19	135	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa and exponent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/07/23 09:54
S20	182	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa and exponent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/07/23 09:54
S21	54	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa and exponent and simd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/07/23 09:56
S22	97	(Bates, Joseph).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/23 10:22
S23	9	(Bates, Joseph).in. and (Singular Computing LLC).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/23 10:22

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	1	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or G06F7/$.cpc.) and array.clm. and edge.clm. and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT	OR	ON	2020/08/18 10:56
L9	0	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or G06F7/$.cpc.) and array.clm. and edge.clm. and floating.clm. and	US-PGPUB; USPAT	OR	ON	2020/08/18 10:57

		multiplier.clm. and memory and binary and (edge near5 array)				
L10	3	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or G06F7/$.cpc.) and array.clm. and edge.clm. and floating.clm. and multiplier.clm.	US-PGPUB; USPAT	OR	ON	2020/08/18 10:57

8/18/2020 10:57:51 AM
C:\Users\myaary\Documents\EAST\Workspaces\16882686.wsp

Electronic Acknowledgement Receipt

EFS ID:	40234842
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin
Filer Authorized By:	
Attorney Docket Number:	SNG.1001C9
Receipt Date:	10-AUG-2020
Filing Date:	25-MAY-2020
Time Stamp:	11:02:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	Response.pdf	60751 c3e5486814a097f5fb015eb88cc0230d965abf22	no	3

Warnings:

Information:	
Total Files Size (in bytes):	60751

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

ATTORNEY'S DOCKET NO: SNG.1001C9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	16/882,694
Confirmation No.:	3296
Title:	Processing with Compact Arithmetic Processing Element
First Inventor:	BATES, Joseph
Filing Date:	May 25, 2020
Examiner:	Michael D. Yaary
Art Unit:	2182
Office Action Mailing Date:	07/28/2020

RESPONSE TO NON-FINAL OFFICE ACTION

In response to the Non-Final Office Action mailed on the Office Action Mailing Date indicated above, the following amendments and/or remarks are respectfully submitted:

Remarks/Arguments begin on page 2 of this paper.

Conclusions begin on page 3 of this paper.

REMARKS/ARGUMENTS

Double Patenting

The double-patenting rejection of claims 1-24 hereby is obviated by the filing of a Terminal Disclaimer over U.S. Pat. App. No. 16/882,686.

Google Ex. 1002 - Page 307

CONCLUSIONS

Any dependent claims not specifically discussed above depend, either directly or indirectly, from the independent claims discussed above and therefore are patentable for at least the same reason(s).

If the Examiner wishes to discuss this Response, the Examiner is requested to call the Applicant's attorney at the phone number listed below.

No admission is made herein, explicitly or implicitly, that any amendments made herein are made for reasons of patentability.

If this response is not considered timely filed and if a request for extension of time is otherwise absent, applicant hereby requests any extension of time. Please charge any fees or make any credits, to Deposit Account No. 60/1293.

Respectfully submitted,

/Robert Plotkin/ August 10, 2020

Robert Plotkin, Esq.
Reg. No. 43,861

Blueshift IP
1 Broadway, 14th Floor,
Cambridge, MA 02142
Tel: (617) 207-6141
Fax: (617) 207-6215

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed	PTO/SB/25 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION**
Application Number	16882694
Filing Date	25-May-2020
First Named Inventor	Joseph Bates
Attorney Docket Number	SNG.1001C9
Title of Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Singular Computing LLC	100%

The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)

16882686 filed on 05/25/2020

as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.	
Applicant claims the following fee status: ○ Small Entity ○ Micro Entity ◉ Regular Undiscounted I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.	
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number 43861 ○ A sole inventor ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ○ A joint inventor; all of whom are signing this request	
Signature	/Robert Plotkin/
Name	Robert Plotkin

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	16882694
Filing Date:	25-May-2020
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Filer:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 16882694

Filing Date: 25-May-2020

Applicant/Patent under Reexamination: Bates

Electronic Terminal Disclaimer filed on July 28, 2020

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt	
EFS ID:	40125618
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin
Filer Authorized By:	
Attorney Docket Number:	SNG.1001C9
Receipt Date:	28-JUL-2020
Filing Date:	25-MAY-2020
Time Stamp:	14:47:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$160
RAM confirmation Number	E20207RE47246942
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	34010 88fd194b8e829cfe765cc4587311a8a537c3ab83	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30513 0f61cc10bfe77e5585952376089638 98bd321fdc	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	64523		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

144359 7590 07/28/2020

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

EXAMINER	
YAARY, MICHAEL D	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
07/28/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@blueshiftip.com
eofficeaction@appcoll.com
mail@blueshiftip.com

Office Action Summary	**Application No.** 16/882,694	**Applicant(s)** Bates, Joseph	
	Examiner MICHAEL D YAARY	**Art Unit** 2182	**AIA (FITF) Status** Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 07/14/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-24 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-24 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 05/25/2020 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 07/14/2020.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 are pending in the application.

Notice of Pre-AIA or AIA Status

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*,

686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-24, are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over 1-25 of copending Application No. 16/882,686. Although the claims at issue are not identical, they are not patentably distinct from each other because the claims are directed to the same limitations recited in similar manner. For example, all of the limitations of instant claim 16, are found in claim 7 of the '686 application. The only differences between the claims are minor wording differences. This is a provisional nonstatutory double patenting rejection because the patentably

indistinct claims have not in fact been patented. Example mapping below (underlined for emphasis):

Application 16/882,694	Application 16/882,696
Claim 16 – A circuit board connected to a host computer, the circuit board comprising: a plurality of processing element arrays, each comprising: a plurality of first processing elements, wherein the plurality of first processing elements of said processing element array is no less than 5000 in number, wherein each of a first subset of the plurality of first processing elements of said processing element array is positioned at a first edge of said processing element array, and wherein each of a second subset of the plurality of first processing elements of said processing element array is positioned in the interior of said processing element array;	Claim 7 - A computing system, comprising: *a host computer*; a computing chip comprising: a processing element array comprising a plurality of first processing elements, wherein the plurality of first processing elements is no less than 5000 in number, wherein each of a first subset of the plurality of first processing elements is positioned at a first edge of the processing element array, and wherein each of a second subset of the plurality of first processing elements is positioned in the interior of the processing element array; an input-output unit connected to each of the first subset of the plurality of first processing elements;

a plurality of processing element connections, each processing element connection connecting one of the plurality of first processing elements of said processing element array with another of the plurality of first processing elements of said processing element array, wherein each of the plurality of first processing elements of said processing element array is connected to at least one other of the plurality of first processing elements of said processing element array by at least one of the plurality of processing element connections of said processing element array; a plurality of memory units, wherein each of the plurality of first processing elements of said processing element array is associated with a corresponding one of the plurality of memory units of said processing element array, and wherein each of the plurality of memory units of said processing element array is	a plurality of processing element connections, each processing element connection connecting one of the plurality of first processing elements with another of the plurality of first processing elements, wherein each of the plurality of first processing elements is connected to at least one other of the plurality of first processing elements by at least one of the plurality of processing element connections; a plurality of memory units, wherein each of the plurality of first processing elements is associated with a corresponding one of the plurality of memory units, and wherein each of the plurality of memory units is local to its associated one of the plurality of first processing elements; and, a plurality of arithmetic units, wherein each of the plurality of first processing elements has positioned therein at least

local to its associated one of the plurality of first processing elements of said processing element array; and, a plurality of arithmetic units, wherein each of the plurality of first processing elements of said processing element array has positioned therein at least one of the plurality of arithmetic units of said processing element array; wherein the plurality of arithmetic units of said processing element array each comprises a first corresponding multiplier circuit adapted to receive as a first input to the first corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the first corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits; and,	one of the plurality of arithmetic units; and, a host connection at least partially connecting the input-output unit with the host computer; wherein the plurality of arithmetic units each comprises a first corresponding multiplier circuit adapted to receive as a first input to the first corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the first corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits.

an input-output unit connected to at least one of the plurality of processing element arrays; and, a host connection at least partially connecting the input-output unit with the host computer.	
Claim 19 - The circuit board of claim 16, wherein the circuit board further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits; wherein other than the second processing elements the circuit board has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and, wherein a total count of the	Claim 8 - The computing system of claim 7, wherein the computing chip further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits; wherein, other than the plurality of second processing elements, the computing chip has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and wherein the plurality of

pluralities of first processing elements of the plurality of processing element arrays exceeds in number, by at least 100 more, the plurality of second processing elements.	first processing elements is greater in number, by at least 100, than the plurality of second processing elements.

Allowable Subject Matter

4. Claims 1-24 would be allowable if rewritten or amended to overcome the rejection(s) under Double Patenting, set forth in this Office action.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Pat. 7,242,414 - A processor having a compare extension of an instruction set architecture which incorporates a set of high performance floating point operations. The instruction set architecture incorporates a variety of data formats including single precision and double precision data formats, as well as the paired-single data format that allows two simultaneous operations on a pair of operands. The extension includes instructions directed to a magnitude compare of floating point numbers and conversions between a pair of 32-bit fixed point integers and paired-single floating point format.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL D YAARY whose telephone number is (571)270-1249. The examiner can normally be reached on Mon-Fri 9-5:30.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on (571)272-3702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MICHAEL D. YAARY/
Primary Examiner, Art Unit 2182

Notice of References Cited	Application/Control No. 16/882,694	Applicant(s)/Patent Under Reexamination Bates, Joseph	
	Examiner MICHAEL D YAARY	Art Unit 2182	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-7242414-B1	07-2007	Thekkath; Radhika	G06F9/30014	345/623
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	Art Unit
	MICHAEL D YAARY	2182

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST search with keywords	07/23/2020	MY
NPL search	07/23/2020	MY
Inventor name search	07/23/2020	MY

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/882,694	Bates, Joseph
	Examiner	**Art Unit**
	MICHAEL D YAARY	2182

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/23/2020								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
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	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								
	23	✓								
	24	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2,125	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/07/23 09:53
L2	1,225	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/07/23 09:54
L3	140	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/07/23 09:54
L4	135	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa and exponent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/07/23 09:54
L5	182	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa and exponent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/07/23 09:54
L6	54	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or "708".clas.) and array and edge and cycle and mantissa and exponent and simd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/07/23 09:56
L7	97	(Bates, Joseph).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/23 10:22

L8	9	(Bates, Joseph).in. and (Singular Computing LLC).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/07/23 10:22
S1	666	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/06/29 09:16
S2	249	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 09:20
S3	242	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier and memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 09:25
S4	165	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier and memory and binary	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 09:25
S5	39	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 09:29
S6	97	(Bates, Joseph).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/29 10:46
S7	9	(Bates, Joseph).in. and (Singular Computing LLC).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/29 10:47

S8	39	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc.) and array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 11:41
S9	62	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or G06F7/$.cpc.) and array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 11:42
S10	1	"42271192".FMID.	US-PGPUB; USPAT; FPRS; JPO	OR	OFF	2020/06/29 11:42
S11	1	"42271192".FMID.	US-PGPUB; USPAT; FPRS; JPO	OR	OFF	2020/06/29 11:42
S12	62	(G06F7/38,483,4833,5235.cpc. or H03K19/17728.cpc. or G06F7/$.cpc.) and array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 12:34
S13	395	array and edge and floating and multiplier and memory and binary and (edge near5 array)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 13:40
S14	29	array and edge and floating and multiplier and memory and binary and (edge near5 array) and mantissa	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 14:32
S15	28	array and edge and floating and multiplier and memory and binary and (edge near5 array) and mantissa and exponent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/29 14:36

7/23/2020 10:22:44 AM
C:\Users\myaary\Documents\EAST\Workspaces\16882686.wsp

Bibliographic Data

Application No: 16/882,694

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☐ No ☐ Met After Allowance

Verified and Acknowledged: /MICHAEL D. YAARY/ (Examiner's Signature) | (Initials)

Title: PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
05/25/2020	708	2182	SNG.1001C9
RULE			

APPLICANTS

Singular Computing LLC, Newton, MA, UNITED STATES

INVENTORS

Joseph Bates, Newton, MA, UNITED STATES

CONTINUING DATA

This application is a CON of 16571871 09/16/2019 PAT 10664236

16571871 is a CON of 16175131 10/30/2018 PAT 10416961

16175131 is a CON of 15784359 10/16/2017 PAT 10120648

15784359 is a CON of 14976852 12/21/2015 PAT 9792088

14976852 is a CON of 13849606 03/25/2013 PAT 9218156

13849606 is a CON of 13399884 02/17/2012 PAT 8407273

13399884 is a CON of 12816201 06/15/2010 PAT 8150902

12816201 has PRO of 61218691 06/19/2009

FOREIGN APPLICATIONS

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06/24/2020

STATE OR COUNTRY

UNITED STATES

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Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142
UNITED STATES

FILING FEE RECEIVED

$6,260

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16882694
Filing Date	2020-05-25
First Named Inventor	Joseph Bates
Art Unit	
Examiner Name	
Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/MY/	1	5153848	A	1992-10-06	Elkind et al.	
/MY/	2	7746104	B1	2010-06-29	Gaide et al.	
/MY/	3	7746108	B1	2010-06-29	Young et al.	
/MY/	4	10664236	B2	2020-05-26	Bates	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	
	Examiner Name	
	Attorney Docket Number	SNG.1001C9

	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
/MY/	1	KAHAN, W., "Pracniques: further remarks on reducing truncation errors", Communications of the ACM, Vol. 8, No. 1, page 40 (January, 1965)	
/MY/	2	Notice of Allowance mailed July 06, 2020 for U.S. Patent Application No. 16/882,686 of Joseph Bates, filed May 25, 2020, 11 pages	

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EXAMINER SIGNATURE

Examiner Signature	/MICHAEL D. YAARY/	Date Considered	07/23/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	
	Examiner Name	
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2020-07-14
Name/Print	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9	3296

144359 7590 07/23/2020

Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

EXAMINER	
YAARY, MICHAEL D	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
07/23/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@blueshiftip.com
eofficeaction@appcoll.com
mail@blueshiftip.com

Decision Granting Request for Prioritized Examination (Track I)	**Application No.** 16/882,694	**Applicant(s)** Bates, Joseph	
	Examiner APRIL M WISE	**Art Unit** OPET	**AIA (FITF) Status** Yes

1. THE REQUEST FILED 25 May 2020 IS **GRANTED** .

The above-identified application has met the requirements for prioritized examination

A. ☑ for an original nonprovisional application (Track I).
B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination**. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

A. filing a **petition for extension of time** to extend the time period for filing a reply;

B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims** , or a multiple dependent claim;

C. filing a **request for continued examination** ;

D. filing a notice of appeal;

E. filing a request for suspension of action;

F. mailing of a notice of allowance;

G. mailing of a final Office action;

H. completion of examination as defined in 37 CFR 41.102; or

I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to undersigned at (571)272-1642.

In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.

/APRIL M WISE/ Paralegal Specialist, Office of Petitions	

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16882694
Filing Date	2020-05-25
First Named Inventor	Joseph Bates
Art Unit	
Examiner Name	
Attorney Docket Number	SNG.1001C9

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5153848	A	1992-10-06	Elkind et al.	
	2	7746104	B1	2010-06-29	Gaide et al.	
	3	7746108	B1	2010-06-29	Young et al.	
	4	10664236	B2	2020-05-26	Bates	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	
	Examiner Name	
	Attorney Docket Number	SNG.1001C9

	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	KAHAN, W., "Pracniques: further remarks on reducing truncation errors", Communications of the ACM, Vol. 8, No. 1, page 40 (January, 1965)	
	2	Notice of Allowance mailed July 06, 2020 for U.S. Patent Application No. 16/882,686 of Joseph Bates, filed May 25, 2020, 11 pages	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16882694
	Filing Date	2020-05-25
	First Named Inventor	Joseph Bates
	Art Unit	
	Examiner Name	
	Attorney Docket Number	SNG.1001C9

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert Plotkin/	Date (YYYY-MM-DD)	2020-07-14
Name/Print	Robert Plotkin	Registration Number	43861

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application Number	16/882,694
	Filing Date	05/25/2020
	First Named Inventor	Joseph Bates
	Art Unit	
	Client Number	SNG
Page 1 of 1	**Matter Number**	1001C9

GENERAL

Pursuant to 37 C.F.R. 1.97 and 1.98 and to the duty of disclosure set forth in 37 C.F.R. 1.56, the Examiner in charge of the above-identified application is requested to consider and make of record the references listed herewith. A copy of each listed reference, other than U.S. patents/applications and references cited in a parent application, is enclosed.

Although the information submitted herewith may be "material" to the Examiner's consideration of the subject application, this submission is not intended to constitute an admission that such information is "prior art" as to the claimed invention.

In accordance with 37 C.F.R. 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made.

TIMING

In accordance with 37 CFR 1.97(b), this Information Disclosure Statement is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits; or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

CERTIFICATION STATEMENT

No certification statement is required. This Information Disclosure Statement is being filed in accordance with 37 CFR 1.97(b).

FEE

No fee is required. This Information Disclosure Statement is being filed in accordance with 37 CFR 1.97(b).

If necessary, the Director is hereby authorized to charge or credit Deposit Account No. 60/1293 for any additional fees, or any underpayment or credit for overpayment in connection herewith. Please reference attorney docket number SNG-1001C9 for any such charge or credit.

ADDITIONAL COMMENTS

SIGNATURE

Signature	/Robert Plotkin/	**Date**	07/14/2020
Name	Robert Plotkin	**Registration Number**	43861

SyncIDS.com

Electronic Acknowledgement Receipt

EFS ID:	39997031
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	14-JUL-2020
Filing Date:	25-MAY-2020
Time Stamp:	15:56:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	SNG-1001C9_PTO_IDS-Form_Initial_Filing.pdf	1053423 a4f3bb3ba19bc1febe511b7869edf227f352d829	no	4

Warnings:

Information:					
2	Transmittal Letter	SNG-1001C9_Transmittal-Letter.pdf	513841 e1cf531ddca2a7fc371c13a062aaad9f0c10e53a	no	1
Warnings:					
Information:					
3	Non Patent Literature	SNG-1001C9-NPL-001.pdf	303367 c14a5b06e58f4e0f6d95fbd4a3deece64c5c0e39	no	1
Warnings:					
Information:					
4	Non Patent Literature	SNG-1001C9-NPL-002.pdf	537905 d5d5e6a8607a1d5d5b1606a40d5a5d31e59393ce	no	11
Warnings:					
Information:					
		Total Files Size (in bytes):	2408536		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/882,694	05/25/2020		2120	SNG.1001C9	24	3

CONFIRMATION NO. 3296

144359
Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

UPDATED FILING RECEIPT

OC000000118346123

Date Mailed: 07/13/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Joseph Bates, Newton, MA;

Applicant(s)

Singular Computing LLC, Newton, MA;

Power of Attorney: The patent practitioners associated with Customer Number 144359

Domestic Priority data as claimed by applicant

This application is a CON of 16/571,871 09/16/2019 PAT 10664236
which is a CON of 16/175,131 10/30/2018 PAT 10416961
which is a CON of 15/784,359 10/16/2017 PAT 10120648
which is a CON of 14/976,852 12/21/2015 PAT 9792088
which is a CON of 13/849,606 03/25/2013 PAT 9218156
which is a CON of 13/399,884 02/17/2012 PAT 8407273
which is a CON of 12/816,201 06/15/2010 PAT 8150902
which claims benefit of 61/218,691 06/19/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 06/24/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/882,694**

Projected Publication Date: 10/22/2020

Non-Publication Request: No

Early Publication Request: No

Title

PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: Yes

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Google Ex. 1002 - Page 351

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/882,694

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	24 minus 20 =	* 4			OR	x 100 =	400
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2120

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

ATTORNEY'S DOCKET NO: SNG.1001C9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.:	16/882,694
Confirmation No.:	3296
Title:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Inventor:	Bates, Joseph
Filing Date:	05/25/2020

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

We are in receipt of the Notice to File Corrected Application Papers in connection with application 16/882,694, mailed June 26, 2020. The Notice indicates FIGS. 7-11 are missing and/or blurry and, therefore, not electronically reproducible.

The general purpose of FIGS. 7-11 is to show an original image (FIG. 7) and a blurred version of that image (FIG. 8), and then to show the results of applying various processes for de-blurring (i.e., removing the blurring from) the blurred image (FIGS. 9-11).

Because FIGS. 7-11 are all images, and because it is intended and necessary for FIGS. 7-11 to include some degree of blurring for the purpose of illustrating embodiments of the present invention which remove blurring from images, Applicant requests that FIGS. 7-11 be allowed to remain in the application in their current form. In particular, it would not be possible to re-draw FIGS. 7-11 as line drawings while in accordance with the purpose of FIGS. 7-11,

because line drawings would not be capable of showing the blurring needed in FIGS. 7-11.

More specifically, as described in the specification, FIG. 7 is an image, namely a satellite picture of a building used during Barack Obama's inauguration (see paragraph [00121]).

As further described in the specification, FIG. 8 shows the result of significantly blurring the image of FIG. 7. In other words, FIG. 8 is intentionally blurry. As stated in the specification, it is intended that it be difficult to see any particular objects in the image of FIG. 8 (see paragraph [00122]).

As further described in the specification, FIG. 9 shows the result of deblurring the image of FIG. 7 using standard floating point arithmetic, FIG. 10 shows the result of deblurring the image of FIG. 7 using fp+noise arithmetic, and FIG. 11 shows the result of deblurring the image of FIG. 7 using lns arithmetic (see paragraph [00121]). Because the purpose of FIGS. 9-11 is to show differences between the results produced by different methods of deblurring, it would not be possible to redraw FIGS. 9-11 as line drawings and still illustrate clearly the effects of deblurring. In fact, such line drawings would fail to show any blurring at all, and therefore would not clearly illustrate the meaning of FIGS. 9-11.

It is not necessary that FIGS. 7-11 be reproducible perfectly. It is only necessary that FIGS. 7-11 be reproducible clearly enough

to illustrate the differences among the deblurring techniques used to produce FIGS. 9, 10, and 11. Applicant submits that the reproduction techniques used to create the US publication will be sufficient for this purpose.

Therefore, Applicant submits that it is not necessary to re-create FIGS. 7-11 as line drawings, and furthermore that any such line drawings would conform with the purpose of FIGS. 7-11 much less accurately than the current versions of FIGS. 7-11.

Google Ex. 1002 - Page 355

CONCLUSIONS

If this response is not considered timely filed and if a request for extension of time is otherwise absent, applicant hereby requests any extension of time. Please charge any fees or make any credits, to Deposit Account No. 60/1293.

Respectfully submitted,

/Robert Plotkin/ July 8, 2020
Robert Plotkin, Esq. Date
Reg. No. 43861

Blueshift IP LLC,
1 Broadway, 14th Floor,
Cambridge, MA 02142
Tel: (617) 207-6141
Fax: (617) 207-6215

Electronic Acknowledgement Receipt

EFS ID:	39946994
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin/Kimberly Hauser
Filer Authorized By:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9
Receipt Date:	08-JUL-2020
Filing Date:	25-MAY-2020
Time Stamp:	16:40:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	SNG-1001C9_Response_Not_File_Corr_Drawings.pdf	57607 250faace80d4cbc3c2a969c484a44bfb67b8516c	no	4

Warnings:

Information:	
Total Files Size (in bytes):	57607

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE
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PRESORTED
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Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

Courtesy Reminder for
Application Serial No: 16/882,694

Attorney Docket No: SNG.1001C9
Customer Number: 144359
Date of Electronic Notification: 06/26/2020

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

mail@blueshiftip.com
eofficeaction@appcoll.com
docketing@blueshiftip.com

To view your correspondence online or update your email addresses, please visit us anytime at **https://ppair-my.uspto.gov/pair/PrivatePair.**
If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/882,694

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	24 minus 20 =	* 4			OR	x 100 =	400
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2120

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/882,694	05/25/2020		2120	SNG.1001C9	24	3

CONFIRMATION NO. 3296

144359
Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

FILING RECEIPT

OC000000017993230

Date Mailed: 06/26/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Joseph Bates, Newton, MA;

Applicant(s)

Singular Computing LLC, Newton, MA;

Power of Attorney: The patent practitioners associated with Customer Number 144359

Domestic Priority data as claimed by applicant

This application is a CON of 16/571,871 09/16/2019 PAT 10664236
which is a CON of 16/175,131 10/30/2018 PAT 10416961
which is a CON of 15/784,359 10/16/2017 PAT 10120648
which is a CON of 14/976,852 12/21/2015 PAT 9792088
which is a CON of 13/849,606 03/25/2013 PAT 9218156
which is a CON of 13/399,884 02/17/2012 PAT 8407273
which is a CON of 12/816,201 06/15/2010 PAT 8150902
which claims benefit of 61/218,691 06/19/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 06/24/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/882,694**

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No

Title

PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: Yes

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

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Google Ex. 1002 - Page 364

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/882,694	05/25/2020	Joseph Bates	SNG.1001C9

CONFIRMATION NO. 3296

144359
Blueshift IP LLC
1 Broadway, 14th Floor
Cambridge, MA 02142

FORMALITIES LETTER

OC000000117993231

Date Mailed: 06/26/2020

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given **TWO MONTHS** from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings submitted to the Office are not electronically reproducible because portions of figures 7 to 11 are missing and/or blurry.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tnguyen/

Transmittal for Power of Attorney

to One or More Registered Practitioners

Equivalent to USPTO Form PTO/AIA/82A

Application Number:		Attorney Docket Number:	SNG.1001C9
Filing Date:	05/25/2020	Examiner Name:	
First Named Inventor:	BATES, Joseph	Art Unit:	
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT		

This form is being submitted with the attached Power of Attorney by Applicant (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5.

Signature of Patent Practitioner

/Robert Plotkin/	05-25-2020
Signature	Date
Robert Plotkin	617-207-6141
Name	Telephone
43861	
Registration Number	

Power of Attorney

Equivalent to USPTO Form PTO/AIA/82B

1. Revocation of Previous Powers of Attorney

I/we hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter (form PTO/AIA/82A or equivalent).

2. Appointment of Practitioner(s)

I/we hereby appoint the Practitioner(s) associated with Customer Number 144359 (which is associated with the law firm of Blueshift IP LLC) as my/our attorney(s)/agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent). By signing this Power of Attorney, I hereby affirm that I am authorized to act on behalf of one of the following: (1) an Assignee; (2) a person to whom the inventor is under an obligation to assign; and (3) a person who otherwise shows sufficient proprietary interest.

3. Change of Correspondence Address

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to the address associated with the above-mentioned customer number 144359 (which is associated with the law firm of Blueshift IP LLC).

4. Signature(s)

a. Applicant 1

I am an Applicant:

- ☐ Inventor or Joint Inventor
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

or

I am authorized to act on behalf of the Applicant:

- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

Signature	Date: 16 October 2017
Name: Joseph Bates	Telephone: 781-538-5664
Title: President	Company: Singular Computing LLC

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Filer:	Robert Plotkin
Attorney Docket Number:	SNG.1001C9

Filed as Large Entity

Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
REQUEST FOR PRIORITIZED EXAMINATION	1817	1	4000	4000
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	4	100	400
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	1830	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**6260**

Electronic Acknowledgement Receipt	
EFS ID:	39528114
Application Number:	16882694
International Application Number:	
Confirmation Number:	3296
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT
First Named Inventor/Applicant Name:	Joseph Bates
Customer Number:	144359
Filer:	Robert Plotkin
Filer Authorized By:	
Attorney Docket Number:	SNG.1001C9
Receipt Date:	25-MAY-2020
Filing Date:	
Time Stamp:	21:04:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$6260
RAM confirmation Number	E20205OL04594374
Deposit Account	601293
Authorized User	Robert Plotkin
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	SNG-1001C9_ADS.pdf	1256646 e4a6e0967b7ac67e4be05bd7c1494c6bf851ddef	no	9
Warnings:					
Information:					
2	TrackOne Request	SNG-1001C9_Track_One_Cert.pdf	124214 7dfe6214ce99255e463eff95a51f892e2a2ca5a9	no	2
Warnings:					
Information:					
3	Specification	SNG-1001C9_Specification.pdf	206063 bca55b217d57785ad10c8b437b124b068e58e627	no	76
Warnings:					
Information:					
4	Drawings-only black and white line drawings	SNG-1001C9_Drawings.pdf	906057 bdb09602e428bda21f6323a20fc7d436fc8cea4f	no	11
Warnings:					
Information:					
5	Oath or Declaration filed	SNG-1001C9_Declaration.pdf	828744 0404c37c5a56fb7e3dcdfdbb002308050a9e4a33	no	4
Warnings:					
Information:					
6	Power of Attorney	SNG-1001C9_POA_Transmittal.pdf	106091 59243ca1988a62b397c2efbb44eb1b0b2d2d4acb	no	1
Warnings:					
Information:					

7	Power of Attorney	SNG-1001C9_POA.pdf	350602 4a83f277c61c48451ec674f0d410be4462d8a631	no	2
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	41860 c132e29bbb9c5b5864890555cae71acc2683cab6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3820277		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SNG.1001C9
	Application Number	
Title of Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Joseph		Bates	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Newton	State/Province	MA	Country of Residence	US

Mailing Address of Inventor:

Address 1	c/o Singular Computing LLC
Address 2	10 Regent Street

City	Newton	State/Province	US
Postal Code	02465	**Country** i	MA

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	144359		
Email Address	mail@blueshiftip.com	Add Email	Remove Email

Application Information:

Title of the Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT		
Attorney Docket Number	SNG.1001C9	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	11	**Suggested Figure for Publication (if any)**	1

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SNG.1001C9
	Application Number	
Title of Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	144359		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of		

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SNG.1001C9
	Application Number	
Title of Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT	

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16571871	2019-09-16

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16571871	Continuation of	16175131	2018-10-30	10416961	2019-09-17

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16175131	Continuation of	15784359	2017-10-16	10120648	2018-11-06

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15784359	Continuation of	14976852	2015-12-21	9792088	2017-10-17

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14976852	Continuation of	13849606	2013-03-25	9218156	2015-12-22

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13849606	Continuation of	13399884	2012-02-17	8407273	2013-03-26

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13399884	Continuation of	12816201	2010-06-15	8150902	2012-04-03

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12816201	Claims benefit of provisional	61218691	2009-06-19

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SNG.1001C9
	Application Number	
Title of Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☒ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SNG.1001C9
	Application Number	
Title of Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SNG.1001C9
	Application Number	
Title of Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Singular Computing LLC		
Mailing Address Information For Applicant:			
Address 1	10 Regent Street		
Address 2			
City	Newton	**State/Province**	MA
Country	US	Postal Code	02465
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SNG.1001C9
	Application Number	
Title of Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Robert Plotkin/			Date (YYYY-MM-DD)	2020-05-25
First Name	Robert	Last Name	Plotkin	Registration Number	43861

Additional Signature may be generated within this form by selecting the Add button. Add

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SNG.1001C9
	Application Number	
Title of Invention	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (04-14)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Joseph Bates	Nonprovisional Application Number (if known):	
Title of Invention:	PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.

2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.

3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Robert Plotkin/	Date 05-25-2020
Name (Print/Typed) Robert Plotkin	Practitioner Registration Number 43861

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☑ *Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

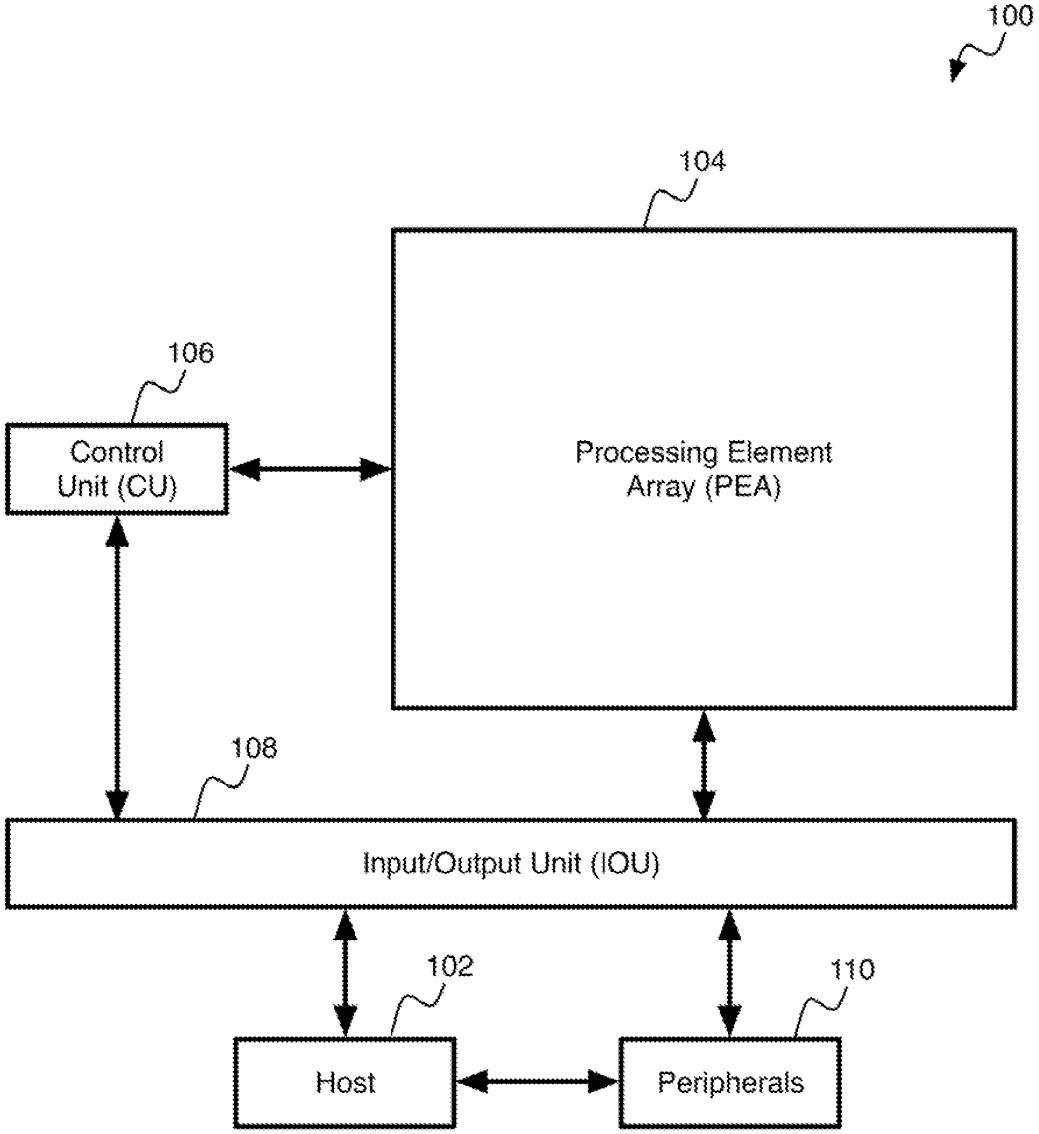

100
104
106
Control Unit (CU)
Processing Element Array (PEA)
108
Input/Output Unit (IOU)
102
110
Host
Peripherals

FIG. 1

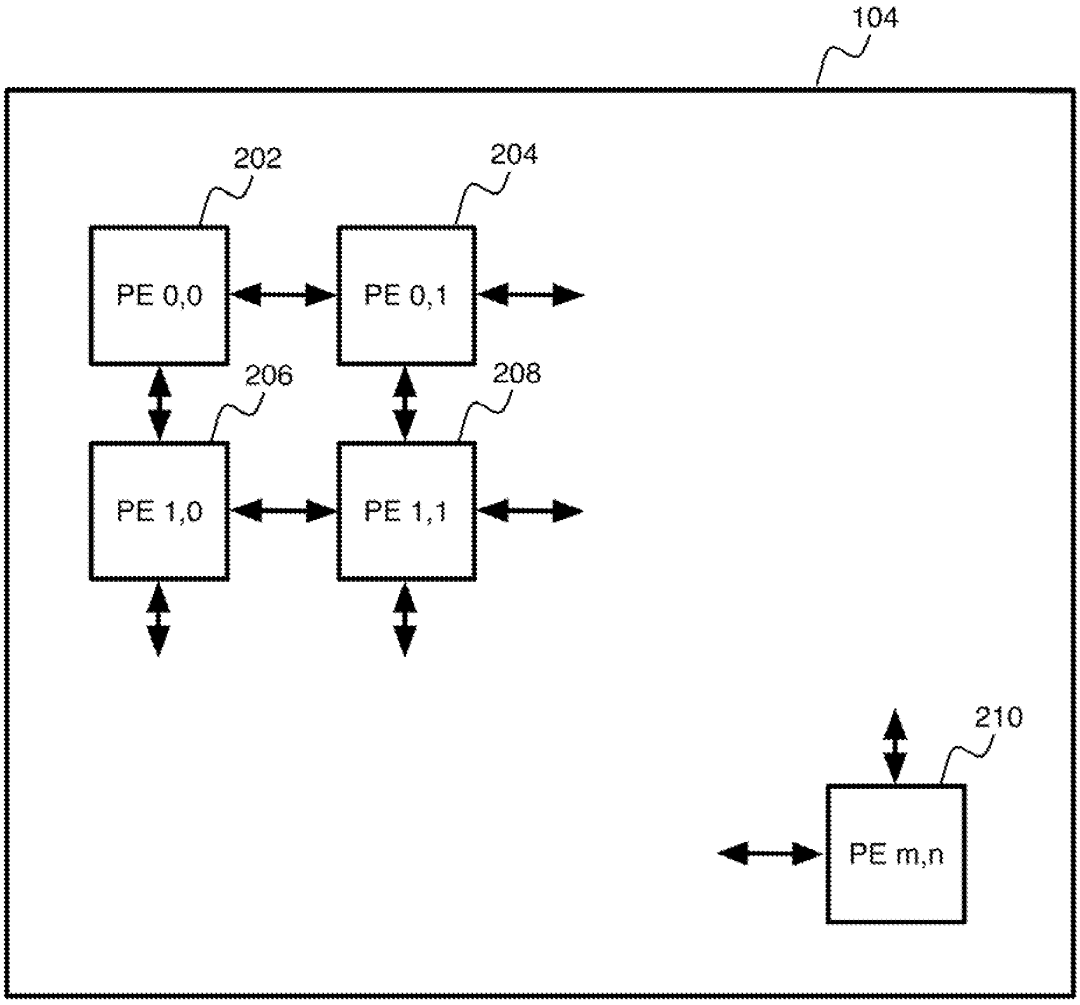


FIG. 2

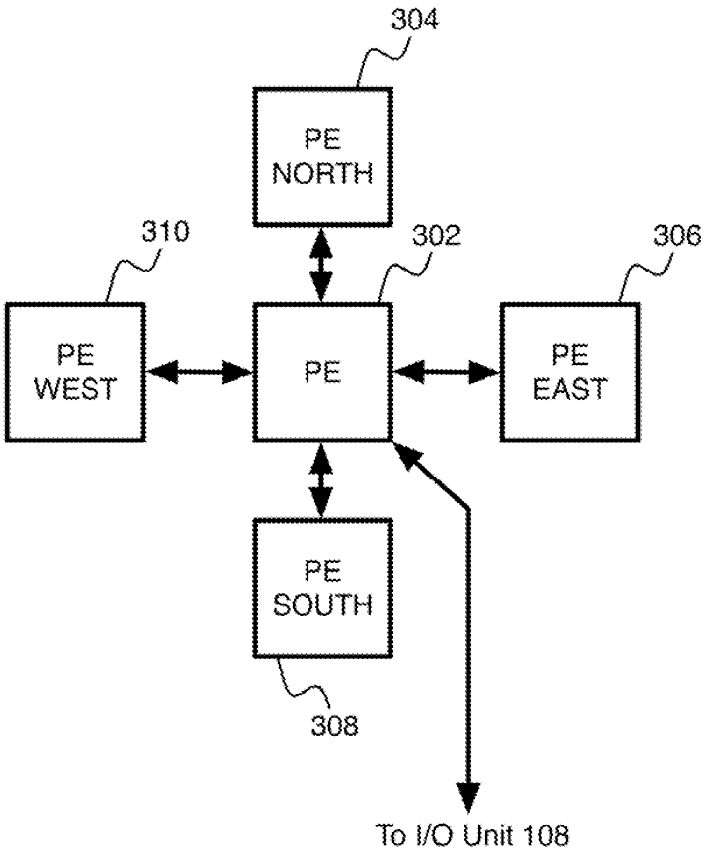

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FIG. 3

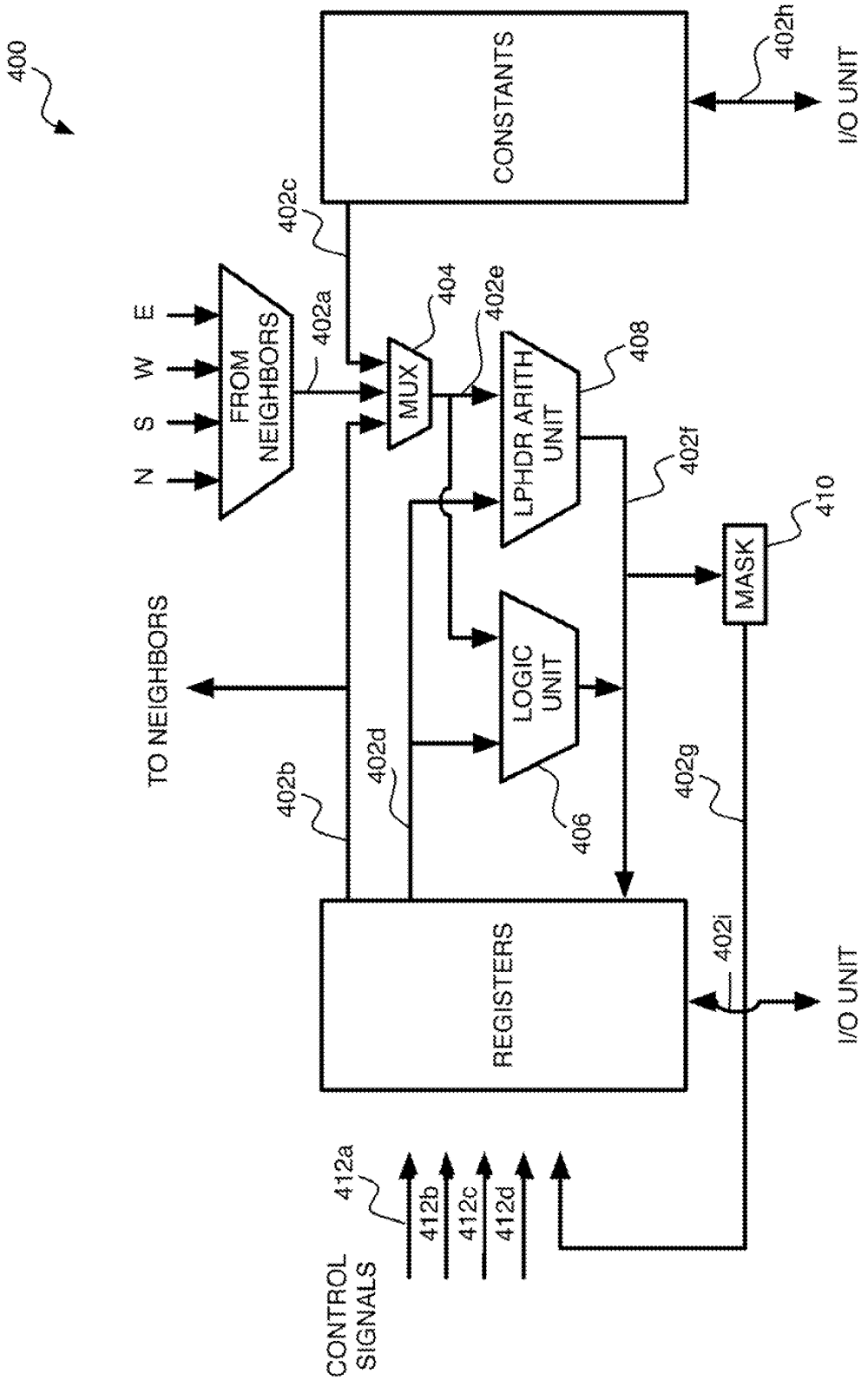

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408
402f
MASK
410
TO NEIGHBORS
LOGIC UNIT
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402d
402g
REGISTERS
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I/O UNIT
CONTROL SIGNALS
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FIG. 4

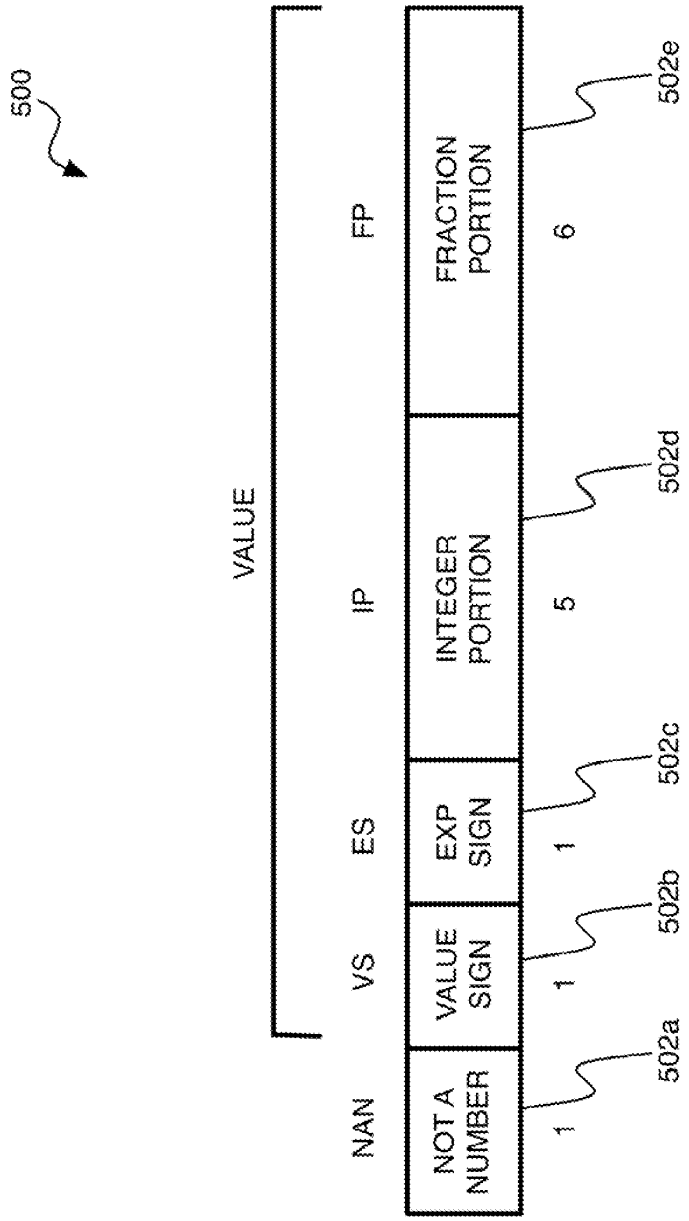

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IP
FP
NOT A NUMBER
VALUE SIGN
EXP SIGN
INTEGER PORTION
FRACTION PORTION
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502c
502d
502e

FIG. 5

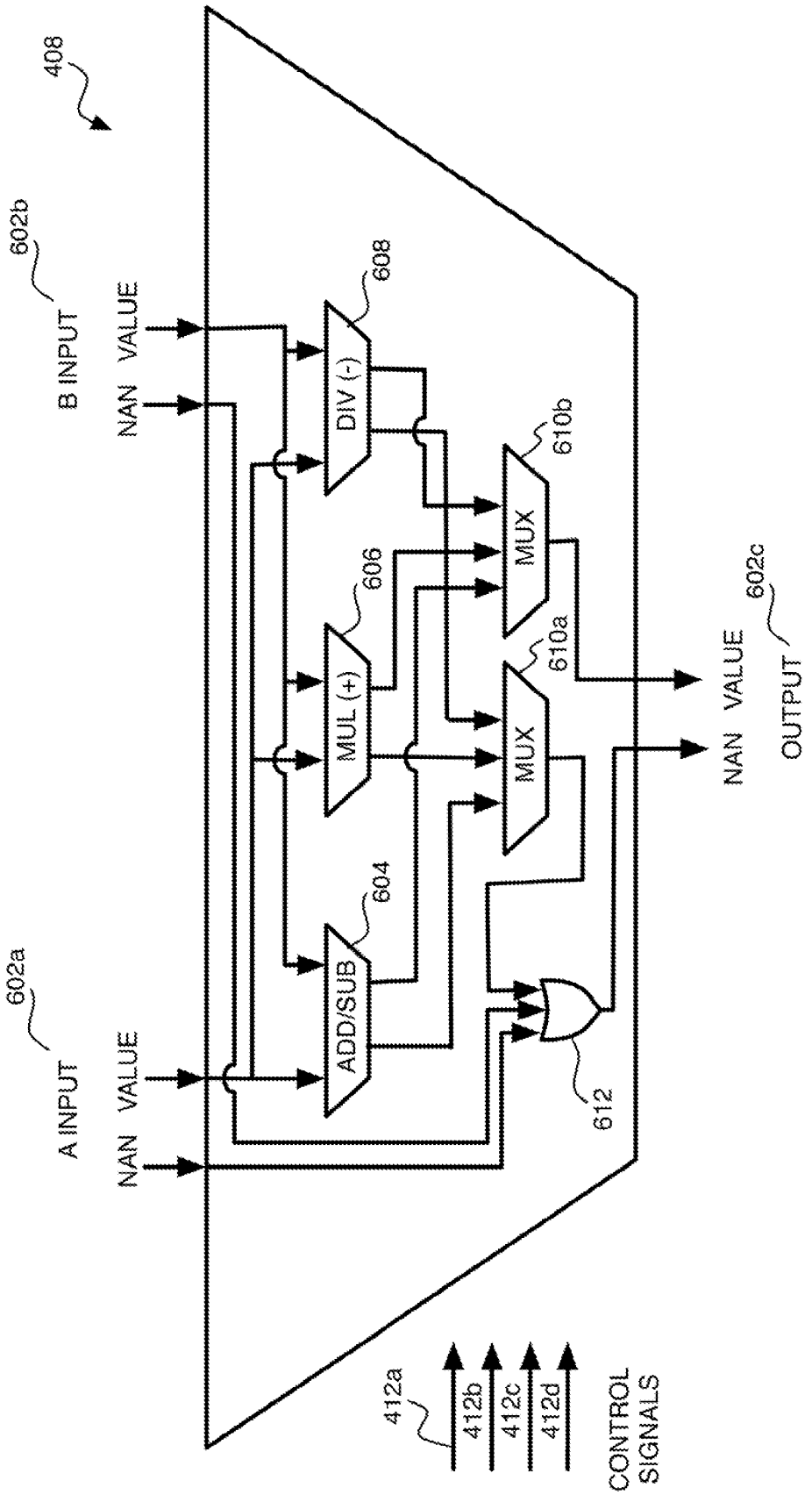

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DIV (-)
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MUX
606
MUL (+)
610a
MUX
602c
NAN VALUE
OUTPUT
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NAN VALUE
604
ADD/SUB
612
412a
412b
412c
412d
CONTROL SIGNALS

FIG. 6



FIG. 7

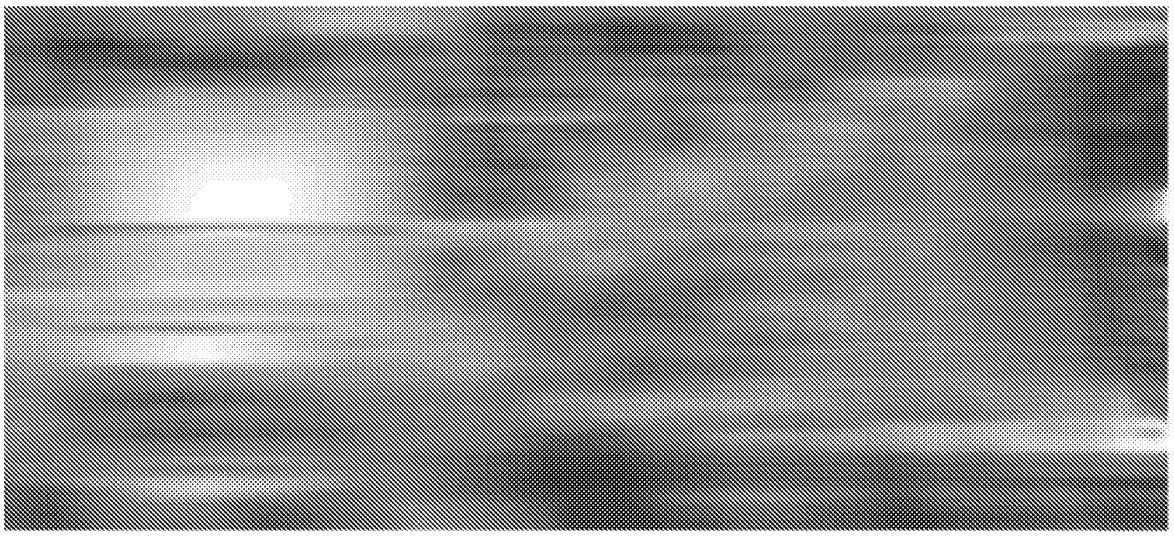


FIG. 8



FIG. 9



FIG. 10



FIG. 11

Declaration

Equivalent to USPTO Form PTO/AIA/01

Application Number:	13/849,606	Attorney Docket Number:	A0006-1001C2
Filing Date:	03/25/2013	Examiner Name:	Michael D. Yaary
First Named Inventor:	BATES, Joseph	Art Unit:	N/A
Title of Invention:	Processing with Compact Arithmetic Processing Element		

Each below-named inventor hereby declares that:

1. Application

This Declaration is directed to:

☐ the attached application; or

☒ United States application or PCT international application number 13/849,606,

filed on 03/25/2013 (mm/dd/yyyy).

2. Declaration

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this Declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

3. Duty of Disclosure

I hereby acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which become available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

4. Warning

The undersigned is/are cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. The undersigned is/are advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

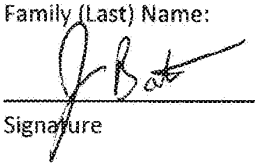
Google Ex. 1002 - Page 398

5. **Signature(s)**

a. Inventor 1

Given Name (First and Middle): Joseph

Family (Last) Name: Bates



Signature

29 MARCH 2013

Date

b. Inventor 2

Given Name (First and Middle): _____

Family (Last) Name: _____

_____ _____

Signature Date

c. Inventor 3

Given Name (First and Middle): _____

Family (Last) Name: _____

_____ _____

Signature Date

d. Inventor 4

Given Name (First and Middle): _____

Family (Last) Name: _____

_____ _____

Signature Date

e. Inventor 5

Given Name (First and Middle): _____

Family (Last) Name: _____

_____ _____

Signature Date

f. Inventor 6

Given Name (First and Middle): _____

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PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

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Background

[0002] The ability to compute rapidly has become enormously important to humanity. Weather and climate prediction, medical applications (such as drug design and non-invasive imaging), national defense, geological exploration, financial modeling, Internet search, network communications, scientific research in varied fields, and even the design of new computing hardware have each become dependent on the ability to rapidly perform massive amounts of calculation. Future progress, such as the computer-aided design of complex nano-scale systems or development of consumer products that can see, hear, and understand, will demand economical delivery of even greater computing power.

[0003] Gordon Moore's prediction, that computing performance per dollar would double every two years, has proved valid for over 30 years and looks likely to continue in some form. But despite this rapid exponential improvement, the reality is that the inherent computing power available from silicon has grown far more quickly than it has been made available to software. In other words, although the theoretical computing power of

computing hardware has grown exponentially, the interfaces through which software is required to access the hardware limits the ability of software to use hardware to perform computations at anything approaching the hardware's theoretical maximum computing power.

[0004] Consider a modern silicon microprocessor chip containing about one billion transistors, clocked at roughly 1 GHz. On each cycle the chip delivers approximately one useful arithmetic operation to the software it is running. For instance, a value might be transferred between registers, another value might be incremented, perhaps a multiply is accomplished. This is not terribly different from what chips did 30 years ago, though the clock rates are perhaps a thousand times faster today.

[0005] Real computers are built as physical devices, and the underlying physics from which the machines are built often exhibits complex and interesting behavior. For example, a silicon MOSFET transistor is a device capable of performing interesting non-linear operations, such as exponentiation. The junction of two wires can add currents. If configured properly, a billion transistors and wires should be able to perform some significant fraction of a billion interesting computational operations within a few propagation delays of the basic components (a "cycle" if the overall design is a traditional digital design). Yet, today's CPU chips use their billion transistors to enable software to perform merely a few such operations per cycle, not the significant fraction of the billion that might be possible.

Summary

[0006] Embodiments of the present invention are directed to a processor or other device, such as a programmable and/or massively parallel processor or other device, which includes processing elements designed to perform arithmetic operations (possibly but not necessarily including, for example, one or more of addition, multiplication, subtraction, and division) on numerical values of low precision but high dynamic range ("LPHDR arithmetic"). Such a processor or other device may, for example, be implemented on a single chip. Whether or not implemented on a single chip, the number of LPHDR arithmetic elements in the processor or other device in certain embodiments of the present invention significantly exceeds (e.g., by at least 20 more than three times) the number of arithmetic elements in the processor or other device which are designed to perform high dynamic range arithmetic of traditional precision (such as 32 bit or 64 bit floating point arithmetic).

[0007] In some embodiments, “low precision” processing elements perform arithmetic operations which produce results that frequently differ from exact results by at least .1% (one tenth of one percent). This is far worse precision than the widely used IEEE 754 single precision floating point standard. Programmable embodiments of the present invention may be programmed with algorithms that function adequately despite these unusually large relative errors. In some embodiments, the processing elements have “high dynamic range” in the sense that they are capable of operating on inputs and/or producing outputs spanning a range at least as large as from one millionth to one

million.

Brief Description of the Drawings

[0008] FIG. 1 is an example overall design of a SIMD processor according to one embodiment of the present invention.

[0009] FIG. 2 is an example of the Processing Element Array of a SIMD processor according to one embodiment of the present invention.

[0010] FIG. 3 is an example of how a Processing Element in a Processing Element Array communicates data with other parts of the processor according to one embodiment of the present invention.

[0011] FIG. 4 is an example design for a Processing Element according to one embodiment of the present invention.

[0012] FIG. 5 is an example LPHDR data word format according to one embodiment of the present invention.

[0013] FIG. 6 is an example design for an LPHDR arithmetic unit according to one embodiment of the present invention.

[0014] FIG. 7 is an original image.

[0015] FIG. 8 is an image blurred by a blur kernel according to one embodiment of the present invention.

[0016] FIG. 9 is an image produced by Richardson Lucy deconvolution using floating point arithmetic according to one embodiment of the present invention.

[0017] FIG. 10 is an image produced by Richardson Lucy deconvolution using LPHDR floating point arithmetic with added noise (fp+noise) according to one embodiment of the present invention.

[0018] FIG. 11 is an image produced by Richardson Lucy

deconvolution using LPHDR logarithmic arithmetic (lns) according to one embodiment of the present invention.

Detailed Description

[0019] As described above, today's CPU chips make inefficient use of their transistors. For example, a conventional CPU chip containing a billion transistors might enable software to perform merely a few operations per clock cycle. Although this is highly inefficient, those having ordinary skill in the art design CPUs in this way for what are widely accepted to be valid reasons. For example, such designs satisfy the (often essential) requirement for software compatibility with earlier designs. Furthermore, they deliver great precision, performing exact arithmetic with integers typically 32 or 64 bits long and performing rather accurate and widely standardized arithmetic with 32 and 64 bit floating point numbers. Many applications need this kind of precision. As a result, conventional CPUs typically are designed to provide such precision, using on the order of a million transistors to implement the arithmetic operations.

[0020] There are many economically important applications, however, which are not especially sensitive to precision and that would greatly benefit, in the form of application performance per transistor, from the ability to draw upon a far greater fraction of the computing power inherent in those million transistors. Current architectures for general purpose computing fail to deliver this power.

[0021] Because of the weaknesses of conventional computers, such as typical microprocessors, other kinds of computers have been developed to attain higher performance.

These machines include single instruction stream/multiple data stream (SIMD) designs, multiple instruction stream/multiple data stream (MIMD) designs, reconfigurable architectures such as field programmable gate arrays (FPGAs), and graphics processing unit designs (GPUs) which, when applied to general purpose computing, may be viewed as single instruction stream/multiple thread (SIMT) designs.

[0022] SIMD machines follow a sequential program, with each instruction performing operations on a collection of data. They come in two main varieties: vector processors and array processors. Vector processors stream data through a processing element (or small collection of such elements). Each component of the data stream is processed similarly. Vector machines gain speed by eliminating many instruction fetch/decode operations and by pipelining the processor so that the clock speed of the operations is increased.

[0023] Array processors distribute data across a grid of processing elements (PEs). Each element has its own memory. Instructions are broadcast to the PEs from a central control until, sequentially. Each PE performs the broadcast instruction on its local data (often with the option to sit idle that cycle). Array processors gain speed by using silicon efficiently—using just one instruction fetch/decode unit to drive many small simple execution units in parallel.

[0024] Array processors have been built using fixed point arithmetic at a wide variety of bit widths, such as 1, 4, 8, and wider, and using floating point arithmetic. Small bit widths allow the processing elements to be small, which allows more of them to fit in the computer, but many operations must be carried out in sequence to perform

conventional arithmetic calculations. Wider widths allow conventional arithmetic operations to be completed in a single cycle. In practice, wider widths are desirable. Machines that were originally designed with small bit widths, such as the Connection Machine-1 and the Goodyear Massively Parallel Processor, which each used 1 bit wide processing elements, evolved toward wider data paths to better support fast arithmetic, producing machines such as the Connection Machine-2 which included 32 bit floating point hardware and the MasPar machines which succeeded the Goodyear machine and provided 4 bit processing elements in the MasPar-1 and 32 bit processing elements in the MasPar-2.

[0025] Array processors also have been designed to use analog representations of numbers and analog circuits to perform computations. The SCAMP is such a machine. These machines provide low precision arithmetic, in which each operation might introduce perhaps an error of a few percentage points in its results. They also introduce noise into their computations, so the computations are not repeatable. Further, they represent only a small range of values, corresponding for instance to 8 bit fixed point values rather than providing the large dynamic range of typical 32 or 64 bit floating point representations. Given these limitations, the SCAMP was not intended as a general purpose computer, but instead was designed and used for image processing and for modeling biological early vision processes. Such applications do not require a full range of arithmetic operations in hardware, and the SCAMP, for example, omits general division and multiplication from its design.

[0026] While SIMD machines were popular in the 1980s,

as price/performance for microprocessors improved designers began building machines from large collections of communicating microprocessors. These MIMD machines are fast and can have price/performance comparable to their component microprocessors, but they exhibit the same inefficiency as those components in that they deliver to their software relatively little computation per transistor.

[0027] Field Programmable Gate Arrays (FPGAs) are integrated circuits containing a large grid of general purpose digital elements with reconfigurable wiring between those elements. The elements originally were single digital gates, such as AND and OR gates, but evolved to larger elements that could, for instance, be programmed to map 6 inputs to 1 output according to any Boolean function. This architecture allows the FPGA to be configured from external sources to perform a wide variety of digital computations, which allows the device to be used as a co-processor to a CPU to accelerate computation. However, arithmetic operations such as multiplication and division on integers, and especially on floating point numbers, require many gates and can absorb a large fraction of an FPGA's general purpose resources. For this reason, modern FPGAs often devote a significant portion of their area to providing dozens or hundreds of multiplier blocks, which can be used instead of general purpose resources for computations requiring multiplication. These multiplier blocks typically perform 18 bit or wider integer multiplies, and use many transistors, as similar multiplier circuits do when they are part of a general purpose CPU.

[0028] Existing Field Programmable Analog Arrays (FPAAs) are analogous to FPGAs, but their configurable

elements perform analog processing. These devices generally are intended to do signal processing, such as helping model neural circuitry. They are relatively low precision, have relatively low dynamic range, and introduce noise into computation. They have not been designed as, or intended for use as, general purpose computers. For instance, they are not seen by those having ordinary skill in the art as machines that can run the variety of complex algorithms with floating point arithmetic that typically run on high performance digital computers.

[0029] Finally, Graphics Processing Units (GPUs) are a variety of parallel processor that evolved to provide high speed graphics capabilities to personal computers. They offer standard floating point computing abilities with very high performance for certain tasks. Their computing model is sometimes based on having thousands of nearly identical threads of computing (SIMT), which are executed by a collection of SIMD-like internal computing engines, each of which is directed and redirected to perform work for which a slow external DRAM memory has provided data. Like other machines that implement standard floating point arithmetic, they use many transistors for that arithmetic. They are as wasteful of those transistors, in the sense discussed above, as are general purpose CPUs.

[0030] Some GPUs include support for 16 bit floating point values (sometimes called the “Half” format). The GPU manufacturers, currently such as NVIDIA or AMD/ATI, describe this capability as being useful for rendering images with higher dynamic range than the usual 32 bit RGBA format, which uses 8 bits of fixed point data per color, while also saving space over using 32 bit floating point for color components. The special effects movie firm

Industrial Light and Magic (ILM) independently defined an identical representation in their OpenEXR standard, which they describe as "a high dynamic-range (HDR) image file format developed by Industrial Light & Magic for use in computer imaging applications." Wikipedia (late 2008) describes the 16 bit floating point representation thusly: "This format is used in several computer graphics environments including OpenEXR, OpenGL, and D3DX. The advantage over 8-bit or 16-bit binary integers is that the increased dynamic range allows for more detail to be preserved in highlights and shadows. The advantage over 32-bit single precision binary formats is that it requires half the storage and bandwidth."

[0031] When a graphics processor includes support for 16 bit floating point, that support is alongside support for 32 bit floating point, and increasingly, 64 bit floating point. That is, the 16 bit floating point format is supported for those applications that want it, but the higher precision formats also are supported because they are believed to be needed for traditional graphics applications and also for so called "general purpose" GPU applications. Thus, existing GPUs devote substantial resources to 32 (and increasingly 64) bit arithmetic and are wasteful of transistors in the sense discussed above.

[0032] The variety of architectures mentioned above are all attempts to get more performance from silicon than is available in a traditional processor design. But designers of traditional processors also have been struggling to use the enormous increase in available transistors to improve performance of their machines. These machines often are required, because of history and economics, to support large existing instruction sets, such

as the Intel x86 instruction set. This is difficult, because of the law of diminishing returns, which does not enable twice the performance to be delivered by twice the transistor count. One facet of these designers' struggle has been to increase the precision of arithmetic operations, since transistors are abundant and some applications could be sped up significantly if the processor natively supported long (e.g., 64 bit) numbers. With the increase of native fixed point precision from 8 to 16 to 32 to 64 bits, and of floating point from 32 to 64 and sometimes 128 bits, programmers have come to think in terms of high precision and to develop algorithms based on the assumption that computer processors provide such precision, since it comes as an integral part of each new generation of silicon chips and thus is “free.”

[0033] Embodiments of the present invention efficiently provide computing power using a fundamentally different approach than those described above. In particular, embodiments of the present invention are directed to computer processors or other devices which use low precision high dynamic range (LPHDR) processing elements to perform computations (such as arithmetic operations).

[0034] One variety of LPHDR arithmetic represents values from one millionth up to one million with a precision of about 0.1%. If these values were represented and manipulated using the methods of floating point arithmetic, they would have binary mantissas of no more than 10 bits plus a sign bit and binary exponents of at least 5 bits plus a sign bit. However, the circuits to multiply and divide these floating point values would be relatively large. One example of an alternative embodiment

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is to use a logarithmic representation of the values. In such an approach, the values require the same number of bits to represent, but multiplication and division are implemented as addition and subtraction, respectively, of the logarithmic representations. Addition and subtraction may be implemented efficiently as described below. As a result, the area of the arithmetic circuits remains relatively small and a greater number of computing elements can be fit into a given area of silicon. This means the machine can perform a greater number of operations per unit of time or per unit power, which gives it an advantage for those computations able to be expressed in the LPHDR framework.

[0035] Another embodiment is to use analog representations and processing mechanisms. Analog implementation of LPHDR arithmetic has the potential to be superior to digital implementation, because it tends to use the natural analog physics of transistors or other physical devices instead of using only the digital subset of the device's behavior. This fuller use of the devices' natural abilities may permit smaller mechanisms for doing LPHDR arithmetic. In recent years, in the field of silicon circuitry, analog methods have been supplanted by digital methods. In part, this is because of the ease of doing digital design compared to analog design. Also in part, it is because of the continued rapid scaling of digital technology ("Moore's Law") compared to analog technology. In particular, at deep submicron dimensions, analog transistors no longer work as they had in prior generations of larger-scale technology. This change of familiar behavior has made analog design still harder in recent years. However, digital transistors are in fact analog

transistors used in a digital way, meaning digital circuits are really analog circuits designed to attempt to switch the transistors between completely on and completely off states. As scaling continues, even this use of transistors is starting to come face to face with the realities of analog behavior. Scaling of transistors for digital use is expected either to stall or to require digital designers increasingly to acknowledge and work with analog issues. For these reasons, digital embodiments may no longer be easy, reliable, and scalable, and analog embodiments of LPHDR arithmetic may come to dominate commercial architectures.

[0036] Because LPHDR processing elements are relatively small, a single processor or other device may include a very large number of LPHDR processing elements, adapted to operate in parallel with each other, and therefore may constitute a massively parallel LPHDR processor or other device. Such a processor or other device has not been described or practiced as a means of doing general purpose computing by those having ordinary skill in the art for at least two reasons. First, it is commonly believed by those having ordinary skill in the art, that LPHDR computation, and in particular massive amounts of LPHDR computation, whether performed in a massively parallel way or not, is not practical as a substrate for moderately general computing. Second, it is commonly believed by those having ordinary skill in the art that massive amounts of even high precision computation on a single chip or in a single machine, as is enabled by a compact arithmetic processing unit, is not useful without a corresponding increase in bandwidth between processing elements within the machine and into and out of the machine

because computing is wire limited and arithmetic can be considered to be available at no cost.

[0037] Despite these views—that massive amounts of arithmetic on a chip or in a massively parallel machine are not useful, and that massive amounts of LPHDR arithmetic are even worse—embodiments of the present invention disclosed herein demonstrate that massively parallel LPHDR designs are in fact useful and provide significant practical benefits in at least several significant applications.

[0038] To conclude, modern digital computing systems provide high precision arithmetic, but that precision is costly. A modern double precision floating point multiplier may require on the order of a million transistors, even though only a handful of transistors is required to perform a low precision multiplication. Despite the common belief among those having ordinary skill in the art that modern applications require high precision processing, in fact a variety of useful algorithms function adequately at much lower precision. As a result, such algorithms may be performed by processors or other devices implemented according to embodiments of the present invention, which come closer to achieving the goal of using a few transistors to multiply and a wire junction to add, thus enabling massively parallel arithmetic computation to be performed with relatively small amounts of physical resources (such as a single silicon chip). Although certain specialized tasks can function at low precision, it is not obvious, and in fact has been viewed as clearly false by those having ordinary skill in the art, that relatively general purpose computing such as is typically performed today on general purpose computers can be done at low

precision. However, in fact a variety of useful and important algorithms can be made to function adequately at much lower than 32 bit precision in a massively parallel computing framework, and certain embodiments of the present invention support such algorithms, thereby offering much more efficient use of transistors, and thereby provide improved speed, power, and/or cost, compared to conventional computers.

[0039] Various computing devices implemented according to embodiments of the present invention will now be described. Some of these embodiments may be an instance of a SIMD computer architecture. Other architectures may be used, such as MIMD architectures, programmable array architectures (such as FPGAs and FPAAs), or GPU/SIMT architectures. The techniques disclosed herein may, for example, be implemented using any processor or other device having such an existing architecture, and replacing or augmenting some or all existing arithmetic units in the processor or other device, if any, with LPHDR arithmetic units in any of the ways disclosed herein. Devices implemented according to embodiments of the present invention, however, need not start with an existing processor design, but instead may be designed from scratch to include LPHDR arithmetic units within any of the architectures just described, or any other architecture.

[0040] Embodiments of the present invention may, for example, be implemented using the architecture of a particular kind of SIMD computer, the array processor. There are many variations and specific instances of array processors described in the scientific and commercial literature. Examples include the Illiac 4, the Connection Machine 1 and 2, the Goodyear MPP, and the MasPar line of

computers.

[0041] Embodiments of the present invention need not, however, be implemented as SIMD computers. For example, embodiments of the present invention may be implemented as FPGAs, FPAAs, or related architectures that provide for flexible connectivity of a set of processing elements. For example, embodiments of the present invention may be implemented as GPU/SIMTs and as MIMDs, among others. For example, embodiments of the present invention may be implemented as any kind of machine which uses LPHDR arithmetic processing elements to provide computing using a small amount of resources (e.g., transistors or volume) compared with traditional architectures. Furthermore, references herein to "processing elements" within embodiments of the present invention should be understood more generally as any kind of execution unit, whether for performing LPHDR operations or otherwise.

[0042] An example SIMD computing system 100 is illustrated in FIG. 1. The computing system 100 includes a collection of many processing elements (PEs). Sometimes present are a control unit (CU) 106, an I/O unit (IOU) 108, various Peripheral devices 110, and a Host computer 102. The collection of PEs is referred to herein as "the Processing Element Array" (PEA), even though it need not be two-dimensional or an array or grid or other particular layout. Some machines include additional components, such as an additional memory system called the "Staging Memory" in the Goodyear MPP, but these additional elements are neither essential in the computer nor needed to understand embodiments of the present invention and therefore are omitted here for clarity of explanation. One embodiment of the present invention is a SIMD computing system of the

kind shown in FIG. 1, in which one or more (e.g., all) of the PEs in the PEA 104 are LPHDR elements, as that term is used herein.

[0043] The Host 102 is responsible for overall control of the computing system 100. It performs the serial, or mostly serial, computation typical of a traditional uni-processor. The Host 102 could have more complicated structure, of course, including parallelism of various sorts. Indeed a heterogeneous computing system combining multiple computing architectures in a single machine is a good use for embodiments of the present invention.

[0044] A goal of the Host 102 is to have the PEA 104 perform massive amounts of computation in a useful way. It does this by causing the PEs to perform computations, typically on data stored locally in each PE, in parallel with one another. If there are many PEs, much work gets done during each unit of time.

[0045] The PEs in the PEA 104 may be able to perform their individual computations roughly as fast as the Host 102 performs its computations. This means it may be inefficient to have the Host 102 attempt to control the PEA 104 on a time scale as fine as the Host's or PEA's minimal time step. (This minimal time, in a traditional digital design, would be the clock period.) For this reason, the specialized control unit (CU) 106 may be included in the architecture. The CU 106 has the primary task of retrieving and decoding instructions from an instruction memory, which conceptually is part of the CU 106, and issuing the partially decoded instructions to all the PEs in the PEA 104. (This may be viewed by the CU software as happening roughly simultaneously for all the PEs, though it need not literally be synchronous, and in fact it may be effective

to use an asynchronous design in which multiple instructions at different stages of completion simultaneously propagate gradually across the PEA, for instance as a series of wave fronts.)

[0046] In a design which includes the CU 106, the Host 102 typically will load the instructions (the program) for the PEA 104 into the CU instruction memory (not shown in FIG. 1), then instruct the CU 106 to interpret the program and cause the PEA 104 to compute according to the instructions. The program may, for example, look generally similar to a typical machine language program, with instructions to cause data movement, logical operations, arithmetic operations, etc., in and between the PEs and other instructions to do similar operations together with control flow operations within the CU 106. Thus, the CU 106 may run a typical sort of program, but with the ability to issue massively parallel instructions to the PEA 104.

[0047] In order to get data into and out of the CU 106 and PEA 104, the I/O Unit 108 may interface the CU 106 and PEA 104 with the Host 102, the Host's memory (not shown in FIG. 1), and the system's Peripherals 110, such as external storage (e.g., disk drives), display devices for visualization of the computational results, and sometimes special high bandwidth input devices (e.g., vision sensors). The PEA's ability to process data far faster than the Host 102 makes it useful for the IOU 108 to be able to completely bypass the Host 102 for some of its data transfers. Also, the Host 102 may have its own ways of communicating with the Peripherals 110.

[0048] The particular embodiment illustrated in FIG. 1 is shown merely for purposes of example and does not constitute a limitation of the present invention. For

example, alternatively the functions performed by the CU 106 could instead be performed by the Host 102 with the CU 106 omitted. The CU 106 could be implemented as hardware distant from the PEA 104 (e.g., off-chip), or the CU 106 could be near to the PEA 104 (e.g., on-chip). I/O could be routed through the CU 106 with the IOU 108 omitted or through the separate I/O unit 108, as shown. Furthermore, the Host 102 is optional; the CU 106 may include, for example, a CPU, or otherwise include components sufficient to replace the functions performed by the Host 102. The Peripherals 110 shown in FIG. 1 are optional. The design shown in FIG. 1 could have a special memory, such as the Goodyear MPP's "staging memory," which provides an intermediate level of local storage. Such memory could, for example, be bonded to the LPHDR chip using 3D fabrication technology to provide relatively fast parallel access to the memory from the PEs in the PEA 104.

[0049] The PEA 104 itself, besides communicating with the CU 106 and IOU 108 and possibly other mechanisms, has ways for data to move within the array. For example, the PEA 104 may be implemented such that data may move from PEs only to their nearest neighbors, that is, there are no long distance transfers. FIGS. 2 and 3 show embodiments of the present invention which use this approach, where the nearest neighbors are the four adjacent PEs toward the North, East, West, and South, called a NEWS design. For example, FIG. 2 shows a subset of the PEs in PEA 104, namely PE 202, PE 204, PE 206, PE 208, and PE 210. When the CU 106 issues data movement instructions, all the PEs access data from or send data to their respective specified nearest neighbor. For instance, every PE might access a specified data value in its neighbor to the West and copy

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it into its own local storage. In some embodiments, such as some analog embodiments, these kinds of transfers may result in some degradation of the value copied.

[0050] FIG. 3 shows a PE 302 that includes data connections to the IOU 108. PE 302 is connected at the North to PE 304, at the East to PE 306, at the South to PE 308, and at the West to PE 310. However, driving signals from inside the PEA 104 out to the IOU 108 usually requires a physically relatively large driving circuit or analogous mechanism. Having those at every PE may absorb much of the available resources of the hardware implementation technology (such as VLSI area). In addition, having independent connections from every PE to the IOU 108 means many such connections, and long connections, which also may absorb much of the available hardware resources. For these reasons, the connections between the PEs and the IOU 108 may be limited to those PEs at the edges of the PE array 104. In this case, to get data out of, and perhaps into, the PEA 104, the data is read and written at the edges of the array and CU instructions are performed to shift data between the edges and interior of the PEA 104. The design may permit data to be pushed from the IOU 108 inward to any PE in the array using direct connections, but may require readout to occur by using the CU 106 to shift data to the edges where it can be read by the IOU 108.

[0051] Connections between the CU 106 and PEA 104 have analogous variations. One design may include the ability to drive instructions into all the PEs roughly simultaneously, but another approach is to have the instructions flow gradually (for instance, shift in discrete time steps) across the PEA 104 to reach the PEs. Some SIMD designs, which may be implemented in embodiments of the present

invention, have a facility by which a "wired-or" or "wired-and" of the state of every PE in the PEA 104 can be read by the CU 106 in approximately one instruction delay time.

[0052] There are many well studied variations on these matters in the literature, any of which may be incorporated into embodiments of the present invention. For example, an interconnect, such as an 8-way local interconnect, may be used. The local connections may include a mixture of various distance hops, such as distance 4 or 16 as well as distance 1. The outside edges may be connected using any topology, such as a torus or twisted torus. Instead of or in addition to a local interconnect, a more complex global interconnect, such as the hypercube design, may be used. Furthermore, the physical implementation of the PEA 104 (e.g., a chip) could be replicated (e.g., tiled on a circuit board) to produce a larger PEA. The replication may form a simple grid or other arrangement, just as the component PEAs may but need not be grids.

[0053] FIG. 4 shows an example design for a PE 400 (which may be used to implement any one or more of the PEs in the PEA 104). The PE 400 stores local data. The amount of memory for the local data varies significantly from design to design. It may depend on the implementation technologies available for fabricating the PE 400. Sometimes rarely changing values (Constants) take less room than frequently changing values (Registers), and a design may provide more Constants than Registers. For instance, this may be the case with digital embodiments that use single transistor cells for the Constants (e.g., floating gate Flash memory cells) and multiple transistor cells for the Registers (e.g., 6-transistor SRAM cells). Sometimes the situation is reversed, as may be the case in analog

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embodiments, where substantial area for capacitance may be needed to ensure stable long term storage of Constants, and such embodiments may have more Registers than Constants. Typical storage capacities might be tens or hundreds of arithmetic values stored in the Registers and Constants in each PE, but these capacities are adjustable by the designer. Some designs, for instance, may have Register storage but no Constant storage. Some designs may have thousands or even many more values stored in each PE. All of these variations may be reflected in embodiments of the present invention.

[0054] Each PE needs to operate on its local data. For this reason within the PE 400 there are data paths 402a-i, routing mechanisms (such as the multiplexor MUX 404), and components to perform some collection of logical and arithmetic operations (such as the logic unit 406 and the LPHDR arithmetic unit 408). The LPHDR arithmetic unit 408 performs LPHDR arithmetic operations, as that term is used herein. The input, output, and intermediate "values" received by, output by, and operated on by the PE 400 may, for example, take the form of electrical signals representing numerical values.

[0055] The PE 400 also may have one or more flag bits, shown as Mask 410 in FIG. 4. The purpose of the Mask 410 is to enable some PEs, the ones in which a specified Mask bit is set, to ignore some instructions issued by the CU 106. This allows some variation in the usual lock-step behaviors of all PEs in the PEA 104. For instance, the CU 106 may issue an instruction that causes each PE to reset or set its Mask 410 depending on whether a specified Register in the PE is positive or negative. A subsequent instruction, for instance an arithmetic instruction, may include a bit

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meaning that the instruction should be performed only by those PEs whose Mask 410 is reset. This combination has the effect of conditionally performing the arithmetic instruction in each PE depending on whether the specified Register in that PE was positive. As with the Compare instructions of traditional computers, there are many possible design choices for mechanisms to set and clear Masks.

[0056] The operation of the PEs is controlled by control signals 412a-d received from the CU 106, four of which are shown in FIG. 4 merely for purposes of example and not limitation. We have not shown details of this mechanism, but the control signals 412a-d specify which Register or Constant memory values in the PE 400 or one of its neighbors to send to the data paths, which operations should be performed by the Logic unit 406 or LPHDR Arithmetic Unit 408 or other processing mechanisms, where the results should be stored in the Registers, how to set, reset, and use the Mask 410, and so on. These matters are well described in the literature on SIMD processors.

[0057] Many variations of this PE 400 and PEA design are possible and fall within the scope of the present invention. Digital PEs can have shifters, lookup tables, and many other mechanisms such as described in the literature. Analog PEs can have time-based operators, filters, comparators with global broadcast signals and many other mechanisms such as described in the literature. The PEA 104 can include global mechanisms such as wired-OR or wired-AND for digital PEAs or wired-SUM for analog PEAs. Again, there are many variations well described in the literature on digital and analog computing architectures.

[0058] For example, LPHDR operations other than and/or

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in addition to addition and multiplication may be supported. For example, a machine which can only perform multiplication and the function (1-X) may be used to approximate addition and other arithmetic operations. Other collections of LPHDR operations may be used to approximate LPHDR arithmetic operations, such as addition, multiplication, subtraction, and division, using techniques that are well-known to those having ordinary skill in the art.

[0059] One aspect of embodiments of the present invention that is unique is the inclusion of LPHDR arithmetic mechanisms in the PEs. Embodiments of such mechanisms will now be described.

[0060] One digital embodiment of the LPHDR arithmetic unit 408 operates on digital (binary) representations of numbers. In one digital embodiment these numbers are represented by their logarithms. Such a representation is called a Logarithmic Number System (LNS), which is well-understood by those having ordinary skill in the art.

[0061] In an LNS, numbers are represented as a sign and an exponent. There is an implicit base for the logarithms, typically 2 when working with digital hardware. In the present embodiment, a base of 2 is used for purposes of example. As a result, a value, say B, is represented by its sign and a base 2 logarithm, say b, of its absolute value. For numbers to have representation errors of at most, say, 1% (one percent), the fractional part of this logarithm should be represented with enough precision that the least possible change in the fraction corresponds to about a 1% change in the value B. If fractions are represented using 6 bits, increasing or decreasing the fraction by 1 corresponds to multiplying or dividing B by

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the 64th root of 2, which is approximately 1.011. This means that numbers may be represented in the present embodiment with a multiplicative error of approximately 1%. So, in this example embodiment the fraction part of the representation has 6 bits.

[0062] Furthermore, the space of values processed in the present embodiment have high dynamic range. To represent numbers whose absolute value is from, say, one billionth to one billion, the integer part of the logarithm must be long enough to represent plus or minus the base 2 logarithm of one billion. That logarithm is about 29.9. In the present embodiment the integer part of the logarithm representation is 5 bits long to represent values from 0 to 31, which is sufficient. There also is a sign bit in the exponent. Negative logarithms are represented using two's complement representation.

[0063] In an LNS, the value zero corresponds to the logarithm negative infinity. One can choose a representation to explicitly represent this special value. However, to minimize resources (for instance, area) used by arithmetic circuits, the present embodiment represents zero by the most negative possible logarithm, which is -32, corresponding to the two's complement bit representation '100000 000000', and denoting a value of approximately 2.33E-10.

[0064] When computing, situations can arise in which operations cannot produce reasonable values. An example is when a number is too large to be represented in the chosen word format, such as when multiplying or adding two large numbers or upon divide by zero (or nearly zero). One common approach to this problem is to allow a value to be marked as Not A Number (NAN) and to make sure that each operation

produces NAN if a problem arises or if either of its inputs is NAN. The present embodiment uses this approach, as will be described in the following.

[0065] FIG. 5 shows the word format 500 for these numbers, in the present embodiment. It has one NAN bit 502a, one bit 502b for the sign of the value, and 12 bits 502c-e representing the logarithm. The logarithm bits include a 5 bit integer part 502d and a 6 bit fraction part 502e. To permit the logarithms to be negative, there is a sign bit 502c for the logarithm which is represented in two's complement form. The NAN bit is set if some problem has arisen in computing the value. The word format 500 shown in FIG. 5 is merely an example and does not constitute a limitation of the present invention. Other variations may be used, so long as they have low precision and high dynamic range.

[0066] FIG. 6 shows an example digital implementation of the LPHDR arithmetic unit 408 for the representation illustrated in FIG. 5. The unit 408 receives two inputs, A 602a and B 602b, and produces an output 602c. The inputs 602a-b and output 602c may, for example, take the form of electrical signals representing numerical values according to the representation illustrated in FIG. 5, as is also true of signals transmitted within the unit 408 by components of the unit 408. The inputs 602a-b and output 602c each are composed of a Value and a NAN (Not A Number) bit. The unit 408 is controlled by control signals 412a-d, coming from the CU 106, that determine which available arithmetic operation will be performed on the inputs 602a-b. In this embodiment, all the available arithmetic operations are performed in parallel on the inputs 602a-b by adder/subtractor 604, multiplier 606, and divider 608.

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Adder/subtractor 604 performs LPHDR addition and subtraction, multiplier 606 performs LPHDR multiplication, and divider 608 performs LPHDR division.

[0067] The desired result (from among the outputs of adder/subtractor 604, multiplier 606, and divider 608) is chosen by the multiplexers (MUXes) 610a and 610b. The right hand MUX 610b sends the desired value to the output 602c. The left hand MUX 610a sends the corresponding NAN bit from the desired operation to the OR gate 612, which outputs a set NAN bit if either input is NAN or if the specified arithmetic operation yields NAN. The computing architecture literature discusses many variations which may be incorporated into the embodiment illustrated in FIG. 6.

[0068] LNS arithmetic has the great advantage that multiplication (MUL) and division (DIV) are very easy to compute and take few physical resources (e.g., little area in a silicon implementation). The sign of the result is the exclusive-or of the signs of the operands. The logarithm part of the output is the sum, in the case of MUL, or the difference, in the case of DIV, of the logarithm parts of the operands. The sum or difference of the logarithms can overflow, producing a NAN result. Certain other operations also are easy in LNS arithmetic. For instance, square root corresponds to dividing the logarithm in half, which in our representation means simply shifting it one bit position to the right.

[0069] Thus, the multiplier 606 and divider 608 in FIG. 6 are implemented as circuits that simply add or subtract their inputs, which are two's complement binary numbers (which in turn happen to be logarithms). If there is overflow, they output a 1 for NAN.

[0070] Implementing addition and subtraction in LNS,

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that is, the adder/subtractor 604 in FIG. 6, follows a common approach used in the literature on LNS. Consider addition. If we have two positive numbers B and C represented by their logarithms b and c, the representation of the sum of B and C is log(B+C). An approach to computing this result that is well known to those skilled in the art is based on noticing that log(B+C) = log(B*(1+C/B)) = log(B)+log(1+C/B) = b+F(c-b) where F(x)=log(1+2^x). Thus, the present embodiment computes c-b, feeds that through F, and adds the result to b, using standard digital techniques known to those skilled in the art.

[0071] Much of the published literature about LNS is concerned with how to compute F(x), the special function for ADD, along with a similar function for SUB. Often these two functions share circuitry, and this is why a single combined adder/subtractor 604 is used in the embodiment of FIG. 6. There are many published ways to compute these functions or approximations to them, including discussions of how to do this when the values are of low precision. Any such method, or other method, may be used. Generally speaking, the more appropriate variations for massively parallel LPHDR arithmetic are those that require the minimal use of resources, such as circuit area, taking advantage of the fact that the representation used in the embodiment of FIG. 6 is low precision and that the arithmetic operations need not be deterministic nor return the most accurate possible answer within the low precision representation. Thus, embodiments of the present invention may use circuitry that does not compute the best possible answer, even among the limited choices available in a low precision representation.

[0072] In order to enable conditional operation of

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selected PEs, the present embodiment is able to reset and set the MASK flag 410 based on results of computations. The mechanism for doing this is that the CU 106 includes instructions that cause the MASK 410 in each PE to unconditionally reset or set its flag along with other instructions to perform basic tests on values entering the MASK 410 on data path 402f and to set the flag accordingly. Examples of these latter instructions include copying the sign bit or NAN bit of the word on data path 402f into the MASK bit 410. Another example is to set the MASK bit 410 if the 12 bit value part of the word on data path 402f is equal to binary zero. There are many additional and alternative ways for doing this that are directly analogous to comparison instructions in traditional processors and which are well understood by those skilled in the art.

[0073] It is worth noting that while the obvious method of using the above LNS operations is to do LPHDR arithmetic, the programmer also may consider selected values to be 12 bit two's complement binary numbers. MUL and DIV may be used to add and subtract such values, since that is precisely their behavior in LNS implementations. The Mask setting instructions can compare these simple binary values. So besides doing LPHDR computations, this digital embodiment using LNS can perform simple binary arithmetic on short signed integers.

[0074] Some embodiments of the present invention may include analog representations and processing methods. Such embodiments may, for example, represent LPHDR values as charges, currents, voltages, frequencies, pulse widths, pulse densities, various forms of spikes, or in other forms not characteristic of traditional digital implementations. There are many such representations discussed in the

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literature, along with mechanisms for processing values so represented. Such methods, often called Analog methods, can be used to perform LPHDR arithmetic in the broad range of architectures we have discussed, of which SIMD is one example.

[0075] An example of an analog SIMD architecture is the SCAMP design (and related designs) of Dudek. In that design values have low dynamic range, being accurate roughly to within 1%. Values are represented by charges on capacitors. Those capacitors typically are the gates of transistors. Each PE has several memory cells, analogous to the Registers shown in FIG. 4. Addition is performed by turning on pass transistors from the two operands, which transfer their charge onto an analog bus, where it is summed by the natural physics of charge and wires, upon which it is gated onto another Register to charge up its capacitor, which then represents the sum of the operands. The detailed mechanism disclosed by Dudek actually produces the negative of the sum, but the basic concept is as described and is a simple way to perform addition and subtraction using analog representations and simple processing mechanisms.

[0076] Variations of the SCAMP design have been fabricated and used to perform a range of low precision, low dynamic range computations related to image processing. These designs do not perform high dynamic range arithmetic, nor do they include mechanisms for performing multiplication or division of values stored in Registers. However, the Dudek designs suggest the general feasibility of constructing analog SIMD machines. The following describes how to build an analog SIMD machine that performs LPHDR arithmetic, and is thus an embodiment of the present

invention.

[0077] One embodiment of the present invention represents values as a mixture of analog and digital forms. This embodiment represents values as low precision, normalized, base 2 floating point numbers, where the mantissa is an analog value and the exponent is a binary digital value. The analog value may be accurate to about 1%, following the approach of Dudek, which is well within the range of reasonable analog processing techniques. The exponent may be 6 bits long, or whatever is needed to provide the desired high dynamic range.

[0078] To multiply values, the embodiment proceeds by analogy to traditional floating point methods. The digital exponents are summed using a binary arithmetic adder, a standard digital technique. The analog mantissas are multiplied. Since they represent normalized values between approximately 1/2 and 1, their product may be as small as approximately 1/4. Such a product value needs to be normalized back to the range 1/2 to 1. This is done, in the present embodiment, by comparing the analog mantissa to an analog representation of 1/2, using a threshold circuit. If the mantissa is below 1/2, then it is doubled and one is subtracted from the exponent, where such subtraction is simple digital subtraction. Doubling the mantissa is implemented in a way that corresponds to the chosen analog representation. For example, whatever means are being used to add two analog values can be used to double the mantissa, by adding it to a copy of itself. For example, if the mantissa is represented as a current, such as copy may be produced by a current mirror, or other suitable mechanism, and addition may be performed by a current summing junction.

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[0079] The means of multiplying the original analog mantissas depends on the representation chosen. For example, if mantissas are represented using charge, following SCAMP, then any known method from the literature may be used to convert charge to current. For instance, since the charge on a capacitor determines the voltage on the capacitor, this may be implemented as a conversion from voltage to current, which is a basic technique in analog electronics known to those skilled in the art. In any case, if the mantissas are represented as currents, or once the mantissas are converted to currents, they may be multiplied using, for instance, the techniques of Gilbert. The Gilbert multiplier produces a current, representing the product, which may, if necessary, then be converted back to charge (or whatever representation is used). These are merely examples of how the needed operations might be performed. The literature discusses these matters extensively and these kinds of analog circuits are known to those skilled in the art.

[0080] Adding and subtracting values requires pre-normalization of the values to the same exponent, as is done in traditional digital floating point arithmetic. The present embodiment does this by comparing the exponents and choosing the smaller one. Then the smaller one is subtracted from the larger, using digital means. The difference specifies how many times the mantissa which corresponds to the smaller exponent needs to be divided in half. If that mantissa is represented by (or converted to) a current, then an analog R-2R style ladder may be used to divide the current in half the required number of times, with the stage of the ladder specified by the difference of exponents calculated as above. The resulting scaled down

current is added to (or subtracted from, if this is an LPHDR subtraction operation) the current corresponding to the mantissa associated with the larger exponent to yield the output mantissa. The output exponent associated with the output mantissa is the larger exponent. Post-normalization may be needed at this point. If the output mantissa is greater than 1, then it needs to be divided in half and the output exponent needs to be incremented. If it is less than 1/2, then it needs to be doubled enough times to exceed 1/2 and the output exponent must be decremented correspondingly, which may be performed by a series of threshold circuits, doubler circuits, and associated decrementer circuits. These increments and decrements of the binary digital exponent, and corresponding doublings and halvings of the analog mantissa current, are straightforward operations well known to those skilled in the art.

[0081] The present embodiment represents the exponent as a digital binary number. Alternate embodiments may represent the exponent as an analog value. However, it is important that the exponent be represented in storage and computation in such a manner that neither noise nor other errors cause a change in the value it represents. Such changes in the exponent could introduce factors of two (or in some embodiments larger) changes in the values of the stored numbers. To maintain accuracy of the exponents, an embodiment may quantize the exponent to relatively few levels, for instance 16 values plus a sign bit. During processing, slight variations in the analog representation of the exponent may then be removed by circuitry that restores values to the 16 standard quantization levels. To get sufficient dynamic range in such an embodiment, the

floating point numbers may be processed as base 4 numbers, rather than the usual base 2 numbers. This means, for instance, that normalized mantissas are in the range 1/4 to 1. The methods discussed above for addition, subtraction, and multiplication apply as described, with slight and straightforward variations.

[0082] The analog and mixed signal embodiments discussed above are merely examples and do not constitute a limitation of the present invention. The published literature on neuromorphic, analog, and mixed signal techniques provides a wealth of methods that enable LPHDR storage and processing to be implemented. Such storage and processing may introduce noise as well as fabrication errors into the behavior of machines performing LPHDR arithmetic. The results we present below, on software applications running using "fp+noise" arithmetic, show that despite these very "un-digital" qualities a machine built in this way is surprisingly useful.

[0083] Evidence that LPHDR arithmetic is useful in several important practical computing applications will now be provided. The evidence is presented for a broad variety of embodiments of the present invention, thereby showing that the usefulness does not depend much on the detailed implementation.

[0084] For the goal of showing usefulness, we choose a very general embodiment of an LPHDR machine. Our model of the machine is that it provides at least the following capabilities: (1) is massively parallel, (2) provides LPHDR arithmetic possibly with noise, (3) provides a small amount of memory local to each arithmetic unit, (4) provides the arithmetic/memory units in a two-dimensional physical layout with only local connections between units (rather

than some more powerful, flexible, or sophisticated connection mechanism), and (5) provides only limited bandwidth between the machine and the host machine. Note that this model is merely an example which is used for the purpose of demonstrating the utility of various embodiments of the present invention, and does not constitute a limitation of the present invention. This model includes, among others, implementations that are digital or analog or mixed, have zero or more noise, have architectures which are FPGA-like, or SIMD-like, or MIMD-like, or otherwise meet the assumptions of the model. More general architectures, such as shared memory designs, GPU-like designs, or other sophisticated designs subsume this model's capabilities, and so LPHDR arithmetic in those architectures also is useful. While we are thus showing that LPHDR arithmetic is useful for a broad range of designs, of which SIMD is only an instance, for purpose of discussion below, we call each unit, which pairs memory with arithmetic, a Processing Element or "PE".

[0085] Several applications are discussed below. For each, the discussion shows (1) that the results are useful when computation is performed in possibly noisy LPHDR arithmetic, and (2) that the computation can be physically laid out in two dimensions with only local flow of data between units, only limited memory within each unit, and only limited data flow to/from the host machine, in such a way that the computation makes efficient use of the machine's resources (area, time, power). The first requirement is referred to as "Accuracy" and the second requirement "Efficiency." Applications that meet both requirements running in this model will function well on many kinds of LPHDR machines, and thus those machines are a

broadly useful invention.

[0086] Applications are tested using two embodiments for the machine's arithmetic. One uses accurate floating point arithmetic but multiplies the result of each arithmetic operation by a uniformly chosen random number between .99 and 1.01. In the following discussion, this embodiment is denoted "fp+noise". It may represent the results produced by an analog embodiment of the machine.

[0087] A second embodiment uses logarithmic arithmetic with a value representation as shown in FIG. 5. The arithmetic is repeatable, that is, not noisy, but because of the short fraction size it produces errors of up to approximately 1-2% in each operation. In the following discussion, this embodiment is denoted "lns". It may represent the results produced by a particular digital embodiment of the machine.

[0088] To demonstrate usefulness of embodiments of the invention, we shall discuss three computational tasks that are enabled by embodiments of the invention and which in turn enable a variety of practical applications. Two of the tasks are related to finding nearest neighbors and the other is related to processing visual information. We shall describe the tasks, note their practical application, and then demonstrate that each task is solvable using the general model described above and thus solvable using embodiments of the present invention.

Application 1: Finding Nearest Neighbors

[0089] Given a large set of vectors, called Examples, and a given vector, called Test, the nearest neighbor problem ("NN") is to find the Example which is closest to Test where the distance metric is the square of the Euclidean distance (sum of squares of distances between

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respective components).

[0090] NN is a widely useful computation. One use is for data compression, where it is called "vector quantization". In this application we have a set of relatively long vectors in a "code book" (these are the Examples) and associated short code words (for instance the index of the vector in the code book). We move through a sequence of vectors to be compressed, and for each such vector (Test), find the nearest vector in the code book and output the corresponding code word. This reduces the sequence of vectors to the shorter sequence of code words. Because the code words do not completely specify the original sequence of vectors, this is a lossy form of data compression. Among other applications, it may be used in speech compression and in the MPEG standards.

[0091] Another application of NN would be in determining whether snippets of video occur in a large video database. Here we might abstract frames of video from the snippet into feature vectors, using known methods, such as color histograms, scale invariant feature extraction, etc. The Examples would be analogous feature vectors extracted from the video database. We would like to know whether any vector from the snippet was close to any vector from the database, which NN can help us decide.

[0092] In many applications of nearest neighbor, we would prefer to find the true nearest neighbor but it is acceptable if we sometimes find another neighbor that is only slightly farther away or if we almost always find the true nearest neighbor. Thus, an approximate solution to the nearest neighbor problem is useful, especially if it can be computed especially quickly, or at low power, or with some other advantage compared to an exact solution.

[0093] We shall now show that approximate nearest neighbor is computable using embodiments of the present invention in a way that meets the criteria of Accuracy and Efficiency.

[0094] Algorithm. The following describes an algorithm which may be performed by machines implemented according to embodiments of the present invention, such as by executing software including instructions for performing the algorithm. The inputs to the algorithm are a set of Examples and a Test vector. The algorithm seeks to find the nearest (or almost nearest) Example to the Test.

[0095] In the simplest version of the algorithm, the number of Examples may be no larger than the number of PEs and each vector must be short enough to fit within a single PE's memory. The Examples are placed into the memories associated with the PEs, so that one Example is placed in each PE. Given a Test, the Test is passed through all the PEs, in turn. Accompanying the Test as it passes through the PEs is the distance from the Test to the nearest Example found so far, along with information that indicates what PE (and thus what Example) yielded that nearest Example found so far. Each PE computes the distance between the Test and the Example stored in that PE's memory, and then passes along the Test together with either the distance and indicator that was passed into this PE (if the distance computed by this PE exceeded the distance passed into the PE) or the distance this PE computed along with information indicating this PE's Example is the nearest so far (if the distance computed by this PE is less than the distance passed into the PE). Thus, the algorithm is doing a simple minimization operation as the Test is passed through the set of PEs. When the Test and associated

information leave the last PE, the output is a representation of which PE (and Example) was closest to the Test, along with the distance between that Example and the Test.

[0096] In a more efficient variant of this algorithm, the Test is first passed along, for example, the top row, then every column passes the Test and associated information downward, effectively doing a search in parallel with other columns, and once the information reaches the bottom it passes across the bottom row computing a minimum distance Example of all the columns processed so far as it passes across the row. This means that the time required to process the Test is proportional to (the greater of) the number of PEs in a row or column.

[0097] An enhancement of this algorithm proceeds as above but computes and passes along information indicating both the nearest and the second nearest Example found so far. When this information exits the array of PEs, the digital processor that is hosting the PE array computes (in high precision) the distance between the Test and the two Examples indicated by the PE array, and the nearer of the two is output as the likely nearest neighbor to the Test.

[0098] Accuracy. We expressed the arithmetic performed by the enhanced algorithm described above as code in the C programming language. That code computes both nearest neighbors, which are discussed here, along with weighted scores, which are discussed below.

[0099] The C code performs the same set of arithmetic operations in the same order using the same methods of performing arithmetic as an actual implementation of the present invention, such as one implemented in hardware. It thus yields the same results as the enhanced algorithm

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would yield when running on an implementation of the present invention. (How the algorithm is organized to run efficiently on such an implementation is discussed below in the section on Efficiency.)

[00100] In particular, when computing the distance between the Test and each Example, the code uses Kahan's method, discussed below, to perform the possibly long summation required to form the sum of the squares of the distances between vector components of the Test and Example.

[00101] The C code contains several implementations for arithmetic, as discussed above. When compiled with "#define fp" the arithmetic is done using IEEE standard floating point. If a command line argument is passed in to enable noisy arithmetic, then random noise is added to the result of every calculation. This is the "fp+noise" form of arithmetic. When compiled without "#define fp" the arithmetic is done using low precision logarithmic arithmetic with a 6 bit base-2 fraction. This is the "lns" form of arithmetic.

[00102] When the code was run it produced traces showing the results of the computations it performed. These traces, shown below, show that with certain command line arguments the enhanced algorithm yielded certain results for LPHDR nearest neighbor calculations. These results provide details showing the usefulness of this approach. We shall discuss the results briefly here.

[00103] The first results are for "fp+noise". Ten distinct runs were performed. Each run generated one million random Example vectors of length five, where each component of each vector was drawn from N(0,1)—the Gaussian (normal) distribution with mean zero and standard deviation

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1. Each run then generated one hundred Test vectors of length five, where each component of each vector also was drawn from N(0,1). For each Test, the nearest neighbor was computed both according to the enhanced algorithm above and according to the standard nearest neighbor method using high precision floating point arithmetic. A count was kept of the number of times the enhanced algorithm yielded the same result as the standard floating point method. The results were as follows:

```
% ./a.out 5 10 1000000 100 1
Representation is Floating Point with noise.
Run 1. On 100 tests, 100(100.0%) matches and 0.81%
mean score error.
Run 2. On 100 tests, 100(100.0%) matches and 0.84%
mean score error.
Run 3. On 100 tests, 100(100.0%) matches and 0.98%
mean score error.
Run 4. On 100 tests, 100(100.0%) matches and 0.81%
mean score error.
Run 5. On 100 tests, 100(100.0%) matches and 0.94%
mean score error.
Run 6. On 100 tests, 100(100.0%) matches and 0.82%
mean score error.
Run 7. On 100 tests, 100(100.0%) matches and 0.78%
mean score error.
Run 8. On 100 tests, 100(100.0%) matches and 0.86%
mean score error.
Run 9. On 100 tests, 100(100.0%) matches and 0.85%
mean score error.
Run 10. On 100 tests, 99(99.0%) matches and 0.86% mean
score error.
```


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Average percentage of time LPHDR (with final DP correction) finds nearest example = 99.90%.
Average score error between LPHDR and DP = 0.85%.

[00104] The "mean score error" values are considered below in the discussion of weighted scores. The "matches" information is relevant here.

[00105] Of the ten runs, only one had any test, of the 100 tests performed, which yielded a nearest neighbor different from what the usual high precision method yielded. Thus, the average percentage of matches between the enhanced algorithm running with "fp+noise" arithmetic and the usual method was 99.9%.

[00106] A similar computation was then performed using "lns" arithmetic. In this case, the results were:

```
% ./a.out 5 10 1000000 100 0
Representation is LNS without noise.
Run 1. On 100 tests, 100(100.0%) matches and 0.15%
mean score error.
Run 2. On 100 tests, 100(100.0%) matches and 0.07%
mean score error.
Run 3. On 100 tests, 100(100.0%) matches and 0.08%
mean score error.
Run 4. On 100 tests, 100(100.0%) matches and 0.09%
mean score error.
Run 5. On 100 tests, 100(100.0%) matches and 0.11%
mean score error.
Run 6. On 100 tests, 100(100.0%) matches and 0.16%
mean score error.
Run 7. On 100 tests, 100(100.0%) matches and 0.07%
mean score error.
```


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Run 8. On 100 tests, 100(100.0%) matches and 0.13% mean score error.
Run 9. On 100 tests, 99(99.0%) matches and 0.17% mean score error.
Run 10. On 100 tests, 98(98.0%) matches and 0.16% mean score error.
Average percentage of time LPHDR (with final DP correction) finds nearest example = 99.70%.
Average score error between LPHDR and DP = 0.12%.

[00107] The average percentage of matches was 99.7%, slightly worse than for "fp+noise".

[00108] The accuracy shown by the enhanced nearest neighbor algorithm using two forms of LPHDR arithmetic is surprising. To perform many calculations sequentially with 1% error and yet produce a final result with less than 1% error may seem counter-intuitive. Nonetheless, the LPHDR arithmetic proves effective, and the accuracy shown is high enough to be useful in applications for which approximate nearest neighbor calculations are useful.

[00109] As an extreme case, a variant of fp+noise was tested in which the noise varied uniformly from +10% to -5%. Thus, each arithmetic operation produced a result that was between 10% too large and 5% too small. The enhanced nearest neighbor algorithm, as described above, was performed where each run generated 100,000 Example vectors. The surprising results, below, show that even with this extreme level of imprecise, noisy, and non-zero mean LPHDR arithmetic, useful results can be achieved.

Run 1. On 100 tests, 97(97.0%) matches.
Run 2. On 100 tests, 100(100.0%) matches.

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Run 3. On 100 tests, 100(100.0%) matches.
Run 4. On 100 tests, 98(98.0%) matches.
Run 5. On 100 tests, 98(98.0%) matches.
Run 6. On 100 tests, 99(99.0%) matches.
Run 7. On 100 tests, 99(99.0%) matches.
Run 8. On 100 tests, 99(99.0%) matches.
Run 9. On 100 tests, 99(99.0%) matches.
Run 10. On 100 tests, 99(99.0%) matches.
Average percentage of time LPHDR (with final DP correction) finds nearest example = 98.80%.

[00110] Efficiency. In contrast to the surprising Accuracy results, it is clear to those having ordinary skill in the art that the calculations of the enhanced nearest neighbor algorithm can be performed efficiently in the computing model presented, where the arithmetic/memory units are connected in a two-dimensional physical layout, using only local communication between PEs. However, this does not address the matter of keeping the machine busy doing useful work using only low bandwidth to the host machine.

[00111] When computing the nearest neighbor to a single Test, the Test flows across all the PEs in the array. As discussed above, if the array is an MxM grid, it takes at least O(M) steps for the Test to pass through the machine and return results to the host. During this time the machine performs O(MxM) nearest neighbor distance computations, but since the machine is capable of performing O(MxM) calculations at each step, a factor of O(M) is lost.

[00112] This speedup, compared to a serial machine, of a factor of O(M) is significant and useful. However, the

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efficiency can be even higher. If sufficiently many Test vectors, say O(M), or more, are to be processed then they can be streamed into the machine and made to flow through in a pipelined fashion. The time to process O(M) Tests remains O(M), the same as for a single Test, but now the machine performs O(M) x O(MxM) distance computations, and thus within a constant factor the full computing capacity of the machine is used.

[00113] Thus, the machine is especially efficient if it is processing at least as many Test vectors as the square root of the number of PEs. There are applications that fit well into this form, such as pattern recognition or compression of many independent Tests (e.g., blocks of an image, parts of a file, price histories of independent stocks) as well as the problem of finding the nearest neighbor to every Example in the set of Examples. This is in contrast to the general view among those having ordinary skill in the art, as discussed above, that machines with very many arithmetic processing elements on a single chip, or similar, are not very useful.

Application 2: Distance Weighted Scoring

[00114] A task related to Nearest Neighbor is Distance Weighted Scoring. In this task, each Example has an associated Score. This is a number that in some way characterizes the Example. For instance, if the Examples are abstractions of the history of prices of a given stock, the Scores might be historical probabilities of whether the price is about to increase or decrease. Given a Test vector, the task is to form a weighted sum of the Scores of all the Examples, where the weights are a diminishing function of the distance from the Test to the respective Examples. For example, this weighted score might be taken

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as a prediction of the future price of the stock whose history is represented by the Test. This use of embodiments of the invention might help support, for instance, high speed trading of stocks, as is performed by certain "quantitative" hedge funds, despite the general view by those having ordinary skill in the art that low precision computation is not of use in financial applications.

[00115] The C code described above computes weighted scores along with nearest neighbors. The scores assigned to Examples in this computation are random numbers drawn uniformly from the range [0,1]. The weight for each Example in this computation is defined to be the un-normalized weight for the Example divided by the sum of the un-normalized weights for all Examples, where the un-normalized weight for each Example is defined to be the reciprocal of the sum of one plus the squared distance from the Example to the Test vector. As discussed above, the code performs a number of runs, each producing many Examples and Tests, and compares results of traditional floating point computations with results calculated using fp+noise and lns arithmetic.

[00116] Looking again at the trace results of running the simulation, above, we see that for fp+noise the LPHDR weighted scores on average were within .85% of the correct value and never were as much as 1% different. For lns arithmetic the errors were even smaller, averaging just .12% error.

[00117] These results are surprising given that computing an overall weighted score involves summing the individual weighted scores associated with each Example. Since each run was processing 1,000,000 Examples, this means that the sums were over one million small positive

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values. The naive method of summing one million small values with errors of about 1% in each addition should yield results that approximate noise. However, the code performs its sums using a long known method invented by Kahan (Kahan, William (January 1965), "Further remarks on reducing truncation errors", Communications of the ACM 8 (1): 40). The method makes it feasible to perform long sums, such as are done for Distance Weighted Scores, or as might be used in computational finance when computing prices of derivative securities using Monte Carlo methods, or for performing deconvolution in image processing algorithms, as will be discussed next.

[00118] The Efficiency of this algorithm is similar to that of NN, as discussed earlier. If many Test vectors are processed at once, the machine performs especially efficiently.

Application 3: Removing motion blur in images

[00119] In order to gather sufficient light to form an image, camera shutters are often left open for long enough that camera motion can cause blurring. This can happen as a result of camera shake in inexpensive consumer cameras as well as with very expensive but fast moving cameras mounted on satellites or aircraft. If the motion path of the camera is known (or can be computed) then the blur can be substantially removed using various deblurring algorithms. One such algorithm is the Richardson-Lucy method ("RL"), and we show here that embodiments of the present invention can run that algorithm and produce useful results. Following the discussion format above, we discuss criteria of Accuracy and Efficiency.

[00120] Algorithm. The Richardson-Lucy algorithm is well known and widely available. Assume that an image has

been blurred using a known kernel. In particular, assume that the kernel is a straight line and that the image has been oriented so that the blur has occurred purely in a horizontal direction. Consider the particular kernel for which the J'th pixel in each row of the blurred image is the uniformly weighted mean of pixels J through J+31 in the original unblurred image.

[00121] Accuracy. We implemented in the C programming language a straightforward version of the RL method that uses LPHDR arithmetic. The program reads a test image, blurs it using the kernel discussed above, then deblurs it using either fp+noise or lns arithmetic. The RL algorithm computes sums, such as when convolving the kernel with the current approximation of the deblurred image. Our implementation computes these sums using the Kahan method, discussed earlier. FIG. 7 shows the test image in original form. It is a satellite picture of a building used during Barack Obama's inauguration. FIG. 8 shows the image extremely blurred by the kernel. It is difficult to see any particular objects in this image. FIG. 9 shows the result of deblurring using standard floating point arithmetic. FIG. 10 shows the result of deblurring using fp+noise arithmetic, and FIG.11 shows the result of deblurring using lns arithmetic. In all these cases the image is sufficiently restored that it is possible to recognize buildings, streets, parking lots, and cars.

[00122] In addition to displaying the images herein for judgement using the human eye, we computed a numerical measure of deblurring performance. We computed the mean difference, over all pixels in the image, between each original pixel value (a gray scale value from 0 to 255) and the corresponding value in the image reconstructed by the

RL method. Those numerical measures are shown below in Table 1:

Image type	Mean pixel error
Blurred	32.0
RL using standard floating point	13.0
RL using fp+noise	13.8
RL using lns	14.8

Table 1

[00123] These results, together with the subjective but important judgements made by the human eye, show that LPHDR arithmetic provides a substantial and useful degree of deblurring compared to standard floating point arithmetic. Further, in this example we chose an extreme degree of blurring, to better convey the concept and visual impact of the deblurring using LPHDR arithmetic. On more gentle and typical blur kernels, the resulting deblurred images are much closer to the originals than in this case, as can be seen by shrinking the kernel length and running the RL algorithm with LPHDR arithmetic on those more typical cases.

[00124] Efficiency. It is clear to those with ordinary skill in the art that Richardson-Lucy using a local kernel performs only local computational operations. An image to be deblurred can be loaded into the PE array, storing one or more pixels per PE, the deconvolution operation of RL can then be iterated dozens or hundreds of times, and the deblurred image can be read back to the host processor. As long as sufficient iterations are performed, this makes efficient use of the machine.

[00125] An extreme form of image deblurring is the Iterative Reconstruction method used in computational

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tomography. Reconstructing 3D volumes from 2D projections is an extremely computational task. The method discussed above generalizes naturally to Iterative Reconstruction and makes efficient use of the machine.

[00126] Among the advantages of embodiments of the invention are one or more of the following.

[00127] PEs implemented according to certain embodiments of the present invention may be relatively small for PEs that can do arithmetic. This means that there are many PEs per unit of resource (e.g., transistor, area, volume), which in turn means that there is a large amount of arithmetic computational power per unit of resource. This enables larger problems to be solved with a given amount of resource than does traditional computer designs. For instance, a digital embodiment of the present invention built as a large silicon chip fabricated with current state of the art technology might perform tens of thousand of arithmetic operations per cycle, as opposed to hundreds in a conventional GPU or a handful in a conventional multicore CPU. These ratios reflect an architectural advantage of embodiments of the present invention that should persist as fabrication technology continues to improve, even as we reach nanotechnology or other implementations for digital and analog computing.

[00128] Doing arithmetic with few resources generally means, and in the embodiments shown specifically means, that the arithmetic is done using low power. As a result, a machine implemented in accordance with embodiments of the present invention can have extremely high performance with reasonable power (for instance in the tens of watts) or low power (for instance a fraction of a watt) with reasonably high performance. This means that such embodiments may be

suitable for the full range of computing, from supercomputers, through desktops, down to mobile computing. Similarly, and since cost is generally associated with the amount of available resources, embodiments of the present invention may provide a relatively high amount of computing power per unit of cost compared to conventional computing devices.

[00129] The SIMD architecture is rather old and is frequently discarded as an approach to computer design by those having ordinary skill in the art. However, if the processing elements of a SIMD machine can be made particularly small while retaining important functionality, such as general arithmetic ability, the architecture can be useful. The embodiments presented herein have precisely those qualities.

[00130] The discovery that massive amounts of LPHDR arithmetic is useful as a fairly general computing framework, as opposed to the common belief that it is not useful, can be an advantage in any (massively or non-massively) parallel machine design or non-parallel design, not just in SIMD embodiments. It could be used in FPGAs, FPAAs, GPU/SIMT machines, MIMD machines, and in any kind of machine that uses compact arithmetic processing elements to perform large amounts of computation using a small amount of resources (like transistors or volume).

[00131] Another advantage of embodiments of the present invention is that they are not merely useful for performing computations efficiently in general, but that they can be used to tackle a variety of real-world problems which are typically assumed to require high-precision computing elements, even though such embodiments include only (or predominantly) low-precision computing elements. Although

several examples of such real-world problems have been presented herein, and although we have also had success implementing non-bonded force field computations for molecular dynamics simulation and other tasks, these are merely examples and do not constitute an exhaustive set of the real-world problems that embodiments of the present invention may be used to solve.

[00132] The embodiments disclosed above are merely examples and do not constitute limitations of the present invention. Rather, embodiments of the present invention may be implemented in a variety of other ways, such as the following.

[00133] For example, embodiments of the present invention may represent values in any of a variety of ways, such as by using digital or analog representations, such as fixed point, logarithmic, or floating point representations, voltages, currents, charges, pulse width, pulse density, frequency, probability, spikes, timing, or combinations thereof. These underlying representations may be used individually or in combination to represent the LPHDR values. LPHDR arithmetic circuits may be implemented in any of a variety of ways, such as by using various digital methods (which may be parallel or serial, pipelined or not) or analog methods or combinations thereof. Arithmetic elements may be connected using various connection architectures, such as nearest 4, nearest 8, hops of varying degree, and architectures which may or may not be rectangular or grid-like. Any method may be used for communication among arithmetic elements, such as parallel or serial, digital or analog or mixed-mode communication. Arithmetic elements may operate synchronously or asynchronously, and may operate globally simultaneously or

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not. Arithmetic elements may be implemented, for example, on a single physical device, such as a silicon chip, or spread across multiple devices and an embodiment built from multiple devices may have its arithmetic elements connected in a variety of ways, including for example being connected as a grid, torus, hypercube, tree, or other method. Arithmetic elements may be connected to a host machine, if any, in a variety of ways, depending on the cost and bandwidth and other requirements of a particular embodiment. For example there may be many host machines connected to the collection of arithmetic elements.

[00134] Although certain embodiments of the present invention are described as being implemented as a SIMD architecture, this is merely an example and does not constitute a limitation of the present invention. For example, embodiments of the present invention may be implemented as reconfigurable architectures, such as but not limited to programmable logic devices, field programmable analog arrays, or field programmable gate array architectures, such as a design in which existing multiplier blocks of an FPGA are replaced with or supplemented by LPHDR arithmetic elements of any of the kinds disclosed herein, or for example in which LPHDR elements are included in a new or existing reconfigurable device design. As another example, embodiments of the present invention may be implemented as a GPU or SIMT-style architecture which incorporates LPHDR arithmetic elements of any of the kinds disclosed herein. For example, LPHDR elements could supplement or replace traditional arithmetic elements in current or new graphics processing unit designs. As yet another example, embodiments of the present invention may be implemented as a MIMD-style architecture

which incorporates LPHDR arithmetic elements of any of the kinds disclosed herein. For example, LPHDR arithmetic elements could supplement or replace traditional arithmetic elements in current or new MIMD computing system designs. As yet another example, embodiments of the present invention may be implemented as any kind of machine, including a massively parallel machine, which uses compact arithmetic processing elements to provide large amounts of arithmetic computing capability using a small amount of resources (for example, transistors or area or volume) compared with traditional architectures.

[00135] Although certain embodiments of the present invention are described herein as executing software, this is merely an example and does not constitute a limitation of the present invention. Alternatively, for example, embodiments of the present invention may be implemented using microcode or a hardware sequencer or state machine or other controller to control LPHDR arithmetic elements of any of the kinds disclosed herein. Alternatively, for example, embodiments of the present invention may be implemented using hardwired, burned, or otherwise pre-programmed controllers to control LPHDR arithmetic elements of any of the kinds disclosed herein.

[00136] Although certain embodiments of the present invention are described herein as being implemented using custom silicon as the hardware, this is merely an example and does not constitute a limitation of the present invention. Alternatively, for example, embodiments of the present invention may be implemented using FPGA or other reconfigurable chips as the underlying hardware, in which the FPGAs or other reconfigurable chips are configured to perform the LPHDR operations disclosed herein. As another

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example, embodiments of the present invention may be implemented using any programmable conventional digital or analog computing architecture (including those which use high-precision computing elements, including those which use other kinds of non-LPHDR hardware to perform LPHDR arithmetic, and including those which are massively parallel) which has been programmed with software to perform the LPHDR operations disclosed herein. For example, embodiments of the present invention may be implemented using a software emulator of the functions disclosed herein.

[00137] As yet another example, embodiments of the present invention may be implemented using 3D fabrication technologies, whether based on silicon chips or otherwise. Some example embodiments are those in which a memory chip has been bonded onto a processor or other device chip or in which several memory and/or processor or other device chips have been bonded to each other in a stack. 3D embodiments of the present invention are very useful as they may be denser than 2D embodiments and may enable 3D communication of information between the processing units, which enables more algorithms to run efficiently on those embodiments compared to 2D embodiments.

[00138] Although certain embodiments of the present invention are described herein as being implemented using silicon chip fabrication technology, this is merely an example and does not constitute a limitation of the present invention. Alternatively, for example, embodiments of the present invention may be implemented using technologies that may enable other sorts of traditional digital and analog computing processors or other devices. Examples of such technologies include various nanomechanical and

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nanoelectronic technologies, chemistry based technologies such as for DNA computing, nanowire and nanotube based technologies, optical technologies, mechanical technologies, biological technologies, and other technologies whether based on transistors or not that are capable of implementing LPHDR architectures of the kinds disclosed herein.

[00139] Certain embodiments of the present invention have been described as "massively parallel" embodiments. Although certain embodiments of the present invention may include thousands, millions, or more arithmetic units, embodiments of the present invention may include any number of arithmetic units (as few as one). For example, even an embodiment which includes only a single LPHDR unit may be used within a serial processing unit or other device to provide a significant amount of LPHDR processing power in a small, inexpensive processor or other device.

[00140] For certain embodiments of the present invention, even if implemented using only digital techniques, the arithmetic operations may not yield deterministic, repeatable, or the most accurate possible results within the chosen low precision representation. For instance, on certain specific input values, an arithmetic operation may produce a result which is not the nearest value in the chosen representation to the true arithmetic result.

[00141] The degree of precision of a "low precision, high dynamic range" arithmetic element may vary from implementation to implementation. For example, in certain embodiments, a LPHDR arithmetic element produces results which include fractions, that is, values greater than zero and less than one. For example, in certain embodiments, a

LPHDR arithmetic element produces results which are sometimes (or all of the time) no closer than 0.05% to the correct result (that is, the absolute value of the difference between the produced result and the correct result is no more than one-twentieth of one percent of the absolute value of the correct result). As another example, a LPHDR arithmetic element may produce results which are sometimes (or all of the time) no closer than 0.1% to the correct result. As another example, a LPHDR arithmetic element may produce results which are sometimes (or all of the time) no closer than 0.2% to the correct result. As yet another example, a LPHDR arithmetic element may produce results which are sometimes (or all of the time) no closer than 0.5% to the correct result. As yet further examples, a LPHDR arithmetic element may produce results which are sometimes (or all of the time) no closer than 1%, or 2%, or 5%, or 10%, or 20% to the correct result.

[00142] Besides having various possible degrees of precision, implementations may vary in the dynamic range of the space of values they process. For example, in certain embodiments, a LPHDR arithmetic element processes values in a space which may range approximately from one millionth to one million. As another example, in certain embodiments, a LPHDR arithmetic element processes values in a space which may range approximately from one billionth to one billion. As yet another example, in certain embodiments, a LPHDR arithmetic element processes values in a space which may range approximately from one sixty five thousandth to sixty five thousand. As yet further examples, in certain embodiments, a LPHDR arithmetic element processes values in a space which may range from any specific value between zero and one sixty five thousandth up to any specific value

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greater than sixty five thousand. As yet further examples, other embodiments may process values in spaces with dynamic ranges that may combine and may fall between the prior examples, for example ranging from approximately one billionth to ten million. In all of these example embodiments of the present invention, as well as in other embodiments, the values that we are discussing may be signed, so that the above descriptions characterize the absolute values of the numbers being discussed.

[00143] The frequency with which LPHDR arithmetic elements may yield only approximations to correct results may vary from implementation to implementation. For example, consider an embodiment in which LPHDR arithmetic elements can perform one or more operations (perhaps including, for example, trigonometric functions), and for each operation the LPHDR elements each accept a set of inputs drawn from a range of valid values, and for each specific set of input values the LPHDR elements each produce one or more output values (for example, simultaneously computing both sin and cos of an input), and the output values produced for a specific set of inputs may be deterministic or non-deterministic. In such an example embodiment, consider further a fraction F of the valid inputs and a relative error amount E by which the result calculated by an LPHDR element may differ from the mathematically correct result. In certain embodiments of the present invention, for each LPHDR arithmetic element, for at least one operation that the LPHDR unit is capable of performing, for at least fraction F of the possible valid inputs to that operation, for at least one output signal produced by that operation, the statistical mean, over repeated execution, of the numerical values

represented by that output signal of the LPHDR unit, when executing that operation on each of those respective inputs, differs by at least E from the result of an exact mathematical calculation of the operation on those same input values, where F is 1% and E is 0.05%. In several other example embodiments, F is not 1% but instead is one of 2%, or 5%, or 10%, or 20%, or 50%. For each of these example embodiments, each with some specific value for F, there are other example embodiments in which E is not 0.05% but instead is 0.1%, or 0.2%, or 0.5%, or 1%, or 2%, or 5%, or 10%, or 20%. These varied embodiments are merely examples and do not constitute limitations of the present invention.

[00144] For certain devices (such as computers or processors or other devices) embodied according the present invention, the number of LPHDR arithmetic elements in the device (e.g., computer or processor or other device) exceeds the number, possibly zero, of arithmetic elements in the device which are designed to perform high dynamic range arithmetic of traditional precision (that is, floating point arithmetic with a word length of 32 or more bits). If NL is the total number of LPHDR elements in such a device, and NH is the total number of elements in the device which are designed to perform high dynamic range arithmetic of traditional precision, then NL exceeds T(NH), where T() is some function. Any of a variety of functions may be used as the function T(). For example, in certain embodiments, T(NH) may be twenty plus three times NH, and the number of LPHDR arithmetic elements in the device may exceed twenty more than three times the number of arithmetic elements in the device, if any, designed to perform high dynamic range arithmetic of traditional

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precision. As another example, in certain embodiments, the number of LPHDR arithmetic elements in the device may exceed fifty more than five times the number of arithmetic elements in the device, if any, designed to perform high dynamic range arithmetic of traditional precision. As yet another example, in certain embodiments, the number of LPHDR arithmetic elements in the device may exceed one hundred more than five times the number of arithmetic elements in the device, if any, designed to perform high dynamic range arithmetic of traditional precision. As yet another example, in certain embodiments, the number of LPHDR arithmetic elements in the device may exceed one thousand more than five times the number of arithmetic elements in the device, if any, designed to perform high dynamic range arithmetic of traditional precision. As yet another example, in certain embodiments, the number of LPHDR arithmetic elements in the device may exceed five thousand more than five times the number of arithmetic elements in the device, if any, designed to perform high dynamic range arithmetic of traditional precision. Certain embodiments of the present invention may be implemented within a single physical device, such as but not limited to a silicon chip or a chip stack or a chip package or a circuit board, and the number NL of LPHDR elements in the physical device and the number NH of elements designed to perform high dynamic range arithmetic of traditional precision in the physical device may be the total counts of the respective elements within that physical device. Certain embodiments of the present invention may be implemented in a computing system including more than one physical device, such as but not limited to a collection of silicon chips or chip stacks or chip packages or circuit

boards coupled to and communicating with each other using any means (such as a bus, switch, any kind of network connection, or other means of communication), and in this case the number NL of LPHDR elements in the computing system and the number NH of elements designed to perform high dynamic range arithmetic of traditional precision in the computing system may be the total counts of the respective elements within all those physical devices jointly.

[00145] Certain embodiments of the present invention may constitute, or may be part of, processors, which are devices capable of executing software to perform computations. Such processors may include mechanisms for storing software, for using the software to determine what operations to perform, for performing those operations, for storing numerical data, for modifying data according to the software specified operations, and for communicating with devices connected to the processor. Processors may be reconfigurable devices, such as, without limitation, field programmable arrays. Processors may be co-processors to assist host machines or may be capable of operating independently of an external host. Processors may be formed as a collection of component host processors and co-processors of various types, such as CPUs, GPUs, FPGAs, or other processors or other devices, which in the art may be referred to as a heterogeneous processor design or heterogeneous computing system, some or all of which components might incorporate the same or distinct varieties of embodiments of the present invention.

[00146] Embodiments of the present invention may, however, be implemented in devices in addition to or other than processors. For example, a computer including a

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processor and other components (such as memory coupled to the processor by a data path), wherein the processor includes components for performing LPHDR operations in any of the ways disclosed herein, is an example of an embodiment of the present invention. More generally, any device or combination of devices, whether or not falling within the meaning of a "processor," which performs the functions disclosed herein may constitute an example of an embodiment of the present invention.

[00147] More generally, any of the techniques described above may be implemented, for example, in hardware, software tangibly stored on a computer-readable medium, firmware, or any combination thereof. The techniques described above may be implemented in one or more computer programs executing on a programmable computer including a processor, a storage medium readable by the processor (including, for example, volatile and non-volatile memory and/or storage elements), at least one input device, and at least one output device. Program code may be applied to input entered using the input device to perform the functions described and to generate output. The output may be provided to one or more output devices.

[00148] Each computer program within the scope of the claims below may be implemented in any programming language, such as assembly language, machine language, a high-level procedural programming language, or an object-oriented programming language. The programming language may, for example, be a compiled or interpreted programming language.

[00149] Each such computer program may be implemented in a computer program product tangibly embodied in a machine-readable storage device for execution by a computer

processor. Method steps of the invention may be performed by a computer processor executing a program tangibly embodied on a computer-readable medium to perform functions of the invention by operating on input and generating output. Suitable processors include, by way of example, both general and special purpose microprocessors. Generally, the processor receives instructions and data from a read-only memory and/or a random access memory. Storage devices suitable for tangibly embodying computer program instructions include, for example, all forms of non-volatile memory, such as semiconductor memory devices, including EPROM, EEPROM, and flash memory devices; magnetic disks such as internal hard disks and removable disks; magneto-optical disks; and CD-ROMs. Any of the foregoing may be supplemented by, or incorporated in, specially-designed ASICs (application-specific integrated circuits) or FPGAs (Field-Programmable Gate Arrays). A computer can generally also receive programs and data from a storage medium such as an internal disk (not shown) or a removable disk. These elements will also be found in a conventional desktop or workstation computer as well as other computers suitable for executing computer programs implementing the methods described herein, which may be used in conjunction with any digital print engine or marking engine, display monitor, or other raster output device capable of producing color or gray scale pixels on paper, film, display screen, or other output medium.

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Claims

1. A computing system, comprising:

a host computer;

a computing chip comprising:

a processing element array comprising a first edge processing element positioned at a first edge of the processing element array, a second edge processing element positioned at the first edge of the processing element array, a first interior processing element positioned at a first location in the interior of the processing element array, and a second interior processing element positioned at a second location in the interior of the processing element array;

a first processing element connection connecting the first edge processing element with the first interior processing element;

a second processing element connection connecting the second edge processing element with the second interior processing element;

an input-output unit connected to the first edge processing element and the second edge processing element;

a first memory local to the first edge processing element;

a second memory local to the second edge processing element;

a third memory local to the first interior processing element;

a fourth memory local to the second interior processing element; and,

a fifth arithmetic unit;

wherein the first edge processing element comprises a first arithmetic unit;

wherein the second edge processing element comprises a second arithmetic unit;

wherein the first interior processing element comprises a third arithmetic unit; and

wherein the second interior processing element comprises a fourth arithmetic unit; and,

a host connection at least partially connecting the input-output unit with the host computer;

wherein the first, second, third and fourth arithmetic units each comprises a corresponding multiplier circuit adapted to receive as a first input to the corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits;

wherein the fifth arithmetic unit comprises a corresponding multiplier circuit adapted to receive as inputs to the corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein the multiplier circuit corresponding to the first arithmetic unit comprises a first plurality of transistors and has no other transistors, the multiplier circuit corresponding to the second arithmetic unit comprises a second plurality of transistors and has no other transistors, the multiplier circuit corresponding to the third arithmetic unit comprises a third plurality of transistors and has no other transistors, the multiplier

circuit corresponding to the fourth arithmetic unit comprises a fourth plurality of transistors and has no other transistors, and the multiplier circuit corresponding to the fifth arithmetic unit comprises a fifth plurality of transistors; and,

wherein the fifth plurality of transistors exceeds in number each of the first plurality of transistors, the second plurality of transistors, the third plurality of transistors, and the fourth plurality of transistors.

2. The computing system of claim 1, wherein said host computer is programmed to provide instructions to said computing chip that, when executed, cause said processing element array to perform an operation whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.

3. The computing system of claim 1, wherein the computing chip further comprises a control unit connected to the processing element array, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the processing element array to cause the processing element array to operate according to the at least one instruction.

4. The computing system of claim 3, wherein the computing chip further comprises an instruction memory adapted to store the at least one instruction received from the host computer via the input-output unit, wherein the control

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unit is further adapted to retrieve the at least one instruction from the instruction memory.

5. The computing system of claim 1, wherein the width of each first binary mantissa is no more than 10 bits plus a first sign bit, and wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit.

6. The computing system of claim 5, wherein the width of each first binary exponent is at least 5 bits plus a third sign bit and wherein the width of each second binary exponent is at least 5 bits plus a fourth sign bit.

7. A computing system, comprising:

a host computer;

a computing chip comprising:

a processing element array comprising a plurality of first processing elements, wherein the the plurality of first processing elements is no less than 5000 in number, wherein each of a first subset of the plurality of first processing elements is positioned at a first edge of the processing element array, and wherein each of a second subset of the plurality of first processing elements is positioned in the interior of the processing element array;

an input-output unit connected to each of the first subset of the plurality of first processing elements;

a plurality of processing element connections, each processing element connection connecting one of the plurality of first processing elements with another of the plurality of first processing elements,

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wherein each of the plurality of first processing elements is connected to at least one other of the plurality of first processing elements by at least one of the plurality of processing element connections;

a plurality of memory units, wherein each of the plurality of first processing elements is associated with a corresponding one of the plurality of memory units, and wherein each of the plurality of memory units is local to its associated one of the plurality of first processing elements;

a plurality of first arithmetic units, wherein each of the plurality of first processing elements has positioned therein at least one of the plurality of first arithmetic units;

a plurality of second processing elements; and

a plurality of second arithmetic units, wherein each of the plurality of second processing elements has positioned therein at least one of the plurality of second arithmetic units; and

a host connection at least partially connecting the input-output unit with the host computer;

wherein the plurality of first arithmetic units each comprises a first corresponding multiplier circuit adapted to receive as a first input to the first corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the first corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits;

wherein the first multiplier circuits corresponding to the plurality of first arithmetic units each comprises a first respective plurality of transistors and has no other transistors;

wherein the plurality of second arithmetic units each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein the second multiplier circuits corresponding to the plurality of second arithmetic units each comprises a second respective plurality of transistors;

wherein each of the second respective pluralities of transistors of the second multiplier circuits corresponding to the plurality of second arithmetic units exceeds in number each of the first respective pluralities of transistors of the first multiplier circuits corresponding to the plurality of first arithmetic units.

8. The computing system of claim 7,

wherein, other than the plurality of second processing elements, the computing chip has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and

wherein the plurality of first processing elements exceeds in number, by at least 100, the plurality of second processing elements.

9. The computing system of claim 7, wherein the plurality of memory units each comprises a corresponding register.

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10. The computing system of claim 8, wherein said host computer is programmed to provide instructions to said computing chip that, when executed, cause said processing element array to perform an operation whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.

11. The computing system of claim 8, wherein an aggregate maximum bandwidth of the plurality of processing element connections exceeds a maximum bandwidth of the host connection.

12. The computing system of claim 11, wherein the computing chip further comprises a control unit connected to the processing element array, the control unit comprising circuitry adapted to decode at least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the processing element array to cause the processing element array to operate according to the at least one instruction.

13. The computing system of claim 12, wherein the computing chip further comprises an instruction memory adapted to store the at least one instruction received from the host computer via the input-output unit, wherein the control unit is further adapted to retrieve the at least one instruction from the instruction memory.

14. The computing system of claim 7, wherein the width of each first binary mantissa is no more than 10 bits plus a

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first sign bit, and wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit.

15. The computing system of claim 14, wherein the width of each first binary exponent is at least 5 bits plus a third sign bit and wherein the width of each second binary exponent is at least 5 bits plus a fourth sign bit.

16. A circuit board connected to a host computer, the circuit board comprising:

a plurality of processing element arrays, each comprising:

a plurality of first processing elements, wherein the plurality of first processing elements of said processing element array is no less than 5000 in number, wherein each of a first subset of the plurality of first processing elements of said processing element array is positioned at a first edge of said processing element array, and wherein each of a second subset of the plurality of first processing elements of said processing element array is positioned in the interior of said processing element array;

a plurality of processing element connections, each processing element connection connecting one of the plurality of first processing elements of said processing element array with another of the plurality of first processing elements of said processing element array, wherein each of the plurality of first processing elements of said processing element array is connected to at least one other of the plurality of first processing elements of said processing element

array by at least one of the plurality of processing element connections of said processing element array;

a plurality of memory units, wherein each of the plurality of first processing elements of said processing element array is associated with a corresponding one of the plurality of memory units of said processing element array, and wherein each of the plurality of memory units of said processing element array is local to its associated one of the plurality of first processing elements of said processing element array; and,

a plurality of arithmetic units, wherein each of the plurality of first processing elements of said processing element array has positioned therein at least one of the plurality of arithmetic units of said processing element array;

wherein the plurality of arithmetic units of said processing element array each comprises a first corresponding multiplier circuit adapted to receive as a first input to the first corresponding multiplier circuit a first floating point value having a first binary mantissa of width no more than 11 bits and a first binary exponent of width at least 6 bits, and to receive as a second input to the first corresponding multiplier circuit a second floating point value having a second binary mantissa of width no more than 11 bits and a second binary exponent of width at least 6 bits; and,

an input-output unit connected to at least one of the plurality of processing element arrays; and,

a host connection at least partially connecting the input-output unit with the host computer.

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17. The circuit board of claim 16,

wherein the circuit board further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein other than the second processing elements, the circuit board has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and,

wherein a total count of the pluralities of first processing elements of the plurality of processing element arrays exceeds in number, by at least 20 more than three times, the plurality of second processing elements.

18. The circuit board of claim 16,

wherein the circuit board further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein other than the second processing elements the circuit board has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and,

wherein a total count of the pluralities of first processing elements of the plurality of processing element

arrays exceeds in number, by at least 1000 more than five times, the plurality of second processing elements.

19. The circuit board of claim 16,

wherein the circuit board further comprises a plurality of second processing elements, wherein the plurality of second processing elements each comprises a second corresponding multiplier circuit adapted to receive as inputs to the second corresponding multiplier circuit two floating point values each of width at least 32 bits;

wherein other than the second processing elements the circuit board has no other processing element that comprises a multiplier circuit adapted to receive as inputs to the multiplier circuit two floating point values each of width at least 32 bits; and,

wherein a total count of the pluralities of first processing elements of the plurality of processing element arrays exceeds in number, by at least 100 more, the plurality of second processing elements.

20. The circuit board of claim 18, wherein said circuit board is adapted to receive instructions from the host computer that, when executed, cause at least one of said processing element arrays to perform an operation whose output is used to identify at least one image, from a plurality of images to be searched, that is similar to at least one input image.

21. The circuit board of claim 18, wherein the circuit board further comprises a control unit connected to at least one of the plurality of processing element arrays, the control unit comprising circuitry adapted to decode at

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least one instruction received from the host computer via the input-output unit, and to send at least one control signal to the at least one of the plurality of processing element arrays to cause the at least one of the plurality of processing element arrays to operate according to the at least one instruction.

22. The circuit board of claim 21,

wherein the circuit board further comprises an instruction memory connected to the control unit, the instruction memory comprising circuitry adapted to store the at least one instruction received from the host computer via the input-output unit, and

wherein the control unit further comprises circuitry adapted to retrieve the at least one instruction from the instruction memory.

23. The circuit board of claim 16, wherein the width of each first binary mantissa is no more than 10 bits plus a first sign bit, and wherein the width of each second binary mantissa is no more than 10 bits plus a second sign bit.

24. The circuit board of claim 23, wherein the width of each first binary exponent is at least 5 bits plus a third sign bit and wherein the width of each second binary exponent is at least 5 bits plus a fourth sign bit.

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Abstract

Low precision computers can be efficient at finding possible answers to search problems. However, sometimes the task demands finding better answers than a single low precision search. A computer system augments low precision computing with a small amount of high precision computing, to improve search quality with little additional computing.

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