

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Overview and Summaries

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2004 ITRS SUMMARY

2004 UPDATE OVERVIEW



The ITRS process is an ongoing event. The industry is dynamic—continually innovating; introducing new products; and achieving solutions. To keep the ITRS information as current as possible with this dynamic industry environment, during each year following an edition such as the *2003 ITRS*, the roadmap information is reviewed. Data adjustments, corrections, and new information items are agreed to among the ITWG members and by soliciting public feedback during the annual ITRS

Summer Conference in San Francisco. For the 2004 Update effort, all the ITRS tables were reviewed. If necessary, data and notations were updated to match industry advancements.

[Link to the 2003 ITRS](#)

Key Changes of the 2004 Update

A significant task was performed during this past year by annualizing all the tables. Previous years for the “long-term” technology requirements tables were indicated only for those years of technology generations, also referred to as “node” years. New for the 2004 Update, and set in place for the more involved effort of the complete revision of the 2005 ITRS, all 15 years of the ITRS timeframe are now indicated in all tables.

All chapters of the *2003 ITRS* have updates. Of the 219 tables contained in the 2003 ITRS, 128 tables were updated and 4 new tables were added. Additionally, 12 figures were updated. Many of the difficult challenges for the ITRS were revisited and updated to reflect the most current thinking and most critical tasks for semiconductor R&D. The *Overall Technology Roadmap Characteristics* were updated to reflect chapter table updates as well as indicate some revisions to be consistent with the technology tables. Please refer to the Appendix for the complete listing of ITRS tables and updates.

The reader should realize, that for the 2003 ITRS, the Near-term years span from 2003 to 2009 while the Long-term years span from 2010 to 2018. The reader will notice however that the year 2010 represents the year in which the hp45 technology node will occur. Several ITWGs have included any consideration related to this technology node in their Near-term challenges since it was easier for many of them to concentrate their attention on a well-defined technology node. Normally the technology nodes are studied very attentively while the data shown in the tables for the intermediate years are obtained by interpolation.

During this global review of the 2003 ITRS, a key message is that many of the difficult challenges and technology requirements were verified as correctly assessed for the semiconductor industry.

Although the update years focus on the table values, several chapters added new topics. A section introducing Emerging Research Materials was added to the Emerging Research Devices chapter, which was reviewed and updated in its entirety.

CD control tolerances and the timing of the introduction of 450nm were pervasive discussions among the teams. Edge exclusion was aligned among Front End Processes, Lithography, Factory Integration, and Yield Enhancement.

Other specific changes and challenges among the teams are as follows:

The Design chapter is revised to include an updated section on Design for Manufacturability and Design Verification, with several additional figures and tables.

Simultaneous modeling, using integrated input from a variety of related simulations [interconnect and packaging, or device and circuit] is viewed as critical.

Parametrically sensitive yield models that include new materials and comprehend the increased complexity within the fab are noted as a critical challenge in yield management. Other challenges for maintaining cost-effective yield management

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include new high aspect ratio inspection tools, testable and diagnosable designs for ICs, improvement in yield learning data management and test structures, as well as the critical need for achieving historic yield ramps and mature yield levels through efficient yield learning cycles.

New criteria for assessing potential solutions for Lithography now must address leading-edge manufacturing in at least two geographic regions with infrastructure in place [such as resists and mask capability]. Immersion lithography requirements and challenges were expanded, as this technology now appears viable down to 22nm. Particular parameters for mask and resists needs were evaluated to the current industry capability also resulting in revisions to timing of likely capability.

Interconnect added Cu resistivity numbers to reflect surface and sidewall scattering effects. The deterioration of resistivity as copper wire linewidth decreases is a key concern. Low κ values remain unchanged. For the first time in the past 10 years, the low κ portion of the roadmap was unaltered (κ value targets not delayed) with respect to the prior edition. Small changes were made to the shading of the boxes for bulk and effective dielectric constant over the next five years, recognizing that materials that deliver an effective $\kappa=2.7$ are in production today, and those material systems that will deliver an effective $\kappa=2.4$ are expected to be available with manufacturable solutions in the next three years.

DRAM interconnect requirements with respect to contact resistivity have been updated. Also, specific interconnect requirements for other memory products, such as embedded memory and Flash, will be distinguished from DRAM in the 2005 ITRS.

A discussion on Gate CD tolerances throughout 2004 between Front End Processes and Lithography, and based on a industry survey, indicated this is a critical requirement to be resolved in the ITRS. The Front End Processes review also addressed the acceleration for the introduction of silicon-on-insulator [SOI]. Additionally, back surface particles are now included in the Surface Preparation section, with further study and discussion to occur in 2005.

Technology Requirements Guideline

“Interim Solutions are Known” is an additional category to the requirements tables’ legend for the 2003 ITRS. This cell color is used in updated tables in many of the chapters, particularly Lithography, Interconnect, Metrology, and Modeling and Simulation. This requirements category appears as patterned colored cell with a red tag next to the data.

White—Manufacturable Solutions Exist, and Are Being Optimized

Yellow—Manufacturable Solutions are Known

Red—Manufacturable Solutions are NOT Known

Interim Solutions are Known



A definition of interim solutions is included in the Glossary.

The Glossary now includes the added definition of Interim Solutions to augment the new legend category.

FEATURES OF THE 2004 UPDATE ON THE CD

- Links to the 2003 ITRS chapters are provided for convenience and easy review.
- Updated tables are noted with a line-item comparison of the 2003 ITRS [noted as “Was”] and the 2004 Update data [noted as “Is”], with the changed cells clearly outlined and data in underlined font. If a line item was either deleted or added during the 2004 Update, the line is indicated.

WAS	Line item	2003 data	2003 data	2003 data	2003 data	2003 data
IS	Line item	2004 data	2003 data	2004 data	2004 data	2004 data

Delete	Line-item	2003-data	2003-data	2003-data	2003-data
Add	New line item	data	data	data	data

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS TABLES

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
ASIC/Low Operating Power Printed Gate Length (nm) ††	90	75	65	53	45	40	35
ASIC/Low Operating Power Physical Gate Length (nm)	65	53	45	37	32	28	25

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term Years [UPDATED](#)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	ASIC/Low Operating Power Printed Gate Length (nm) ††	32		25	22		18	16		13
IS	ASIC/Low Operating Power Printed Gate Length (nm) ††	32	28	25	22	20	18	16	14	13
WAS	ASIC/Low Operating Power Physical Gate Length (nm)	22		18	16		13	11		9
IS	ASIC/Low Operating Power Physical Gate Length (nm)	22	20	18	16	14	13	11	10	9

Notes for Tables 1a and 1b

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also “as etched in polysilicon,” in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC “physical” gate lengths may be reduced from the “as-printed” dimension. These “physical” gate-length targets are driven by the need for maximum speed performance in logic Microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design ITWG Tables as needs that drive device design and process technology requirements.

In addition, during the 2003 ITRS development, an attempt has been made to reconcile the many published press releases by Logic manufacturers referencing “90 nm” technology node manufacturing in 2003. Since the metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that the public citations were in reference to an “indexed” technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance).

The IRC has decided that the best way to minimize confusion between the ITRS and individual company public announcements is to identify the ITRS table header node with the industry's most aggressive half-pitch targets, and to label these targets as hpXX (i.e., hp90, hp65, hp45, etc.). Currently the industry's most aggressive half pitch is the DRAM cell metal half-pitch. Refer to the Glossary for definitions of Introduction, Production, InTRegeneration, and InTRAgeneration terms.

4 Overall Roadmap Technology Characteristics Tables

Table 1c DRAM Production Product Generations and Chip Size Model—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Cell area factor [a]	8	8	7.5	7	7	6	6
Cell area [Ca = a ²] (μm ²)	0.082	0.065	0.048	0.036	0.028	0.019	0.015
Cell array area at production (% of chip size) §	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%
Generation at production §	1G	1G	1G	2G	2G	4G	4G
Functions per chip (Gbits)	1.07	1.07	1.07	2.15	2.15	4.29	4.29
Chip size at production (mm ²)§	139	110	82	122	97	131	104
Gbits/cm ² at production §	0.77	0.97	1.31	1.76	2.22	3.27	4.12

Table 1d DRAM Production Product Generations and Chip Size Model—Long-term Years **UPDATED**

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
WAS	Cell area factor [a]	6		6	6		6	5		5
IS	Cell area factor [a]	6	<u>6</u>	6	6	<u>6</u>	6	5	<u>5</u>	5
WAS	Cell area [Ca = a ²] (mm ²)	0.012		0.0077	0.0061		0.0038	0.0025		0.0016
IS	Cell area [Ca = a ²] (μm ²)	0.012	<u>0.0096</u>	0.0077	0.0061	<u>0.005</u>	0.0038	0.0025	<u>0.002</u>	0.0016
WAS	Cell array area at production (% of chip size) §	63.00%		63.00%	63.00%		63.00%	63.00%		63.00%
IS	Cell array area at production (% of chip size) §	63.00%	<u>63.00%</u>	63.00%	63.00%	<u>63.00%</u>	63.00%	63.00%	<u>63.00%</u>	63.00%
WAS	Generation at production §	4G		8G	8G		16g	32G		32G
IS	Generation at production §	4G	<u>8G</u>	8G	8G	<u>16g</u>	16g	32G	<u>32G</u>	32G
WAS	Functions per chip (Gbits)	4.29		8.59	8.59		17.18	34.36		34.36
IS	Functions per chip (Gbits)	4.29	<u>8.59</u>	8.59	8.59	<u>17.18</u>	17.18	34.36	<u>34.36</u>	34.36
WAS	Chip size at production (mm ²)§	83		104	83		104	138		87
IS	Chip size at production (mm ²)§	83	<u>131</u>	104	83	<u>131</u>	104	138	<u>110</u>	87
WAS	Gbits/cm ² at production §	5.19		8.23	10.37		16.46	24.89		39.51
IS	Gbits/cm ² at production §	5.19	<u>6.53</u>	8.23	10.37	<u>13.07</u>	16.46	24.89	<u>31.36</u>	39.51

Notes for Tables 1c and 1d

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows

1999-2004/8× 2005/7.5×; 2006-2007/7×; 2008-2015/6×; 2016-2018/5×. The delay of the “6” DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of “Moore’s Law” bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

InTER-generation chip size growth rate model target for Production-phase DRAMs is now “flat” at less than 140 nm², similar to the MPU model. This new flat-chip-size model target requires the bits/chip “Moore’s Law” model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Table 1c, d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63%, which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above). The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Cell area factor [a]	8	8	7.5	7	7	6	6
Cell area [$Ca = af^2$] (μm ²)	0.082	0.065	0.048	0.036	0.028	0.019	0.015
Cell array area at introduction (% of chip size) §	72.23%	72.61%	72.95%	73.25%	73.52%	73.76%	73.97%
Generation at introduction §	4G	4G	8G	8G	16G	16G	16G
Functions per chip (Gbits)	4.29	4.29	8.59	8.59	17.18	17.18	17.18
Chip size at introduction (mm ²) §	485	383	568	419	662	449	356
Gbits/cm ² at introduction §	0.88	1.12	1.51	2.05	2.59	3.82	4.83

6 Overall Roadmap Technology Characteristics Tables

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years [UPDATED](#)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	-	42	38	-	30	27	-	21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
WAS	Cell area factor [a]	6	-	6	6	-	6	5	-	5
IS	Cell area factor [a]	6	<u>6</u>	6	6	<u>6</u>	6	5	<u>5</u>	5
WAS	Cell area [Ca = af ²] (mm ²)	0.012	-	0.0077	0.0061	-	0.0038	0.0025	-	0.0016
IS	Cell area [Ca = af ²] (μm ²)	0.0120	<u>0.01</u>	0.0077	0.0061	<u>0.005</u>	0.0038	0.0025	<u>0.0020</u>	0.0016
WAS	Cell array area at introduction (% of chip size) §	74.16%	-	74.47%	74.61%	-	74.83%	74.93%	-	75.09%
IS	Cell array area at introduction (% of chip size) §	74.16%	<u>74.30%</u>	74.47%	74.61%	<u>74.70%</u>	74.83%	74.93%	<u>75.00%</u>	75.09%
WAS	Generation at introduction §	32G	-	32G	64G	-	64G	128G	-	128G
IS	Generation at introduction §	32G	<u>32G</u>	32G	64G	<u>64G</u>	64G	128G	<u>128G</u>	128G
WAS	Functions per chip (Gbits)	34.36	-	34.36	68.72	-	68.7	137.4	-	137.4
IS	Functions per chip (Gbits)	34.36	<u>34.36</u>	34.36	68.72	<u>68.72</u>	68.7	137.4	<u>137.4</u>	137.4
WAS	Chip size at introduction (mm ²) §	563	-	353	560	-	351	464	-	292
IS	Chip size at introduction (mm ²) §	563	<u>458</u>	353	560	<u>456</u>	351	464	<u>378</u>	292
WAS	Gbits/cm ² at introduction §	5.2	-	8.2	10.4	-	16.5	24.9	-	39.5
IS	Gbits/cm ² at introduction §	<u>6.10</u>	<u>7.71</u>	<u>9.73</u>	<u>12.3</u>	<u>15.5</u>	<u>19.6</u>	<u>29.6</u>	<u>37.3</u>	<u>47.1</u>

Notes for Tables 1e and 1f

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows

1999–2004/8× 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the “6” DRAM Cell design improvement Factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of “Moore’s Law” bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a 3-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4×bits/chip every four years with interim 2×bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation/2007, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation/2003, the introduction rate is 4×/five years (2×/two–three years).

The original 2001 ITRS InTER-generation chip size growth rate was targeted to fit one chip per 572 mm² field at Introduction and two chips per 572 mm² field at Production. Due to the delay of the cell area factor reductions, Introduction chip sizes increased, but the new 704 mm² maximum affordable Litho field allows the Introduction chip to double bits per chip every two years through the 16 Gbit generation (660 mm²/2007). Slowing the “Moore’s Law” bits per chip of the Introduction-phase DRAM model to an average of 2×per 2.5 years enables the Introduction DRAMs to remain under the original 572 mm² affordable target after 2007. The InTRA-generation chip size shrink model remains at 0.5× every technology node in-between cell factor reductions, and eventually (ranging from five to six years), the Introduction-phase DRAMs shrink below the 140 mm² Production-phase chip size target.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years [UPDATED](#)

Year of Production		2003	2004	2005	2006	2007	2008	2009
Technology Node			hp90			hp65		
DRAM ½ Pitch (nm)		100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)		120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)		107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††		65	53	45	40	35	32	28
MPU Physical Gate Length (nm)		45	37	32	28	25	22	20
SRAM Cell (6-transistor) Area factor ++		120.3	117.8	115.6	113.7	111.9	110.4	109
Logic Gate (4-transistor) Area factor ++		320	320	320	320	320	320	320
SRAM Cell (6-transistor) Area efficiency ++		0.63	0.63	0.63	0.63	0.63	0.63	0.63
Logic Gate (4-transistor) Area efficiency ++		0.50	0.50	0.50	0.50	0.50	0.50	0.50
NEW	SRAM Cell (6-transistor) Area ++	1.23	0.95	0.74	0.58	0.45	0.35	0.28
	SRAM Cell (6-transistor) Area w/overhead ++	2.0	1.5	1.2	0.93	0.73	0.57	0.45
NEW	Logic Gate (4-transistor) Area ++	3.27	2.59	2.06	1.63	1.30	1.03	0.82
	Logic Gate (4-transistor) Area w/overhead ++	6.5	5.2	4.1	3.3	2.6	2.1	1.6
WAS	Transistor density SRAM (Mtransistors/cm ²)	305	393	504	646	827	1,057	1,348
	Transistor density logic (Mtransistors/cm ²)	61	77	97	122	154	194	245
	Generation at introduction *	--	p07c	--	--	p10c	--	--
	Functions per chip at introduction (million transistors [Mtransistors])	180	226	285	360	453	571	719
	IS Functions per chip at introduction (million transistors [Mtransistors])	<u>307</u>	<u>386</u>	<u>487</u>	<u>614</u>	<u>773</u>	<u>974</u>	<u>1227</u>
IS	Chip size at introduction (mm ²) ‡	280	280	280	280	280	280	280
	Cost performance MPU (Mtransistors/cm ² at introduction) (including on-chip SRAM) ‡	110	138	174	219	276	348	438
	Generation at production *	--	p04c	--	--	p07c	--	--
	Functions per chip at production (million transistors [Mtransistors])	153	193	243	307	386	487	614
	Chip size at production (mm ²) §§	140	140	140	140	140	140	140
	Cost performance MPU (Mtransistors/cm ² at production, including on-chip SRAM) ‡	110	138	174	219	276	348	438

8 Overall Roadmap Technology Characteristics Tables

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
WAS	SRAM Cell (6-transistor) Area factor ++	107.8		105.7	104.8		103.4	102.8		101.7
IS	SRAM Cell (6-transistor) Area factor ++	107.8	<u>106.7</u>	105.7	104.8	<u>104.1</u>	103.4	102.8	<u>102.2</u>	101.7
WAS	Logic Gate (4-transistor) Area factor ++	320		320	320		320	320		320
IS	Logic Gate (4-transistor) Area factor ++	320	<u>320</u>	320	320	<u>320</u>	320	320	<u>320</u>	320
WAS	SRAM Cell (6-transistor) Area efficiency ++	0.625		0.625	0.625		0.625	0.625		0.625
IS	SRAM Cell (6-transistor) Area efficiency ++	0.625	<u>0.625</u>	0.625	0.625	<u>0.625</u>	0.625	0.625	<u>0.625</u>	0.625
WAS	Logic Gate (4-transistor) Area efficiency ++	0.5		0.5	0.5		0.5	0.5		0.5
IS	Logic Gate (4-transistor) Area efficiency ++	0.50	<u>0.50</u>	0.50	0.50	<u>0.50</u>	0.50	0.50	<u>0.50</u>	0.50
NEW	SRAM Cell (6-transistor) Area	<u>0.22</u>	<u>0.17</u>	<u>0.13</u>	<u>0.11</u>	<u>0.084</u>	<u>0.066</u>	<u>0.052</u>	<u>0.041</u>	<u>0.032</u>
WAS	SRAM Cell (6-transistor) Area w/overhead ++	0.22		0.13	0.11		0.066	0.052		0.032
IS	SRAM Cell (6-transistor) Area w/overhead ++	<u>0.35</u>	<u>0.27</u>	<u>0.22</u>	<u>0.17</u>	<u>0.13</u>	<u>0.106</u>	<u>0.083</u>	<u>0.07</u>	<u>0.052</u>
NEW	Logic Gate (4-transistor) Area	<u>0.65</u>	<u>0.51</u>	<u>0.41</u>	<u>0.32</u>	<u>0.26</u>	<u>0.20</u>	<u>0.16</u>	<u>0.13</u>	<u>0.10</u>
WAS	Logic Gate (4-transistor) Area w/overhead ++	1.3		0.82	0.65		0.41	0.32		0.2
IS	Logic Gate (4-transistor) Area w/overhead ++	1.30	<u>1.03</u>	0.82	0.65	<u>0.51</u>	0.41	0.32	<u>0.26</u>	0.20
WAS	Transistor density SRAM (Mtransistors/cm ²)	1,718		2,781	3,532		5,687	7,208		11,558
IS	Transistor density SRAM (Mtransistors/cm ²)	1,718	<u>2,187</u>	2,781	3,532	<u>4,484</u>	5,687	7,208	<u>9,130</u>	11,558
WAS	Transistor density logic (Mtransistors/cm ²)	309		490	617		980	1,235		1,960
IS	Transistor density logic (Mtransistors/cm ²)	309	<u>389</u>	490	617	<u>778</u>	980	1,235	<u>1,555</u>	1,960

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years **UPDATED** (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	Generation at introduction *	p13c		--	p16c		--	p19c		--
IS	Generation at introduction *	p13c	--	--	p16c	--	--	p19c	--	--
WAS	Functions per chip at introduction (million transistors [Mtransistors])	1,546		2,454	3,092		4,908	6,184		9,816
IS	Functions per chip at introduction (million transistors [Mtransistors])	<u>1,546</u>	<u>1,948</u>	<u>2,454</u>	<u>3,092</u>	<u>3,896</u>	<u>4,908</u>	<u>6,184</u>	<u>7,791</u>	<u>9,816</u>
WAS	Chip size at introduction (mm ²) ‡	280		280	280		280	280		280
IS	Chip size at introduction (mm ²) ‡	280	<u>280</u>	280	280	<u>280</u>	280	280	<u>280</u>	280
WAS	Cost performance MPU (Mtransistors/cm ² at introduction) (including on-chip SRAM) ‡	552		876	1,104		1,753	2,209		3,506
IS	Cost performance MPU (Mtransistors/cm ² at introduction) (including on-chip SRAM) ‡	552	<u>696</u>	876	1,104	<u>1,391</u>	1,753	2,209	<u>2,783</u>	3,506
WAS	Generation at production *	p10c		--	p13c		--	p16c		--
IS	Generation at production *	p10c	--	--	p13c	--	--	p16c	--	--
WAS	Functions per chip at production (million transistors [Mtransistors])	773		1,227	1,546		2,454	3,092		4,908
IS	Functions per chip at production (million transistors [Mtransistors])	773	<u>974</u>	1,227	1,546	<u>1,948</u>	2,454	3,092	<u>3,896</u>	4,908
WAS	Chip size at production (mm ²) §§	140		140	140		140	140		140
IS	Chip size at production (mm ²) §§	140	<u>140</u>	140	140	<u>140</u>	140	140	<u>140</u>	140
WAS	Cost performance MPU (Mtransistors/cm ² at production, including on-chip SRAM) ‡	552		876	1,104		1,753	2,209		3,506
IS	Cost performance MPU (Mtransistors/cm ² at production, including on-chip SRAM) ‡	552	<u>696</u>	876	1,104	<u>1,391</u>	1,753	2,209	<u>2,783</u>	3,506

Notes for Tables 1g and 1h

++ The MPU area factors are analogous to the “cell area factor” for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

* p is processor; numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p01c, was introduced in 1999, but not ramped into volume production until 2001; similarly, the p04c, is introduced in 2001, but is targeted for volume production in 2004.

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/1999), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm²/cost-performance at introduction; 140 mm²/cost-performance at production; 310 mm²/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions

10 Overall Roadmap Technology Characteristics Tables

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years
UPDATED

Year of Production		2003	2004	2005	2006	2007	2008	2009
Technology Node			hp90			hp65		
DRAM ½ Pitch (nm)		100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)		120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)		107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††		65	53	45	40	35	32	28
MPU Physical Gate Length (nm)		45	37	32	28	25	22	20
Logic (Low-volume Microprocessor) High-performance ‡								
WAS	Generation at production **	p03h	--	p05h	--	p07h	--	p09h
IS	Generation at production **	--	<u>p04h</u>	--	--	p07h	--	--
Functions per chip (million transistors)		439	553	697	878	1,106	1,393	1,756
Chip size at production (mm ²) §§		310	310	310	310	310	310	310
High-performance MPU Mtransistors/cm ² at production (including on-chip SRAM) ‡		142	178	225	283	357	449	566
ASIC								
ASIC usable Mtransistors/cm ² (auto layout)		142	178	225	283	357	449	566
ASIC max chip size at production (mm ²) (maximum lithographic field size)		572	572	572	572	572	572	572
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)		810	1,020	1,286	1,620	2,041	2,571	3,239

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years
UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
	Logic (Low-volume Microprocessor) High-performance ‡									
WAS	Generation at production **	--		--	p13h		p15h	--		--
IS	Generation at production **	p10h	--	--	p13h	--	--	p16h	--	--
WAS	Functions per chip (million transistors)	2,212		3,511	4,424		7,022	8,848		14,045
IS	Functions per chip (million transistors)	2,212	<u>2,787</u>	3,511	4,424	<u>5,574</u>	7,022	8,848	<u>11,147</u>	14,045
WAS	Chip size at production (mm ²) §§	310		310	310		310	310		310
IS	Chip size at production (mm ²) §§	310	<u>310</u>	310	310	<u>310</u>	310	310	<u>310</u>	310
WAS	High-performance MPU Mtransistors/cm ² at production (including on-chip SRAM) ‡	714		1,133	1,427		2,265	2,854		4,531
IS	High-performance MPU Mtransistors/cm ² at production (including on-chip SRAM) ‡	714	<u>899</u>	1,133	1,427	<u>1,798</u>	2,265	2,854	<u>3,596</u>	4,531
	ASIC									
WAS	ASIC usable Mtransistors/cm ² (auto layout)	714		1,133	1,427		2,265	2,854		4,531
IS	ASIC usable Mtransistors/cm ² (auto layout)	714	<u>899</u>	1,133	1,427	<u>1,798</u>	2,265	2,854	<u>3,596</u>	4,531
WAS	ASIC maximum chip size at production (mm ²) (maximum lithographic field size)	572		572	572		572	572		572
IS	ASIC maximum chip size at production (mm ²) (maximum lithographic field size)	572	<u>572</u>	572	572	<u>572</u>	572	572	<u>572</u>	572
WAS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081		6,479	8,163		12,958	16,326		25,915
IS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081	<u>5,142</u>	6,479	8,163	<u>10,284</u>	12,958	16,326	<u>20,569</u>	25,915

Notes for Tables 1i and 1j

** p is processor, numerals reflect year of production; h indicates high-performance product. Examples—the high-performance processor, p99h, was ramped into volume production in 1999; similarly, the p01h, is introduced in 2001, the p03h in 2003, and so forth.

‡ MPU High-performance Model—High-performance MPU includes large L2 and L3 on-chip SRAM (2MByte/1999) plus a larger logic core (P99h core = 25M transistor (Mtransistors) both SRAM and Logic functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm²/cost-performance at introduction; 140 mm²/cost-performance at production; 310 mm²/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions

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Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Lithography Field Size							
Lithography Field Size—area (mm ²)	704	704	704	704	704	704	704
Lithographic field size—length (mm)	32	32	32	32	32	32	32
Lithographic field size—width (mm)	22	22	22	22	22	22	22
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	300	300	300	300	300	300	300

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	-	42	38	-	30	27	-	21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
	Lithography Field Size									
WAS	Lithography Field Size—area (mm ²)	704		704	704		704	704		704
IS	Lithography Field Size—area (mm ²)	704	<u>704</u>	704	704	<u>704</u>	704	704	<u>704</u>	704
WAS	Lithographic field size—length (mm)	32	-	32	32	-	32	32	-	32
IS	Lithographic field size—length (mm)	32	<u>32</u>	32	32	<u>32</u>	32	32	<u>32</u>	32
WAS	Lithographic field size—width (mm)	22	-	22	22	-	22	22	-	22
IS	Lithographic field size—width (mm)	22	<u>22</u>	22	22	<u>22</u>	22	22	<u>22</u>	22
	Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)									
WAS	Bulk or epitaxial or SOI wafer	300		450	450		450	450		450
IS	Bulk or epitaxial or SOI wafer	300	<u>300</u>	450	450	<u>450</u>	450	450	<u>450</u>	450

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years [UPDATED](#)

Year of Production		2003	2004	2005	2006	2007	2008	2009
Technology Node			hp90			hp65		
DRAM ½ Pitch (nm)		100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)		120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)		107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††		65	53	45	40	35	32	28
MPU Physical Gate Length (nm)		45	37	32	28	25	22	20
Number of Chip I/Os (Number of Total Chip Pads)—Maximum								
WAS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,328	3,584
IS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072
WAS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,109	1,195
IS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,024	1,024
WAS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,219	2,389
IS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,048	2,048
WAS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,600	4,800
IS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,400	4,600
WAS	Signal I/O pads—ASIC high-performance	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Signal I/O pads—ASIC high-performance	1700	1800	2000	2100	2200	2200	2300
WAS	Power and ground pads—ASIC high-performance (½ of total pads)	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Power and ground pads—ASIC high-performance (½ of total pads)	1700	1800	2000	2100	2200	2200	2300
Number of Total Package Pins—Maximum [1]								
WAS	Microprocessor/controller, cost-performance	500–1,452	500–1,600	550–1,760	550–1,936	600–2,140	660–2,354	720–2,568
IS	Microprocessor/controller, cost-performance	--	500–1600	550–1760	550–1936	600–2140	600–2400	660–2800
WAS	Microprocessor/controller, high-performance	1,452	1,600	1,760	1,936	2,140	2,354	2,568
IS	Microprocessor/controller, high-performance	--	1,600	1,760	1,936	2,140	2,400	2,800
WAS	ASIC (high-performance)	2,400	3,000	3,400	3,800	4,000	4,400	4,600
IS	ASIC (high-performance)	--	3,000	3,400	3,800	4,000	4,400	4,600

Notes for Tables 3a and 3b

[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by PWB technology and system cost.

The highest pin count applications will as a result use larger pitches and larger package sizes.

The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2:1 to 1:4.

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Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years [UPDATED](#)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
Number of Chip I/Os (Number of Total Chip Pads)—Maximum										
WAS	Total pads—MPU	3,840		4,096	4,224		4,352	4,416		4,544
IS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072
WAS	Signal I/O—MPU (1/3 of total pads)	1,280		1,365	1,408		1,451	1,472		1,515
IS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024
WAS	Power and ground pads—MPU (2/3 of total pads)	2,560		2,731	2,816		2,901	2,944		3,029
IS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048
WAS	Total pads—ASIC high-performance	4,800		5,200	5,400		5,800	6,000		6,400
IS	Total pads—ASIC high-performance	4,800	4,800	5,000	5,400	5,400	5,600	6,000	6,000	6,200
WAS	Signal I/O pads—ASIC high-performance	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Signal I/O pads—ASIC high-performance	2,400	2,400	2,500	2,700	2,700	2,800	3,000	3,000	3,100
WAS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	2,400	2,500	2,700	2,700	2,800	3,000	3,000	3,100
Number of Total Package Pins—Maximum [1]										
	Microprocessor/controller, cost-performance	780–2,782		936–3,338	1014–3,616		1217–4,340	1318–4,702		1521–5,426
	Microprocessor/controller, high-performance	2,782		3,338	3,616		4,340	4,702		5,426
	ASIC (high-performance)	4,009		4,810	5,335		6,402	7,042		8,450

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years [UPDATED](#)

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Chip Pad Pitch (micron)							
WAS Pad pitch—ball bond	40	35	30	25	25	20	20
IS Pad pitch—ball bond	<u>40</u>	<u>40</u>	<u>35</u>	<u>35</u>	<u>30</u>	<u>30</u>	<u>25</u>
WAS Pad pitch—wedge bond	30	25	20	20	20	20	20
IS Pad pitch—wedge bond	<u>30</u>	<u>30</u>	<u>30</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>20</u>
Pad Pitch—area array flip-chip (cost-performance, high-performance)	150	150	130	130	120	110	100
Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	60	60	40	40	30	30	20
Cost-Per-Pin							
Package cost (cents/pin) (cost-performance)—minimum-maximum	.75–1.30	.71–1.24	.67–1.17	.64–1.11	.61–1.05	.58–1.00	.55–.96
WAS Package cost (cents/pin) (Memory)— minimum-maximum	0.30–0.56	0.29–.53	.27–.50	.26–.48	.25–.45	.23–.43	.22–.41
IS Package cost (cents/pin) (Memory)— minimum-maximum	0.30–0.56	<u>0.30–.53</u>	.27–.50	.26–.48	.25–.45	.23–.43	.22–.41

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Table 4b Performance and Package Chips: Pads, Cost—Long-term Years *UPDATED*

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
	Chip Pad Pitch (micron)									
WAS	Pad pitch—ball bond	20		20	20		20	20		20
IS	Pad pitch—ball bond	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>
WAS	Pad Pitch—wedge bond	20		20	20		20	20		20
IS	Pad Pitch—wedge bond	20	<u>20</u>	20	20	<u>20</u>	20	20	<u>20</u>	20
WAS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	100		90	90		80	80		70
IS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	<u>90</u>	--	90		--	80	--	--	70
WAS	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	20		20	20		15	15		15
IS	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	20	<u>20</u>	20	20	--	15	15	<u>15</u>	15
	Cost-Per-Pin									
	Package cost (cents/pin) (cost-performance)— minimum—maximum	0.52–0.94		0.5–.86	0.5–.77		0.5–0.69	0.5–0.65		0.5–0.59
	Package cost (cents/pin) (Memory)— minimum—maximum	.22–.41		0.22–0.36	0.22–0.35		0.22–0.31	0.22–0.29		0.22–0.27

Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Chip Frequency (MHz)							
On-chip local clock	2,976	4,171	5,204	6,783	9,285	10,972	12,369
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	2,000	2,500	3,125	3,906	4,883	6,103	7,629
Maximum number wiring levels—maximum	13	14	15	15	15	16	16
Maximum number wiring levels—minimum	9	10	11	11	11	12	12

Table 4d Performance and Package Chips: Frequency, On-chip Wiring Levels—Long-term Years

UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
Chip Frequency (MHz)										
	On-chip local clock	15,079		20,065	22,980		33,403	39,683		53,207
	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	9,536		14,901	18,626		29,103	36,379		56,843
WAS	Maximum number wiring levels—maximum	16		16	16		17	18		18
IS	Maximum number wiring levels—maximum	16	<u>16</u>	16	16	<u>17</u>	17	18	<u>18</u>	18
WAS	Maximum number wiring levels—minimum	12		12	12	-	13	14	-	14
IS	Maximum number wiring levels—minimum	12	<u>12</u>	12	12	<u>13</u>	13	14	<u>14</u>	14

Note for Tables 4c and 4d

[1] The off-chip frequency is expected to increase for a small number of high-speed pins that will be used in combination with a large number of lower speed pins

[2] In 2001, high-speed serial communications transceiver devices are achieving chip-board frequencies of 3.125 GHz using CMOS, and 10 GHz using SiGe. In 2002 it is expected that 10 GHz transceivers will be fabricated using CMOS. 40 GHz SiGe devices are expected in 2003. The roadmap for higher levels of integration with wider bus widths, is shown in the High Frequency Serial Communications section in the Test chapter.

[3] The minimum number of wiring levels represents the interconnect metal levels, and the maximum number of interconnect wiring levels includes the Minimum number of wiring levels plus additional optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

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Table 5a Electrical Defects—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §	2,216	2,791	3,751	2,532	3,190	2,345	2,954
MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	1,395	1,395	1,395	1,395	1,395	1,395	1,395
# Mask Levels—MPU	29	31	33	33	33	35	35
# Mask Levels—DRAM	24	24	24	24	24	24	24

Table 5b Electrical Defects—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
WAS	DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §	3,722		2,954	3,722		2,954	2,233		3,545
IS	DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §	3,722	<u>2,353</u>	2,954	3,722	<u>2,353</u>	2,954	2,233	<u>2,803</u>	3,545
WAS	MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§	1,395		1,395	1,395		1,395	1,395		1,395
IS	MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§	1,395	<u>1,395</u>	1,395	1,395	<u>1,395</u>	1,395	1,395	<u>1,395</u>	1,395
WAS	# Mask Levels—MPU	35		35	35		37	39		39
IS	# Mask Levels—MPU	35	<u>35</u>	35	35	<u>37</u>	37	39	<u>39</u>	39
WAS	# Mask Levels—DRAM	26		26	26		26	26		26
IS	# Mask Levels—DRAM	26	<u>26</u>	26	26	<u>26</u>	26	26	<u>26</u>	26

Notes for Tables 5a and 5b

D_0 — defect density

§ DRAM Model—Cell factor (design/process improvement) targets are as follows

1999–2004/8× 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the “6” DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of “Moore’s Law” bits/chip from 2× every 1.5–2 years to 2×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

Table 6a Power Supply and Power Dissipation—Near-term Years [UPDATED](#)

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Power Supply Voltage (V)							
V _{dd} (high-performance)	1.2	1.2	1.1	1.1	1.1	1	1
V _{dd} (Low Operating Power, high V _{dd} transistors)	1	0.9	0.9	0.9	0.8	0.8	0.8
Allowable Maximum Power [1]							
WAS High-performance with heatsink (W)	149	158	167	180	189	200	210
IS High-performance with heatsink (W)	149	158	167	180	189	198	198
Cost-performance (W)	80	84	91	98	104	109	114
Battery (W)—(low-cost/hand-held)	2.1	2.2	2.3	2.4	2.5	2.6	2.7

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 6b Power Supply and Power Dissipation—Long-term Years [UPDATED](#)

Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node	hp45			hp32			hp22		
WAS DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
Power Supply Voltage (V)									
WAS V _{dd} (high-performance)	1		0.9	0.9		0.8	0.8		0.7
IS V _{dd} (high-performance)	1	1	0.9	0.9	0.9	0.8	0.8	0.7	0.7
WAS V _{dd} (Low Operating Power, high V _{dd} transistors)	0.7		0.7	0.6		0.6	0.5		0.5
IS V _{dd} (Low Operating Power, high V _{dd} transistors)	0.7	0.7	0.7	0.6	0.6	0.6	0.5	0.5	0.5
Allowable Maximum Power [1]									
WAS High-performance with heatsink (W)	218		240	251		270	288		300
IS High-performance with heatsink (W)	198	198	198	198	198	198	198	198	198
Cost-performance (W)	120		131	138		148	158		168
Battery (W)—(hand-held)	2.8		3	3		3	3		3

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 7a Cost—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	10.5	7.4	5.3	3.7	2.6	1.9	1.3
DRAM cost/bit at (packaged microcents) at production §	3.8	2.7	1.9	1.4	0.96	0.7	0.5
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	88	62	44	31	22	15.6	11.0
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	53	38	27	19	13.3	9.4	6.7
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	49	34	24	17	12	8.6	6.1
Cost-Per-Pin							
Test Cost							
Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—maximum	3	3	3	3	3	3	3
Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—minimum	1	1	1	1	1	1	2

Notes for Tables 7a and 7b

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years InTER-generation reduction rate model used; .55×/year InTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when InTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two to four years after introduction).

§ DRAM Model—Cell factor (design/process improvement) targets are as follows

1999–2004/8×; 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the “6” DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of “Moore’s Law” bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

InTER-generation chip size growth rate model target for Production-phase DRAMs is now “flat” at less than 140 mm², similar to the MPU model. This new flat-chip-size model target requires the bits/chip “Moore’s Law” model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Tables 1c and d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63%, which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above). The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm²/cost-performance at introduction; 140 mm²/cost-performance at production; 310 mm²/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 7b Cost—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
	Affordable Cost per Function ++									
WAS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93		0.46	0.33		0.16	0.12		0.06
IS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93	<u>0.66</u>	0.46	0.33	<u>0.23</u>	0.16	0.12	<u>0.08</u>	0.06
WAS	DRAM cost/bit (packaged microcents) at production §	0.34		0.17	0.12		0.06	0.042		0.021
IS	DRAM cost/bit (packaged microcents) at production §	0.34	<u>0.24</u>	0.17	0.12	<u>0.08</u>	0.06	0.04	<u>0.03</u>	0.02
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78		3.89	2.75		1.38	0.97		0.49
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78	<u>5.50</u>	3.89	2.75	<u>1.94</u>	1.38	0.97	<u>0.69</u>	0.49
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71		2.35	1.66		0.83	0.59		0.29
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71	<u>3.33</u>	2.35	1.66	<u>1.18</u>	0.83	0.59	<u>0.42</u>	0.29
WAS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.305		2.15	1.52		0.76	0.54		0.27
IS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.30	<u>3.04</u>	2.15	1.52	<u>1.08</u>	0.76	0.54	<u>0.38</u>	0.27
	Cost-Per-Pin									
	Test Cost									
WAS	Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—maximum	4		4	4		4	4		4
IS	Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—maximum	4	<u>4</u>	4	4	<u>4</u>	4	4	<u>4</u>	4
WAS	Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—minimum	2		2	3		3	4		4
IS	Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—minimum	2	<u>2</u>	2	3	<u>3</u>	3	4	<u>4</u>	4

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

Technology Node—The minimum half-pitch of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated circuits and is selected to define an ITRS Technology Node. For each Node, this defining metal half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other parameters are also important for characterizing IC technology. For example, in the case of microprocessors (MPUs), physical bottom gate length is most representative of the leading-edge technology level required for maximum performance. Each technology node step represents the creation of significant technology progress in metal half-pitch — approximately 70% of the preceding node, 50% of two preceding nodes.

Example: DRAM half pitches of 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, and 22 nm.

For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

An official 2003 ITRS metal half-pitch node indicator, “hpXX,” has been added to differentiate the ITRS definition from commercial technology generation numbers .

Moore’s Law—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a “self-fulfilling” prophecy, “Moore’s Law” has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore’s Law, there is a historically-based “corollary” to the “law,” which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every three years, as suggested by consensus DRAM and MPU models of the 2003 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market “tops-down” needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1Mbytes/2001). Logic functionality and L2 cache typically double every three-year generation.

High-performance MPU—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example two cores at 25Mt cores in 2001) with a large (example 4Mbyte/2001) level-two (L2) SRAM. Logic functionality and L2 cache typically double every three-year technology generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law ($2\times$ /two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology-node scaling ($.7\times$ linear, $.5\times$ area) is every three years, an additional device/process design improvement of $.8\times$ per two years must be achieved. This requirement represents a design-related (cell-area-factor) area-reduction improvement of at least -11% per year, and this design-related productivity improvement is in addition to the basic lithography-based area reduction of -21% per year (three-year node cycle).

The present 2003 ITRS consensus target for the rate of increase of DRAM bits/chip has increased from $2\times$ bits/chip every two years to $2\times$ /chip every two and half years average. This slower bits/chip growth is required due to the new consensus 2003 ITRS forecast of cell-area-factor improvement of only negative $4\text{--}6\%$ per year on average rather than the 2001 ITRS target of -7% per year average. This results in an average DRAM inTER-generation approximately flat chip-size growth. Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the 2003 ITRS MPU inTER-generation functionality model target is $2\times$ transistors/chip every technology node, in order maintain a flat chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The 2003 ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration-level manufacturing tools and processes. Historically, DRAM products have been demonstrated at $4\times$ bits-per-chip every four years at the leading-edge process technology node, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples. Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples ($<1K$). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at $2\times$ functionality per chip every two years (every technology node, in the case of MPUs). In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturer begins shipping volume quantities (initially, at least 10K/month) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (*Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume

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production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready 12–24 months prior to Production Ramp “Time Zero” [see Figure 2 in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1Gb/production, 4G/introduction, plus 512Mb/256Mb/128Mb/64Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm²)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the *ITRS* consensus models).

Functions/cm²—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2003 *ITRS*, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 63% at the production level, and less than 50–55% for smaller previous generation shrunk die at the high-volume ramp level).

DRAM Cell Area (μm²)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified *ITRS*-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 1999: A=8; square of the half-pitch, $f^2 = (180 \text{ nm})^2 = .032 \mu\text{m}^2$; cell area, $C = Af^2 = 0.26 \mu\text{m}^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E = 0.37 \mu\text{m}^2$; therefore, the 1 Gb Chip Size Area = $2^{30} \text{ bits} * 0.37 \text{e-}6 \text{ mm}^2/\text{bit} = 397 \text{ mm}^2$.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, 1.6×1.6=2.5, etc.).

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm² (High-performance ASIC, Auto Layout)—Number of transistors per cm² designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density

calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os—Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os—Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first 20K wafer-starts-per-month manufacturing facility.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd} —Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($\$/pin$)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

WORKING GROUP SUMMARIES

DESIGN

This update includes (a) a revised "General" design technology requirements (revised), with some new rows, and new explanations as footnotes for each row, but no changes in the values of existing rows, (b) a new design technology solutions table after the requirements table, which includes a definition of each row, (c) a new Design For Manufacturability (DFM) section with completely new content, and (d) an update of the verification section.

Table A Design For Manufacturability Challenges ADDED

<i>Challenges ≥ 50 nm/Through 2009</i>	<i>Summary Of Issues</i>
Mask cost	ALL—CAD tools that explicitly account for mask cost in their algorithms
Data explosion	ALL—RET tools that are explicitly aware of circuit metrics (timing, power)
Limitations of lithography hardware resolution	ALL—RET-aware CAD tools, radically-restricted design rules, including yield prediction and optimization
Voltage supply and threshold variability	ALL—Statistical analysis tools and flows that account for this variability, including yield prediction and optimization
BEOL Planarization and dimensional variability	ALL—Statistical design tools and flows that account for this variability; including yield prediction and optimization
Heterogeneous components (analog, MEMS, eRAM)	
Leakage as a limiter of manufacturability	ALL—Statistical leakage analysis and optimization tools
<i>Additional Challenges < 50 nm/Beyond 2009</i>	
Leakage as a limiter of manufacturability	ALL—Statistical leakage optimization tools
Uncontrollable CD and doping variability	ALL—Statistical parametric optimization tools
Extreme device and circuit variability	ALL—Architectures fundamentally resistant to variability (redundancy, ECC)
Critical need to integrate RET into design	ALL—RET-aware CAD tools
Package, system, and software variability	ALL—adaptable and redundant circuits that can adapt to these variations
BEOL planarization and dimensional variability	ALL—post-tapeout RET that interacts with synthesis, timing, and P&R

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory, ALL—all of these).

TEST

The 2004 update to the ITRS Test chapter is focused on minor corrections to previously published trend information and completion of the annualized long term tables. The most significant corrections occurred in the memory tables to eliminate portions of missing data from the 2003 revision. The modifications contained in this update do not represent fundamental changes in the direction of test in the industry.

ITWG activities have shifted to the 2005 chapter revision. In 2005 an effort will be made to reduce the number of table line items significantly by eliminating entries that do not show significant trending that will drive technology development for equipment or methods. In addition, the ITWG is reviewing proposals to merge some of the sections into broader topic categories to better focus on the key challenges - such as the merging of microprocessor, ASIC, and microcontroller topics into a single "Logic Test" section as a possible example. The purpose of this reorganization of chapter content is intended to focus ITWG activities on the emerging key challenges in the test area.

Table 23a Test and Test Equipment Difficult Challenges—Near-term

<i>Five Difficult Challenges ≥45 nm/Through 2010</i>	<i>Summary of Issues</i>
High-speed Device Interfaces	A major roadblock will be the need for high frequency, high pin count probes and test sockets; research and development is urgently required to enable cost-effective solutions with reduced parasitic impedence. High-speed serial interface speed and port count trends will continue to drive high-speed analog source/capture and jitter analysis instrument capability for characterization. DFT/DFM techniques must be developed for manufacturing. Device interface circuitry must not degrade equipment bandwidth and accuracy, or introduce noise, especially for high-frequency differential I/O and analog circuits.
Highly Integrated Designs	Highly structured DFT approaches are required to enable test access to embedded cores. Individual cores require special attention when using DFT and BIST to enable test. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever-increasing instrument capability trends. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits. DFT must enable test reuse for reusable design cores to reduce test development time for highly complex designs.
Reliability Screens	Existing methodologies are limited (burn-in versus thermal runaway, IDDQ versus background current increases). Research is required to identify novel infant mortality defect acceleration stress conditions
Manufacturing Test Cost	Test cell throughput enhancements are needed to reduce manufacturing test cost. Opportunities include massively parallel test, wafer-level test, wafer-level burn-in, and others. Challenges include device interfacing/contacting, power and thermal management. Device test needs must be managed through DFT to enable low-cost manufacturing test solutions; including reduced pin count test, equipment reuse, and reduced test time. Automatic test program generators are needed to reduce test development time. Test standards are required to enable test content reuse and manufacturing agility.
Modeling and Simulation	Logic and timing accurate simulation of the ATE, device interface, and DUT is needed to enable pre-silicon test development and minimize costly post-silicon test content development/debug on expensive ATE. High-performance digital and analog I/O and power requirements require significant improvements to test environment simulation capability to ensure signal accuracy and power quality at the die. Equipment suppliers must provide accurate simulation models for pin electronics, power supplies, and device interfaces to enable interface design.

Table 23b Test and Test Equipment Difficult Challenges—Long-term

<i>Five Difficult Challenges <45 nm/Beyond 2010</i>	<i>Summary of Issues</i>
DUT to ATE interface	Probing capability for optical and other disruptive technologies Support for massively parallel test—including full wafer contacting Decreasing die size and increasing circuit density are driving dramatic increases in die thermal density. This problem is further magnified by the desire to enable parallel test to maximize manufacturing throughput. New thermal control techniques will be needed for wafer probe and component test. DFT to enable test of device pins not contacted by the interface and test equipment.
Test Methodologies	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years). New test methods for control and observation are needed. Tests will need to be developed utilizing the design hierarchy. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever increasing instrument capability trends Logic BIST techniques must evolve to support new fault models, failure analysis, and deterministic test. EDA tools for DFT insertion must support DFT selection with considerations for functionality, coverage, cost, circuit performance and ATPG performance.
Defect Analysis	Defect types and behavior will continue to evolve with advances in fabrication process technology. Fundamental research in existing and novel fault models to address emerging defects will be required. Significant advances in EDA tools for ATPG capacity and performance for advanced fault models and DFT insertion are required to improve efficiency and reduce design complexities associated with test.
Failure Analysis	Realtime analysis of defects in multi-layer metal processes is needed. Failure analysis methods for analog devices must be developed and automated. Transition from a destructive physical inspection process to a primarily non-destructive diagnostic capability. Characterization capabilities must identify, locate, and distinguish individual defect types.
Disruptive Device Technologies	Develop new test methods for MEMS and sensors. Develop new fault models for advanced/disruptive transistor structures.

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

The 2004 update for the Process Integration, Devices and Structures (PIDS) section of the ITRS has minor changes and corrections from the 2003 edition. The most notable change is that in the long-term technology requirements tables, the years 2011, 2014, and 2017 have been added, so that all years from 2010 through 2018 are now included. As expected, the parameter values for these added years are generally close to midway between the values for the previous and succeeding years. In Figure 23, which is for low standby power logic, the curve for maximum allowed gate leakage current density (labeled “J_{g,limit}”) has been corrected. In the 2003 edition, this curve was low by a factor of 2 to 3. Even with the correction, the implication of the figure is unchanged, that oxynitride gate dielectric is projected to be unable to meet the gate leakage current limits by 2006.

Table 46a Process Integration Difficult Challenges—Near-term

<i>Difficult Challenges ≥ 45 nm/Through 2010</i>	<i>Summary of Issues</i>
1. High-performance applications: meeting performance and power dissipation requirements for highly scaled MOSFETs	Cost effectiveness, process control, and reliability of very thin oxynitride gate dielectrics, especially considering the high gate leakage Difficulty in controlling short-channel effects for highly scaled devices Negative impact of high channel doping needed for highly scaled devices. Also, the difficulty in controlling threshold voltage due to statistical fluctuations in the doping Need to reduce series S/D parasitic resistance Controlling static power dissipation in the face of rapidly increasing leakage: architecture and circuit design improvement and innovation will be needed.
2. Low-power applications: meeting performance and leakage requirements for highly scaled MOSFETs	Early availability of manufacturing-worthy high-κ gate dielectrics is necessary to meet stringent gate leakage and performance requirements. Slow scaling of V_{dd} for low standby power logic will make overall device scaling difficult. Rapid scaling of V_{dd} for low operating power logic will make overall device scaling difficult.
3. Assuring the reliability and implementing into manufacturing of multiple material, process, and structural changes in a relatively short period of time	Multiple material changes projected: high-κ gate dielectric, metal gate electrodes, strained Si, nickel silicide by 2008 or so Elevated S/D (selective epi) Ultra-thin body (UTB) SOI by 2008 or so, followed by multiple-gate structures. Near mid-gap metal gate electrodes will be desirable to set the threshold voltage for UTB SOI. Difficulty in ensuring reliability of all these new materials, processes, and structures in a timely manner

Table 46a Process Integration Difficult Challenges—Near-term (continued)

4. Implementation of DRAM, SRAM, and high-density nonvolatile memory (NVM) for scaled technologies	DRAM main issues—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities with scaling. Also, difficult lithography and etch issues with scaling NVM, flash—Scaling of tunnel dielectric and interpoly dielectric involves many complex tradeoffs. Dielectric material properties and dimensional control are key issues NVM, FeRAM—Ferroelectric material properties and dimensional control. Sensitivity to IC processing temperatures and conditions NVM, SONOS—ONO stack dimensions and material properties, including nitride layer trap distribution in space and energy NVM, MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions
5. High-performance and low-cost RF and analog/mixed-signal solutions	Signal isolation Optimizing RF/analog CMOS devices with scaled technologies: mismatch, $1/f$ noise, and leakage with high-κ gate dielectrics High density integrated passive element scaling and use of new materials: Q-factor value for inductors; matching and linearity for capacitors Reduced power supply voltages: degradation in SNR (signal-to-noise ratio) and signal distortion performance Reduced device breakdown voltage in scaled technologies High-frequency devices with increased operating voltage for base station applications Compound semiconductor substrates with good thermal dissipation and process equipment for fabrication at low cost See section on RF and A/MS Technologies for Wireless Communications for detailed discussion of these issues

Table 46b Process Integration Difficult Challenges—Long-term

<i>Difficult Challenges < 45 nm/Beyond 2010</i>	<i>Summary of Issues</i>
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate, ultra-thin body [UTB] MOSFETs) with lightly doped body will be needed to effectively scale MOSFETs to well under 20 nm gate length (L_g). Most likely, advanced material solutions such as strained Si (enhanced mobility) channels, elevated source/drain, high-κ gate dielectric, metal gate electrode, etc., will be utilized along with the advanced non-classical CMOS Particularly for the highly scaled UTB MOSFETs required towards the end of the Roadmap, with body thickness well under 10 nm, electrical performance and the impact of quantum effects are not well understood To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced carrier saturation velocity appears to be needed See Emerging Research Devices section for more detail.
7. Dealing with atomic-level fluctuations and statistical process variations in sub-20 nm MOSFETs	Fundamental issues of atomic-level statistical fluctuations for sub-20 nm MOSFETs are not completely understood, including the impact of quantum effects.
8. Identifying, selecting, and implementing new memory structures	Highly scaled, dense, fast, non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness, attaining the very low leakage currents that will be required, and reducing the cell area factor All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc.) are currently unclear.
10. Toward the end of the Roadmap or beyond, identification, selection, and implementation of advanced, beyond-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of beyond-CMOS devices need to extend well beyond CMOS limits. Beyond-CMOS devices need to integrate into a CMOS platform. Integration of the two may be difficult, especially for mixed signal. See Emerging Research Devices sections for more discussion and detail.

EMERGING RESEARCH DEVICES

Table 58 Emerging Technologies Difficult Challenges

<i>Difficult Challenges ≥45 nm/Through 2009</i>	<i>Summary of Issues</i>
Implementation into manufacturing of non-classical MOSFET device structures integrated with new materials and processes (for example, a strained silicon channel integrated with a new high-κ gate dielectric material)	Selection of most promising device structure(s) and/or materials technologies ["Technology Booster(s)"] to sustain the required annual 17% increase in performance Introduction of two or more "Technology Booster" options (material, process, and/or device structure changes) simultaneously in a single node
Development and implementation into manufacturing of a non-volatile memory technology combining the best performance features of both volatile and non-volatile memory technologies for both stand-alone and embedded applications	Realization of a manufacturable, cost-effective fabrication technology for electrically accessible high-speed, high-density non-volatile RAM integrable with the fabrication process flow for CMOS logic
<i>Difficult Challenges <45 nm/Beyond 2009</i>	
Toward the end of CMOS scaling or beyond, discovery, reduction to practice, and implementation into manufacturing of novel, non-CMOS devices and architectures integrated (monolithically, mechanically, or functionally) with a CMOS platform technology	Discovery and reduction to practice of new information processing technologies integrable with silicon CMOS Discovery and reduction to practice of new, low-cost methods of manufacturing novel information processing technologies

Table ERM-1 Emerging Research Materials Difficult Challenges ADDED

<u><i>Difficult Challenges <32 nm/Beyond 2009</i></u>	<u><i>Summary of Issues</i></u>
<u>The characterization of critical material properties at the nanometer scale for both charge transport and non-charge transport based devices is very limited and may hinder our ability to improve materials properties.</u>	<u>The primary tools to extract properties at the nanometer scale are SEM, TEM, AFM, and STEM, and these measure structural information, so critical materials properties are not measured at these dimensions.</u> <u>Characterization of the 2D/3D chemical, structural, electronic, and atomic bonding at the nanometer scale is very difficult and not possible in some cases.</u> <u>At the nanometer scale, the separation of "bulk" and interface properties will be very difficult, because the surface becomes a large part of the material.</u>
<u>As materials become smaller, identifying contact materials that don't damage the bonding in the molecule or material may limit the ability to fabricate functional devices.</u>	<u>Metals that form contacts chemically react with the material and this generates energy that can break other bonds.</u> <u>Very few metals form bonds to carbon and these usually form carbides, which may be more resistive materials, and this may limit the contact resistance to molecules and carbon nanotubes.</u>
<u>For modeling and simulation to predict the right trends of properties of nanometer sized materials, correct physical models must be developed.</u>	<u>Modeling tools are very inaccurate in predicting excited states and these are critical in modeling transport through materials or across interfaces.</u> <u>Correlation effects become significant at small material size and these are not modeled</u>

RF AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

Analog and Mixed Signal: The technology requirements are now aligned for analog speed devices with the LSTP roadmap instead of, as in the past, with the LOP roadmap. It is becoming more challenging to keep a constant ratio of transconductance gm to drain conductance gds for high performance analog devices in new technologies. The challenges for reducing $1/f$ noise in high- k gate dielectrics are relaxed to a color coding of "yellow" from "red." However, $1/f$ noise in high- k gate dielectrics still remains challenging. The published reports about solutions for high density capacitors meeting density, leakage, and matching specifications suggested changes to capacitor color coding for the 2004 ITRS update from red to yellow for the years 2013 to 2016.

RF Transceivers: Similar to the Near Term Table, a lag between RFCMOS gate length and BiCMOS gate length now occurs in the Long Term Table. For RFCMOS, the technology requirements maintained one-year lag from the LSTP CMOS roadmap.

Power Amplifiers & Power Management: The major trends appear to have been correctly anticipated in 2003 for handsets. The first two RFCMOS Dual Band GSM power amplifiers (PAs) were sampled by cellular customers in 2004. These PAs are not expected to be players in the market until 2005. However, RFCMOS PAs could play a major role in 2006. The success of RFCMOS PA's may erode price margins at a faster rate than anticipated. Multi-band cellular SiGe PAs also are being sampled. Highly integrated modules with multi-layer laminates of low temperature cindered ceramics (LTCC) are dramatically reducing total RF front-end area. The cost (\$\$/Watt) for base station PAs will decrease more rapidly than shown in the 2003 Roadmap and are expected to reach \$0.40 per watt in 2008. Saturated power density (W/mm) of all technologies will increase more rapidly and will reach 1.4 W/mm, 1.8 W/mm, 3 W/mm, and 5 W/mm by 2008 for LDMOS, GaAs, SiC, and GaN, respectively. Manufacturing solutions now exist for 28V GaAs FET's, 60W SiC FET's, and 28 V GaN FET's. Linear operation is expected to achieve less than half the RF power of saturated operation. In the 2003 Roadmap, linear operation was expected to achieve half the RF power of saturated operation.

Millimeter Wave (10-100GHz): There are no major changes for the 2004 Update. InP HBTs are expected to advance more quickly due to aggressive R&D funding than they were predicted to do so in the 2003 ITRS. The 2005-2006 color coding for all InP HBT device requirements are changed from yellow to white. Also, the 2007-2008 figures of merit for device f_T and f_{MAX} are more aggressive. Copper interconnects are expected to be introduced in 2007. The use of today's gold and aluminum interconnects is expected to continue until at least 2009.

FRONT END PROCESSES

The 2004 FEP ITRS update presents a refinement of the 2003 Roadmap in several areas. These areas include timing of 450mm wafer introduction, accelerated introduction of SOI, back surface particle metrics, gate CD tolerance, gate dielectric leakage current, and the co-introduction of metal gate electrodes and high-k gate dielectrics. In addition, other typographical mistakes and inconsistencies have been corrected.

The projected introduction of 450mm wafers to manufacturing was not consistent across all working groups in the 2003 ITRS. This will be addressed and corrected in 2005. In the meantime, additional notes identifying this issue have been added to Table 68b and to the footnotes of Table 69.

Due to an improved outlook and accelerated introduction for SOI, the qualification/ and preproduction date for SOI has been moved to 2004 in figure 44, “Starting Materials Potential Solutions.”

Following a survey of several IC fabs, the surface preparation team was able to add experience-based metrics for back surface particles that now appear in Tables 70a and 70b. The surface preparation team will continue to study this area and attempt to introduce yield-model-based metrics in 2005.

An industry survey was conducted in 2004 on the partitioning of gate CD tolerance. The survey revealed several important pieces of information: first, most manufacturers are not currently able to meet the 10% overall CD tolerance on the physical gate length; nor are they able to achieve the “ITRS-required” partitioning of this tolerance between litho and etch. Despite the fact that very few are able to achieve the tolerance, there is still a consensus that the “requirement” should be maintained, with different companies employing a work-around to be successful. Accordingly 2004 update reflects the same absolute tolerances and partitioning of those tolerances as the 2003 roadmap even though it is widely recognized that they are mostly not being met. The survey also revealed that the trimming of gate photoresist is more aggressive than is reflected by values in the table; however, dimensions in the photoresist are higher than the table values in many instances. At this writing, proposals are being considered for the 2005 roadmap that will relax the gate dimensions in exposed photoresist, while maintaining the same final, after-trim dimensions.

In the area of gate dielectric leakage currents, clarifications were added to table 71 and the associated footnotes. Allowable gate dielectric leakage is now specified at 100°C and as a multiple of the device off-state leakage.

The footnotes to table 71 point out that there is a growing consensus that both high k and metal gates are likely to be introduced simultaneously, rather than staggered.

The expectation of higher mobility channels, built into the 2003 roadmap, came to fruition in 2004, validating the EOT values presented in 2003. In the 2003 ITRS, mobility enhanced channels allowed a slower reduction of EOT, thereby delaying the introduction date of high k.

Table 68a Front End Processes Difficult Challenges—Near-term [UPDATED](#)

	MPU/ASIC Physical Gate Length ≥ 20 nm/ Through 2009	Summary of Issues
WAS	New gate stack processes and materials	Extension of oxynitride gate dielectric materials to < 1.0 nm E.O.T for high performance MOSFETs, consistent with device reliability requirements Introduction and process integration of high-κ gate stack materials and processes for high performance, low operating and low standby power MOSFETs CMOS integration of enhanced channel mobility, e.g., strained layers Control of boron penetration from doped polysilicon gate electrode Minimized depletion of dual-doped polysilicon electrodes Introduction of dual metal gate electrodes with appropriate work function (toward end of period) Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization
IS	New gate stack processes and materials	Extension of oxynitride gate dielectric materials to < 1.0 nm E.O.T for high performance MOSFETs, consistent with device reliability requirements Introduction and process integration of high-κ gate stack materials and processes for high performance, low operating and low standby power MOSFETs CMOS integration of enhanced channel mobility, e.g., strained layers Control of boron penetration from doped polysilicon gate electrode <u>Control of silicon loss at spacer etch and gate etch needs to be much tighter on thin SOI and SiGe wafers, where the total silicon thickness is 20-50 nm</u> Minimized depletion of dual-doped polysilicon electrodes <u>Removal of high K dielectric without loss of the underlying silicon, especially in the case of SOI or non planar devices</u> Introduction of dual metal gate electrodes with appropriate work function (toward end of period) Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization
	Critical dimension and effective channel length (L_{eff}) control	Control of gate etch processes that yield a physical gate length that is smaller than the feature size printed in the resist, while maintaining $<10\%$ overall 3-sigma control of the combined lithography and etch processes Control of profile shape, edge roughness, line and space width for isolated as well as closely-spaced fine line patterns Control of self-aligned doping processes and thermal activation budgets to achieve L_{eff} control Maintenance of CD and profile control throughout the transition to new gate stack materials and processes CD and etch metrology Site flatness to ensure effective lithographic printing

Table 68a Front End Processes Difficult Challenges—Near-term [UPDATED](#) (continued)

MPU/ASIC Physical Gate Length ≥ 20 nm/ Through 2009	Summary of Issues
Introduction and CMOS integration of new memory materials and processes	Development and introduction of very high-κ DRAM capacitor dielectric layers Migration of DRAM capacitor structures from silicon-insulator-metal to metal-insulator-metal Integration and scaling of FeRAM ferroelectric materials Scaling of Flash inter-poly and tunnel dielectric layers may require high κ Limited temperature stability of high-κ and ferroelectric materials challenges CMOS Integration
Surfaces and interfaces—structure, composition, and contamination control	Contamination, composition, and structure control of channel/gate dielectric interface as well as gate dielectric/gate electrode interface Interface control for DRAM capacitor structures Maintenance of surface and interface integrity through full-flow CMOS processing Statistically significant characterization of surfaces having extremely low defect concentrations for starting materials and pre-gate clean surfaces
Scaled MOSFET dopant introduction and control	Doping and activation processes to achieve shallow source/drain regions having parasitic resistance that is less than ~ 17–33% of ideal channel resistance ($=V_{dd}/I_{on}$) Control of parasitic capacitance to achieve less than ~ 23–29% of gate capacitance, consistent with acceptable I_{on} and minimum short channel effect Achievement of activated dopant concentration greater than solid solubility in dual-doped polysilicon gate electrodes Formation of continuous self-aligned silicide contacts over shallow source and drain regions Metrology issues associated with 2D dopant profiling

Table 68b Front End Processes Difficult Challenges—Long-term [UPDATED](#)

	MPU/ASIC Physical Gate Length <20 nm/ Beyond 2009	Summary of Issues
WAS	Continued scaling of planar CMOS devices	Higher κ gate dielectric materials including temperature constraints Metal gate electrodes with appropriate work function Sheet resistance of clad junctions CD and Leff control Chemical, electrical, and structural characterization
	Introduction and CMOS integration of non-standard, double gate MOSFET devices	Devices are needed starting from 2011 and may be needed as early as 2007 (this is a backup for high- κ materials and metal gates on standard CMOS) Selection and characterization of optimum device types CMOS integration with other devices, including planar MOSFETs. Introduction, characterization, and production hardening of new FEP unit processes Device and FEP process metrology Increased funding of long term research Role of SOI utilization (and structural configuration) for advanced non-classical CMOS
IS	Introduction and CMOS integration of non-standard, double gate MOSFET devices	Devices are needed starting from 2011 and may be needed as early as 2007 (this is a backup for high-k materials and metal gates on standard CMOS) Selection and characterization of optimum device types. CMOS integration with other devices, including planar MOSFETs Introduction, characterization, and production hardening of new FEP unit processes. Device and FEP process metrology Increased funding of long term research Role of SOI and strained silicon utilization (and structural configuration) for advanced non-classical CMOS
WAS	Starting silicon material alternatives greater than 300 mm diameter require the start of wafer manufacturing development in year 2003	Need for future productivity enhancement dictates the requirement for a next generation, large silicon substrate material Historical trends suggest that the new starting material have nominally twice the area of present generation substrates, e.g., 450 mm. Economies of the incumbent Czochralski crystal pulling, wafer slicing, and polishing processes are questionable beyond 300 mm; research is required for a cost-effective substrate alternative to bulk silicon If 450 mm wafers are to become available for production in 2011 as currently forecasted, wafer-manufacturing development should be implemented eight years earlier, e.g., 2003.
IS	Starting silicon material alternatives greater than 300 mm diameter require the start of wafer manufacturing development in year 2005	Need for future productivity enhancement dictates the requirement for a next generation, large silicon substrate material Historical trends suggest that the new starting material have nominally twice the area of present generation substrates, e.g., 450 mm. Economies of the incumbent Czochralski crystal pulling, wafer slicing, and polishing processes are questionable beyond 300 mm; research is required for a cost-effective substrate alternative to bulk silicon. If 450 mm wafers are to become available for production in 2011 as currently forecasted, wafer manufacturing is already behind schedule and must be implemented in 2004-2005. Enhanced coordination is required amongst Starting Materials, Factory Integration, Yield Enhancement and the IRC to more effectively assess the anticipated onset of 450 mm use.

Table 68b Front End Processes Difficult Challenges—Long-term [UPDATED](#) (continued)

<i>MPU/ASIC Physical Gate Length <20 nm/ Beyond 2009</i>	<i>Summary of Issues</i>
New memory storage cells, storage devices, and memory architectures	Scaling of DRAM storage capacitor beyond $6F^2$ Further scaling of Flash memory interpoly and tunnel oxide thickness FeRAM storage cell scaling Introduction of new memory types and storage concepts (Candidates—MRAM, phase-change memory for 2010, and single electron, molecular, nano-floating products beyond 2010)
Surface and interface structural, contamination, and compositional control	Achievement and maintenance of structural, chemical, and contamination control of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface Metrology and characterization of surfaces that may be horizontally or vertically oriented relative to the chip surface Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface

LITHOGRAPHY

In the 2004 update of the ITRS Lithography tables, no significant changes were made to the coloring or values in the overall lithography requirements tables other than adding a definition of overlay. For the long term, solutions are not known to reach the overall lithographic requirements for resolution combined with adequate overlay or CD control for any circuit type with any known lithographic technology. The lithography working group has participated in discussion with working groups developing other chapters to define CD control requirements. The US and Japan working groups separately conducted simulation studies that concluded that $<4\text{nm } 3\sigma$ CD control has no known solutions with any technology presently being developed. The simulations also predict that if the gate length in resist were increased, CD control would be improved. However, this change would require larger post-development linewidth reduction using reactive ion etching or other processes.

Significant changes were made to the tables on difficult challenges and potential solutions. In developing the 2004 update, working group members defined new criteria for evaluating near-term potential solutions. Solutions shown in the table for the present and next two nodes must address leading edge requirements in at least two geographic regions, and all infrastructure including resist and mask must be ready for the timing of the node. Solutions for three nodes or more in the future are somewhat more broad ranging and inclusive to encourage continued innovation. With these criteria 193nm wavelength exposure systems, including 193nm immersion systems, became dominant solutions for the next two nodes; in addition, 157-nm wavelength exposure was only listed with immersion as a less likely option. Furthermore, immersion lithography appears as potential solution at the 32-nm and 22-nm nodes. In the difficult challenges tables, stronger emphasis was placed on challenges related to immersion lithography. Continued emphasis was placed on challenges for implementing cost-effective post-optical lithography solutions.

Many individual parameters for masks and resist were evaluated, and colors or values were changed. In the tables of mask requirements, the scaling of data volume requirements was delayed by one year. Manufacturing solutions are also available for mask protection and for achieving phase and transmission control for attenuated phase shift masks in 2007 since the use of 157-nm wavelength technology is not likely before the 45-nm node. Pellicles and phase-shifting materials are mature for use with 193-nm wavelength exposure. Minor changes were made to the EUV and EPL mask tables. In the resist tables, thickness requirements for single layer and ultrathin layer resist strategies were merged since resist thickness will need to be less than 300nm to maintain aspect ratio values where the resist doesn't collapse. The range of resist dose for 193-nm wavelength exposure was increased, and the dose values for electron beam exposure were adjusted to account for sensitivity differences in resist for exposure with low and high beam energies. Furthermore, the definition of line width roughness was adjusted to account for metrology precision.

Table 76 Lithography Difficult Challenges UPDATED

WAS	Five Difficult Challenges/ ≥ 50 nm Through 2009	Summary of Issues
	Optical masks with features for resolution enhancement and post-optical mask fabrication	--Registration, CD control, defectivity, and 157 nm pellicles; defect free multi-layer EUV substrates or EPL membrane masks --Equipment infrastructure (writers, inspection, repair)
IS	Optical masks with features for resolution enhancement and post-optical mask fabrication	<u>--Registration, CD control, defect control for optical masks</u> <u>--Development of defect free multi-layer EUV mask blanks or EPL membrane masks</u> <u>--Equipment infrastructure (writers, inspection, repair)</u> <u>--Data volume</u>
WAS	Cost Control and Return on Investment (ROI)	--Achieving constant/improved ratio of tool cost to throughput over time --Cost-effective resolution enhanced optical masks and post-optical masks --Sufficient lifetimes for the technologies --Resources for developing multiple technologies at the same time --High output, cost-effective, EUV light source
IS	Cost Control and Return on Investment (ROI)	<u>--Achieving constant/improved ratio of exposure related tool cost to throughput over time</u> <u>--Cost-effective resolution enhanced optical masks and post-optical masks</u> <u>--Sufficient lifetimes for exposure tool technologies</u> <u>--Resources for developing multiple technologies at the same time</u> <u>--ROI for small volume products</u>
WAS	Process Control	--Processes to control gate CDs to less than 1.8 nm (3 sigma) --New and improved alignment and overlay control methods independent of technology option to < 19 nm overlay --Accuracy of OPC
IS	Process Control	<u>--Processes to control gate CDs to less than 4nm (3 sigma)</u> <u>--New and improved alignment and overlay control methods independent of technology option to < 19 nm overlay</u> <u>--Accuracy of OPC, especially in presence of polarization effects</u> <u>--Control of flare in exposure tool</u> <u>--Lithography friendly design and design for manufacturability</u>
WAS	Resists for ArF, Immersion Lithography and F ₂	--Outgassing, LER, SEM-induced CD changes, defects ≥ 30 nm.
IS	<u>Resists for 193nm and 193nm immersion lithography</u>	<u>--Outgassing and leaching during immersion</u> <u>--Reduction of line edge and line width roughness</u> <u>--Finding and eliminating defects >30nm in size</u> <u>--Reducing SEM-induced CD changes</u>
~~Delete~~	~~CaF₂~~	~~--Yield, cost, quality~~
IS	<u>Defect control</u>	<u>--Control of defects caused in immersion environment</u>

Table 76 Lithography Difficult Challenges (continued)

	Five Difficult Challenges/ < 45 nm Beyond 2010	
WAS	Mask Fabrication and Process Control	--Defect-free NGL masks --Equipment infrastructure (writers, inspection, repair) --Mask process control methods
IS	Mask Fabrication and Process Control	<u>--Defect-free NGL masks, especially for 1X masks for nanoimprint and EUVL mask blanks free of printable defects</u> <u>--Timeliness and capability of mask equipment infrastructure (writers, inspection, repair), especially for 1X masks</u> <u>--Mask process control methods and yield enhancement</u> <u>--Pellicles for 157nm immersion and protection of EUVL masks from defects without pellicles</u>
WAS	Metrology and Defect Inspection	--Capability for critical dimensions down to 7 nm and metrology for overlay down to 7.2 nm, and patterned wafer defect inspection for defects < 30 nm
IS	Metrology and Defect Inspection	<u>--Resolution and precision for critical dimension measurement down to 7 nm, including metrology for 2.2nm 3 sigma line width roughness</u> <u>--Metrology for overlay down to 7.2 nm</u> <u>--Defect inspection for patterned wafers for defects < 30 nm</u>
WAS	Cost Control and ROI	--Achieving constant/improved ratio of tool cost to throughput --Development of cost-effective post-optical masks --Achieving ROI for industry with sufficient lifetimes for the technologies
IS	<u>Cost Control and return on investment (ROI)</u>	<u>--Achieving constant/improved ratio of exposure related tool cost to throughput</u> <u>--Development of cost-effective optical and post-optical masks</u> <u>--Achieving ROI for industry with sufficient lifetimes for exposure tool technologies and ROI for small volume products</u>
WAS	Gate CD Control Improvements, Process Control, Resist Materials	--Development of processes to control gate CDs < 1 nm (3 sigma) with appropriate line-edge roughness --Development of new and improved alignment and overlay control methods independent of technology option to < 7.2 nm overlay
IS	Gate CD Control Improvements, Process Control, Resist Materials	<u>--Development of processes to control gate CDs < 4 nm (3 sigma) with appropriate line-edge roughness</u> <u>--Development of new and improved alignment and overlay control methods independent of technology option to < 7.2 nm overlay, especially for nanoimprint</u> <u>--Process control and design for low k1 lithography</u> <u>--Resists with high index of refraction, high index fluids and high index optical materials to extend optical immersion to its limits</u> <u>--Limits of chemically amplified resist sensitivity for <50-nm linewidths due to acid diffusion length</u>
WAS	Tools for Mass Production	--Optical and NGL exposure tools capable of meeting requirements of the Roadmap --EUV sources with power sufficient for high throughput
IS	Tools for Mass Production	<u>--Optical and NGL exposure tools capable of meeting requirements of the ITRS</u> <u>--High output, cost-effective EUV sources</u> <u>--CaF2 cost, yield, and quantity for 157nm immersion</u>

INTERCONNECT

In general the 2004 ITRS Interconnect requirements tables will change very little from the numbers published in 2003. However, there are additions and expansions of some metrics that are intended to clarify specific interconnect issues.

- There has been further clarification of what is meant by “Metal 1” as opposed to “local wiring.” In the latest chapter, the deteriorating resistivity of copper wires, as linewidth decreases, is highlighted.
- For Logic, additional Cu resistivity numbers are being added to reflect the effect of surface or sidewall scattering. A model, which incorporates resistivity of copper $\rho_o = \text{constant } 1.9 \mu\Omega\text{-cm}$ at 300 K, a mean free path of charge carriers $\lambda = 3.4 \times 10^{-6} \text{cm}$ (34nm), a wire width W (cm), a probability for reflection of electrons at the grain boundaries of 0.2, and the portion, p , of electrons specularly reflected from the walls (surface or interface), has been used to generate a series of new metrics in the Technology requirements tables (81a and 81b). The new metrics tabulate the impact to line resistivity at; Metal 1, intermediate, and global wiring. In these tables, interconnect delay (ps) is calculated for a one mm copper wire, assuming width dependent scattering (as described above) and a conformal barrier of thickness specified in the table. For the first time in the past 10 years, the low κ portion of the roadmap was unaltered (κ value targets not delayed) with respect to the prior edition. Small changes were made to the shading of the boxes for bulk and effective dielectric constant over the next five years, recognizing that materials that deliver an effective $\kappa = 2.7$ are in production today, and those material systems that will deliver an effective $\kappa = 2.4$ are expected to be available with manufacturable solutions in the next three years.
- The proposed changes for DRAM are relatively minor and center on the contacts. There are some changes in specific via and contact resistivity, with the contact A/R rising to >20 in 2018. This is now a “red” challenge associated with 16 nm DRAM half pitch. Cu has been delayed to 2007. The need to distinguish the requirements for embedded, Flash, and traditional DRAM was identified by the committee, but will not be addressed until the next major revision in 2005.
- In the Interconnect surface cleans tables, the notes clarifying the contributors to damage due to rework, strip, and clean, have been updated.

In assessing the Interconnect roadmap as a whole, however, it still becomes almost entirely “red bricks” (red = “no known solution”) by the end of this decade. No new discoveries or major breakthroughs have occurred in the year since closing the 2003 roadmap to change the outlook.

Table 80 *Interconnect Difficult Challenges*

<i>Five Difficult Challenges ≥45 nm/Through 2009</i>	<i>Summary of Issues</i>
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures compatible with new materials and processes*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/package architecture design optimization tool.
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Three-dimensional control (3D CD) of interconnect features (with its' associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
<i>Five Difficult Challenges <45 nm/Beyond 2009</i>	<i>Summary of Issues</i>
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control (3D CD) of interconnect features (with its' associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual-Damascene metal structures and DRAM at nano dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address global wiring scaling issues*	Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

* Top three challenges

FACTORY INTEGRATION

The International Technology Roadmap for Semiconductors (ITRS) is a 15 year roadmap that analyzes the industry's difficult challenges and technology requirements and then formulates potential solutions to meet these needs. The pace of technology is governed by the desire to stay on Moore's law, reduce cost per function by 30% per year [historic norms], and deliver new and compelling IC devices that continue our industry's growth.

While most of the ITRS focuses on process technology, the objective of the Factory Integration chapter is to ensure that our factories fully integrate physical and data elements of the factories to enable the development and high volume running of these process technologies so that the right products are made in the right volumes on schedule, while meeting cost targets. Historically, cost per function has been reduced through a technology advances such as device feature size reductions, yield improvement to near 100% and wafer size increases (i.e. 300mm wafers). It is expected that improvements in manufacturing productivity will play an even greater future role in reducing time to money and getting the most out of the factory investment. The need for future break-through technologies and capabilities that radically improve semiconductor factory design and manufacturing has never been greater. The scope of factory integration covers operations, AMHS, information systems, facilities and equipment in the fab area.

The focus for the FI team this year is to review difficult challenges, update technology requirements table, potential solutions table and to identify key focus areas to work on. For year 2004, the difficult challenges remained the same and most of the technology requirements and potential solutions table were unchanged except for small changes. However, the team identified the following 9 focus areas including AMC, 450mm wafer transition, etc.:

2004 ITRS FI focus areas:

- Airborne Molecular Contamination (AMC) Implications at < 45nm process technologies (Now → 2006)
- Implications of Relaxed Fab Facility Cleanliness (Now →)
- Litho EUV: Design for Manufacturability (2006 → 2010?)
- Fab Point of Use vs. Bulk Systems (Now →)
- Rapid Equipment Install and Qualification (Now →)
- Integrated Metrology Guidelines (Now →)
- Wafer and Unit Traceability from Fab through Packaging (Now →)
- "Proactive Visual" manufacturing (Now →)
- 450mm Wafer Size Transition (2005 → 2012)

The team is currently working on selecting top 3-4 focus areas in order to put together sub-teams to define the impact of these focus areas on FI and also on other cross-cut ITRS chapters.

Table 84a *Factory Integration Difficult Challenges—Near-term*

<i>Difficult Challenges ≥ 45 nm/Through 2009</i>	<i>Summary of Issues</i>
Responding to Rapidly Changing, Complex Business Requirements	Many new and co-existing business models including IDM, Foundry, Joint Ventures, Collaborations, other Outsourcing, etc Increased expectations by customers for faster delivery of new and volume products Need for improve integration of the entire product design and manufacturing process Faster design -> prototype and prototype -> volume production Enhanced customer visibility into outsourced production operations Reduced time to ramp factories, products, and processes to stay competitive within the rapidly changing business environment Building 30+ mask layer System on a Chip (SoC) with long cycle times where needs are rapidly changing Rapid and frequent factory plan changes driven by changing business needs Ability to model factory performance so that output can be optimized Ability to constantly adjust equipment loading to keep the factory profitable Need to run globally disparate factories as single “virtual factory”
Achieving Growth Targets while Margins are Declining	Implications of rising wafer, packaging, and other materials cost on meeting cost targets Meeting high factory yield much faster at startup Addressing increased complexity while keeping costs in check Reducing complexity and waste across the supply chain Inefficiencies introduced by non-product wafers (NPW) competing for resources with production wafers High cost and cycle time of mask sets for manufacturers impacting affordability of new product designs Increasing dedication of masks and equipment causing manufacturing inefficiencies Challenges introduced with sharing of mask sets Difficulty maintaining the historical 0.7× transistor shrink per year for die size and cost efficiency
Managing Ever Increasing Factory Complexity	Quickly and effectively integrating rapid changes in process technologies Managing carriers with multiple lots, wafers with multiple products, or multiple package form factors Comprehending increased purity requirements for process and materials Need to run aluminum and copper back end in the same factory Increasing number of processing steps coupled with process and product complexity Need to concurrently manage new and legacy software systems and systems with increasingly high interdependencies Explosive growth of data collection/analysis requirements driven by process and modeling needs Increased requirements for wafer level tracking and die level tracking
Meeting Factory and Equipment Reliability, Capability or Productivity Requirements per the Roadmap	Process equipment not meeting availability, run rate, and utilization targets out of the box Stand alone and integrated reliability for equipment and systems to keep factories operating Increased impacts that single points of failure have on a highly integrated and complex factory Quality issues with production equipment embedded controllers Lack of good data to measure equipment and factory effectiveness for optimization and improvement programs Factory capacity planning and supply chain management systems are not continuously base lined with actual factory data creating errors Lack of migration paths which inhibit movement from old inefficient systems to new highly productive systems

Table 84b *Factory Integration Difficult Challenges—Long-term*

<i>Difficult Challenges ≥ 45 nm/Through 2009</i>	<i>Summary of Issues</i>
Meeting the Flexibility, Extendibility, and Scalability Needs of a Cost-effective, Leading-edge Factory	Need to quickly convert factories to new process technologies while reusing equipment, facilities, and skills Minimizing downtime to on-going operations while converting factories to new technologies Scalability implications to meet large 300 mm factory needs [50K WSPM] Continued need to improve both throughput and cycle time Reuse of building, production and support equipment, and factory information and control systems across multiple technology nodes Understanding up-front costs to incorporate EFS Ability to convert 200 mm facilities to 300 mm wafer size Comprehending increased purity requirements for process and materials Accelerating the pace of standardization to meet industry needs
Meeting Process Requirements at 65 nm and 45 nm Nodes Running Production Volumes	Small process windows and tight process targets at 65 nm and 45 nm nodes in many modules make process control increasingly difficult Complexity of integrating next generation lithography equipment into the factory Overall development and volume production timelines continuing to shrink Device and process complexity make the ability to trace functional problems to specific process areas more difficult Difficulty in running different process parameters for each wafer while maintaining control windows and cycle time goals Reducing the impacts of parametric variation
Increasing Global Restrictions on Environmental Issues	Need to meet regulations in different geographical areas Need to meet technology restrictions in some countries while still meeting business needs Comprehending tighter ESH/Code requirements Lead free and other chemical and materials restrictions New material introduction
<i>Difficult Challenges < 45 nm/2010 Through 2018</i>	<i>Summary of Issues</i>
Post-conventional CMOS Manufacturing Uncertainty	Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements will have on factory design Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency Need to run CMOS and post CMOS processes in the same factory
Emerging Factory Paradigm and Next Wafer Size Change	Uncertainty about the next wafer size [450 mm] and the conversion timing [See Backup material as a link in the electronic chapter at http://public.itrs.net.] Traditional strategies to scale wafers and carriers for the next wafer size conversion may not work with [450 mm] 25 wafer carriers and drive significant production equipment and material handling changes Uncertainty concerning how to reuse buildings, equipment, and systems to enable the next wafer size conversion [to 450 mm] at an affordable cost

ASSEMBLY AND PACKAGING

The 2004 Assembly and Packaging Roadmap updates focused on three primary areas; expansion on the difficult challenges, new materials challenges, and changes in the near term package cost roadmap. In the difficult challenges tables focus has been increased on to need to close the gap between on chip interconnect and chip to chip interconnect in packages. This problem is seen as becoming more severe as chip interconnect continues to shrink at a faster rate than package based interconnect limiting the benefits of chip scaling. Longer term the packaging challenge of new MEMS, nanostructure, and emerging device technologies will also become very critical and have been identified as a critical research area for the industry. The materials challenges were expanded to include new lead free requirements, dielectrics for imbedded passives, organics which are compatible with higher temperature lead free solder assembly operations. The projections on future cost reductions in the low end were also modified to reflect the slow down in cost reduction. This is due to increasing material cost and the maturity of many package types. To put packaging industry back on an aggressive cost reduction curve completely new approaches are required which have not yet been identified.

Table 92a Assembly and Packaging Difficult Challenges—Near-term UPDATED

Difficult Challenges ≥ 45 nm/Through 2010		Summary of Issues
WAS	Improved Organic Substrates	Tg compatible with Pb free solder processing Increased wireability at low cost Improved impedance control and lower dielectric loss to support higher frequency applications Improved planarity and low warpage at higher process temperatures Low-moisture absorption Low-cost embedded passives Substrate cost is barrier to flip chip wide spread adoption today Increased via density in substrate core Alternative plating finish to improve reliability
IS	<u>Close gap between Chip and substrate -</u> Improved Organic Substrates	Tg compatible with Pb free solder processing Increased wireability at low cost Improved impedance control and lower dielectric loss to support higher frequency applications Improved planarity and low warpage at higher process temperatures Low-moisture absorption Low-cost embedded passives, <u>R, L, C</u> <u>Embedded active devices</u> Substrate cost is barrier to flip chip wide spread adoption today Increased via density in substrate core Alternative plating finish to improve reliability <u>Solutions for operation temp up to 200C</u> <u>Interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology)</u> <u>Production techniques will require silicon-like production and process technologies after 2005.</u>
WAS	Improved Underfills for Flip Chip on Organic Substrates	Thermal performance and thermal coupling between parts Materials which enable integration of SMT, varying semiconductors, and substrate types reliably Thin die, stack die, very large and very small die, passives component integration, SAW, shielding interconnect process Narrowing gaps Higher bump densities
Delete	~~Improved Underfills for Flip Chip on Organic Substrates~~	~~Thermal performance and thermal coupling between parts~~ ~~Materials which enable integration of SMT, varying semiconductors, and substrate types reliably~~ ~~Thin die, stack die, very large and very small die, passives component integration, SAW, shielding interconnect process~~ ~~Narrowing gaps~~ ~~Higher bump densities~~
	Coordinated Design Tools and Simulators to address Chip, Package, and Substrate Co-design	Mix signal co-design and simulation environment Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis Electrical (power disturbs, EMI, signal integrity associated with higher frequency/current and lower voltage switching) Commercial EDA supplier support System level co-design is needed now. EDA support for "native" area array is required to meet the Roadmap projections. Educational programs required to train engineers in these technologies/requirements.

Table 92a Assembly and Packaging Difficult Challenges—Near-term UPDATED (continued)

	Difficult Challenges ≥ 45 nm/Through 2010	Summary of Issues
WAS	Impact of Cu/low κ on Packaging	Direct wirebond and bump to Cu Bump and underfill technology to assure low- κ dielectric integrity Improved mechanical strength of dielectrics Interfacial adhesion Reliability of first level interconnect with low κ Mechanisms to measure the critical properties need to be developed. Probing over copper/low κ due to damage and bonding over probe mark
IS	Impact of <u>BEOL incl</u> Cu/low κ on Packaging	Direct wirebond and bump to Cu or improved barrier systems bondable pads Bump and underfill technology to assure low- κ dielectric integrity <u>including lead free solder bump system</u> Improved mechanical strength of dielectrics <u>and other interfaces</u> Interfacial adhesion Reliability of first level interconnect with low κ Mechanisms to measure the critical properties need to be developed. Probing over copper/low κ due to damage and bonding over probe mark
	High Current Density Packages	Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. Whisker growth Thermal dissipation
Add	<u>Flexible System Packaging</u>	<u>Conformal low cost organic substrates</u> <u>Small and thin die assembly</u> <u>Handling in low cost operation</u> <u>Different carrier materials (organics, silicon, ceramics, glass, laminat core) impact</u> <u>Establish infrastructure for new value chain</u> <u>Establish new process flows</u> <u>Reliability</u> <u>Testability</u> <u>Different active devices</u> <u>Electrical and optical interface integration</u>
	Wafer Level CSP	I/O pitch between 250um 400um less than 100 I/O solder joint reliability and cleaning processes for low stand-off Wafer thinning and handling technologies Compact ESD structures

Table 92b Assembly and Packaging Difficult Challenges—Long-term UPDATED

	<i>Difficult Challenges <45 nm/Beyond 2010</i>	<i>Summary of Issues</i>
WAS	Package Cost does not follow the Die Cost Reduction Curve	-Margin in packaging inadequate to support investment required to reduce cost
	Small Die with High Pad Count, High Power Density, and/or High Frequency	-Current density, operating temperature, etc for these devices exceed the capabilities of current assembly and packaging technology
IS	Small Die with High Pad Count, High Power Density, and/or High Frequency	- <u>New solder/UBM with improved current density capabilities</u> , operating temperature, etc for these devices exceed the capabilities of current assembly and packaging technology
WAS	High Frequency Die	-Substrate wiring density to support >20 lines/mm '-Lower loss dielectrics—skin effect above 10 GHz" -Hot spot" thermal management needs to be addressed before 2007. There is a "brick wall" at five-micron lines and spaces. Design TWG would like to have an upper bound on thermal management capability of future packages.
	Close Gaps between Substrate Technology and the Chip	-Interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology '-Production techniques will require silicon-like production and process technologies after 2005.
Delete	~~Close Gaps between Substrate Technology and the Chip~~	~~-Interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology '-Production techniques will require silicon-like production and process technologies after 2005.~~
	System-level Design Capability to Integrated Chips, Passives, and Substrates	-Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required. Hardware only '-This is also an issue before 2007. Embedded passives may be integrated into the "bumps" as well as the substrates.
	New Device Types (Organic, Nanostructures, Biological) that require New Packaging Technologies	-Organic device packaging requirements not yet define (will chips grow their own packages) '-Biological interfaces will require new interface types
	Bumpless area array technologies will be needed during this period. Face to face packages and other 3D packages are examples. High frequency, low power and low profile are driving forces	

ENVIRONMENT, SAFETY, AND HEALTH

Elimination of Requirements that are already “ESH Best Practices”

1. Exposure Data
2. Dependency upon Personal Protective Equipment
3. Equipment/Process Risk Assessments
4. Ergonomic Stressor Evaluation
5. Collection of Regulatory Requirements
6. Pollutant Release and Transfer Disclosure

Restructured “Design for ESH” Section

1. Interim solutions are being used for Life Cycle Assessments (LCA) and for Chemical Risk Assessments.
2. Pollutant Release and Transfer Disclosure was dropped.
3. Regulatory requirements were dropped because they are covered by existing Environmental Management Systems
1. Ratio of Fab Equipment to Facilities energy use was changed from 50/50 to 40/60.

Water Conservation (Tables 102 and 105)

1. Eliminated redundancy by locating data only in Table 102.

Chemical/Materials and Equipment Management (Table 103)

1. Dropped requirements for safe dopant delivery systems (goal achieved) and expanded definition of dopant requirements.
2. Revised high-k materials of concern.

Table 101a ESH Difficult Challenges—Near-term

<i>Five Difficult Challenges ≥ 50 nm/Through 2009</i>	<i>Summary of Issues/Needs</i>
Chemicals, Materials, and Equipment Management	<i>New Chemical Assessment</i> Need for quality rapid assessment methodologies to ensure that new chemicals (or those carried over from previous technologies but that now face new restrictions) can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation. <i>Chemical Data Collection</i> Need to document and make available environment, safety, and health characteristics of chemicals <i>Chemical Reduction</i> Need to develop processes that meet technology demands while reducing impact on human health, safety and the environment, both through replacement of hazardous materials with materials that are more benign, and by reducing chemical quantity requirements through more efficient and cost-effective process management <i>Environment Management</i> Need to develop effective management systems to address issues related to disposal of equipment, and hazardous and non-hazardous residue from the manufacturing process
Resource Conservation	<i>Natural Resource Conservation (Energy, Water)</i> Need to implement known (from supplier optimization studies, benchmarking surveys and best known methods) energy and water use reduction solutions Continue to design innovative energy and water efficient processing equipment <i>Chemicals and Materials Use</i> Need more efficient utilization of chemicals and materials <i>Resource Recycling</i> Increase resource reuse and recycling <i>Sustainable Growth</i> Continued expansion of semiconductor manufacturing with reduced impact on natural resources
Workplace Protection	<i>Equipment Safety</i> Continue to design ergonomically correct and safe equipment Minimize ergonomic stressors and health and safety risks during maintenance activities <i>Chemical Exposure Protection</i> Increase knowledge base on health and safety characteristics of chemicals, materials, and process byproducts in the manufacturing and maintenance processes and design out potential for chemical exposures and need for PPE
Climate Change Mitigation	<i>Reduce Energy Use of Process Equipment</i> Need to design energy efficient processing equipment <i>Reduce Energy Use of the Manufacturing Facility</i> Need to develop energy efficient facilities systems <i>Reduce High Global Warming Potential (GWP) Chemicals Emission</i> Need ongoing improvement in methods that reduce emissions from processes using GWP chemicals
Design for Environment, Safety, and Health (DFESH)	<i>Evaluate and Quantify ESH Impact</i> Need integrated way to evaluate and quantify ESH impact of process, chemicals, and process equipment, and to make ESH a design parameter in development of new equipment and processes

Table 101b ESH Difficult Challenges—Long-term

<i>Five Difficult Challenges <50 nm/Beyond 2009</i>	<i>Summary of Issues/Needs</i>
Chemicals, Materials and Equipment Management	<i>Chemical Use Information</i> Need to understand regulatory requirements that set chemical restrictions Need for comprehensive material life cycle analysis of semiconductor products
Resource Conservation	<i>Reduce Water, Energy, Chemicals and Materials Use</i> Need resource efficient processing and facility support equipment driving toward resource sustainability and greener fabs
Workplace Protection	<i>Equipment Safety</i> Need more emphasis on safety of fab automation systems/robotics and sub-system isolation (e.g., lock-out, tag-out (LOTO) of components of cluster tools) for tool maintenance
Climate Change Mitigation	<i>Reduce Energy Use</i> The importance of reducing energy use to minimize/slow climate change will grow <i>Reduce High GWP Chemicals Emissions</i> The international pressures to reduce emissions of GWP chemicals will continue
Design for Environment, Safety, and Health (DFESH)	<i>Evaluate and Quantify ESH Impact</i> Need ESH integrated into the design and development of new equipment and processes

YIELD ENHANCEMENT

The Yield Enhancement community is challenged by the following topics:

- Need for high-speed and cost-effective high aspect ratio inspection tools.
- Achieve testable and diagnosable designs for Integrated circuits.
- Data management and test structures for rapid yield learning.
- Correlation of Impurity level to yield.
- Development of parametric sensitive yield models including new materials and considering the high complexity of integration. The understandings of systematic mechanism limited yield are mandatory for achieving historic yield ramps in the future.
- Detection of ever-shrinking yield critical defects.
- Need for fast and short yield learning cycles at simultaneously increasing process complexity, to achieve historic yield ramps and mature yield levels.
- Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughput.

The priorities are according the listing above. The key changes were at:

- Defect Detection and Characterization
 - The edge exclusion was aligned between YE, FEP, Litho, and Factory Integration
 - Update and new calculation of the cost of ownership for defect inspection tools.
- Wafer Environment Contamination Control
 - Address table 114 to wafer environment as e.g. clean room or mini environment
 - Adjustment of the table values
 - Add new contamination issues within the table

Table 107 Yield Enhancement Difficult Challenges -- WAS

<i>Difficult Challenge ≥ 45 nm/Through 2010</i>	<i>Summary of Issues</i>
Design for Manufacture and Test (DFM and DFT) and Systematic Mechanisms Limited Yield (SMLY)—IC designs must be optimized for a given process capability and must be testable and diagnosable. Understanding SMLY is mandatory for achieving historic yield ramps in the future.	Design to process compatibility, design for manufacturability, design for test, design for diagnosability, systematic mechanisms limited yield (SMLY) model development.
High-Aspect-Ratio Inspection—High-speed, cost-effective tools are needed to rapidly detect defects at 1/2 X ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches and especially defects near or at the bottoms of these features	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
Detection of Ever Shrinking Yield Critical Defects—High throughput, high capture rate detection tools are needed for ever shrinking critical defects of interest.	Line edge roughness, ACLV, subtle process variation. Where does process variation stop and defect start? Need to improve signal to noise to delineate defect from process variation.
Non-visual Defect Sourcing—Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected.	Many defects that cause electrical faults are not detectable inline.
<i>Difficult Challenge <45 nm/Beyond 2010</i>	<i>Summary of Issues</i>
Develop Yield Models that include New Materials and Integration—Models must comprehend greater parametric sensitivities, complex integration issues, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Develop test structures for new technology nodes. Address complex integration issues. Model ultra-thin film integrity issues. Improve scaling methods for front-end processes including increased transistor packing density.
Defect Detection—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughput.	Existing techniques trade-off throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size may not exist.
Correlation of Impurity Level to Yield—Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product.	Establish an employment methodology for each material type. Define a standard test for yield/parametric effect.
Yield Ramp and Mature Yields—With increasing process complexity and fewer yield learning cycles with each subsequent technology node, it would be impossible to achieve historic yield ramps and mature yield levels.	Long and complex process will make achieving historic yield ramps challenging. Also, new materials will introduce previously unseen yield problems. Need tools and methods to shorten yield learning cycles

Table 107 Yield Enhancement Difficult Challenges -- IS

	<i>Difficult Challenge ≥ 45 nm/Through 2010</i>	<i>Summary of Issues</i>
IS	High-Aspect-Ratio Inspection—High-speed, cost-effective tools are needed to rapidly detect defects at 1/2 X ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches and especially defects near or at the bottoms of these features	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
IS	Design for Manufacture and Test (DFM and DFT) and Systematic Mechanisms Limited Yield (SMLY)—IC designs must be optimized for a given process capability and must be testable and diagnosable. Understanding SMLY is mandatory for achieving historic yield ramps in the future.	Design to process compatibility Design for manufacturability, test, and diagnosability SMLY model development.
IS	Data Management and Test Structures for Rapid Yield Learning to enable the rapid root-cause analysis of yield-limiting conditions.	Development of automated, intelligent structures, analysis, and reduction algorithms that correlate facility, design, process, test, and work-in-process (WIP) data
IS	Detection of Ever-Shrinking Yield Critical Defects - High throughput, cost-effective, high capture rate detection tools are needed for ever-shrinking critical defects of interest. Where does process variation stop and defect start?	Non-visual Defect Sourcing - In-line and end-of-line failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected. Wafer inspection of backside, bevel, edge, nanotopography and geometry Line edge roughness, ACLV, subtle process variation. Need to improve signal to noise ratio to delineate defect from process variation.
	<i>Difficult Challenge <45 nm/Beyond 2010</i>	<i>Summary of Issues</i>
IS	Correlation of Impurity Level to Yield— Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and determine required control limits.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product. Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect.
IS	Develop Yield Models that include New Materials and Integration— Models must comprehend greater parametric sensitivities, complex integration issues, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Develop test structures for new technology nodes. Address complex integration issues. Model ultra-thin film integrity issues. Improve scaling methods for front-end processes including increased transistor packing density.
IS	Yield Ramp and Mature Yields—With increasing process complexity and fewer yield learning cycles with each subsequent technology node, it would be impossible to achieve historic yield ramps and mature yield levels. Also, new materials will introduce previously unseen yield problems.	Need of tools and methods for short yield learning cycles. Understanding of Systematic Mechanisms Limited Yield (SMLY) is mandatory for achieving historic yield ramps in the future.
IS	Defect Detection—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughput.	Existing techniques trade-off throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size may not exist.

METROLOGY

The changes to the 2003 ITRS Technology Requirements tables come from the Metrology TWG assessments of the state of the art of metrology equipment capability. The requirement values have remained the same. One of the most important new messages is that Critical Dimension measurement technology is now believed to be extendable to ~ the 32 nm Node. CD-SEM and scatterometry are both considered capable of being improved and extended to the 32 nm node. Since in some cases, the equipment will require improvement to meet precision requirements, those areas are now listed by using the color yellow. Previously, all CD measurement requirements were listed in the red color for near term years. Some measurement requirements such as CD for Dense Lines can be met through 2009 by existing technology. Another requirement for CD measurement was added to the Requirements Table. The aspect ratio for trench structures makes CD measurement much more difficult. Values for this requirement can now be found in the table. Some of the values for gate dielectric thickness measurement were refined after inputs from the FEP TWG.

The TWG also found that the Materials Characterization community now has a critical new capability. Aberration corrected TEM is moving from the research labs to the commercialized systems. The first evidence of 3D TEM imaging is being published. Electron energy loss can locate a single atom to one column of atoms in a crystalline sample.

Table 115 Metrology Difficult Challenges

<i>Five Difficult Challenges ≥ 45 nm/Through 2009</i>	<i>Summary of Issues</i>
Factory level and company wide metrology integration for real-time <i>in situ</i> , integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species /energy /dosage (current), and wafer temperature during RTA.
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of high-aspect ratio technologies such as Damascene challenges all metrology methods. Key requirements are dimensional control, void detection in copper lines, and pore size distribution and detection of killer pores in patterned low- κ dielectrics.	New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures in new, low- κ dielectrics. Sidewall roughness impacts barrier integrity and the electrical properties of lines and vias.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new, high- κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low- κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates. The same is true for measurement of barrier layers. High frequency dielectric constant measurements have shown a constant frequency response and are no longer a pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. There is a concern that measurements on test structures located in scribe lines do not correlate with in die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.

Table 115 Metrology Difficult Challenges (continued)

<i>Five Difficult Challenges < 45 nm/Beyond 2009</i>	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for Damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in die properties is becoming more difficult as device shrinks.
Statistical limits of sub-45 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions.	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

* SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.

MODELING AND SIMULATION

The most important trend in the 2004 Update of the Modeling and Simulation chapter is the ever increasing need for improved integration between the various areas of simulation, like device and circuit, or interconnect and packaging. Different effects which could in the past be simulated separately will in future need to be treated simultaneously, such as thermal-mechanical, thermodynamic and electronic properties of interconnect materials. Due to the ongoing extension of the PIDS chapter to detail the requirements for high-frequency technologies, the simulation of III/V materials has been added to the short-term challenge on high-frequency device/circuit modeling. Furthermore, various new aspects and additional details were added to the items which explain the challenges and the requirements for Modeling and Simulation.

Concerning the Modeling and Simulation Technology Requirement table, four new features have been added: Full chip lithography simulation, novel memory devices, the impact of processes and materials on electrical performance, and material properties in general. The items which detail the requirements have been considerably extended, and their timing updated.

Table 121 Modeling and Simulation Difficult Challenges UPDATED

	Difficult Challenges ≥ 45 nm/Through 2010	Summary of Issues
WAS	High-frequency circuit modeling for 5–40 GHz applications	Efficient extraction and simulation of full-chip interconnect delay Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters High-frequency circuit models including non-quasi-static, substrate noise and parasitic coupling Parameter extraction assisted by numerical electrical simulation instead of RF measurements
IS	High-frequency <u>device and</u> circuit modeling for 5– <u>100</u> GHz applications	Efficient extraction and simulation of full-chip interconnect delay Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters <u>Extension of physical device models to III/V materials</u> High-frequency circuit models including non-quasi-static, substrate noise, <u>1/f noise</u> and parasitic coupling Parameter extraction assisted by numerical electrical simulation instead of RF measurement <u>Scalable active and passive component models for compact circuit simulation</u> <u>Co-design between interconnects and packaging</u>
WAS	Front-end process modeling for nanometer Structures	Diffusion/activation/damage models and parameters including low thermal budget processes in Si-based substrate, i.e., Si, SiGe:C (incl. strain), SOI, and ultra-thin body devices Characterization tools/methodologies for these ultra shallow geometries/junctions and low dopant levels Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
IS	Front-end process modeling for nanometer Structures	Diffusion/activation/damage models and parameters including <u>SPE and</u> low thermal budget processes in Si-based substrate, i.e., Si, SiGe:C, <u>Ge</u> (incl. strain), SOI, and ultra-thin body devices Characterization tools/methodologies for these ultra shallow geometries/junctions and low dopant levels Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces <u>Front-end processing impact on reliability</u>

Table 121 Modeling and Simulation Difficult Challenges *UPDATED* (continued)

Difficult Challenges ≥ 45 nm/Through 2010		Summary of Issues
WAS	Modeling of equipment Influences on features generated in deposition and etching processes	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry); reaction mechanisms, and reduced models for complex chemistry Linked equipment/feature scale models CMP (full wafer and chip level, pattern dependent effects) MOCVD, PECVD, and ALD modeling Multi-generation equipment/wafer models
IS	<u>Integrated modeling of equipment, materials, feature scale processes and influences on devices</u>	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry <u>for ULK, photoresists and high-k metal gate</u>); reaction mechanisms, and reduced models for complex chemistry Linked equipment/feature scale models <u>(including high-k metal gate integration, damage prediction)</u> CMP (full wafer and chip level, pattern dependent effects) MOCVD, PECVD, ALD, <u>electroplating and electroless deposition</u> modeling Multi-generation equipment/wafer models
WAS	Lithography simulation including NGL	Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM) Predictive resist models including line-edge roughness, etch resistance and mechanical stability Multi-generation lithography system models
IS	Lithography simulation including NGL	Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM) Predictive resist models <u>(e.g. mesoscale models)</u> including line-edge roughness, etch resistance, <u>adhesion</u>, and mechanical stability <u>Methods to easily calibrate resist model kinetic and transport parameters</u> <u>Models that bridge requirements of OPC (speed) and process development (predictive)</u> <u>Experimental verification and simulation of ultra-high NA vector models, including polarization</u> <u>Models and experimental verification of non-optical immersion lithography effects (e.g. topography and change of refractive index distribution)</u> Multi-generation lithography system models <u>Simulation of defect influences/defect printing</u>
WAS	Ultimate nanoscale CMOS simulation capability	Methods and algorithms that contribute to prediction of CMOS limits Quantum based simulators Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS Phenomenological gate stack models for ultra-thin dielectrics Models for device impact of statistical fluctuations in structures and dopant distributions
IS	Ultimate nanoscale CMOS simulation capability	Methods and algorithms that contribute to prediction of CMOS limits Quantum based simulators Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS Gate stack models for ultra-thin dielectrics Models for device impact of statistical fluctuations in structures and dopant distributions <u>Phenomenological material models for stress engineering</u>

Table 121 Modeling and Simulation Difficult Challenges UPDATED (continued)

Difficult Challenges ≥ 45 nm/Through 2010		Summary of Issues
WAS	Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical and electronic properties of low κ , high κ , and conductors and the impact of processing on these properties Model reliability of packages and interconnects, e.g. stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion
	Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical, <u>thermodynamic</u> and electronic properties of low κ , high κ , and conductors and the impact of processing on these properties <u>especially for interfaces and films under 1 micron dimension</u> Model reliability of packages and interconnects, e.g. stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion. <u>Models for electron transport in ultra fine patterned conductors.</u>
Difficult Challenges <45 nm/Beyond 2010		Summary of Issues
WAS	Modeling of processing and electrical properties of new materials	Computational materials science tools to understand materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions
	Modeling of <u>chemical, thermomechanical</u> , and electrical properties of new materials	Computational materials science tools to <u>describe</u> materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, <u>thermomechanical (including stress effects on mobility)</u> , <u>optical properties</u> , reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. <u>Models for air gap and novel integrations in 3D interconnects including data for ultrathin material properties.</u>
WAS	Compact modeling including more physical models and statistics	Computer-efficient inclusion of influences of statistics (incl. correlations) before process freeze, quantum/ballistic transport, etc., into compact modeling
	Nano-scale modeling	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes, quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects)
	Nano-scale modeling	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes <u>(incl. doping)</u> , quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects)
IS	Optoelectronics modeling	Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling Physical design tools for integrated electrical/optical systems

APPENDIX A LIST OF UPDATES

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EMERGING RESEARCH DEVICES AND MATERIALS

Emerging Research Materials [Section **ADDED** for 2004 Update]

Introduction

Critical Materials Properties

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For More Information

The 2004 Update is available free online to download at the website <http://public.itrs.net>.

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Overall Roadmap Technology Characteristics

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OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

[Link to the 2003 ITRS Executive Summary](#)

ORTC TABLES

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
ASIC/Low Operating Power Printed Gate Length (nm) ††	90	75	65	53	45	40	35
ASIC/Low Operating Power Physical Gate Length (nm)	65	53	45	37	32	28	25

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term Years [UPDATED](#)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	ASIC/Low Operating Power Printed Gate Length (nm) ††	32		25	22		18	16		13
IS	ASIC/Low Operating Power Printed Gate Length (nm) ††	32	28	25	22	20	18	16	14	13
WAS	ASIC/Low Operating Power Physical Gate Length (nm)	22		18	16		13	11		9
IS	ASIC/Low Operating Power Physical Gate Length (nm)	22	20	18	16	14	13	11	10	9

2 Overall Roadmap Technology Characteristics

Notes for Tables 1a and 1b

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also “as etched in polysilicon,” in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC “physical” gate lengths may be reduced from the “as-printed” dimension. These “physical” gate-length targets are driven by the need for maximum speed performance in logic Microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design ITWG Tables as needs that drive device design and process technology requirements.

In addition, during the 2003 ITRS development, an attempt has been made to reconcile the many published press releases by Logic manufacturers referencing “90 nm” technology node manufacturing in 2003. Since the metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that the public citations were in reference to an “indexed” technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance).

The IRC has decided that the best way to minimize confusion between the ITRS and individual company public announcements is to identify the ITRS table header node with the industry's most aggressive half-pitch targets, and to label these targets as hpXX (i.e., hp90, hp65, hp45, etc.). Currently the industry's most aggressive half pitch is the DRAM cell metal half-pitch.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1c DRAM Production Product Generations and Chip Size Model—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Cell area factor [a]	8	8	7.5	7	7	6	6
Cell area [$Ca = af^2$] (mm ²)	0.082	0.065	0.048	0.036	0.028	0.019	0.015
Cell array area at production (% of chip size) §	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%
Generation at production §	1G	1G	1G	2G	2G	4G	4G
Functions per chip (Gbits)	1.07	1.07	1.07	2.15	2.15	4.29	4.29
Chip size at production (mm ²)§	139	110	82	122	97	131	104
Gbits/cm ² at production §	0.77	0.97	1.31	1.76	2.22	3.27	4.12

Table 1d DRAM Production Product Generations and Chip Size Model—Long-term Years [UPDATED](#)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Cell area factor [a]	6		6	6		6	5		5
IS	Cell area factor [a]	6	6	6	6	6	6	5	5	5
WAS	Cell area [$Ca = af^2$] (mm ²)	0.012		0.0077	0.0061		0.0038	0.0025		0.0016
IS	Cell area [$Ca = af^2$] (mm ²)	0.012	0.0096	0.0077	0.0061	0.005	0.0038	0.0025	0.002	0.0016
WAS	Cell array area at production (% of chip size) §	63.00%		63.00%	63.00%		63.00%	63.00%		63.00%
IS	Cell array area at production (% of chip size) §	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%
WAS	Generation at production §	4G		8G	8G		16g	32G		32G
IS	Generation at production §	4G	8G	8G	8G	16g	16g	32G	32G	32G
WAS	Functions per chip (Gbits)	4.29		8.59	8.59		17.18	34.36		34.36
IS	Functions per chip (Gbits)	4.29	8.59	8.59	8.59	17.18	17.18	34.36	34.36	34.36
WAS	Chip size at production (mm ²)§	83		104	83		104	138		87
IS	Chip size at production (mm ²)§	83	131	104	83	131	104	138	110	87
WAS	Gbits/cm ² at production §	5.19		8.23	10.37		16.46	24.89		39.51
IS	Gbits/cm ² at production §	5.19	6.53	8.23	10.37	13.07	16.46	24.89	31.36	39.51

4 Overall Roadmap Technology Characteristics

Notes for Tables 1c and 1d

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows

1999-2004/8× 2005/7.5×; 2006-2007/7×; 2008-2015/6×; 2016-2018/5×. The delay of the “6” DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of “Moore's Law” bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

InTER-generation chip size growth rate model target for Production-phase DRAMs is now “flat” at less than 140 mm², similar to the MPU model. This new flat-chip-size model target requires the bits/chip “Moore's Law” model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Table 1c,d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63% , which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above).The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Cell area factor [a]	8	8	7.5	7	7	6	6
Cell area [Ca = a ²] (mm ²)	0.082	0.065	0.048	0.036	0.028	0.019	0.015
Cell array area at introduction (% of chip size) §	72.23%	72.61%	72.95%	73.25%	73.52%	73.76%	73.97%
Generation at introduction §	4G	4G	8G	8G	16G	16G	16G
Functions per chip (Gbits)	4.29	4.29	8.59	8.59	17.18	17.18	17.18
Chip size at introduction (mm ²) §	485	383	568	419	662	449	356
Gbits/cm ² at introduction §	0.88	1.12	1.51	2.05	2.59	3.82	4.83

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	-	42	38	-	30	27	-	21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
WAS	Cell area factor [a]	6	-	6	6	-	6	5	-	5
IS	Cell area factor [a]	6	<u>6</u>	6	6	<u>6</u>	6	5	<u>5</u>	5
WAS	Cell area [Ca = a ²] (mm ²)	0.012	-	0.0077	0.0061	-	0.0038	0.0025	-	0.0016
IS	Cell area [Ca = a ²] (mm ²)	0.0120	<u>0.01</u>	0.0077	0.0061	<u>0.005</u>	0.0038	0.0025	<u>0.0020</u>	0.0016
WAS	Cell array area at introduction (% of chip size) §	74.16%	-	74.47%	74.61%	-	74.83%	74.93%	-	75.09%
IS	Cell array area at introduction (% of chip size) §	74.16%	<u>74.30%</u>	74.47%	74.61%	<u>74.70%</u>	74.83%	74.93%	<u>75.00%</u>	75.09%
WAS	Generation at introduction §	32G	-	32G	64G	-	64G	128G	-	128G
IS	Generation at introduction §	32G	<u>32G</u>	32G	64G	<u>64G</u>	64G	128G	<u>128G</u>	128G
WAS	Functions per chip (Gbits)	34.36	-	34.36	68.72	-	68.7	137.4	-	137.4
IS	Functions per chip (Gbits)	34.36	<u>34.36</u>	34.36	68.72	<u>68.72</u>	68.7	137.4	<u>137.4</u>	137.4
WAS	Chip size at introduction (mm ²) §	563	-	353	560	-	351	464	-	292
IS	Chip size at introduction (mm ²) §	563	<u>458</u>	353	560	<u>456</u>	351	464	<u>378</u>	292
WAS	Gbits/cm ² at introduction §	5.2	-	8.2	10.4	-	16.5	24.9	-	39.5
IS	Gbits/cm ² at introduction §	<u>6.10</u>	<u>7.71</u>	<u>9.73</u>	<u>12.3</u>	<u>15.5</u>	<u>19.6</u>	<u>29.6</u>	<u>37.3</u>	<u>47.1</u>

Notes for Tables 1e and 1f

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows

1999-2004/8× 2005/7.5×; 2006-2007/7×; 2008-2015/6×; 2016-2018/5×. The delay of the “6” DRAM Cell design improvement Factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of “Moore’s Law” bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a 3-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation/2007, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation/2003, the introduction rate is 4×/five years (2×/two–three years).

The original 2001 ITRS InTER-generation chip size growth rate was targeted to fit one chip per 572 mm² field at Introduction and two chips per 572 mm² field at Production. Due to the delay of the cell area factor reductions, Introduction chip sizes increased, but the new 704 mm² maximum affordable Litho field allows the Introduction chip to double bits per chip every two years through the 16 Gbit generation (660 mm²/2007). Slowing the “Moore’s Law” bits per chip of the Introduction-phase DRAM model to an average of 2× per 2.5 years enables the Introduction DRAMs to remain under the original 572 mm² affordable target after 2007. The InTRA-generation chip size shrink model remains at 0.5× every technology node in-between cell factor reductions, and eventually (ranging from five to six years), the Introduction-phase DRAMs shrink below the 140 mm² Production-phase chip size target.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

6 Overall Roadmap Technology Characteristics

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years [UPDATED](#)

Year of Production		2003	2004	2005	2006	2007	2008	2009
Technology Node			hp90			hp65		
DRAM ½ Pitch (nm)		100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)		120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)		107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††		65	53	45	40	35	32	28
MPU Physical Gate Length (nm)		45	37	32	28	25	22	20
SRAM Cell (6-transistor) Area factor ++		120.3	117.8	115.6	113.7	111.9	110.4	109
Logic Gate (4-transistor) Area factor ++		320	320	320	320	320	320	320
SRAM Cell (6-transistor) Area efficiency ++		0.63	0.63	0.63	0.63	0.63	0.63	0.63
Logic Gate (4-transistor) Area efficiency ++		0.50	0.50	0.50	0.50	0.50	0.50	0.50
ADD	SRAM Cell (6-transistor) Area ++	1.23	0.95	0.74	0.58	0.45	0.35	0.28
	SRAM Cell (6-transistor) Area w/overhead ++	2.0	1.5	1.2	0.93	0.73	0.57	0.45
ADD	Logic Gate (4-transistor) Area ++	3.27	2.59	2.06	1.63	1.30	1.03	0.82
	Logic Gate (4-transistor) Area w/overhead ++	6.5	5.2	4.1	3.3	2.6	2.1	1.6
	Transistor density SRAM (Mtransistors/cm ²)	305	393	504	646	827	1,057	1,348
	Transistor density logic (Mtransistors/cm ²)	61	77	97	122	154	194	245
	Generation at introduction *	--	p07c	--	--	p10c	--	--
WAS	Functions per chip at introduction (million transistors [Mtransistors])	180	226	285	360	453	571	719
IS	Functions per chip at introduction (million transistors [Mtransistors])	<u>307</u>	<u>386</u>	<u>487</u>	<u>614</u>	<u>773</u>	<u>974</u>	<u>1227</u>
	Chip size at introduction (mm ²) ‡	280	280	280	280	280	280	280
	Cost performance MPU (Mtransistors/cm ² at introduction) (including on-chip SRAM) ‡	110	138	174	219	276	348	438
	Generation at production *	--	p04c	--	--	p07c	--	--
	Functions per chip at production (million transistors [Mtransistors])	153	193	243	307	386	487	614
	Chip size at production (mm ²) §§	140	140	140	140	140	140	140
	Cost performance MPU (Mtransistors/cm ² at production, including on-chip SRAM) ‡	110	138	174	219	276	348	438

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
WAS	SRAM Cell (6-transistor) Area factor ++	107.8		105.7	104.8		103.4	102.8		101.7
IS	SRAM Cell (6-transistor) Area factor ++	107.8	<u>106.7</u>	105.7	104.8	<u>104.1</u>	103.4	102.8	<u>102.2</u>	101.7
WAS	Logic Gate (4-transistor) Area factor ++	320		320	320		320	320		320
IS	Logic Gate (4-transistor) Area factor ++	320	<u>320</u>	320	320	<u>320</u>	320	320	<u>320</u>	320
WAS	SRAM Cell (6-transistor) Area efficiency ++	0.625		0.625	0.625		0.625	0.625		0.625
IS	SRAM Cell (6-transistor) Area efficiency ++	0.625	<u>0.625</u>	0.625	0.625	<u>0.625</u>	0.625	0.625	<u>0.625</u>	0.625
WAS	Logic Gate (4-transistor) Area efficiency ++	0.5		0.5	0.5		0.5	0.5		0.5
IS	Logic Gate (4-transistor) Area efficiency ++	0.50	<u>0.50</u>	0.50	0.50	<u>0.50</u>	0.50	0.50	<u>0.50</u>	0.50
ADD	SRAM Cell (6-transistor) Area	<u>0.22</u>	<u>0.17</u>	<u>0.13</u>	<u>0.11</u>	<u>0.084</u>	<u>0.066</u>	<u>0.052</u>	<u>0.041</u>	<u>0.032</u>
WAS	SRAM Cell (6-transistor) Area w/overhead ++	0.22		0.13	0.11		0.066	0.052		0.032
IS	SRAM Cell (6-transistor) Area w/overhead ++	<u>0.35</u>	<u>0.27</u>	<u>0.22</u>	<u>0.17</u>	<u>0.13</u>	<u>0.106</u>	<u>0.083</u>	<u>0.07</u>	<u>0.052</u>
ADD	Logic Gate (4-transistor) Area	<u>0.65</u>	<u>0.51</u>	<u>0.41</u>	<u>0.32</u>	<u>0.26</u>	<u>0.20</u>	<u>0.16</u>	<u>0.13</u>	<u>0.10</u>
WAS	Logic Gate (4-transistor) Area w/overhead ++	1.3		0.82	0.65		0.41	0.32		0.2
IS	Logic Gate (4-transistor) Area w/overhead ++	1.30	<u>1.03</u>	0.82	0.65	<u>0.51</u>	0.41	0.32	<u>0.26</u>	0.20
WAS	Transistor density SRAM (Mtransistors/cm ²)	1,718		2,781	3,532		5,687	7,208		11,558
IS	Transistor density SRAM (Mtransistors/cm ²)	1,718	<u>2,187</u>	2,781	3,532	<u>4,484</u>	5,687	7,208	<u>9,130</u>	11,558
WAS	Transistor density logic (Mtransistors/cm ²)	309		490	617		980	1,235		1,960
IS	Transistor density logic (Mtransistors/cm ²)	309	<u>389</u>	490	617	<u>778</u>	980	1,235	<u>1,555</u>	1,960

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Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	Generation at introduction *	p13c		--	p16c		--	p19c		--
IS	Generation at introduction *	p13c	<u>--</u>	--	p16c	<u>--</u>	--	p19c	<u>--</u>	--
WAS	Functions per chip at introduction (million transistors [Mtransistors])	1,546		2,454	3,092		4,908	6,184		9,816
IS	Functions per chip at introduction (million transistors [Mtransistors])	<u>1,546</u>	<u>1,948</u>	<u>2,454</u>	<u>3,092</u>	<u>3,896</u>	<u>4,908</u>	<u>6,184</u>	<u>7,791</u>	<u>9,816</u>
WAS	Chip size at introduction (mm ²) ‡	280		280	280		280	280		280
IS	Chip size at introduction (mm ²) ‡	280	<u>280</u>	280	280	<u>280</u>	280	280	<u>280</u>	280
WAS	Cost performance MPU (Mtransistors/cm ² at introduction) (including on-chip SRAM) ‡	552		876	1,104		1,753	2,209		3,506
IS	Cost performance MPU (Mtransistors/cm ² at introduction) (including on-chip SRAM) ‡	552	<u>696</u>	876	1,104	<u>1,391</u>	1,753	2,209	<u>2,783</u>	3,506
WAS	Generation at production *	p10c		--	p13c		--	p16c		--
IS	Generation at production *	p10c	<u>--</u>	--	p13c	<u>--</u>	--	p16c	<u>--</u>	--
WAS	Functions per chip at production (million transistors [Mtransistors])	773		1,227	1,546		2,454	3,092		4,908
IS	Functions per chip at production (million transistors [Mtransistors])	773	<u>974</u>	1,227	1,546	<u>1,948</u>	2,454	3,092	<u>3,896</u>	4,908
WAS	Chip size at production (mm ²) §§	140		140	140		140	140		140
IS	Chip size at production (mm ²) §§	140	<u>140</u>	140	140	<u>140</u>	140	140	<u>140</u>	140
WAS	Cost performance MPU (Mtransistors/cm ² at production, including on-chip SRAM) ‡	552		876	1,104		1,753	2,209		3,506
IS	Cost performance MPU (Mtransistors/cm ² at production, including on-chip SRAM) ‡	552	<u>696</u>	876	1,104	<u>1,391</u>	1,753	2,209	<u>2,783</u>	3,506

Notes for Tables 1g and 1h

++ The MPU area factors are analogous to the “cell area factor” for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

* p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p01c, was introduced in 1999, but not ramped into volume production until 2001; similarly, the p04c, is introduced in 2001, but is targeted for volume production in 2004.

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/1999), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm²/cost-performance at introduction; 140 mm²/cost-performance at production; 310 mm²/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years
UPDATED

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Logic (Low-volume Microprocessor) High-performance ‡							
WAS Generation at production **	p03h	--	p05h	--	p07h	--	p09h
IS Generation at production **	--	<u>p04h</u>	--	--	p07h	--	--
Functions per chip (million transistors)	439	553	697	878	1,106	1,393	1,756
Chip size at production (mm ²) §§	310	310	310	310	310	310	310
High-performance MPU Mtransistors/cm ² at production (including on-chip SRAM) ‡	142	178	225	283	357	449	566
ASIC							
ASIC usable Mtransistors/cm ² (auto layout)	142	178	225	283	357	449	566
ASIC max chip size at production (mm ²) (maximum lithographic field size)	572	572	572	572	572	572	572
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	810	1,020	1,286	1,620	2,041	2,571	3,239

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Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years
UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
	Logic (Low-volume Microprocessor) High-performance ‡									
WAS	Generation at production **	--		--	p13h		p15h	--		--
IS	Generation at production **	<u>p10h</u>	--	--	p13h	--	--	<u>p16h</u>	--	--
WAS	Functions per chip (million transistors)	2,212		3,511	4,424		7,022	8,848		14,045
IS	Functions per chip (million transistors)	2,212	<u>2,787</u>	3,511	4,424	<u>5,574</u>	7,022	8,848	<u>11,147</u>	14,045
WAS	Chip size at production (mm ²) §§	310		310	310		310	310		310
IS	Chip size at production (mm ²) §§	310	<u>310</u>	310	310	<u>310</u>	310	310	<u>310</u>	310
WAS	High-performance MPU Mtransistors/cm ² at production (including on-chip SRAM) ‡	714		1,133	1,427		2,265	2,854		4,531
IS	High-performance MPU Mtransistors/cm ² at production (including on-chip SRAM) ‡	714	<u>899</u>	1,133	1,427	<u>1,798</u>	2,265	2,854	<u>3,596</u>	4,531
	ASIC									
WAS	ASIC usable Mtransistors/cm ² (auto layout)	714		1,133	1,427		2,265	2,854		4,531
IS	ASIC usable Mtransistors/cm ² (auto layout)	714	<u>899</u>	1,133	1,427	<u>1,798</u>	2,265	2,854	<u>3,596</u>	4,531
WAS	ASIC maximum chip size at production (mm ²) (maximum lithographic field size)	572		572	572		572	572		572
IS	ASIC maximum chip size at production (mm ²) (maximum lithographic field size)	572	<u>572</u>	572	572	<u>572</u>	572	572	<u>572</u>	572
WAS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081		6,479	8,163		12,958	16,326		25,915
IS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081	<u>5,142</u>	6,479	8,163	<u>10,284</u>	12,958	16,326	<u>20,569</u>	25,915

Notes for Tables 1i and 1j

** p is processor, numerals reflect year of production; h indicates high-performance product. Examples—the high-performance processor, p99h, was ramped into volume production in 1999; similarly, the p01h, is introduced in 2001, the p03h in 2003, and so forth.

‡ MPU High-performance Model—High-performance MPU includes large L2 and L3 on-chip SRAM (2MByte/1999) plus a larger logic core (P99h core = 25M transistor (Mtransistors) both SRAM and Logic functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm²/cost-performance at introduction; 140 mm²/cost-performance at production; 310 mm²/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions

Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Lithography Field Size							
Lithography Field Size—area (mm ²)	704	704	704	704	704	704	704
Lithographic field size—length (mm)	32	32	32	32	32	32	32
Lithographic field size—width (mm)	22	22	22	22	22	22	22
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	300	300	300	300	300	300	300

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years [UPDATED](#)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	-	42	38	-	30	27	-	21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
Lithography Field Size										
WAS	Lithography Field Size—area (mm ²)	704		704	704		704	704		704
IS	Lithography Field Size—area (mm ²)	704	<u>704</u>	704	704	<u>704</u>	704	704	<u>704</u>	704
WAS	Lithographic field size—length (mm)	32	-	32	32	-	32	32	-	32
IS	Lithographic field size—length (mm)	32	<u>32</u>	32	32	<u>32</u>	32	32	<u>32</u>	32
WAS	Lithographic field size—width (mm)	22	-	22	22	-	22	22	-	22
IS	Lithographic field size—width (mm)	22	<u>22</u>	22	22	<u>22</u>	22	22	<u>22</u>	22
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)										
WAS	Bulk or epitaxial or SOI wafer	300		450	450		450	450		450
IS	Bulk or epitaxial or SOI wafer	300	<u>300</u>	450	450	<u>450</u>	450	450	<u>450</u>	450

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Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years [UPDATED](#)

Year of Production		2003	2004	2005	2006	2007	2008	2009
Technology Node			hp90			hp65		
DRAM ½ Pitch (nm)		100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)		120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)		107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††		65	53	45	40	35	32	28
MPU Physical Gate Length (nm)		45	37	32	28	25	22	20
Number of Chip I/Os (Number of Total Chip Pads)—Maximum								
WAS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,328	3,584
IS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072
WAS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,109	1,195
IS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,024	1,024
WAS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,219	2,389
IS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,048	2,048
WAS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,600	4,800
IS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,400	4,600
WAS	Signal I/O pads—ASIC high-performance	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Signal I/O pads—ASIC high-performance	1700	1800	2000	2100	2200	2200	2300
WAS	Power and ground pads—ASIC high-performance (½ of total pads)	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Power and ground pads—ASIC high-performance (½ of total pads)	1700	1800	2000	2100	2200	2200	2300
Number of Total Package Pins—Maximum [1]								
WAS	Microprocessor/controller, cost-performance	500–1,452	500–1,600	550–1,760	550–1,936	600–2,140	660–2,354	720–2,568
IS	Microprocessor/controller, cost-performance	--	500–1600	550–1760	550–1936	600–2140	600–2400	660–2800
WAS	Microprocessor/controller, high-performance	1,452	1,600	1,760	1,936	2,140	2,354	2,568
IS	Microprocessor/controller, high-performance	--	1,600	1,760	1,936	2,140	2,400	2,800
WAS	ASIC (high-performance)	2,400	3,000	3,400	3,800	4,000	4,400	4,600
IS	ASIC (high-performance)	--	3,000	3,400	3,800	4,000	4,400	4,600

Notes for Tables 3a and 3b

[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by PWB technology and system cost.

The highest pin count applications will as a result use larger pitches and larger package sizes.

The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2:1 to 1:4.

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
Number of Chip I/Os (Number of Total Chip Pads)—Maximum										
WAS	Total pads—MPU	3,840		4,096	4,224		4,352	4,416		4,544
IS	Total pads—MPU	<u>3,072</u>	<u>3,072</u>	<u>3,072</u>	<u>3,072</u>	<u>3,072</u>	<u>3,072</u>	<u>3,072</u>	<u>3,072</u>	<u>3,072</u>
WAS	Signal I/O—MPU (1/3 of total pads)	1,280		1,365	1,408		1,451	1,472		1,515
IS	Signal I/O—MPU (1/3 of total pads)	<u>1,024</u>	<u>1,024</u>	<u>1,024</u>	<u>1,024</u>	<u>1,024</u>	<u>1,024</u>	<u>1,024</u>	<u>1,024</u>	<u>1,024</u>
WAS	Power and ground pads—MPU (2/3 of total pads)	2,560		2,731	2,816		2,901	2,944		3,029
IS	Power and ground pads—MPU (2/3 of total pads)	<u>2,048</u>	<u>2,048</u>	<u>2,048</u>	<u>2,048</u>	<u>2,048</u>	<u>2,048</u>	<u>2,048</u>	<u>2,048</u>	<u>2,048</u>
WAS	Total pads—ASIC high-performance	4,800		5,200	5,400		5,800	6,000		6,400
IS	Total pads—ASIC high-performance	4,800	<u>4,800</u>	<u>5,000</u>	5,400	<u>5,400</u>	<u>5,600</u>	6,000	<u>6,000</u>	<u>6,200</u>
WAS	Signal I/O pads—ASIC high-performance	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Signal I/O pads—ASIC high-performance	2,400	<u>2,400</u>	<u>2,500</u>	2,700	<u>2,700</u>	<u>2,800</u>	3,000	<u>3,000</u>	<u>3,100</u>
WAS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	<u>2,400</u>	<u>2,500</u>	2,700	<u>2,700</u>	<u>2,800</u>	3,000	<u>3,000</u>	<u>3,100</u>
Number of Total Package Pins—Maximum [1]										
	Microprocessor/controller, cost-performance	780–2,782		936–3,338	1014–3,616		1217–4,340	1318–4,702		1521–5,426
	Microprocessor/controller, high-performance	2,782		3,338	3,616		4,340	4,702		5,426
	ASIC (high-performance)	4,009		4,810	5,335		6,402	7,042		8,450

14 Overall Roadmap Technology Characteristics

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years [UPDATED](#)

Year of Production		2003	2004	2005	2006	2007	2008	2009
Technology Node			hp90			hp65		
DRAM ½ Pitch (nm)		100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)		120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)		107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††		65	53	45	40	35	32	28
MPU Physical Gate Length (nm)		45	37	32	28	25	22	20
Chip Pad Pitch (micron)								
WAS	Pad pitch—ball bond	40	35	30	25	25	20	20
IS	Pad pitch—ball bond	<u>40</u>	<u>40</u>	<u>35</u>	<u>35</u>	<u>30</u>	<u>30</u>	<u>25</u>
WAS	Pad pitch—wedge bond	30	25	20	20	20	20	20
IS	Pad pitch—wedge bond	<u>30</u>	<u>30</u>	<u>30</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>20</u>
	Pad Pitch—area array flip-chip (cost-performance, high-performance)	150	150	130	130	120	110	100
	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	60	60	40	40	30	30	20
Cost-Per-Pin								
	Package cost (cents/pin) (cost-performance)—minimum-maximum	.75–1.30	.71–1.24	.67–1.17	.64–1.11	.61–1.05	.58–1.00	.55–.96
WAS	Package cost (cents/pin) (Memory)— minimum-maximum	0.30–0.56	0.29–.53	.27–.50	.26–.48	.25–.45	.23–.43	.22–.41
IS	Package cost (cents/pin) (Memory)— minimum-maximum	0.30–0.56	<u>0.30–.53</u>	.27–.50	.26–.48	.25–.45	.23–.43	.22–.41

Table 4b Performance and Package Chips: Pads, Cost—Long-term Years **UPDATED**

Year of Production		2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node		hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
Chip Pad Pitch (micron)										
WAS	Pad pitch—ball bond	20		20	20		20	20		20
IS	Pad pitch—ball bond	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>	<u>25</u>
WAS	Pad Pitch—wedge bond	20		20	20		20	20		20
IS	Pad Pitch—wedge bond	20	<u>20</u>	20	20	<u>20</u>	20	20	<u>20</u>	20
WAS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	100		90	90		80	80		70
IS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	<u>90</u>	--	90		--	80	--	--	70
WAS	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	20		20	20		15	15		15
IS	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	20	<u>20</u>	20	20	--	15	15	<u>15</u>	15
Cost-Per-Pin										
Package cost (cents/pin) (cost-performance)— minimum—maximum		0.52–0.94		0.5–.86	0.5–.77		0.5–0.69	0.5–0.65		0.5–0.59
Package cost (cents/pin) (Memory)— minimum—maximum		.22–.41		0.22–0.36	0.22–0.35		0.22–0.31	0.22–0.29		0.22–0.27

Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Chip Frequency (MHz)							
On-chip local clock	2,976	4,171	5,204	6,783	9,285	10,972	12,369
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	2,000	2,500	3,125	3,906	4,883	6,103	7,629
Maximum number wiring levels—maximum	13	14	15	15	15	16	16
Maximum number wiring levels—minimum	9	10	11	11	11	12	12

Table 4d Performance and Package Chips: Frequency, On-chip Wiring Levels—Long-term Years

UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
	Chip Frequency (MHz)									
	On-chip local clock	15,079		20,065	22,980		33,403	39,683		53,207
	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	9,536		14,901	18,626		29,103	36,379		56,843
WAS	Maximum number wiring levels—maximum	16		16	16		17	18		18
IS	Maximum number wiring levels—maximum	16	<u>16</u>	16	16	<u>17</u>	17	18	<u>18</u>	18
WAS	Maximum number wiring levels—minimum	12		12	12	-	13	14	-	14
IS	Maximum number wiring levels—minimum	12	<u>12</u>	12	12	<u>13</u>	13	14	<u>14</u>	14

Note for Tables 4c and 4d

[1] The off-chip frequency is expected to increase for a small number of high-speed pins that will be used in combination with a large number of lower speed pins

[2] In 2001, high-speed serial communications transceiver devices are achieving chip-board frequencies of 3.125 GHz using CMOS, and 10 GHz using SiGe. In 2002 it is expected that 10 GHz transceivers will be fabricated using CMOS. 40 GHz SiGe devices are expected in 2003. The roadmap for higher levels of integration with wider bus widths, is shown in the High Frequency Serial Communications section in the Test chapter.

[3] The minimum number of wiring levels represents the interconnect metal levels, and the maximum number of interconnect wiring levels includes the Minimum number of wiring levels plus additional optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

Table 5a Electrical Defects—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §	2,216	2,791	3,751	2,532	3,190	2,345	2,954
MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	1,395	1,395	1,395	1,395	1,395	1,395	1,395
# Mask Levels—MPU	29	31	33	33	33	35	35
# Mask Levels—DRAM	24	24	24	24	24	24	24

Table 5b Electrical Defects—Long-term Years **UPDATED**

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
WAS	DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §	3,722		2,954	3,722		2,954	2,233		3,545
IS	DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §	3,722	<u>2,353</u>	2,954	3,722	<u>2,353</u>	2,954	2,233	<u>2,803</u>	3,545
WAS	MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§	1,395		1,395	1,395		1,395	1,395		1,395
IS	MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§	1,395	<u>1,395</u>	1,395	1,395	<u>1,395</u>	1,395	1,395	<u>1,395</u>	1,395
WAS	# Mask Levels—MPU	35		35	35		37	39		39
IS	# Mask Levels—MPU	35	<u>35</u>	35	35	<u>37</u>	37	39	<u>39</u>	39
WAS	# Mask Levels—DRAM	26		26	26		26	26		26
IS	# Mask Levels—DRAM	26	<u>26</u>	26	26	<u>26</u>	26	26	<u>26</u>	26

Notes for Tables 5a and 5b

 D_0 — defect density

§ DRAM Model—Cell factor (design/process improvement) targets are as follows

1999–2004/8×; 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the “6” DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of “Moore’s Law” bits/chip from 2× every 1.5–2 years to 2×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

Table 6a Power Supply and Power Dissipation—Near-term Years [UPDATED](#)

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Power Supply Voltage (V)							
V _{dd} (high-performance)	1.2	1.2	1.1	1.1	1.1	1	1
V _{dd} (Low Operating Power, high V _{dd} transistors)	1	0.9	0.9	0.9	0.8	0.8	0.8
Allowable Maximum Power [1]							
WAS High-performance with heatsink (W)	149	158	167	180	189	200	210
IS High-performance with heatsink (W)	149	158	167	180	189	198	198
Cost-performance (W)	80	84	91	98	104	109	114
Battery (W)—(low-cost/hand-held)	2.1	2.2	2.3	2.4	2.5	2.6	2.7

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 6b Power Supply and Power Dissipation—Long-term Years [UPDATED](#)

Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node	hp45			hp32			hp22		
WAS DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
Power Supply Voltage (V)									
WAS V _{dd} (high-performance)	1		0.9	0.9		0.8	0.8		0.7
IS V _{dd} (high-performance)	1	1	0.9	0.9	0.9	0.8	0.8	0.7	0.7
WAS V _{dd} (Low Operating Power, high V _{dd} transistors)	0.7		0.7	0.6		0.6	0.5		0.5
IS V _{dd} (Low Operating Power, high V _{dd} transistors)	0.7	0.7	0.7	0.6	0.6	0.6	0.5	0.5	0.5
Allowable Maximum Power [1]									
WAS High-performance with heatsink (W)	218		240	251		270	288		300
IS High-performance with heatsink (W)	198	198	198	198	198	198	198	198	198
Cost-performance (W)	120		131	138		148	158		168
Battery (W)—(hand-held)	2.8		3	3		3	3		3

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 7a Cost—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	10.5	7.4	5.3	3.7	2.6	1.9	1.3
DRAM cost/bit at (packaged microcents) at production §	3.8	2.7	1.9	1.4	0.96	0.7	0.5
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	88	62	44	31	22	15.6	11.0
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	53	38	27	19	13.3	9.4	6.7
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	49	34	24	17	12	8.6	6.1
Cost-Per-Pin							
Test Cost							
Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—maximum	3	3	3	3	3	3	3
Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—minimum	1	1	1	1	1	1	2

Notes for Tables 7a and 7b

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two to four years after introduction).

§ DRAM Model—Cell factor (design/process improvement) targets are as follows

1999–2004/8× 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the “6” DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of “Moore’s Law” bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

InTER-generation chip size growth rate model target for Production-phase DRAMs is now “flat” at less than 140 mm², similar to the MPU model. This new flat-chip-size model target requires the bits/chip “Moore’s Law” model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Tables 1c and d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63%, which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above). The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm²/cost-performance at introduction; 140 mm²/cost-performance at production; 310 mm²/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

20 Overall Roadmap Technology Characteristics

Table 7b Cost—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	<u>48</u>	42	38	<u>34</u>	30	27	<u>24</u>	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	<u>22</u>	20	18	<u>16</u>	14	13	<u>11</u>	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
Affordable Cost per Function ++										
WAS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93		0.46	0.33		0.16	0.12		0.06
IS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93	<u>0.66</u>	0.46	0.33	<u>0.23</u>	0.16	0.12	<u>0.08</u>	0.06
WAS	DRAM cost/bit (packaged microcents) at production \$	0.34		0.17	0.12		0.06	0.042		0.021
IS	DRAM cost/bit (packaged microcents) at production \$	0.34	<u>0.24</u>	0.17	0.12	<u>0.08</u>	0.06	0.04	<u>0.03</u>	0.02
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78		3.89	2.75		1.38	0.97		0.49
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78	<u>5.50</u>	3.89	2.75	<u>1.94</u>	1.38	0.97	<u>0.69</u>	0.49
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71		2.35	1.66		0.83	0.59		0.29
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71	<u>3.33</u>	2.35	1.66	<u>1.18</u>	0.83	0.59	<u>0.42</u>	0.29
WAS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.305		2.15	1.52		0.76	0.54		0.27
IS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.30	<u>3.04</u>	2.15	1.52	<u>1.08</u>	0.76	0.54	<u>0.38</u>	0.27
Cost-Per-Pin										
Test Cost										
WAS	Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—maximum	4		4	4		4	4		4
IS	Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—maximum	4	<u>4</u>	4	4	<u>4</u>	4	4	<u>4</u>	4
WAS	Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—minimum	2		2	3		3	4		4
IS	Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—minimum	2	<u>2</u>	2	3	<u>3</u>	3	4	<u>4</u>	4

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

Technology Node—The minimum half-pitch of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated circuits and is selected to define an ITRS Technology Node. For each Node, this defining metal half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other parameters are also important for characterizing IC technology. For example, in the case of microprocessors (MPUs), physical bottom gate length is most representative of the leading-edge technology level required for maximum performance. Each technology node step represents the creation of significant technology progress in metal half-pitch — approximately 70% of the preceding node, 50% of two preceding nodes.

Example: DRAM half pitches of 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, and 22 nm.

For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

An official 2003 ITRS metal half-pitch node indicator, “hpXX,” has been added to differentiate the ITRS definition from commercial technology generation numbers .

Moore’s Law—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a “self-fulfilling” prophecy, “Moore’s Law” has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore’s Law, there is a historically-based “corollary” to the “law,” which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every three years, as suggested by consensus DRAM and MPU models of the 2003 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market “top-down” needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

22 Glossary

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1Mbytes/2001). Logic functionality and L2 cache typically double every three-year generation.

High-performance MPU—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example two cores at 25Mt cores in 2001) with a large (example 4Mbyte/2001) level-two (L2) SRAM. Logic functionality and L2 cache typically double every three-year technology generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law ($2\times$ /two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology-node scaling ($.7\times$ linear, $.5\times$ area) is every three years, an additional device/process design improvement of $.8\times$ per two years must be achieved. This requirement represents a design-related (cell-area-factor) area-reduction improvement of at least -11% per year, and this design-related productivity improvement is in addition to the basic lithography-based area reduction of -21% per year (three-year node cycle).

The present 2003 ITRS consensus target for the rate of increase of DRAM bits/chip has increased from $2\times$ bits/chip every two years to $2\times$ /chip every two and half years average. This slower bits/chip growth is required due to the new consensus 2003 ITRS forecast of cell-area-factor improvement of only negative $4-6\%$ per year on average rather than the 2001 ITRS target of -7% per year average. This results in an average DRAM inTER-generation approximately flat chip-size growth. Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the 2003 ITRS MPU inTER-generation functionality model target is $2\times$ transistors/chip every technology node, in order maintain a flat chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The 2003 ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration-level manufacturing tools and processes. Historically, DRAM products have been demonstrated at $4\times$ bits-per-chip every four years at the leading-edge process technology node, typically two-three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples. Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples ($<1K$). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at $2\times$ functionality per chip every two years (every technology node, in the case of MPUs). In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturer begins shipping volume quantities (initially, at least 10K/month) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (*Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24-36 months prior to volume

production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready 12–24 months prior to Production Ramp “Time Zero” [see Figure 2 in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1Gb/production, 4G/introduction, plus 512Mb/256Mb/128Mb/64Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm²)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm²—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2003 ITRS, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 63% at the production level, and less than 50–55% for smaller previous generation shrunk die at the high-volume ramp level).

DRAM Cell Area (μm²)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 1999: A=8; square of the half-pitch, $f^2 = (180 \text{ nm})^2 = .032 \mu\text{m}^2$; cell area, $C = Af^2 = 0.26 \mu\text{m}^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E = 0.37 \mu\text{m}^2$; therefore, the 1 Gb Chip Size Area = $2^{30} \text{ bits} * 0.37 \text{e-6 mm}^2/\text{bit} = 397 \text{ mm}^2$.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, 1.6×1.6=2.5, etc.).

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm² (High-performance ASIC, Auto Layout)—Number of transistors per cm² designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density

calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os—Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os—Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHz)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first 20K wafer-starts-per-month manufacturing facility.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd} —Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin (\$K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Design

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DESIGN

2004 UPDATE HIGHLIGHTS

This update includes (a) a revised "General" design technology requirements (revised), with some new rows, and new explanations as footnotes for each row, but no changes in the values of existing rows, (b) a new design technology solutions table after the requirements table, which includes a definition of each row, (c) a new Design For Manufacturability (DFM) section with completely new content, and (d) an update of the verification section.

[Link to the 2003 ITRS Design chapter](#)

WORKING GROUP SECTION UPDATES

DESIGN FOR MANUFACTURABILITY **[NEW SECTION ADDED]**

Increasing variability, mask cost and data explosion, and lithography hardware limitations, are posing significant design challenges for the manufacturability of integrated circuits:

1. Architecture challenges—architectural redundancy will be required due to the difficulty in making circuits yield. It will be hard to do much more at this level of abstraction.

2. Logic and circuit challenges—digital and mixed-signal adaptive circuits will be increasingly necessary. Statistical design, including power and timing convergence will be fundamental. But it will be hard to make work without addressing two primary challenges: characterization and modeling inputs to statistical design tools; and the evolution from statistical analysis to optimization with the subsequent increase in computation complexity. Finally, statistical timing tools and statistical optimization methods must model actual variations rather than crude and inaccurate abstractions. The composition of variations during statistical analyses and optimizations should match the methods used for initial decomposition via statistical metrology techniques during process characterization. A mismatch between composition and decomposition will introduce unnecessary error and impart dubious value to the computationally costly results.

3. Layout and physical design challenges— First, the complexity of design rules checking is increasing (include graph). Rules have evolved to a two-tier system (required versus suggested rules) and may need to evolve either to a three-tier system or to a no-tier system (where rules are not pass-fail but provide a point in a curve and the designer needs to apply criteria for tape-out). All this will need to be done without increasing designer-perceived complexity. Second, the limitation in lithography hardware resolution will require design flows to more explicitly account for the impact of Resolution Enhancement Techniques (RET). RET tools, such as OPC and CMP fill, must become explicitly aware of circuit metrics such as timing and power. Such awareness aligns the tools to overall product goals and enables yield enhancements, manufacturing cost reductions, and mask data preparation time. As an example, OPC would be applied only to features in critical timing paths. This entails a tighter flow integration to communicate circuit intent downstream, and to avoid independent modifications by several tools leading to incorrect results.

4. Yield prediction and optimization as design challenge— The ground rules as specified are not longer 'hard numbers', where designer and EDA tools used to consider as strict 'hard' numbers. To archive reasonable mature yields and steep ramp capability a strategy for meaningful relaxation have to be used. These 'recommended' rules have been derived from the interaction of the design layout and wafer process requirements, such as alignment tolerances, optical proximity corrections, RET enhancements and many other constrains. DFM measures acts different for each design because it impacts power, area and speed as you tune for yield. During design process the mutual interaction off yield, area, power and speed must be analyzed and a commercial useful trade off must be found. This involvement of DFM measures effecting the functional yield and parametric yield must be integrated as a new optimization feature into the design flow and tools, not as post processing that allows only limited results and is time consuming. That means that yield prediction has to be integrated into design tools for Synthesis and Place & Route to consider all design targets to optimize simultaneously yield, performance, power, signal integrity and area (Yield as explicit new design target).

2 Design

Table A Design For Manufacturability Challenges ADDED

<i>Challenges ≥ 50 nm/Through 2009</i>	<i>Summary Of Issues</i>
Mask cost	ALL—CAD tools that explicitly account for mask cost in their algorithms
Data explosion	ALL—RET tools that are explicitly aware of circuit metrics (timing, power)
Limitations of lithography hardware resolution	ALL—RET-aware CAD tools, radically-restricted design rules, including yield prediction and optimization
Voltage supply and threshold variability	ALL—Statistical analysis tools and flows that account for this variability, including yield prediction and optimization
BEOL Planarization and dimensional variability	ALL—Statistical design tools and flows that account for this variability; including yield prediction and optimization
Heterogeneous components (analog, MEMS, eRAM)	
Leakage as a limiter of manufacturability	ALL—Statistical leakage analysis and optimization tools
<i>Additional Challenges < 50 nm/Beyond 2009</i>	
Leakage as a limiter of manufacturability	ALL—Statistical leakage optimization tools
Uncontrollable CD and doping variability	ALL—Statistical parametric optimization tools
Extreme device and circuit variability	ALL—Architectures fundamentally resistant to variability (redundancy, ECC)
Critical need to integrate RET into design	ALL—RET-aware CAD tools
Package, system, and software variability	ALL—adaptable and redundant circuits that can adapt to these variations
BEOL planarization and dimensional variability	ALL—post-tapeout RET that interacts with synthesis, timing, and P&R

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

VARIABILITY MODELING AND ROADMAP

Since variability is expected to be the source of multiple critical DFM challenges, a systematic method to roadmap required and/or desired variability trends will become a crucial component of the overall Design roadmap. It may also allow for design-manufacturing “co-roadmapping”, which may help gather indications of whether our industry should invest in variability reduction or in design productivity improvements. The requirement for such a framework is underlined by the sensitivity of variability-related information for industry participants. Since the design community needs to view variability from their parameter-based perspective, such a variability framework needs to be multi-level, i.e., it needs to cover multiple levels of design abstraction.

A Variability Roadmap Framework (VRF) is being developed by the Design TWG as illustrated in Figure 19. In this Framework the following three levels of abstraction have initially been considered:

- *Circuit/chip level:* this is the abstraction level most relevant to designers. Ideally, timing and power consumption variability for a given circuit would be road-mapped at this level, based on lower-level parametric variations.
- *Device level:* since circuits are composed of devices, at this level device-related parameters are roadmapped, such as the threshold voltage V_t , or the off-current I_{off} .
- *Physical level:* this is the level closest to the design-manufacturing interface, where parameters such as CD or effective device length (L_e), and actual doping level (N_A) are road-mapped. These parameters’ variability stems from some of challenging issues enumerated above, including lithography hardware resolution limitations, and the inability to control the exact number of dopants in a channel.

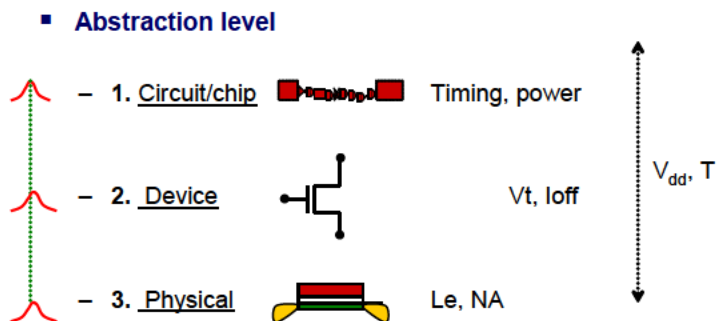


Figure a Possible variability abstraction levels ADDED

In this framework, the modeling process can be symbolically described as

$$\Delta \text{ outputs} = \text{model}(\Delta \text{ inputs}) \quad [1]$$

Based on published approximated models, this model is based on a simplified gate + wire circuit slice where parameters are decomposed into gate-related and wire-related parameters. Performance is analytically modeled in the current model as total delay, which in turn is decomposed into gate delay and wire delay. Delay variability is modeled as a delta that is statistically computed from a statistical distribution of individual delay values that stems from “simulating” distributions of the input parameters in a Monte Carlo style. Model inputs include gate channel length and width, and oxide thickness; wire width, length, and thickness; ILD thickness, and wire sheet resistance.

Among other applications, this framework will be used for circuit performance variability trending. For example, estimated delay variability will be estimated over time for two possible scenarios: 10% required CD (actual channel feature length) variation, and 20% required CD variation. In this particular illustration, the model could indicate that circuit performance variability does not seem to vary very significantly with the CD tolerance requirement, which might suggest the possibility of a relaxation of the requirement.

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Table 13 Near-term Breakthroughs in Design Technology for AMS

<i>Field Of Breakthrough</i>	<i>2003</i>	<i>2004–2005</i>	<i>2006–2007</i>
Specification, validation	Mixed-signal description languages	Multi-language support	Complete specification-driven design flow
Architectural design	Algorithm-oriented design	Language-based performance evaluation	Synthesizable AMS description
Mixed A/D and RF physical design	Procedural layout generation	Design centering, performance estimation	Constraint-driven synthesis: behavior to layout
Parasitic extraction, modeling, simulation	EMI simulation	2D/3D modeling, order reduction	Fault-tolerant circuit architectures, robustness

Table 14 Design Process Challenges

<i>Challenges ≥ 50 nm/Through 2009</i>	<i>Summary Of Issues</i>
Silicon Complexity: devices and interconnects	All—Exponential increase in leakage power S, P, A—Power density and distribution All—Technology and library characterization S, P, A—High-frequency noise analysis S, P, A—Transmission-line interconnects All—eDRAM, eFPGA, SiGe, optical, MEMS
System Complexity: number of states, design diversity	S, P—Verifying systems with exploding number of states S, P, A—Concurrent multi-factor analysis and optimization S, P—Scalable algorithms S, A—Design and test of mixed analog and digital designs All—Complex package analysis S, A—Integrating A/D tools
Design Productivity	S—Integrating third party components S, P—Design tool interoperability S, P—Early analysis and verification methods
Time-to-Market	S, A—Support for platform-based design S, P, A—Exploiting parallel processing
<i>Challenges < 50 nm/Beyond 2009</i>	
Manufacturability	All—Cross-chip variability All—Sub-wavelength mask correction (AltPSM, OPC, RET) All—Design for yield and manufacturability All—Standards for sharing design and manufacturing data
System-level Design	S—Common hardware/software (HW/SW) representation S—SW synthesis, HW/SW optimization

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

Table 14 summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S = SOC, P = MPU, A = AMS, M = Memory). The remainder of this section gives explanatory comments.

Table 15 System-level Design Challenges

<i>Challenges ≥ 50 nm/Through 2009</i>	<i>Summary Of Issues</i>
System complexity	S—Higher-level abstraction and specification S—Dynamism and softness S, A—System-level reuse S, A, P—Design space exploration and system-level estimation S—Efficiency of behavioral synthesis and software compilation S—Automatic interface synthesis
System power consumption	P, S—Energy-performance-flexibility trade-offs P, S—Novel data transfer and storage techniques
Integration of heterogeneous technologies	S, P, A—Codesign (HW–SW, chip-package-board, fixed-reprogrammable) A, S—Non-scalability of analog circuits; analog behavioral modeling and synthesis P, S, A—Top-down implementation planning with diverse fabrics (digital, AMS, RF, MEMS, EO, SW)
Embedded software	S—SW–SW codesign onto highly programmable platforms S—System capture and abstraction S—New automation from high level description to HW–SW implementations, including SW synthesis S—Formal verification for SW S—HW–SW coverification
Links to verification, test and culture	S—Integration-oriented verification and test architectures S, P, A—Divergent design practices and cultures
<i>Additional Challenges <50 nm/Beyond 2009</i>	
System complexity	S, P—Communication-centric design and network-based communications on chip All—Design robustness
System power consumption	P—Non-scaling of centrally organized architectures S—Building large systems from heterogeneous SOCs
Integration of heterogeneous technologies	S—Total system integration including new integrated technologies (MEMS, electro-optical, electro-chemical, electro-biological or organic)

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

Table 16 Logical, Circuit, and Physical Design Challenges

<i>Challenges ≥ 50 nm/Through 2009</i>	<i>Summary Of Issues</i>
Efficient and predictable implementation	P—Scalable, incremental analyses and optimizations P, S—Unified implementation/interconnect planning and estimation/prediction P, S—Synchronization and global signaling S, A, P—Heterogeneous system composition P, S—Links to verification and test
Variability and design-manufacturing interface	P, S, A—Uncertainty of fundamental chip parameters (timing, skew, matching) due to manufacturing and dynamic variability sources All—Process modeling and characterization P, S—Cost-effective circuit, layout and reticle enhancement to manage manufacturing variability
Silicon complexity, non-ideal device scaling and power management	P, S—Leakage and power management All—Reliability and fault tolerance, soft error P, S—Analysis complexity and consistent analyses / synthesis objectives
Circuit design to fully exploit device technology innovation	P—Support for new circuit families that address power and performance challenges P, S—Implementation tools for SOI A, S—Analog synthesis
<i>Additional Challenges < 50 nm/Beyond 2009</i>	
Efficient and predictable implementation	S—Reliable, predictable fabric- and application-specific silicon implementation platforms S—Cost-driven implementation flows
Variability and design-manufacturing interface	P, S, A—Increasing atomic-scale variability effects
Silicon complexity, non-ideal device scaling and power management	P—Recapture of reliability lost in manufacturing test
Circuit design to fully exploit device technology innovation	P, A—Increasing atomic-scale effects P, S, A—Adaptive and self-repairing circuits A, S—Low-power sensing and sensor interface circuits; micro-optical devices

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

DESIGN VERIFICATION UPDATED

Design verification is the task of establishing that a given design accurately implements the intended behavior. The prevailing view by much of the semiconductor industry is that design verification plays a relatively minor supporting role to the design process. (Possibly, such a view is reflected in the very structure of this document.) Current reality, however, is markedly different. Verification has become the dominant cost in the design process. On current projects, verification engineers outnumber designers, with this ratio reaching two or three to one for the most complex designs. Design conception and implementation are becoming mere preludes to the main activity of verification.

This unfortunate situation is the result of two processes. First, the functional complexity of modern designs is increasing at a breathtaking pace. Design size is growing exponentially with Moore's Law. In the worst case, functional complexity, as measured by the number of distinct states of the system that must be verified, can grow exponentially in the size of the design, producing a doubly exponential blow-up.¹ Second, the historically greater emphasis on other aspects of the design process has produced enormous progress (automated tools for logic synthesis, place-and-route, and test pattern generation, etc.), leaving verification as the bottleneck. Without major breakthroughs, verification will be a non-scalable, show-stopping barrier to further progress in the semiconductor industry.

The overall trend from which these breakthroughs will emerge is the shift from ad-hoc verification methods to more structured, formal processes. The mainstream methodology used in industry today attempts to verify the functionality of a system design by repeatedly building models, simulating them on an ad hoc selection of vectors, and then patching any bugs that happen to be triggered. However, such a trial-and-error verification methodology lacks the metrics that make the verification process predictable and repeatable. More structured approaches relay on planning the verification effort, modeling and measuring coverage as verification tasks are being executed. This deliberate verification strategy makes use of simulation engines at the unit, chip and system level as well as formal engines at the unit level.² Formal verification techniques are starting to gain momentum and they are complementing simulation methods in the process of verification. Formal methods span multiple aspects of verification: from a formalized verification process, to a formal notation for specification and verification and formal solvers and proof techniques.

In tackling the complexity of very complex systems, and in particular, systems-on-a-chip, a "hierarchical" verification methodology seems to be needed, along with the development of specific methods and tools associated with each level of the hierarchy. In this context, the design and implementation pyramid can be summarized roughly as follows: 1) Module level (structural, dataflow and behavioral module description and synthesis) where the verification tools must prove the correctness of systems in the range of 10K to 500K logic gates. 2) Sub-System level (for the most part, this is the result of structural composition of modules) producing systems with 100k to 10M logic gates. 3) System/Full chip level (obtained by composing sub-systems) producing designs of 1M to more than 100M logic gates. In a hierarchical verification approach different verification techniques would be used at each design level: At the module level, the goal is to produce high-quality modules through the formal verification of properties and assertions. For sub-systems, verification would entail a mix of property verification for the interface and simulation with constrained random pattern generation. Property verification at the sub-system level could be achieved in the future, for instance, through the definition of aggressive automatic design-abstraction techniques, and of automatic techniques for the refinement of such abstractions, driven by counter-examples, which would allow proving sub-system properties while posing a minimum demand on the verification engineering resources. At the system level, simulation-based assertion checking paired with coverage metrics seem the most appropriate among the techniques available. Technological progress depends on developing rigorous and efficient methods to achieve these verification goals (the bulk of formal and semi-formal verification research today), and eventually codifying reliable, predictable engineering practices that simplify many verification challenges. Tables 17 and 18 summarize the main challenges in design verification. The remainder of this section provides explanatory comments.

¹ There are many variations that arrive at this conclusion. For example, a new design that requires doubling the number of transistors on a chip is likely to also double the number of latches on the chip, which likely means roughly squaring the number of reachable states of the design. This analysis assumes that the correct behavior can be verified by examining the set of reachable states of the system, or a similar computation. If verifying correct behavior requires reasoning over sequences of states, the computational challenge will be even worse.

² This argument applies to hardware emulation as well as to conventional simulation. Hardware emulation buys several orders of magnitude improvement in "simulation" speed, providing an invaluable aid to verification. It also often allows an earlier start to system integration and software development. An emulation system, however, still runs vectors one-at-a-time, so it cannot possibly provide a scalable, long-term solution to the verification problem.

Table 17a Design Verification Challenges—Near-term **UPDATED**

Challenges ≥ 50 nm/Through 2009	Summary Of Issues
Increased verification capacity	S, P, A—Verification complexity is double-exponential in design size S, P, A—Need high coverage as well as capacity to handle large designs S, P, A—Semi-formal techniques
Robust verification tools	S, P, A—Highly unpredictable verification algorithms demand improved heuristics and characterizations of problem difficulty
Verification metrics	S, P, A—Code, structural and functional coverage S, P, A—Realistic bug models are needed, along with algorithms to determine bug coverage
Software verification	S—Software intrinsically more difficult to verify S—Traditional software verification techniques inapplicable S—Integrated hardware/software systems S—Design for verifiability
Verification reuse	S—Must allow reuse of verification of IP blocks S—Specify abstract behavior of IP blocks S—Specify environmental constraints of IP blocks S—Hierarchical verification algorithms
Verification methodology	S, P—Different cost-benefit trade-off (higher cost acceptable) S, P—Need exceptionally high capacity S, P—Must be very predictable due to long design cycle and pipelined development teams
Design for verifiability	S,P—Will be necessary sooner than for other system drivers; specialized techniques are likely
Greater concurrency	S,P—Far more concurrency in new processors greatly increases verification complexity

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

DESIGN VERIFICATION CHALLENGES—NEAR TERM (>50 nm)

Many of the most important challenges for verification are relevant to most or all system drivers. In the near-term, eight primary issues (1–8 below) center around making formal and semi-formal verification techniques more reliable and controllable. In particular, major advances in the capacity and robustness of formal verification tools are needed, as well as meaningful metrics of the quality of verification. In the longer term, four primary issues (9–12 below) center around raising the level of abstraction and broadening the scope of formal verification. These longer-term issues are actually relevant now, but the near-term challenges are already crises. In general, all of the verification challenges apply to SOC. In addition, the following near term challenges are especially important for SOC. MPUs present a distinct verification challenge, both because of their leading-edge complexity, and because of the unique economics of an incredibly complex design that is produced in incomparably high volumes. As a result, different, domain-specific verification challenges and opportunities exist, both near- and long-term.

1. *Capacity*—Figure 19 relates the current landscape of available verification tools and design granularity. The horizontal axis presents increasing design complexity, from module components, to sub-systems, multiple modules connected together providing some high-level functionality, to systems, complete systems-on-a-chip integrating multiple functionalities on a single die, and to the application software running on the system; the vertical axis indicates the verification techniques available. Conventional simulation-based methods³ span a large range; they are practically used

³ “Conventional simulation” here refers to verification techniques based on simulating possible behaviors of the system one-at-a-time. “Formal verification” refers to any techniques, such as symbolic simulation, symbolic trajectory evaluation, model checking, and theorem proving, that provide the effect of an exhaustive analysis of all possible behaviors of the system. An occasionally useful distinction can be drawn between theorem-proving approaches, which tend to provide the greatest expressive and analytical power at the expense of requiring substantial human expertise, versus the other approaches, which tend to trade off theoretical power for greater automation. “Semi-formal” refers to a broad range of techniques that attempt to handle larger designs by sacrificing complete, formal coverage, usually by blending techniques from formal verification and conventional simulation.

for anything from module to full-system verification. However, the quality of the results varies: For small modules it is possible to run many simulation vectors in a short time and thus achieve a fairly good coverage of the design under verification. At the system level the performance of simulation is very low, since the complexity of the algorithms involved is linear on the design size and the number of simulation vectors. Thus, for very complex systems, only a few simulation vectors can be run within a reasonable amount of time, and the fraction of design coverage they provide is even much smaller considering the complexity of the system that is being simulated. Formal verification can achieve very high coverage, granted that a broad set of properties are in place, targeting the various aspects of the system. The downside of these techniques is their limited scalability that usually cannot go above the module level. Semi-formal verification attempts to blend formal and simulation-based techniques. As the Figure shows, they present generally better capacity, sometimes at the cost of lower design coverage. For very complex systems and when the project involves software development, software tools are insufficient to provide any confidence in the correctness in the system. Solutions used at this level include FPGA-based rapid prototyping and/or a silicon production of the hardware. The challenge is to create new solutions that together provide high coverage at all levels of complexity. The two orthogonal methodologies of formal verification and simulation in use today have both important downsides: while formal tools can only handle small to medium size designs, simulation-based tools can simulate designs of almost arbitrary complexity, but they provide a vanishingly small coverage even with extremely long simulation times. Emulation and rapid hardware prototyping perform several orders of magnitude faster than software logic simulators, thus providing the ability to achieve higher coverage. However, the improvement is only a constant factor and does not scale at the same rate as design complexity.

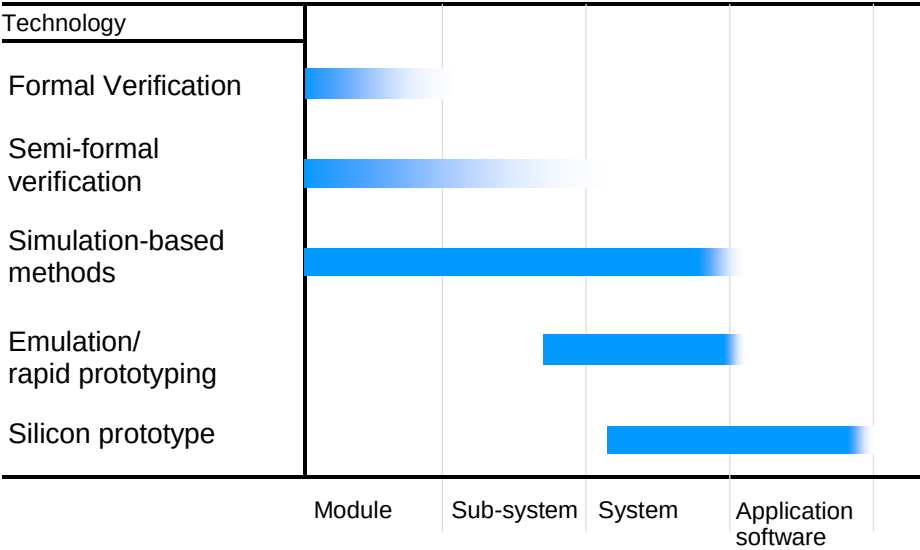


Figure b Current Verification Tool Landscape ADDED

2. *Robustness*— A crucial aspect of current verification solutions that is not shown in Figure 19 is their reliability. On one hand, simulation-based methods are fairly predictable, because their execution time per simulation vector scales linearly with design complexity. Their performance, thus, will linearly decrease as we move towards the most complex design levels. Emulation techniques present a similar trend, while silicon prototypes are consistently reliable. On the other hand, formal verification techniques depend on highly temperamental heuristics, in order to cope with the complexity of the verification problem. For any given pair of design and verification algorithm, even an expert can be hard-pressed to determine whether the verification algorithm will complete. Common measures of problem size, such as transistor, gate, or latch counts, correlate only vaguely with formal verification complexity; it is easy to find designs with less than one hundred latches that defy all known verification methods, as well as designs with thousands of latches that can be verified easily. Such unpredictability is not acceptable in a production environment. A crucial verification challenge is to make the verification process more robust. This can take the form of either improved heuristics for the verification algorithms, or improved characterization of the difficulty of verifying a given design, leading to methodologies for easy-to-verify design.

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3. *Verification metrics*— An important near-term verification challenge is the need to quantify the quality of the verification effort. In particular, a meaningful notion of coverage is needed. Multiple types of coverage metrics are available, each with their own benefits and limitations:

- Code coverage is concerned with measuring which fraction of the design source code has been stimulated during simulation (for example, lines of code, expression coverage). Variants of line coverage are concerned with covering all components of expressions in the code, or all cases in switch statements, etc...The limitation of line coverage is in its projecting a dynamic simulation execution to a static source code, thus missing many potential problems that could be still present because of all the possible paths of execution available during simulation.
- Structural coverage, such as state or pair arc coverage. State coverage focuses on the finite state machines of the design and measures which states have been covered by simulation. However, it is generally not possible to consider the whole design as a single finite state machine, rather only a few machines are considered by coverage. The downside is that while the coverage provides good results for single machines, combinations of states resulting from products of multiple machines are not considered.
- Functional coverage targets each of the design's functionalities. Since these differ for each distinct design, the specific definition needs to be provided by the verification team based on the design's specification. The quality of the result is thus dependent also on the quality of the coverage definition.

Code and structural coverage metrics quantify aspects of the designs that do not necessarily imply its correctness. Functional coverage potentially could achieve this goal of measuring the fraction of a design's functionality that has been verified. However, the challenge is in the definition of a good functional coverage. In the current landscape, there is a lack and a need for a common foundation metric for functional coverage in a unified environment, so that achieving a certain level of coverage in a design could have a meaning beyond the specific functional coverage used in that particular design. Moreover, there is no general methodology in designing the functional coverage units; an abstract fundamental model to use as a guideline during the development is needed and could support the development methodology. Ultimately, there is a need for a defect model for functional bugs, much like there is a defect model for testing, to support the development of coverage and a unified metric for verification.

4. *Software*— The verification of complex systems, such as systems-on-a-chip (SOC) entails the verification of the hardware components, of the hardware/software interface and of the application software running on the system. The software components of an SOC can be divided into application software, running over an operating system, or, in general, a layer that is hardware-independent, and a lower-level hardware-dependent software, such as drivers, etc. Because in these systems the software layer could provide much of the functionality, a major challenge in SOC verification is how to verify software and the hardware/software interface. Presently, software development is not as rigorous as hardware development in terms of design reviews, analysis tools, and testing. Software is intrinsically harder to verify: it has more complex, dynamic data and an enormous state space. Techniques used today include “on-chip-verification”, that is, running the software on a production version of the hardware components to verify the software. While this technique is required by the intrinsic complexity of software, and allows very fast simulation, its downside is that software verification can only happen very late in the design cycle. Classical formal techniques for software verification are still too labor-intensive to be widely applicable for SOC, to attack systems with such large state spaces, and require very aggressive abstraction techniques. The verification of the hardware/ software interface is a challenge on its own, since it requires verifying the two domains together, a task of enormous complexity. To make this task manageable, there is a need for techniques that provide a proper abstraction of the interface activity, verification techniques to check the correctness of the abstracted driver layers, and assertion checking for drivers' invariants at the non-abstract level. The near-term challenge will be to develop techniques that allow verification of even elementary and low-level pieces of software. The longer-term challenge will be to develop robust verification methods for software, and hardware/ software interfaces, as well as an understanding of design-for-verifiability as applied to software.

5. *Reuse*—Pre-designed IP blocks promise to allow assembling SOC's of unprecedented complexity in a very short time. The major challenge is to develop the corresponding verification methodology to allow rapid verification of a system assembled from pre-designed (and pre-verified) blocks. Key issues are how to rigorously and completely describe the abstract behavior of an IP block, how to describe the environmental constraints assumed by the IP block, and how to exploit the hierarchy to simplify verification. Some IP components have started to ship with associated verification IPs, from standard protocols verification IPs, to abstract models for general IP blocks, protocol checkers to check environmental constraints surrounding the block, to transaction generators. However, these are still preliminary attempts,

while there is a need for consistent availability of verification IPs associated with any IP block in order to develop a reuse methodology. Besides verification components associated with IP blocks, there is some availability of independent verification IPs, such as environment generators for specific protocols. Near-term progress will most likely occur for standardized IP interconnects, such as on-chip buses, but the general problem for arbitrary IP block interfaces must be eventually solved.

6. Specialized verification methodology—The biggest issue in design verification is that all currently known algorithmic solutions are running out of capacity with respect to the designs being developed today. The only foreseeable way to overcome this issue in the short term is with an adequate verification methodology. Current trends in this direction include coverage-driven verification, both for simulation-based verification and semi-formal verification, more in use today than in the past; specification documents in formal notation, that make easily available the set of formal properties to be verified in the implementation; coverage model templates. Many challenges are still to be solved to obtain a sufficiently robust and complete methodology. For instance, there is a need for ways to obtain consistent abstraction techniques of design components, interfaces, etc. that do not drop key aspects of the design in the abstraction, and, obviously, these aspects depend on the context where the abstraction is used. Formal specifications are starting to be developed; however, a major challenge is the completeness of such specifications, a challenge that becomes even more compelling in a world where different IP components in the same system are developed by completely unrelated design teams. The acceptance of new verification methodologies is progressing slowly, even the basic deployment of formal properties in a design is a challenge since it often requires a global understanding of some specific aspect of a design, which involves additional effort on the development team. Finally, verification methodology is ultimately an evolving target that can only provide a risk reduction to the development, not a guarantee of correctness through a well-defined recipe.

7. Specialized design-for-verifiability—To enable more effective verification, a few specialized activities in design for verifiability are already foreseeable. For instance, facilities for software and/or hardware debug can be put in silicon. In this direction there is preliminary work being done on self-checking processors, in which a small watchdog processor verifies the correct execution of the main processor. For mixed-signal designs, the insertion of loop-back modes to bypass the analog portion of the design allows to verify the system as a fully digital design. The use of synchronizers, in particular at the software level forces tasks not to proceed independently past the synchronization points, creating checkpoints for verification and reducing the searchable state space. In MPU designs synchronizers would reduce the complexity of verifying speculative execution systems. The challenges in this area will be the development and the adoption of design-for-verifiability techniques for a few major domains. Efforts are also made in developing design methodologies by incremental refinement to produce systems that are correct-by-construction; however, it is not clear how automatic the refinement process can be made, while, on the other hand, manual intervention is a potential source of design errors.

8. New kinds of concurrency—As MPU designs become more complex, new kinds of concurrency become important. Already, many of the bugs that elude verification relate to cache coherence and other concurrency issues. New designs greatly complicate the verification process by increasing the level of concurrency via techniques such as chip-level multiprocessing and on-chip cache coherence protocols, and simultaneous multithreading. In the future, new kinds of concurrency both at the intra-processor level and in multi-processor systems, or in other hardware context will present difficult challenges to verification. There is a need for new models of failure to grasp this additional level of complexity. The solution will probably require a mix of hardware and software techniques to reduce the complexity of the interactions and make the concurrent protocols verifiable.

Table 17b Design Verification Challenges—Long-term [UPDATED](#)

Additional Challenges <50 nm/Beyond 2009	
Design for verifiability	S, P, A—New methodology needed S, P, A—Characterize and minimize performance and area impact
Higher levels of abstraction	S, P, A—New algorithms needed S, P, A—Complexity of designs enabled by higher-level design S, P, A—Equivalence checking vs. RTL
Specification for verifiability	S, P, A—Specifications of correctness will become unmanageable S, P, A—Need to understand what kinds of specifications are most understandable S, P, A—Need to consider how to make specifications modular and modifiable
Verification in the presence of non-digital effects	S, P, M, A—Hybrid systems verification for analog effects S, P, M, A—Hybrid systems verification for analog properties S, P, M, A—Verification of probabilistic systems
Heterogeneous systems	A, S—How to model, analyze, and verify MEMS, EO devices, and electro-biological devices
Analog-Mixed signal	A—Extremely primitive state-of-the-art forces difficult hybrid-systems issues into near term
Soft failures	S, P, M—Reliable systems in face of soft errors
Verification of redundancy	S, P, M—Sufficient reliability in face of soft errors

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

DESIGN VERIFICATION CHALLENGES—LONG TERM (<50 nm)

1. *Design for verifiability*— As the solutions to the near-term challenges produce understandings of what is easy or hard to verify and how design errors occur, the longer-term challenge arises of how to codify that understanding into producing easy-to-verify designs. Without design-for-verifiability, it is unlikely that verification will be tractable for the designs envisioned beyond 2007. Major changes in methodology may be required, and some performance degradation is likely. A useful analogy is to sequential testability, where the computational intractability of sequential ATPG has resulted in near-universal adoption of scan-based testing.

2. *Higher levels of abstraction*— As design moves to a level of abstraction above RTL, verification will have to keep up. The challenges will be to adapt and develop verification methods for the higher-levels of abstraction, to cope with the increased system complexity made possible by higher-level design, and to develop means to check the equivalence between the higher-level and lower-level models. This longer-term challenge will be made much more difficult if decisions about the higher-level of abstraction are made without regard for verification (e.g., languages with ill-defined or needlessly complex semantics, or a methodology relying on simulation-only models that have no formal relationship to the RTL model).

3. *Specification for verifiability*—A continuing challenge for design verification is how to specify the desired behavior of a design. Current available notations for specification are not powerful enough to approach this problem in a generalized way. A deeper understanding of what makes a specification clear or opaque, modifiable or intractable will be needed to guide development of languages that are used to specify ever more complex designs. For instance, there is a need for automatic ways to check the self-consistency of a specification document, so that different specifications don't state conflicting requirements. In addition, specific training is needed for designers to use these specification notations and to be able to develop formal specifications consistently.

4. *Verification in presence of non-digital effects*— To date, design verification has mainly focused on the discrete behavior of digital systems. The dual challenges of silicon complexity and system complexity will force future verification efforts to analyze a broader class of aspects. The complexity of silicon integrated circuit systems is making the clean, digital abstraction of a VLSI system increasingly precarious. Analog electrical effects will impact performance and, eventually, functionality. The existing simulation methodology (SPICE) for analyzing these effects is too slow, and

may become unreliable as smaller devices become increasingly sensitive to process variations. In this direction there is preliminary work being done on architectural simulation of microprocessors, in which the high-level architectural simulator, interacts with a low-level context-specific simulator to acquire metrics such as timing and voltage, which are then fed back for overall system evaluation with minimal performance impact. In the long term, formal techniques will be needed to verify these issues at the boundary of analog and digital, treating them as hybrid systems.⁴ Similarly, at the highest-levels of design, system complexity dictates that future verification tasks will likely require specifying and verifying analog and probabilistic behaviors (such as quality of service guarantees in a network processor). Thus, there will be the challenges of hybrid systems and probabilistic verification.

5. Heterogeneous systems— The development of new technologies that are placed side-by-side to a digital design in a silicon die presents a whole set of new challenges. Examples are MEMS, electro-optical devices, and electro-biological devices. These new components will require modeling of both the interface between the digital portion and the non-digital components and a proper abstraction of the non-digital system behavior in order to still be able to verify the digital portion of the system.

6. Analog-Mixed signal— Today analog systems are mostly verified through classic systems analysis tools for continuous systems, through system modeling and analysis in the frequency domain. The bulk of verification happens in the post-design phase, by verifying test dies with analog lab equipment. Mixed-signal designs undergo separate verification activities for the digital and analog portions. In the future, mixed-signal systems will become a more relevant fraction of all silicon developments, bringing the development of proper verification methodologies in this arena to a critical level. The challenge in this area is in tying the verification of the analog portion of a system with its digital counterpart. One of the requirements in achieving this goal is in bridging the current performance gap between digital and analog simulation.

7. Soft failures— In the long term there is a need to develop verification techniques that can provide information on a system's reliability in presence of soft errors.

8. Verification of redundancy— The quantifiable evaluation of the reliability of a redundant system, and the estimation of the level of redundancy needed to achieve a certain level of reliability is particularly important for safety-critical application. In the future, the increased complexity of electrical effects in a system performance and correctness will make these evaluations even more important, even for non safety-critical designs.

⁴ Hybrid systems have both complex discrete behavior (e.g., finite-state machines) as well as complex continuous behavior (e.g., differential equation models). The discipline borrows techniques from both discrete formal verification as well as classical control theory.

Table 18 Design Test Challenges

<i>Challenges ≥ 50 nm/Through 2009</i>	<i>Summary Of Issues</i>
Effective speed test with increasing core frequencies and widespread proliferation of multi-GHz serial I/O protocols	P, S—Continuation (avoidance) of at-speed functional test with increased clock frequencies P, S—At-speed structure test with increased clock frequencies P, S, A—DFT, test and on-chip measurement techniques for multi-gigahertz serial I/Os and non-deterministic interfaces
Capacity gap between DFT/test generation/fault grading tools and design complexity	P, S—Better EDA tools for advanced (open, delay, etc.) fault models P, S—DFT to enable low-cost ATE P, S—Non-intrusive logic BIST (including advanced fault models) A—AMS DFT/BIST, especially at beyond-baseband frequencies
Quality and yield impact due to test process and diagnostic limitations	P, S—Power and thermal management during test P, S—Fault diagnosis and design for diagnosability S—Yield improvement and failure analysis tools and methods All—Increasing difficulty to fault isolate and root cause yield limiting defects
Signal integrity testability and new fault models	P, S—Signal integrity (noise, interference, capacitive/inductive coupling, etc.) testability A—Fault models for analog (parametric) failures
SOC and SIP test	S—Integration of SOC test methods into chip-level DFT S—Integration of multiple fabric-specific test methodologies in cost-effective manufacturing flows A—DFT, BIST and test methods compatible with core-based SOC environment and constraints M—Embedded memory (DRAM, SRAM, Flash) built-in self-diagnosis and self-repair All—Test reuse in context of higher integration
<i>Additional Challenges < 50 nm/Beyond 2009</i>	
Integrated self-testing for heterogeneous SOC and SIPs	A—Test of multi-gigahertz RF front ends on chip S—Use of on-chip programmable resources for SOC and SIP self-test S, A—Dependence on self-test solutions for SOC (including RF and analog) A— (Analog) signal integrity test issues caused by interference from digital to analog circuitry S—Test methods for heterogeneous SOC and SIP including MEMS and EO components
Diagnosis, reliability screens, and yield improvement	A—Diagnosis and failure analysis for AMS parts P, S—Electrical automated fault isolation techniques below gate level P, S—Design for efficient and effective burn-in to screen out latent defects P, S—Quality and yield impact due to test equipment limits P, S—New timing-related fault models for defects/noise
Fault tolerance and on-line testing	P, S—DFT and fault tolerant design for logic soft errors S—Logic self-repair using on-chip reconfigurability S—System-level on-line testing

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

Table 19 Additional Design Technology Requirements UPDATED

Year of Production	2003	2004	2005	2006	2007	2008	2009	2012	2015	2018	Driver
Technology Node		hp90			hp65						
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50	35	25	18	
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50	35	25	18	
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28	20	15	10	
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	14	10	7	
Add Complexity --> (system) % of memory		47%	50%	53%	55%	58%	61%	65%	65%	65%	
WAS SOC new design cycle (months)	12	12	12	12	12	12	11	11	10	9	SOC
IS Productivity --> design cycle (mo) [1]	12	12	12	12	12	12	11	11	10	9	SOC
WAS SOC logic Mtx per designer-year (10-person team)	1.9	2.5	3.3	4.3	5.4	7.4	10.6	24.6	73.4	113	SOC
IS Productivity --> Logic Mtx per designer-year (10-person team [2]	1.9	2.5	3.3	4.3	5.4	7.4	10.6	24.6	73.4	113	SOC
Add Productivity --> % software in design cycle (mo[3])	---	60%	60%	60%	60%	60%	60%	60%	60%	60%	SOC
WAS SOC dynamic power reduction beyond scaling (X)	0	0.1	0.1	0.2	0.2	0.2	0.2	6	4.7	8.1	SOC
IS SOC dynamic power reduction beyond scaling (X) [4]	0	0.1	0.1	0.2	0.2	0.2	0.2	6	4.7	8.1	SOC
WAS SOC standby power reduction beyond scaling (X)	0.37	1.4	2.4	3.4	5.1	6.4	8.73	18.8	44.4	232	SOC
IS SOC standby power reduction beyond scaling (X) [5]	0.37	1.4	2.4	3.4	5.1	6.4	8.73	18.8	44.4	232	SOC
WAS %Test covered by BIST	20	20	25	30	35	40	45	60	75	90	MPU, SOC
IS Manufacturing interface --> %logic Test covered by BIST [6]	20	20	25	30	35	40	45	60	75	90	MPU, SOC
Add Design cost --> improvement, normalized[7]	---	100%	86%	120%	56%	78%	105%	143%	149%	155%	SOC
Add Area density --> increase (X) [8]	---	1	1.4	2	2.8	4	5.6	15.6	43.8	122.8	SOC
Add Area density --> increase beyond scaling (X) [9]	---	0	0	0	0	0	0	0	0	0	SOC

Mtx—Million transistors

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known

Added Notes for Table 19:[1] Number of months from design requirements definition to tape-out.[2] Number of logic transistors in a chip divided by the number of person-years in a design team, for a 10-person team.[3] % of software design effort as the number of software development person-years versus the total number of person-years.[4] % of dynamic power savings on top of the % of active power savings derived from technology scaling..[5] % of leakage power savings on top of the % of leakage power savings derived from technology scaling.[6] % of the logic gates' stuck-at faults covered by BIST.[7] % improvement in design cost per year for low-power PDA SoC driver. It accounts for all design technology improvements.[8] Increase in absolute area density (number of gates per unit chip area.[9] Increase in area density on top of density improvement coming from technology scaling (feature reduction).

Table 20 Design Technology Improvements and Impact on Designer Productivity

<i>DT Improvement</i>	<i>Year</i>	<i>Productivity Delta</i>	<i>Productivity (Gates/Desn-Year)</i>	<i>Cost of Component Affected</i>	<i>Description of Improvement</i>
None	1990		4K		
In-house place and route	1993	+38.9%	5.55K	PD Integration	Automated block placement and routing.
Engineer	1995	+63.6%	9.09K	Chip/circuit/PD Verification	Engineer than can pursue all required tasks to complete a design block, from RTL to GDSII.
Reuse—small blocks	1997	+340%	40K	Circuit/PD Verification	Blocks from 2,500–74,999 gates.
Reuse—large blocks	1999	+38.9%	56K	Chip/circuit/PD Integration Verification	Blocks from 75,000–1M gates.
IC implementation suite	2001	+63.6%	91K	Chip/circuit/PD Integration EDA support	Tightly integrated tool set that goes from RTL synthesis to GDS II through IC place and route.
Intelligent testbench	2003	+37.5%	125K	SW development Verification	RTL verification tool (“cockpit”) that takes an ES-level description and partitions it into verifiable blocks, then executes verification tools on the blocks, while tracking and reporting code coverage.
Electronic system-level (ES-level) methodology	2005	+60%	200K	SW development Verification	Level above RTL, including both HW and SW design. It consists of a behavioral (where the system function has not been partitioned) and an architectural level (where HW and SW are identified and handed off to design teams).
Very large block reuse	2007	+200%	600K	Chip/circuit/PD Verification	Blocks >1M gates; intellectual-property cores
TOTAL		+15,000%			

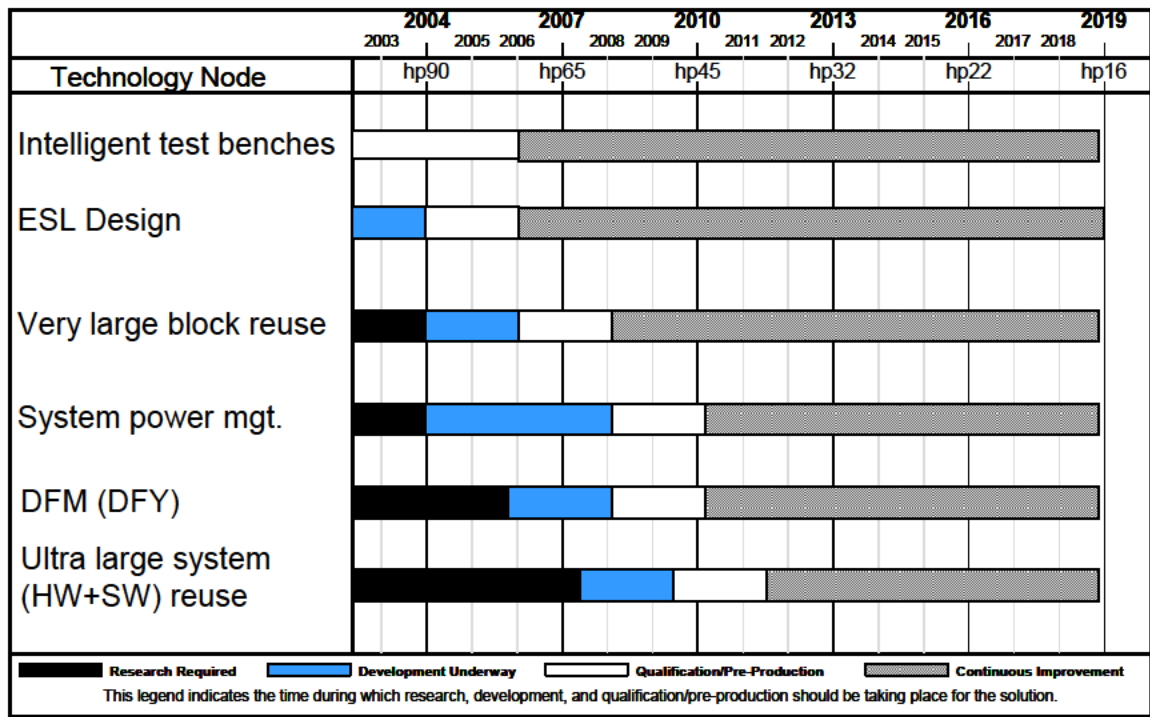


Figure c General Design Potential Solutions ADDED DEFINITIONS

Intelligent test benches—RTL verification tool that takes ES-level description, partitions it, verifies blocks, and tracks code coverage

ESL design—Level above RTL, includes HW and SW design. It consists of a behavioral (before HW/SW partitioning) and architectural level (after)

Very large block reuse—Blocks >1M gates; intellectual-property cores

System power management—Automated design of power management features applied at the system level

DFM (DFY)—Design-For-Manufacturability and Design For Yield automation

Ultra large system (HW+SW) reuse—Reuse of ultra-large blocks, including massively parallel processing HW and SW units (>10M “gates”)

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Process Integration, Devices, and Structures

Jointly Sponsored
by

European Semiconductor Industry Association

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PROCESS INTEGRATION, DEVICES, AND STRUCTURES

2004 UPDATE HIGHLIGHTS

The 2004 update for the Process Integration, Devices and Structures (PIDS) section of the ITRS has minor changes and corrections from the 2003 edition. The most notable change is that in the long-term technology requirements tables, the years 2011, 2014, and 2017 have been added, so that all years from 2010 through 2018 are now included. As expected, the parameter values for these added years are generally close to midway between the values for the previous and succeeding years. In Figure 23, which is for low standby power logic, the curve for maximum allowed gate leakage current density (labeled “J_{g,limit}”) has been corrected. In the 2003 edition, this curve was low by a factor of 2 to 3. Even with the correction, the implication of the figure is unchanged, that oxynitride gate dielectric is projected to be unable to meet the gate leakage current limits by 2006.

[Link to the 2003 ITRS Process Integration, Devices, and Structures chapter](#)

WORKING GROUP TABLES

Table 46a Process Integration Difficult Challenges—Near-term

<i>Difficult Challenges ≥ 45 nm/Through 2010</i>	<i>Summary of Issues</i>
1. High-performance applications: meeting performance and power dissipation requirements for highly scaled MOSFETs	Cost effectiveness, process control, and reliability of very thin oxynitride gate dielectrics, especially considering the high gate leakage Difficulty in controlling short-channel effects for highly scaled devices Negative impact of high channel doping needed for highly scaled devices. Also, the difficulty in controlling threshold voltage due to statistical fluctuations in the doping Need to reduce series S/D parasitic resistance Controlling static power dissipation in the face of rapidly increasing leakage: architecture and circuit design improvement and innovation will be needed.
2. Low-power applications: meeting performance and leakage requirements for highly scaled MOSFETs	Early availability of manufacturing-worthy high-κ gate dielectrics is necessary to meet stringent gate leakage and performance requirements. Slow scaling of V_{dd} for low standby power logic will make overall device scaling difficult. Rapid scaling of V_{dd} for low operating power logic will make overall device scaling difficult.
3. Assuring the reliability and implementing into manufacturing of multiple material, process, and structural changes in a relatively short period of time	Multiple material changes projected: high-κ gate dielectric, metal gate electrodes, strained Si, nickel silicide by 2008 or so Elevated S/D (selective epi) Ultra-thin body (UTB) SOI by 2008 or so, followed by multiple-gate structures. Near mid-gap metal gate electrodes will be desirable to set the threshold voltage for UTB SOI. Difficulty in ensuring reliability of all these new materials, processes, and structures in a timely manner

2 Process Integration, Devices, and Structures

Table 46a Process Integration Difficult Challenges—Near-term (continued)

4. Implementation of DRAM, SRAM, and high-density nonvolatile memory (NVM) for scaled technologies	DRAM main issues—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities with scaling. Also, difficult lithography and etch issues with scaling NVM, flash—Scaling of tunnel dielectric and interpoly dielectric involves many complex tradeoffs. Dielectric material properties and dimensional control are key issues NVM, FeRAM—Ferroelectric material properties and dimensional control. Sensitivity to IC processing temperatures and conditions NVM, SONOS—ONO stack dimensions and material properties, including nitride layer trap distribution in space and energy NVM, MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions
5. High-performance and low-cost RF and analog/mixed-signal solutions	Signal isolation Optimizing RF/analog CMOS devices with scaled technologies: mismatch, 1/f noise, and leakage with high-κ gate dielectrics High density integrated passive element scaling and use of new materials: Q-factor value for inductors; matching and linearity for capacitors Reduced power supply voltages: degradation in SNR (signal-to-noise ratio) and signal distortion performance Reduced device breakdown voltage in scaled technologies High-frequency devices with increased operating voltage for base station applications Compound semiconductor substrates with good thermal dissipation and process equipment for fabrication at low cost See section on RF and A/MS Technologies for Wireless Communications for detailed discussion of these issues

Table 46b Process Integration Difficult Challenges—Long-term

<i>Difficult Challenges < 45 nm/Beyond 2010</i>	<i>Summary of Issues</i>
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate, ultra-thin body [UTB] MOSFETs) with lightly doped body will be needed to effectively scale MOSFETs to well under 20 nm gate length (L_g). Most likely, advanced material solutions such as strained Si (enhanced mobility) channels, elevated source/drain, high-κ gate dielectric, metal gate electrode, etc., will be utilized along with the advanced non-classical CMOS Particularly for the highly scaled UTB MOSFETs required towards the end of the Roadmap, with body thickness well under 10 nm, electrical performance and the impact of quantum effects are not well understood To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced carrier saturation velocity appears to be needed See Emerging Research Devices section for more detail.
7. Dealing with atomic-level fluctuations and statistical process variations in sub-20 nm MOSFETs	Fundamental issues of atomic-level statistical fluctuations for sub-20 nm MOSFETs are not completely understood, including the impact of quantum effects.
8. Identifying, selecting, and implementing new memory structures	Highly scaled, dense, fast, non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness, attaining the very low leakage currents that will be required, and reducing the cell area factor All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc.) are currently unclear.
10. Toward the end of the Roadmap or beyond, identification, selection, and implementation of advanced, beyond-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of beyond-CMOS devices need to extend well beyond CMOS limits. Beyond-CMOS devices need to integrate into a CMOS platform. Integration of the two may be difficult, especially for mixed signal. See Emerging Research Devices sections for more discussion and detail.

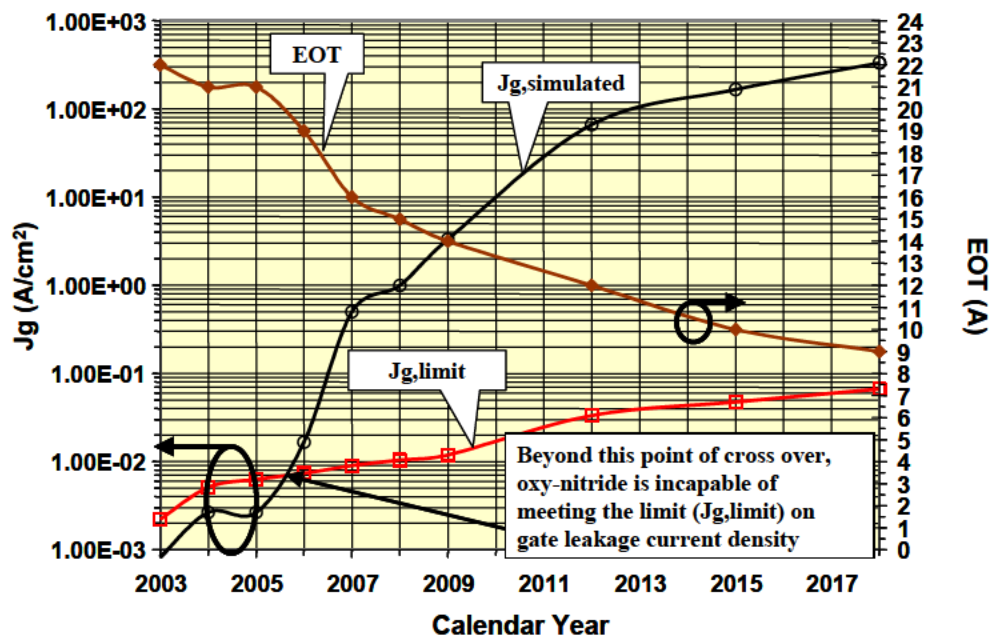


Figure 23 LSTP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling WAS

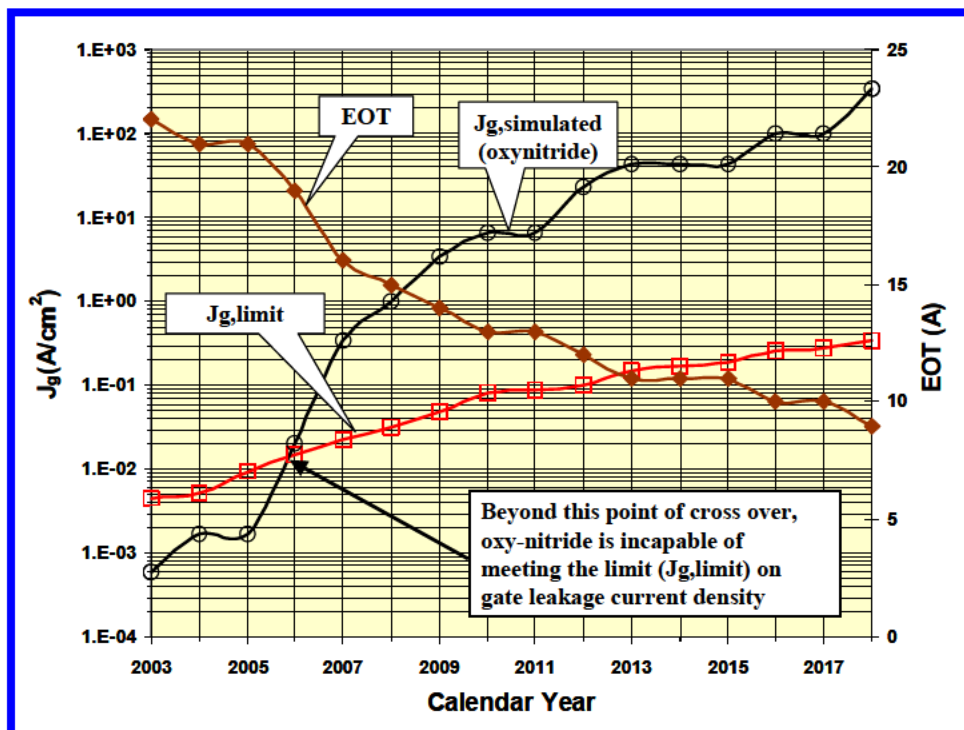


Figure 23 LSTP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling UPDATED

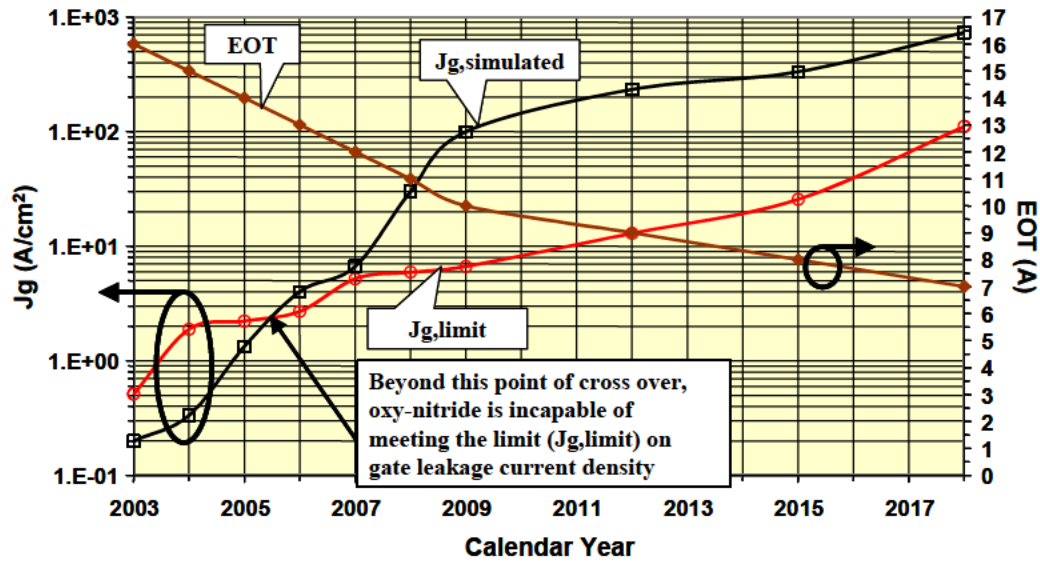


Figure 24 LOP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling WAS

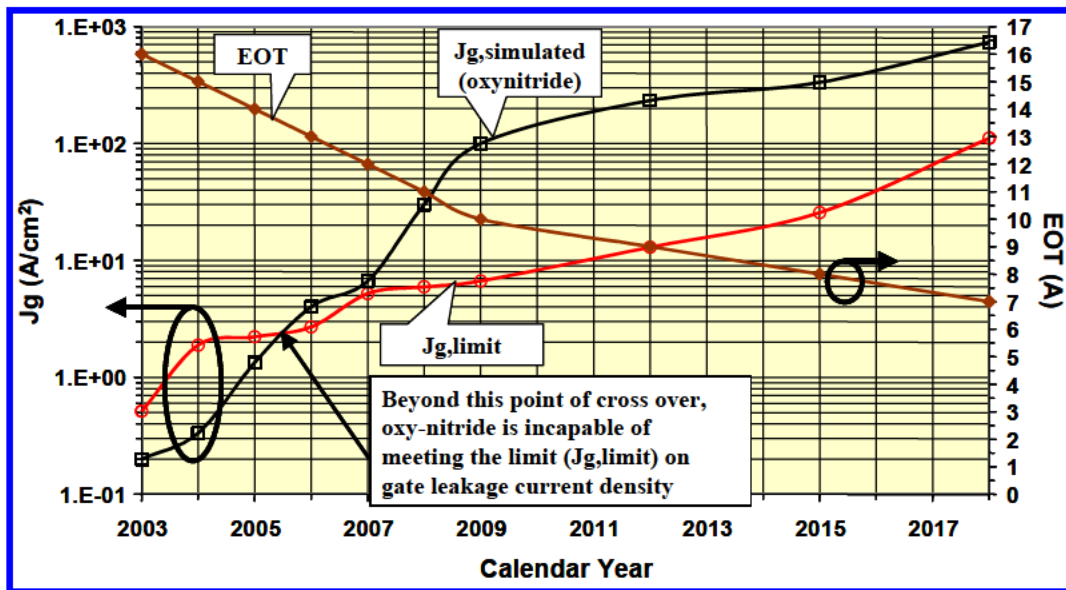


Figure 24 LOP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling UPDATED

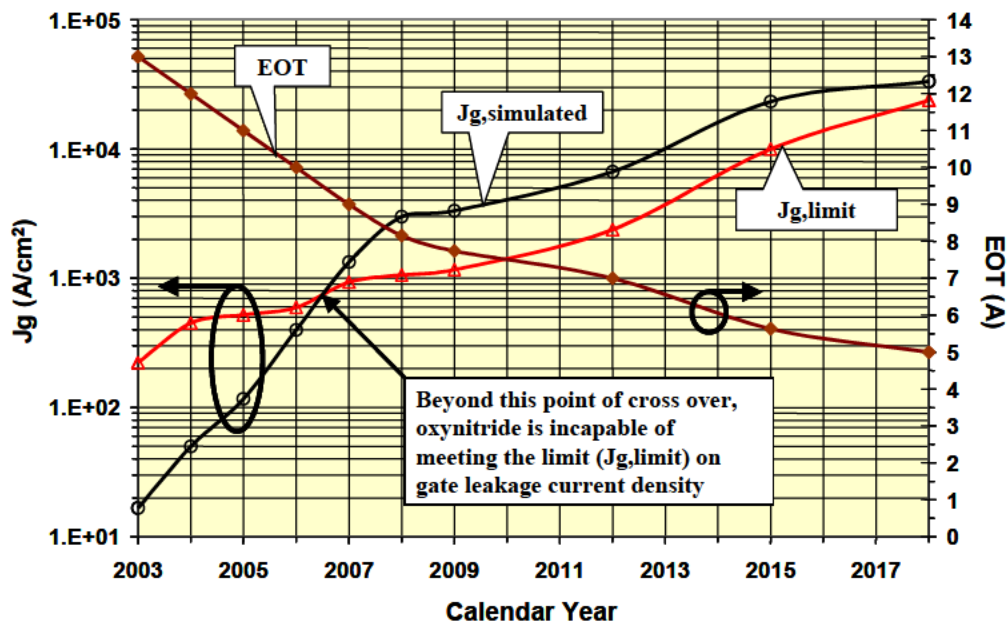


Figure 25 High-performance Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling WAS

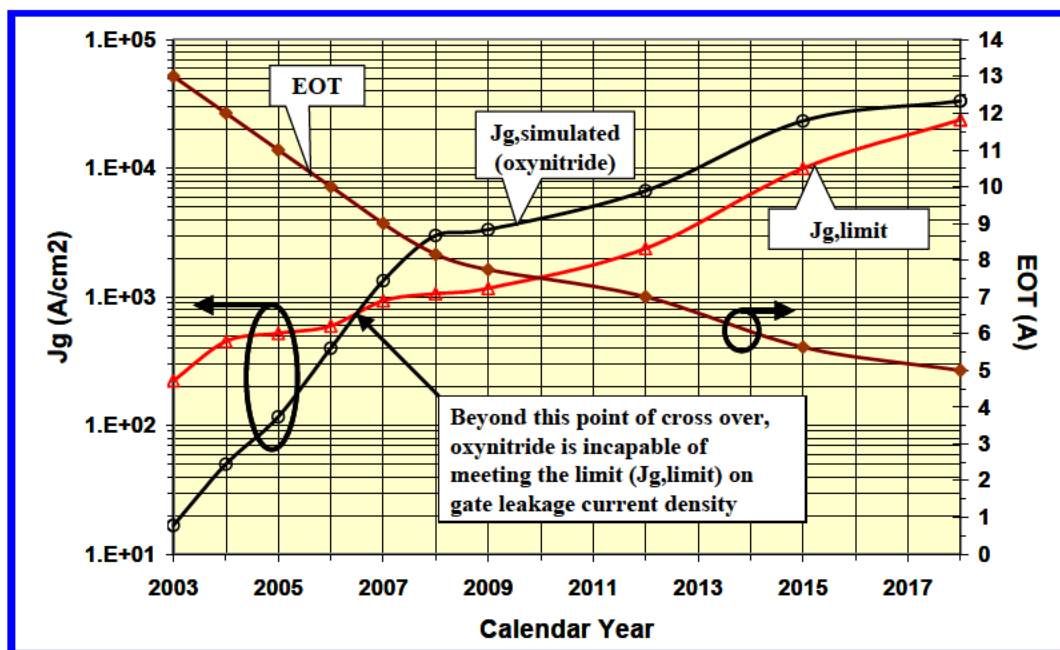


Figure 25 High-performance Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling UPDATED

Table 47a High-performance Logic Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Physical gate length high-performance (HP) (nm) [1]	45	37	32	28	25	22	20
EOT equivalent oxide thickness (physical) for high-performance (nm) [2]	1.3	1.2	1.1	1.0	0.9	0.8	0.8
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.4	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	2.1	2.0	1.8	1.7	1.3	1.2	1.2
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	2.2E+02	4.5E+02	5.2E+02	6.0E+02	9.3E+02	1.1E+03	1.2E+03
Nominal power supply voltage (V_{dd}) (V) [6]	1.2	1.2	1.1	1.1	1.1	1.0	1.0
Saturation threshold voltage (V) [7]	0.21	0.20	0.20	0.21	0.18	0.17	0.16
Nominal high-performance NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) ($\mu A/\mu m$) [8]	0.03	0.05	0.05	0.05	0.07	0.07	0.07
Nominal high-performance NMOS saturation drive current, $I_{d,sat}$ (at V_{dd} , at 25°C) (mA/mm) [9]	♦ 980	1110	1090	1170	1510	1530	1590
Required "mobility/transconductance improvement" factor [10]	1.0	1.3	1.3	1.4	2.0	2.0	2.0
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	1.0	1.0	1.0	1.0	1.0	0.8	0.7
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Parasitic source/drain series resistance (R_{sd}) (Ohm- μm) [13]	♦ 180	180	180	171	162	153	144
Ideal NMOS device gate capacitance (F/ μm) [14]	7.40E-16	6.39E-16	6.14E-16	5.69E-16	6.64E-16	6.33E-16	5.76E-16
Parasitic fringe/overlap capacitance (F/ μm) [15]	2.40E-16	2.40E-16	2.40E-16	2.30E-16	2.20E-16	2.00E-16	1.90E-16
High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	♦ 1.20	0.95	0.86	0.75	0.64	0.54	0.48
Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	♦ 1.00	1.26	1.39	1.60	1.86	2.20	2.49
Nominal logic gate delay (NAND Gate) (ps) [18]	♦ 30.24	23.94	21.72	18.92	16.23	13.72	12.13
NMOSFET power-delay product (J/ μm) [19]	1.41E-15	1.27E-15	1.03E-15	9.66E-16	1.07E-15	8.33E-16	7.66E-16
NMOSFET static power dissipation due to drain and gate leakage (W/ μm) [20]	3.96E-07	6.60E-07	6.05E-07	6.05E-07	8.47E-07	7.70E-07	7.70E-07

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

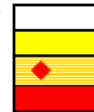


Table 47b High-performance Logic Technology Requirements—Long-term **UPDATED**

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Physical gate length high-performance (HP) (nm) [1]	18		14	13		10	9		7
IS	Physical gate length high-performance (HP) (nm) [1]	18	<u>16</u>	14	13	<u>11</u>	10	9	<u>8</u>	7
WAS	EOT equivalent oxide thickness (physical) for high-performance (nm) [2]	0.7		0.7	0.6		0.6	0.5		0.5
IS	EOT equivalent oxide thickness (physical) for high-performance (nm) [2]	0.7	<u>0.7</u>	0.7	0.6	<u>0.6</u>	0.6	0.5	<u>0.5</u>	0.5
WAS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4		0.4	0.4		0.4	0.4		0.4
IS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	<u>0.4</u>	0.4	0.4	<u>0.4</u>	0.4	0.4	<u>0.4</u>	0.4
WAS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.1		1.1	1		1	0.9		0.9
IS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.1	<u>1.1</u>	1.1	1	<u>1</u>	1	0.9	<u>0.9</u>	0.9
WAS	Nominal gate leakage current density limit (at 25°C) (A/cm ²) [5]	1.90E+03		2.40E+03	7.70E+03		1.00E+04	1.90E+04		2.40E+04
IS	Nominal gate leakage current density limit (at 25°C) (A/cm ²) [5]	1.90E+03	<u>2.08E+03</u>	2.40E+03	7.70E+03	<u>9.09E+03</u>	1.00E+04	1.90E+04	<u>2.08E+04</u>	2.40E+04
WAS	Nominal power supply voltage (V _{dd}) (V) [6]	1		0.9	0.9		0.8	0.8		0.7
IS	Nominal power supply voltage (V _{dd}) (V) [6]	1	<u>1</u>	0.9	0.9	<u>0.9</u>	0.8	0.8	<u>0.7</u>	0.7
WAS	Saturation threshold voltage (V) [7]	0.15		0.14	0.11		0.12	0.1		0.11
IS	Saturation threshold voltage (V) [7]	0.15	<u>0.15</u>	0.14	0.11	<u>0.11</u>	0.12	0.1	<u>0.1</u>	0.11
WAS	Nominal high-performance NMOS sub-threshold leakage current, I _{sd,leak} (at 25°C) (μA/μm) [8]	0.1		0.1	0.3		0.3	0.5		0.5
IS	Nominal high-performance NMOS sub-threshold leakage current, I _{sd,leak} (at 25°C) (μA/μm) [8]	0.1	<u>0.1</u>	0.1	0.3	<u>0.3</u>	0.3	0.5	<u>0.5</u>	0.5

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table 47b High-performance Logic Technology Requirements—Long-term **UPDATED** (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Nominal high-performance NMOS saturation drive current, $I_{d,sat}$ (at V_{dd} , at 25°C) (mA/μm) [9]	1900		1790	2050		2110	2400		2190
IS	Nominal high-performance NMOS saturation drive current, $I_{d,sat}$ (at V_{dd} , at 25°C) (μA/μm) [9]	1900	<u>1940</u>	1790	2050	<u>2230</u>	2110	2400	<u>2120</u>	2190
WAS	Required "mobility/transconductance improvement" factor [10]	2		2	2		2	2		2
IS	Required "mobility/transconductance improvement" factor [10]	2	<u>2</u>	2	2	<u>2</u>	2	2	<u>2</u>	2
WAS	Sub-threshold slope adjustment factor (Full depletion/multiple-gate effects) (0–1) [11]	0.6		0.5	0.5		0.5	0.5		0.5
IS	Sub-threshold slope adjustment factor (Full depletion/multiple-gate effects) (0–1) [11]	0.6	<u>0.6</u>	0.5	0.5	<u>0.5</u>	0.5	0.5	<u>0.5</u>	0.5
WAS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.1		1.1	1.1		1.3	1.3		1.3
IS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.1	<u>1.1</u>	1.1	1.1	<u>1.2</u>	1.3	1.3	<u>1.3</u>	1.3
WAS	Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	135		116	107		88	79		60
IS	Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	135	<u>125</u>	116	107	<u>98</u>	88	79	<u>70</u>	60
WAS	Ideal NMOS device gate capacitance (F/μm) [14]	5.65E-16		4.39E-16	4.49E-16		3.45E-16	3.45E-16		2.69E-16
IS	Ideal NMOS device gate capacitance (F/μm) [14]	5.65E-16	<u>5.02E-16</u>	4.39E-16	4.49E-16	<u>3.76E-16</u>	3.45E-16	3.45E-16	<u>3.07E-16</u>	2.69E-16
WAS	Parasitic fringe/overlap capacitance (F/μm) [15]	1.80E-16		1.50E-16	1.40E-16		1.20E-16	1.00E-16		8.00E-17
IS	Parasitic fringe/overlap capacitance (F/μm) [15]	1.80E-16	<u>1.65E-16</u>	1.50E-16	1.40E-16	<u>1.30E-16</u>	1.20E-16	1.00E-16	<u>9.00E-17</u>	8.00E-17
WAS	High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.39		0.3	0.26		0.18	0.15		0.11
IS	High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.39	<u>0.34</u>	0.3	0.26	<u>0.21</u>	0.18	0.15	<u>0.13</u>	0.11

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

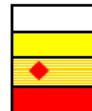


Table 47b High-performance Logic Technology Requirements—Long-term **UPDATED** (continued)

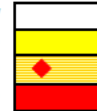
Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node	hp45			hp32			hp22		
DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.06		4.05	4.64		6.8	8.08		10.77
IS Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.1	3.5	4.1	4.6	5.7	6.8	8.1	9.2	10.8
WAS Nominal logic gate delay (NAND gate) (ps) [18]	9.88		7.47	6.52		4.45	3.74		2.81
IS Nominal logic gate delay (NAND gate) (ps) [18]	9.88	8.67	7.47	6.52	5.19	4.45	3.74	3.30	2.81
WAS NMOSFET power-delay product ($J/\mu m$) [19]	7.45E-16		4.77E-16	4.77E-16		2.98E-16	2.85E-16		1.71E-16
IS NMOSFET power-delay product ($J/\mu m$) [19]	7.45E-16	6.67E-16	4.77E-16	4.77E-16	4.10E-16	2.98E-16	2.85E-16	1.95E-16	1.71E-16
WAS NMOSFET static power dissipation due to drain and gate leakage ($W/\mu m$) [20]	1.10E-06		9.90E-07	2.97E-06		2.64E-06	4.40E-06		3.85E-06
IS NMOSFET static power dissipation due to drain and gate leakage ($W/\mu m$) [20]	1.1E-06	1.1E-06	9.9E-07	3.0E-06	3.0E-06	2.6E-06	4.4E-06	3.9E-06	3.9E-06

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Notes for Tables 47a and 47b

A Microsoft Excel file containing the worksheet in which the details of the model-based scaling are described is located in the electronic version of this chapter at <http://public.itrs.net>, including the formulas used in the MOSFET modeling. All the entries in this High-performance Logic Technology Requirements Table are from the worksheet. Please refer to this Excel file for detailed questions about the table.

WAS The scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goal for high-performance logic, 17% per year average improvement in the NMOS intrinsic switching speed (see Note [16]), while delaying as long as feasible the projected need for major innovations. These include innovations such as metal gate electrode, high- κ gate dielectric, and novel doping and annealing techniques to reduce the value of the parasitic series source/drain resistance. However, there are numerous parameters (such as EOT, V_{dd} , $I_{sd,leak}$ etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters (see text for more detail on this point).

IS The scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goal for high-performance logic, 17% per year average improvement in the NMOS intrinsic switching speed (see Note [16]), while delaying as long as feasible the projected need for major innovations. These include innovations such as metal gate electrode, high- κ gate dielectric, and novel doping and annealing techniques to reduce the value of the parasitic series source/drain resistance. However, there are numerous parameters (such as EOT, V_{dd} , $I_{sd,leak}$ etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters (see text for more detail on this point).

[1] This is the final, as-etched length of the bottom of the gate electrode. Values set by ORTC. Gate dimensional control is set by the Lithography and FEP Etch ITWGs, and is assumed to have a three-sigma value of $\pm 10\% \times L_g$. It is expected that meeting this 10% requirement will become increasingly difficult with scaling (refer to the Lithography chapter and the FEP chapter). Gate length variation is assumed to be a primary factor responsible for driving device parameter variation.

[2] For a gate dielectric of thickness T_d and relative dielectric constant κ , EOT is defined by $EOT = T_d / (\kappa/3.9)$, where 3.9 is the relative dielectric constant of thermal silicon dioxide. For a MOSFET with the gate dielectric of thickness T_d , the ideal gate capacitance per unit area is the same as that of a similar MOSFET, but with a gate dielectric made up of thermal silicon dioxide with a thickness of EOT. Yellow coloring in 2006 is set by FEP TWG projections of difficulties in achieving adequate thickness control and reliability capability for thin silicon oxy-nitride gate dielectrics. Red coloring for 2007 and beyond is due to projected inability of oxy-nitride gate dielectric to meet the gate leakage current density limits (see Note [5], and see text as well as Figure 25 for detail). Utilization of high- κ gate dielectric is a potential solution. Measurement of EOT is complicated, and is usually done via sophisticated MOS capacitor-voltage (CV) measurements on MOS capacitors or via optical measurements.

[3] Accounts (approximately) for gate electrode depletion and inversion-layer effects, including quantum effects. The portion of the electrical thickness adjustment due to inversion-layer effects is assumed to remain constant at 0.4 nm. For polysilicon gate electrodes, the portion of the electrical thickness adjustment due to gate electrode depletion is dependent on the polysilicon doping. The yellow coloring for 2005 and 2006 reflects the FEP TWG assessment of difficulty in adequately doping polysilicon (particularly

for the P^+ , boron-doped electrodes) to meet the gate depletion thickness adjustment requirements. The red coloring for 2007 and beyond reflects the projected inability to adequately dope polysilicon gate electrodes to meet the gate depletion thickness adjustment requirements. Introduction of metal-gate electrodes, which reduce the gate depletion effect to zero, is a potential solution.

[4] Sum of EOT and electrical thickness adjustment (see Notes [2] and [3] above). For MOSFETs in inversion, ideal gate capacitance per unit area (see Note [14]) is $\epsilon_{ox} / (equivalent\ electrical\ oxide\ thickness)$, where ϵ_{ox} is the dielectric constant of thermal silicon dioxide. The equivalent electrical oxide thickness in inversion is used in calculations of the CV/I intrinsic delay (see Note [16]) and of the CV^2 dynamic switching energy (see Note [19]). Red/yellow coloring follows that of EOT and Electrical Thickness Adjustment (see Notes [2] and [3] above).

[5] This is the maximum allowed gate leakage at 25°C, and is related to $I_{sd,leak}$, the nominal subthreshold leakage current per micron device width (see Note [8] below). Specifically, gate leakage current density limit = $[I_{sd,leak} / (physical\ gate\ length)] \times [temp.\ factor] / [stack\ and\ overlap\ factor]$. "Temp factor" = 10, and it accounts for the high operating temperature expected for high-performance logic, by adjusting for both the rapid increase in $I_{sd,leak}$ with temperature and the insensitivity of gate leakage current (since it is due to direct tunneling) to temperature. Stack and overlap factor=3, and accounts for the different effects on $I_{sd,leak}$ and gate leakage current of stacked transistors in logic gates and of transistor gate overlap. The values of both temp factor and stack and overlap factor are rough order of magnitude estimates. The yellow and red coloring follows that of EOT (see Note [2] above).

[6] Nominal power supply voltage has been chosen to maintain sufficient voltage over-drive [V_{dd} – saturation threshold voltage (see Note 7)] in order to meet the required saturation current drive values (see Note 9), while still maintaining reasonable vertical gate dielectric electric field strengths. Target power supply voltage values for actual ICs may vary $\pm 10\%$ (or more) from the values in this table, depending on the particular circuit design application or technology optimization.

[7] Calculated threshold voltage for minimum nominal gate length transistor with drain bias set equal to V_{dd} (see Note [6]). The threshold voltage values and the corresponding subthreshold leakage current values (see Note [8]) have been chosen to maintain sufficient voltage over-drive (V_{dd} – saturation threshold voltage) in order to meet the required saturation current drive values (see Note [9]). Since control of short-channel effects for scaled MOSFETs is a key issue here, the yellow/red coloring follows that of the subthreshold slope adjustment factor (see Note [11] below).

[8] Nominal subthreshold leakage current is defined as the NMOSFET source current per micron of device width, at 25°C, with the drain bias set equal to V_{dd} (see Note [6]) and with the gate, source, and substrate biases set to zero volts. All MOSFET device dimensions are assumed to be at their nominal/target values. Total NMOS off-state current is the NMOSFET drain current per micron of device width at 25°C, and is the sum of the NMOS subthreshold, gate, and junction leakage current components. The subthreshold leakage current is assumed to be larger than the junction leakage current component at either 25°C or high-temperature conditions, but see Note [5] for the relation between $I_{sd,leak}$ and gate leakage current density. Yellow and red coloring follows that of the subthreshold slope adjustment factor, which takes account of the impact of using advanced devices ultra-thin body, fully depleted MOSFETs and multiple-gate MOSFETs (see Note [11] below). The above subthreshold, gate, and junction leakage current scaling scenario also applies to PMOS devices. Note that subthreshold current values here apply to the fastest MOSFETs only; slower/lower-leakage MOSFETs will also be available, since current and future chips consist/will consist of a mix of both high and lower-leakage devices (see text for further discussion).

WAS

[9] Nominal saturation current drive, $I_{d,sat}$, is defined as the NMOSFET drain current per micron device width, at 25°C, with the gate bias and the drain bias set equal to V_{dd} (see Note [6]) and the source and substrate biases set to zero; all MOSFET device dimensions are assumed to be at their nominal/target values. The saturation drive current values have been chosen to continue the historical approximate 17% per year device performance scaling (see Note [17] below). Nominal PMOS saturation current-drive value is assumed to be (40–50)% of the nominal NMOS saturation current-drive value. Yellow/red coloring follows that of three items: the parasitic source/drain series resistance, R_{sd} (see Note [13] below), the equivalent electrical oxide thickness in inversion (see Note [4]), and the required mobility/transconductance improvement factor (see Note [10]). Note that saturation current drive values here apply to the fastest MOSFETs only; lower saturation current drive/lower-leakage MOSFETs will also be available, since current and future chips consist/will consist of a mix of both high and lower-leakage devices (see text for further discussion).

IS

[9] Nominal saturation current drive, $I_{d,sat}$, is defined as the NMOSFET drain current per micron device width, at 25°C, with the gate bias and the drain bias set equal to V_{dd} (see Note [6]) and the source and substrate biases set to zero; all MOSFET device dimensions are assumed to be at their nominal/target values. The saturation drive current values have been chosen to continue the historical approximate 17% per year device performance scaling (see Note [17] below). Nominal PMOS saturation current-drive value is assumed to be (40–50)% of the nominal NMOS saturation current-drive value. Yellow/red and striped coloring follows that of three items: the parasitic source/drain series resistance, R_{sd} (see Note [13] below), the equivalent electrical oxide thickness in inversion (see Note [4]), and the required mobility/transconductance improvement factor (see Note [10]). Note that saturation current drive values here apply to the fastest MOSFETs only; lower saturation current drive/lower-leakage MOSFETs will also be available, since current and future chips consist/will consist of a mix of both high and lower-leakage devices (see text for further discussion).

[10] Fundamental device mobility/transconductance improvement (strained Si channel is the current implementation choice) is captured by a factor multiplying the carrier mobility. Such improvement is projected to be needed by 2004 in order to meet the required saturation current drive values (see Note [9]). Yellow coloring in 2004 and beyond reflects projected implementation of strained Si channel devices. Red coloring in 2007 and beyond reflects the difficulty in optimizing this mobility enhancement to a factor of 2.0, and the difficulty of implementing enhanced mobility channels for advanced, ultra-thin body devices.

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[11] Subthreshold slope adjustment factor takes account of the impact of using advanced, single-gate, ultra-thin body, fully depleted SOI MOSFETs and eventually, ultra-thin body, multiple-gate MOSFETs, which are needed to control short-channel effects for highly scaled transistors. Specifically, this is a multiplying factor for the subthreshold slope, reducing it towards its minimum ideal value of 60 mV/decade. The factor ranges from 1.0 for classical, planar bulk MOSFETs, to 0.7 to 0.8 for single-gate, ultra-thin body MOSFETs, to 0.6 to 0.5 for ultra-thin body, multiple-gate MOSFETs. These numbers are rough estimates of the impact of these advanced devices. (See Non-Classical CMOS tables in the Emerging Research Devices section for further discussion of the ultra-thin body MOSFETs.) The yellow coloring reflects the projected introduction of the single-gate, ultra-thin body MOSFET in 2008, and the red coloring reflects the projected introduction of the multiple-gate MOSFET in 2010.

[12] This is a multiplying factor for carrier saturation velocity, reflecting quasi-ballistic transport in highly scaled, ultra-thin body MOSFETs, particularly multi-gate MOSFETs. The red coloring in 2010 and beyond reflects the projected need for saturation velocity enhancement in order to meet the required saturation current drive values (see Note [9]).

WAS [13] Rsd is the maximum allowable parasitic series source plus drain resistance for a MOSFET of one micron width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow/red coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.

IS [13] Rsd is the maximum allowable parasitic series source plus drain resistance for a MOSFET of one micron width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow/red and striped coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.

[14] This is $C_{g,ideal}$, the ideal gate capacitance per micron device width, in inversion. $C_{g,ideal} = [\epsilon_{ox} / (EOT_{inv})] \times L_g$, where ϵ_{ox} is the dielectric constant of thermal silicon dioxide, EOT_{inv} is the equivalent electrical oxide thickness in inversion (see Note [4]), and L_g is the physical gate length (see Note [1]). The red/yellow coloring follows that of EOT_{inv} (see Note [4]).

[15] This is the parasitic gate overlap/fringing capacitance per micron device width [$3 \times$ the overlap/fringing capacitance value per side, including the Miller effect]. These values are assumed to be independent of bias conditions.

WAS [16] τ is the intrinsic transistor delay for NMOS devices at 25°C. $\tau = (C_{gate} \times V_{dd}) / I_{d,sat}$ where C_{gate} is the sum of the ideal device gate capacitance per micron device width (Note 14) and the parasitic gate overlap/fringing capacitance per micron device width (see Note [15]). τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat} \sim (0.4-0.5) \times (NMOS I_{d,sat})$ (see Note [9]). τ is a good metric for the intrinsic switching delay of the device, while $1/\tau$ is a good metric for the intrinsic switching speed of the device. Red/yellow coloring follows that of both saturation current-drive (see Note [9]) and ideal gate capacitance (see Note [14]).

IS [16] τ is the intrinsic transistor delay for NMOS devices at 25°C. $\tau = (C_{gate} \times V_{dd}) / I_{d,sat}$ where C_{gate} is the sum of the ideal device gate capacitance per micron device width (Note 14) and the parasitic gate overlap/fringing capacitance per micron device width (see Note [15]). τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat} \sim (0.4-0.5) \times (NMOS I_{d,sat})$ (see Note [9]). τ is a good metric for the intrinsic switching delay of the device, while $1/\tau$ is a good metric for the intrinsic switching speed of the device. Red/yellow and striped coloring follows that of both saturation current-drive (see Note [9]) and ideal gate capacitance (see Note [14]).

WAS [17] NMOS performance metric ($1/\tau$, NMOS intrinsic switching speed—see Note [16]), normalized to the year 2003. Maintenance of the historical approximate 17% per year device performance improvement scaling trend is the key scaling goal for high-performance logic. Red/yellow coloring follows that of τ (see Note [16]).

IS [17] NMOS performance metric ($1/\tau$, NMOS intrinsic switching speed—see Note [16]), normalized to the year 2003. Maintenance of the historical approximate 17% per year device performance improvement scaling trend is the key scaling goal for high-performance logic. Red/yellow and striped coloring follows that of τ (see Note [16]).

WAS [18] This is the calculated nominal delay for a 2-input, fan-out of 3, NAND gate, which is chosen to represent a typical logic gate (for details of the calculation, see link provided in the electronic version, online at <http://public.itrs.net>). Red/yellow coloring follows that of τ (see Note [16]).

IS [18] This is the calculated nominal delay for a 2-input, fan-out of 3, NAND gate, which is chosen to represent a typical logic gate (for details of the calculation, see link provided in the electronic version, online at <http://public.itrs.net>). Red/yellow and striped coloring follows that of τ (see Note [16]).

[19] This is the energy dissipated per micron of MOSFET width during a full switching cycle, defined as $C_{gate} \times V_{dd}^2$, where C_{gate} is the sum of the ideal device gate capacitance per micron width (Note [14]) and the parasitic gate overlap/fringing capacitance per micron width (see Note [15]). (This is the same C_{gate} used in calculating τ [see Note [16]). The dynamic power dissipation is directly related to this power-delay product. Red/yellow coloring follows that of $C_{g,ideal}$ (see Note [14]).

[20] This is the static power dissipation per micron of MOSFET width, defined as $V_{dd} \times \{I_{sd,leak} \text{ (see Note 8)}\} + \{ \text{maximum gate leakage current per micron device width (defined as } L_g \times \text{gate leakage current density limit, from Note 5)} \}$. (The junction leakage current is assumed to be much smaller than either the source/drain subthreshold leakage current or the gate leakage current). Yellow/red coloring follows that of nominal gate leakage current density limit (see Note [5]).

Table 48a Low Operating Power (LOP) Logic Technology Requirements—Near-term

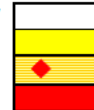
Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Physical gate length low operating power (LOP) (nm) [1]	65	53	45	37	32	28	25
EOT equivalent oxide thickness (physical) for LOP (nm) [2]	1.6	1.5	1.4	1.3	1.2	1.1	1.0
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.7	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	2.4	2.3	2.1	2.0	1.9	1.5	1.4
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	0.51	1.89	2.22	2.70	5.21	5.95	6.67
Nominal LOP power supply voltage (V_{dd}) (V) [6]	1.0	0.9	0.9	0.9	0.8	0.8	0.8
Saturation threshold voltage (V) [7]	0.31	0.26	0.27	0.28	0.26	0.25	0.25
Nominal LOP NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) ($\mu A/\mu m$) [8]	1.0E-03	3.0E-03	3.0E-03	3.0E-03	5.0E-03	5.0E-03	5.0E-03
Nominal LOP NMOS saturation drive current, $I_{d,sat}$ (at V_{dd} at 25°C) ($\mu A/\mu m$) [9]	520	530	580	610	570	730	770
Required "mobility/transconductance improvement" factor [10]	1.0	1.0	1.0	1.0	1.0	1.3	1.3
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Parasitic source/drain series resistance (R_{sd}) (Ohm- μm) [13]	180	180	180	180	180	180	180
Ideal NMOS device gate capacitance (F/ μm) [14]	9.35E-16	7.96E-16	7.40E-16	6.39E-16	5.82E-16	6.45E-16	6.17E-16
Parasitic fringe/overlap capacitance (F/ μm) [15]	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16
LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	2.26	1.76	1.52	1.30	1.15	0.97	0.89
Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	1.00	1.29	1.49	1.74	1.96	2.33	2.54
Nominal logic gate delay (NAND gate) (ps) [18]	57.0	44.3	38.3	32.7	29.1	24.4	22.4
NMOSFET power-delay product (J/ μm) [19]	1.18E-15	8.39E-16	7.94E-16	7.12E-16	5.26E-16	5.66E-16	5.48E-16
NMOSFET static power dissipation due to drain and gate leakage (W/ μm) [20]	2.0E-09	5.4E-09	5.4E-09	5.4E-09	8.0E-09	8.0E-09	8.0E-09

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



14 Process Integration, Devices, and Structures

Table 48b Low Operating Power (LOP) Logic Technology Requirements—Long-term [UPDATED](#)

Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node	hp45			hp32			hp22		
DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS Physical gate length low operating power (LOP) (nm) [1]	22		18	16		13	11		9
IS Physical gate length low operating power (LOP) (nm) [1]	22	20	18	16	14	13	11	10	9
WAS EOT equivalent oxide thickness (physical) for LOP (nm) [2]	0.9	-	0.9	0.8	-	0.8	0.7	-	0.7
IS EOT equivalent oxide thickness (physical) for LOP (nm) [2]	0.9	0.9	0.9	0.8	0.8	0.8	0.7	0.7	0.7
WAS Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	-	0.4	0.4	-	0.4	0.4	-	0.4
IS Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
WAS Equivalent electrical oxide thickness in inversion (nm) [4]	1.3	-	1.3	1.2	-	1.2	1.1	-	1.1
IS Equivalent electrical oxide thickness in inversion (nm) [4]	1.3	1.3	1.3	1.2	1.2	1.2	1.1	1.1	1.1
WAS Nominal gate leakage current density limit (at 25°C) (A/cm ²) [5]	11	-	13	21	-	26	91	-	111
IS Nominal gate leakage current density limit (at 25°C) (A/cm ²) [5]	11	12	13	21	24	26	91	100	111
WAS Nominal LOP power supply voltage (V _{dd}) (V) [6]	0.7	-	0.7	0.6	-	0.6	0.5	-	0.5
IS Nominal LOP power supply voltage (V _{dd}) (V) [6]	0.7	0.7	0.7	0.6	0.6	0.6	0.5	0.5	0.5
WAS Saturation threshold voltage (V) [7]	0.22	-	0.23	0.21	-	0.19	0.16	-	0.17
IS Saturation threshold voltage (V) [7]	0.22	0.22	0.23	0.21	0.2	0.19	0.16	0.16	0.17
WAS Nominal LOP NMOS sub-threshold leakage current, I _{sd,leak} (at 25°C) (μA/μm) [8]	0.007	-	0.007	0.01	-	0.01	0.03	-	0.03
IS Nominal LOP NMOS sub-threshold leakage current, I _{sd,leak} (at 25°C) (μA/μm) [8]	0.007	0.007	0.007	0.01	0.01	0.01	0.03	0.03	0.03
WAS Nominal LOP NMOS saturation drive current, I _{d,sat} (at V _{dd} at 25°C) (μA/μm) [9]	770	-	830	780	-	900	920	-	950
IS Nominal LOP NMOS saturation drive current, I _{d,sat} (at V _{dd} at 25°C) (μA/μm) [9]	770	800	830	780	840	900	920	935	950

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table 48b Low Operating Power (LOP) Logic Technology Requirements—Long-term [UPDATED](#)
(continued)

Year of Production		2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node		hp45			hp32			hp22		
DRAM ½ Pitch (nm)		45	40	35	32	28	25	22	20	18
WAS	Required "mobility/transconductance improvement" factor [10]	1.3	-	2	2	-	2	2	-	2
IS	Required "mobility/transconductance improvement" factor [10]	1.3	<u>1.3</u>	2	2	<u>2</u>	2	2	<u>2</u>	2
WAS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8	-	0.8	0.8	-	0.5	0.5	-	0.5
IS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8	<u>0.8</u>	0.8	0.8	<u>0.8</u>	0.5	0.5	<u>0.5</u>	0.5
WAS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1	-	1	1.1	-	1.1	1.3	-	1.3
IS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1	<u>1</u>	1	1.1	<u>1.1</u>	1.1	1.3	<u>1.3</u>	1.3
WAS	Parasitic source/drain series resistance (R_{sd}) (Ohm- μm) [13]	160	-	135	126	-	107	98	-	80
IS	Parasitic source/drain series resistance (R_{sd}) (Ohm- μm) [13]	160	<u>148</u>	135	126	<u>117</u>	107	98	<u>89</u>	80
WAS	Ideal NMOS device gate capacitance (F/ μm) [14]	5.84E-16	-	4.78E-16	4.60E-16	-	3.74E-16	3.45E-16	-	2.83E-16
IS	Ideal NMOS device gate capacitance (F/ μm) [14]	5.84E-16	<u>5.31E-16</u>	4.78E-16	4.60E-16	<u>4.03E-16</u>	3.74E-16	3.45E-16	<u>3.14E-16</u>	2.83E-16
WAS	Parasitic fringe/overlap capacitance (F/ μm) [15]	2.20E-16	-	1.80E-16	1.60E-16	-	1.40E-16	1.30E-16	-	1.10E-16
IS	Parasitic fringe/overlap capacitance (F/ μm) [15]	2.20E-16	<u>2.00E-16</u>	1.80E-16	1.60E-16	<u>1.50E-16</u>	1.40E-16	1.30E-16	<u>1.20E-16</u>	1.10E-16
WAS	LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.73	-	0.56	0.48	-	0.34	0.26	-	0.21
IS	LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.73	<u>0.64</u>	0.56	0.48	<u>0.39</u>	0.34	0.26	<u>0.23</u>	0.21
WAS	Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.1	-	4.1	4.7	-	6.6	8.7	-	10.9
IS	Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.1	<u>3.54</u>	4.1	4.7	<u>5.72</u>	6.6	8.7	<u>9.75</u>	10.9
WAS	Nominal logic gate delay (NAND Gate) (ps) [18]	18.4	-	14	12	-	8.6	6.5	-	5.2
IS	Nominal logic gate delay (NAND Gate) (ps) [18]	18.4	<u>16.1</u>	14	12	<u>9.9</u>	8.6	6.5	<u>5.8</u>	5.2
WAS	NMOSFET power-delay product (J/ μm) [19]	3.94E-16	-	3.22E-16	2.23E-16	-	1.85E-16	1.19E-16	-	9.81E-17
IS	NMOSFET power-delay product (J/ μm) [19]	3.94E-16	<u>3.58E-16</u>	3.22E-16	2.23E-16	<u>1.99E-16</u>	1.85E-16	1.19E-16	<u>1.08E-16</u>	9.81E-17
WAS	NMOSFET static power dissipation due to drain and gate leakage (W/ μm) [20]	9.80E-09	-	9.80E-09	1.20E-08	-	1.20E-08	3.00E-08	-	3.00E-08
IS	NMOSFET static power dissipation due to drain and gate leakage (W/ μm) [20]	9.80E-09	<u>9.80E-09</u>	9.80E-09	1.20E-08	<u>1.20E-08</u>	1.20E-08	3.00E-08	<u>3.00E-08</u>	3.00E-08

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table 48c Low Standby Power (LSTP) Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Physical gate length low standby power (LSTP) (nm) [1]	75	65	53	45	37	32	28
EOT equivalent oxide thickness (physical) for LSTP (nm) [2]	2.2	2.1	2.1	1.9	1.6	1.5	1.4
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.7	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	3	2.9	2.8	2.6	2.3	1.9	1.8
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	4.4E-03	5.1E-03	9.4E-03	1.5E-02	2.3E-02	3.1E-02	4.8E-02
Nominal LSTP power supply voltage (V_{dd}) (V) [6]	1.2	1.2	1.2	1.2	1.1	1.1	1.1
Saturation threshold voltage (V) [7]	0.50	0.50	0.51	0.52	0.50	0.47	0.47
Nominal LSTP NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) ($\mu A/\mu m$) [8]	1.0E-05	1.0E-05	1.5E-05	2.0E-05	2.5E-05	3.0E-05	4.0E-05
Nominal LSTP NMOS saturation drive current, $I_{d,sat}$ (at V_{dd} at 25°C) ($\mu A/\mu m$) [9]	410	440	470	510	510	670	700
Required "mobility/transconductance improvement" factor [10]	1.0	1.0	1.0	1.0	1.0	1.3	1.3
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Parasitic source/drain series resistance (R_{sd}) (Ohm- μm) [13]	180	180	180	180	180	180	180
Ideal NMOS device gate capacitance (F/ μm) [14]	8.63E-16	7.74E-16	6.54E-16	5.98E-16	5.55E-16	5.82E-16	5.37E-16
Parasitic fringe/overlap capacitance (F/ μm) [15]	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16
LSTP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	3.23	2.77	2.28	1.97	1.72	1.35	1.22
Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	1.00	1.17	1.42	1.64	1.88	2.39	2.64
Nominal logic gate delay (NAND Gate) (ps) [18]	81.4	69.7	57.5	49.7	43.2	34.0	30.8
NMOSFET power-delay product (J/ μm) [19]	1.6E-15	1.5E-15	1.3E-15	1.2E-15	9.6E-16	9.9E-16	9.4E-16
NMOSFET static power dissipation due to drain and gate leakage (W/ μm) [20]	2.4E-11	2.4E-11	3.6E-11	4.8E-11	5.5E-11	6.6E-11	8.8E-11

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table 48d Low Standby Power (LSTP) Technology Requirements—Long-term **UPDATED**

Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node	hp45			hp32			hp22		
DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS Physical gate length low standby power (LSTP) (nm) [1]	25		20	18		14	13		10
IS Physical gate length low standby power (LSTP) (nm) [1]	25	<u>23</u>	20	18	<u>16</u>	14	13	<u>12</u>	10
WAS EOT equivalent oxide thickness (physical) for LSTP (nm) [2]	1.3		1.2	1.1		1.1	1		0.9
IS EOT equivalent oxide thickness (physical) for LSTP (nm) [2]	1.3	<u>1.3</u>	1.2	1.1	<u>1.1</u>	1.1	1	<u>1</u>	0.9
WAS Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4		0.4	0.4		0.4	0.4		0.4
IS Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	<u>0.4</u>	0.4	0.4	<u>0.4</u>	0.4	0.4	<u>0.4</u>	0.4
WAS Equivalent electrical oxide thickness in inversion (nm) [4]	1.7		1.6	1.5		1.5	1.4		1.3
IS Equivalent electrical oxide thickness in inversion (nm) [4]	1.7	<u>1.7</u>	1.6	1.5	<u>1.5</u>	1.5	1.4	<u>1.4</u>	1.3
WAS Nominal gate leakage current density limit (at 25°C) (A/cm ²) [5]	8.00E-02		1.00E-01	1.48E-01		1.90E-01	2.56E-01		3.33E-01
IS Nominal gate leakage current density limit (at 25°C) (A/cm ²) [5]	<u>0.08</u>	<u>0.09</u>	<u>0.10</u>	<u>0.15</u>	<u>0.17</u>	<u>0.19</u>	<u>0.26</u>	<u>0.28</u>	<u>0.33</u>
WAS Nominal LSTP power supply voltage (V _{dd}) (V) [6]	1		1	0.9		0.9	0.8		0.8
IS Nominal LSTP power supply voltage (V _{dd}) (V) [6]	1	<u>1</u>	1	0.9	<u>0.9</u>	0.9	0.8	<u>0.8</u>	0.8
WAS Saturation threshold voltage (V) [7]	0.39		0.43	0.34		0.38	0.36		0.4
IS Saturation threshold voltage (V) [7]	0.39	<u>0.42</u>	0.43	0.34	<u>0.36</u>	0.38	0.36	<u>0.39</u>	0.4
WAS Nominal LSTP NMOS sub-threshold leakage current, I _{sd,leak} (at 25°C) (μA/μm) [8]	6.00E-05		6.00E-05	8.00E-05		8.00E-05	1.00E-04		1.00E-04
IS Nominal LSTP NMOS sub-threshold leakage current, I _{sd,leak} (at 25°C) (μA/μm) [8]	6.00E-05	<u>6.00E-05</u>	6.00E-05	8.00E-05	<u>8.00E-05</u>	8.00E-05	1.00E-04	<u>1.00E-04</u>	1.00E-04
WAS Nominal LSTP NMOS saturation drive current, I _{d,sat} (at V _{dd} at 25°C) (μA/μm) [9]	760		790	880		870	860		990
IS Nominal LSTP NMOS saturation drive current, I _{d,sat} (at V _{dd} at 25°C) (μA/μm) [9]	760	<u>750</u>	790	880	<u>870</u>	870	860	<u>880</u>	990

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

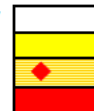


Table 48d Low Standby Power (LSTP) Technology Requirements—Long-term **UPDATED** (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Required "mobility/transconductance improvement" factor [10]	1.3		1.3	1.3		1.3	2		2
IS	Required "mobility/transconductance improvement" factor [10]	1.3	<u>1.3</u>	1.3	1.3	<u>1.3</u>	1.3	2	<u>2</u>	2
WAS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8		0.8	0.5		0.5	0.5		0.5
IS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8	<u>0.8</u>	0.8	0.5	<u>0.5</u>	0.5	0.5	<u>0.5</u>	0.5
WAS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1		1	1		1	1.1		1.3
IS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1	<u>1</u>	1	1	<u>1</u>	1	1.1	<u>1.2</u>	1.3
WAS	Parasitic source/drain series resistance (R_{sd}) (Ohm- μm) [13]	180		144	135		116	107		88
IS	Parasitic source/drain series resistance (R_{sd}) (Ohm- μm) [13]	180	<u>160</u>	144	135	<u>125</u>	116	107	<u>97</u>	88
WAS	Ideal NMOS device gate capacitance ($F/\mu\text{m}$) [14]	5.08E-16		4.32E-16	4.14E-16		3.22E-16	3.21E-16		2.66E-16
IS	Ideal NMOS device gate capacitance ($F/\mu\text{m}$) [14]	5.08E-16	<u>4.67E-16</u>	4.32E-16	4.14E-16	<u>3.68E-16</u>	3.22E-16	3.21E-16	<u>2.96E-16</u>	2.66E-16
WAS	Parasitic fringe/overlap capacitance ($F/\mu\text{m}$) [15]	2.40E-16		1.90E-16	1.70E-16		1.50E-16	1.40E-16		1.20E-16
IS	Parasitic fringe/overlap capacitance ($F/\mu\text{m}$) [15]	2.40E-16	<u>2.15E-16</u>	1.90E-16	1.70E-16	<u>1.60E-16</u>	1.50E-16	1.40E-16	<u>1.30E-16</u>	1.20E-16
WAS	LSTP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.98		0.79	0.6		0.49	0.43		0.31
IS	LSTP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.98	<u>0.90</u>	0.79	0.6	<u>0.55</u>	0.49	0.43	<u>0.39</u>	0.31
WAS	Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.28		4.1	5.4		6.61	7.54		10.36
IS	Relative NMOS intrinsic switching speed, $1/\tau$, normalized to 2003 [17]	3.28	<u>3.58</u>	4.1	5.4	<u>5.91</u>	6.61	7.54	<u>8.34</u>	10.36
WAS	Nominal logic gate delay (NAND gate) (ps) [18]	24.8		19.83	15.06		12.31	10.8		7.85
IS	Nominal logic gate delay (NAND gate) (ps) [18]	24.8	<u>22.78</u>	19.83	15.06	<u>13.71</u>	12.31	10.8	<u>9.73</u>	7.85
WAS	NMOSFET power-delay product ($J/\mu\text{m}$) [19]	7.48E-16		6.22E-16	4.73E-16		3.83E-16	2.95E-16		2.47E-16
IS	NMOSFET power-delay product ($J/\mu\text{m}$) [19]	7.48E-16	<u>6.82E-16</u>	6.22E-16	4.73E-16	<u>4.28E-16</u>	3.83E-16	2.95E-16	<u>2.73E-16</u>	2.47E-16
WAS	NMOSFET static power dissipation due to drain and gate leakage ($W/\mu\text{m}$) [20]	1.20E-10		1.20E-10	1.44E-10		1.44E-10	1.60E-10		1.60E-10
IS	NMOSFET static power dissipation due to drain and gate leakage ($W/\mu\text{m}$) [20]	1.20E-10	<u>1.20E-10</u>	1.20E-10	1.44E-10	<u>1.44E-10</u>	1.44E-10	1.60E-10	<u>1.60E-10</u>	1.60E-10

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table 49a DRAM Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm) [1]	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
DRAM cell size (μm^2) [2]	0.082	0.065	0.048	0.036	0.028	0.019	0.015
DRAM storage cell dielectric equivalent physical oxide thickness, EOT (nm) [3]	3.5	2.3	1.8	1.3	0.8	0.8	0.8
Minimum DRAM retention time (ms) [4]	64	64	64	64	64	64	64
DRAM soft error rate (FITs) [5]	1000	1000	1000	1000	1000	1000	1000

Table 49b DRAM Technology Requirements—Long-term UPDATED

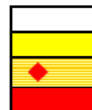
Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node	hp45			hp32			hp22		
DRAM ½ Pitch (nm) [1]	45		35	32		25	22		18
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS DRAM cell size (μm^2) [2]	0.0122		0.0077	0.0061		0.0038	0.0025		0.0016
IS DRAM cell size (μm^2) [2]	0.0122	0.0096	0.0077	0.0061	0.0048	0.0038	0.0025	0.0020	0.0016
WAS DRAM storage cell dielectric equivalent physical oxide thickness, EOT (nm) [3]	0.70		0.58	0.53		0.42	0.37		0.25
IS DRAM storage cell dielectric equivalent physical oxide thickness, EOT (nm) [3]	0.70	0.64	0.58	0.53	0.48	0.42	0.37	0.31	0.25
WAS Minimum DRAM retention time (ms) [4]	64		64	64		64	64		64
IS Minimum DRAM retention time (ms) [4]	64	64	64	64	64	64	64	64	64
WAS DRAM soft error rate (FITs) [5]	1000		1000	1000		1000	1000		1000
IS DRAM soft error rate (FITs) [5]	1000	1000	1000	1000	1000	1000	1000	1000	1000

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



20 Process Integration, Devices, and Structures

Notes for Tables 49a and 49b

[1] From ORTC (Overall Roadmap Technology Characteristics) Table 1a and b. These DRAM half pitch numbers are the same as those in the 2002 ITRS due to no further speed up in the pace of DRAM half pitch scaling during 2002 and the early part of 2003.

[2] The DRAM cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and chip size numbers used by FEP are based on the ORTC Tables 1a and 1b. Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled aggressively. The difficulty will lie in reducing the value of the cell size factor "a", where "a" equals $(\text{cell size} / F^2)$, and F is the DRAM half pitch. The required values of "a" are 8 for the 90 nm node, real 6 for the 55 nm DRAM half pitch in 2008, and 5 (need $4F^2$ layout) for the 32 nm node. The reason for the introduction delay of "a" value of 6 is due to no clear solutions, as illustrated with yellow zone in this line. The "a" value of 5 has no known solution for 32 nm node and beyond, as illustrated with red zone.

[3] The EOT is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and the chip size numbers used by FEP are from ORTC Tables 1a and 1b. Since the values of DRAM capacity and chip size from FEP are quite aggressive, the EOT must also be scaled very aggressively. Up to the 90 nm nodes, the dielectric material is based on Al_2O_3 or Ta_2O_5 with MIS structure, and hence the color is white. Beyond the 90 nm node, breakthroughs such as MIM structure and higher κ material are needed, so the color is yellow. Finally, for the 65 nm node and beyond, there are no known solutions with demonstrated credibility, and hence the color is red. The actual EOT required for each node also depends on the other factors such as cell height and/or 3D structure, film leakage current and contact formation. Trench capacitors have other requirements for the cell dielectric material.

[4] Retention time is defined at 85°C, and is the minimum time during which the data from memory can still be sensed correctly without refreshing a row bit line. The 64 ms specified here is the value needed for PC applications. The retention time depends on the combined interaction of device leakage current, signal strength and signal sensing circuit sensitivity, and also depends on operational frequency and temperature.

[5] This is a typical FIT rate and depends on cycle time and the quality of cell capacitor and sensing circuits.

Table 50a Non-Volatile Memory Technology Requirements—Near-term UPDATED

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
WAS Flash technology node – F (nm) [1]	107	90	80	70	65	55	50
IS Flash technology node – F (nm) [1]	107	90	80	70	65	<u>57</u>	50
Flash NOR cell size – area factor a in multiples of F ² [2]	10–12	11–14	11–14	11–14	11–14	12–14	12–15
Flash NAND cell size – area factor a in multiples of F ² SLC/MLC [3]	5.5	5.5	5.5	5.5	4.5	4.5	4.5
WAS Flash NOR typical cell size (μm ²) [4]	0.135	0.101	0.08	0.061	0.053	0.039	0.034
IS Flash NOR typical cell size (μm ²) [4]	0.135	0.101	0.08	0.061	0.053	<u>0.042</u>	0.034
Flash NOR L _g -stack (physical – μm) [5]	0.22–0.24	0.2–0.22	0.2–0.22	0.19–0.21	0.19–0.21	0.18–0.20	0.18–0.20
Flash NOR highest W/E voltage (V) [6]	8–10	7–9	7–9	7–9	7–9	7–9	7–9
Flash NAND highest W/E voltage (V) [7]	18–20	17–19	17–19	17–19	15–17	15–17	15–17
Flash NOR I _{read} (μA) [8]	34–42	31–39	29–37	28–36	27–35	26–34	25–33
Flash coupling ratio [9]	0.65–0.75	0.65–0.75	0.65–0.75	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
WAS Flash NOR tunnel oxide thickness (nm) [10]	9–10	8.5–9.5	8.5–9.5	8.5–9.5	8–9	8–9	8–9
IS Flash NOR tunnel oxide thickness <u>EOT</u> (nm) [10]	9–10	<u>8.5–9.5</u>	8.5–9.5	<u>8–9</u>	8–9	8–9	8–9
WAS Flash NAND tunnel oxide thickness (nm) [11]	7–8	7–8	7–8	7–8	6–7	6–7	6–7
IS Flash NAND tunnel oxide thickness <u>EOT</u> (nm) [11]	7–8	7–8	7–8	<u>6–7</u>	6–7	6–7	6–7
WAS Flash NOR interpoly dielectric thickness (nm) [12]	11–13	10–12	9–11	9–11	8.5–10.5	8.5–10.5	8.5–10.5
IS Flash NOR interpoly dielectric thickness <u>EOT</u> (nm) [12]	<u>13–15</u>	<u>11–13</u>	<u>11–13</u>	<u>11–13</u>	<u>10–12</u>	<u>10–12</u>	<u>10–12</u>
Flash NAND interpoly dielectric thickness (nm) [13]	13–15	13–15	13–15	13–15	10–13	10–13	10–13
Flash endurance (erase/write cycles) [14]	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05
Flash nonvolatile data retention (years) [15]	10–20	10–20	10–20	10–20	10–20	10–20	10–20
Flash maximum number of bits per cell (MLC) [16]	2	2	4	4	4	4	4

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table 50a Non-Volatile Memory Technology Requirements—Near-term **UPDATED** (continued)

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
WAS	FeRAM technology node – F (nm) [17]	250	180	180	150	130	120	110
IS	FeRAM technology node – F (nm) [17]	250	180	<u>130</u>	<u>130</u>	<u>120</u>	<u>110</u>	110
WAS	FeRAM cell size – area factor a in multiples of F^2 [18]	24	16	12	12	12	10	10
IS	FeRAM cell size – area factor a in multiples of F^2 [18]	<u>15</u>	<u>15</u>	12	12	12	10	10
WAS	FeRAM cell size (μm^2) [19]	1.5	0.518	0.389	0.27	0.203	0.144	0.121
IS	FeRAM cell size (μm^2) [19]	<u>0.937</u>	<u>0.486</u>	<u>0.203</u>	<u>0.203</u>	<u>0.173</u>	<u>0.121</u>	0.121
WAS	FeRAM cell structure [20]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
IS	FeRAM cell structure [20]	1T1C	1T1C	<u>1T1C</u>	<u>1T1C</u>	1T1C	1T1C	1T1C
WAS	FeRAM capacitor structure [21]	stack	stack	stack	stack	3D	3D	3D
IS	FeRAM capacitor structure [21]	stack	stack	<u>stack</u>	<u>stack</u>	3D	3D	3D
WAS	FeRAM capacitor footprint (μm^2) [22]	0.5	0.26	0.13	0.09	0.07	0.06	0.05
IS	FeRAM capacitor footprint (μm^2) [22]	<u>0.44</u>	<u>0.23</u>	<u>0.12</u>	<u>0.12</u>	0.086	0.081	0.076
WAS	FeRAM capacitor active area (μm^2) [23]	0.5	0.26	0.13	0.09	0.09	0.09	0.08
IS	FeRAM capacitor active area (μm^2) [23]	<u>0.44</u>	<u>0.23</u>	<u>0.12</u>	<u>0.12</u>	0.058	0.048	0.04
WAS	FeRAM cap active area/footprint ratio [24]	1	1	1	1	1.29	1.5	1.6
IS	FeRAM cap active area/footprint ratio [24]	1	1	1	1	<u>1.48</u>	<u>1.67</u>	<u>1.89</u>
WAS	Ferro capacitor voltage (V) [25]	2.5	1.8	1.5	1.5	1.2	1.2	1.2
IS	Ferro capacitor voltage (V) [25]	<u>2.5-3</u>	1.8	1.5	1.5	1.2	1.2	1.2
WAS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	11.2	17.2	34.5	34.5	40	40	40
IS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	<u>12.8</u>	<u>19.8</u>	<u>30.5</u>	<u>30.5</u>	40	40	40
	FeRAM endurance (read/write cycles) [27]	1.00E+13	1.00E+14	1.00E+15	>1E16	>1E16	>1E16	>1E16
	FeRAM nonvolatile data retention (years) [28]	10	10	10	10	10	10	10

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table 50a Non-Volatile Memory Technology Requirements—Near-term **UPDATED** (continued)

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
SONOS/NROM technology node – F (nm) [29]	130	115	100	90	70	65	55
SONOS/NROM cell size – area factor a in multiples of F^2 [30]	5	5	5.5	5.5	6	6	6
SONOS/NROM typical cell size (mm^2) [31]	0.085	0.066	0.055	0.045	0.029	0.025	0.018
SONOS/NROM maximum number of bits per cell (MLC) [32]	2	2	2	2	2	2	2
SONOS/NROM area per bit (mm^2) [33]	0.042	0.033	0.028	0.022	0.015	0.013	0.009
SONOS L_g -stack (physical – μm) [34]	0.18	0.18	0.17	0.17	0.16	0.16	0.16
SONOS highest W/E voltage (V) [35]	6.0–7.0	6.0–7.0	5.0–6.0	5.0–6.0	5.0–5.5	5.0–5.5	5.0–5.5
SONOS/NROM I_{read} (μA) [36]	35–45	33–43	31–41	29–39	27–37	25–35	25–35
SONOS/NROM tunnel oxide thickness (nm) [37]	5	5	4.5	4	3.5	3.5	3.5
SONOS/NROM nitride dielectric thickness (nm) [38]	6	5	5	4.5	4	4	4
SONOS/NROM blocking (top) oxide thickness (nm) [39]	5	5	4.5	4.5	4	4	4
SONOS/NROM endurance (erase/write cycles) [40]	1.00E+06	1.00E+06	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07
SONOS/NROM nonvolatile data retention (years) [41]	10–20	10–20	10–20	10–20	10–20	10–20	10–20
MRAM technology node F (nm) [42]	180	130	90	90	65	55	50
MRAM cell size area factor a in multiples of F^2 [43]	24.7	23.7	24.7	22.2	22.2	22.2	22.2
MRAM typical cell size (μm^2) [44]	0.8	0.4	0.2	0.18	0.09	0.07	0.06
MRAM switching field (Oe) [45]	50	60	80	70	90	100	110
MRAM write energy (pJ) [46]	150	100	70	70	50	45	40
MRAM active area per cell (μm^2) [47]	0.28	0.2	0.11	0.1	0.05	0.04	0.03
MRAM resistance-area product (Kohm- μm^2) [48]	3	2.5	2	1.7	1.5	1.3	1.2
MRAM magnetoresistance ratio(%) [49]	45	45	50	50	60	60	60
MRAM nonvolatile data retention (years) [50]	>10	>10	>10	>10	>10	>10	>10
MRAM write endurance (read/write cycles) [51]	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15
MRAM endurance – tunnel junction reliability (years at bias) [52]	>10	>10	>10	>10	>10	>10	>10

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

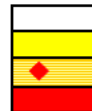


Table 50b Non-Volatile Memory Technology Requirements—Long-term **UPDATED**

Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
Technology Node	hp45			hp32			hp22		
DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS Flash technology node – F (nm) [1]	50		39	35		28	25		20
IS Flash technology node – F (nm) [1]	45	40	35	32	28	25	22	20	18
WAS Flash NOR cell size – area factor a in multiples of F ² [2]	12–15		12–15	13–16		14–17	14–17		15–18
IS Flash NOR cell size – area factor a in multiples of F ² [2]	12–15	12–15	12–15	13–16	13–16	14–17	14–17	15–18	15–18
WAS Flash NAND cell size – area factor a in multiples of F ² SLC/MLC [3]	4.5/2.3		4.5/2.3	4.5/2.3		4.5/2.3	4.5/2.3		4.5/2.3
IS Flash NAND cell size – area factor a in multiples of F ² SLC/MLC [3]	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3
WAS Flash NOR typical cell size (μm ²) [4]	0.034		0.021	0.018		0.012	0.01		0.007
IS Flash NOR typical cell size (μm ²) [4]	0.027	0.022	0.017	0.017	0.011	0.01	0.008	0.007	0.005
WAS Flash NOR L _g -stack (physical – μm) [5]	0.17–0.19		0.15–0.17	0.14–0.16		0.13–0.15	0.12–0.14		0.11–0.13
IS Flash NOR L _g -stack (physical – μm) [5]	0.17–0.19	0.16–0.18	0.15–0.17	0.14–0.16	0.14–0.16	0.13–0.15	0.12–0.14	0.12–0.14	0.11–0.13
WAS Flash NOR highest W/E voltage (V) [6]	7–9		7–9	7–9		7–9	7–9		7–9
IS Flash NOR highest W/E voltage (V) [6]	7–9	7–9	7–9	7–9	7–9	7–9	7–9	7–9	7–9
WAS Flash NAND highest W/E voltage (V) [7]	15–17		15–17	15–17		15–17	15–17		15–17
IS Flash NAND highest W/E voltage (V) [7]	15–17	15–17	15–17	15–17	15–17	15–17	15–17	15–17	15–17
WAS Flash NOR I _{read} (μA) [8]	27–33		26–32	25–31		23–29	22–28		20–26
IS Flash NOR I _{read} (μA) [8]	27–33	27–33	26–32	25–31	24–30	23–29	22–28	21–27	20–26
WAS Flash Coupling Ratio [9]	0.6–0.7		0.6–0.7	0.6–0.7		0.6–0.7	0.6–0.7		0.6–0.7
IS Flash Coupling Ratio [9]	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
WAS Flash NOR tunnel oxide thickness (nm) [10]	8–9		8–9	8		8	8		8
IS Flash NOR tunnel oxide thickness (nm) [10]	8–9	8–9	8–9	8–9	8	8	8	8	8
WAS Flash NAND tunnel oxide thickness (nm) [11]	6–7		6–7	6–7		6–7	6–7		6–7
IS Flash NAND tunnel oxide thickness (nm) [11]	6–7	6–7	6–7	6–7	6–7	6–7	6–7	6–7	6–7
WAS Flash NOR interpoly dielectric thickness (nm) [12]	8–10		7–9	6–8		5–7	4–6		3–5
IS Flash NOR interpoly dielectric thickness (nm) [12]	8–10	8–10	8–10	8–10	7–9	6–8	6–8	6–8	6–8
WAS Flash NAND interpoly dielectric thickness (nm) [13]	10–13		10–13	9–10		9–10	9–10		9–10
IS Flash NAND interpoly dielectric thickness (nm) [13]	10–13	10–13	10–13	9–10	9–10	9–10	9–10	9–10	9–10

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known



Table 50b Non-Volatile Memory Technology Requirements—Long-term *UPDATED* (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Flash endurance (erase/write cycles) [14]	1.00E+06		1.00E+06	1.00E+06		1.00E+06	1.00E+07		1.00E+07
IS	Flash endurance (erase/write cycles) [14]	1.E+06	<u>1.E+06</u>	1.E+06	1.E+06	<u>1.E+06</u>	1.E+06	1.E+07	<u>1.E+07</u>	1.E+07
WAS	Flash nonvolatile data retention (years) [15]	10–20		10–20	20		20	20		20
IS	Flash nonvolatile data retention (years) [15]	10–20	<u>10–20</u>	10–20	20	<u>20</u>	20	20	<u>20</u>	20
WAS	Flash maximum number of bits per cell (MLC) [16]	8		8	8		8	8		8
IS	Flash maximum number of bits per cell (MLC) [16]	8	<u>8</u>	8	8	<u>8</u>	8	8	<u>8</u>	8
WAS	FeRAM technology node – F (nm) [17]	100		80	70		57	50		45
IS	FeRAM technology node – F (nm) [17]	100	<u>90</u>	80	70	<u>64</u>	57	50	<u>48</u>	45
WAS	FeRAM cell size – area factor a in multiples of F ² [18]	8		8	8		8	8		8
IS	FeRAM cell size – area factor a in multiples of F ² [18]	8	<u>8</u>	8	8	<u>8</u>	8	8	<u>8</u>	8
WAS	FeRAM cell size (μm ²) [19]	0.08		0.051	0.039		0.026	0.02		0.016
IS	FeRAM cell size (μm ²) [19]	0.08	<u>0.065</u>	0.051	0.039	<u>0.033</u>	0.026	0.02	<u>0.018</u>	0.016
WAS	FeRAM cell structure [20]	1T1C		1T1C	1T1C		1T1C	1T1C		1T1C
IS	FeRAM cell structure [20]	1T1C	<u>1T1C</u>	1T1C	1T1C	<u>1T1C</u>	1T1C	1T1C	<u>1T1C</u>	1T1C
WAS	FeRAM capacitor structure [21]	3D		3D	3D		3D	3D		3D
IS	FeRAM capacitor structure [21]	3D	<u>3D</u>	3D	3D	<u>3D</u>	3D	3D	<u>3D</u>	3D
WAS	FeRAM capacitor footprint (μm ²) [22]	0.03		0.019	0.015		0.01	0.0075		0.0061
IS	FeRAM capacitor footprint (μm ²) [22]	0.071	<u>0.065</u>	0.06	0.057	<u>0.052</u>	0.048	0.045	<u>0.042</u>	0.038
WAS	FeRAM capacitor active area (μm ²) [23]	0.076		0.065	0.06		0.052	0.048		0.045
IS	FeRAM capacitor active area (μm ²) [23]	0.024	<u>0.02</u>	0.015	0.013	<u>0.01</u>	0.008	0.0061	<u>0.005</u>	0.0037
WAS	FeRAM cap active area/footprint ratio [24]	2.53		3.42	4		5.2	6.4		7.38
IS	FeRAM cap active area/footprint ratio [24]	<u>2.9</u>	<u>3.25</u>	<u>4</u>	<u>4.4</u>	<u>5.2</u>	<u>6</u>	<u>7.4</u>	<u>8.4</u>	<u>10.3</u>
WAS	Ferro capacitor voltage (V) [25]	1		1	0.7		0.7	0.7		0.7
IS	Ferro capacitor voltage (V) [25]	1	<u>1</u>	1	0.7	<u>0.7</u>	0.7	0.7	<u>0.7</u>	0.7
WAS	FeRAM minimum switching charge density (μC/cm ²) [26]	40		40	40		40	40		40
IS	FeRAM minimum switching charge density (μC/cm ²) [26]	40	<u>40</u>	40	40	<u>40</u>	40	40	<u>40</u>	40

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

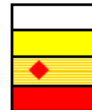


Table 50b Non-Volatile Memory Technology Requirements—Long-term **UPDATED** (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	FeRAM endurance (read/write cycles) [27]	>1E16		>1E16	>1E16		>1E16	>1E16		>1E16
IS	FeRAM endurance (read/write cycles) [27]	>1E16	≥1E16	>1E16	>1E16	≥1E16	>1E16	>1E16	≥1E16	>1E16
WAS	FeRAM nonvolatile data retention (years) [28]	10		10	10		10	10		10
IS	FeRAM nonvolatile data retention (years) [28]	10	10	10	10	10	10	10	10	10
WAS	SONOS/NROM technology node – F (nm) [29]	50		40	35		28	25		20
IS	SONOS/NROM technology node – F (nm) [29]	50	45	40	35	32	28	25	23	20
WAS	SONOS/NROM cell size – area factor a in multiples of F ² [30]	6		6	6.5		6.5	7		7
IS	SONOS/NROM cell size – area factor a in multiples of F ² [30]	6	6	6	6.5	6.5	6.5	7	7	7
WAS	SONOS/NROM typical cell size (nm ²) [31]	0.015		0.01	0.008		0.005	0.004		0.003
IS	SONOS/NROM typical cell size (nm ²) [31]	0.015	0.012	0.01	0.008	0.007	0.005	0.004	0.0037	0.003
WAS	SONOS/NROM maximum number of bits per cell (MLC) [32]	4		4	4		4	4		4
IS	SONOS/NROM maximum number of bits per cell (MLC) [32]	4	4	4	4	4	4	4	4	4
WAS	SONOS/NROM area per bit (nm ²) [33]	0.0038		0.0024	0.002		0.0013	0.0011		0.0007
IS	SONOS/NROM area per bit (nm ²) [33]	0.0038	0.003	0.0024	0.002	0.0018	0.0013	0.0011	0.0009	0.0007
WAS	SONOS L _g -stack (physical – μm) [34]	0.16		0.16	0.15		0.15	0.14		0.14
IS	SONOS L _g -stack (physical – μm) [34]	0.16	0.16	0.16	0.15	0.15	0.15	0.14	0.14	0.14
WAS	SONOS highest W/E voltage (V) [35]	5.0–5.5		5.0–5.5	5.0–5.5		5.0–5.5	4.5–5.0		4.0–4.5
IS	SONOS highest W/E voltage (V) [35]	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	4.5–5.0	4.5–5.0	4.0–4.5
WAS	SONOS/NROM I _{read} (μA) [36]	25–35		24–34	23–33		22–32	21–31		20–30
IS	SONOS/NROM I _{read} (μA) [36]	25–35	25–35	24–34	23–33	23–33	22–32	21–31	21–31	20–30

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table 50b Non-Volatile Memory Technology Requirements—Long-term *UPDATED* (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	SONOS/NROM tunnel oxide thickness (nm) [37]	3		3	2.5		2.5	2		2
IS	SONOS/NROM tunnel oxide thickness (nm) [37]	3	<u>3</u>	3	2.5	<u>2.5</u>	2.5	2	<u>2</u>	2
WAS	SONOS/NROM nitride dielectric thickness (nm) [38]	4		4	4		4	3.5		3.5
IS	SONOS/NROM nitride dielectric thickness (nm) [38]	4	<u>4</u>	4	4	<u>4</u>	4	3.5	<u>3.5</u>	3.5
WAS	SONOS/NROM blocking (top) oxide thickness (nm) [39]	4		4	4		4	4		4
IS	SONOS/NROM blocking (top) oxide thickness (nm) [39]	4	<u>4</u>	4	4	<u>4</u>	4	4	<u>4</u>	4
WAS	SONOS/NROM endurance (erase/write cycles) [40]	1.00E+08		1.00E+08	1.00E+08		1.00E+08	1.00E+09		1.00E+09
IS	SONOS/NROM endurance (erase/write cycles) [40]	1.E+08	<u>1.E+08</u>	1.E+08	1.E+08	<u>1.E+08</u>	1.E+08	1.E+09	<u>1.E+09</u>	1.E+09
WAS	SONOS/NROM nonvolatile data retention (years) [41]	10–20		10–20	10–20		10–20	10–20		10–20
IS	SONOS/NROM nonvolatile data retention (years) [41]	10–20	<u>10–20</u>	10–20	10–20	<u>10–20</u>	10–20	10–20	<u>10–20</u>	10–20
WAS	MRAM technology node – F (nm) [42]	45		35	32		25	22		18
IS	MRAM technology node – F (nm) [42]	45	<u>40</u>	35	32	<u>28</u>	25	22	<u>20</u>	18
WAS	MRAM cell size – area factor a in multiples of F^2 [43]	22.2		22.2	22.2		22.2	22.2		22.2
IS	MRAM cell size – area factor a in multiples of F^2 [43]	22.2	<u>22.2</u>	22.2	22.2	<u>22.2</u>	22.2	22.2	<u>22.2</u>	22.2
WAS	MRAM typical cell size (μm^2) [44]	0.04		0.03	0.02		0.01	0.01		0.01
IS	MRAM typical cell size (μm^2) [44]	<u>0.045</u>	<u>0.036</u>	<u>0.027</u>	<u>0.023</u>	<u>0.017</u>	<u>0.014</u>	0.01	<u>0.009</u>	<u>0.007</u>
WAS	MRAM switching field (Oe) [45]	120		120	120		120	120		120
IS	MRAM switching field (Oe) [45]	120	<u>120</u>	120	120	<u>120</u>	120	120	<u>120</u>	120
WAS	MRAM write energy (pJ) [46]	35		30	25		23	20		18
IS	MRAM write energy (pJ) [46]	35	<u>33</u>	30	25	<u>24</u>	23	20	<u>19</u>	18
WAS	MRAM active area per cell (μm^2) [47]	0.03		0.02	0.01		0.01	0.01		0.01
IS	MRAM active area per cell (μm^2) [47]	0.03	<u>0.025</u>	0.02	0.01	<u>0.01</u>	0.01	0.01	<u>0.01</u>	0.01

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table 50b Non-Volatile Memory Technology Requirements—Long-term **UPDATED** (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MRAM resistance-area product (Kohm- μm^2) [48]	1.1		0.95	0.8		0.7	0.6		0.55
IS	MRAM resistance-area product (Kohm- μm^2) [48]	1.1	<u>1</u>	0.95	0.8	<u>0.75</u>	0.7	0.6	<u>0.6</u>	0.55
WAS	MRAM magnetoresistance ratio(%) [49]	60		65	70		70	70		70
IS	MRAM magnetoresistance ratio(%) [49]	60	<u>65</u>	65	70	<u>70</u>	70	70	<u>70</u>	70
WAS	MRAM nonvolatile data retention (years) [50]	>10		>10	>10		>10	>10		>10
IS	MRAM nonvolatile data retention (years) [50]	>10	<u>>10</u>	>10	>10	<u>>10</u>	>10	>10	<u>>10</u>	>10
WAS	MRAM write endurance (read/write cycles) [51]	>1e15		>1e15	>1e15		>1e15	>1e15		>1e15
IS	MRAM write endurance (read/write cycles) [51]	>1e15	<u>>1e15</u>	>1e15	>1e15	<u>>1e15</u>	>1e15	>1e15	<u>>1e15</u>	>1e15
WAS	MRAM endurance – tunnel junction reliability (years at bias) [52]	>10		>10	>10		>10	>10		>10
IS	MRAM endurance – tunnel junction reliability (years at bias) [52]	>10	<u>>10</u>	>10	>10	<u>>10</u>	>10	>10	<u>>10</u>	>10

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Notes for Tables 50a and 50b

[1] In the past Flash devices tended to lag behind the current CMOS technology node, but that delay no longer exists. This entry provides the F value for designs in the indicated time period.

[2] The area factor “a” = cell area/ F^2 , so this entry presents the expected range for Flash NOR cell area in multiples of the implementation technology node F^2 . Note the lack of long term scaling.

[3] The area factor “a” = cell area/ F^2 , so this entry presents the Flash NAND cell area in multiples of F^2 the implementation technology node. Flash NAND enjoys a small cell size because much of the cell structure is shared among a group of cells. (SLC single level cell, MLC multilevel cell.)

[4] A typical Flash NOR cell size in micrometers squared is estimated using the midrange area factor “a.”

[5] This is the physical length of the control gate of Flash NOR devices.

[6, 7] This is the highest voltage relative to ground seen in the cell array. It is not usually an external supply.

[8] The current reduces with scaling at a rate higher than $W/(L \cdot C_{ox})$ to reduce the voltage overdrive factor.

[9] The coupling ratio is the (control gate to floating gate capacitance)/(total floating gate to source, drain and substrate capacitance).

[10, 11] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This difficult trade off problem hinders scaling.

[12, 13] Interpoly dielectric must be thick enough to assure retention but thin enough to assure an almost constant coupling ratio. Charge retention when the dielectric is scaled downward is the major issue.

[14] E/W endurance requirements vary with the specifics of an application, but $1E5$ cycles have been accepted as the historical minimum acceptable level for a useful product. It is expected that emerging technology will allow both tradeoffs of endurance for retention as well as increases in the specified minimum endurance capability as device design options.

[15] Retention is a defect related parameter rather than an intrinsic device characteristic. Improvement in defect control and accumulation of device history is expected to eventually allow specification of 20 years retention. Also, it should become possible to accept a reduced retention specification as a tradeoff for increased E/W endurance.

[16] Cell read out distinguishes between four levels of charge storage to provide two storage bits. Progression to 16 and 256 levels is anticipated. (MLC multilevel cell).

[17] This entry is the critical dimension “F” within the FeRAM cell for stand-alone memory devices (not embedded devices).

[18] This is the area factor “a” = cell size/ F^2 . FeRAM cell size is presented in terms of F^2 multiples of the FeRAM implementation technology node.

[19] FeRAM cell size is presented in terms of micrometers squared. It is the product $a \times F^2$.

[20] FeRAM cell structures have migrated to one transistor, one capacitor (1T1C) formats. Other alternative configurations are under investigation such as Chain-FeRAM.

[21] The geometry of the capacitor is a key factor in determining cell size. Stacked planar films are expected to be replaced by more efficient 3D structures.

- [22] This is the footprint of the capacitor in micrometers squared. It is this area that constitutes the capacitor area contribution to the cell size. For 2003–2004 $8F^2$, for 2005–2009 $4F^2$, and for 2010–2018 F^2 are assumed.
- [23] This is the actual effective area of the capacitor. It can be larger than the footprint because of the utilization of area in the third dimension.
- [24] This ratio of the effective area to the footprint gives a measure of the impact of utilization of the third dimension.
- [25] This is the operating voltage (V_{op}) applied to the capacitor. Low voltage operation is a difficult key design issue.
- [26] The minimum switching charge density in $\mu C/cm^2$ is a useful design parameter. It is equal to the cell minimum switching charge divided by the capacitor actual effective area. The capacitor voltage is taken as V_{op} .
- [27] FeRAM is a destructive read-out technology, so every read is accompanied by a write to restore the data. Endurance cycles are taken as the sum of all read and all write cycles. For FeRAM to compete with DRAM and SRAM the cycle endurance should be about $1E15$. Test time is a serious concern. Note that operation at 100 MHz for 10 years would accumulate $1E16$ cycles.
- [28] This is the data retention requirement while the device is disconnected from power. It is usually specified at $85^\circ C$.
- [29] SONOS/NROM devices have recently been introduced into the commercial market and will tend to lag the current CMOS technology node by one year; however, similar to Flash floating-gate technology, this gap will close rapidly due to low programming voltages combined with CMOS compatibility (i.e. single-level polysilicon). This entry provides the F value for designs in the indicated time period.
- [30] The area factor “ a ” = cell area/ F^2 . This entry depicts the expected SONOS/NROM NOR cell area in multiples of the implementation technology node F^2 . The reduced ONO gate stack thickness and low programming voltages should permit long range scaling of this technology.
- [31] The expected “typical” SONOS/NROM NOR cell size is presented in terms of micrometers squared.
- [32] MBC signifies “multiple bit storage,” while MLC signifies “multiple level storage.” The SONOS/NROM cell stores charge in two distinct locations – in the nitride over the source and drain junctions. Thus, in the simplest case there are two distinct bits within each cell; however, each charge location may be partitioned into multiple levels, thereby, increasing the bit storage per cell.
- [33] The expected “typical” SONOS/NROM NOR area per bit is presented in terms of micrometers squared.
- [34] This is the physical length of the gate of SONOS/NROM devices in micrometers as there is only a single gate, similar to a MOSFET.
- [35] This is the highest voltage relative to ground seen in the cell array. It is not usually an external supply.
- [36] Reduction rate is higher than $(W/L) \cdot Cox$ to reduce the voltage overdrive factor.
- [37] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This offers a challenge to scaling.
- [38] The nitride dielectric provides the charge storage medium and its thickness is a compromise between program/erase voltages, erase/write window, retention, process control and endurance. This offers a challenge to scaling.
- [39] The blocking (top) oxide thickness isolates the charge storage region (nitride) from the gate electrode. Its thickness is a compromise between program/erase voltages and retention. This offers a challenge to scaling.
- [40] E/W endurance (erase/write cycles) requirements vary with the specifics of an application, but $1E5$ cycles has been accepted as the historical minimum acceptable level for a useful product. It is expected that emerging technology will allow both tradeoffs of endurance for retention as well as increases in the specified minimum endurance capability as device design options.
- [41] Retention is a defect related parameter rather than an intrinsic device characteristic. Improvement in defect control and accumulation of device history is expected to eventually allow specification of 20 years retention. Also, it should become possible to accept a reduced retention specification as a tradeoff for increased E/W endurance.
- [42] MRAM devices are expected to lag the CMOS current technology node up until the 65 nm node in 2007. This entry provides the F value for designs in the indicated time period.
- [43] The area factor “ a ” = cell area/ F^2 . This entry is the expected MRAM cell area in multiples of the implementation technology node F^2 .
- [44] The expected “typical” MRAM cell size is presented in micrometers squared.
- [45] The MRAM switching field is the magnetic intensity H required to change the direction of magnetization of the cell.
- [46] MRAM switching energy per bit is calculated as (write current * power supply voltage * write time). It is preferred to use the median value of switching energy measured on a multi-megabit array. A good estimate of power drain is (switching energy * number of writes per second).
- [47] MRAM active bit area is the area of the magnetic material stack within the cell. It represents the “ A ” in the $R \cdot A$ product.
- [48] MRAM resistance-area product (i.e., the $R \cdot A$ product) is an intrinsic property of the magnetic material stack that provides a convenient basis for comparing cells of different sizes. The $R \cdot A$ product can be computed by measuring the effective low state resistance (R_{low}) of the magnetic tunnel junction and multiply it by the active bit area of the magnetic stack.
- [49] MRAM magnetoresistive ratio is calculated as $100 \cdot (R_{high} - R_{low}) / R_{low}$. This ratio summarizes the difference between a logic ONE and a logic ZERO, and as such it represents the intrinsic capability of the magnetic stack. The magnetic tunnel junction resistance values are to be measured at low currents.
- [50] MRAM devices are required to retain data while unpowered. This entry states the retention requirement in years.
- [51] This entry is the required number of read/write cycles that an MRAM device must be able to endure without degradation that impacts the ability of the device to pass all operating specifications.
- [52] An MRAM device is required to meet this minimum life requirement when the magnetic material stack is continuously under bias.

Table 51 Reliability Difficult Challenges

<i>Difficult Challenges ≥ 45 nm/ Through 2010</i>	<i>Summary of Issues</i>
High- κ Gate Dielectrics	Dielectric breakdown characteristics (hard and soft breakdown) Influence of charge trapping and NBTI on threshold voltage stability Stability and number of fixed charges
Metal Gate	Impact of metal-ion drift and/or diffusion on gate dielectric reliability Work function control and stability Metal susceptibility to oxidation Thermo-mechanical issues due to large thermal expansion mismatch Impact of implantation
Copper/Low- κ Interconnects	Stress migration of Cu vias and lines Cu via and line electromigration performance Thermal-mechanical stability of the interfaces between metals, barriers and interlevel dielectrics and resulting line-to-line leakage Time Dependent Dielectric Breakdown (TDDB) of the Cu/low- κ system Reliability impact of lower thermal conductivity of low- κ dielectric Reliability issues due to the porous nature of the low- κ dielectrics and moisture Reliability impact of the lower mechanical strength in the Cu/low- κ system, including the impact of packaging
Packaging	Ability of bumps to withstand thermal and mechanical stresses while providing sufficient current carrying capability Solder joints fracture at 1 st and 2 nd level interconnects Electromigration in package traces, vias and bumps Impact of increasing Coefficient of Thermal Expansion (CTE) mismatch between low- κ , silicon and organic packages
Design and Test for Reliability	Simulation tools for concurrent optimization of circuit performance and reliability Tools to simulate electromigration, thermal-mechanical stress and process induced charging Soft error detection and correction at chip and system level, including random logic faults Screens for resistive and capacitively coupled interconnect defects Alternative screens for decreasing burn-in effectiveness

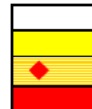
Table 52a Reliability Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009	
Technology Node		hp90			hp65			
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50	
Early failures (ppm) (First 4000 operating hours)** [1]	50–2000	50–2000	50–2000	50–2000	◆50–2000	◆50–2000	◆50–2000	Customer needs; new materials (High κ in 2004)
Long term reliability (FITs = failures in 1E9 hours) [2]	10–100	10–100	10–100	10–100	◆10–100	◆10–100	◆10–100	Customer needs; new materials (High κ in 2004)
Soft error rate (FITs)	1000	1000	1000	1000	◆1000	◆1000	◆1000	Scaling
Relative failure rate per transistor (normalized to 130 nm) [3]	1	0.8	0.63	0.5	◆ 0.4	TBD	TBD	Number of transistors
Relative failure rate per m of interconnect (normalized to 130 nm node) [4]	1	0.84	0.64	0.58	◆ 0.52	◆ 0.41	◆ 0.37	Customer needs; J11 length of interconnect

Table 52b Reliability Technology Requirements—Long-term

Year of Production	2010	2012	2013	2015	2016	2018
Technology Node	hp45		hp32		hp22	
DRAM ½ Pitch (nm)	45	35	32	25	22	18
Early failures (ppm) (First 4000 operating hours)**[1]	◆50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
Long term reliability (FITs = failures in 1E9 hours) [2]	◆10–100	10–100	10–100	10–100	10–100	10–100
Soft error rate (FITs)	◆ 1000	1000	1000	1000	1000	1000
Relative failure rate per transistor (normalized to 130 nm) [3]	◆ 0.2		0.1		0.04	
Relative failure rate per m of interconnect (normalized to 130 nm) [4]	◆ 0.36	0.26	0.25	0.16	0.17	0.11

Manufacturable solutions exist, and are being optimized
 Manufacturable solutions are known
 Interim solutions are known
 Manufacturable solutions are NOT known



Notes for Tables 52a and 52b

Reliability requirements vary with different applications. For many mainstream customers it will be sufficient to hold current reliability levels steady during this period of rapid technological change. However, other customers would like reliability levels to be improved. Degradation of current reliability levels is not acceptable. Reliability requirements are for the packaged device and include both chip and package related failure modes.

A reliability qualification can always be attempted with available knowledge. The better the knowledge the less risk in the qualification and vice versa. Yellow coloring indicates some risk. Striped indicates a greater risk (due to changed and possible new failure mode). Finally, red indicates an unspecified solution (e.g., what technology will be used for post-CU) for which the reliability risk cannot be assessed until details about the solution are provided.

[1] Failures during the first 4000 hours of operation (~1 year's use at 50% duty cycle). Early failures are associated with defects.

[2] Long term reliability rate applies for the specified lifetime of the IC.

[3] While the overall IC failure rate does not change with time, as the number of transistors increase [from ORTC], the relative failure rate per transistor must decrease.

[4] As the length of interconnect increases [from Interconnect Technology Requirements Tables], the failure rate per m of interconnect must decrease. Even more important for reliability is the increase in the number of vias.