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1. I am a Records Request Processor at the Internet Archive. I make this declaration of my own personal knowledge.

2. The Internet Archive is a website that provides access to a digital library of Internet sites and other cultural artifacts in digital form. Like a paper library, we provide free access to researchers, historians, scholars, and the general public. The Internet Archive has partnered with and receives support from various institutions, including the Library of Congress.

3. The Internet Archive has created a service known as the Wayback Machine. The Wayback Machine makes it possible to browse more than 450 billion pages stored in the Internet Archive's web archive. Visitors to the Wayback Machine can search archives by URL (i.e., a website address). If archived records for a URL are available, the visitor will be presented with a display of available dates. The visitor may select one of those dates, and begin browsing an archived version of the Web. Links on archived files in the Wayback Machine point to other archived files (whether HTML pages or other file types), if any are found for the URL indicated by a given link. For instance, the Wayback Machine is designed such that when a visitor clicks on a hyperlink on an archived page that points to another URL, the visitor will be served the archived file found for the hyperlink's URL with the closest available date to the initial file containing the hyperlink.

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5. The Internet Archive assigns a URL on its site to the archived files in the format http://web.archive.org/web/[Year in yyyy][Month in mm][Day in dd][Time code in hh:mm:ss]/[Archived URL] aka an "extended URL". Thus, the extended URL http://web.archive.org/web/19970126045828/http://www.archive.org/ would be the URL for the record of the Internet Archive home page HTML file (http://www.archive.org/) archived on January 26, 1997 at 4:58 a.m. and 28 seconds (1997/01/26 at 04:58:28). The date indicated by an extended URL applies to a preserved instance of a file for a given URL, but not necessarily to any other files linked therein. Thus, in the case of a page constituted by a primary HTML file and other separate files (e.g., files with images, audio, multimedia, design elements, or other embedded content) linked within that primary HTML file, the primary HTML file and the other files will each have their own respective extended URLs and may not have been archived on the same dates.

6. Attached hereto as Exhibit A are true and accurate copies of screenshots of the Internet Archive's records of the archived files for the URLs and the dates specified in the attached coversheet of each printout.

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INTERNET ARCHIVE
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7. Attached hereto as Exhibit B are true and accurate copies of the Internet Archive's records of the archived files for the URLs and the dates specified in the following table.

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2	https://web.archive.org/web/20070713160842/http://www.itrs.net/Links/2000UpdateFinal/ProcessInt2000final.pdf
3	https://web.archive.org/web/20070712171234/http://www.itrs.net/Links/2002Update/2002UpdateForeword.pdf
4	https://web.archive.org/web/20070712170801/http://www.itrs.net/Links/2002Update/2002UpdateTOC.pdf
5	https://web.archive.org/web/20070712171252/http://www.itrs.net/Links/2002Update/2002UpdateIntroduction.pdf
6	https://web.archive.org/web/20070712171206/http://www.itrs.net/Links/2002Update/2002Update_ORTC.pdf
7	https://web.archive.org/web/20070712171327/http://www.itrs.net/Links/2002Update/2002UpdatePIDS.pdf
8	https://web.archive.org/web/20050504213554/http://www.itrs.net/Common/2004Update/2004_00_Overview.pdf
9	https://web.archive.org/web/20050504214740/http://www.itrs.net/Common/2004Update/2004_000_ORTC.pdf
10	https://web.archive.org/web/20050504212107/http://www.itrs.net/Common/2004Update/2004_01_Design.pdf
11	https://web.archive.org/web/20050504213243/http://www.itrs.net/Common/2004Update/2004_03_PIDS.pdf
12	https://web.archive.org/web/20091123045129/http://www.itrs.net/Links/2007ITRS/ExecSum2007.pdf
13	https://web.archive.org/web/20090306164145/http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_PIDS.pdf
14	https://web.archive.org/web/20100331015639/http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_ExecSum.pdf
15	https://web.archive.org/web/20100331062345/http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_PIDS.pdf
16	https://web.archive.org/web/20110626201042/http://www.itrs.net/Links/2010ITRS/2010Update/ToPost/2010_Update_Overview.pdf

8. I declare under penalty of perjury that the foregoing is true and correct.

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Nathaniel E Frank-White

Nathaniel E Frank-White

EXHIBIT A

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International Technology Roadmap for Semiconductors

The ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual products or equipment.

Welcome to the International Technology Roadmap for Semiconductors web site!

- The 2004 Update is now available here. Of the 219 tables contained in the 2003 ITRS, 128 tables were updated and 4 new tables were added. Additionally, 12 figures were updated. Many of the difficult challenges for the ITRS were revisited and updated to reflect the most current thinking and most critical tasks for semiconductor R&D.
- A presentation of 2004 Key Messages from the working groups is available here.
- *The next ITRS public conference will be held in Munich, Germany.*
  Date: April 12, 2005 - Assembly & Packaging presentation in the afternoon
  April 13, 2005 - all other Working Group presentation
  Location: Munich Fair along with SEMICON Europe

  More Information Coming Soon !

The First International Nanotechnology Conference on Communication & Cooperation 2005 (INC1)

The First International Nanotechnology Conference on Communication & Cooperation 2005 (INC1) will be held June 1 - 3, 2005 at the San Francisco Marriott Hotel in California, USA.

The conference is being organized by the European Commission, Fraunhofer, IMEC, LETI, NSF/NNI, SIA, SRC, and SEMATECH. The Cabinet Office of Japan and JEITA/JSIA join

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2004 Update Tables

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If you are having problems opening the PDF files after you download them to your harddrive, please go to the Adobe site and download the latest version of Acrobat Reader and install it on your computer. This should solve your problem.

Overview
Overall Roadmap Technology Characteristics (ORTC)
Design
Test & Test Equipment
Process Integration, Devices & Structures
RF & A/MS Technologies for Wireless
Emerging Research Devices
Front End Processes
Lithography
Interconnect
Factory Integration
Assembly & Packaging
Environment, Safety & Heatlh
Yield Enhancement
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Thank you for your interest and visit! The International Technology Roadmap for Semiconductors, known throughout the world as the ITRS, is the fifteen-year assessment of the semiconductor industry's future technology requirements. These future needs drive present-day strategies for world-wide research and development among manufacturers' research facilities, universities, and national labs.

The International Roadmap Committee (IRC) clarifies the ITRS position on the Roadmap product drivers, technology pacing, and use of the term "technology nodes" by the industry and press. This link is **an excerpt of the 2007 ITRS Technology Pacing section** discussing these concepts in detail.

The **2007 Executive Summary** is now available for download!
The 2007 ITRS ITWG chapters are also online at the **2007 ITRS Reports page**.

The most recent Roadmap was presented in Makuhari, Japan on December 5, during the ITRS Winter Public Conference. **As part of the 2007 ITRS release, all presentations are available for download.**

We are reviewing the final drafts of the ITRS ITWG chapters. These are scheduled to be posted later this month.

The ITRS teams encourage feedback from the community of ITRS users. You can be a part of this community. Please request an account with us to access the Public Forum area, and provide your comments on the ITRS. The subscription process is quick and your privacy is ensured. We do not share any of your personal information.

For questions, please contact the ITRS manager, **Linda Wilson**.

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On-Line Documents

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2007 Edition
2006 Update
2005 Edition
2004 Update
2003 Edition
2002 Update
2001 Edition
2000 Update

Other ITRS Materials (books, CDs)

A limited number of hard copy books are available for the 2005 ITRS and previous roadmaps (1994, 1997, 1999, 2001, 2003).

The 2005 ITRS book is sold by the Japan Electronics and Information Technology Association [JEITA]; order this report from **the JEITA website**.

The 2005 ITRS is also available as a CD set that includes a printed version of the Executive Summary.

Ordering Information

To order a roadmap report, download the order form as a **MS Word** auto form or a **printable PDF** form.

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2000 Update

Overall Roadmap Technology Characteristics (ORTC)
Design
Test
PIDS
Front End Processes
Lithography
Interconnect
Factory Integration
Assembly & Packaging
Environment, Safety & Heatlh
Defect Reduction
Metrology
Modeling & Simulation

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2002 Update

Key Changes
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Process Integration, Devices & Structures (includes Emerging Research Devices)
Front End Processes
Lithography
Interconnect
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Assembly & Packaging
Environment, Safety & Health
Yield Enhancement
Metrology
Modeling & Simulation

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ITRS 2007 Edition

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Front End Processes
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Acronyms

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2009 ROADMAP INFORMATION

The NEW **ITRS 2009 Edition** is now released!

As part of the 2009 release, the **2009 Winter Conference Presentations** are available.

The ITRS media partner, **Future Fab International,** devotes the January 2010 issue to the new 2009 ITRS.



The International Roadmap Committee (IRC) clarifies the ITRS position on the Roadmap product drivers, technology pacing, and use of the term "technology nodes" by the industry and press. This link is **an excerpt of the 2007 ITRS Technology Pacing section** discussing these concepts in detail.

2010 Nanoelectronics Events !

The International Nanotechnology Conference on Communication and Cooperation (INC6).
17 - 20 May, 2010
Grenoble, France

17 May 2010
European Nano Day
These sessions will provide an overview of nanotechnology in Europe.

WMSN-MtM Workshop
The results from this Workshop are expected to provide relevant inputs for:

1) The planning of future editions of the ITRS and

2) How the ITRS relates to other organizations that have ongoing and planned international roadmaps concerning nanoelectronics. These other organizations include the International Electrotechnical Commission, the International Standards Organization, and the Institute of Electrical and Electronics Engineers.

18 – 20 May 2010
INC6

We hope to see you at this most important meeting discussing international cooperation and the direction of nanotechnologies within the research communities of Europe, Japan, and the USA.

Come hear world-renowned speakers from around the world, and participate in a venue of direct dialog with them.

For questions, please contact the ITRS manager, **Linda Wilson**.

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ITRS 2009 Edition

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Test & Test Equipment
Process Integration, Devices & Structures *[PIDS files re-posted on Feb 25 to include Table PIDS5A]*
RF and A/MS Technologies for Wireless Communications
Emerging Research Devices
Emerging Research Materials
Front End Processes
Lithography
Interconnect - in review
Factory Integration
Assembly & Packaging - in review
Environment, Safety & Health
Yield Enhancement - in review
Metrology
Modeling & Simulation

2009 ITRS Table Files Links

ORTC Tables	Overall Technology Roadmap Characters. (Key Roadmap Drivers)
FOCUS A Tables	Test & Test Equipment | RF and AMS for Wireless
FOCUS B Tables	Emerging Research Devices (ERD) | Emerging Research Materials (ERM)
FOCUS C Tables	Front-end Processes (FEP) | Process Integration, Devices, & Structures (PIDS)
FOCUS D Tables	Lithography | Factory Integration
FOCUS E Tables	Interconnect | Assembly and Packaging
FOCUS F Tables	System Drivers | Design
CROSS CUT A Tables	Environment, Safety, & Health (ESH) | Metrology | Modeling & Simulation
CROSS CUT B Tables	Yield Enhancement
Acronyms	

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The 2010 Update is now online! These downloadable files contain the most recent information from the ITRS International Technology Working Groups. The 2010 Update is a collection of updated tables and figures from the 2009 ITRS and are based on the latest information from the industry.

The International Roadmap Committee (IRC) clarifies the ITRS position on the Roadmap product drivers, technology pacing, and use of the term "technology nodes" by the industry and press. This link is **an excerpt of the 2007 ITRS Technology Pacing section** discussing these concepts in detail.

More than Moore White Paper

The IRC has released a new white paper on the topic "More than Moore" and roadmapping. This white paper proposes a methodology to help the ITRS community identify those More than Moore (MtM) technologies for which a roadmapping effort is feasible and desireable. This document is now available for download.

2011 ITRS EVENTS !

Mark your calendars! More information coming soon!

2011 ITRS Spring More Than Moore Workshop
April 13, 2011
Pottsdam, Germany

2011 ITRS Summer Public Conference
July 13, 2011
San Francisco, California

2011 ITRS Winter Public Conference
December 14, 2011
Seoul, Korea

For questions, please contact the ITRS manager, **Linda Wilson**.

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ITRS 2010 Update

2010 Acknowledgments

The 2010 Update files below are a result of continued review by each of the working groups and contain the latest information available from these committees. Based on the 2009 ITRS, these files now include printable table notes for all the tables. Links to the 2009 chapters are included on this page, too.

2010 Update Overview

2010 Overall Roadmap Technology Characteristics (ORTC) Tables

2009 Executive Summary

International Technology Working Group	*2010 Update*	*2009 ITRS*
System Drivers	2010 updated figures	2009 chapter
Design	2010 updated section and figure	2009 chapter
Test and Test Equipment	2010 tables	2009 chapter
Process Integration, Devices, and Structures (PIDS)	2010 tables	2009 chapter
RF and A/MS Technologies for Wireless Communications	2010 tables	2009 chapter
Emerging Research Devices (ERD) Emerging Research Materials (ERM)	2010 Future Memory Devices Workshop Summary	ERD 2009 chapter ERM 2009 chapter
Front End Processes (FEP)	2010 tables	2009 chapter
Lithography	2010 tables	2009 chapter
Interconnect	2010 tables	2009 chapter
Factory Integration	2010 tables	2009 chapter
Assembly & Packaging	2010 tables	2009 chapter
Environment, Safety & Health	2010 tables	2009 chapter
Yield Enhancement	2010 tables	2009 chapter
Metrology	2010 tables	2009 chapter
Modeling & Simulation	2010 tables	2009 chapter
		2009 ERRATA-Executive Summary, list of corrections

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EXHIBIT B

FOLDER 1

International Technology Roadmap for Semiconductors

2000 Update

Overall Roadmap Technology Characteristics

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OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS & GLOSSARY

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) 2000 Update Tables have been revised from the *International Technology Roadmap for Semiconductors, 1999 edition* (ITRS) ORTC to highlight the current rapid pace of advancement in semiconductor technology. They represent a "snapshot" of the work in progress by the International Roadmap Committee (IRC) and the International Technology Working Groups (ITWGs) as they prepare for the full revision of the ITRS in 2001.

The ORTC tables are used throughout the update and renewal of the ITRS to identify rapidly changing, leading-edge trends and provide synchronization among the ITWGs. In July 2000, the IRC reached consensus on proposing "most aggressive" values for a few high-level ORTC line items that were then used to drive the complete ORTC update. These values represent the most optimistic of three scenarios (see details below) that are still under discussion in preparation for the 2001 edition of the ITRS. Thus, they represent a start toward creating new ORTC tables early in the 2001 ITRS revisondevelopment process.

With respect to the ITWG tables, the activities for the 2000 Update are limited to review and correction as possible considering all tables from the 1999 ITRS. Some ITWG tables do not comprehend this "most aggressive" ORTC 2000 Update. Inconsistencies among the ITWG and ORTC tables are part of this work-in-progress as we move towards the full revision of the ITRS in 2001. Therefore we encourage review of the ITWG tables as a response-to-date.

The 2001 activities focus on a complete revision of the ITRS. Once we have consensus on the 2001 ORTC tables, they will serve as a guide for the activities of the International Technology Working Groups in producing their detailed chapters for the 2001 edition.

The complete 1999 ITRS, along with the latest 2000 Update Tables are available for viewing and printing as an electronic document at the International SEMATECH internet web site http://public.itrs.net.

UPDATE OVERVIEW AND OBSERVATION SUMMARY

Please note that the year header on the tables may refer to different points in the development/life cycle of integrated circuits (ICs), depending on the individual line item metric. However, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds 10,000 units per month of ICs from a manufacturing site using "production tooling." Additional clarification was provided this year by the IRC, requiring a second company to start production within 3 months. To satisfy this definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility.

Furthermore, new IRC guidelines clarified the definition of a Technology Node as the achievement of significant advancement in the process technology. To be explicit, a Technology Node was defined as the achievement of an approximate 0.7x reduction per node (0.5x per two nodes). The period of time in which a new Technology Node is reached is called a "technology-node cycle." It is acknowledged that continuous improvement occurs between Technology Nodes, and this is reflected by arithmetic interpolation between nodes in the annual columns of the "Near-Term Years" tables. The "Long Term Years" table columns are snapshots at 3-year increments and do not necessarily coincide with Technology Node Years.

In the 1998 ITRS Roadmap Update and the 1999 ITRS Renewal development, a trend was first identified which indicated that the technology node cycle had accelerated by at least one year compared to the 1997 National Technology Roadmap for Semiconductors (NTRS). Additionally, it was discussed that the technology

implementation trend could be moving from a 3-year technology-node cycle to a 2-year rate, and a pull-in of the 130nm node to 2001 was anticipated. However, by the completion of the work on the 1999 ITRS in November, 1999, the 180nm node was pulled in one year to 1999, a 3-year technology node cycle was applied, and the 130nm DRAM half-pitch node target remained in 2002.

During their 2000 ITRS Update activities, the ITWGs and the IRC have concluded that a two-year DRAM half-pitch node cycle rate will indeed be maintained through 2001, pulling in the original 1999 ITRS 130nm node target from 2002 to 2001. Beyond 2001, three possible scenarios were considered for potential technology node (DRAM half-pitch) trends, as summarized below:

Scenario 1 (Sc. 1.0): Pull-in the 130nm DRAM half-pitch to 2001, but then intersect with the original 100nm 1999 ITRS target in 2005. Next, interpolate the annual numbers in-between and extrapolate from the 100nm/2005 point at a 70%/node (0.5×/2nodes) reduction rate.

Scenario 1.5 (Sc. 1.5): Pull-in the 130nm DRAM half-pitch to 2001, but move 100nm to 2004 (a corresponding 1-year pull-in from the original 1999 ITRS point in 2005); then, interpolate the annual numbers in-between, and extrapolate from the new 100nm/2004 point at a 70%/node (0.5×/2nodes) reduction rate.

Scenario 2.0 (also known as the "Best-Case Opportunity" or "Most Aggressive" case) (Sc. 2.0): Pull-in the 130nm DRAM half-pitch to 2001, and also correct the original 100nm, 70nm, 50nm, and 35nm "nodes" to the 70%/node definition (0.5×/2nodes rate): 90nm, 65nm, 33nm, and 23nm, respectively.

Please note in Figure 1 and in Table A the 3-year node cycle is being forecast as a future trend for all scenarios. However, only the new “most aggressive” scenario proposal, Scenario 2.0, includes a correction to the IRC-defined trend rate. The new correction results in a 2-year pull-in of the sub-100-nanometer DRAM half-pitch nodes.

As previously mentioned, for simplification and focus in the 2000 Update publication, only the proposed “most aggressive” Scenario 2.0 was used to develop the complete ORTC Update Tables included in this ORTC 2000 Update document. Scenario 2.0 was also recommended by the IRC for use by the ITWGs as guidance in developing their 2000 Update Tables. The ITWGs responded in their ITWG 2000 Update tables.

For reference and ease of comparison by the reader, the original 1999 ITRS ORTC target roadmap data has been included and identified as **“1999 ITRS”** in the line item labels. The new proposal targets for the 2000 Update “most aggressive” scenario are identified as “**Sc. 2.0**” in the line item identifier, and modified targets are highlighted in **bold blue text**.

Note in Figure 1 that the “printed in resist” MPU Gate Length trend, originally introduced in the 1998/99 ITRS development, remains unchanged from its original trend, but now the leading-edge ASIC and MPU are at the same technology level. New for the 2000 Update is the addition of a trend to track the actual “Physical Bottom Gate Length” of leading-edge MPU and ASIC devices.

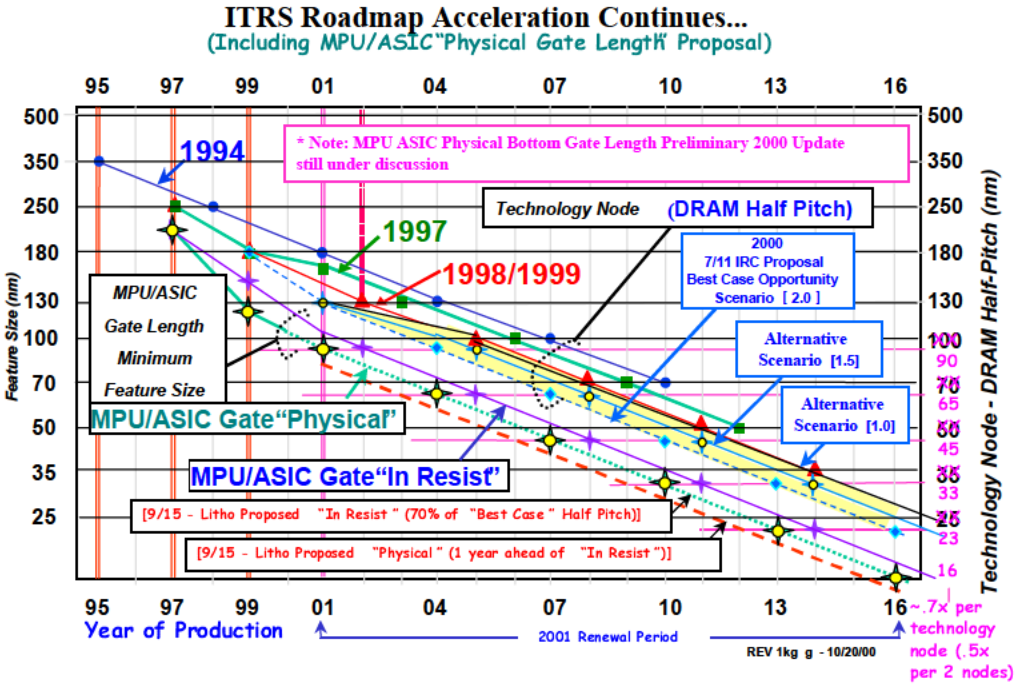


Figure 1 ITRS Roadmap Acceleration Continues...
(Including MPU/ASIC "Physical Gate Length" Proposal and Half-Pitch Trend Correction)

Table A Product Generations and Chip Size Model - ***Technology Node Scenarios***

Year of Production / *Technology Node* **WAS (1999 ITRS)**	*1999* *180nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*		*2008* *70 nm*	*2011* *50 nm*	*2014* *35 nm*
DRAM ½ Pitch (nm) **WAS (1999 ITRS)**	180	165	150	130	120	110	100		70	50	35
DRAM ½ Pitch (nm) ***IS [Sc.1.0]*** ***[pull-in 130nm 1 year; 100nm/2005; then .7x/3yrs reduction rate]***	180	**150**	**130**	**120**	**115**	**105**	100		70	50	35
DRAM ½ Pitch (nm) ***IS [Sc. 1.5]*** ***[pull-in 130nm 1 year; 100nm/2004; then.7x/3yrs reduction rate]***	180	**150**	**130**	**120**	**110**	**100**	**90**		**65**	**45**	**33**
DRAM ½ Pitch (nm) ***IS [Sc.2.0]*** ***[pull-in 130nm 1 year; then .7x/3yrs reduction rate]***	180	**150**	**130**	**115**	**100**	**90**	**80**		**[60]§**	**[40]§**	**[30]§**

§ Note that proposed node years for Scenario 2.0 are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1a Product Generations and Chip Size Model Technology Nodes—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
Lithography-Based Characteristics								
DRAM ½ Pitch (nm) (1999)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch (nm) (SC. 2.0)	180	150	130	115	100	90	80	D ½
MPU/ASIC ½ Pitch (nm) (1999)	230	210	180	160	145	130	115	M AND A ½
MPU/ASIC ½ Pitch (nm) (SC. 2.0) [Tied to DRAM]	230	190	160	145	130	115	100	M AND A ½
MPU Gate Length (nm) †† (1999)	140	120	100	85-90	80	70	65	M GATE
ASIC Gate Length (nm) (1999)	180	165	150	130	120	110	100	A GATE
MPU/ASIC Gate Length (In Resist) (nm) †† (SC. 2.0)	140	120	100	90	80	70	65	M AND A GATE
Physical Bottom Gate-Length								
MPU/ASIC Gate Length (nm) †† [NEW]	120	100	90	80	70	65	60	COST/PERFORMANCE

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1b Product Generations and Chip Size Model Technology Nodes—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Lithography-Based Characteristics			
DRAM ½ Pitch (nm) (1999)	70	50	35
DRAM ½ Pitch (nm) (SC. 2.0)	60	40	30
MPU/ASIC ½ Pitch (nm) (1999)	80	55	40
MPU/ASIC ½ Pitch (nm) (SC. 2.0) [Tied to DRAM]	70	50	35
MPU Gate Length (nm) †† (1999)	45	30-32	20-22
ASIC Gate Length (nm) (1999)	70	50	35
MPU/ASIC Gate Length (In Resist) (nm) †† (SC. 2.0)	45	33	23
Physical Bottom Gate-Length			
MPU/ASIC Gate Length (nm) †† [NEW]	40	30	20

†† MPU and ASIC Gate-length (In Resist) node targets refer to most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon", in the 1999 ITRS).

NEW: Trends have been identified, in which the MPU and ASIC "physical bottom" gate lengths may be reduced from the "as-printed" dimension. These "physical bottom" gate-length targets are also included in the FEP, PIDs, and Design TWG Tables as needs which drive device and process technology requirements.

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1c **DRAM Production** Product Generations and Chip Size Model—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
DRAM ½ Pitch [f] (nm) (1999)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch [f] (nm) SC. 2.0)	180	150	130	115	100	90	80	D ½
Cell area factor [A] (1999)	8.0	7.3	6.6	6.0	5.4	4.9	4.4	Market — Cost/Timing
Cell area factor [A] (SC. 2.0)	8.0	8.0	8.0	8.0	8.0	8.0	6.0	Market — Cost/Timing
Cell area [Ca = Af^2] (μm^2) (1999)	0.26	0.20	0.15	0.10	0.08	0.059	0.044	Market — Cost/Timing
Cell area [Ca = Af^2] (μm^2) (SC. 2.0)	0.26	0.18	0.13	0.10	0.082	0.065	0.039	Market — Cost/Timing
Cell array area at production (% of chip size) § (1999)	53%	—	55%	—	53%	—	54%	Market — Cost/Timing
Cell array area at production (% of chip size) § (SC. 2.0)	53.0%	54.0%	54.8%	55.3%	55.7%	56.1%	56.4%	Market — Cost/Timing
Generation at production § (1999)/(SC. 2.0)	256M	—	512M	—	1G	—	2G	Market — Cost/Timing
Functions per chip (Gbits) [NEW]	0.268	0.380	0.537	0.759	1.07	1.52	2.15	Market — Cost/Timing
Chip size at production (mm^2) § (1999)	132	—	145	—	159	—	174	Market — Cost/Timing
Chip size at production (mm^2) § (SC. 2.0)	131	129	127	141	157	175	147	Market — Cost/Timing
Gbits/cm^2 at production § (1999)	0.20	—	0.37	—	0.68	—	1.23	Market — Cost/Timing
Gbits/cm^2 at production § (SC. 2.0)	0.20	0.29	0.42	0.54	0.68	0.87	1.46	Market — Cost/Timing

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1d DRAM Production Product Generations and Chip Size Model—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (Sc. 2.0)	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]
DRAM ½ Pitch [f] (nm) (1999)	70	50	35
DRAM ½ Pitch [f] (nm) (SC. 2.0)	60	40	30
Cell area factor [A] (1999)	3.5	3.0	2.5
Cell area factor [A] (SC. 2.0)	6.0	4.0	4.0
Cell area [Ca = Af²] (μm^2) (1999)	0.017	0.008	0.003
Cell area [Ca = Af²] (μm^2) (SC. 2.0)	0.019	0.0064	0.0032
Cell array area at production (% of chip size) § (1999)	52%	56%	57%
Cell array area at production (% of chip size) § (SC. 2.0)	57.3%	57.8%	58.2%
Generation at production § (1999)	[5.7]	16G	[45.2G]
Generation at production § (SC. 2.0)	[6G]	16G	[48G]
Functions per chip (Gbits) [NEW]	6.1	17.2	48.6
Chip size at production (mm^2) § (1999)	199	229	262
Chip size at production (mm^2) § (SC. 2.0)	205	191	268
Gbits/cm^2 at production § (1999)	3.05	7.51	18.5
bits/cm^2 at production § (SC. 2.0)	2.97	8.99	18.1

§ DRAM Model—Cell Factor (design/process improvement) targets are: 1999-2004/8x; 2005-2010/6x; 2011-2016/4x. DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except: 1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4x/5years (2x/2-3yrs); and 2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4x/5years (2x/2-3yrs). InTER-generation chip size growth rate varies to maintain 1 chip per 572mm^2 field at Introduction and 2 chip per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2x bits/chip every 2 years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Note: Long-Term nodes now fall on: 2010/45; 2013/33; 2016/25

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1e **DRAM Introduction** Product Generations and Chip Size Model—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
DRAM ½ Pitch [f] (nm) (1999)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch [f] (nm) (SC. 2.0)	180	150	130	115	100	90	80	D ½
Cell area factor [A] (1999)	8.0	7.3	6.6	6.0	5.4	4.9	4.4	Market — Cost/Timing
Cell area factor [A] (SC. 2.0)	8.0	8.0	8.0	8.0	8.0	8.0	6.0	Market — Cost/Timing
Cell area [Ca = Af^2] (μm^2) (1999)	0.26	0.20	0.15	0.10	0.08	0.059	0.044	Market — Cost/Timing
Cell area [Ca = Af^2] (μm^2) (SC. 2.0)	0.259	0.183	0.130	0.103	0.082	0.065	0.039	Market — Cost/Timing
Cell array area at introduction (% of chip size) § (1999)	70%	—	72%	—	70%	—	72%	Market — Cost/Timing
Cell array area at introduction (% of chip size) § (SC. 2.0)	69.5%	70.5%	71.3%	71.8%	72.2%	72.6%	72.9%	Market — Cost/Timing
Generation at introduction § (1999)	1G	—	2G	—	4G	—	8G	—
Generation at introduction § (SC. 2.0)	1G	—	2G	—	4G	—	8G	—
Functions per chip (Gbits) (1999)	1.07	—	2.15	—	4.29	—	8.59	Market — Moore's Law
Functions per chip (Gbits) (SC. 2.0)	1.07	1.52	2.15	3.04	4.29	6.07	8.59	Market — Cost/Timing
Chip size at introduction (mm^2) § (1999)	400	—	438	—	480	—	526	Market — Cost/Timing
Chip size at introduction (mm^2) § (SC. 2.0)	400	395	390	435	485	542	454	Market — Cost/Timing
Gbits/cm^2 at introduction § (1999)	0.27	—	0.49	—	0.89	—	1.63	Market — Cost/Timing
Gbits/cm^2 at introduction § (SC. 2.0)	0.27	0.38	0.55	0.70	0.88	1.12	1.89	Market — Cost/Timing

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1f **DRAM Introduction** Product Generations and Chip Size Model—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
DRAM ½ Pitch [f] (nm) (1999)	70	50	35
DRAM ½ Pitch [f] (nm) (SC. 2.0)	60	40	30
Cell area factor [A] (1999)	3.5	3.0	2.5
Cell area factor [A] (SC. 2.0)	6.0	4.0	4.0
Cell area [Ca = Af²] (μm^2) (1999)	0.017	0.008	0.003
Cell area [Ca = Af²] (μm^2) (SC. 2.0)	0.019	0.0064	0.0032
Cell array area at introduction (% of chip size) § (1999)	69%	75%	75%
Cell array area at introduction% of chip size) § (SC. 2.0)	73.3%	74.3%	74.7%
Generation at introduction § (1999)	[22.6G]	64G	[181G]
Generation at introduction § (SC. 2.0)	[20G]	[45G]	[104G]
Functions per chip (Gbits) (1999)	24.3	68.7	194
Functions per chip (Gbits) (SC. 2.0)	19.7	45.3	104.2
Chip size at introduction (mm^2) § (1999)	603	691	792
Chip size at introduction (mm^2) § (SC. 2.0)	516	392	448
Gbits/cm^2 at introduction § (1999)	4.03	9.94	24.5
Gbits/cm^2 at introduction § (SC. 2.0)	3.82	11.56	23.25

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1g **MPU (High-volume Microprocessor) Cost-Performance** Product Generations and Chip Size Model—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
Process/design annual improvement factor ++ (1999)	0.90	0.90	0.90	0.91	0.92	0.93	0.93	Market — Cost/Timing
(SC. 2.0)	1.00	1.00	1.00	0.93	0.93	0.93	0.93	
Transistor density SRAM at introduction (Mtransistors/cm^2) (1999)/(SC. 2.0)	35	50	70	95	128	173	234	Market — Cost/Timing
Transistor density logic at introduction (Mtransistors/cm^2) (1999)/(SC. 2.0)	6.6	9.4	13	18	24	33	44	Market — Cost/Timing
Generation at introduction * (1999)/(SC. 2.0)	p99c	—	p01c	—	p03c	—	p05c	—
Functions per chip (million transistors [Mtransistors]) (1999)	23.8	—	47.6	—	95.2	—	190	Market — Moore's Law
(1999)/(SC. 2.0)	23.8	33.7	47.6	67.3	95.2	135	190	
Chip size at introduction (mm^2) ‡ (1999)	340	—	340	—	372	—	408	Market — Cost/Timing
(SC. 2.0)	340	340	340	356	372	390	408	
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡ (1999)	7	—	14	—	26	—	47	M Gate and M and A ½
(SC. 2.0)	7.0	9.9	14.0	18.9	25.6	34.5	46.7	
Generation at production *	p97c	—	p99c	—	p01c	—	P03c	—
Chip size at production (mm^2) §§ (1999)	170	—	170	—	214	—	235	Market — Cost/Timing
(SC. 2.0)	170	170	170	178	186	195	204	
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡ (1999)	7	—	14	—	22	—	41	M Gate and M and A ½
(SC. 2.0)	7.0	9.9	14.0	18.9	25.6	34.5	46.7	

++ *The MPU Process/design improvement factor is an estimate of the additional annual functional area reduction required beyond the area reduction contributed by the MPU metal half-pitch reduction. Note that this additional area reduction for transistor density plays a role generally analogous to the "cell area factor" for DRAMs. It has been achieved historically through a combination of many factors, for example: use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout.*

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Process/design improvement factor (1999)	0.93	0.93	0.93
(SC. 2.0)	0.93	0.93	0.93
Transistor density SRAM at introduction (Mtransistors/cm^2) (1999)/(SC. 2.0)	577	1,423	3,510
Transistor density logic at introduction (Mtransistors/cm^2) (1999)/(SC. 2.0)	109	269	664
Generation at introduction * (1999)/(SC. 2.0)	—	p11c	—
Functions per chip (million transistors (Mtransistors) (1999)/(SC. 2.0)	539	1,523	4,308
Chip size at introduction (mm^2) ‡ (1999)	468	536	615
(SC. 2.0)	468	536	615
Cost-performance MPU Mtransistors/cm^2 at introduction (including on-chip SRAM) ‡ (1999)	115	284	701
(SC. 2.0)	115	284	701
Generation at production * (1999)/(SC. 2.0)	—	p09c	—
Chip size at production (mm^2) § (1999)/(SC. 2.0)	269	308	354
(SC. 2.0)	234	268	307
Cost performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡ (1999)	100	247	609
(SC. 2.0)	115	284	701

* p is processor, numerals reflect year of introduction, c is cost-performance product.

** p is processor, numerals reflect year at ramp, h is high-performance product.

† MPU Cost-performance Model—Cost-performance MPU includes small level 1 (L1) on-chip SRAM (32Kbyte/1999), but consists primarily of logic transistor functionality; both SRAM and Logic functionality doubles every two years.

‡ MPU High-performance Model—High-performance MPU includes large level 2 (L2) on-chip SRAM (2MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + 98Mtransistors (2048 bytes × 8 bits/byte × 6 transistors/bit) L2 SRAM = 110Mtransistors/1999); both SRAM and Logic functionality doubles every two years.

‡ MPU High-performance Model—High-performance MPU includes large level 2 (L2) on-chip SRAM (1MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + 49Mtransistors (1024 bytes × 8 bits/byte × 6 transistors/bit) L2 SRAM = 61Mtransistors/1999); both SRAM and Logic functionality doubles every two years.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates can be kept flat through 2001, due to the more aggressive MPU/ASIC half-pitch technology node trend; but beyond 2001, the target growth rate is 1.2× growth every four years. The InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1i **High-Performance MPU and ASIC** Product Generations and Chip Size Model—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
Logic (Low-volume Microprocessor) High-performance ‡								
Generation at production ** (1999)/(SC. 2.0)	p99h	—	p01h	—	p03h	—	p05h	—
Functions per chip (million transistors) (1999)	110	—	220	—	441	—	882	Market — Moore's Law
(SC. 2.0)	61	86	122	173	244	345	488	
Chip size at production (mm^2) § (1999)	450	—	450	—	567	—	622	Market — Cost/Timing
(SC. 2.0)	310	310	310	325	340	356	372	
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡ (1999)	24	—	49	—	78	—	142	M Gate and M and A ½
(SC. 2.0)	19.7	27.8	39.4	53.2	71.9	97.1	131	
ASIC								
ASIC usable Mtransistors/cm^2 (auto layout) (1999)	20	28	40	54	73	99	133	M Gate and M and A ½
(SC. 2.0)	19.7	27.8	39.4	53.2	71.9	97.1	131	
ASIC max chip size at production (mm^2) (maximum lithographic field size) (1999)	800	800	800	800	800	800	800	Lithographic Field Size
(SC. 2.0)	800	800	800	800	572	572	572	
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size) (1999)	160	224	320	432	584	800	1064	Market — Performance/ Timing
(SC. 2.0)	157	223	315	426	411	556	751	

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All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**

Table 1j ***High-Performance MPU and ASIC*** *Product Generations and Chip Size Model—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 **[60 NM]**	2011 **[40 NM]**	2014 **[30 NM]**
Logic (Low-volume Microprocessor) High-performance ‡			
Generation at production ‡ (1999)/(SC. 2.0)	—	p11h	—
Functions per chip (million transistors) (1999)	2,494	7,053	19,949
(SC. 2.0)	**1,381**	**3,907**	**11,052**
Chip size at production (mm^2) § (1999)	713	817	937
(SC. 2.0)	**427**	**489**	**561**
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡ (1999)	350	863	2,130
(SC. 2.0)	**324**	**799**	**1,970**
ASIC			
ASIC usable Mtransistors/cm^2 (auto layout) (1999)	328	811	2,000
(SC. 2.0)	**324**	**799**	**1,970**
ASIC maximum chip size at production (mm^2) (maximum lithographic field size) (1999)	800	800	800
(SC. 2.0)	**572**	**572**	**572**
ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size) (1999)	2,624	6,488	16,000
(SC. 2.0)	**1,852**	**4,568**	**11,269**

Since only the 2011 odd-year product generation data column is available in the Long Term table format, interpolated numbers were calculated and included in the 2008 and 2014 node columns. The extended market-need-based product trends for the product generation two-year-cycle years (1999, 2001, 2003, 2005, 2007, 2009, 2011, 2013) are forecast to follow patterns established in Near Term Table 1a.

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.*

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OTHER ORTC TABLES, TWG LINE ITEMS/OWNERS

Table	Line Item	TWG Owner
♦ Table 2a,b	Litho Field Size	Lithography
♦	Wafer Size	Front End Processes, Factory Integration
♦ Table 3a,b	# of Chip I/O's	Test, Design
♦	# of Package Pins/Balls	Test, Assembly & Packaging
♦ Table 4a,b	Chip Pad Pitch	Assembly & Packaging
♦	Cost-Per-Pin	Assembly & Packaging
♦ Table 4c,d	Chip Frequency	Design
♦	Chip-to-Board Freq.	Assembly & Packaging
♦	Max # Wire Levels	Interconnect
♦ Table 5a,b	Electrical Defects	Defect Reduction
♦ Table 6a,b	P.Supply Volt.	Process Integration, Devices, Structures
♦	Max. Power	Design, Process Integration, Devices, Structures
♦ Table 7a,b	Affordable Cost	Economic (Alan Allan acting)
♦	Test Cost	Test

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 2a ~~Chip Size,~~ Lithographic-Field and Wafer-Size Trends—Near Term Years*

(Note: 1999 Lithographic field sizes represent current capability)

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Lithography Field Size							
Maximum lithographic field size — area (mm^2) (1999)	800	800	800	800	800	800	800
Lithography Field Size—area (mm^2) (SC. 2.0)	800	800	800	800	800	572	572
Maximum lithographic field size — length (mm) (1999)	32	32	32	32	32	32	32
Maximum lithographic field size — width (mm) (1999)	25	25	25	25	25	25	25
Lithographic field size (width X length [mm^2]) (SC. 2.0)	25x32	25x32	25x32	25x32	25x32	22x26	22x26
Maximum Substrate Diameter (mm) — High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer (1999)	200	200	300	300	300	300	300
(SC. 2.0)	200	200	300	300	300	300	300

Table 2b ~~Chip Size~~, Lithographic-Field and Wafer Size Trends—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Lithography Field Size			
Maximum lithographic field size—area (mm^2) (1999)	800	800	800
Lithography Field Size—area (mm^2) (SC. 2.0)	572	572	572
Maximum lithographic field size—length (mm) (1999)	32	32	32
Maximum lithographic field size—width (mm) (1999)	25	25	25
Lithographic field size (width X length [mm^2]) (SC. 2)	22x26	22x26	22x26
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)			
Bulk or epitaxial or SOI wafer (1999)	300	300	450
(SC. 2.0)	300	450	450

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001 130 nm	2002 130 nm	2003	2004 90 nm	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90 nm	2005
Number of Chip I/Os (Number of Total Chip Pads) — Maximum							
Total pads—MPU (1999)	2,304	2,560	3,042	3,042	3,042	3,042	3,042
Signal I/O—MPU (1/3 of total pads) (1999)	768	1,024	1,024	1,024	1,024	1,024	1,024
Power and ground pads—MPU (2/3 of total pads) (1999)	1,536	1,536	2,018	2,018	2,018	2,018	2,018
Total pads—ASIC high-performance (1999)	1,400	1,800	2,200	2,600	3,000	3,400	3,800
Signal I/O pads—ASIC high-performance (½ of total pads) (1999)	700	900	1,100	1,300	1,500	1,700	1,900
Power and ground pads—ASIC high-performance (½ of total pads) (1999)	700	900	1,100	1,300	1,500	1,700	1,900
Chip-to-package pads (Peripheral) (1999)	368	397	429	464	501	541	584
Number of Total Package Pins/Balls—Maximum							
Microprocessor/controller, cost-performance (1999)	740	821	912	1,012	1,123	1,247	1,384
ASIC (high-performance) (1999)	1,600	1,792	2,007	2,248	2,518	2,820	3,158

*Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]
Number of Chip I/Os (Number of Total Chip Pads)—Maximum			
Total pads—MPU (1999)	3,840	4,224	4,416
Signal I/O pads—MPU (1/3 of total pads) (1999)	1,280	1,408	1,472
Power and ground pads—MPU (2/3 of total pads) (1999)	2,560	2,816	2,944
Total pads—ASIC high-performance (1999)	4,600	5,400	6,000
Signal I/O pads—ASIC high-performance (½ of total pads) (1999)	2,300	2,700	3,000
Power and ground pads—ASIC high-performance (½ of total pads) (1999)	2,300	2,700	3,000
Chip-to-package pads (Peripheral) (1999)	736	927	1,167
Number of Total Package Pins/Balls—Maximum			
Microprocessor/controller, cost-performance (1999)	1,893	2,589	3,541
ASIC (high-performance) (1999)	4,437	6,234	8,758

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 4a Performance and Package Chips: Pads, Cost~~, and Frequency~~—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Chip Pad Pitch (micron)							
Pad pitch—ball bond (1999)	50	48	47	45	43	42	40
(2000)	50	50	45	35	30	25	20
Pad pitch—wedge bond (1999)	45	43	42	40	39	38	35
(2000)	45	45	40	35	30	25	20
Package cost (cents/pin) (cost-performance)—minimum (1999)	200	200	200	200	182	165	150
(2000)	200	200	175	175	150	150	130
Pad Pitch—area array (handheld, low-cost, harsh) NEW	180	165	150	130	120	110	100
Cost-Per-Pin							
Package cost (cents/pin) (cost-performance)—maximum (1999)	1.90	1.81	1.71	1.63	1.55	1.47	1.40
(2000)	1.90	1.40	1.33	1.26	1.20	1.14	1.08
Package cost (cents/pin) (cost-performance)—minimum (1999)/(2000)	0.90	0.86	0.81	0.77	0.73	0.70	0.66
Package cost (cents/pin) (Memory)—maximum (1999)/(2000)	1.90	1.71	1.54	1.39	1.25	1.12	1.01
Package cost (cents/pin) (Memory)—minimum (1999)/(2000)	0.40	0.38	0.36	0.34	0.33	0.31	0.29

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 4b Performance and Package Chips: Pads, Cost~~, and Frequency~~—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)		2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)		2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Chip Pad Pitch (micron)				
Pad pitch—ball bond	(1999)	40	40	40
	(2000)	20	20	20
Pad Pitch—wedge bond	(1999)	35	35	35
	(2000)	20	20	20
Pad Pitch—area array (cost-performance, high-performance)	(1999)	150	150	150
	(2000)	115	100	80
Pad Pitch—area array (handheld, low-cost, harsh)	NEW	70	50	35
Cost-Per-Pin				
Package cost (cents/pin) (cost-performance)—maximum	(1999)	1.20	1.03	0.88
	(2000)	1.03	0.98	0.93
Package cost (cents/pin) (cost-performance)—minimum	(1999)/(2000)	0.57	0.49	0.42
	(1999)/(2000)	0.74	0.54	0.39
Package cost (cents/pin) (memory)—minimum	(1999)/(2000)	0.25	0.22	0.19

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All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 4c Performance and Package Chips: ~~Pads, Cost, and~~ Frequency, On-Chip Wiring Levels—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001 130 nm	2002 130 nm	2003	2004 90 nm	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90 nm	2005
Chip Frequency (MHz)							
On-chip local clock, (high-performance) (1999)	1,250	1,486	1,767	2,100	2,490	2,952	3,500
(2000)		1620	2,100	2,490	2,952	3,500	4,150
On-chip, across-chip clock (high-performance) (1999)	1,200	1,321	1,454	1,600	1,724	1,857	2,000
(2000)		1,386	1,600	1,724	1,857	2,000	2,155
On-chip, across-chip clock, high-performance ASIC (1999)	500	559	626	700	761	828	900
(2000)		592	700	761	828	900	980
On-chip, across-chip clock (cost-performance) (1999)	600	660	727	800	890	989	1,100
(2000)		693	800	890	989	1,100	1,225
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus) (1999)	1,200	1,321	1,454	1,600	1,724	1,857	2,000
(2000)		1386	1,600	1,724	1,857	2,000	2,155
Chip-to-board (off-chip) speed (high-performance, for peripheral buses) (1999)	480	589	722	885	932	982	1,035
(2000)	480	693	800	862	929	1000	1078
Maximum number wiring levels—maximum (1999)/(2000)	7	7	7	8	8	8	9
Maximum number wiring levels—minimum (1999)/(2000)	6	6	7	7	8	8	8

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All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 4d Performance and Package Chips: ~~Pads, Cost, and~~ Frequency, On-Chip Wiring Levels —Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)		2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)		2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Chip Frequency (MHz)				
On-chip local clock, (high-performance)	(1999)	6,000	10,000	13,500
	(2000)	7,115	11,050	14,920
On-chip, across-chip clock (high-performance)	(1999)	2,500	3,000	3,600
	(2000)	2,655	3,190	3,825
On-chip, across-chip clock (high-performance ASIC)	(1999)	1,200	1,500	1,800
	(2000)	1,295	1,595	1,913
On-chip, across-chip clock (cost-performance)	(1999)	1,400	1,800	2,200
	(2000)	1,522	1,925	2,350
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)	(1999)	2,500	3,000	3,600
	(2000)	2,655	3,190	3,825
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)	(1999)	1,285	1,540	1,800
	(2000)	1328	1595	1913
Maximum number wiring levels—minimum	(1999)/(2000)	9	10	10
Maximum number wiring levels—minimum	(1999)/(2000)	9	9	10

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 5a Electrical Defects—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005
Defect Reduction							
DRAM at production electrical D_0 chip size at 85% yield (d/m^2) § (1999)	1,249	1,193	1,140	1,089	1,040	994	950
(2000)	**1,259**	**1,282**	**1,302**	**1,170**	**1,050**	**942**	**1126**
MPU at production electrical D_0 chip size at 75% yield (d/m^2) §§ (1999)	1,742	1,742	1,742	1,552	1,383	1,321	1,262
(2000)	1,742	1,742	1,742	**1,664**	**1,590**	**1,519**	**1,452**
ASIC first year electrical D_0 at 65% yield (d/m^2) (1999)	562	562	562	562	562	562	562
(2000)	562	562	562	562	**787**	**787**	**787**
Minimum, mask count—maximum (1999)	24	24	24	24	25	25	26
(2000)	24	24	24	**25**	25	**26**	26
Minimum, mask count—minimum (1999)	22	23	23	24	24	24	24
(2000)	22	23	**24**	24	24	24	24

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YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 5b Electrical Defects—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Defect Reduction			
DRAM at production electrical D_0 chip size at 85% yield (d/m^2) § (1999)	828	723	630
(2000)	807	865	660
MPU at production electrical D_0 chip size at 75% yield (d/m^2) §§ (1999)	1,101	960	837
(2000)	1,266	1,104	963
ASIC first year electrical D_0 at 65% yield (d/m^2) (1999)	562	562	562
(2000)	787	787	787
Minimum, mask count—maximum (1999)	28	28	30
(2000)	28	28	30
Minimum, mask count—minimum (1999)	26	28	29
(2000)	26	28	29

D_0—defect density

§ DRAM Model—Cell Factor (design/process improvement) targets are: 1999-2004/8x; 2005-2010/6x; 2011-2016/4x. DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except: 1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4x/5years (2x/2-3yrs); and 2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4x/5years (2x/2-3yrs). InTER-generation chip size growth rate varies to maintain 1 chip per 572mm^2 field at Introduction and 2 chip per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2x bits/chip every 2 years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates can be kept flat through 2001, due to the more aggressive MPU/ASIC half-pitch technology node trend; but beyond 2001, the target growth rate is 1.2× growth every four years. The InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.

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*Table 6a Power Supply and Power Dissipation—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Power Supply Voltage (V)							
Minimum logic V_{dd} (V)—maximum (for maximum performance) (1999)	1.8	1.8	1.5	1.5	1.5	1.2	1.2
(2000)	1.8	1.8	1.5	1.5	1.2	1.2	1.1
Minimum logic V_{dd} (V)—minimum (for lowest power) (1999)	1.5	1.5	1.2	1.2	1.2	0.9	0.9
(2000)	1.5	1.5	1.2	1.2	0.9	0.9	0.8
Maximum Power							
High-performance with heatsink (W)	90	100	115	130	140	150	160
(2000)	90	108	130	140	150	160	170
Battery (W)—(hand-held) (1999)	1.4	1.6	1.7	2.0	2.1	2.3	2.4
(2000)	1.4	1.7	2.0	2.1	2.3	2.4	2.6

*Table 6b Power Supply and Power Dissipation—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (Sc. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Power Supply Voltage (V)			
Minimum logic V_{dd} (V)—maximum (for maximum performance) (1999)	0.9	0.6	0.60
(2000)	0.9	0.6	0.60
Minimum logic V_{dd} (V)—minimum (for lowest power) (1999)	0.6	0.5	0.30
(2000)	0.6	0.5	0.30
Maximum Power			
High-performance with heatsink (W) (1999)	170	174	183
(2000)	171	177	186
Battery (W)—(hand-held) (1999)	2.0	2.2	2.4
(2000)	2.1	2.3	2.5

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*Table 7a Cost—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction (1999)/(SC. 2.0)	42	—	21	—	11	—	5.3
DRAM cost/bit at (packaged microcents) at production § (1999)/(SC. 2.0)	15	—	7.6	—	3.8	—	1.9
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§ (1999)/(SC. 2.0)	1,735	—	868	—	434	—	217
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	1,050	—	525	—	262	—	131
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	245	—	123	—	61	—	31
Cost-Per-Pin (see Table 4) (1999)/(SC. 2.0)	—	—	—	—	—	—	—
Test							
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum (1999)/(SC. 2.0)	8	7	7	6	6	5	5
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum (1999)/(SC. 2.0)	4	3	3	3	3	2	2
Volume tester cost/pin ($K/pin) (cost-performance MPU) (1999)/(SC. 2.0)	8	8	7	7	6	6	5

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Table 7b Cost—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Affordable Cost per Function ++			
DRAM cost/bit (packaged microcents) at samples/introduction (1999)/(SC. 2.0)	—	0.66	—
DRAM cost/bit (packaged microcents) at production § (1999)/(SC. 2.0)	—	0.24	—
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§ (1999)/(SC. 2.0)	—	27	—
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	—	16	—
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	—	3.8	—
Cost-Per-Pin (see Table 4) (1999)/(SC. 2.0)	—	—	—
Test			
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum (1999)/(SC. 2.0)	5	5	5
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum (1999)/(SC. 2.0)	N/A	N/A	N/A
Volume tester cost/pin ($K/pin) (cost-performance MPU) (1999)/(SC. 2.0)	4	2	2

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically 7–8 years after introduction; MPU unit volume life-cycle peak occurs typically after four years, when the next generation processor enters its ramp phase (typically two years after introduction).

§ DRAM Model—Cell Factor (design/process improvement) targets are: 1999-2004/8x; 2005-2010/6x; 2011-2016/4x. DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except: 1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4x/5years (2x/2-3yrs); and 2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4x/5years (2x/2-3yrs). InTER-generation chip size growth rate varies to maintain 1 chip per 572mm^2 field at Introduction and 2 chip per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2x bits/chip every 2 years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

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ITRS TABLE DEFINITIONS/GUIDELINES

Proposal Rev1, 7/11/00

- Technology Requirements Perspective
  - Near-Term Years : First Yr. Ref.+ 6 yrs F'cast (ex. 1999 through 2005), annually
  - Long-Term Years : Following 9 years (ex.: 2008, 2011, and 2014), every 3 years
- Technology Node :
  - General indices of technology development.
  - Approximately 70% of the preceding node, 50% of 2 preceding nodes.
  - Each step represents the creation of significant technology progress
  - Example: DRAM half pitches (2000 ITRS) of 180, 130, 90, 65, 45 and 33nm

  *Year 2000 : Smallest 1/2 pitch among DRAM, ASIC, MPU, etc
- Year of Production:
  - The volume = *10K units (devices)/month. ASICs manufactured by same process technology are granted as same devices
  - Beginning of manufacturing by *a company and another company starts production within 3 months
- Technology Requirements Color:
  - Red : Manufacturable Solutions are NOT known
  - Yellow : Manufacturable Solutions are known
  - White : Manufacturable Solutions exist, and they are being optimized

  *Year 2000 : Red cannot exist in next 3 years (2000, 2001, 2002)**

  *Year 2000 : Yellow cannot exist in next 1 year (2000)

** Exception: Solution NOT known, but does not prevent Production manufacturing

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GLOSSARY – ORTC 2000 UPDATE EDITION

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY
(WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

TECHNOLOGY NODE (nm)—

Each technology node step represents the creation of significant technology progress - approximately 70% of the preceding node, 50% of 2 preceding nodes. Example: DRAM half pitches (2000 ITRS) of 180, 130, 90, 65, 45 and 33 nm. The ground rules of process governed by the smallest feature printed. The half-pitch of first-level interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. For logic, such as microprocessors (MPUs), physical bottom gate length is most representative of the leading-edge technology level required for maximum performance. MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first metal layer and lags behind DRAM half-pitch, which may refer either first layer polysilicon or metal. For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

"MOORE'S LAW"—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend, and key indicator of successful leading-edge semiconductor products and companies, for the past 30 years.

"COST-PER-FUNCTION" MANUFACTURING PRODUCTIVITY IMPROVEMENT DRIVER—In addition to "Moore's Law", there is a historically-based "corollary" to the "law," which suggests that, to be competitive, manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every two years, as suggested by consensus DRAM and MPU models of the 1999 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

"Affordable" Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by ***Functions/Chip.*** Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership (CoO); 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

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DRAM Generation* at *(product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration, Introduction, Sample, Production, Ramp, Peak).

MPU Generation* at (*product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction, Ramp, Peak, Embedded).

Cost-Performance MPU—MPU product optimized for lowest cost by minimizing on-chip SRAM to level-one (L1) cache only (32Kbytes/1999). Logic functionality and L1 cache typically double every 2-year generation. This typically has a 6-year (introduction plus ramp plus peak) computer-market-application life-cycle before being replaced by the next generation cost-performance MPU, then continues on in embedded applications.

High-performance MPU—MPU product optimized for maximum system performance by using a shrunk cost-performance ramp-level MPU core combined with a large (1Mbyte/1999) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two-year generation. Typically has only a 4-year (ramp and peak) life cycle in the relatively low-volume, higher-priced, high-performance computer market. There is no classic "embedded" application for the high-SRAM-content MPU, but that may change as future market demand develops for multiple-MPU-per box internet server and communication processor applications emerge. Those applications will provide increased demand for more cost-effective inTRA generation shrinks of the high-performance MPU, thus extending the life-cycles of future generations.

PRODUCT INTER-GENERATION—Product generation-to-generation targets for periodically increasing on-chip functionality and allowable chip size. The targets are set to maintain "Moore's Law," while preserving economical manufacturability. The 1999 ITRS consensus target for the rate of increase of DRAM and MPU inTER-generation functionality is 2×/chip every two years. The allowable inTER-generational chip size growth for DRAMs was 1.2× every four years in the 1999 ITRS, but is now limited by the maximum available lithography field size and also the cell shrink limitations imposed by the achievable cell area factor targets . For MPUs, the allowable chip size growth is flat through 2001, then grows at 1.2× every four years. To add only 20% in area every four years, while quadrupling functionality, requires an inTER-generation design productivity which further reduces chip size by an additional minus 7–8 % per year. This design-related productivity reduction is in addition to the basic lithography-provided area reduction of -11% per year.

PRODUCT INTRA-GENERATION—Within a given product generation. The consensus-based targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS consensus targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node. For DRAM, this reduction of minus 50% occurs every three years, or minus 37% every two years. For MPU, the 50% reduction occurs every two years through 2001, then slows to minus 37% per two years (same as DRAM).

YEAR OF DEMONSTRATION—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three years at the leading-edge process technology node, typically 2–3 years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure

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techniques that are feasible only for very small quantities of laboratory samples.
Example: 1997/ISSCC/1Gb DRAM.

YEAR OF INTRODUCTION (DRAM)—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, DRAM products will be introduced at 2× functionality per chip every two years. In addition, manufacturers will delay introduction until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to 1.2× every 4 years, or approximately 1.1× every 2-year generation **in the 1999 ITRS, but is now limited by the maximum available lithography field size and also the cell shrink limitations imposed by the achievable cell area factor targets** Example: 1999/1Gb DRAM.

YEAR OF PRODUCTION (DRAM)—Year in which leading chip manufacturers begin shipping volume quantities (**10K/month**) of product manufactured with qualified production tooling and processes **and is followed within three months by a second manufacturer**. This product typically contains one-fourth (1/4) the bits per chip of the introduction-level generation design, from which it is "cut-down." Example: 1999/256Mb DRAM.

YEAR OF INTRODUCTION (MPU)—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. The introduction cost-performance MPU may be combined in a multi-chip module, along with L2 cache, in low-volume computer applications which demand high performance.

YEAR OF PRODUCTION (MPU)— Year in which leading chip manufacturers begin shipping volume quantities (**10K/month**) of product manufactured with qualified production tooling and processes **and is followed within three months by a second manufacturer**. As demand increases, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity. Lower-volume, high-performance MPUs are also ramping concurrently as its co-existing cost-performance MPU core, but the L2 cache is now included on-chip but with twice the memory as its high-performance-generation predecessor.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs, application-specific integrated circuits [ASICs]) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS analyst consensus models).

Functions/cm^2—The density of functions in a given square centimeter = ***Functions/Chip*** on a single monolithic chip divided by the ***Chip Size***. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. Most typical ASIC designs will be slightly less dense than the high-performance MPUs, which are mostly SRAM.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe

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YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 55% at the production level, and less than 50% at the ramp level).

DRAM Cell Area (μm^2)—The measure of the maximum allowable DRAM memory bit cell area specified by the requirement to meet the target chip size and cell array area percentage requirements. May also be expressed as the cell area factor – number of equivalent units of area of a square of the DRAM half-pitch. Minimizing the area for the cell is in conflict with the desire to maximize the capacitance storage capability of the continuously shrinking cell. This creates a conflict between the technical feasibility of the cell area required to meet the economic constraints of the maximum allowable chip size.

DRAM Cell Area Factor—The measure of the maximum allowable DRAM memory bit cell area, expressed as the number of equivalent units of area of a square of the DRAM half-pitch.

Example: 1999: square of the half-pitch = $(180\ nm)^2 = .032\ \mu m^2$; maximum cell area for 1Gb DRAM to be < 70% of total chip area = $0.26\ \mu m^2$; therefore, the maximum cell area factor = 0.26/0.32 = 8. The cell factor is also often expressed by equivalent aspect ratios of the half-pitch units (2×4 = 8, 2×3 = 6, 2×2=4, 1.6×1.6=2.5, etc.).

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os – Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os – Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package cost (cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

Chip Frequency (MHz)

On-chip, local clock, high-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

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On-chip, across-chip clock—On-chip clock frequency of microprocessors and ASICs for interconnect signals that run across the full width of the chip (Typically, this is lower than the localized clock performance due to capacitance loading of the long cross-chip interconnect.).

Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)—Maximum signal I/O frequency to specialized board reduced-width, multiplexed buses.

Chip-to-board (off-chip) speed (high-performance, peripheral buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

Other Attributes

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. **The specification represents the mimimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.**

Maximum Number Of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration Technology Working Group, are based on the first 20K wafer-starts-per-month manufacturing facility, versus the first-pilot-line timing target of the 1997 NTRS.

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ELECTRICAL DESIGN AND TEST METRICS

Power Supply Voltage (V)

Minimum Logic V_{dd}— Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power

High-performance with heat sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

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FOLDER 2

International Technology Roadmap for Semiconductors

2000 Update

Process Integration, Devices, and Structures

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PROCESS INTEGRATION, DEVICES, & STRUCTURES

SUMMARY

Since the publication of the 1999 ITRS, it has become clear that some of the forecast trends were too conservative. In particular, both the MPU transistor gate length scaling and the technology node timing keyed mainly to the DRAM half pitch are proceeding faster than predicted. Also, the ASIC gate length scaling is no longer trailing the MPU scaling. In response, the PIDS TWG has accelerated the scaling of MPU transistor gate length and associated specifications in the 2000 Roadmap update and has set the ASIC gate length equal to the MPU gate length at all nodes. The changes are in Table 28a, Memory and Logic Technology Requirements—Near Term. In the table, for each year through 2001, the MPU gate length is moved forward by one year in the 2000 update compared to the 1999 ITRS, but the gate lengths are left unchanged from 2002 on. Other key specifications such as equivalent T_{ox}, V_{dd}, maximum I_{off}, etc., are also moved forward by one year, following the gate length. The acceleration is halted with the year 2002 because the TWG is concerned about the "red brick wall" in equivalent T_{ox} that appears in 2005 in the 1999 ITRS. The equivalent T_{ox} is small enough in 2005 to perhaps require high K material for the gate dielectric to keep the gate leakage within acceptable limits, but the industry has no solution in hand. Furthermore, prospects of such a solution by 2005 are highly uncertain. Moving the gate length and thus the equivalent T_{ox} forward by one year for the 2002 node and beyond could result in requiring high K gate dielectric earlier than 2005, which the TWG found unrealistic. The issue of accelerating the gate length and other parameters for 2002 and beyond requires careful analysis of scaling issues.

Other changes are relatively minor, to correct minor errors, update several values in the tables, and clarify explanations in the notes. In Table 28, the changes include an improved definition of the gate delay metric in Rows 9 and 13, making the S/D extension junction depth values and colors in Row 16 the same as those in the Front End Processing Table 34, and recognition of special difficulty, starting in 2002, in meeting the gate leakage requirements for low power transistors (see Note 11). In Table 29, many of the values have been updated.

Currently, there is not a consensus amongst the TWGs and the IRC on the acceleration in scaling trends for DRAM half pitch and MPU/ASIC gate length, especially in 2002 and beyond. It is vitally important to come to consensus early in 2001 regarding the appropriate scaling trend to use. A major challenge for the PIDS TWG will be to then analyze in detail the resulting impact on device and DRAM scaling and characteristics, including especially the accelerated development and integration of high K gate dielectric. Another key challenge will be to work with the FEP TWG to add flash and FERAM characteristics to the tables, and to expand the logic low power requirements. Other key challenges will be to work with the Design TWG to resolve linked device, circuit, and system issues, such as the impact of gate leakage on logic circuitry, the impact of V_{dd} and I_{off} specifications on circuit and system power, etc. Finally, updating and improving the novel devices table will be a major focus.

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YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

2000 UPDATE TABLES

MEMORY AND LOGIC

*Table 28a Memory and Logic Technology Requirements—Near Term***

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
1	DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	
2	MPU/ASIC Physical Gate Length	120	100	90	85-90	80	70	65	
3	MPU / ASIC ½pitch (nm)	230	210	180	160	145	130	115	
4									
5	Minimum logic V_{dd} (V) (desktop)	1.5–1.8	1.2-1.5	1.2–1.5	1.2–1.5	1.2–1.5	0.9–1.2	0.9–1.2	
6	T_{ox} equivalent (nm)	1.9–2.5	1.5-1.9	1.5–1.9	1.5–1.9	1.5–1.9	1.2–1.5	1.0–1.5	M GATE
7	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] high-performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	M GATE
8	Maximum I_{off} at 25 °C (nA/µm) (For minimum L device) high performance	7	8	10	10	13	16	20	M GATE
9	Gate delay metric CV/I (ps) high-performance	12.5	11.4	10.3	9.7	9.1	8.1	7.5	
10	Percent static power reduction necessary due to innovative circuit/system design	0	48	55	55	71	77	81	M GATE M & A ½
11	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] low power	490/230	490/230	490/230	490/230	490/230	490/230	490/230	A GATE
12	Maximum I_{off} at 25 °C (pA/µm) (For minimum L device) low power	7	8	10	10	13	16	20	A GATE
13	Gate delay metric CV/I (ps) low power	20.9	17.6	15.9	15.0	14.1	12.9	11.6	
14	Percent static power reduction necessary due to innovative circuit/system design	0	55	65	65	80	85	88	A GATE M & A ½
15	V_t 3σ variation (±mV) (for nominal L_g device)	50	42	42	42	42	33	33	M GATE
16	S/D extension junction depth, nominal (nm)	36–60	30–50	25–43	25–43	24–40	20-35	20-33	M GATE

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All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 28a Memory and Logic Technology Requirements—Near Term (continued)***

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
1	DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	
2	MPU/ASIC Physical Gate Length	120	100	90	85-90	80	70	65	
3	MPU / ASIC ½pitch (nm)	230	210	180	160	145	130	115	
17	Gate sheet resistance (Ω/sq) at minimum dimension	4–6	4–6	4–6	4–6	4–6	4–6	4–6	M Gate
18	Interconnect levels	6–7	6–7	7	7–8	8	8	8–9	M & A ½
19	Short wire minimum pitch (nm)	360-460	330-420	300-360	260-320	240-290	220–260	200–230	M & A ½, D ½
20	Maximum wire length for local levels, Lm (µm)	2243	2036	1828	1621	1468	1315	1162	M & A ½
21	DRAM cell size (µm²)	0.26	0.22	0.18	0.10	0.08	0.065	0.044	D ½
22	DRAM cell dielectric T_{ox} equivalent (nm)	3	2.40	1.80	0.95	0.80	0.65	0.45	
23	DRAM retention time (ms)	250	250	250	250	250	250	250–500	
24	DRAM soft error rate (fits)	1000	1000	1000	1000	1000	1000	1000	
25	Nonvolatile data retention (Years)	10	10	10	10	10	10	10	
26	NOR cell size (µm²)	0.34	0.29	0.24	0.17	0.15	0.13	0.1	M & A ½
27	+/- V_{pp} (V)	8–10	8–10	8–9.5	8–9.5	8–9.5	7–9	7–9	
28	Tunnel oxide (nm)	8–10	8–10	8–9.5	8–9.5	8–9.5	8–9	8–9	
29	NVM endurance (erase/write cycles)	100K	100K	100K	100K	100K	100K	100K	
30	ESD protection voltage (V/µm)	7.5	7.5	10.5	10.5	10.5	12	12	
31	(V/µm²)	2.5	2.5	3.0	3.0	3.0	3.5–4.0	3.5–4.0	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

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YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 28b Memory and Logic Technology Requirements—Long Term**

	Year Technology Node	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
[1]	DRAM ½ Pitch (nm)	70	50	35	
[2]	MPU Gate Length (nm)	45	32	22	
[3]	MPU / ASIC ½ Pitch (nm)	80	55	40	
[4]	ASIC Gate Length (nm)	70	50	35	
[5]	Minimum logic V_{dd} (V) (desktop)	0.6–0.9	0.5–0.6	0.3–0.6	M Gate
[6]	T_{ox} equivalent (nm)	0.8–1.2	0.6–0.8	0.5–0.6	M Gate
[7]	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] high performance	750/350	750/350	750/350	M Gate
[8]	Maximum I_{off} at 25 °C (nA/µm) (For minimum L device) high-performance	40	80	160	M Gate
[9]	Gate delay metric CV/I (ps) high-performance	4.9	3.4	3.0	
[10]	Percent static power reduction necessary due to innovative circuit/system design	91	97	98	M Gate M & A ½
[11]	Nominal I_{on} at 25 °C (µA/µm) [NMOS/PMOS] low power	490/230	490/230	490/230	A Gate
[12]	Maximum I_{off} at 25 °C (pA/µm) (For minimum L device) low power	40	80	160	A Gate
[13]	Gate delay metric CV/I (ps) low power	7.4	5.7	2.8	
[14]	Percent static power reduction necessary due to innovative circuit/system design	95	98	99	A Gate M & A ½
[15]	V_T 3σ variation (±mV) (for nominal L_g device)	25	17	17	M Gate
[16]	S/D extension junction depth, nominal (nm)	16–26	11–19	8–13	
[17]	Gate sheet resistance (Ω/sq) at minimum dimension	4–6	4–6	4–6	M Gate

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*Table 28b Memory and Logic Technology Requirements—Long Term (continued)***

	Year Technology Node	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
[1]	DRAM ½ Pitch (nm)	70	50	35	
[2]	MPU Gate Length (nm)	45	32	22	
[3]	MPU / ASIC ½ Pitch (nm)	80	55	40	
[4]	ASIC Gate Length (nm)	70	50	35	
[18]	Interconnect levels	9	9–10	10	M & A ½
[19]	Short wire *minimum* pitch (µm)	140-160	100-110	70-80	M & A ½, D ½
[20]	Maximum wire length *for local levels*, Lm (µm)	697	325	201	M & A ½
[21]	DRAM cell size (µm²)	0.018	0.0075	0.0031	D ½
[22]	Cell dielectric T_{ox} equivalent (nm)	0.15	0.06	0.043	
[23]	*DRAM retention time* (ms)	250–500	250–500	250–500	
[24]	Soft error rate (fits)	1000	1000	1000	
[25]	Nonvolatile data retention (*Years*)	10	10	0.1–10	
[26]	NOR cell size (µm²)	0.05	0.025	0.012	M & A ½
[27]	+/- V_{pp} (*V*)	7–8.5	6.5–8.5		
[28]	Tunnel oxide (nm)	7.5–8.5	2–8	2–7	
[29]	NVM endurance (erase/write cycles)	100K	0.1–1M	0.1–10M	
[30]	ESD protection voltage (V/µm)	13.5	15	17.5	
[31]	(V/µm²)	4.5–5.0	5.5–6.0	7.5–10	

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

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Notes for Table 28a and b Memory and Logic Requirements

General Notes:

[A] *The power supply voltage control is ±10%.*

[B] *Control of L_{gate} is ±10% and ±20% for L_{eff}*

[C] *The total series resistance of the S/D is expected to be <10% of the channel "ON" resistance, $R_{on}=V_{dd}/I_{on}D$. Flash products will not make use of a technology node at the time it is introduced for microprocessor or DRAM usage.*

Explanatory Notes for each row of Table 28a and b:

[1] ***These DRAM half pitch numbers are unchanged from the 1999 ITRS. However, developments since the publication of the 1999 ITRS strongly suggest that the scaling trend here is too conservative. A proposal has been made to accelerate this trend (see ORTC tables), and this proposal will be carefully evaluated and its impact analyzed in preparing the 2001 ITRS.***

[2] ***This is the final, as-etched length at the bottom of the gate electrode. These numbers have been changed from those in the 1999 ITRS because developments since the publication of that document strongly suggest that scaling is proceeding faster than expected. Furthermore, the ASIC gate length scaling no longer trails the MPU scaling, so the ASIC gate length has been set equal to the MPU gate length. In this updated table, for each year through 2001 the gate length value is moved to the left by one year (i.e., one year earlier) compared to the 1999 ITRS, but the gate length values are left unchanged from 2002 on. Other key specifications such as equivalent T_{ox}, V_{dd}, maximum I_{off}, nominal I_{on}, etc., are linked to the gate length, and hence are also moved to the left by one year through 2001 and left unchanged for 2002 and beyond.***

The accelerated scaling is not extended beyond 2001 mainly because of concerns about the equivalent T_{ox} specification. In the 1999 ITRS, the equivalent T_{ox} is small enough in 2005 to perhaps require high K material for the gate dielectric in order to keep the gate leakage within acceptable limits. However, the industry has no solution in hand for such a high K gate dielectric, and prospects of implementing such a solution in production by 2005 are highly uncertain. Accelerated scaling of the gate length and thus the equivalent T_{ox} for 2002 and beyond could result in requiring high K gate dielectric earlier than 2005, which is unrealistic. There are proposals (see the ORTC tables) for accelerated scaling of the gate length in 2002 and beyond, and these will be evaluated in preparing the 2001 ITRS. Such accelerated scaling will require re-evaluation of the equivalent T_{ox} scaling and resolution of difficult overall transistor scaling, CD control, and other issues

[3] *From ORTC table*

[4] ***Row 4 was for the ASIC Gate Length in the 1999 ITRS. However, as explained in Note 2 above, the ASIC gate length scaling has matched the MPU gate length scaling, so ASIC gate length has been set equal to the MPU gate length in the 2000 update. Hence, for the 2000 ITRS, Row 2 covers both MPU and ASIC gate length, and Row 4 is unnecessary.***

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YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

[5] Power supply voltage is based on controlling the active power dissipation (see linked spreadsheet) and keeping the field in the gate dielectric at reasonable levels per reliability concerns. Generally, the higher values in the range will be used for high-performance applications, while the lower values in the range will be used for low-power applications.

[6] This is the equivalent effective physical SiO_2 thickness. (Note that the electrically determined oxide thickness from C-V measurements would be larger than the thickness in this line because of polysilicon depletion and quantum effects.) **The values here are the same as those in Table 34 in the Front End Processes chapter.** Generally, as with V_{dd}, the higher values in the range will be used for high-performance applications, while the lower values in the range will be used for low-power applications. For the 180 through the 110 nm nodes, the range of equivalent T_{ox} is chosen to keep $V_{dd}/T_{ox} \leq 8$ MV/cm because of oxide reliability concerns, where V_{dd}/T_{ox} is a metric for the electric field in the oxide. At the 100 nm technology node, there is a distinct likelihood that high κ materials other than SiO_2 or oxynitride will be used for the gate dielectric. For such materials, the gate leakage current is much smaller than for oxide dielectric with the same equivalent Tox, allowing smaller Tox and hence higher I_{on} for the high κ case. Also, the $V_{dd}/T_{ox} \leq 8$ MV/cm requirement may not hold for the high κ materials, and hence from a reliability point of view, T_{ox} can be scaled further for these materials. Thus, at the 100 nm node, the wide range of 1.0–1.5 nm for equivalent T_{ox} comprehends the uncertainty of what dielectric material will be used, with the high end of the range appropriate for SiO_2 or oxynitride and the very bottom end of the range appropriate for high κ materials. Beyond the 100 node, the use of high κ material for the gate dielectric becomes much more likely, and the $V_{dd}/T_{ox} \leq 8$ MV/cm requirement is no longer followed

[7] The device I_{on} value is expected to remain relatively constant for succeeding technology generations. **The white, yellow, and red coloring here follows that of T_{ox} in Line 6.**

[8] The device I_{off} value is projected to increase with successive technology generations to maintain I_{on} constant per Line 7. I_{off} is measured with $V_s=V_g=V_{substrate}=0$ and $V_d=V_{dd}$. I_{off} is the difference between the drain current and the gate (leakage) current (I_{off} is the sum of the subthreshold current [the current in the source lead] and the junction leakage current [the current in the substrate lead]). The requirements on the gate leakage current are listed in the Front End Processes (FEP) chapter in Table 34. **This row is colored white throughout because through adjustment of the threshold voltage implant (and perhaps use of other techniques such as optimized halo implants), meeting the I_{off} specification should be achievable. What will be difficult is to simultaneously meet the I_{off} requirement and other key device requirements, especially for I_{on}, at the later technology nodes. The coloring of Row 7 captures this difficulty for I_{on}.**

[9] **The gate delay metric for high-performance devices is calculated using the approach in Taur and Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998, pp. 228 - 230. We assume a CMOS inverter with Wp = (Ion,n/Ion,p) * Wn = (750/350) * Wn, where Wn and Wp are the widths of, respectively, the NMOS and PMOS transistors, and the inverter is driven by an ideal square wave at its input. Also, the inverter's load is an identical inverter. Under those circumstances, the CV/I gate delay metric equals the switching delay, τ, in Taur and Ning, where τ = (τn + τp)/2, and τn and τp are defined, respectively, in Equations 5.3 and 5.4 in Taur and Ning. The highest values of V_{dd} from Row 5 are used in this analysis, along with the largest T_{ox} equivalent values from Row 6. It is assumed that the channel width scales with the channel length. The MPU gate length is used for L. Since the gate delay metric is only a calculated number using transistor characteristics such as T_{ox} V_{dd}, etc., the coloring here is white.**

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All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

[10] For each technology node, maximum system-imposed limits for total chip leakage current, $I_{L,SYS}$, were estimated by assuming a static power dissipation limit of 10% of the maximum heat-sink limit, and dividing this static power dissipation by V_{dd}. Given the projected device I_{off} value from Line 8, the total projected static leakage current for the chip was calculated based on the total number of transistors and an assumed W/L ratio of 3. This projected chip static leakage current was increased by a factor of 100 to account for the leakage current increase due to device self heating (T=100°C). If this projected T=100°C chip static leakage current value is greater than $I_{L,SYS}$, then the excess percentage of static power dissipation is listed in Line 9. This excess must be eliminated through innovative circuit or system design techniques such as using dynamic or multi-V_t techniques to reduce the effective I_{off} of the chip or by turning off sections of the chip temporarily. System values of the heat-sink dissipation limit, the power-supply voltage, chip size and transistor density were obtained from the ORTC tables.

[11] For successive technology generations, the device I_{on} value is expected to remain relatively constant. The low-power device performance is a calculated percentage of the high-performance I_{on} value; this calculated value takes into account the loss in current drive due to the higher required threshold voltage necessary in order to satisfy more stringent I_{off} requirements. **The color is yellow at the 130 nm node (2002) because of difficulty in meeting the gate leakage specification of ≤10 pA/μm at 100 °C, and the color is red for 2004 and beyond because of the greater difficulty of meeting the gate leakage specifications with the increasingly thin equivalent T_{ox} values at those nodes.**

[12] The device I_{off} value is set to three orders of magnitude less than the I_{off} for the high-performance chips (Line 8), and is similarly projected to increase with succeeding technology generations. I_{off} is the difference between the drain current and the gate (leakage) current (I_{off} is the sum of the subthreshold current [the current in the source lead] and the junction leakage current [the current in the substrate lead]). The requirements on the gate leakage current are listed in the Front End Processes chapter in Table 34.

[13] **The gate delay metric for the low-power devices is calculated using the approach in Yuan and Taur, similarly to calculating the gate delay metric for high-performance devices (see Note 9 above). The only difference from the high-performance case is that the smallest values of V_{dd} from Row 5 and the smallest T_{ox} equivalent values from Row 6 are used in the analysis, and the I_{on} values are those for low-power devices.**

[14] For each technology node, maximum system-imposed limits for total chip leakage current, $I_{L,SYS}$, were estimated by assuming a static power dissipation limit of 10% of the maximum chip power dissipation, and dividing this static power dissipation by V_{dd}. A reasonable value for the maximum dissipation for high density, battery-operated chips is 100 μW, in order to preserve battery life. Given the projected device I_{off} value from Line 11, the total projected static leakage current for the chip was calculated based on the total number of transistors and an assumed W/L ratio of 3. If this projected chip static leakage current value is greater than $I_{L,SYS}$, then the excess percentage of static power dissipation is listed in Line 12. This excess must be eliminated through innovative circuit or system design techniques such as using dynamic or multi-V_t techniques to reduce the effective I_{off} of the chip or by turning off sections of the chip temporarily.

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

[15] The V_t 3-sigma variation was scaled proportionately with the reduction in the midrange power supply voltage. **The V_t 3-sigma variation here is the total statistical variation in V_t, including the effects of statistical variation in T_{ox}, L_g, implant dose and energy, etc.**

[16] A range of junction depths can be used depending on the drain and channel engineering used (such as pocket implants versus shallow drain extensions). **The values and the white, yellow, and red coloring here are the same as those in Table 34 in the Front End Processes chapter.**

[17] Difficult to obtain gate sheet resistance targets with silicide at 70 nm and beyond.

[18] The number of interconnect levels is driven by high-performance microprocessor.

[19] The short wire pitch is equal to two times the half pitch.

[20] For the metal layers with the smallest pitch, this is the calculated value of the maximum wire length for the propagation delay to be $0.9*f_{max,\ local}$, where $f_{max,\ local}$ is the maximum local frequency from the ORTC tables. The gates are three-input NAND gates, with a Wn/L ratio of 5. (The formula used in calculating the delay as a function of maximum wire length is in P.D. Fisher, et al.[6]) Also refer to the linked spreadsheet.

[21] The cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Processes chapter Table 34b. The capacity and chip size numbers used by FEP are from the Overall Roadmap Technology Characteristics (ORTC) Tables 1a and 1b, and reflect the "generation at introduction" option. (This is for the DRAM chip that is just being introduced and sampled, having the highest DRAM capacity and most aggressive but still quite large chip size. Note that the "Generation at production" option in the ORTC tables has one quarter the DRAM capacity of the generation at introduction option, and correspondingly smaller chip size that allows the chip price to be affordable.) Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled very aggressively. The difficulty will lie in reducing the value of the cell size factor, a, where a = cell size/F2 and F is the DRAM half pitch. The required values for a are 8 for the 180 nm node, 6 for the 130 nm node, and 4.4 for the 100 nm node. a = 8 is probably achievable with current techniques, but a =6 will require innovative solutions, as indicated by the yellow coloring of the 130 nm node for this line, while a=4.4 has no known solution, as indicated by the red coloring of the 100 nm node and beyond.

[6] P. D. Fisher, et al., "The Test of Time," *IEEE Circuits and Devices Magazine*, vol. 14, pp. 37–44 (March 1998).

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2000 UPDATE										
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YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

[22] Cell dielectric T_{ox} equivalent thickness is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Processes chapter, Table 34b. The capacity and chip size numbers used by FEP are from the Overall Roadmap Technology Characteristics (ORTC) Tables 1a and 1b, and reflect the "generation at introduction" option. (This is for the DRAM chip that is just being introduced and sampled, having the highest DRAM capacity and most aggressive but still quite large chip size. Note that the "generation at production" option in the ORTC tables has one quarter the DRAM capacity of the Generation at introduction option, and correspondingly smaller chip size that allows the chip price to be affordable.) Since the FEP DRAM capacity and chip size numbers are quite aggressive, the equivalent T_{ox} must also be scaled very aggressively. For the 180 nm–150 nm nodes, the dielectric is based on ONO/Ta_2O_5. For the 130 nm node and beyond, breakthroughs are needed to utilize MIM structures and eventually BST, while for the 70 nm node and beyond, there are no known solutions. The actual T_{ox} equivalent requirement for each node depends on factors such as area enhancement (by height and 3D structures), film leakage, and contact formation. Trench capacitors may have different requirements for the cell dielectric material, but the trends should be valid..

[23] Retention time is the minimum time without refreshing a row that the data from memory is still sensed correctly at 85°C. This is the measure of the combined interaction of device leakage, signal strength, and the sense amplifier circuit's sensitivity. This requirement can vary with operating frequency and temperature, and also depending on the application specifics.

[24] Soft error: This is a typical FIT rate and can vary with cycle time and other quality/reliability testing conditions.

[25] Retention requirements will remain at ten years in the near term, but future alternative technologies will exploit retention-endurance tradeoffs.

[26] The need for high electric fields will complicate scaling and eventually force use of alternative NVM technology.

[27] The meaning of V_{pp} has become uncertain because it is no longer an external supply. In this table it is intended to indicate the highest voltage relative to ground seen in the cell array.

[28] Tunnel oxides must be thin enough to allow ease of program/erase, but thick enough to assure retention. Scaling difficulties will force consideration of alternative cell structures.

[29] Endurance of 100K cycles is a minimum need, and in emerging nodes the possibility of higher endurance and lower retention will be explored.

[30] ESD V/μm in terms of NMOS capability per micron width, **based on the Human Body Model**. Particularly critical in NMOS ESD circuits and self-protected circuits.

[31] ESD $V/\mu m^2$ in terms of protection circuit effectiveness per unit area of the protection circuit including guard ring, **based on the Human Body Model**.

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2000 UPDATE										
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YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

ANALOG, MIXED-SIGNAL, AND RF

*Table 29a Analog, Mixed-signal, and RF Technology Requirements—Near Term***

[1]	YEAR TECHNOLOGY NODE		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
	DRAM ½ Pitch (nm)		180	165	150	130	120	110	100	D
	MPU Gate Length (nm)		140	120	100	85	80	70	65	M Gate
	MPU/ASIC ½ Pitch (nm)		230	210	180	160	145	130	115	M & A
	ASIC Gate Length (nm)		180	165	150	130	120	110	100	A Gate
[2]	Minimum Digital Supply Voltage (V)		1.8–1.5		1.5–1.2			1.2–0.9		M Gate
[3]	Minimum Analog Supply Voltage (V)		3.3–2.5	3.3–1.8			2.5–1.8			
[4]	RF Frequency (GHz)		0.9–2.5	0.9–10						
[5]	Analog Frequency (GHz)		<0.1	0.1–5						
[6]	RF Transistor	Current (μA)	100	100	100	100	75	75	75	M Gate
[7]		f_{max} (GHz)	25	28	32	35	40	45	50	
[8]		f_τ (GHz)	20	20	25	30	30	35	40	
[9]		Noise figure (dB)	1.5	1.5	1.5	1.5	1.2	1.2	1.2	
[10]		1/f Noise (V^2-μm^2)	1×10^{-11}	1×10^{-11}	1×10^{-11}	5×10^{-12}	5×10^{-12}	5×10^{-12}	1×10^{-10}	
[11]	Analog	Current (μA)	75	70	65	60	55	50	50	
[12]		1/f Noise (V^2-μm^2)	1×10^{-11}	1×10^{-11}	1×10^{-11}	5×10^{-12}	5×10^{-12}	5×10^{-12}	2×10^{-10}	
[13]		Gate oxide leakage (A/cm^2)	—	—	—	—	—	—	1×10^{-10}	
[14]		Current matching ($\Delta\% \pm 3\sigma$)	≤1	≤1	≤1	≤1	≤1	≤1	≤1	
[15]	RF Coupling	Density ($fF/\mu m^2$)	1	1.2	1.4	1.5	1.7	1.9	2	
[16]		Q	≥15	≥18	≥22	≥25	≥27	≥29	≥30	
[17]	Filter	Density ($fF/\mu m^2$)	2.5	2.8	3.2	3.5	3.7	3.8	4	
[18]		Matching ($\Delta\% \pm 3\sigma$)	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	
[19]	RF Bypass	Density ($fF/\mu m^2$)	5	6	7	7.5	8	9	10	
[20]		Linearity (ppm/V)	≤1000	≤1000	≤1000	≤1000	≤1000	≤1000	≤1000	
[21]		Q	≥15	≥18	≥22	≥25	≥27	≥29	≥30	

*** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.*

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2000 UPDATE										
YEAR OF PRODUCTION / TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION / TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 29a Analog, Mixed-signal, and RF Technology Requirements—Near Term (continued)***

[1]	YEAR / TECHNOLOGY NODE		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
	DRAM ½ Pitch (nm)		180	165	150	130	120	110	100	D
	MPU Gate Length (nm)		140	120	100	85	80	70	65	M Gate
	MPU/ASIC ½ Pitch (nm)		230	210	180	160	145	130	115	M & A
	ASIC Gate Length (nm)		180	165	150	130	120	110	100	A Gate
[22]	Analog	Density (fF/μm^2)	1	1	1	1.5	1.5	1.5	2	
[23]		Linearity (ppm/V)	≤100	≤100	≤100	≤100	≤100	≤100	≤100	
[24]		Leakage (pA/pF-V)	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	
[25]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	
[26]	RF Resonator	Q	<50	<50	<50	50–1000				
[27]	Analog	Matching (Δ% ±3σ)	≤1	≤1	≤1	≤0.1	≤0.1	≤0.1	≤0.1	
[28]		1/f Noise (A^2-μm^2)	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	1×10^{-18}	
[29]		TC (ppm/°C)	≤100	≤100	≤100	≤10	≤10	≤10	≤10	
[30]	Inductor	Q	≥15	≥15	≥25	≥25	≥25	≥25	≥30	
[31]	Signal Isolation	S_{21} (dB)	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-120	
[32]	Benchmark	Gain (dB)	≥20	≥20	≥20	≥20	≥20	≥20	≥20	
[33]		IIP3 (dBm)	-4	-4	-4	-3	-3	-3	-2.5	
[34]		Noise figure (dB)	1.5	1.5	1.5	1.3	1.3	1.3	1.2	
[35]		Noise (dB)	4	4	4	3.5	3.5	3.5	3	
[36]		Resolution (Bits)	8–14			8–14				

Solutions Exist *Solutions Being Pursued* *No Known Solutions*

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

*Table 29b Analog, Mixed-signal, and RF Technology Requirements—Long Term***

			2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
[1]	YEAR TECHNOLOGY NODE					
	DRAM ½ Pitch (nm)		70	50	35	D
	MPU Gate Length (nm)		45	32	22	M Gate
	MPU / ASIC ½ Pitch (nm)		80	55	40	M & A
	ASIC Gate Length (nm)		70	50	35	A Gate
[2]	Minimum Digital Supply Voltage (V)		0.9–0.6	0.6–0.5	0.5–0.3	M Gate
[3]	Minimum Analog Supply Voltage (V)		1.8–1.5		1.5	
[4]	RF Frequency (GHz)		0.9–10	0.9–100		
[5]	Analog Frequency (GHz)		0.1–5	0.1–10		
[6]	RF Transistor	Current (μA)	50	50	50	M Gate
[7]		f_{max} (GHz)	60	150	175	
[8]		f_τ (GHz)	50	120	140	
[9]		Noise figure (dB)	≤1	≤1	≤1	
[10]		1/f Noise (V^2-μm^2)	5×10^{-11}	2×10^{-11}	1×10^{-11}	
[11]	Analog	Current (μA)	40	30	20	
[12]		1/f Noise (V^2-μm^2)	1×10^{-10}	1×10^{-10}	5×10^{-11}	
[13]		Gate oxide leakage (A/cm^2)	1×10^{-08}	1×10^{-08}	1×10^{-05}	
[14]		Current matching (Δ% ±3σ)	≤1	≤1	≤1	
[15]	RF Coupling	Density ($fF/\mu m^2$)	3	4	6	
[16]		Q	≥35	≥40	≥40	
[17]	Filter	Density ($fF/\mu m^2$)	5	7	10	
[18]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	
[19]	RF Bypass	Density ($fF/\mu m^2$)	15	20	30	
[20]		Linearity (ppm/V)	≤1000	≤1000	≤1000	
[21]		Q	≥35	≥40	≥40	

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2000 UPDATE										
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YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 29b Analog, Mixed-signal, and RF Technology Requirements—Long Term (continued)**

[1]	YEAR TECHNOLOGY NODE		2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
	DRAM ½ Pitch (nm)		70	50	35	D
	MPU Gate Length (nm)		45	32	22	M Gate
	MPU / ASIC ½ Pitch (nm)		80	55	40	M & A
	ASIC Gate Length (nm)		70	50	35	A Gate
[22]	Analog	Density (fF/μm^2)	3	4	6	
[23]		Linearity (ppm/V)	≤100	≤50	≤50	
[24]		Leakage (pA/pF-V)	≤0.001	≤0.001	≤0.001	
[25]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	
[26]	RF	Q	50–1000		≥1000	
[27]	Analog	Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.01	
[28]		1/f noise (A^2-μm^2)	1×10^{-18}	1×10^{-18}	1×10^{18}	
[29]		TC (ppm/°C)	≤10	≤10	≤1	
[30]	Inductor	Q	≥50	≥75	≥75	
[31]	Signal Isolation	S_{21} (dB)	≤-120	≤-120	≤-120	
[32]	Benchmark	Gain (dB)	≥20	≥20	≥20	
[33]		IIP3 (dBm)	-1.5	-1	-1	
[34]		Noise figure (dB)	1.0	1.0	1.0	
[35]		Noise (dB)	2.5	2	2	
[36]		Resolution (Bits)	8–14		≥24	

Solutions Exist Solutions Being Pursued No Known Solutions

Notes for Table 29a and bAnalog, Mixed-signal, and RF Requirements

Explanatory Notes for each row of Tables 29

[1] Year of first digital product for a given technology generation. Lithographic drivers for key technologies at each node are indicated. Year of first analog, RF, and mixed-signal product at the same technology may lag by one generation.

[2] Digital (logic V_{dd}) supply voltage, driven by MPU gate length (M Gate), is repeated here for reference.

[3] Analog supply voltage is expected to lag digital by two or more generations. Additional voltage headroom is needed to avoid excessive power dissipation under reduced signal swing conditions. Analog CMOS designs may use thick gate oxide and low V_t techniques. The analog power supply reduction trend may lag digital backward compatibility trend for I/O such that a common thick gate oxide solution is not feasible.

[4] RF applications will focus on the 0.9– 2.5 GHz, 5– 6 GHz, 17– 20 GHz, 40– 45 GHz, and 60– 65 GHz frequency spectrums. Design of applications at the lower frequencies will continue throughout the duration of the roadmap (lower frequency bands are not "obsoleted" and will continue to be used). Higher frequency bands will drive performance requirements.

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 **130 nm**	2002	2003	2004 **90nm**	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

[5] General purpose analog frequency (such as DSP, audio/video, ADC) trend is in parallel with RF. Very clean, jitter-free, clock frequency generation is required. Transistors: It is expected that speed × power characteristics favor use of bipolar for W_e < 180 nm. MOS speed × power may be favorable relative to bipolar at L_{eff} > 180 nm. Bipolar device assumed through 110 nm (see Potential Solutions Figure 14) followed by MOS device.

[6] Absolute current (independent of device geometry) at which these key RF transistor parameters are measured.

[7] Assumes a "rule of thumb" of approximately 10× the transmit/receive frequency.

[8] Assumes that ft generally follows the progression of f_{max}.

[9] Measured at the specified current (Row 5) and at the application transmit/receive frequency (Row 4).

[10] Bipolar device assumed **up to and including the 110 nm node** (see Potential Solutions Figure 14) followed by MOS device. Assume SPICE model for MOS device: $SVG=Kf/(C_{ox}^2 \times W \times L \times f)$. Values scaled assuming t_{ox}^2 relationship.1/f spectral density is normalized to active device area=1 μm^2, frequency=1Hz. RF MOS device assumed to be realized with the thinnest gate oxide and shortest L_{eff} available at a given node. For this reason, the minimum MPU gate length (M Gate) is indicated as a driver for this device. Although the effects are acute at baseband, 1/f noise can be "mixed up" to RF if present in RF devices. The effect is prominent in MOS devices due to carrier recombination in traps at the insulator-semiconductor interface (surface effect).

[11] Absolute current (independent of device geometry) at which these key analog transistor parameters are measured.

[12] Bipolar device assumed **upto and including the 110 nm node** (see Potential Solutions Figure 14) followed by MOS device. Assume SPICE model for MOS device: $SVG=Kf/(C_{ox}^2 \times W \times L \times f)$. Values scaled assuming t_{ox}^2 relationship. 1/f spectral density is normalized to active device area=1 μm^2, frequency=1Hz. Analog MOS device assumed to use the thicker or analog gate oxide available at a given node. The effect is prominent in MOS devices due to carrier recombination in traps at the insulator-semiconductor interface (surface effect). Vertical devices (bipolar) or sub-surface devices (JFETs) are superior in this regard.

[13] **Bipolar device assumed up to and including the 110 nm node (see Potential Solutions Figure 14) followed by MOS device. Hence, gate oxide leakage has no meaning until the 110 nm node (2004), and the boxes for the previous nodes are left with just a dash in them. For CMOS, analog** power supply constrains minimum gate oxide thickness (and therefore leakage). **T_{ox}=4 nm (100 nm node)**; T_{ox}=3.5 nm (70–50 nm nodes); T_{ox}=3 nm (35 nm node).

[14] Matching specification assumes "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity are required.

[14] **Bipolar device assumed up to and including the 110 nm node (see Potential Solutions Figure 14) followed by MOS device.** Matching specification assumes "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity are required. **Bipolar values specified for an emitter area of 20μm^2, CMOS values specified at a gate overdrive, $V_{gs}-V_{th}$, of 200mV and an area of 250μm^2.**

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[15] RF coupling capacitors are not expected to drive density. Linearity is not driven by this capacitor.

[16] Q is the most important parameter for this type of capacitor. Low series R and low parasitics are key.

[17] Analog filter implementations will drive density to 7 fF/μm^2. As digital filter solutions dominate beyond 2003, bypass capacitor applications will drive density. As digital content increases, chip size decreases, and capacitors occupy a larger percentage of a chip. Choice of implementation is driven by complexity/chip size tradeoff (cost). microelectromechanical systems (MEMS) implementation for filter applications may be favorable at density =7 fF/μm^2. Voltage linearity and leakage are not driven by this capacitor.

[18] Matching important for this capacitor. Specified at a value of 1 pF.

[19] As digital filter solutions dominate beyond 2003, bypass capacitor applications will drive density. High κ dielectrics may be cost-effective as chip size decreases in the 5– 15 year timeframe. Density is driven by low frequency requirements and chip size considerations.

[20] Voltage linearity not driven by this capacitor.

[21] Q is important for this capacitor to provide bypass response at high frequency. Massively parallel, parasitic implementations are expected to dominate for the next five years.

[22] Analog capacitors do not drive density.

[23] Voltage linearity is driven by switched capacitor applications. Low series R is key.

[24] Leakage is driven by feedback capacitor applications where a long time constant is required. Requirement is relaxed with increasing analog clock frequency. Highest quality dielectric is suggested.

[25] Matching is key for analog capacitors. Specified at a value of 1 pF.

[26] Q is important for this resonator. Low RF parasitic structures such as MEMS polysilicon structures are long-term solutions (see Potential Solutions Figure 14).

[27] Matching is important for the analog resistor. Careful layout and photolithographic uniformity are required. Minimum dimensions assumed to be larger than minimum technology dimensions. **Specified at a value of 1 MΩ.**

[28] 1/f noise requirement is most important for the analog resistor. It is assumed that low 1/f solutions other than polysilicon coincide with high Q RF resistor solutions. **1/f spectral density is normalized to resistor area=1 μm^2, frequency=1 Hz.**

[29] Temperature coefficient is important for the analog resistor. Low TC films or TC canceling techniques may be utilized

[30] Q is most important for the inductor. Low series R implementations such as thick copper is assumed for the next five years. CMOS trend toward increasing substrate doping conflicts with inductor integration. Solutions that mitigate the CMOS conflict and maintain Q are assumed.

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[30] Q is most important for the inductor. Low series R implementations such as thick copper is assumed for the next five years. CMOS trend toward increasing substrate doping conflicts with inductor integration. Solutions that mitigate the CMOS conflict and maintain Q are assumed. **Specified at L = 1 nH and f = 1 GHz.**

[31] Signal isolation is best defined as the transmission efficiency (S21 in dB) between a noise source and a noise sensor. Transient sensitivity (in V peak-to-peak) is also an important measure of signal isolation but is not quantified due to its dependence on layout and package. System partitioning, metal interconnect scheme, substrate resistivity, and package design have significant impact on the signal isolation performance. Final result is dependent on application and design tradeoffs.

[32] Gain for low-noise amplifier and mixer benchmark circuits

[33] IIP3 for low-noise amplifier and mixer benchmark circuits

[34] Noise figure for a low-noise amplifier benchmark circuit

[35] Noise for a mixer benchmark circuit

[36] Resolution for A/D, D/A benchmark circuits required for audio/video applications

Several trends have been identified for analog, RF and mixed-signal requirements that will lead to higher levels of integration with logic: raw speed of the logic process will enable more signal processing in the digital realm and the implementation of some RF functions; use of dual-gate oxides for higher voltage logic I/O's will support analog requirements for signal headroom; continued focus on 1/f noise, capacitor density and component matching will be required for power and area efficient design.

Modularity of process features will be desirable in order to adapt the technology to specific SoC architectures. Optimization of the logic process to meet analog transistor specifications may add process complexity, but will be required to achieve mixed-signal integration goals. CMOS will continue to be the technology of choice except for applications where Si or SiGe BiCMOS offers a clear performance or area advantage in high-speed circuits.

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RELIABILITY

Table 30a Reliability Technology Requirements—Near Term

	YEAR / TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
Customer Reliability Expectations (at 85° C Junction Temperature)								
[1]	Early failures (ppm) (First 4000 operating hours)	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
[2]	Long term reliability (5–10 Years) (FITs = failures in 1E9 hours)	10–100	10–100	10–100	10–100	10–100	10–100	10–100
[3]	Soft error rate (FITs)	1000	1000	1000	1000	1000	1000	1000
[4]	Relative failure rate per transistor (normalized to 180 nm)	1	1	1	.62	.62	.62	.34
[5]	Relative failure rate per m of Interconnect (normalized to 180 nm)	1	1	1	.51	.51	.51	.34
[6]	System-on-a-Chip reliability prediction	Logic and Memory			MicroMachine			Micro Optics
[7]	Failure analysis cycle time (days)	1–12	1–12	1–12	1–10	1–10	1–10	1–10

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

Note: Reliability requirement includes chip and package failures. Additional parameters (such as temperature cycling and humidity) need to be specified for package reliability.

Table 30b Reliability Technology Requirements—Long Term

	YEAR / TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
Customer Reliability Expectations (at 85° C Junction Temperature)				
[1]	Early failures (ppm) (First 4000 operating hours)	50–2000	50–2000	50–2000
[2]	Long term reliability (FITs = Failures in 1E9 hours) (5–10 Years)	10–100	10–100	10–100
[3]	Soft error rate (FITs)	1000	1000	1000
[4]	Relative failure rate per transistor (normalized to 180 nm)	.16	.07	.03
[5]	Relative failure rate per m of interconnect (normalized to 180 nm)	.18	.10	
[6]	System-on-a-Chip reliability prediction	Micro Biological		
[7]	Failure analysis cycle time (days)	1–10	1–10	1–10

Solutions Exist (white) *Solutions Being Pursued* (yellow) *No Known Solutions* (red)

Notes for Table 30a and b Reliability Requirements

[1, 2, 3, 5] *Reliability requirements vary with application. For many mainstream customers it will be sufficient to hold current reliability levels steady during this period of rapid technological change. However, other customers would like reliability levels to improve. Degradation of current reliability levels is not acceptable.*

[1] *Early failures are generally associated with defects.*

[3, 4] *Inverse of number of transistors per generation (3) or meters of interconnect per generation (4). For the reliability levels of the chip to remain constant (1,2) the failure rate per transistor or per meter of interconnect must be reduced.*

[6] *Need to develop the capability to predict the reliability of advanced technologies then will be integrated onto advanced Systems-on-a-Chip. Dates when technologies will be inserted are approximate.*

[7] *The time to complete the determination of the cause of a yield, field or design failure.*

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BEYOND CMOS / NOVEL DEVICES

Non – Bulk CMOS Devices Table

Device	INSERTION NODE (NM)	APPLICATION DRIVER (PERFORMANCE, POWER, COST)	INSERTABILITY (SYSTEM)	INSERTABILITY (INFRASTRUCTURE)	ADVANTAGES	CHALLENGES
SOI (PD)	*180*	*Low Power especially. Performance*	*OK*	*OK*	*Low power, high speed, low voltage operation, reduced SER*	*Cost, Dynamic body charge*
SOI (FD)	*130*	*"*	*"*	*"*	*Low power, high speed, low voltage operation, reduced SER*	*Cost, Control of very thin Si layer*
Multi-Vt Logic MOS	*180*	*Performance*	*OK*	*OK*	*High system speed @ relatively low power*	*Cost*
Multi-value logic	*≤100*	*Cost*	*Very Difficult*	*Difficult*	*Density*	*V t control, speed.*
Dynamic Vt logic (gate tied to body)	*≤100 (0.6V restriction on Vdd drives this choice.)*	*"*	*". (Note: 0.6V restriction on Vdd is less than ITRS's Vdd for 100 nm node.)*	*"*	*High speed @ relatively low power*	*Cost, Junction leakage. Restricted to Vdd≤0.6 V. For bulk, isolation is an issue.*
Vertical MOSFET	*≤130 (DRAM)* *≤70 (logic)*	*Performance*	*Issues. (Only one Lg =>no good for analog.)*	*Difficult Issues*	*Litho independence, high Idrive*	*Processing,* *Process integration. Standard CMOS needed on same chip.*
Double Gate SOI	*≤70*	*Performance*	*"*	*Difficult Issues*	*Improved short channel, high Idrive*	*Cost, how to fabricate self-aligned double gate*
Epi channels, including SiGe	*≤70*	*Performance*	*OK*	*OK*	*High mobilities for electrons and holes*	*Process complexity, novel materials and processes*

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Non-Bulk MOS Technology Descriptions

TECHNOLOGY	DESCRIPTION
SOI (PD)	Partially depleted SOI MOSFETs
SOI (FD)	Fully depleted SOI MOSFETs
Multi-Vt Logic	Multiple threshold voltages provided by a second gate fabricated as a mirror image of the control gate
Multi-Value Logic	Logic gates/primitives providing 3 or more logic states
Dynamic-Vt Logic	Second gate is connected to the body providing high Vt in the off-state and low Vt in the on-state
Vertical MOSFET	MOSFETs fabricated with the source/gate/drain vertically aligned providing for either horizontal or vertical current flow
Double Gate SOI	SOI MOSFETs fabricated with 2 gates providing charge control on the two channel interfaces between the source/drain
Epi Channels	MOSFETs containing group IV alloy (SiGe, SiGeC, etc.) epitaxially grown channels
Delta-Type MOSFET	MOSFET in which the channel has a spiked or delta doping
MEM(D)S	Micro-Electro-Mechanical devices/structures fabricated in silicon (e.g., electrical and optical switches, RF resonators, imagers, etc.)

Novel Logic Devices Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
MEMS	100 (dependent on solving difficult problems, not on 100 nm node CDs)	-Cost, Sys on Chip (RF resonators, imaging, sensors) -ULSI switching (open and close) -Microelectronic chem. Sensors	Difficult issues	Difficult issues	Great SOC flexibility, possible speed, lower power, and low crosstalk (optical interconnect)	Integration of MEMS and Si systems; reliability
Resonant Tunneling IC	≤35	Performance, RF	Difficult issues	Difficult issues	Density, performance, RF	Entirely new IC device
3D Stack Structures	≤35	Cost, power	Issues, especially with interconnect	Difficult issues	Very high density & Short interconnects	Process complexity, Heat dissipation
Organic Transistors (could be on plastic substrate)	≤35	Cost, power	Difficult issues	Difficult issues	Cost, power	Entirely new IC device. Temperature limitations during processing
CHINTS (chan. hot electron injection transistor)	≤35	Performance, power	Difficult issues	Issues	Density, power, performance (multi-value logic)	Entirely new IC device
Carbon Nanotube transistor	≤35	Performance, power	Difficult issues	Difficult issues	Density, power	New device & system

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Novel Logic Device Tables (continued)

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
Single Electron Transfer	≤35	Cost	Difficult Issues	Difficult Issues	Desity	New devices & system, Room temp operation questionable, noise (offset charge). Lack of drive current
Crbon Nanotube Transistor	≤35	Performance, Power	Difficult Issues	Difficult Issues	Desity, Power	New Devices & System

Novel Logic Device Technology Descriptions

TECHNOLOGY	DESCRIPTION
3D Stack Structures	CMOS gates fabricated with the p-channel MOSFET stacked on top the n-channel MOSFET. Also, ICs fabricated with 2 or more active layers (containing CMOS gates with interconnect layers) stacked Resonant
Tunnel Diode (RTD) IC	An IC fabricated solely using resonant tunneling diodes (negative differential resistance diodes whose conduction state depends upon energetic coincidence of an electrode Fermi energy with a quantum state formed between 2 high-energy barrier potentials). The IC may also consist of RTDs combined with CMOS gates.
Organic Transistors	Transistors fabricated in polymer materials, perhaps, using plastic substrates
CHINTS	Channel hot electron injection transistor - Channel charge density is supplied by the injection of hot electrons from an electrode
Carbon Nanotube Transistor	A transistor fabricated using amphoteric carbon nanotube technology
Single Electron Transistor	A 3-terminal device based on the Coulomb blockade where the number of electrons on an island or a dot is an integer number controlled by a gate

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Novel Storage Devices Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
FERAM	180	Cost, performance for nonvolatile	OK	OK	high capacitance, nonvolatile, low voltage and power (nonvolatile)	Cost, fab., reliability, esp. for highly scaled technology
Multi level Flash	180	Cost	OK	OK	High density - ==>cost reduction	Accurately placing charge on gate, process control, material and reliability
MRAM	≤ 100	Cost	Issues	Difficult Issues	Density, power, performance, nonvolatility	Reliability and integration. Material quality.
Quantum Dot Memories, including single electron	<35	Cost	Difficult Issues	Difficult Issues	Density, power, , nonvolatile capability	New device & system. Room temperature operation difficult.

Novel Storage Device Technology Descriptions

TECHNOLOGY	DESCRIPTION
FERAM	Ferroelectric RAM
Multi-Level Flash	A flash memory cell containing two or more addressable floating gates for charge storage
MRAM	An array of ultra-small magnetic sensors with hysteresis forming the bits. The bits are set by a magnetic field generated by 2 crossed conductors carrying a current, with a bit consisting of magnetic thin multilayers exhibiting magnetoresistance, the conductance of which is based on the spin state of the bit
Quantum Dot	A memory device in which the storage element consists of 2-terminal Memories quantum dot for storage of multiple or single electrons

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Novel Systems Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
Cryoelectronics, esp. device optimization for reduced temp. operation	*180 (modest cooling); ≤50 (≤ liq. Nitrogen temp.)*	*Performance*	*OK (180 nm) -Packaging and cooling issues*	*Some Issues*	*Speed, power*	*Cost*
Molecular Electronics	*<35*	*Cost*	*Difficult Issues*	*Difficult Issues*	*Desity*	*Entirely new device, system.*
DNA and Biological Computing	*<35*	*Cost, performance*	*Difficult Issues*	*Difficult Issues*	*Density, power, performance*	*Entirely new device, system.*
Quantum Computing -Spin State Structures - Tunneling Phase Logic	*<35*	*Performance, power*	*Difficult Issues*	*Difficult Issues*	*Density, power, performance*	*Entirely new device, system (NMR readout?)*
Quantum devices: Josephson Junction Tunneling devices	*<35*	*Performance*	*Difficult Issues*	*Difficult Issues*	*Speed and relatively low power*	*Entire new device, system. Room temp. operation.*
All-optical integrated computing and swithing	*<35*	*Performance*	*Difficult Issues*	*Difficult Issues*	*Performance crosstalk reduction*	*Entirely new device and system.*

Novel Systems Technology Descriptions

TECHNOLOGY	DESCRIPTION
Cryoelectronics	*CMOS technology cooled for special, high performance applications*
Molecular Electronics	*Electronic logic and memory elements that function as voltage-operated switches fabricated in single molecules*
DNA & Biological Computing	*DNA Computing: Computational functions performed by a DNA molecule; DNA molecules more likely will guide fabrication of nano-structures via self assembly techniques Biological Computing: Biological cells containing intelligent genes that can add numbers, store bits, keep time and execute programs*
Quantum Computing	*Performance of computational functions using quantum effects realized in systems utilizing the spin states of atomic nuclei or, alternatively, of electrons. Each atom or electron provides two basis functions (spin-up & spin-down) that define the eigenstates of the system; these coupled (or entangled) eigenstates define quantum bits or qubits as a superposition of the eigenstates. Calculations are based on the controlled coherent interaction between the two qubits (entanglement).*
Josephson Junction	*Also known as Rapid Single Flux Quantum Logic (RSFQ) Logic Tunneling Devices where a flux quantum is used as a bit. The switching elements are Josephson Junctions formed of a semiconductor-insulator-semiconductor structure.*

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FOLDER 3

FOREWORD

The International Technology Roadmap for Semiconductors (ITRS) is the result of a worldwide consensus building process. This document predicts the main trends in the semiconductor industry spanning across 15 years into the future. The participation of experts from Europe, Japan, Korea, and Taiwan as well as the U.S.A. ensures that the *ITRS* is a valid source of guidance for the semiconductor industry as we strive to extend the historical advancement of semiconductor technology and the worldwide integrated circuit (IC) market. These five regions jointly sponsor the *ITRS*.

The Semiconductor Industry Association (SIA) coordinated the first efforts of producing what was originally *The National Technology Roadmap for Semiconductors* (*NTRS*). The *NTRS* provided a 15-year outlook on the major trends of the semiconductor industry. As such, it was a good reference document for all semiconductor manufacturers. Most of all, the *NTRS* documents provided useful guidance for suppliers of equipment, materials, and software and clear targets for researchers in the outer years.

The semiconductor industry became a global industry in the 1990s, as many semiconductor chip manufacturers established manufacturing or assembly facilities in multiple regions of the world. Similarly, the suppliers to the semiconductor industry have established worldwide operations. Furthermore, alliances, joint ventures, and many forms of cooperation have been established among semiconductor manufacturers as well as among equipment, materials, and software suppliers.

The above considerations led to the realization that a Roadmap that provides guidance for the whole industry would benefit from inputs from all regions of the world that have leadership activities in the field of semiconductors. This realization has led to the creation of the *International Technology Roadmap for Semiconductors* (*ITRS*). The invitation to cooperate on the *ITRS* was extended by the SIA at the World Semiconductor Council in April of 1998 to Europe, Japan, Korea, and Taiwan. The initial collaboration of these five regions produced the *ITRS 1998 Update*, which consisted of a comprehensive revision of the *1997 NTRS* technology requirements tables. Subsequently, the five regions jointly produced *The International Technology Roadmap for Semiconductors, 1999 Edition* and jointly sponsored *The International Technology Roadmap for Semiconductor, 2000 Update*.

The most recent full revision occurred in 2001. The *2001 ITRS* presented the latest prediction of the industry needs and potential solutions through 2016. Additionally, it also began to address the limits of traditional scaling, the opportunity for "equivalent scaling" [the extension of the device scaling approach by improving electrical performance with new or improved materials], the challenges of the industry to maintain historical trends in productivity, and the introduction of the investigation and feasibility of new device candidates within the timeframe of the Roadmap (2013-2016).

In 2002, the *ITRS* international technology working groups (TWGs) reviewed the tables of the *2001 ITRS* edition. The resulting update and clarification produced the *2002 ITRS Update*. Over 100 tables are revised. Table line items are corrected to correlate with other TWG chapters. Several tables now contain new line items or indicate a change in the difficulty of achieving a particular requirement by indicating a color change in the cell.

For the first time, the *ITRS* does not predict a further acceleration in the timing of introduction of new technologies as the industry struggles through the worst recession of its history. The *2002 ITRS Update* table headers and *Overall Roadmap Technology Characteristics* (*ORTC*) tables 1a–1j remain unchanged with the original timing as announced in the *2001 ITRS*. However, once recovery is fully underway, the progress made by companies during these trying times will be realized. The *2003 ITRS* effort, which will be a complete review and rewrite, will indicate whether this pace is a new trend or just a moment of reflection within the industry during the phase of early recovery.

It is the purpose of the *ITRS* documents to provide a reference of requirements, potential solutions, and their timing for the semiconductor industry. This objective has been accomplished by providing a forum for international discussion, cooperation, and agreement among the leading semiconductor manufacturers and the leading suppliers of equipment, materials, and software, as well as researchers from university, consortia, and government labs.

In the last few years, the *ITRS* documents have become a truly common reference for the entire semiconductor industry. Indeed, the cooperative efforts of the *ITRS* participants have fostered cooperation among international consortia, universities, and research institutions around the world. It is hoped that the *2002 ITRS Update* will further contribute to stimulate cooperative R&D investments so that the financial burden can be more uniformly shared by the whole industry. It is also hoped that the *2002 ITRS Update* will continue to stimulate the fundamental elements that encourage innovation in individual companies.

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INTRODUCTION [FROM THE 2001 ITRS]

OVERVIEW

For four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (the number of components per chip doubles every 18 months). The most significant trend for society is the decreasing cost-per-function, which has led to significant improvements of productivity and quality of life through proliferation of computers, electronic communication, and consumer electronics.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor clock rate, GHz**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last two decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. *The International Technology Roadmap for Semiconductors (ITRS)* has been an especially successful worldwide cooperation. It presents an industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, research organizations, and governments. The *ITRS* has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that truly need research breakthroughs.

The 2001 edition of the *ITRS* is the result of the continued worldwide consensus building process. The participation of semiconductor experts from Europe, Japan, Korea, Taiwan, and U.S.A. ensures that the *2001 ITRS* continues to be the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. This is the second edition of *ITRS* that has had worldwide participation throughout its two-year cycle of creation. The diverse expertise and dedicated efforts that this international effort mobilized have brought the Roadmap to a new level of worldwide consensus about future semiconductor technology requirements.

The complete 2001 ITRS and past editions of the 2000 Update and the 1999 ITRS editions are available for viewing and printing as an electronic document at the internet web site http://public.itrs.net.

MEANING OF *ITRS* TECHNOLOGY REQUIREMENTS

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of microelectronics would further reduce the cost per function (averaging ~25% per year) and promote market growth for integrated circuits (averaging ~17% per year). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "*What technical capabilities need to be developed for the industry to continue to stay on Moore's Law and the other trends?*" More and more of the semiconductor industry's research effort, including consortia and collaboration with suppliers, has been shared in a precompetitive environment. The *ITRS* identifies the principal technology needs to guide the shared research. It does this in the two following ways: (1) showing the "targets" that need to be met by "technology solutions" currently under development, and (2) indicating where there are no "known manufacturable solutions" (of reasonable

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confidence) to continued scaling in some aspect of the semiconductor technology. This latter situation is highlighted as red cells in the Roadmap technology requirements tables, and is also referred to as the "Red Brick Wall." The red is officially on the Roadmap to clearly warn where historical trends of progress might end if some real breakthroughs are not achieved in the future. For some Roadmap readers, the red designation may not have adequately served its purpose of highlighting serious and exciting challenges. There can be a tendency to view any number on the Roadmap as "on the road to sure implementation" regardless of its color. To do so would be a serious mistake.

An analysis of "red" usage might classify the red parameters into the following two categories:

1. where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which the industry does not have much confidence in any currently proposed solution(s), or
2. where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end).

To achieve the red parameters of the first category, breakthroughs in research are needed. It is hoped that such breakthroughs would result in the "red" turning to "yellow" (defined as "manufacturable solutions are known") and, ultimately, "white" (defined as manufacturable solutions are known and are being optimized") in future editions of *ITRS*. A conservative interpretation might view the red parameters of the second category as effectively "beyond" or "off" the Roadmap.

The *ITRS* time horizon (15 years) provides a limit to what may be considered "on/off the Roadmap." To date, each edition of the *ITRS* has been built around a view toward continued scaling of CMOS (Complementary Metal-Oxide-Silicon) technology. However, with the 2001 edition, we are reaching the point where the horizon of the Roadmap challenges the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths of roughly 9 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, the *2001 ITRS* begins to address post-CMOS devices.

Another constraint by which some items may be on/off the Roadmap is the breadth of technology addressed. The scope of the *2001 ITRS* specifically addresses detailed technology requirements for all CMOS integrated circuits, including mixed-signal products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to manufacture CMOS ICs are also used for other products such as compound-semiconductor, discrete, optical, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most IC-technology-based micro/nanotechnologies even though that is not the explicit purpose of the Roadmap.

POSITION ON POTENTIAL SOLUTIONS

The *ITRS* strives to avoid prematurely identifying definite solutions to the future technology challenges. This is difficult, since guidance on the research needs is intended. Despite this need to provide guidance, the Roadmap participants are continually pursuing new ways to prevent the Roadmap from being interpreted as limiting the range of creative approaches to further advance microelectronics technology. One of the resulting compromises has been to only present illustrative examples of potential solutions to selected challenges in the *ITRS*. These are not to be construed even as complete lists of all solutions suggested to date, much less exhaustive lists of what should be explored. A few of the potential technical solutions are listed, where known, only to inform the readers of current thinking and efforts. Furthermore, the listing of a particular potential solution does not constitute an endorsement by the Roadmap process.

It *is* the intent of this document to identify the technological barriers and when the industry will likely run into them. It is *not* the intent of this document to identify the most likely solutions to be adopted, nor to focus attention on those potential solutions currently known at the expense of other new concepts. In fact, it is eagerly hoped that this Roadmap will inspire additional innovative solutions. *The semiconductor industry's future success continues to depend on new ideas.*

OVERALL ROADMAP PROCESS AND STRUCTURE

Each technology-area chapter of the *ITRS* is written by a corresponding International Technology Working Group (ITWG). The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut

ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points.

For the *2001 ITRS*, the Focus ITWGs are the following:

- Design
- Test
- Process Integration, Devices, and Structures
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging

Crosscut ITWGs are the following:

- Environment, Safety, and Health
- Yield Enhancement
- Metrology
- Modeling and Simulation

Each ITWG receive inputs from the regional Technology Working Groups (TWGs) of the five geographical regions (Europe, Japan, Korea, Taiwan, and the U.S.A.) One-to-two representatives from each regional TWG represent the regional TWG on the corresponding ITWG. The regional TWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. In 2001, a total of 839 experts volunteered their services in the twelve TWGs in five regions. The composition of the total TWG membership is analyzed in Figure 1. For this edition, three 2-day *ITRS* meetings in Grenoble, France (April, 2001), San Francisco, U.S.A. (July, 2001), and Santa Clara, U.S.A. (November, 2001) provided the main forums for face-to-face discussions among the members of each ITWG and coordination among the different ITWGs. In addition, each of the TWG incorporates feedback gathered from an even larger community through "sub-TWG meetings" and public "Roadmap Workshops." The Roadmap resulting from this broad input is, hopefully, a "best-attempt" at building the widest possible consensus on the future technology needs of the semiconductor industry.

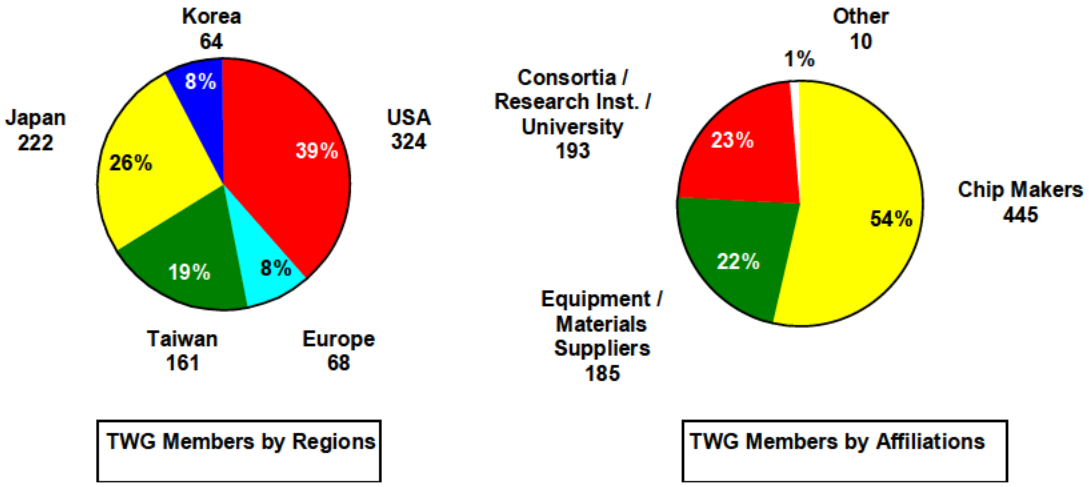


Figure 1 Composition of the Technology Working Group (TWG).

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Overall coordination of the *ITRS* process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each region (representing a regional coordinating committee such as the SIA Roadmap Coordinating Group for the U.S.A.). The principal IRC functions include

- Providing guidance/coordination for the ITWGs,
- Hosting the *ITRS* Workshops, and
- Editing the *ITRS*.

TECHNOLOGY CHARACTERISTICS / REQUIREMENTS TABLES

A central part of the IRC guidance/coordination is provided through the initial creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics (ORTC) tables. These tables summarize key high-level technology requirements, which define the future "technology nodes" and generally establish some common reference points to maintain consistency among the chapters written by individual ITWGs. The high-level targets expressed in the ORTC Tables are based, in part, on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies. Thus, the ORTC provide a "top-down business incentive" to balance the tendency for the ITWGs to become conservative in expressing their individual, detailed future requirements.

Each ITWG chapter contains several principal tables. They are individual ITWGs' technology requirements tables patterned after the ORTC tables. For the *2001 ITRS*, the ORTC and technology requirements tables are separated into "Near-term Years" (2001, 2002… through 2007) and "Long-term Years" (2010, 2013, and 2016). This format is illustrated in Tables B, which contains a few key rows from lithography-related ORTC tables.

Table B ITRS Table Structure—Key Lithography-Related Characteristics by Product Type

Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25

Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. "Production" is defined as when any two companies have reached the production volume of 10k parts per month. Please refer to the Glossary for detailed definitions for Year of Introduction and Year of Production.

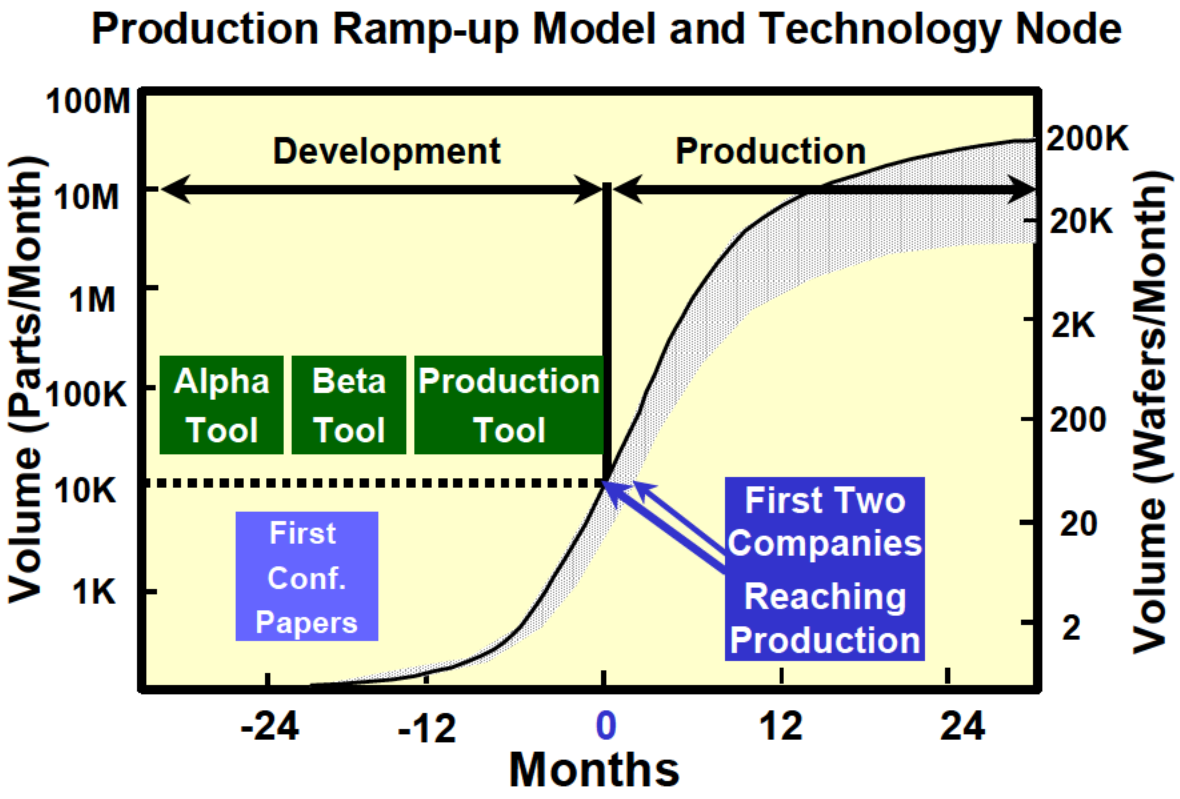


Figure 2 A Typical Production "Ramp" Curve

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "time of Introduction" in the *ITRS* is the "Year of Production," which is defined in Figure 2.

The "Production" time in ITRS refers to the time when the first company brings a technology to production and a second company follows within three months. It is noted that the ITRS Roadmap, by its definition, focuses on forecasting the earliest introduction of the leading-edge technologies in respective fields for producing semiconductors.

Therefore it is obvious that many companies, for a variety of reasons, may choose to introduce a technology node later than the earliest introductions, hence that there is a wide variation of the technologies in actual production status from leading-edge to trailing-edge. Figure 3 shows, in horizontal bar-graph, the actual, annual worldwide wafer production capacity distributions over different process feature sizes. The distributions are quite wide-spread while the ITRS Technology Nodes, shown in small blue marks, are located exactly on the leading-edges of each of them.

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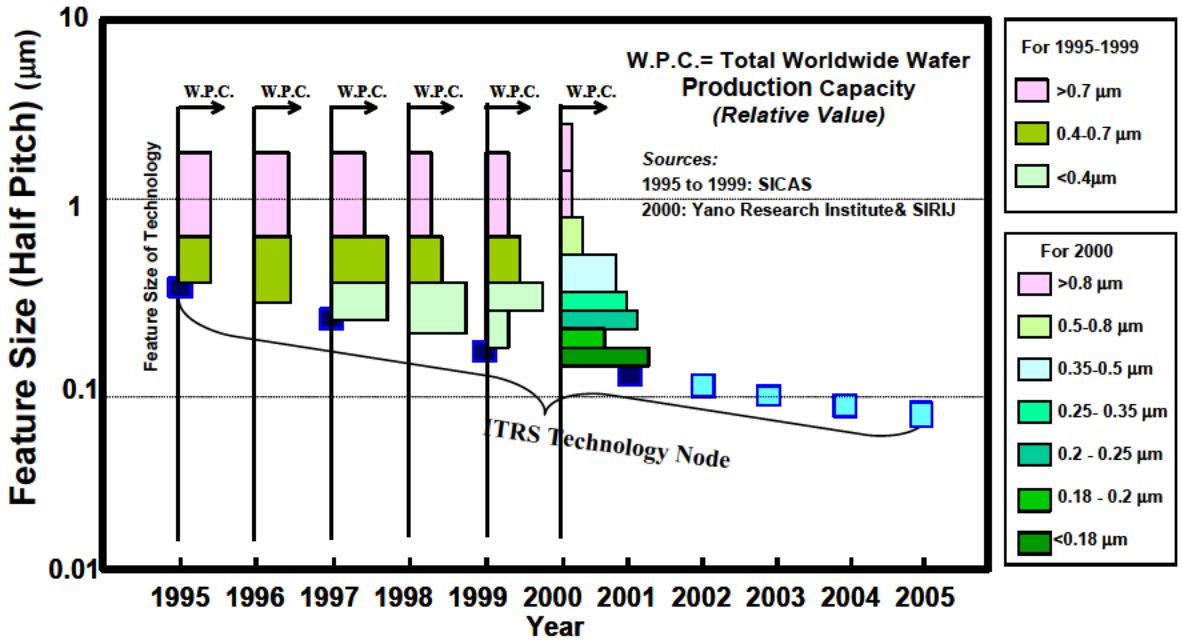
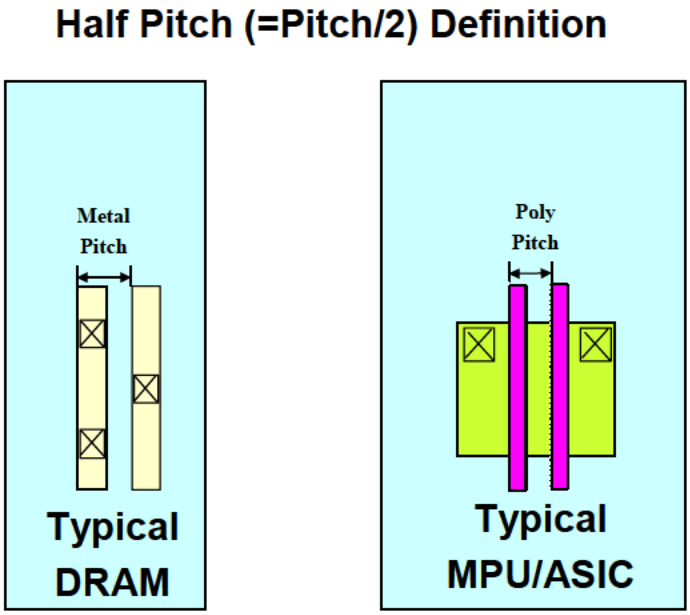


Figure 3 Technology Node Compared to Actual Production Capacity Technology Distribution

Note that some rows in the ORTC and technology requirements tables refer to other timing points, which are defined for each case (e.g., "at sample"). Of course, for the "Long-term Years," for which the table intervals are three years, it is possible for the "best-estimate year of production" to fall in between the selected three-year intervals for some technology requirements. Also note that the "production" ramp in Figure 2 can be viewed as the time to ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (wspm) capacity, the time to ramp from 20 wspm to full capacity can take 9–12 months. This time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month if the chip size were 140 mm^2 (430 gross die per 300 mm wafer × 20K wspm × 70% total yield from wafer starts to finished product = 6M units/month).

TECHNOLOGY NODES

The concept of "technology nodes" used to be quite straightforward to understand as it has historically been linked to the introduction of new Dynamic Random Access Memory (DRAM) generations with a 4× increase in bits/chip between generations. For as long as this cycle strictly followed Moore's Law (three-year cycle for 4×), the technology nodes and DRAM generations were essentially synonymous. However, in recent years, a greater diversity of products serving as technology drivers, faster introduction/optimization of product-specific technology, and the general increase in business and technology complexity are all tending to de-couple the many technology parameters that have traditionally characterized "advance to the next technology node." For example, microprocessor unit (MPU) products have recently driven the reduction of gate length at a faster pace than lithography half-pitch. While DRAM continues to drive the lithography half-pitch, MPU drives the gate length. Even the choice of basic lithography technology has tended to become more product specific (such as "pushing the wavelength as fast as possible" versus "using phase-shift masks"). Following the practice of the *1999 ITRS*, the *2001 ITRS* ORTC tables list the DRAM half-pitch, the MPU half-pitch, and MPU gate length, as shown in Table B. These technology parameters are defined in Figure 4. Any of the four parameters (rows) in Table B may be chosen as the driver for a given technology requirements table of a given ITWG. Nevertheless, for a point of reference, the DRAM half-pitch is still used in the *2001 ITRS* as the designation of the technology node (DRAM still requires the smallest half pitch among all products.). For example, according to Table B, 2003 will be the year of production of the 100 nm node. Again, the "node designation" is defined by DRAM half pitch, not by the transistor gate length or minimum feature size characteristic of that node. Additional (and, in some cases, more precise) definitions related to the *ITRS* tables may be found in the *Glossary*.



** DRAM pitch determines the technology "node" designation*

Figure 4 Definition of the Half Pitch and Gate Length

In recent years the "technology-development cycle" has been closer to two years than three years. On the other hand, the scaling ratio of the minimum feature size of one technology generation to the previous generation may no longer adhere to the historical value of 0.7. For example, 100 nm is not 0.7× of 130 nm. In addition, some companies may choose to introduce a "half node" (for example 150 nm may be considered a half node between the 180 nm node and the 130 nm node) with the intention of introducing the next "full" node at a later time. The *2001 ITRS* acknowledges the validity of these practices and follows the *1999 ITRS* in listing the near-term (2001–2007) technology requirements on yearly intervals and the long-term (2008–2016) requirements on three-year intervals as shown in Table B. Thus, we can say that 2003 is the year of production of the 100 nm node and 2004 is the year of production of the 90 nm node. One may also interpret the long-term three-year interval table as a "challenge" to extend the trend of one major new technology node every three years with scaling ratio of 0.7 between nodes through the "22 nm node" (which include 9 nm transistor gate lengths) in 2016.

DRIVERS FOR ITWG TECHNOLOGY REQUIREMENTS

The particular lithography-related rows selected for Table B from the ORTC tables are special in that any one of them may be designated by an ITWG as a "driver" for any specific row in one of their technology requirements tables. For example, the physical gate length may be the appropriate driver for the gate CD control and the source/drain junction depth. The designation of drivers for technology requirements provides some traceable and supportable assumptions for constructing the ITWG tables. It also provides useful links between the ORTC tables and the ITWG tables. Thus, as the Roadmap is updated in subsequent editions, these links will be used for creating a first-pass version of the new tables. For example, if the requirements in one of these driver rows of the ORTC tables were subsequently pulled-in by one year, it would be assumed that rows in the ITWG technology requirements tables would shift by default along with their designated ORTC driver row.

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FOLDER 6

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) tables are created early in the Roadmap process and are used as the basis for initiating the activities of the International Technology Working Groups (ITWGs) in producing their detailed chapters. These tables are also used throughout the renewal effort of the Roadmap as a means of providing synchronization among the TWGs by highlighting inconsistencies between the specific tables. The process to revise the tables include increasing levels of cross-TWG and international coordination and consensus building to develop underlying models of trends and to reach agreement on target metrics. As a result, the ORTC tables went through several iterations and reviews.

The metric values of the ORTC tables can be found throughout the Roadmap in greater detail in each Technology Working Group chapter. The information in this section is intended to highlight the current rapid pace of advancement in semiconductor technology. It represents a completion of the revision update and renewal work that began in 2000. Additionally, an ORTC Glossary is provided as an appendix.

OVERVIEW OF 2001 REVISIONS

DEFINITIONS

As noted above, the Overall Roadmap Technology Characteristics tables provide a consolidated summary of the key technology metrics. Please note that the year header on the tables may refer to different points in the development/life cycle of integrated circuits (ICs), depending on the individual line item metric. However, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds 10,000 units per month of ICs from a manufacturing site using "production tooling." Additional clarification was provided this year by the *ITRS* executive International Roadmap Committee (IRC), requiring a second company to start production within three months. To satisfy this definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility. Please see the Glossary section for additional details on "Technology Node" and "Production" timing definitions.

Furthermore, new IRC guidelines clarified the definition of a technology node as the achievement of significant advancement in the process technology. To be explicit, a technology node was defined as the achievement of an approximate 0.7× reduction per node (0.5× per two nodes) (Figure 5). The period of time in which a new technology node is reached is called a "technology-node cycle" (Figure 6). It is acknowledged that continuous improvement occurs between the technology nodes, and this is reflected by including data between nodes in the annual columns of the "Near-term years" tables. The "Long-term years" table columns are three-year increments of the *2001 ITRS* timeframe.

ROADMAP TIMELINE

The 2001 edition of the Roadmap maintains a 15-year projection, from 2001 as a reference year and through 2016. However, the timing of future technology nodes has changed from the 1999 edition.

By international consensus, the 130 nm node was pulled in an additional year, continuing the historical precedent for two-year technology-node cycles since 350 nm/1995 (250 nm node in 1997, 180 nm node in 1999). Although there is the possibility of a continuation of the two-year-node cycle trend, the present consensus projects a three-year cycle for DRAM interconnect half-pitch nodes throughout the 2001–2016 Roadmap period (Figure 7).

DRAM interconnect (metal or polysilicon—refer to the Glossary for additional detail) half-pitch will continue to be used as the most representative feature of leading-edge semiconductor manufacturing technology for defining the achievement of a technology node. However, additional data analysis indicates an aggressive trend for the lagging MPU and ASIC interconnect half-pitches to catch up to DRAM half-pitch by 2004 (Figure 7).

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The *2001 ITRS* includes a correction of the past "rounding" convention for the technology node labels. The actual mathematical trend reduces the nodes by 50% every other node, resulting in an actual versus rounded node number targets, starting from 350 nm in 1995 as follows:

Table C Rounded versus Actual Trend Numbers

YEAR OF PRODUCTION	1995	1997	1999	2001	2004	2007	2010	2013	2016
Actual Trend Numbers (nm)	**350**	**247.5**	**175**	**123.7**	**87.5**	**61.9**	**43.8**	**30.9**	**21.9**
ITRS Rounded Node Numbers (nm)	**350**	**250**	**180**	**130**	**90**	**65**	**45**	**32**	**22**

Note the new "rounding" corrections become more critical as the industry moves into the double-digit technology nodes. Some regions, for past publication consistency, will continue to track the previous technology nodes beginning with 100 nm/2003, resulting in milestones that are placed one year earlier than the present 2001 roadmap convention (70 nm/2006; 50 nm/2009; 35nm/2012; 25 nm/2015).

The *printed* MPU gate length received a major correction to more an aggressive starting point in 2001. In addition, a new *physical* gate length is being tracked that further reduces the bottom gate length dimension of a fully-processed transistor. Both the printed and physical gate length trends are forecast to continue scaling by about 70% per two-year cycle through the 32nm physical MPU gate length in 2005, but are expected to return to a three-year cycle trend thereafter, consistent with the present DRAM half-pitch trend forecast (Figure 8).

The ORTC metrics, which guide the Roadmap, are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to achieve industry leadership. Thus, the highly competitive environment of the semiconductor industry quickly tends to make obsolete many portions of the ORTC metrics and, consequently, the Roadmap. Hopefully, our annual update process will provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the *ITRS* to the industry.

For example, there is some anticipation that DRAM half-pitch nodes could undergo an additional one-year pull-in. This possibility will be re-evaluated during the year *2002 ITRS* Update process, along with the possibility of using a two-year node cycle as a longer-term trend. To reflect the variety of cycles and to allow for closer monitoring of future roadmap shifts, it was agreed to continue the practice of publishing annual technology requirements from 2001 through 2007, called the "Near-Term Years," and at three-year (node) intervals thereafter, called the "Long-Term Years" (2010, 2013, 2016).

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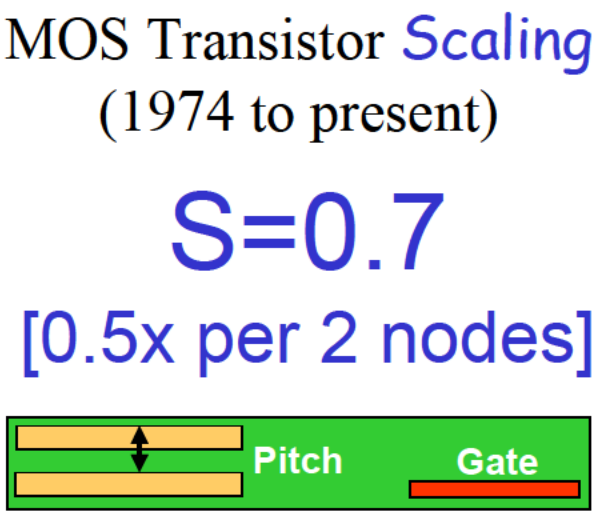


Figure 5 MOS Transistor Scaling—1974 to present

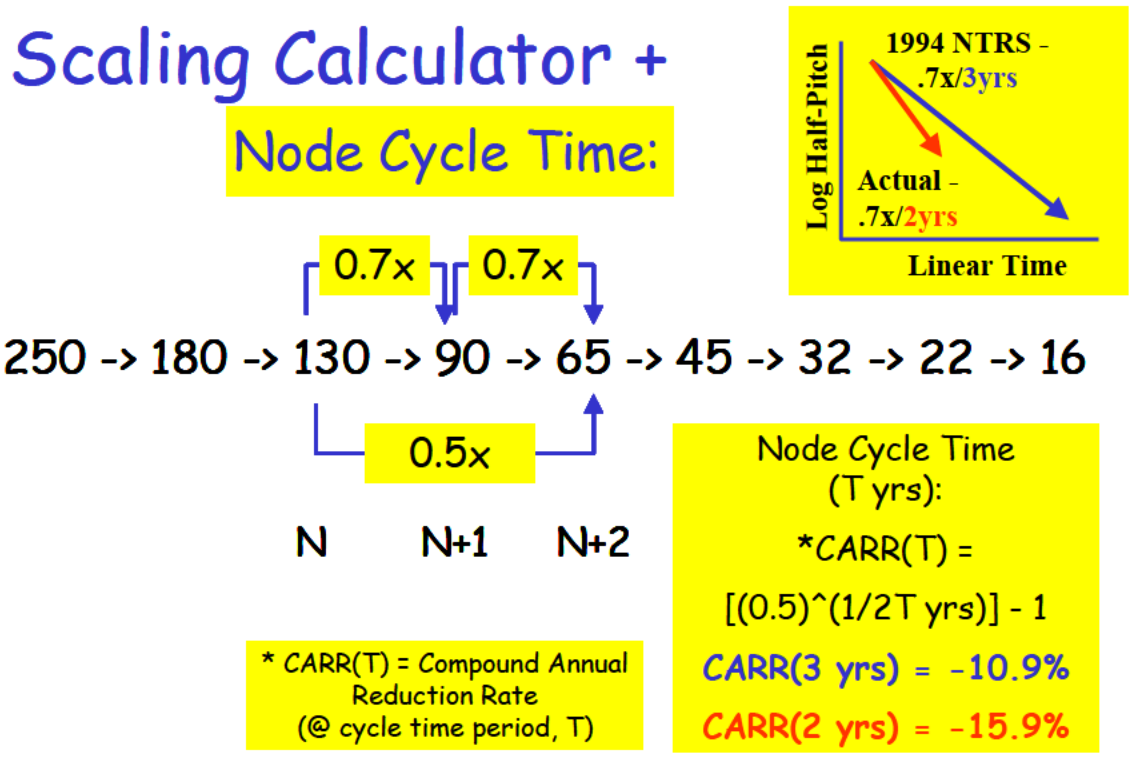


Figure 6 Scaling Calculator

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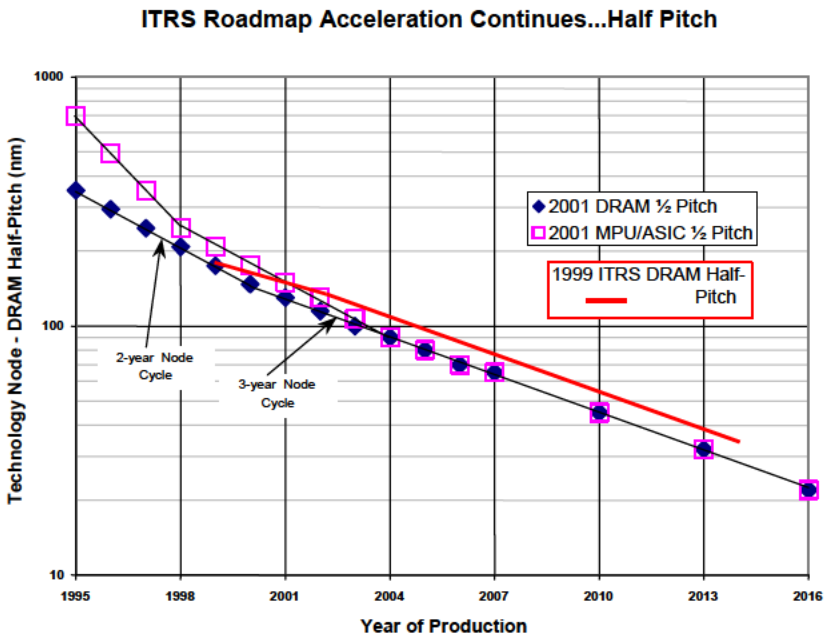


Figure 7 ITRS Roadmap Acceleration Continues—Half Pitch Trends

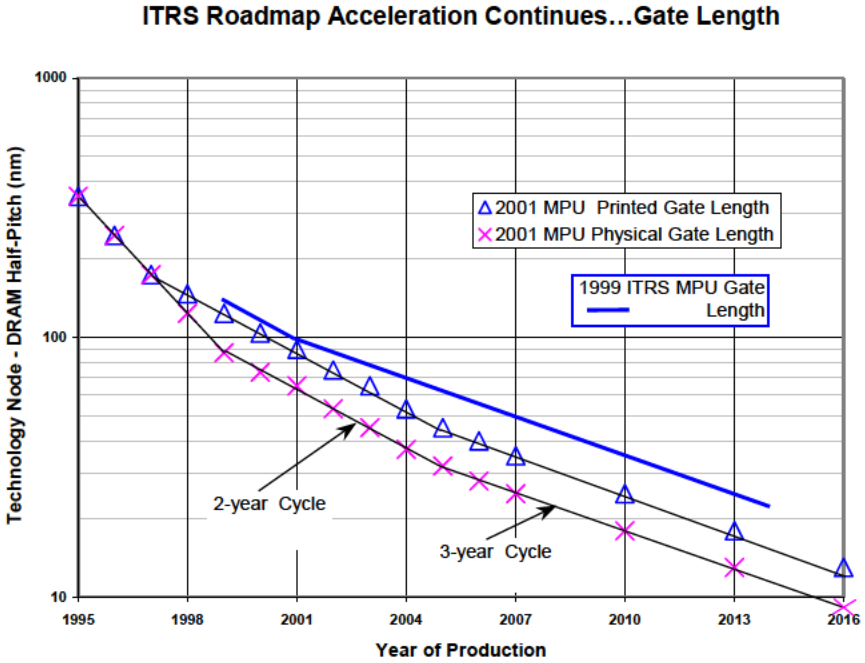


Figure 8 ITRS Roadmap Acceleration Continues—Gate Length Trends

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PRODUCT GENERATIONS AND CHIP-SIZE MODEL

In this section, we will discuss "product generations" and their relationship to the technology nodes, since, in the past, these terms have often been used interchangeably. However, the historically simple picture of a new DRAM product generation every three years (at 4× the previous density and based on an essentially new set of technology features) has become obsolete as a way to define technology nodes. For this 2001 edition, the "technology node" is still linked to an anticipated DRAM feature size (minimum metal or polysilicon half-pitch). However, implications of this connection are diminishing as the product evolution/shrink path becomes more complex.

Historically, DRAM products have been recognized as the technology drivers for the entire semiconductor industry. Prior to the early 1990s, logic (as exemplified by MPU) technology was developed at a slower pace than DRAM technology. During the last few years, the development rate of new technologies used to manufacture microprocessors has accelerated. Microprocessor products are closing the half-pitch technology gap with DRAM, and are now driving the most leading-edge lithography tools and processes—especially for the capability to process the isolated-line feature of the printed and physical gate length. With this 2001 Roadmap it is recognized that DRAM and microprocessor products share the technology leadership role.

However, several fundamental differences exist between the two families of products. Due to strong commodity market economic pressure to reduce cost and increase fab output productivity, DRAM product emphasizes the minimization of the chip size. Therefore development of DRAM technology focuses mainly on minimization of the area occupied by the memory cell. However, this pressure to minimize cell size is in conflict with the requirement to maximize the capacitance of the cell for charge storage performance, which puts pressure on memory cell designers to find creative ways through design and materials to meet minimum capacitance requirements while reducing cell size. In addition, to closely pack the highest number of DRAM cells in the smallest area requires minimization of cell pitch.

Microprocessors have also come under strong market pressure to reduce costs while maximizing performance. Performance is enabled primarily by the length of the transistor gate and by the number of interconnect layers. The 2001 *ITRS* teams have reached consensus on models for the required functionality, chip size, cell area, and density for the ORTC tables. Additional line items were added to communicate the model consensus, and the underlying model assumptions are included in notations. Table 1a and 1b summarize the near and long technology node metrics. As agreed, the key *ITRS* technology node identifier would continue to be the DRAM half-pitch, but also included are the aggressive MPU gate-length performance-driven feature sizes. For completeness, the MPU/ASIC product metal half-pitch are also tracked and that will trail slightly behind or equal to the DRAM half-pitch. The ASIC/low power gate lengths are also included, and lag behind the leading-edge MPU in order to maximize standby and operating current drain. See the Glossary section for additional detail on the definition of the half-pitch and gate-length features. For each product generation, both the leading-edge ("at introduction") and the high-volume ("at production") DRAM products are indicated

It should be noted that the long-term average annualized reduction rate in feature size is projected to continue at approximately 11%/year (~30% reduction/three years), even though this rate accelerated to approximately 16%/year (~30% reduction/two years) in the time interval 1995–2001 (refer to Figure 5). As mentioned above, the overall schedule for introduction of a new product generation has been accelerated by one additional year.

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm) ††	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length) (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
ASIC/Low Power Printed Gate Length (nm) ††	**130**	**107**	**90**	**75**	**65**	**53**	**45**
ASIC/Low Power Physical Gate Length) (nm)	**90**	**75**	**65**	**53**	**45**	**37**	**32**

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm) ††	**25**	**18**	**13**
MPU Physical Gate Length) (nm)	**18**	**13**	**9**
ASIC/Low Power Printed Gate Length (nm) ††	**32**	**22**	**16**
ASIC/Low Power Physical Gate Length) (nm)	**22**	**16**	**11**

Notes for Tables 1a and 1b

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "Physical" gate lengths may be reduced from the "as-printed" dimension. These "Physical" gate-length targets are driven by the need for maximum speed performance in logic Microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design ITWG Tables as needs that drive device design and process technology requirements.

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Table 1c DRAM Production Product Generations and Chip Size Model—Near-term Years

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Cell area factor [a]	8	8	6	6	6	6	6
Cell area [$Ca = af^2$] (μm^2)	0.130	0.103	0.061	0.049	0.039	0.031	0.024
Cell array area at production (% of chip size) §	54.8%	55.3%	55.7%	56.1%	56.4%	56.7%	57.0%
Generation at production §	512M	512M	1G	1G	2G	2G	4G
Functions per chip (Gbits)	0.54	0.54	1.07	1.07	2.15	2.15	4.29
Chip size at production (mm^2)§	127	100	118	93	147	116	183
Gbits/cm^2 at production §	0.42	0.54	0.91	1.15	1.46	1.85	2.35

Table 1d DRAM Production Product Generations and Chip Size Model—Long-term Years

Year of Production	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Cell area factor [a]	6	4	4
Cell area [$Ca = af^2$] (μm^2)	0.012	0.004	0.002
Cell array area at production (% of chip size) §	57.7%	58.1%	58.4%
Generation at production §	8G	32G	64G
Functions per chip (Gbits)	8.59	34.36	68.72
Chip size at production (mm^2)§	181	239	238
Gbits/cm^2 at production §	4.75	14.35	28.85

Notes for Tables 1c and 1d

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows

1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

3. *at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and*
4. *at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).*

InTER-generation chip size growth rate varies to maintain one chip per 572mm^2 field at Introduction and two chips per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Cell area factor [a]	8	8	6	6	6	6	6
Cell area [$Ca = af^2$] (μm^2)	0.130	0.103	0.061	0.049	0.039	0.031	0.024
Cell array area at introduction (% of chip size) §	71.3%	71.8%	72.2%	72.6%	72.9%	73.2%	73.5%
Generation at introduction §	2G	2G	4G	4G	8G	8G	16G
Functions per chip (Gbits)	2.15	2.15	4.29	4.29	8.59	8.59	17.18
Chip size at introduction (mm^2) §	390	308	364	287	454	359	568
Gbits/cm^2 at introduction §	0.55	0.70	1.18	1.49	1.89	2.39	3.03

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years

Year of Production	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Cell area factor [a]	6	4	4
Cell area [$Ca = af^2$] (μm^2)	0.012	0.004	0.002
Cell array area at introduction (% of chip size) §	74.2%	74.6%	74.9%
Generation at introduction §	32G	64G	64G
Functions per chip (Gbits)	34.36	68.72	68.72
Chip size at introduction (mm^2) §	563	373	186
Gbits/cm^2 at introduction §	6.10	18.42	37.00

Notes for Tables 1e and 1f

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows

1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

5. *at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and*
6. *at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).*

InTER-generation chip size growth rate varies to maintain one chip per 572mm^2 field at Introduction and two chips per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

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Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
SRAM Cell (6-transistor) Area factor ++	126.1	123.0	120.3	117.8	115.6	113.7	111.9
Logic Gate (4-transistor) Area factor ++	320.0	320.0	320.0	320.0	320.0	320.0	320.0
SRAM Cell (6-transistor) Area efficiency ++	0.63	0.63	0.63	0.63	0.63	0.63	0.63
Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50	0.50	0.50	0.50	0.50
SRAM Cell (6-transistor) Area w/overhead ++	3.3	2.5	2.0	1.5	1.2	0.93	0.73
Logic Gate (4-transistor) Area w/overhead ++	10.4	8.2	6.5	5.2	4.1	3.3	2.6
Transistor density SRAM (Mtransistors/cm^2)	184	237	305	393	504	646	827
Transistor density logic (Mtransistors/cm^2)	38.6	48.6	61.2	77.2	97.2	122.5	154.3
Generation at introduction *	p04c	—	—	p07c	—	—	p10c
Functions per chip at introduction (million transistors [Mtransistors])	193	243	307	386	487	614	773
Chip size at introduction (mm^2) ‡	280	280	280	280	280	280	280
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	69	87	110	138	174	219	276
Generation at production *	p01c	—	—	p04c	—	—	p07c
Functions per chip at production (million transistors [Mtransistors])	97	122	153	193	243	307	386
Chip size at production (mm^2) §§	140	140	140	140	140	140	140
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	69.0	87.0	109.6	138.0	173.9	219.1	276.1

Notes for Tables 1g and 1h

++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples— the cost-performance processor, p01c, was introduced in 1999, but not ramped into volume production until 2001; similarly, the p04c, is introduced in 2001, but is targeted for volume production in 2004.*

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/1999), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5× every two-year technology node through 2001, then 0.5×every three-year technology node after 2001.

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
SRAM Cell (6-transistor) Area factor ++	**107.8**	**106.7**	**105.7**
Logic Gate (4-transistor) Area factor ++	**320.0**	**320.0**	**320.0**
SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**
Logic Gate (4-transistor) Area efficiency ++	**0.50**	**0.50**	**0.50**
SRAM Cell (6-transistor) Area w/overhead ++	**0.22**	**0.17**	**0.13**
Logic Gate (4-transistor) Area w/overhead ++	**0.82**	**0.65**	**0.51**
Transistor density SRAM (Mtransistors/cm^2)	**1718**	**3532**	**7208**
Transistor density logic (Mtransistors/cm^2)	**309**	**617**	**1235**
*Generation at introduction **	**p13c**	**p16c**	**p19c**
Functions per chip at introduction (million transistors [Mtransistors])	**1546**	**3092**	**6184**
Chip size at introduction (mm^2) ‡	**280**	**280**	**280**
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**552**	**1104**	**2209**
*Generation at production **	**p10c**	**p13c**	**p16c**
Functions per chip at production (million transistors [Mtransistors])	**773**	**1546**	**3092**
Chip size at production (mm^2) §§	**140**	**140**	**140**
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**552**	**1104**	**2209**

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Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years

Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Logic (Low-volume Microprocessor) High-performance ‡							
Generation at production **	p01h	—	p03h	—	p05h	—	p07h
Functions per chip (million transistors)	276	348	439	553	697	878	1106
Chip size at production (mm^2) §§	310	310	310	310	310	310	310
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	89	112	142	178	225	283	357
ASIC							
ASIC usable Mtransistors/cm^2 (auto layout)	89	112	142	178	225	283	357
ASIC max chip size at production (mm^2) (maximum lithographic field size)	800	800	572	572	572	572	572
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	714	899	810	1020	1286	1620	2041

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years

Year of Production	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Logic (Low-volume Microprocessor) High-performance ‡			
Generation at production **	—	p13h	—
Functions per chip (million transistors)	2212	4424	8848
Chip size at production (mm^2) §§	310	310	310
High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	714	1427	2854
ASIC			
ASIC usable Mtransistors/cm^2 (auto layout)	714	1427	2854
ASIC maximum chip size at production (mm^2)(maximum lithographic field size)	572	572	572
ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4081	8163	16326

Notes for Tables 1i and 1j

*** p is processor, numerals reflect year of production; h indicates high-performance product. Examples—the high-performance processor, p99h, was ramped into volume production in 1999; similarly, the p01h, is introduced in 2001.*

‡ MPU High-performance Model—High-performance MPU includes large L2 and L3 on-chip SRAM (2MByte/1999) plus a larger logic core (P99h core = 25M transistor (Mtransistors) both SRAM and Logic functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5x every two-year technology node through 2001, then 0.5x every three-year technology node after 2001.

CHIP-SIZE, LITHOGRAPHIC-FIELD, AND WAFER-SIZE TRENDS

Despite the continuous reduction in feature size of about 30% every three years, the size of first DRAM product demonstration in technical forums such as the IEEE International Solid State Circuits Conference (ISSCC) has continued to double every six years (an increase of about 12%/year). This increase in chip area has been necessary to accommodate 59% more bits/capacitors/transistors per year in accordance with Moore's Law (historically doubling functions per chip every 1.5–2 years). However, to maintain the historical trend of reducing cost/function by ~25–30%/year, it is necessary to continuously enhance equipment productivity, increase manufacturing yields, use the largest wafer size available, and, most of all, increase the number of chips available on a wafer.

The increase in the gross number of chips available on a wafer is primarily obtained by reducing the area of the chip by means of a combination of smaller feature size (shrink/scaling) and product/process redesign (compaction). For instance, using the latest models, it is forecast that the introduction chip area of a cost-effective product generation [which doubles the inter-generation (generation-to-generation) functionality every two years] must either remain flat or grow no faster than 20% every four years. Furthermore, the area must be shrunk at an intra-generation (within a generation) annual reduction rate of 50% (the square of the .7× lithography reduction rate) during every technology node period.

Affordable DRAM products must also achieve virtually flat intra-generation chip-sizes, and they must also maintain a cell area array efficiency ratio of less than 70% of total chip area. Therefore, DRAM products require aggressive cell area factors (cell area in units of minimum-feature-size-squared). The Front End Processes International Technology Working Group has provided the cell area factors and detailed the challenges and needs for solutions to meet the aggressive cell area goals in the Front End Processes chapter. Due to the importance of tracking/coordinating these new challenges, the DRAM cell area factor, the target cell sizes, and the cell array area percentage of total chip-size line items will continue to be tracked in ORTC Tables 1c, d, e, and f. (Refer to the Glossary for additional details.)

In 2001 the Design ITWG improved the MPU chip size model to update with the latest transistor densities, large on-chip SRAM, and smaller target chip sizes. The Design ITWG has also added additional detail to the model, including transistor design improvement factors. The Design ITWG notes that design improvements occur at a slow rate in SRAM transistors and very little in logic gate transistors. Almost all the "shrink" and density improvement comes from lithography-enabled interconnect half-pitch scaling alone.

The present MPU chip size model reflects additional competitive requirements for affordability and power management by targeting flat chip size trends for both high-performance MPUs ($310mm^2$) and cost-performance MPUs ($140mm^2$). Due to the MPU two-year-cycle half-pitch "catch-up phase" through the year 2004, the MPU products may be able to maintain flat chip sizes due to lithography improvements alone. However, after 2004, the intra-generation chip size of MPUs can remain flat only by slowing the rate of on-chip transistors to double every technology node.

Due to the forecasted return to a three-year technology node cycle, the present MPU chip-size model slows the Moore's Law rate of on-chip transistors to 2× every three years. In order to maintain a flat chip size target and also return to the historical doubling every two years of on-chip functionality (transistors), MPU chip and process designers must add additional design/process improvements to the fundamental lithography-based scaling trends. The new target metrics of the MPU model are summarized in Tables 1g, h, I, and j.

To improve productivity, it is necessary to increase the output of good chips at each step in the fabrication process. The ability of printing multiple chips in a single exposure is a key productivity driver and is determined by the field size of the lithographic tool and the size and aspect ratio of the chips being printed on the wafer. In the past, lithography exposure field sizes doubled every other technology node to meet the demand for increasing chip sizes. The result was the achievement of very large step-and-scan fields ($25\times32 = 800mm^2$) by 1999. However, the Lithography ITWG indicates that maintaining the large field size under continued reduction of exposure features is increasing costs dramatically. Therefore, the ITWG forecasts a requirement for the economically affordable lithography field to be reduced to a $572mm^2$ level (22×26) by the 90 nm node. That trend is shown in Tables 2a and b.

DRAM chip sizes were deemed to be the most appropriate driver of affordable lithography field sizes. In the present *ITRS* chip-size model for DRAMs, the introduction-level chip size is targeted to be smaller than the new affordable $572mm^2$ lithography field size, fitting at least one introduction-level chip size within the field. The production-level DRAM model fits at least two die within the affordable field. The combination of technology-node scaling and cell design improvements (A-factor reduction) accomplishes that goal, while also maintaining a goal of doubling on-chip bits every two years. However, the slowing of DRAM design improvements causes a requirement to add fewer on-chip bits to stay under the

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affordable lithography field limit. This accomplished in the present DRAM model by slowing the short-term Moore's Law bits/chip rate from 2×/1.5 years to 2×/ two years. In the later years of the Roadmap the rate is stretched even more to 2×/2.5 to three years, as required. The data targets for the DRAM model are included in Tables 1c, d, e, and f.

Both the DRAM and MPU models depend upon achieving the aggressive DRAM and MPU design and process improvement targets. If those targets slip, then pressure will increase to print chip sizes larger than the present roadmap, or further slow the rate of "Moore's-Law" on-chip functionality. Either of these consequences will result in a negative impact upon cost-per-function reduction rates—the classical measure of our industries productivity-improvement and competitiveness.

With increasing cost reduction pressures, the need for the 300 mm productivity boost will also increase in urgency, especially for leading-edge manufacturers, but the poor economy will create challenges and limit capital investment. The 2001 Wafer-Diameter Generation roadmap (see Tables 2a and b) is consistent with the ramp of 300 mm capacity beginning 2001. Also, the first manufacturing capability for the next 1.5× wafer size conversion to 450 mm diameter is not anticipated to be required until 2013 in the present roadmap. However, should the other productivity-improvement drivers (lithography and design/process improvements) fail to stay on schedule, there would be a need to accelerate the use of increased wafer diameter as a productivity improvement.

The affects of future technology acceleration/deceleration and the timing of the next wafer generation conversion requires the development and application of comprehensive long-range factory productivity and industry economic models. Such industry economic modeling (IEM) work is being sponsored and carried out jointly by SEMI and International SEMATECH.

Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

(Note: 2001 Lithographic field sizes represent current capability)

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length(nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Lithography Field Size							
Lithography Field Size—area (mm^2)	**800**	**800**	**800**	**800**	**800**	**800**	**572**
Lithographic field size — length (mm)	**32**	**32**	**32**	**32**	**32**	**32**	**26**
Lithographic field size — width (mm)	**25**	**25**	**25**	**25**	**25**	**25**	**22**
Maximum Substrate Diameter (mm) — High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	**300**	**300**	**300**	**300**	**300**	**300**	**300**

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Lithography Field Size			
Maximum lithographic field size—area (mm^2)			
Lithography Field Size—area (mm^2)	**572**	**572**	**572**
Maximum lithographic field size—length (mm)	**26**	**26**	**26**
Maximum lithographic field size—width (mm)	**22**	**22**	**22**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)			
Bulk or epitaxial or SOI wafer	**300**	**450**	**450**

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PERFORMANCE OF PACKAGED CHIPS

NUMBER OF PADS AND PINS / PAD PITCH, COST PER PIN, FREQUENCY

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or bits (memory cells) for each product generation. Typically, the number of pads and pins necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases. (Refer to Tables 3a and b)

Additional power and ground connections to the chip are also necessary to optimize power management and to increase noise immunity. Based upon chip pad-count numbers supplied by the Test ITWG, logic products (MPUs and high-performance ASICs) both approach 4-6K pads over the *ITRS* period. The MPU products are forecast to increase the total number of pads through this period by nearly 50%, and the ASICs double the maximum number of pads per chip. The two product types also differ significantly in the ratio of power/ground pads. The MPU product pad counts typically have 1:3 signal I/O pads and 2:3 power and ground pads, or two power/ground pads for every signal I/O pad. Unlike MPUs, high-performance ASIC product pad counts typically include one power/ground pad for each signal I/O pad.

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Number of Chip I/Os (Number of Total Chip Pads) — Maximum							
Total pads—MPU	**3072**	**3072**	**3072**	**3072**	**3072**	**3072**	**3072**
Signal I/O—MPU (1/3 of total pads)	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**	**1024**
Power and ground pads—MPU (2/3 of total pads)	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**	**2048**
Total pads—ASIC high-performance	**3000**	**3200**	**3400**	**3600**	**4000**	**4200**	**4400**
Signal I/O pads—ASIC high-performance	**1500**	**1600**	**1700**	**1800**	**2000**	**2100**	**2200**
Power and ground pads—ASIC high-performance (½ of total pads)	**1500**	**1600**	**1700**	**1800**	**2000**	**2100**	**2200**
Number of Total Package Pins—Maximum [1]							
Microprocessor/controller, cost-performance	**480–1,200**	**480–1320**	**500–1452**	**500–1600**	**550–1760**	**550–1936**	**600–2140**
Microprocessor/controller, high-performance	**1200**	**1320**	**1452**	**1,600**	**1,760**	**1,936**	**2,140**
ASIC (high-performance)	**1700**	**1870**	**2057**	**2263**	**2489**	**2738**	**3012**

Notes for Tables 3a and 3b

[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by PWB technology and system cost.

The highest pin count applications will as a result use larger pitches and larger package sizes.

The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2 1 to 1 4

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Number of Chip I/Os (Number of Total Chip Pads) — Maximum			
Total pads—MPU	**3840**	**4224**	**4416**
Signal I/O—MPU (1/3 of total pads)	**1280**	**1408**	**1472**
Power and ground pads—MPU (2/3 of total pads)	**2560**	**2816**	**2944**
Total pads—ASIC high-performance	**4800**	**5400**	**6000**
Signal I/O pads—ASIC high-performance	**2400**	**2700**	**3000**
Power and ground pads—ASIC high-performance (½ of total pads)	**2400**	**2700**	**3000**
Number of Total Package Pins—Maximum [1]			
Microprocessor/controller, cost-performance	**780–2782**	**1014–3616**	**1318–4702**
Microprocessor/controller, high-performance	**2782**	**3616**	**4702**
ASIC (high-performance)	**4009**	**5335**	**7100**

Package pin count (Tables 3 a and b) and cost-per-pin (Tables 4 a and b), provided by the Assembly and Packaging ITWG, point out challenges to future manufacturing economics. Based upon the projected growth in the number of transistors/chip, it is forecast that the number of package pin/balls will continue to grow at an annual rate of approximately 10%, while the cost/pin decreases at 5%/year. These trends make it more challenging for suppliers of packaging technologies to deliver cost-effective solutions, because the overall average cost of packaging will increase annually at 5%/year (.95 cost/pin × 1.10 pins/year = 1.05 cost/year).

In the very competitive consumer electronics product environment, prices for high-volume, high-tech products such as PCs and cell phones tend to remain flat or even decrease. These same high-tech products typically also deliver twice the performance every two years. This is the end-use market environment of the leading-edge semiconductor manufacturer, and it is the fundamental economic driver behind the *ITRS* economic requirement to reduce cost per function (bits, transistors) at an annual 30% or faster rate (2× functionality/chip at flat price every two years = 29%/year).

If future semiconductor component products must be targeted to maintain constant or decreasing prices and the average number of pins per unit increases at 10% while the average cost per pin decreases at only 5%, then the following will occur:

1. the average packaging share of total product cost will double over the 15-year roadmap period, and
2. the ultimate result will be greatly reduced gross profit margins and limited ability to invest in R&D and factory capacity.

This conclusion is one of the drivers behind the industry trends to reduce the overall system pin requirements by combining functionality into Systems-on-Chip (SoC) and through the use of multi-chip modules, bumped chip-on-board (COB), and other creative solutions.

In addition to the need to increase functionality while exponentially decreasing cost per function, there is also a market demand for higher-performance, cost-effective products. Just as Moore's Law predicts that functions-per-chip will double every 1.5–2 years to keep up with consumer demand, there is a corresponding demand for processing electrical signals at progressively higher rates. In the case of MPUs, processor instructions/second have also historically doubled every 1.5–2 years. For MPU products, increased processing power, measured in millions of instructions per second (MIPs), is accomplished through a combination of "raw technology performance" (clock frequency) multiplied by "architectural performance" (instructions per clock cycle). The need for a progressively higher operational frequency associated with an

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increasing average chip size will continue to demand the development of novel process, design, and packaging techniques.

These considerations are reflected in Tables 4c and d, which includes line items contributed by the Design and Assembly and Packaging ITWGs to forecast the maximum on-chip and chip-to-board frequency trends. The highest frequency obtainable in each product generation is directly related to the intrinsic transistor performance (on-chip, local clock). The difference between this "local" frequency and the frequency of signals traveling across the chip increases due to degradation of signal propagation delay caused by line-to-line and line-to-substrate capacitive coupling. Additional signal degradation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be the only viable way to eliminate any parasitic effect introduced by the package. To optimize signal and power distribution across the chip, it is expected that the number of layers of interconnect will continue to increase. As size downscaling of interconnect also continues, wider use of copper (low resistivity) and various inter-metal insulating materials of progressively lower dielectric constant (κ~2–3) will be adopted in the chip fabrication process. Multiplexing techniques will also be used to increase the chip-to-board operating frequency (off-chip).

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years [Update]

	Year of Production	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
	Chip Pad Pitch (micron)							
Was	Pad pitch—ball bond	45	35	30	25	20	20	20
Is	Pad pitch—ball bond	45	40	35	30	25	20	20
Was	Pad pitch—wedge bond	40	35	30	25	20	20	20
Is	Pad pitch—wedge bond	50	50	40	40	35	35	30
Was	Pad Pitch—area array flip-chip (cost-performance, high-performance)	160	160	150	150	130	130	120
Is	Pad Pitch—area array flip-chip (cost-performance, high-performance)	200	180	150	150	100	100	80
Was	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	150	130	120	110	100	90	80
Is	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	80	80	60	60	40	40	30
	Cost-Per-Pin							
Was	Package cost (cents/pin) (cost-performance)—minimum–maximum	0.80–1.60	0.75–1.44	0.70–1.30	0.66–1.17	0.61–1.06	0.56–1.03	0.64–1.00
Is	Package cost (cents/pin) (cost-performance)—minimum–maximum	0.80–1.60	0.75–1.30	0.70–1.24	0.66–1.17	0.61–1.11	0.56–1.06	0.64–1.01
	Package cost (cents/pin) (Memory)—minimum–maximum	0.36–1.54	0.34–1.39	0.32–1.26	0.30–1.14	0.28–1.03	0.27–0.93	0.27–0.84

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Table 4b Performance and Package Chips: Pads, Cost—Long-term Years [Update]

	Year of Production	2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU/ASIC ½ Pitch (nm)	45	32	22
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	Chip Pad Pitch (micron)			
	Pad pitch—ball bond	20	20	20
	Pad Pitch—wedge bond	20	20	20
Was	Pad Pitch—area array (cost-performance, high-performance)	90	80	70
Is	Pad Pitch—area array (cost-performance, high-performance)	70	70	50
Was	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	60	45	30
Is	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	20	20	15
	Cost-Per-Pin			
	Package cost (cents/pin) (cost-performance)— minimum–maximum	0.49–0.98	0.42–0.93	0.36–0.79
	Package cost (cents/pin) (Memory)— minimum–maximum	0.22–0.54	0.19–0.39	0.19–0.33

Table 4c Performance and Package Chips: Frequency On-Chip Wiring Levels—Near-term Years [Update]

	YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
	Chip Frequency (MHz)							
	On-chip local clock	1,684	2,317	3,088	3,990	5,173	5,631	6,739
	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	1,684	2,317	3,088	3,990	5,173	5,631	6,739
Was	Maximum number wiring levels—maximum	7	8	8	8	9	9	9
Is	Maximum number wiring levels—maximum	10	10	12	13	14	14	14
Was	Maximum number wiring levels—minimum	7	7	8	8	8	9	9
Is	Maximum number wiring levels—maximum	10	10	12	9	10	10	10

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*Table 4d Performance and Package Chips: Frequency, On-Chip Wiring Levels—Long-term Years [**Update**]*

	Year of Production	2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU/ASIC ½ Pitch (nm)	45	32	22
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	Chip Frequency (MHz)			
	On-chip local clock	11,511	19,348	28,751
	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	11,511	19,348	28,751
Was	Maximum number wiring levels—maximum	10	10	10
Is	Maximum number wiring levels—maximum	14	15	15
Was	Maximum number wiring levels—minimum	9	9	10
Is	Maximum number wiring levels—minimum	10	11	11

Note for Tables 4c and 4d

[1] The off chip frequency is expected to increase for a small number of high speed pins which will be used in combination with a large number of lower speed pins

[2] In 2001, high-speed serial communications transceiver devices are achieving chip-board frequencies of 3.125 GHz using CMOS, and 10 GHz using SiGe. In 2002 it is expected that 10 GHz transceivers will be fabricated using CMOS. 40 GHz SiGe devices are expected in 2003. The roadmap for higher levels of integration with wider bus widths, is shown in the High Frequency Serial Communications section in the Test chapter.

Add

[3] The Minimum number of wiring levels represents the Interconnect metal levels, and the Maximum number of Interconnect wiring levels includes the Minimum number of wiring levels plus additional optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

ELECTRICAL DEFECT DENSITY

The latest targets for electrical defect density of DRAM, MPU, and ASIC (necessary to achieve 83–89.5 % chip yield in the year of volume production) are shown in Tables 5a and b. The allowable number of defects is calculated by taking into account the different chip sizes based on the latest chip size model forecasts, as reported in Table 1 for DRAM and microprocessors. In addition, the data in the table are now reported only at the production-level of the product life-cycle. Other defect densities may be calculated at different chip sizes at the same technology node by using the formula found in the *Yield Enhancement* chapter. The approximate number of masks for logic devices is included as an indicator of the ever-increasing process complexity.

Table 5a Electrical Defects—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	**1,963**	**2,493**	**2,148**	**2,748**	**1,752**	**2236**	**1426**
MPU Random Defect D_0 at production chip size and 83% yield (faults/m^2) §§	**1,356**	**1,356**	**1,356**	**1,356**	**1,356**	**1,356**	**1,356**
# Mask Levels – MPU	**25**	**25**	**25**	**25**	**25**	**27**	**27**
# Mask Levels – DRAM	**21**	**22**	**24**	**24**	**24**	**24**	**24**

Table 5b Electrical Defects—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	**1356**	**1356**	**1356**
MPU Random Defect D_0 at production chip size and 83% yield (faults/m^2) §§	**1464**	**1116**	**1134**
# Mask Levels – MPU	**27**	**29**	**29**
# Mask Levels – DRAM	**26**	**26**	**26**

Notes for Tables 5a and 5b

D_0 — defect density

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows

1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. *at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and*
2. *at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).*

InTER-generation chip size growth rate varies to maintain one chip per 572mm^2 field at Introduction and two chips per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5× every two-year technology node through 2001, then 0.5× every three-year technology node after 2001.

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POWER SUPPLY AND POWER DISSIPATION

Reduction of power supply voltage (see Tables 6a and b) is driven by several factors—reduction of power dissipation, reduced transistor channel length, and reliability of gate dielectrics. As seen in Tables 6a and b, the value of the power supply voltage is now given as a range.

Selection of a specific V_{dd} value continues to be a part of the analysis undertaken to simultaneously optimize speed and power for an IC, leading to a range of usable power supply voltages in each product generation. Values of V_{dd} as low as 0.5 volts are expected to be achieved by 2013, but the lowest target is now 0.4V by 2016 (versus 0.3V by 2014 in the *1999 ITRS*).

Maximum power trends (e.g., for MPUs) are presented in three categories—1) high-performance desktop applications, for which a heat sink on the package is permitted; 2) cost-performance, where economical power management solutions of the highest performance are most important; and 3) portable battery operations. In all cases, total power consumption continues to increase, despite the use of a lower supply voltage. The increased power consumption is driven by higher chip operating frequencies, the higher interconnect overall capacitance and resistance; and the increasing gate leakage of exponentially-growing and scaled on-chip transistors.

Table 6a Power Supply and Power Dissipation—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Power Supply Voltage (V)							
V_{dd} (high performance)	**1.1**	**1.0**	**1.0**	**1**	**0.9**	**0.9**	**0.7**
V_{dd} (Low Operating Power, high V_{dd} transistors)	**1.2**	**1.2**	**1.1**	**1.1**	**1.0**	**1.0**	**0.9**
V_{dd} (Low Standby Power, high V_{dd} transistors)	**1.2**	**1.2**	**1.2**	**1.2**	**1.2**	**1.2**	**1.1**
Allowable Maximum Power [1]							
High-performance with heatsink (W)	**130**	**140**	**150**	**160**	**170**	**180**	**190**
Cost-performance (W)	**61**	**75**	**81**	**85**	**92**	**98**	**104**
Battery (W)—(hand-held)	**2.4**	**2.6**	**2.8**	**3.2**	**3.2**	**3.5**	**3.5**

Table 6b Power Supply and Power Dissipation—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Power Supply Voltage (V)			
V_{dd} (high performance)	**0.6**	**0.5**	**0.4**
V_{dd} (Low Operating Power, high V_{dd} transistors)	**0.8**	**0.7**	**0.6**
V_{dd} (Low Standby Power, high V_{dd} transistors)	**1.0**	**0.9**	**0.9**
Allowable Maximum Power [1]			
High-performance with heatsink (W)	**218**	**251**	**288**
Cost-performance (W)	**120**	**138**	**158**
Battery (W)—(hand-held)	**3.0**	**3.0**	**3.0**

Note for Table 6a and 6b

[1] Power will be limited more by system level cooling and test constraints than packaging

COST

Tables 7a and b are dedicated to cost trends. The ability to reduce the cost per function by an average 25–30% each year represents one of the unique features of the semiconductor industry and is a direct consequence of the market pressure to continue to deliver twice the functionality on-chip every 1.5–2 years in an environment of constant or reducing prices. In support of this cost reduction, a continuously increasing amount of investment is needed for R&D and manufacturing capital. Even on a per-factory basis, the capital cost of manufacturing continues to escalate. Yet, the semiconductor industry has historically delivered two times as many functions per chip every 1.5–2 years with no or only a moderate increase in chip size and cost (approximately constant cost per cm^2 of silicon). This technological and economic performance is the fundamental engine behind the growth of the semiconductor industry.

However, the customers in today's competitive market environment are resistant to even "moderate" increases in cost and the rate of doubling functions per chip (Moore's Law) is slowing. Therefore, the semiconductor manufacturers must seek a new model to deliver the same cost-per-function reduction requirements that have fueled industry growth. Consequently, the *1999 ITRS* proposed a new model for achieving the required reduction: provide the customer twice the functionality every two years at a constant cost and average selling price (ASP) per chip. The *2001 ITRS* uses the model and results in the same 29% cost reduction of a function (bit, transistor, etc.) that has been achieved historically by delivering four times the functionality per chip every three years at 1.4× increase in cost per unit. The DRAM and MPU cost models continue to use the need for that 29% cost-per-function productivity reduction rate as an economic driver of the industry. Therefore, that core cost-per-function trend has been used to set the INTRA-generation trends for the affordable cost/bit and cost/transistor for DRAM and microprocessors, respectively. Extrapolation of historical trends would indicate an "at introduction" affordable cost/bit of approximately 21 microcents for 2-Gbit DRAMs in 2001. In addition, the historical trends indicate that, within a DRAM generation, a 45%/year reduction in cost/bit should be expected.[2] A corresponding analysis conducted from published data for microprocessors yields similar results.[3] As a result the 29%/year target for reduction in affordable cost/transistor from generation to generation is also being used in the MPU model , along with the 45%/year reduction rate within the same generation.

However, the Design ITWG has updated the MPU model, based upon recent data. The new data indicates that logic transistor size is improving only at the rate of the lithography (0.7× linear, 0.5×area reduction every technology node). Therefore in order to keep the MPU chip sizes flat, the number of transistors can be doubled only every technology node. The technology node rate is projected to return to a three-year cycle after 2001, therefore the transistors per MPU chip can double only every three years after 2001. DRAM memory bit cell design improvements are also slowing down, and the rate of bits per chip will also be slowing in the future to keep chip sizes under control. To compensate for slowing DRAM and MPU functions-per-chip, there will be increasing pressure to find alternative productivity enhancements from the equivalent productivity scaling benefits of chip and system-level architecture and designs.

Even though the rate of increase of on-chip functionality could slow in the future, the amount of functions/chip is still growing exponentially. As the number of functions/chip continues to increase, it becomes increasingly difficult and, therefore, costly to test the final products. This is reflected in the escalating cost of testers. Even though the cost/pin of testers is forecast to decline between 0% and 10% per year (Tables 7 a and b), the number of pins grows at 10%year (Tables 4 a and b). Therefore, the need for accelerated implementation of Built-In-Self-Test (BIST) and Design-For-Testability (DFT) techniques will continue within the time frame of the 2001 International Technology Roadmap for Semiconductors. Further discussion is detailed in the *Test* chapter.

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[2] *McClean, William J., ed. Mid-Term 1994:* Status and Forecast of the IC Industry. *Scottsdale: Integrated Circuit Engineering Corporation, 1994.*

McClean, William J., ed. Mid-Term 1995: Status and Forecast of the IC Industry. *Scottsdale: Integrated Circuit Engineering Corporation, 1995.*

[3] *a) Dataquest Incorporated.* x86 Market: Detailed Forecast, Assumptions, and Trends. *MCRO–WW–MT–9501. San Jose: Dataquest Incorporated, January 16, 1995.*

b) Port, Otis; Reinhardt, Andy; McWilliams, Gary; and Brull, Steven V. "The Silicon Age? It's Just Dawning," Table 1. Business Week, *December 9, 1996, 148–152.*

Table 7a Cost—Near-term Years

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	**130**	**115**	**100**	**90**	**80**	**70**	**65**
MPU/ASIC ½ Pitch (nm)	**150**	**130**	**107**	**90**	**80**	**70**	**65**
MPU Printed Gate Length (nm)	**90**	**75**	**65**	**53**	**45**	**40**	**35**
MPU Physical Gate Length (nm)	**65**	**53**	**45**	**37**	**32**	**28**	**25**
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	**21**	**14.8**	**10.5**	**7.4**	**5.3**	**3.7**	**2.6**
DRAM cost/bit at (packaged microcents) at production §	**7.7**	**5.4**	**3.8**	**2.7**	**1.9**	**1.4**	**0.96**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**176**	**124**	**88**	**62**	**44**	**31**	**22**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**107**	**75**	**53**	**38**	**27**	**19**	**13.3**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**97**	**69**	**49**	**34**	**24**	**17**	**12**
Cost-Per-Pin							
Test Cost							
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	**4.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**

Notes for Tables 7a and 7b

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two-four years after introduction).

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows 1999–2002/8×; 2003–2010/6×; 2011–2016/4×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1) *at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4×/five years (2×/two–three years); and*
2) *at the Production phase, after the interim 32Gbit generation, the introduction rate is 4×/five years (2×/two–three years).*

InTER-generation chip size growth rate varies to maintain one chip per 572mm^2 field at Introduction and two chips per 572mm^2 field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2× bits/chip every two years and still fit within the target of two DRAM chips per 572mm^2 field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2016, made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model is 0.5× every two-year technology node through 2001, then 0.5× every three-year technology node after 2001.

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Table 7b Cost—Long-term Years

Year of Production	*2010*	*2013*	*2016*
DRAM ½ Pitch (nm)	**45**	**32**	**22**
MPU/ASIC ½ Pitch (nm)	**45**	**32**	**22**
MPU Printed Gate Length (nm)	**25**	**18**	**13**
MPU Physical Gate Length (nm)	**18**	**13**	**9**
Affordable Cost per Function ++			
DRAM cost/bit (packaged microcents) at samples/introduction	**0.93**	**0.33**	**0.12**
DRAM cost/bit (packaged microcents) at production §	**0.34**	**0.12**	**0.042**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**7.78**	**2.75**	**0.97**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**4.71**	**1.66**	**0.59**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**4.31**	**1.52**	**0.54**
Cost-Per-Pin			
Test Cost			
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	**4**	**4**	**4**
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	**2**	**3**	**4**

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FOLDER 7

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

Table 34 Process Integration Difficult Challenges [Update]

	Difficult Challenges ≥ 65nm / Through 2007	*Summary of Issues*
Was	1. High-performance applications: meeting performance and power dissipation requirements for highly scaled MOSFETs.	– Cost effectiveness, process control, and reliability of very thin oxy-nitride gate dielectrics, especially considering the high gate leakage. – Implementation of metal gate electrode by about 2007. – Need to reduce series S/D parasitic resistance. – Controlling static power dissipation in the face of rapidly increasing leakage. – Architecture and circuit design improvement and innovation will be needed
Is	1. High-performance applications: meeting performance and power dissipation requirements for highly scaled MOSFETs.	– Cost effectiveness, process control, and reliability of very thin oxy-nitride gate dielectrics, especially considering the high gate leakage. – Implementation of metal gate electrode **and high κ gate dielectric** by about 2007. – Need to reduce series S/D parasitic resistance. – Controlling static power dissipation in the face of rapidly increasing leakage. – Architecture and circuit design improvement and innovation will be needed
	2. Low-power applications: meeting performance and leakage requirements for highly scaled MOSFETs.	– Early availability of manufacturing-worthy high κ gate dielectrics is necessary to meet stringent gate leakage and performance requirements. – Very slow scaling of Vdd will make overall device scaling difficult.
	3. Implementation into manufacturing of non-classical MOSFET devices (for example, double-gate SOI).	– It is likely that these transistors will be necessary eventually to control short-channel and other effects in highly scaled devices. See Emerging Research Devices section, Non-classical CMOS, for more detail.
	4. Ensuring reliability of new materials and structures in a timely manner.	– Accelerated reliability ensurance of high κ material for gate stack will be needed for early insertion into manufacturing. – Ensuring reliability of new gate electrode materials will be a challenge. – Ensuring reliability of new, non-classical CMOS structures will be a challenge. – Ensuring reliability of very thin oxy-nitrides with very high leakage current will be critical for high-performance applications. – Difficulty of screening with high leakage currents
	5. Constructing DRAM, SRAM, and high density nonvolatile memory (NVM) for scaled technologies	– DRAM main issues: adequate storage capacitance for devices with reduced feature size; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs. Also, the availability of manufacturing worthy 193 nm lithography and integrated DRAM etch capability for 100 nm half pitches in 2003. – SRAM: difficult lithography and etch as well as process integration issues. – NVM: very difficult scaling issues with tunnel and interpoly dielectrics.
	6. High-performance mixed-signal solutions for scaled technologies.	– Passive element scaling: embedded inductor densities and Q factor values. – Signal isolation. – Optimizing RF CMOS devices with scaled technologies: gate leakage is a particularly sensitive issue. – Transition to reduced analog supply voltages. – Difficulty and cost of integrating analog/RF and high-performance digital functions on a chip.

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Table 34 Process Integration Difficult Challenges [Update] (continued)

Difficult Challenges < 65 nm, Beyond 2007	*Summary of Issues*
7. Fundamental improvements in MOSFET device effective transconductance needed to maintain device performance scaling trend.	– With sharp reductions in V_{dd} and 17% annual increase in intrinsic transistor speed, basic MOSFET device performance will be inadequate to meet circuit speed requirements.
8. Dealing with atomic-level fluctuations and statistical process variations in sub-30 nm MOSFETs.	– Fundamental problems of atomic-level statistical fluctuations are not completely understood.
9. New interconnect schemes	– Eventually, copper/low κ performances will be inadequate. – Solutions (optical, microwave/RF, etc,) are currently unclear.
10 Toward the end of the Roadmap or beyond, implementation of advanced non-CMOS devices and architectures, including memory.	– Will drive major changes in process, materials, physics, design, etc. – Non-CMOS devices may coexist with CMOS: integration of the two will be difficult, especially for mixed signal. – See Emerging Research Devices sections for more discussion and detail.

Table 35a High-performance Logic Technology Requirements—Near-term

	Year of Production	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
	Physical gate length high-performance (HP) (nm) [1]	65	53	45	37	32	28	25
Was	Equivalent physical oxide thickness for high-performance T_{ox} (EOT)(nm) [2]	1.3–1.6	1.2–1.5	1.1–1.6	0.9–1.4	0.8–1.3	0.7–1.2	0.6–1.1
Is	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	1.3–1.6	1.2–1.5	1.1–1.6	0.9–1.4	0.8–1.3	0.7–1.2	0.6–1.1
	Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]	0.8	0.8	0.8	0.8	0.8	0.8	0.5
Was	T_{ox} electrical equivalent (nm) [4]	2.3	2.1	2	2	1.9	1.9	1.4
Is	Equivalent oxide thickness (electrical) (nm) [4]	2.3	2.1	2	2	1.9	1.9	1.4
	Nominal power supply voltage (V_{dd}) (V) [5]	1.2	1.1	1	1	0.9	0.9	0.7
	Nominal high-performance NMOS sub-threshold leakage current, Isd,leak (at 25° C) (μA/μm) [6]	0.01	0.03	0.07	0.1	0.3	0.7	1
	Nominal high-performance NMOS saturation drive current, I_{dd} (at V_{dd}, at 25° C) (μA/μm) [7]	900	900	900	900	900	900	900
	Required percent current-drive "mobility/transconductance improvement" [8]	0%	0%	0%	0%	0%	0%	0%
	Parasitic source/drain resistance (Rsd) (ohm-μm) [9]	190	180	180	180	180	170	140
	Parasitic source/drain resistance (Rsd) percent of ideal channel resistance (V_{dd}/I_{dd}) [10]	16%	16%	17%	18%	19%	19%	20%
	Parasitic capacitance percent of ideal gate capacitance [11]	19%	22%	24%	27%	29%	32%	27%
	High-performance NMOS device τ (C_{gate} * V_{dd} / I_{dd}-NMOS)(ps) [12]	1.6	1.3	1.1	0.99	0.83	0.76	0.68
	Relative device performance [13]	1	1.2	1.5	1.6	2	2.1	2.5
Was	Energy per (W/L_{gate}=3) device switching transition (C_{gate}*(3*L_{gate})*V^2) (fJ/Device) [14]	0.347	0.212	0.137	0.099	0.065	0.052	0.032
Is	Power-delay product for (W/L_{gate}=3) device [C_{gate}*(3*L_{gate})*V_{dd}^2] (fJ/Device) [14]	0.347	0.212	0.137	0.099	0.065	0.052	0.032
	Static power dissipation per (W/Lgate=3) device (Watts/Device) [15]	5.60E-09	6.70E-09	1.00E-08	1.10E-08	2.60E-08	5.30E-08	5.30E-08

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



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Table 35b High-performance Logic Technology Requirements—Long-term

	Year of Production	2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU / ASIC ½ Pitch (nm)	50	35	25
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	Physical gate length high-performance (HP) (nm) [1]	18	13	9
Was	Equivalent physical oxide thickness for high-performance T_{ox} (EOT) (nm) [2]	0.5-0.8	0.4-0.6	0.4-0.5
Is	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	0.5-0.8	0.4-0.6	0.4-0.5
	Gate depletion and quantum effects electrical thickness adjustment factor (nm) [3]	0.5	0.5	0.5
Was	T_{ox} electrical equivalent (nm) [4]	1.2	1	0.9
Is	Equivalent oxide thickness (electrical) (nm) [4]	1.2	1	0.9
	Nominal power supply voltage (V_{dd}) (V) [5]	0.6	0.5	0.4
	Nominal high-performance NMOS sub threshold leakage current, $I_{sd\ leak}$ (at 25 °C) (μA/μm) [6]	3	7	10
	Nominal high-performance NMOS saturation drive current , I_{dd} (at V_{dd}, at 25 °C) (μA/μm) [7]	1200	1500	1500
	Required percent current-drive "mobility/transconductance improvement" [8]	30%	70%	100%
	Parasitic source/drain resistance (Rsd) (ohm-μm) [9]	110	90	80
	Parasitic source/drain resistance (Rsd) percent of ideal channel resistance (V_{dd}/I_{dd}) [10]	25%	30%	35%
	Parasitic capacitance percent of ideal gate capacitance [11]	31%	36%	42%
	High-performance NMOS device τ (C_{gate} * V_{dd} / I_{dd}-NMOS)(ps) [12]	0.39	0.22	0.15
	Relative device performance [13]	4.3	7.2	10.7
Was	Energy per (W/L_{gate}=3) device switching transition (C_{gate}*(3*L_{gate})*V^2) (fJ/Device) [14]	0.015	0.007	0.002
Is	Power-delay product for (W/L_{gate}=3) device [C_{gate}*(3*L_{gate})*V_{dd}^2] (fJ/Device) [14]	0.015	0.007	0.002
	Static power dissipation per (W/Lgate=3) device (Watts/Device) [15]	9.70E-08	1.40E-07	1.10E-07

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



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Notes for Table 35a and b:

[1] Values set by ORTC. Gate dimensional control is set by the Lithography and FEP Etch ITWGs, and is assumed to have a three sigma value of ± 10%. Gate dimension variation is assumed to be the primary factor responsible for driving device parameter variation.

Was *[2] EOT range set by FEP TWG. Yellow/red feasibility coloring set by FEP TWG projections on thickness control and reliability capability. Calculations in rest of PIDS table (and the underlying PIDS workbook) based on approximate midpoint EOT values.*

Is *[2] EOT range set by FEP TWG. Yellow/red feasibility coloring set by FEP TWG projections on thickness control and reliability capability. Calculations in rest of PIDS table (and the underlying PIDS workbook) based on approximate midpoint EOT values.* ***For a gate dielectric of thickness*** **T_d** ***and relative dielectric constant*** **k, EOT is defined by: EOT = Td / (k/3.9),** ***where 3.9 is the relative dielectric constant of thermal silicon dioxide. The ideal gate capacitance per unit area of the gate dielectric of thickness Td is the same as that of a gate dielectric made up of thermal silicon dioxide with a thickness of EOT.***

[3] Accounts for gate electrode depletion and inversion-layer quantum effects. Yellow feasibility coloring reflects FEP assessment of polysilicon doping capability; red feasibility coloring reflects the introduction of metal-gate electrodes by 2007 (which reduces the gate depletion value).

[4] Sum of midpoint EOT and Electrical Thickness Adjustment Factor. Used in CV/I performance metric and CV^2 dynamic power metric calculations. Red/yellow feasibility coloring determined by worst-case EOT and Electrical Thickness Adjustment Factor red/yellow feasibility coloring.

Was *[5] Nominal power supply voltage has been set to maintain sufficient voltage over-drive to continue historical approximate 17% per year device performance scaling while still enabling approximate 30% per year switching energy reduction and still maintaining reasonable vertical gate dielectric electric field strengths. Actual power supply voltage values may vary +/- 10%, depending on the particular circuit design application or technology optimization.*

Is *[5] Nominal power supply voltage has been set to maintain sufficient voltage over-drive to continue historical approximate 17% per year device performance scaling while still enabling approximate 30% per year switching energy reduction and still maintaining reasonable vertical gate dielectric electric field strengths. Actual* ***target*** *power supply voltage values may vary +/- 10%, depending on the particular circuit design application or technology optimization.*

[6] Nominal sub-threshold leakage current is defined as the NMOSFET source current at room temperature with the drain bias set equal to the nominal power-supply voltage and with the gate, source and substrate biases set to zero volts; all MOSFET device dimensions are assumed to be at their nominal/target values. Total NMOS off-state current is the NMOSFET drain current at room temperature, and is the sum of the NMOS sub-threshold, gate, and junction leakage current components. The sub-threshold leakage current is assumed to be larger than either the gate or junction leakage current components at either room or high-temperature conditions. The threshold voltage value (and the corresponding sub-threshold current) has been set to maintain sufficient voltage over-drive to continue historical approximate 17% per year device performance scaling. Yellow feasibility coloring by 2007 reflects the potential need for non-classical CMOS or ultra-shallow junction technology in order to control short-channel and/or high-field effects (See Emerging Research Devices section). The above sub-threshold, gate, and junction current scaling scenario also applies to PMOS devices. Note, sub-threshold current value applies to fastest MOS devices only; slower/lower-leakage MOS devices will also be available. Future systems will consist of a mix of both high and lower-leakage devices.

[7] Nominal saturation current drive is defined as the MOSFET drain current at room temperature with the gate bias and the drain bias set equal to the nominal power-supply voltage; all MOSFET device dimensions are assumed to be at their nominal/target values. Nominal PMOS saturation current-drive value is assumed to be 40-50% of the nominal NMOS saturation current-drive value. Yellow/red feasibility coloring indicates the projected need for fundamental device current-drive (or transconductance/mobility) improvement by 2010 in order to continue historical approximate 17% per year device performance scaling. NMOS/PMOS current-drive targets are approximate with only 1.5 significant digits of accuracy.

[8] Fundamental device mobility/transconductance improvement needed by 2010 in order to continue historical approximate 17% per year device performance scaling. Yellow/red feasibility coloring indicates the difficulty in implementing fundamental device current-drive (transconductance/mobility) improvement required in 2010 and later to continue historical approximate 17% per year device performance scaling.

Was *[9] Total parasitic device source/drain resistance Rsd (sum of the source and drain parasitic resistances). Rsd targets are consistent with FEP TWG projections. Yellow/red feasibility coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling. Similar Rsd values are assumed for the LOP and LSTP devices.*

Is *[9]* ***Maximum allowable*** *parasitic device source/drain resistance Rsd (sum of the source and drain parasitic resistances). Rsd targets are consistent with FEP TWG projections. Yellow/red feasibility coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling. Similar Rsd values are assumed for the LOP and LSTP devices.*

Was *[10] Maximum ratio of the parasitic device source/drain resistance (Rsd) to the ideal channel resistance (Vdd/Idd). Rsd targets are consistent with FEP TWG projections. Yellow/red feasibility coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.*

Is *10]* ~~***Maximum***~~ *Ratio of the parasitic device source/drain resistance (Rsd) to the ideal channel resistance (Vdd/Idd). Rsd targets are consistent with FEP TWG projections. Yellow/red feasibility coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.*

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Notes for Table 35a and b(continued)

Was

[11] Maximum ratio of the parasitic gate overlap/fringing capacitance to the ideal gate capacitance. Assume constant C-parasitic value of 2.4E-16F/um. [3× the fringing capacitance value per side, including the Miller effect]; this value is assumed to be independent of bias conditions and/or technology. Parasitic capacitance factor is included in CV/I and CV^2 performance and power metric calculations. Similar parasitic capacitance values are assumed for the LOP and LSTP devices.

Is

11] ~~Maximum~~ ratio of the parasitic gate overlap/fringing capacitance to the ideal gate capacitance. Assume constant C-parasitic value of 2.4E-16F/um. [3× the fringing capacitance value per side, including the Miller effect]; this value is assumed to be independent of bias conditions and/or technology. Parasitic capacitance factor is included in CV/I and CV^2 performance and power metric calculations. Similar parasitic capacitance values are assumed for the LOP and LSTP devices.

[12] τ = CV/I intrinsic delay metric for NMOS device; PMOS CV/I metric assumed to scale proportionally. The CV/I metric provides an indication of the intrinsic switching delay of the device, while $1/\tau$, the reciprocal of CV/I, is a good metric for the intrinsic switching speed of the device. Red/yellow feasibility coloring determined by worst-case saturation current-drive feasibility coloring.

[13] Improvement in $1/\tau$ NMOS performance metric normalized to the year 2001. Maintains historical approximate 17% per year device performance improvement scaling trend. Red/yellow feasibility coloring determined by worst-case, saturation current-drive feasibility coloring.

Was

[14] CV^2 switching energy metric for an NMOS device with dimensions W/Lgate=3. The switching energy metric indicates the amount of dynamic power required to switch the device. Maintains approximate 30% per year device switching energy reduction scaling trend. Red/yellow feasibility coloring determined by worst-case saturation current-drive feasibility and mobility/transconductance improvement feasibility coloring.

Is

*14] CV^2 switching energy metric for an NMOS device with dimensions W/Lgate=3. **The power-delay product** indicates the amount of dynamic **energy** required to switch the **device through a full (up and down) transition**. Maintains approximate 30% per year device switching energy reduction scaling trend. Red/yellow feasibility coloring determined by worst-case saturation current-drive feasibility and mobility/transconductance improvement feasibility coloring.*

[15] Static power dissipation for an NMOS device with dimensions W/Lgate=3. Assume that the device static power is primarily determined by the sub-threshold current (since the other junction and leakage current components are assumed to be lower). Yellow feasibility coloring by 2007 reflects the potential need for non-classical CMOS or ultra-shallow junction technology in order to control short-channel and/or high-field effects (See Emerging Research Devices section, Non-classical CMOS).

Table 36a Low Operating Power (LOP) Logic Technology Requirements—Near-term

	Year of Production	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
	Physical gate length low-operating power (LOP) (nm) [1]	90	75	65	53	45	37	32
Was	Equivalent physical oxide thickness for LOP T_{ox} (EOT) (nm) [2]	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4
Is	EOT: equivalent oxide thickness (physical) for LOP (nm) [2]	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4
	Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.8	0.8	0.8	0.8	0.8	0.8	0.5
Was	T_{ox} electrical equivalent (nm) [4]	3	2.8	2.6	2.4	2.2	2.1	1.7
Is	Equivalent oxide thickness (electrical) (nm) [4]	3	2.8	2.6	2.4	2.2	2.1	1.7
	Nominal LOP power supply voltage (V_{dd}) (V) [5]	1.2	1.2	1.1	1.1	1	1	0.9
	Nominal LOP NMOS sub-threshold leakage current, $I_{sd\ leak}$ (@25C) (pA/μm) [6]	100	100	100	300	300	300	700
	Nominal LOP NMOS Saturation drive current, I_{dd} (@V_{dd}, @25C) (μA/μm) [7]	600	600	600	600	600	600	700
	Required percent current-drive "mobility/transconductance improvement" [8]	0%	0%	0%	0%	0%	0%	0%
	LOP NMOS Device τ (C_{gate} * V_{dd} / Id-NMOS) (ps) [9]	2.55	2.45	2.02	1.84	1.58	1.41	1.14
	LOP relative device performance [10]	1	1.04	1.3	1.4	1.6	1.8	2.2
Was	Energy per (W/L_{gate}=3) device switching transition (Cgate*(3*Lgate)*V^2) (fJ/Device) [11]	0.496	0.424	0.26	0.193	0.128	0.094	0.069
Is	Power-delay product for (W/L_{gate}=3) device [C_{gate}*(3*L_{gate})*V_{dd}^2] (fJ/Device) [14]	0.496	0.424	0.26	0.193	0.128	0.094	0.069
	Static power dissipation per (W/L_{gate}=3) device (Watts/device) [12]	3.20E-11	2.90E-11	2.10E-11	5.20E-11	4.10E-11	3.30E-11	6.00E-11

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



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Table 36b Low Operating Power (LOP) Logic Technology Requirements—Long-term

	Year of Production	2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU / ASIC ½ Pitch (nm)	50	35	25
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	Physical gate length low-operating power (LOP) (nm) [1]	22	16	11
Was	Equivalent physical oxide thickness for LOP T_{ox} (EOT) (nm) [2]	0.8-1.2	0.7-1.1	0.6-1.0
Is	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	0.8-1.2	0.7-1.1	0.6-1.0
	Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.5	0.5	0.5
Was	T_{ox} electrical equivalent (nm) [4]	1.5	1.4	1.3
Is	Equivalent oxide thickness (electrical) (nm) [4]	1.5	1.4	1.3
	Nominal LOP power supply voltage (V_{dd}) (V) [5]	0.8	0.7	0.6
	Nominal LOP NMOS sub-threshold leakage current, $I_{sd\ leak}$ (@25C) (pA/μm) [6]	1000	3000	10000
	Nominal LOP NMOS saturation drive current, I_{dd} (@V_{dd}, @25C) (μA/μm) [7]	700	800	900
	Required percent current-drive "mobility/transconductance improvement" [8]	10%	30%	70%
	LOP NMOS device τ (C_{gate} * V_{dd} / I_{dd}-NMOS) (ps) [9]	0.85	0.56	0.35
	LOP relative device Performance [10]	3	4.6	7.2
Was	Energy per (W/L_{gate}=3) device switching transition (C_{gate}*(3*L_{gate})*V^2) (fJ/Device) [11]	0.032	0.015	0.006
Is	Power-delay product for (W/L_{gate}=3) device [C_{gate}*(3*L_{gate})*V_{dd}^2] (fJ/Device) [14]	0.032	0.015	0.006
	Static power dissipation per (W/Lgate=3) device (Watts/Device) [12]	5.30E-11	1.00E-10	2.00E-10

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



Table 36c Low Standby Power (LSTP) Technology Requirements—Near-term

	Year of Production	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Was	Physical gate length low-standby power (LSTP) (nm) [1]	90	75	65	53	45	37	32
Is	Physical gate length low-standby power (LSTP) (nm) [1]	100	90	75	65	53	45	37
Was	Equivalent physical oxide thickness for LSTP T_{ox} (EOT) (nm) [2]	2.4–2.8	2.2–2.6	2.0–2.4	1.8–2.2	1.6–2.0	1.4–1.8	1.2–1.6
Is	EOT: equivalent oxide thickness (physical) for LOP (nm) [2]	2.4–2.8	2.2–2.6	2.0–2.4	1.8–2.2	1.6–2.0	1.4–1.8	1.2–1.6
	Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.8	0.8	0.8	0.8	0.8	0.8	0.5
Was	T_{ox} electrical equivalent (nm) [4]	3.4	3.2	3	2.8	2.6	2.4	1.9
Is	Equivalent oxide thickness (electrical) (nm) [4]	3.4	3.2	3	2.8	2.6	2.4	1.9
	Nominal LSTP power supply voltage (V_{dd}) (V) [5]	1.2	1.2	1.2	1.2	1.2	1.2	1.1
	Nominal LSTP NMOS sub-threshold current (at 25° C) (pA/μm) [6]	1	1	1	1	1	1	1
	Nominal LSTP NMOS saturation current drive (I_{dd}) (at V_{dd}, at 25° C) (mA/μm) [7]	300	300	400	400	400	400	500
	Required percent current-drive "mobility/transconductance improvement" [8]	0%	0%	0%	0%	0%	0%	0%
Was	LSTP NMOS device τ (C_{gate} * V_{dd} / Id-NMOS) (ps) [9]	4.61	4.41	2.96	2.68	2.51	2.32	1.81
Is	LSTP NMOS device τ (C_{gate} * V_{dd} / Id-NMOS) (ps) [9]	5.02	4.84	3.31	3.12	2.83	2.66	2.01
Was	LSTP relative device performance [10]	1	1.05	1.6	1.7	1.8	2	2.6
Is	LSTP relative device performance [10]	1	1.04	1.52	1.61	1.77	1.89	2.50
Was	Energy per (W/L_{gate}=3) device switching transition (C_{gate}*(3*L_{gate})*V^2) (fJ/device) [11]	0.448	0.381	0.277	0.204	0.163	0.123	0.095
Is	Power-delay product for (W/L_{gate}=3) device [C_{gate}*(3*L_{gate})*V_{dd}^2] (fJ/Device) [14]	0.542	0.471	0.357	0.292	0.216	0.172	0.122
Was	Static power dissipation per (W/L_{gate}=3) device (Watts/device) [12]	3.20E-13	2.90E-13	2.30E-13	1.90E-13	1.60E-13	1.30E-13	1.10E-13
Is	Static power dissipation per (W/L_{gate}=3) device (Watts/device) [12]	3.60E-13	3.24E-13	2.70E-13	2.34E-13	1.91E-13	1.62E-13	1.22E-13

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



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Table 36d Low Standby Power (LSTP) Technology Requirements—Long-term

	Year of Production	2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU / ASIC ½ Pitch (nm)	50	35	25
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
Was	Physical gate length low-standby power (LSTP) (nm) [1]	22	16	11
Is	Physical gate length low-standby power (LSTP) (nm) [1]	28	20	16
Was	Equivalent physical oxide thickness for LSTP T_{ox} (EOT) (nm) [2]	0.9-1.3	0.8-1.2	0.7-1.1
Is	EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	0.9-1.3	0.8-1.2	0.7-1.1
	Electrical thickness adjustment factor (gate depletion and quantum effects) (nm) [3]	0.5	0.5	0.5
Was	T_{ox} electrical equivalent (nm) [4]	1.6	1.5	1.4
Is	Equivalent oxide thickness (electrical) (nm) [4]	1.6	1.5	1.4
	Nominal LSTP power supply voltage (V_{dd}) (V) [5]	1	0.9	0.9
	Nominal LSTP NMOS sub-threshold current (at 25 °C) (pA/µm) [6]	3	7	10
	Nominal LSTP NMOS saturation current drive (Idd) (at V_{dd} at 25° C) (µA/µm) [7]	500	600	700
	Required percent current-drive "mobility/transconductance improvement" [8]	10%	30%	50%
Was	LSTP NMOS device τ (C_{gate} * V_{dd} / Id-NMOS) (ps) [9]	1.43	0.91	0.66
Is	LSTP NMOS device τ (C_{gate} * V_{dd} / Id-NMOS) (ps) [9]	1.69	1.05	0.82
Was	LSTP relative device performance [10]	3.2	5.1	7
Is	LSTP relative device performance [10]	2.97	4.78	6.15
Was	Energy per (W/L_{gate}=3) device switching transition (Cgate*(3*Lgate)*V^2) (fJ/device) [11]	0.047	0.024	0.014
Is	Power-delay product for (W/L_{gate}=3) device [C_{gate}*(3*L_{gate})*V_{dd}^2] (fJ/Device) [14]	0.071	0.034	0.025
Was	Static power dissipation per (W/L_{gate}=3) device (Watts/device) [12]	2.00E-13	3.00E-13	3.00E-13
Is	Static power dissipation per (W/L_{gate}=3) device (Watts/device) [12]	2.52E-13	3.78E-13	4.32E-13

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



Notes for Table 36a through d

[1] Values set by ORTC.

[1] Values set by ORTC. Assumed to lag high-performance scaling by 2 years. Gate dimensional control is set by the Lithography and FEP (Etch) ITWGs and is assumed to have a three sigma value of ±10%. Gate dimension variation is assumed to be the primary factor responsible for driving device parameter variation. Gate length for the LOP and LSTP devices are assumed to be identical.

Was

[2] EOT value set by FEP ITWG in the Front End Processes chapter, Thermal and Thin Film, Doping, and Etching Technology Requirements tables Yellow/red feasibility coloring set by FEP ITWG projections on gate leakage, thickness control and reliability capability (high κ gate dielectrics will be required around 2005 in order to suppress gate leakage for LSTP). Due to different system applications, the EOT values for the LOP and LSTP devices have been optimized and set independently of each other. Calculations in rest of PIDS table (and the underlying PIDS workbook) based on approximate midpoint EOT values

Is

[2]] EOT value set by FEP ITWG in the Front End Processes chapter, Thermal and Thin Film, Doping, and Etching Technology Requirements tables Yellow/red feasibility coloring set by FEP ITWG projections on gate leakage, thickness control and reliability capability (high κ gate dielectrics will be required around 2005 in order to suppress gate leakage for LSTP). Due to different system applications, the EOT values for the LOP and LSTP devices have been optimized and set independently of each other. Calculations in rest of PIDS table (and the underlying PIDS workbook) based on approximate midpoint EOT values. ***For a gate dielectric of thickness T_d and relative dielectric constant k, EOT is defined by: EOT = Td / (k/3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide. The ideal gate capacitance per unit area of the gate dielectric of thickness Td is the same as that of a gate dielectric made up of thermal silicon dioxide with a thickness of EOT.***

[3] Accounts for gate electrode depletion and inversion-layer quantum effects. Yellow feasibility coloring reflects FEP assessment of polysilicon doping capability; red feasibility coloring reflects the introduction of metal-gate electrodes by 2007 (which reduces the gate depletion value).

[4] Sum of midpoint EOT and Electrical Thickness Adjustment Factor. Used in CV/I performance metric and CV^2 dynamic power metric calculations. Red/yellow feasibility coloring determined by worst-case EOT and Electrical Thickness Adjustment Factor red/yellow feasibility coloring.

Was

[5] Nominal power supply voltage which has been set to smallest value to still maintain sufficient voltage over-drive to allow sufficient circuit switching noise margin (approximately 2.3 times the threshold voltage). Actual power supply voltage values may vary ± 10%, depending on the particular circuit design application or technology optimization. Due to different system applications, the power-supply voltages for the LOP and LSTP devices have been optimized and set independently of each other. Note, meeting overall system power dissipation requirements will require the use of circuit/system techniques to "turn-off" or "power-down" various circuit blocks.

Is

[5] Nominal power supply voltage ~~*which*~~ *has been set to smallest value to still maintain sufficient* ~~*voltage over-drive to allow sufficient*~~ *circuit switching noise margin (approximately 2.3 times the threshold voltage). Actual power supply voltage target values may vary ± 10%, depending on the particular circuit design application or technology optimization. Due to different system applications, the power-supply voltages for the LOP and LSTP devices have been optimized and set independently of each other. Note, meeting overall system power dissipation requirements will require the use of circuit/system techniques to "turn-off" or "power-down" various circuit blocks.*

Was

[6] Nominal sub-threshold leakage current is defined as the NMOSFET source current at room temperature with the drain bias set equal to the nominal power-supply voltage and with the gate, source, and substrate biases set to zero volts; all MOSFET device dimensions are assumed to be at their nominal/target values. Total NMOS off-state current is the NMOSFET drain current at room temperature, and is the sum of the NMOS sub-threshold, gate, and junction leakage current components. The sub-threshold leakage current is assumed to be larger than either the gate or junction current components at either room or high-temperature conditions. The increase in sub-threshold current (and the corresponding threshold-voltage value reduction) has been set at a pace that lags the rate of increase of the high-performance device, but that still increases sufficiently to enable continued device performance scaling; power dissipation due to off-state leakage is assumed to not exceed 10% of the total chip power, which is assumed to be 100mW in 2001 and 200mW in 2010 for LOP. For LOP, the yellow feasibility coloring reflects the difficulty of meeting the gate leakage requirements with thin oxy-nitride films and the potential need for non-classical CMOS or ultra-shallow junction technology by 2007 to control short-channel effects and to limit lateral high-field effects. For LSTP, the yellow feasibility coloring in 2003 and 2004 reflects the difficulty of meeting the gate leakage requirements with thin oxy-nitride gate dielectric films, while the red feasibility color from 2005 on reflects the difficulty of implementing a high κ gate dielectric to meet the gate leakage requirements. The above sub-threshold, gate, and junction current scaling scenario also applies to PMOS devices.

Is

[6]] Nominal sub-threshold leakage current is defined as the NMOSFET source current at room temperature with the drain bias set equal to the nominal power-supply voltage and with the gate, source, and substrate biases set to zero volts; all MOSFET device dimensions are assumed to be at their nominal/target values. Total NMOS off-state current is the NMOSFET drain current at room temperature, and is the sum of the NMOS sub-threshold, gate, and junction leakage current components. The sub-threshold leakage current is assumed to be larger than either the gate or junction current components at either room or high-temperature conditions. The increase in sub-threshold current (and the corresponding threshold-voltage ~~*value*~~ *reduction) has been set at a pace that lags the rate of increase of the high-performance device, but that still increases sufficiently to enable continued device performance scaling; power dissipation due to off-state leakage is assumed to not exceed 10% of the total chip power, which is assumed to be 100mW in 2001 and 200mW in 2010 for LOP. For LOP, the yellow feasibility coloring reflects the difficulty of meeting the gate leakage requirements with thin oxy-nitride films and the potential need for non-classical CMOS or ultra-shallow junction technology by 2007 to control short-channel effects and to limit lateral high-field effects. For LSTP, the yellow feasibility coloring in 2003 and 2004 reflects the difficulty of meeting the gate leakage requirements with thin oxy-nitride gate dielectric films, while the red feasibility color from 2005 on reflects the difficulty of implementing a high κ gate dielectric to meet the gate leakage requirements. The above sub-threshold, gate, and junction current scaling scenario also applies to PMOS devices.*

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Notes for Table 36a through d (continued)

[7] Nominal saturation current drive is defined as the MOSFET drain current at room temperature with the gate bias and the drain bias set equal to the nominal power-supply voltage; all MOSFET device dimensions are assumed to be at their nominal/target values. Nominal PMOS saturation current-drive value is assumed to be 40–50% of the nominal NMOS saturation current-drive value. Yellow/red feasibility coloring indicates the projected need for fundamental device current-drive (transconductance/mobility) improvement by 2010 in order to continue approximate 14% per year device performance scaling. NMOS/PMOS current-drive targets are approximate with only 1.5 significant digits of accuracy. The sub-threshold slope, parasitic source/drain resistance, and parasitic gate capacitance scaling have been assumed to be similar to that for the high-performance device. (See the enclosed Excel workbook for the detailed calculations).

[8] Fundamental device mobility/transconductance improvement needed by 2010 in order to continue historical approximate 14% per year device performance scaling. Yellow/red feasibility coloring indicates the difficulty of implementing the fundamental device current-drive (transconductance/mobility) improvement required in 2010 and beyond to continue historical approximate 14% per year device performance scaling. The LOP and LSTP required improvement is projected as lagging that required for the high-performance device.

Was	*[9] τ = CV/I intrinsic delay metric for NMOS device; PMOS CV/I metric assumed to scale proportionally. The CV/I metric provides an indication of the intrinsic switching delay of the device, while 1/τ, the reciprocal of CV/I, is a good metric for the intrinsic switching speed of the device. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring. The C term includes the effect of parasitic gate capacitance, which has been assumed to be equivalent to that for the high-performance device.*
Is	*[9]] τ = CV/I intrinsic delay metric for NMOS device; PMOS CV/I metric assumed to scale proportionally. The CV/I metric provides an indication of the intrinsic switching delay of the device, while 1/τ, the reciprocal of CV/I, is a good metric for the intrinsic switching speed of the device. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring. ~~The~~ C (gate capacitance) includes the effect of parasitic gate capacitance, which has been assumed to be equivalent to that for the high-performance device. For LSTP, τ has been adjusted to reflect the change in scaling of the physical gate length compared to the 2001 ITRS.*
Was	*[10] Improvement in 1/τ NMOS performance metric normalized to the year 2001. Maintains approximate 14% per year device performance improvement scaling trend for both LOP and LSTP. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring.*
Is	*10] [10] Improvement in 1/τ NMOS performance metric normalized to the year 2001. Maintains approximate 14% per year device performance improvement scaling trend for both LOP and LSTP. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring. For LSTP, 1/τ has been adjusted to reflect the change in scaling of the physical gate length compared to the 2001 ITRS.*
Was	*[11] CV^2 switching energy metric for an NMOS device with dimensions W/L_{gate}=3. The switching energy metric indicates the amount of dynamic power required to switch the device. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring.*
Is	*[11]] CV^2 switching energy metric for an NMOS device with dimensions W/L_{gate}=3. The power-delay product indicates the amount of dynamic energy required to switch the device through a full (up and down) transition. Red/yellow feasibility coloring determined by saturation current-drive feasibility coloring. For LSTP, the power-delay product has been adjusted to reflect the change in scaling of the physical gate length compared to the 2001 ITRS.*
Was	*[12] Static power dissipation for an NMOS device with dimensions W/L_{gate}=3. Assume that the device static power is primarily determined by the sub-threshold current (since the other junction and leakage current components are assumed to be lower). Yellow/red feasibility coloring is determined by the sub-threshold leakage current feasibility coloring.*
Is	*[12] Static power dissipation for an NMOS device with dimensions W/L_{gate}=3. Assume that the device static power is primarily determined by the sub-threshold current (since the other junction and leakage current components are assumed to be lower). Yellow/red feasibility coloring is determined by the sub-threshold leakage current feasibility coloring. For LSTP, the static power dissipation per device has been adjusted to reflect the change in scaling of the physical gate length compared to the 2001 ITRS.*

Table 37a DRAM Technology Requirements—Near-term

	Year of Production	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)[1]	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
	DRAM cell size (μm^2) [2]	0.135	0.106	0.06	0.049	0.038	0.029	0.025
	DRAM storage cell dielectric equivalent physical oxide thickness, EOT (nm) [3]	2.04	1.8	1.2	1	0.45	0.32	0.22
Was	DRAM retention time (ms) [4]	64	64	64	64	64	64	64
Is	Minimum DRAM retention time (ms) [4]	64	64	64	64	64	64	64
	DRAM soft error rate (fits) [5]	1000	1000	1000	1000	1000	1000	1000

Table 37b DRAM Technology Requirements—Long-term

	Year of Production	2010	2013	2016
	DRAM ½ Pitch (nm) [1]	45	32	22
	MPU / ASIC ½ Pitch (nm)	50	35	25
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	DRAM cell size (μm^2) [2]	0.0122	0.0041	0.0019
	DRAM storage cell dielectric equivalent physical oxide thickness, EOT (nm) [3]	0.084	0.028	0.01
Was	DRAM retention time (ms) [4]	64	64	64
Is	Minimum DRAM retention time (ms) [4]	64	64	64
	DRAM soft error rate (fits) [5]	1000	1000	1000

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



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Notes for Table 37a and b

Was	*[1] From ORTC (Overall Roadmap Technology Characteristics) Table 1a and b. These DRAM half pitch numbers are smaller than those in the 2000 ITRS, reflecting a speedup in technology development since 1999.*
Is	*[1]] From ORTC (Overall Roadmap Technology Characteristics) Table 1a and b. These DRAM half pitch numbers are smaller than those in the 2000 ITRS, reflecting a speedup in technology development since 1999.* ***However, there is no clear evidence for a further speed up in the pace of DRAM half pitch scaling during 2001 and the early part of 2002.***
Was	*[2] The DRAM cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and chip size numbers used by FEP are based on the ORTC tables 1a and 1b. Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled aggressively. The difficulty will lie in reducing the value of the cell size factor "a", where "a" equals (cell size /F^2). and F is the DRAM half pitch. The required values of "a" are 8 for the 130nm node, 6 for 100nm DRAM half pitch, and 4 for the 32nm node. The "a" value of 8 is probably achievable with current techniques, but the "a" value of 6 will require innovative solutions, as illustrated with yellow zone in this line, while the "a" value of 4 has no known solution for 32nm node and beyond, as illustrated with red zone.*
Is	*[2]] The DRAM cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and chip size numbers used by FEP are based on the ORTC tables 1a and 1b. Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled aggressively. The difficulty will lie in reducing the value of the cell size factor "a", where "a" equals (cell size /F^2). and F is the DRAM half pitch. The required values of "a" are 8 for the 130nm node, 6 for 100nm DRAM half pitch* ***in 2003****, and 4 for the 32nm node. The "a" value of 8 is probably achievable with current techniques, but the "a" value of 6 will require innovative solutions, as illustrated with yellow zone in this line,* ***and may be difficult for the industry to achieve per schedule in 2003****. The "a" value of 4 has no known solution for 32nm node and beyond, as illustrated with red zone.*
Was	*[3] The EOT is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and the chip size numbers used by FEP are from ORTC Tables 1a and 1b. Since the values of DRAM capacity and chip size from FEP are quite aggressive, the EOT must also be scaled very aggressively. For the 130nm through the 90 nm nodes, the dielectric material is based on Al_2O_3 or Ta_2O_5 with MIS structure, and hence the color is white Beyond the 90 nm node, breakthroughs such as MIM structure and higher κ material are needed, so the color is yellow. Finally, for the 65nm node and beyond, there are no known solutions with demonstrated credibility, and hence the color is red. The actual EOT required for each node also depends on the other factors such as cell height and/or 3D structure, film leakage current and contact formation. Trench capacitors have other requirements for the cell dielectric material.*
Is	*[3] The EOT is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and the chip size numbers used by FEP are from ORTC Tables 1a and 1b. Since the values of DRAM capacity and chip size from FEP are quite aggressive, the EOT must also be scaled very aggressively. For the 130nm through the 90 nm nodes, the dielectric material is based on Al_2O_3 or Ta_2O_5 with MIS structure, and hence the color is white.* ***(Note that, notwithstanding the trend to Al_2O_3 or Ta_2O_5, many vendors still used oxide-nitride-oxide (ONO) dielectric in 2001.)*** *Beyond the 90 nm node, breakthroughs such as MIM structure and higher κ material are needed, so the color is yellow. Finally, for the 65nm node and beyond, there are no known solutions with demonstrated credibility, and hence the color is red. The actual EOT required for each node also depends on the other factors such as cell height and/or 3D structure, film leakage current and contact formation. Trench capacitors have other requirements for the cell dielectric material.*

[4] Retention time is defined at 85 ºC, and is the minimum time during which the data from memory can still be sensed correctly without refreshing a row bit line. The 64 ms specified here is the value needed for PC applications. The retention time depends on the combined interaction of device leakage current, signal strength and signal sensing circuit sensitivity, and also depends on operational frequency and temperature.

[5] This is a typical FIT rate and depends on cycle time and the quality of cell capacitor and sensing circuits.

Table 38a Non-Volatile Memory Technology Requirements—Near-term

	Year of Production	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Was	Flash technology node - F (nm) [1]	150	130	115	100	90	80	70
Is	Flash technology node - F (nm) [1]	150	130	107	90	80	70	65
	Flash NOR cell size –area factor a in multiples of F^2 [2]	10–12	10–12	10–12	11–14	11–14	11–14	11–14
Was	Flash NAND cell size —area factor a in multiples of F^2 SLC/MLC [3]	5.5	5.5	4.5	4.5	4.5	4.5/2.3	4.5/2.3
Is	Flash NAND cell size —area factor a in multiples of F^2 SLC/MLC [3]	5.5	5.5	5.5	5.5	5.5	5.5	4.5
Was	Flash NOR typical cell size (μm^2) [4]	0.248	0.186	0.145	0.125	0.101	0.08	0.061
Is	Flash NOR typical cell size (μm^2) [4]	0.248	0.186	0.135	0.101	0.08	0.061	0.061
Was	Flash NOR Lg-stack (physical- μm) [5]	0.29–0.31	0.25–0.27	0.22–0.24	0.21–0.23	0.2–0.22	0.2–0.22	0.19–0.21
Is	Flash NOR Lg-stack (physical- μm) [5]	0.29–0.31	0.25–0.27	0.22–0.24	0.2–0.22	0.2–0.22	0.19–0.21	0.19–0.21
Was	Flash NOR highest W/E voltage (V) [6]	8–10	8–10	8–10	8–10	7–9	7–9	7–9
Is	Flash NOR highest W/E voltage (V) [6]	8–10	8–10	8–10	7–9	7–9	7–9	7–9
Was	Flash NAND highest W/E voltage (V) [7]	19–21	18–20	18–20	18–20	18–20	17–19	17–19
Is	Flash NAND highest W/E voltage (V) [7]	19–21	18–20	18–20	17-19	17-19	17-19	15-17
Was	Flash NOR I_{read} (μA) [8]	36–44	35–43	34–42	33–41	31–39	28–36	29–37
Is	Flash NOR I_{read} (μA) [8]	36–44	35–43	34–42	31–39	29-37	28-36	27-35
Was	Flash Coupling Ratio [9]	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.6–0.7
Is	Flash Coupling Ratio [9]	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.65–0.75	0.6–0.7	0.6–0.7
Was	Flash NOR tunnel oxide thickness (nm) [10]	9.5–10.5	9.5–10	9–10	9–10	8.5–9.5	8.5–9.5	8.5–9.5
Is	Flash NOR tunnel oxide thickness (nm) [10]	9.5-10.5	9-10	9-10	8.5-9.5	8.5-9.5	8.5-9.5	8-9
Was	Flash NAND tunnel oxide thickness (nm) [11]	8.5–9.5	8.5–9	8–9	8–9	8–9	7.5–8	7.5–8
Is	Flash NAND tunnel oxide thickness (nm) [11]	8.5-9.5	7-8	7-8	7-8	7-8	7-8	6-7
Was	Flash NOR interpoly dielectric thickness (nm) [12]	13–15	12–14	11–13	11–13	10–12	9–11	9–11
Is	Flash NOR interpoly dielectric thickness (nm) [12]	13-15	12-14	11-13	10-12	9-11	9-11	8.5-10.5
Was	Flash NAND interpoly dielectric thickness (nm) [13]	14–16	13–15	12–14	12–14	12–14	11–13	10–12
Is	Flash NAND interpoly dielectric thickness (nm) [13]	14-16	13-15	13-15	13-15	13-15	13-15	10-13
	Flash endurance (erase/write cycles) [14]	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05
	Flash nonvolatile data retention (years) [15]	10	10–20	10–20	10–20	10–20	10–20	10–20
	Flash maximum number of bits per cell (MLC) [16]	2	2	4	4	4	4	4
	FeRAM technology node - F (nm) [17]	500	350	250	220	180	150	130
	FeRAM cell size —area factor a in multiples of F^2 [18]	60	40	24	16	10	10	10
	FeRAM cell size (μm^2) [19]	15	4.9	1.5	0.518	0.324	0.225	0.169
	FeRAM cell structure [20]	2T2C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
	FeRAM capacitor structure [21]	planar	planar	stack	stack	stack	stack	3D
	Ferro capacitor voltage (V) [22]	3	3	2.5	1.8	1.5	1.3	1.2
	FeRAM endurance (read/write cycles) [23]	1.00E+12	1.00E+13	1.00E+14	1.00E+15	>1E16	>1E16	>1E16
	FeRAM nonvolatile data retention (years) [24]	10	10	10	10	10	10	10

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



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Table 38b Non-Volatile Memory Technology Requirements—Long-term

	Year of Production	2010	2013	2016
	DRAM ½ Pitch (nm)	45	32	22
	MPU / ASIC ½ Pitch (nm)	50	35	25
	MPU Printed Gate Length (nm)	25	18	13
	MPU Physical Gate Length (nm)	18	13	9
	Flash technology node - F (nm) [1]	50	35	25
	Flash NOR cell size –-area factor a in multiples of F^2 [2]	12–15	13–16	14–17
	Flash NAND cell size –-area factor a in multiples of F^2 SLC/MLC [3]	4.5/2.3	4.5/2.3	4.5/2.3
	Flash NOR typical cell size (μm^2) [4]	0.034	0.018	0.01
	Flash NOR Lg-stack (physical- µm) [5]	0.17–0.19	0.14–0.16	0.12–0.14
	Flash NOR highest W/E voltage (V) [6]	7–9	7–9	7–9
Was	Flash NAND highest W/E voltage (V) [7]	17–19	16–18	16–18
Is	Flash NAND highest W/E voltage (V) [7]	15-17	15-17	15-17
	Flash NOR I_read (µA) [8]	27–33	25–31	22–28
	Flash Coupling Ratio [9]	0.6–0.7	0.6–0.7	0.6–0.7
	Flash NOR tunnel oxide thickness (nm) [10]	8–9	8	8
	Flash NAND tunnel oxide thickness (nm) [11]	6–7	6–7	6–7
	Flash NOR interpoly dielectric thickness (nm) [12]	8–10	6–8	4–6
Was	Flash NAND interpoly dielectric thickness (nm) [13]	10–12	9–11	9–11
Is	Flash NAND interpoly dielectric thickness (nm) [13]	10-13	9-10	9-10
	Flash endurance (erase/write cycles) [14]	1.00E+06	1.00E+06	1.00E+07
	Flash nonvolatile data retention (years) [15]	10–20	20	20
	Flash maximum number of bits per cell (MLC) [16]	8	8	8
	FeRAM technology node - F (nm) [17]	100	70	50
	FeRAM cell size –-area factor a in multiples of F^2 [18]	8	8	8
	FeRAM cell size (μm^2) [19]	0.08	0.039	0.02
	FeRAM cell structure [20]	1T1C	1T1C	1T1C
	FeRAM capacitor structure [21]	3D	3D	3D
	Ferro capacitor voltage (V) [22]	1	0.7	0.7
	FeRAM endurance (read/write cycles) [23]	>1E16	>1E16	>1E16
	FeRAM nonvolatile data retention (years) [24]	10	10	10

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known



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FOLDER 8

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Overview and Summaries

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2004 ITRS SUMMARY

2004 UPDATE OVERVIEW



The ITRS process is an ongoing event. The industry is dynamic—continually innovating; introducing new products; and achieving solutions. To keep the ITRS information as current as possible with this dynamic industry environment, during each year following an edition such as the *2003 ITRS,* the roadmap information is reviewed. Data adjustments, corrections, and new information items are agreed to among the ITWG members and by soliciting public feedback during the annual ITRS Summer Conference in San Francisco. For the 2004 Update effort, all the ITRS tables were reviewed. If necessary, data and notations were updated to match industry advancements.

Link to the 2003 ITRS

Key Changes of the 2004 Update

A significant task was performed during this past year by annualizing all the tables. Previous years for the "long-term" technology requirements tables were indicated only for those years of technology generations, also referred to as "node" years. New for the 2004 Update, and set in place for the more involved effort of the complete revision of the 2005 ITRS, all 15 years of the ITRS timeframe are now indicated in all tables.

All chapters of the *2003 ITRS* have updates. Of the 219 tables contained in the 2003 ITRS, 128 tables were updated and 4 new tables were added. Additionally, 12 figures were updated. Many of the difficult challenges for the ITRS were revisited and updated to reflect the most current thinking and most critical tasks for semiconductor R&D. The *Overall Technology Roadmap Characteristics* were updated to reflect chapter table updates as well as indicate some revisions to be consistent with the technology tables. Please refer to the Appendix for the complete listing of ITRS tables and updates.

The reader should realize, that for the 2003 ITRS, the Near-term years span from 2003 to 2009 while the Long-term years span from 2010 to 2018. The reader will notice however that the year 2010 represents the year in which the hp45 technology node will occur. Several ITWGs have included any consideration related to this technology node in their Near-term challenges since it was easier for many of them to concentrate their attention on a well-defined technology node. Normally the technology nodes are studied very attentively while the data shown in the tables for the intermediate years are obtained by interpolation.

During this global review of the 2003 ITRS, a key message is that many of the difficult challenges and technology requirements were verified as correctly assessed for the semiconductor industry.

Although the update years focus on the table values, several chapters added new topics. A section introducing Emerging Research Materials was added to the Emerging Research Devices chapter, which was reviewed and updated in its entirety.

CD control tolerances and the timing of the introduction of 450mm were pervasive discussions among the teams. Edge exclusion was aligned among Front End Processes, Lithography, Factory Integration, and Yield Enhancement.

Other specific changes and challenges among the teams are as follows:

The Design chapter is revised to include an updated section on Design for Manufacturability and Design Verification, with several additional figures and tables.

Simultaneous modeling, using integrated input from a variety of related simulations [interconnect and packaging, or device and circuit] is viewed as critical.

Parametrically sensitive yield models that include new materials and comprehend the increased complexity within the fab are noted as a critical challenge in yield management. Other challenges for maintaining cost-effective yield management

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include new high aspect ratio inspection tools, testable and diagnosable designs for ICs, improvement in yield learning data management and test structures, as well as the critical need for achieving historic yield ramps and mature yield levels through effecient yield learning cycles.

New criteria for assessing potential solutions for Lithography now must address leading-edge manufacturing in at least two geographic regions with infrastructure in place [such as resists and mask capability]. Immersion lithography requirements and challenges were expanded, as this technology now appears viable down to 22nm. Particular parameters for mask and resists needs were evaluated to the current industry capability also resulting in revisions to timing of likely capability.

Interconnect added Cu resistivity numbers to reflect surface and sidewall scattering effects. The deterioration of resistivity as copper wire linewidth decreases is a key concern. Low κ values remain unchanged. For the first time in the past 10 years, the low κ portion of the roadmap was unaltered (κ value targets not delayed) with respect to the prior edition. Small changes were made to the shading of the boxes for bulk and effective dielectric constant over the next five years, recognizing that materials that deliver an effective κ =2.7 are in production today, and those material systems that will deliver an effective κ = 2.4 are expected to be available with manufacturable solutions in the next three years.

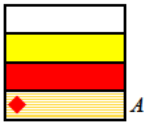
DRAM interconnect requirements with respect to contact resistivity have been updated. Also, specific interconnect requirements for other memory products, such as embedded memory and Flash, will be distinguished from DRAM in the 2005 ITRS.

A discussion on Gate CD tolerances throughout 2004 between Front End Processes and Lithography, and based on a industry survey, indicated this is a critical requirement to be resolved in the ITRS. The Front End Processes review also addressed the acceleration for the introduction of silicon-on-insulator [SOI]. Additionally, back surface particles are now included in the Surface Preparation section, with further study and discussion to occur in 2005.

Technology Requirements Guideline

"Interim Solutions are Known" is an additional category to the requirements tables' legend for the 2003 ITRS. This cell color is used in updated tables in many of the chapters, particularly Lithography, Interconnect, Metrology, and Modeling and Simulation. This requirements category appears as patterned colored cell with a red tag next to the data.

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known
Interim Solutions are Known



A definition of interim solutions is included in the Glossary.

The *Glossary* now includes the added definition of Interim Solutions to augment the new legend category.

FEATURES OF THE 2004 UPDATE ON THE CD

- Links to the *2003 ITRS* chapters are provided for convenience and easy review.
- Updated tables are noted with a line-item comparison of the *2003 ITRS* [noted as "**Was**"] and the *2004 Update* data [noted as "**Is**"], with the changed cells clearly outlined and data in underlined font. If a line item was either deleted or added during the 2004 Update, the line is indicated.

WAS	Line item	2003 data	2003 data	2003 data	2003 data	2003 data
IS	Line item	2004 data	2003 data	2004 data	2004 data	2004 data

~~Delete~~	~~Line item~~	~~2003 data~~	~~2003 data~~	~~2003 data~~	~~2003 data~~
Add	New line item	data	data	data	data

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OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS TABLES

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
ASIC/Low Operating Power Printed Gate Length (nm) ††	90	75	65	53	45	40	35
ASIC/Low Operating Power Physical Gate Length (nm)	65	53	45	37	32	28	25

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	ASIC/Low Operating Power Printed Gate Length (nm) ††	32		25	22		18	16		13
IS	ASIC/Low Operating Power Printed Gate Length (nm) ††	32	28	25	22	20	18	16	14	13
WAS	ASIC/Low Operating Power Physical Gate Length (nm)	22		18	16		13	11		9
IS	ASIC/Low Operating Power Physical Gate Length (nm)	22	20	18	16	14	13	11	10	9

Notes for Tables 1a and 1b

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "physical" gate lengths may be reduced from the "as-printed" dimension. These "physical" gate-length targets are driven by the need for maximum speed performance in logic Microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design ITWG Tables as needs that drive device design and process technology requirements.

In addition, during the 2003 ITRS development, an attempt has been made to reconcile the many published press releases by Logic manufacturers referencing "90 nm" technology node manufacturing in 2003. Since the metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that the public citations were in reference to an "indexed" technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance).

The IRC has decided that the best way to minimize confusion between the ITRS and individual company public announcements is to identify the ITRS table header node with the industry's most aggressive half-pitch targets, and to label these targets as hpXX (i.e., hp90, hp65, hp45, etc.). Currently the industry's most aggressive half pitch is the DRAM cell metal half-pitch. Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

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Table 1c DRAM Production Product Generations and Chip Size Model—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Cell area factor [a]	8	8	7.5	7	7	6	6
Cell area [Ca = af^2] (μm^2)	0.082	0.065	0.048	0.036	0.028	0.019	0.015
Cell array area at production (% of chip size) §	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%
Generation at production §	1G	1G	1G	2G	2G	4G	4G
Functions per chip (Gbits)	1.07	1.07	1.07	2.15	2.15	4.29	4.29
Chip size at production (mm^2)§	139	110	82	122	97	131	104
Gbits/cm^2 at production §	0.77	0.97	1.31	1.76	2.22	3.27	4.12

Table 1d DRAM Production Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Cell area factor [a]	6		6	6		6	5		5
IS	Cell area factor [a]	6	6	6	6	6	6	5	5	5
WAS	Cell area [Ca = af^2] (mm^2)	0.012		0.0077	0.0061		0.0038	0.0025		0.0016
IS	Cell area [Ca = af^2] (μm^2)	0.012	0.0096	0.0077	0.0061	0.005	0.0038	0.0025	0.002	0.0016
WAS	Cell array area at production (% of chip size) §	63.00%		63.00%	63.00%		63.00%	63.00%		63.00%
IS	Cell array area at production (% of chip size) §	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%
WAS	Generation at production §	4G		8G	8G		16g	32G		32G
IS	Generation at production §	4G	8G	8G	8G	16g	16g	32G	32G	32G
WAS	Functions per chip (Gbits)	4.29		8.59	8.59		17.18	34.36		34.36
IS	Functions per chip (Gbits)	4.29	8.59	8.59	8.59	17.18	17.18	34.36	34.36	34.36
WAS	Chip size at production (mm^2)§	83		104	83		104	138		87
IS	Chip size at production (mm^2)§	83	131	104	83	131	104	138	110	87
WAS	Gbits/cm^2 at production §	5.19		8.23	10.37		16.46	24.89		39.51
IS	Gbits/cm^2 at production §	5.19	6.53	8.23	10.37	13.07	16.46	24.89	31.36	39.51

Notes for Tables 1c and 1d
§ DRAM Model—Cell Factor (design/process improvement) targets are as follows
1999-2004/8× 2005/7.5×; 2006-2007/7×; 2008-2015/6×; 2016–2018/5×. The delay of the "6" DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.
DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except
1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).
InTER-generation chip size growth rate model target for Production-phase DRAMs is now "flat" at less than 140 mm^2, similar to the MPU model. This new flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Table 1c, d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63% , which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above).The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.
Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
DRAM ½ Pitch (nm)	**100**	**90**	**80**	**70**	**65**	**57**	**50**
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Cell area factor [a]	**8**	**8**	**7.5**	**7**	**7**	**6**	**6**
Cell area [Ca = af^2] (μm^2)	**0.082**	**0.065**	**0.048**	**0.036**	**0.028**	**0.019**	**0.015**
Cell array area at introduction (% of chip size) §	**72.23%**	**72.61%**	**72.95%**	**73.25%**	**73.52%**	**73.76%**	**73.97%**
Generation at introduction §	**4G**	**4G**	**8G**	**8G**	**16G**	**16G**	**16G**
Functions per chip (Gbits)	**4.29**	**4.29**	**8.59**	**8.59**	**17.18**	**17.18**	**17.18**
Chip size at introduction (mm^2) §	**485**	**383**	**568**	**419**	**662**	**449**	**356**
Gbits/cm^2 at introduction §	**0.88**	**1.12**	**1.51**	**2.05**	**2.59**	**3.82**	**4.83**

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Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Cell area factor [a]	6		6	6		6	5		5
IS	Cell area factor [a]	6	6	6	6	6	6	5	5	5
WAS	Cell area [Ca = af2] (mm^2)	0.012		0.0077	0.0061		0.0038	0.0025		0.0016
IS	Cell area [Ca = af2] (μm^2)	0.0120	0.01	0.0077	0.0061	0.005	0.0038	0.0025	0.0020	0.0016
WAS	Cell array area at introduction (% of chip size) §	74.16%		74.47%	74.61%		74.83%	74.93%		75.09%
IS	Cell array area at introduction (% of chip size) §	74.16%	74.30%	74.47%	74.61%	74.70%	74.83%	74.93%	75.00%	75.09%
WAS	Generation at introduction §	32G		32G	64G		64G	128G		128G
IS	Generation at introduction §	32G	32G	32G	64G	64G	64G	128G	128G	128G
WAS	Functions per chip (Gbits)	34.36		34.36	68.72		68.7	137.4		137.4
IS	Functions per chip (Gbits)	34.36	34.36	34.36	68.72	68.72	68.7	137.4	137.4	137.4
WAS	Chip size at introduction (mm^2) §	563		353	560		351	464		292
IS	Chip size at introduction (mm^2) §	563	458	353	560	456	351	464	378	292
WAS	Gbits/cm2 at introduction §	5.2		8.2	10.4		16.5	24.9		39.5
IS	Gbits/cm2 at introduction §	6.10	7.71	9.73	12.3	15.5	19.6	29.6	37.3	47.1

Notes for Tables 1e and 1f

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows 1999-2004/8× 2005/7.5×; 2006-2007/7×; 2008-2015/6×; 2016–2018/5×. The delay of the "6" DRAM Cell design improvement Factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a 3-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation/2007, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation/2003, the introduction rate is 4×/five years (2×/two–three years).

The original 2001 ITRS InTER-generation chip size growth rate was targeted to fit one chip per 572 mm^2 field at Introduction and two chips per 572 mm^2 field at Production. Due to the delay of the cell area factor reductions, Introduction chip sizes increased, but the new 704 mm^2 maximum affordable Litho field allows the Introduction chip to double bits per chip every two years through the 16 Gbit generation (660 mm^2/2007). Slowing the "Moore's Law" bits per chip of the Introduction-phase DRAM model to an average of 2× per 2.5 years enables the Introduction DRAMs to remain under the original 572 mm^2 affordable target after 2007. The InTRA-generation chip size shrink model remains at 0.5× every technology node in-between cell factor reductions, and eventually (ranging from five to six years), the Introduction-phase DRAMs shrink below the 140 mm^2 Production-phase chip size target.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	SRAM Cell (6-transistor) Area factor ++	120.3	117.8	115.6	113.7	111.9	110.4	109
	Logic Gate (4-transistor) Area factor ++	320	320	320	320	320	320	320
	SRAM Cell (6-transistor) Area efficiency ++	0.63	0.63	0.63	0.63	0.63	0.63	0.63
	Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50	0.50	0.50	0.50	0.50
NEW	SRAM Cell (6-transistor) Area ++	1.23	0.95	0.74	0.58	0.45	0.35	0.28
	SRAM Cell (6-transistor) Area w/overhead ++	2.0	1.5	1.2	0.93	0.73	0.57	0.45
NEW	Logic Gate (4-transistor) Area ++	3.27	2.59	2.06	1.63	1.30	1.03	0.82
	Logic Gate (4-transistor) Area w/overhead ++	6.5	5.2	4.1	3.3	2.6	2.1	1.6
	Transistor density SRAM (Mtransistors/cm^2)	305	393	504	646	827	1,057	1,348
	Transistor density logic (Mtransistors/cm^2)	61	77	97	122	154	194	245
	Generation at introduction *	--	p07c	--	--	p10c	--	--
WAS	Functions per chip at introduction (million transistors [Mtransistors])	180	226	285	360	453	571	719
IS	Functions per chip at introduction (million transistors [Mtransistors])	307	386	487	614	773	974	1227
	Chip size at introduction (mm^2) ‡	280	280	280	280	280	280	280
	Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	110	138	174	219	276	348	438
	Generation at production *	--	p04c	--	--	p07c	--	--
	Functions per chip at production (million transistors [Mtransistors])	153	193	243	307	386	487	614
	Chip size at production (mm^2) §§	140	140	140	140	140	140	140
	Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	110	138	174	219	276	348	438

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	SRAM Cell (6-transistor) Area factor ++	107.8		105.7	104.8		103.4	102.8		101.7
IS	SRAM Cell (6-transistor) Area factor ++	107.8	106.7	105.7	104.8	104.1	103.4	102.8	102.2	101.7
WAS	Logic Gate (4-transistor) Area factor ++	320		320	320		320	320		320
IS	Logic Gate (4-transistor) Area factor ++	320	320	320	320	320	320	320	320	320
WAS	SRAM Cell (6-transistor) Area efficiency ++	0.625		0.625	0.625		0.625	0.625		0.625
IS	SRAM Cell (6-transistor) Area efficiency ++	0.625	0.625	0.625	0.625	0.625	0.625	0.625	0.625	0.625
WAS	Logic Gate (4-transistor) Area efficiency ++	0.5		0.5	0.5		0.5	0.5		0.5
IS	Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
NEW	SRAM Cell (6-transistor) Area	0.22	0.17	0.13	0.11	0.084	0.066	0.052	0.041	0.032
WAS	SRAM Cell (6-transistor) Area w/overhead ++	0.22		0.13	0.11		0.066	0.052		0.032
IS	SRAM Cell (6-transistor) Area w/overhead ++	0.35	0.27	0.22	0.17	0.13	0.106	0.083	0.07	0.052
NEW	Logic Gate (4-transistor) Area	0.65	0.51	0.41	0.32	0.26	0.20	0.16	0.13	0.10
WAS	Logic Gate (4-transistor) Area w/overhead ++	1.3		0.82	0.65		0.41	0.32		0.2
IS	Logic Gate (4-transistor) Area w/overhead ++	1.30	1.03	0.82	0.65	0.51	0.41	0.32	0.26	0.20
WAS	Transistor density SRAM (Mtransistors/cm^2)	1,718		2,781	3,532		5,687	7,208		11,558
IS	Transistor density SRAM (Mtransistors/cm^2)	1,718	2,187	2,781	3,532	4,484	5,687	7,208	9,130	11,558
WAS	Transistor density logic (Mtransistors/cm^2)	309		490	617		980	1,235		1,960
IS	Transistor density logic (Mtransistors/cm^2)	309	389	490	617	778	980	1,235	1,555	1,960

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Generation at introduction *	p13c		--	p16c		--	p19c		--
IS	Generation at introduction *	p13c	--	--	p16c	--	--	p19c	--	--
WAS	Functions per chip at introduction (million transistors [Mtransistors])	1,546		2,454	3,092		4,908	6,184		9,816
IS	Functions per chip at introduction (million transistors [Mtransistors])	1,546	1,948	2,454	3,092	3,896	4,908	6,184	7,791	9,816
WAS	Chip size at introduction (mm^2) ‡	280		280	280		280	280		280
IS	Chip size at introduction (mm^2) ‡	280	280	280	280	280	280	280	280	280
WAS	Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	552		876	1,104		1,753	2,209		3,506
IS	Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	552	696	876	1,104	1,391	1,753	2,209	2,783	3,506
WAS	Generation at production *	p10c		--	p13c		--	p16c		--
IS	Generation at production *	p10c	--	--	p13c	--	--	p16c	--	--
WAS	Functions per chip at production (million transistors [Mtransistors])	773		1,227	1,546		2,454	3,092		4,908
IS	Functions per chip at production (million transistors [Mtransistors])	773	974	1,227	1,546	1,948	2,454	3,092	3,896	4,908
WAS	Chip size at production (mm^2) §§	140		140	140		140	140		140
IS	Chip size at production (mm^2) §§	140	140	140	140	140	140	140	140	140
WAS	Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	552		876	1,104		1,753	2,209		3,506
IS	Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	552	696	876	1,104	1,391	1,753	2,209	2,783	3,506

Notes for Tables 1g and 1h

++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p01c, was introduced in 1999, but not ramped into volume production until 2001; similarly, the p04c, is introduced in 2001, but is targeted for volume production in 2004.*

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/1999), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions

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Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years
UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	Logic (Low-volume Microprocessor) High-performance ‡							
WAS	Generation at production **	p03h	--	p05h	--	p07h	--	p09h
IS	Generation at production **	--	p04h	--	--	p07h	--	--
	Functions per chip (million transistors)	439	553	697	878	1,106	1,393	1,756
	Chip size at production (mm^2) §§	310	310	310	310	310	310	310
	High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	142	178	225	283	357	449	566
	ASIC							
	ASIC usable Mtransistors/cm^2 (auto layout)	142	178	225	283	357	449	566
	ASIC max chip size at production (mm^2) (maximum lithographic field size)	572	572	572	572	572	572	572
	ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	810	1,020	1,286	1,620	2,041	2,571	3,239

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years
UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Logic (Low-volume Microprocessor) High-performance ‡									
WAS	Generation at production **	--		--	p13h		p15h	--		--
IS	Generation at production **	p10h	--	--	p13h	--	--	p16h	--	--
WAS	Functions per chip (million transistors)	2,212		3,511	4,424		7,022	8,848		14,045
IS	Functions per chip (million transistors)	2,212	2,787	3,511	4,424	5,574	7,022	8,848	11,147	14,045
WAS	Chip size at production (mm^2) §§	310		310	310		310	310		310
IS	Chip size at production (mm^2) §§	310	310	310	310	310	310	310	310	310
WAS	High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	714		1,133	1,427		2,265	2,854		4,531
IS	High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	714	899	1,133	1,427	1,798	2,265	2,854	3,596	4,531
	ASIC									
WAS	ASIC usable Mtransistors/cm^2 (auto layout)	714		1,133	1,427		2,265	2,854		4,531
IS	ASIC usable Mtransistors/cm^2 (auto layout)	714	899	1,133	1,427	1,798	2,265	2,854	3,596	4,531
WAS	ASIC maximum chip size at production (mm^2) (maximum lithographic field size)	572		572	572		572	572		572
IS	ASIC maximum chip size at production (mm^2) (maximum lithographic field size)	572	572	572	572	572	572	572	572	572
WAS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081		6,479	8,163		12,958	16,326		25,915
IS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081	5,142	6,479	8,163	10,284	12,958	16,326	20,569	25,915

Notes for Tables 1i and 1j
*** p is processor, numerals reflect year of production; h indicates high-performance product. Examples—the high-performance processor, p99h, was ramped into volume production in 1999; similarly, the p01h, is introduced in 2001, the p03h in2003, and so forth.*
‡ MPU High-performance Model—High-performance MPU includes large L2 and L3 on-chip SRAM (2MByte/1999) plus a larger logic core (P99h core = 25M transistor (Mtransistors) both SRAM and Logic functionality doubles every technology node cycle.
§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.
Refer to the Glossary for definitions

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Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Lithography Field Size							
Lithography Field Size—area (mm^2)	704	704	704	704	704	704	704
Lithographic field size—length (mm)	32	32	32	32	32	32	32
Lithographic field size—width (mm)	22	22	22	22	22	22	22
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	300	300	300	300	300	300	300

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	-	42	38	-	30	27	-	21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Lithography Field Size									
WAS	Lithography Field Size—area (mm^2)	704		704	704		704	704		704
IS	Lithography Field Size—area (mm^2)	704	704	704	704	704	704	704	704	704
WAS	Lithographic field size—length (mm)	32	-	32	32	-	32	32	-	32
IS	Lithographic field size—length (mm)	32	32	32	32	32	32	32	32	32
WAS	Lithographic field size—width (mm)	22	-	22	22	-	22	22	-	22
IS	Lithographic field size—width (mm)	22	22	22	22	22	22	22	22	22
	Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)									
WAS	Bulk or epitaxial or SOI wafer	300		450	450		450	450		450
IS	Bulk or epitaxial or SOI wafer	300	300	450	450	450	450	450	450	450

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	Number of Chip I/Os (Number of Total Chip Pads)—Maximum							
WAS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,328	3,584
IS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072
WAS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,109	1,195
IS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,024	1,024
WAS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,219	2,389
IS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,048	2,048
WAS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,600	4,800
IS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,400	4,600
WAS	Signal I/O pads—ASIC high-performance	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Signal I/O pads—ASIC high-performance	1700	1800	2000	2100	2200	2200	2300
WAS	Power and ground pads— ASIC high-performance (½ of total pads)	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Power and ground pads— ASIC high-performance (½ of total pads)	1700	1800	2000	2100	2200	2200	2300
	Number of Total Package Pins—Maximum [1]							
WAS	Microprocessor/controller, cost-performance	500–1,452	500–1,600	550–1,760	550–1,936	600–2,140	660–2,354	720–2,568
IS	Microprocessor/controller, cost-performance	--	500–1600	550–1760	550–1936	600–2140	600–2400	660–2800
WAS	Microprocessor/controller, high-performance	1,452	1,600	1,760	1,936	2,140	2,354	2,568
IS	Microprocessor/controller, high-performance	--	1,600	1,760	1,936	2,140	2,400	2,800
WAS	ASIC (high-performance)	2,400	3,000	3,400	3,800	4,000	4,400	4,600
IS	ASIC (high-performance)	--	3,000	3,400	3,800	4,000	4,400	4,600

Notes for Tables 3a and 3b
[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by PWB technology and system cost. The highest pin count applications will as a result use larger pitches and larger package sizes. The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2 1 to 1 4.

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Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Number of Chip I/Os (Number of Total Chip Pads)—Maximum									
WAS	Total pads—MPU	3,840		4,096	4,224		4,352	4,416		4,544
IS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072
WAS	Signal I/O—MPU (1/3 of total pads)	1,280		1,365	1,408		1,451	1,472		1,515
IS	Signal I/O—MPU (1/3 of total pads)	1024	1024	1024	1024	1024	1024	1024	1024	1024
WAS	Power and ground pads—MPU (2/3 of total pads)	2,560		2,731	2,816		2,901	2,944		3,029
IS	Power and ground pads—MPU (2/3 of total pads)	2048	2048	2048	2048	2048	2048	2048	2048	2048
WAS	Total pads—ASIC high-performance	4,800		5,200	5,400		5,800	6,000		6,400
IS	Total pads—ASIC high-performance	4,800	4,800	5,000	5,400	5,400	5,600	6,000	6,000	6,200
WAS	Signal I/O pads—ASIC high-performance	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Signal I/O pads—ASIC high-performance	2,400	2,400	2,500	2,700	2,700	2,800	3,000	3,000	3,100
WAS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	2,400	2,500	2,700	2,700	2,800	3,000	3,000	3,100
	Number of Total Package Pins—Maximum [1]									
	Microprocessor/controller, cost-performance	780–2,782		936–3,338	1014–3,616		1217–4,340	1318–4,702		1521–5,426
	Microprocessor/controller, high-performance	2,782		3,338	3,616		4,340	4,702		5,426
	ASIC (high-performance)	4,009		4,810	5,335		6,402	7,042		8,450

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	Chip Pad Pitch (micron)							
WAS	Pad pitch—ball bond	40	35	30	25	25	20	20
IS	Pad pitch—ball bond	40	40	35	35	30	30	25
WAS	Pad pitch—wedge bond	30	25	20	20	20	20	20
IS	Pad pitch—wedge bond	30	30	30	25	25	25	20
	Pad Pitch—area array flip-chip (cost-performance, high-performance)	150	150	130	130	120	110	100
	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	60	60	40	40	30	30	20
	Cost-Per-Pin							
	Package cost (cents/pin) (cost-performance)—minimum-maximum	.75–1.30	.71–1.24	.67–1.17	.64–1.11	.61–1.05	.58–1.00	.55–.96
WAS	Package cost (cents/pin) (Memory)—minimum–maximum	0.30–0.56	0.29–.53	.27–.50	,26–.48	,25–.45	.23–.43	.22–.41
IS	Package cost (cents/pin) (Memory)—minimum–maximum	0.30–0.56	0.30–.53	.27–.50	.26–.48	.25–.45	.23–.43	.22–.41

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Table 4b Performance and Package Chips: Pads, Cost—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Chip Pad Pitch (micron)									
WAS	Pad pitch—ball bond	20		20	20		20	20		20
IS	Pad pitch—ball bond	25	25	25	25	25	25	25	25	25
WAS	Pad Pitch—wedge bond	20		20	20		20	20		20
IS	Pad Pitch—wedge bond	20	20	20	20	20	20	20	20	20
WAS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	100		90	90		80	80		70
IS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	90	--	90		--	80	--	--	70
WAS	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	20		20	20		15	15		15
IS	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	20	20	20	20	--	15	15	15	15
	Cost-Per-Pin									
	Package cost (cents/pin) (cost-performance)— minimum–maximum	0.52–0.94		0.5–.86	0.5–.77		0.5–0.69	0.5–0.65		0.5–0.59
	Package cost (cents/pin) (Memory)— minimum–maximum	.22–.41		0.22–0.36	0.22–0.35		0.22–0.31	0.22–0.29		0.22–0.27

Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Chip Frequency (MHz)							
On-chip local clock	2,976	4,171	5,204	6,783	9,285	10,972	12,369
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	2,000	2,500	3,125	3,906	4,883	6,103	7,629
Maximum number wiring levels—maximum	13	14	15	15	15	16	16
Maximum number wiring levels—minimum	9	10	11	11	11	12	12

Table 4d Performance and Package Chips: Frequency, On-chip Wiring Levels—Long-term Years
UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Chip Frequency (MHz)									
	On-chip local clock	15,079		20,065	22,980		33,403	39,683		53,207
	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	9,536		14,901	18,626		29,103	36,379		56,843
WAS	Maximum number wiring levels—maximum	16		16	16		17	18		18
IS	Maximum number wiring levels—maximum	16	16	16	16	17	17	18	18	18
WAS	Maximum number wiring levels—minimum	12		12	12	-	13	14	-	14
IS	Maximum number wiring levels—minimum	12	12	12	12	13	13	14	14	14

Note for Tables 4c and 4d
[1] The off-chip frequency is expected to increase for a small number of high-speed pins that will be used in combination with a large number of lower speed pins
[2] In 2001, high-speed serial communications transceiver devices are achieving chip-board frequencies of 3.125 GHz using CMOS, and 10 GHz using SiGe. In 2002 it is expected that 10 GHz transceivers will be fabricated using CMOS. 40 GHz SiGe devices are expected in 2003. The roadmap for higher levels of integration with wider bus widths, is shown in the High Frequency Serial Communications section in the Test chapter.
[3] The minimum number of wiring levels represents the interconnect metal levels, and the maximum number of interconnect wiring levels includes the Minimum number of wiring levels plus additional optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

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Table 5a Electrical Defects—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	2,216	2,791	3,751	2,532	3,190	2,345	2,954
MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	1,395	1,395	1,395	1,395	1,395	1,395	1,395
# Mask Levels—MPU	29	31	33	33	33	35	35
# Mask Levels—DRAM	24	24	24	24	24	24	24

Table 5b Electrical Defects—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §	3,722		2,954	3,722		2,954	2,233		3,545
IS	DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §	3,722	2,353	2,954	3,722	2,353	2,954	2,233	2,803	3,545
WAS	MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§	1,395		1,395	1,395		1,395	1,395		1,395
IS	MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§	1,395	1,395	1,395	1,395	1,395	1,395	1,395	1,395	1,395
WAS	# Mask Levels—MPU	35		35	35		37	39		39
IS	# Mask Levels—MPU	35	35	35	35	37	37	39	39	39
WAS	# Mask Levels—DRAM	26		26	26		26	26		26
IS	# Mask Levels—DRAM	26	26	26	26	26	26	26	26	26

Notes for Tables 5a and 5b

D_0 — defect density

§ DRAM Model—Cell factor (design/process improvement) targets are as follows 1999–2004/8× 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the "6" DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

Table 6a Power Supply and Power Dissipation—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	Power Supply Voltage (V)							
	V_{dd} (high-performance)	1.2	1.2	1.1	1.1	1.1	1	1
	V_{dd} (Low Operating Power, high V_{dd} transistors)	1	0.9	0.9	0.9	0.8	0.8	0.8
	Allowable Maximum Power [1]							
WAS	High-performance with heatsink (W)	149	158	167	180	189	200	210
IS	High-performance with heatsink (W)	149	158	167	180	189	198	198
	Cost-performance (W)	80	84	91	98	104	109	114
	Battery (W)—(low-cost/hand-held)	2.1	2.2	2.3	2.4	2.5	2.6	2.7

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 6b Power Supply and Power Dissipation—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Power Supply Voltage (V)									
WAS	Vdd (high-performance)	1		0.9	0.9		0.8	0.8		0.7
IS	Vdd (high-performance)	1	1	0.9	0.9	0.9	0.8	0.8	0.7	0.7
WAS	Vdd (Low Operating Power, high Vdd transistors)	0.7		0.7	0.6		0.6	0.5		0.5
IS	Vdd (Low Operating Power, high Vdd transistors)	0.7	0.7	0.7	0.6	0.6	0.6	0.5	0.5	0.5
	Allowable Maximum Power [1]									
WAS	High-performance with heatsink (W)	218		240	251		270	288		300
IS	High-performance with heatsink (W)	198	198	198	198	198	198	198	198	198
	Cost-performance (W)	120		131	138		148	158		168
	Battery (W)—(hand-held)	2.8		3	3		3	3		3

[1] Power will be limited more by system level cooling and test constraints than packaging

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Table 7a Cost—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	**10.5**	**7.4**	**5.3**	**3.7**	**2.6**	**1.9**	**1.3**
DRAM cost/bit at (packaged microcents) at production §	**3.8**	**2.7**	**1.9**	**1.4**	**0.96**	**0.7**	**0.5**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**88**	**62**	**44**	**31**	**22**	**15.6**	**11.0**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**53**	**38**	**27**	**19**	**13.3**	**9.4**	**6.7**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**49**	**34**	**24**	**17**	**12**	**8.6**	**6.1**
Cost-Per-Pin							
Test Cost							
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	**1**	**1**	**1**	**1**	**1**	**1**	**2**

Notes for Tables 7a and 7b

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two to four years after introduction).

§ DRAM Model—Cell factor (design/process improvement) targets are as follows

1999–2004/8× 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the "6" DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

InTER-generation chip size growth rate model target for Production-phase DRAMs is now "flat" at less than 140 mm^2, similar to the MPU model. This new flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Tables 1c and d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63%, which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above). The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 7b Cost—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Affordable Cost per Function ++									
WAS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93		0.46	0.33		0.16	0.12		0.06
IS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93	0.66	0.46	0.33	0.23	0.16	0.12	0.08	0.06
WAS	DRAM cost/bit (packaged microcents) at production §	0.34		0.17	0.12		0.06	0.042		0.021
IS	DRAM cost/bit (packaged microcents) at production §	0.34	0.24	0.17	0.12	0.08	0.06	0.04	0.03	0.02
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78		3.89	2.75		1.38	0.97		0.49
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78	5.50	3.89	2.75	1.94	1.38	0.97	0.69	0.49
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71		2.35	1.66		0.83	0.59		0.29
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71	3.33	2.35	1.66	1.18	0.83	0.59	0.42	0.29
WAS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.305		2.15	1.52		0.76	0.54		0.27
IS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.30	3.04	2.15	1.52	1.08	0.76	0.54	0.38	0.27
	Cost-Per-Pin									
	Test Cost									
WAS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	4		4	4		4	4		4
IS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	4	4	4	4	4	4	4	4	4
WAS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	2		2	3		3	4		4
IS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	2	2	2	3	3	3	4	4	4

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

Technology Node—The minimum half-pitch of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated circuits and is selected to define an ITRS Technology Node. For each Node, this defining metal half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other parameters are also important for characterizing IC technology. For example, in the case of microprocessors (MPUs), physical bottom gate length is most representative of the leading-edge technology level required for maximum performance. Each technology node step represents the creation of significant technology progress in metal half-pitch — approximately 70% of the preceding node, 50% of two preceding nodes.

Example: DRAM half pitches of 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, and 22 nm.

For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

An official *2003 ITRS* metal half-pitch node indicator, "hpXX," has been added to differentiate the ITRS definition from commercial technology generation numbers .

Moore's Law—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore's Law, there is a historically-based "corollary" to the "law," which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every three years, as suggested by consensus DRAM and MPU models of the *2003 ITRS*, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

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Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1Mbytes/2001). Logic functionality and L2 cache typically double every three-year generation.

High-performance MPU—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example two cores at 25Mt cores in 2001) with a large (example 4Mbyte/2001) level-two (L2) SRAM. Logic functionality and L2 cache typically double every three-year technology generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology-node scaling (.7× linear, .5× area) is every three years, an additional device/process design improvement of .8× per two years must be achieved. This requirement represents a design-related (cell-area-factor) area-reduction improvement of at least -11% per year, and this design-related productivity improvement is in addition to the basic lithography-based area reduction of -21% per year (three-year node cycle).

The present *2003 ITRS* consensus target for the rate of increase of DRAM bits/chip has increased from 2× bits/chip every two years to 2×/chip every two and half years average. This slower bits/chip growth is required due to the new consensus *2003 ITRS* forecast of cell-area-factor improvement of only negative 4–6% per year on average rather than the *2001 ITRS* target of -7% per year average. This results in an average DRAM inTER-generation approximately flat chip-size growth. Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the *2003 ITRS* MPU inTER-generation functionality model target is 2× transistors/chip every technology node, in order maintain a flat chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The *2003 ITRS* consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The *ITRS* targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every four years at the leading-edge process technology node, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples. Example: 1997/ISSCC/1Gb DRAM, versus *ITRS* 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every two years (every technology node, in the case of MPUs). In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturer begins shipping volume quantities (initially, at least 10K/month) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume

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production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready 12–24 months prior to Production Ramp "Time Zero" [see Figure 2 in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1Gb/production, 4G/introduction, plus 512Mb/256Mb/128Mb/64Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the *ITRS* consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the *2003 ITRS*, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 63% at the production level, and less than 50–55% for smaller previous generation shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified *ITRS*-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 1999: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E = 0.37\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.37e-6 mm^2/bit = 397 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, 1.6×1.6=2.5, etc.).

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density

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calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The *ITRS* timing targets, contributed by the Factory Integration ITWG, are based on the first 20K wafer-starts-per-month manufacturing facility.

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ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

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WORKING GROUP SUMMARIES

DESIGN

This update includes (a) a revised "General" design technology requirements (revised), with some new rows, and new explanations as footnotes for each row, but no changes in the values of existing rows, (b) a new design technology solutions table after the requirements table, which includes a definition of each row, (c) a new Design For Manufacturability (DFM) section with completely new content, and (d) an update of the verification section.

Table A Design For Manufacturability Challenges ADDED

Challenges ≥50 nm/Through 2009	*Summary Of Issues*
Mask cost	ALL—CAD tools that explicitly account for mask cost in their algorithms
Data explosion	ALL—RET tools that are explicitly aware of circuit metrics (timing, power)
Limitations of lithography hardware resolution	ALL—RET-aware CAD tools, radically-restricted design rules, including yield prediction and optimization
Voltage supply and threshold variability	ALL—Statistical analysis tools and flows that account for this variability, including yield prediction and optimization
BEOL Planarization and dimensional variability	ALL—Statistical design tools and flows that account for this variability; including yield prediction and optimization
Heterogeneous components (analog, MEMS, eRAM)	
Leakage as a limiter of manufacturability	ALL—Statistical leakage analysis and optimization tools
Additional Challenges <50 nm/Beyond 2009	
Leakage as a limiter of manufacturability	ALL—Statistical leakage optimization tools
Uncontrollable CD and doping variability	ALL—Statistical parametric optimization tools
Extreme device and circuit variability	ALL—Architectures fundamentally resistant to variability (redundancy, ECC)
Critical need to integrate RET into design	ALL—RET-aware CAD tools
Package, system, and software variability	ALL—adaptable and redundant circuits that can adapt to these variations
BEOL planarization and dimensional variability	ALL—post-tapeout RET that interacts with synthesis, timing, and P&R

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory, ALL—all of these).

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TEST

The 2004 update to the ITRS Test chapter is focused on minor corrections to previously published trend information and completion of the annualized long term tables. The most significant corrections occurred in the memory tables to eliminate portions of missing data from the 2003 revision. The modifications contained in this update do not represent fundamental changes in the direction of test in the industry.

ITWG activities have shifted to the 2005 chapter revision. In 2005 an effort will be made to reduce the number of table line items significantly by eliminating entries that do not show significant trending that will drive technology development for equipment or methods. In addition, the ITWG is reviewing proposals to merge some of the sections into broader topic categories to better focus on the key challenges - such as the merging of microprocessor, ASIC, and microcontroller topics into a single "Logic Test" section as a possible example. The purpose of this reorganization of chapter content is intended to focus ITWG activities on the emerging key challenges in the test area.

Table 23a Test and Test Equipment Difficult Challenges—Near-term

Five Difficult Challenges ≥45 nm/Through 2010	*Summary of Issues*
High-speed Device Interfaces	A major roadblock will be the need for high frequency, high pin count probes and test sockets; research and development is urgently required to enable cost-effective solutions with reduced parasitic impedance. High-speed serial interface speed and port count trends will continue to drive high-speed analog source/capture and jitter analysis instrument capability for characterization. DFT/DFM techniques must be developed for manufacturing. Device interface circuitry must not degrade equipment bandwidth and accuracy, or introduce noise, especially for high-frequency differential I/O and analog circuits.
Highly Integrated Designs	Highly structured DFT approaches are required to enable test access to embedded cores. Individual cores require special attention when using DFT and BIST to enable test. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever-increasing instrument capability trends. Testing chips containing RF and audio circuits will be a major challenge if they also contain large numbers of noisy digital circuits. DFT must enable test reuse for reusable design cores to reduce test development time for highly complex designs.
Reliability Screens	Existing methodologies are limited (burn-in versus thermal runaway, IDDQ versus background current increases). Research is required to identify novel infant mortality defect acceleration stress conditions
Manufacturing Test Cost	Test cell throughput enhancements are needed to reduce manufacturing test cost. Opportunities include massively parallel test, wafer-level test, wafer-level burn-in, and others. Challenges include device interfacing/contacting, power and thermal management. Device test needs must be managed through DFT to enable low-cost manufacturing test solutions; including reduced pin count test, equipment reuse, and reduced test time. Automatic test program generators are needed to reduce test development time. Test standards are required to enable test content reuse and manufacturing agility.
Modeling and Simulation	Logic and timing accurate simulation of the ATE, device interface, and DUT is needed to enable pre-silicon test development and minimize costly post-silicon test content development/debug on expensive ATE. High-performance digital and analog I/O and power requirements require significant improvements to test environment simulation capability to ensure signal accuracy and power quality at the die. Equipment suppliers must provide accurate simulation models for pin electronics, power supplies, and device interfaces to enable interface design.

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Table 23b Test and Test Equipment Difficult Challenges—Long-term

Five Difficult Challenges <45 nm/Beyond 2010	*Summary of Issues*
DUT to ATE interface	Probing capability for optical and other disruptive technologies Support for massively parallel test—including full wafer contacting Decreasing die size and increasing circuit density are driving dramatic increases in die thermal density. This problem is further magnified by the desire to enable parallel test to maximize manufacturing throughput. New thermal control techniques will be needed for wafer probe and component test. DFT to enable test of device pins not contacted by the interface and test equipment.
Test Methodologies	New DFT techniques (SCAN and BIST have been the mainstay for over 20 years). New test methods for control and observation are needed. Tests will need to be developed utilizing the design hierarchy. Analog DFT and BIST techniques must mature to simplify test interface requirements and slow ever increasing instrument capability trends Logic BIST techniques must evolve to support new fault models, failure analysis, and deterministic test. EDA tools for DFT insertion must support DFT selection with considerations for functionality, coverage, cost, circuit performance and ATPG performance.
Defect Analysis	Defect types and behavior will continue to evolve with advances in fabrication process technology. Fundamental research in existing and novel fault models to address emerging defects will be required. Significant advances in EDA tools for ATPG capacity and performance for advanced fault models and DFT insertion are required to improve efficiency and reduce design complexities associated with test.
Failure Analysis	Realtime analysis of defects in multi-layer metal processes is needed. Failure analysis methods for analog devices must be developed and automated. Transition from a destructive physical inspection process to a primarily non-destructive diagnostic capability. Characterization capabilities must identify, locate, and distinguish individual defect types.
Disruptive Device Technologies	Develop new test methods for MEMS and sensors. Develop new fault models for advanced/disruptive transistor structures.

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PROCESS INTEGRATION, DEVICES, AND STRUCTURES

The 2004 update for the Process Integration, Devices and Structures (PIDS) section of the ITRS has minor changes and corrections from the 2003 edition. The most notable change is that in the long-term technology requirements tables, the years 2011, 2014, and 2017 have been added, so that all years from 2010 through 2018 are now included. As expected, the parameter values for these added years are generally close to midway between the values for the previous and succeeding years. In Figure 23, which is for low standby power logic, the curve for maximum allowed gate leakage current density (labeled "Jg,limit") has been corrected. In the 2003 edition, this curve was low by a factor of 2 to 3. Even with the correction, the implication of the figure is unchanged, that oxynitride gate dielectric is projected to be unable to meet the gate leakage current limits by 2006.

Table 46a Process Integration Difficult Challenges—Near-term

Difficult Challenges ≥ 45 nm/Through 2010	*Summary of Issues*
1. High-performance applications: meeting performance and power dissipation requirements for highly scaled MOSFETs	Cost effectiveness, process control, and reliability of very thin oxy-nitride gate dielectrics, especially considering the high gate leakage Difficulty in controlling short-channel effects for highly scaled devices Negative impact of high channel doping needed for highly scaled devices. Also, the difficulty in controlling threshold voltage due to statistical fluctuations in the doping Need to reduce series S/D parasitic resistance Controlling static power dissipation in the face of rapidly increasing leakage: architecture and circuit design improvement and innovation will be needed.
2. Low-power applications: meeting performance and leakage requirements for highly scaled MOSFETs	Early availability of manufacturing-worthy high-κ gate dielectrics is necessary to meet stringent gate leakage and performance requirements. Slow scaling of V_{dd} for low standby power logic will make overall device scaling difficult. Rapid scaling of V_{dd} for low operating power logic will make overall device scaling difficult.
3. Assuring the reliability and implementing into manufacturing of multiple material, process, and structural changes in a relatively short period of time	Multiple material changes projected: high-κ gate dielectric, metal gate electrodes, strained Si, nickel silicide by 2008 or so Elevated S/D (selective epi) Ultra-thin body (UTB) SOI by 2008 or so, followed by multiple-gate structures. Near mid-gap metal gate electrodes will be desirable to set the threshold voltage for UTB SOI. Difficulty in ensuring reliability of all these new materials, processes, and structures in a timely manner

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Table 46a Process Integration Difficult Challenges—Near-term (continued)

4. Implementation of DRAM, SRAM, and high-density nonvolatile memory (NVM) for scaled technologies	DRAM main issues—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities with scaling. Also, difficult lithography and etch issues with scaling NVM, flash—Scaling of tunnel dielectric and interpoly dielectric involves many complex tradeoffs. Dielectric material properties and dimensional control are key issues NVM, FeRAM—Ferroelectric material properties and dimensional control. Sensitivity to IC processing temperatures and conditions NVM, SONOS—ONO stack dimensions and material properties, including nitride layer trap distribution in space and energy NVM, MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions
5. High-performance and low-cost RF and analog/mixed-signal solutions	Signal isolation Optimizing RF/analog CMOS devices with scaled technologies: mismatch, 1/f noise, and leakage with high-κ gate dielectrics High density integrated passive element scaling and use of new materials: Q-factor value for inductors; matching and linearity for capacitors Reduced power supply voltages: degradation in SNR (signal-to-noise ratio) and signal distortion performance Reduced device breakdown voltage in scaled technologies High-frequency devices with increased operating voltage for base station applications Compound semiconductor substrates with good thermal dissipation and process equipment for fabrication at low cost See section on RF and A/MS Technologies for Wireless Communications for detailed discussion of these issues

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Table 46b Process Integration Difficult Challenges—Long-term

Difficult Challenges < 45 nm/Beyond 2010	*Summary of Issues*
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate, ultra-thin body [UTB] MOSFETs) with lightly doped body will be needed to effectively scale MOSFETs to well under 20 nm gate length (L_g). Most likely, advanced material solutions such as strained Si (enhanced mobility) channels, elevated source/drain, high-κ gate dielectric, metal gate electrode, etc., will be utilized along with the advanced non-classical CMOS Particularly for the highly scaled UTB MOSFETs required towards the end of the Roadmap, with body thickness well under 10 nm, electrical performance and the impact of quantum effects are not well understood To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced carrier saturation velocity appears to be needed See Emerging Research Devices section for more detail.
7. Dealing with atomic-level fluctuations and statistical process variations in sub-20 nm MOSFETs	Fundamental issues of atomic-level statistical fluctuations for sub-20 nm MOSFETs are not completely understood, including the impact of quantum effects.
8. Identifying, selecting, and implementing new memory structures	Highly scaled, dense, fast, non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness, attaining the very low leakage currents that will be required, and reducing the cell area factor All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc,) are currently unclear.
10. Toward the end of the Roadmap or beyond, identification, selection, and implementation of advanced, beyond-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of beyond-CMOS devices need to extend well beyond CMOS limits. Beyond-CMOS devices need to integrate into a CMOS platform. Integration of the two may be difficult, especially for mixed signal. See Emerging Research Devices sections for more discussion and detail.

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EMERGING RESEARCH DEVICES

Table 58 Emerging Technologies Difficult Challenges

Difficult Challenges≥45 nm/Through 2009	*Summary of Issues*
Implementation into manufacturing of non-classical MOSFET device structures integrated with new materials and processes (for example, a strained silicon channel integrated with a new high-κ gate dielectric material)	Selection of most promising device structure(s) and/or materials technologies ["Technology Booster(s)"] to sustain the required annual 17% increase in performance Introduction of two or more "Technology Booster" options (material, process, and/or device structure changes) simultaneously in a single node
Development and implementation into manufacturing of a non-volatile memory technology combining the best performance features of both volatile and non-volatile memory technologies for both stand-alone and embedded applications	Realization of a manufacturable, cost-effective fabrication technology for electrically accessible high-speed, high-density non-volatile RAM integrable with the fabrication process flow for CMOS logic
Difficult Challenges <45 nm/Beyond 2009	
Toward the end of CMOS scaling or beyond, discovery, reduction to practice, and implementation into manufacturing of novel, non-CMOS devices and architectures integrated (monolithically, mechanically, or functionally) with a CMOS platform technology	Discovery and reduction to practice of new information processing technologies integrable with silicon CMOS Discovery and reduction to practice of new, low-cost methods of manufacturing novel information processing technologies

Table ERM-1 Emerging Research Materials Difficult Challenges ADDED

Difficult Challenges< 32 nm/Beyond 2009	***Summary of Issues***
The characterization of critical material properties at the nanometer scale for both charge transport and non-charge transport based devices is very limited and may hinder our ability to improve materials properties.	**The primary tools to extract properties at the nanometer scale are SEM, TEM, AFM, and STEM, and these measure structural information, so critical materials properties are not measured at these dimensions.** **Characterization of the 2D/3D chemical, structural, electronic, and atomic bonding at the nanometer scale is very difficult and not possible in some cases.** **At the nanometer scale, the separation of "bulk" and interface properties will be very difficult, because the surface becomes a large part of the material.**
As materials become smaller, identifying contact materials that don't damage the bonding in the molecule or material may limit the ability to fabricate functional devices.	**Metals that form contacts chemically react with the material and this generates energy that can break other bonds.** **Very few metals form bonds to carbon and these usually form carbides, which may be more resistive materials, and this may limit the contact resistance to molecules and carbon nanotubes.**
For modeling and simulation to predict the right trends of properties of nanometer sized materials, correct physical models must be developed.	**Modeling tools are very inaccurate in predicting excited states and these are critical in modeling transport through materials or across interfaces.** **Correlation effects become significant at small material size and these are not modeled**

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RF AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

Analog and Mixed Signal: The technology requirements are now aligned for analog speed devices with the LSTP roadmap instead of, as in the past, with the LOP roadmap. It is becoming more challenging to keep a constant ratio of transconductance *gm* to drain conductance *gds* for high performance analog devices in new technologies. The challenges for reducing 1/f noise in high-k gate dielectrics are relaxed to a color coding of "yellow" from "red." However, 1/f noise in high-k gate dielectrics still remains challenging. The published reports about solutions for high density capacitors meeting density, leakage, and matching specifications suggested changes to capacitor color coding for the 2004 ITRS update from red to yellow for the years 2013 to 2016.

RF Transceivers: Similar to the Near Term Table, a lag between RFCMOS gate length and BiCMOS gate length now occurs in the Long Term Table. For RFCMOS, the technology requirements maintained one-year lag from the LSTP CMOS roadmap.

Power Amplifiers & Power Management: The major trends appear to have been correctly anticipated in 2003 for handsets. The first two RFCMOS Dual Band GSM power amplifiers (PAs) were sampled by cellular customers in 2004. These PAs are not expected to be players in the market until 2005. However, RFCMOS PAs could play a major role in 2006. The success of RFCMOS PA's may erode price margins at a faster rate than anticipated. Multi-band cellular SiGe PAs also are being sampled. Highly integrated modules with multi-layer laminates of low temperature cintered ceramics (LTCC) are dramatically reducing total RF front-end area. The cost ($$/Watt) for base station PAs will decrease more rapidly than shown in the 2003 Roadmap and are expected to reach $0.40 per watt in 2008. Saturated power density (W/mm) of all technologies will increase more rapidly and will reach 1.4 W/mm, 1.8 W/mm, 3 W/mm, and 5 W/mm by 2008 for LDMOS, GaAs, SiC, and GaN, respectively. Manufacturing solutions now exist for 28V GaAs FET's, 60W SiC FET's, and 28 V GaN FET's. Linear operation is expected to achieve less than half the RF power of saturated operation. In the 2003 Roadmap, linear operation was expected to achieve half the RF power of saturated operation.

Millimeter Wave (10-100GHz): There are no major changes for the 2004 Update. InP HBTs are expected to advance more quickly due to aggressive R&D funding than they were predicted to do so in the 2003 ITRS. The 2005-2006 color coding for all InP HBT device requirements are changed from yellow to white. Also, the 2007-2008 figures of merit for device fT and fMAX are more aggressive. Copper interconnects are expected to be introduced in 2007. The use of today's gold and aluminum interconnects is expected to continue until at least 2009.

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FRONT END PROCESSES

The 2004 FEP ITRS update presents a refinement of the 2003 Roadmap in several areas. These areas include timing of 450mm wafer introduction, accelerated introduction of SOI, back surface particle metrics, gate CD tolerance, gate dielectric leakage current, and the co-introduction of metal gate electrodes and high-k gate dielectrics. In addition, other typographical mistakes and inconsistencies have been corrected.

The projected introduction of 450mm wafers to manufacturing was not consistent across all working groups in the 2003 ITRS. This will be addressed and corrected in 2005. In the meantime, additional notes identifying this issue have been added to Table 68b and to the footnotes of Table 69.

Due to an improved outlook and accelerated introduction for SOI, the qualification/ and preproduction date for SOI has been moved to 2004 in figure 44, "Starting Materials Potential Solutions."

Following a survey of several IC fabs, the surface preparation team was able to add experience-based metrics for back surface particles that now appear in Tables 70a and 70b. The surface preparation team will continue to study this area and attempt to introduce yield-model-based metrics in 2005.

An industry survey was conducted in 2004 on the partitioning of gate CD tolerance. The survey revealed several important pieces of information: first, most manufacturers are not currently able to meet the 10% overall CD tolerance on the physical gate length; nor are they able to achieve the "ITRS-required" partitioning of this tolerance between litho and etch. Despite the fact that very few are able to achieve the tolerance, there is still a consensus that the "requirement" should be maintained, with different companies employing a work-around to be successful. Accordingly 2004 update reflects the same absolute tolerances and partitioning of those tolerances as the 2003 roadmap even though it is widely recognized that they are mostly not being met. The survey also revealed that the trimming of gate photoresist is more aggressive than is reflected by values in the table; however, dimensions in the photoresist are higher than the table values in many instances. At this writing, proposals are being considered for the 2005 roadmap that will relax the gate dimensions in exposed photoresist, while maintaining the same final, after-trim dimensions.

In the area of gate dielectric leakage currents, clarifications were added to table 71 and the associated footnotes. Allowable gate dielectric leakage is now specified at 100˚C and as a multiple of the device off-state leakage.

The footnotes to table 71 point out that there is a growing consensus that both high k and metal gates are likely to be introduced simultaneously, rather than staggered.

The expectation of higher mobility channels, built into the 2003 roadmap, came to fruition in 2004, validating the EOT values presented in 2003. In the 2003 ITRS, mobility enhanced channels allowed a slower reduction of EOT, thereby delaying the introduction date of high k.

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Table 68a Front End Processes Difficult Challenges—Near-term UPDATED

	MPU/ASIC Physical Gate Length ≥ 20 nm/ Through 2009	*Summary of Issues*
WAS	New gate stack processes and materials	Extension of oxynitride gate dielectric materials to < 1.0 nm E.O.T for high performance MOSFETs, consistent with device reliability requirements Introduction and process integration of high-κ gate stack materials and processes for high performance, low operating and low standby power MOSFETs CMOS integration of enhanced channel mobility, e.g., strained layers Control of boron penetration from doped polysilicon gate electrode Minimized depletion of dual-doped polysilicon electrodes Introduction of dual metal gate electrodes with appropriate work function (toward end of period) Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization
IS	New gate stack processes and materials	Extension of oxynitride gate dielectric materials to < 1.0 nm E.O.T for high performance MOSFETs, consistent with device reliability requirements Introduction and process integration of high-k gate stack materials and processes for high performance, low operating and low standby power MOSFETs CMOS integration of enhanced channel mobility, e.g., strained layers Control of boron penetration from doped polysilicon gate electrode **Control of silicon loss at spacer etch and gate etch needs to be much tighter on thin SOI and SiGe wafers, where the total silicon thickness is 20-50 nm** Minimized depletion of dual-doped polysilicon electrodes **Removal of high K dielectric without loss of the underlying silicon, especially in the case of SOI or non planar devices** Introduction of dual metal gate electrodes with appropriate work function (toward end of period) Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization
	Critical dimension and effective channel length (L_{eff}) control	Control of gate etch processes that yield a physical gate length that is smaller than the feature size printed in the resist, while maintaining <10% overall 3-sigma control of the combined lithography and etch processes Control of profile shape, edge roughness, line and space width for isolated as well as closely-spaced fine line patterns Control of self-aligned doping processes and thermal activation budgets to achieve L_{eff} control Maintenance of CD and profile control throughout the transition to new gate stack materials and processes CD and etch metrology Site flatness to ensure effective lithographic printing

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Table 68a Front End Processes Difficult Challenges—Near-term UPDATED (continued)

MPU/ASIC Physical Gate Length ≥ 20 nm/ Through 2009	*Summary of Issues*
Introduction and CMOS integration of new memory materials and processes	Development and introduction of very high-κ DRAM capacitor dielectric layers Migration of DRAM capacitor structures from silicon-insulator-metal to metal-insulator-metal Integration and scaling of FeRAM ferroelectric materials Scaling of Flash inter-poly and tunnel dielectric layers may require high κ Limited temperature stability of high-κ and ferroelectric materials challenges CMOS Integration
Surfaces and interfaces—structure, composition, and contamination control	Contamination, composition, and structure control of channel/gate dielectric interface as well as gate dielectric/gate electrode interface Interface control for DRAM capacitor structures Maintenance of surface and interface integrity through full-flow CMOS processing Statistically significant characterization of surfaces having extremely low defect concentrations for starting materials and pre-gate clean surfaces
Scaled MOSFET dopant introduction and control	Doping and activation processes to achieve shallow source/drain regions having parasitic resistance that is less than ~17–33% of ideal channel resistance ($=V_{dd}/I_{on}$) Control of parasitic capacitance to achieve less than ~23–29% of gate capacitance, consistent with acceptable Ion and minimum short channel effect Achievement of activated dopant concentration greater than solid solubility in dual-doped polysilicon gate electrodes Formation of continuous self-aligned silicide contacts over shallow source and drain regions Metrology issues associated with 2D dopant profiling

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Table 68b Front End Processes Difficult Challenges—Long-term UPDATED

	MPU/ASIC Physical Gate Length <20 nm/ Beyond 2009	*Summary of Issues*
WAS	Continued scaling of planar CMOS devices	Higher κ gate dielectric materials including temperature constraints Metal gate electrodes with appropriate work function Sheet resistance of clad junctions CD and Leff control Chemical, electrical, and structural characterization
WAS	Introduction and CMOS integration of non-standard, double gate MOSFET devices	Devices are needed starting from 2011 and may be needed as early as 2007 (this is a backup for high-κ materials and metal gates on standard CMOS) Selection and characterization of optimum device types CMOS integration with other devices, including planar MOSFETs. Introduction, characterization, and production hardening of new FEP unit processes Device and FEP process metrology Increased funding of long term research Role of SOI utilization (and structural configuration) for advanced non-classical CMOS
IS	Introduction and CMOS integration of non-standard, double gate MOSFET devices	Devices are needed starting from 2011 and may be needed as early as 2007 (this is a backup for high-k materials and metal gates on standard CMOS) Selection and characterization of optimum device types. CMOS integration with other devices, including planar MOSFETs Introduction, characterization, and production hardening of new FEP unit processes. Device and FEP process metrology Increased funding of long term research **Role of SOI and strained silicon utilization (and structural configuration) for advanced non-classical CMOS**
WAS	Starting silicon material alternatives greater than 300 mm diameter require the start of wafer manufacturing development in year 2003	Need for future productivity enhancement dictates the requirement for a next generation, large silicon substrate material Historical trends suggest that the new starting material have nominally twice the area of present generation substrates, e.g., 450 mm. Economies of the incumbent Czochralski crystal pulling, wafer slicing, and polishing processes are questionable beyond 300 mm; research is required for a cost-effective substrate alternative to bulk silicon If 450 mm wafers are to become available for production in 2011 as currently forecasted, wafer-manufacturing development should be implemented eight years earlier, e.g., 2003.
IS	Starting silicon material alternatives greater than 300 mm diameter require the start of wafer manufacturing development in year 2005	Need for future productivity enhancement dictates the requirement for a next generation, large silicon substrate material Historical trends suggest that the new starting material have nominally twice the area of present generation substrates, e.g., 450 mm. Economies of the incumbent Czochralski crystal pulling, wafer slicing, and polishing processes are questionable beyond 300 mm; research is required for a cost-effective substrate alternative to bulk silicon. **If 450 mm wafers are to become available for production in 2011 as currently forecasted, wafer manufacturing is already behind schedule and must be implemented in 2004-2005.** **Enhanced coordination is required amongst Starting Materials, Factory Integration, Yield Enhancement and the IRC to more effectively assess the anticipated onset of 450 mm use.**

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Table 68b Front End Processes Difficult Challenges—Long-term UPDATED (continued)

MPU/ASIC Physical Gate Length <20 nm/ Beyond 2009	*Summary of Issues*
New memory storage cells, storage devices, and memory architectures	Scaling of DRAM storage capacitor beyond $6F^2$ Further scaling of Flash memory interpoly and tunnel oxide thickness FeRAM storage cell scaling Introduction of new memory types and storage concepts (Candidates—MRAM, phase-change memory for 2010, and single electron, molecular, nano-floating products beyond 2010)
Surface and interface structural, contamination, and compositional control	Achievement and maintenance of structural, chemical, and contamination control of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface Metrology and characterization of surfaces that may be horizontally or vertically oriented relative to the chip surface Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface

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LITHOGRAPHY

In the 2004 update of the ITRS Lithography tables, no significant changes were made to the coloring or values in the overall lithography requirements tables other than adding a definition of overlay. For the long term, solutions are not known to reach the overall lithographic requirements for resolution combined with adequate overlay or CD control for any circuit type with any known lithographic technology. The lithography working group has participated in discussion with working groups developing other chapters to define CD control requirements. The US and Japan working groups separately conducted simulation studies that concluded that <4nm 3σ CD control has no known solutions with any technology presently being developed. The simulations also predict that if the gate length in resist were increased, CD control would be improved. However, this change would require larger post-development linewidth reduction using reactive ion etching or other processes.

Significant changes were made to the tables on difficult challenges and potential solutions. In developing the 2004 update, working group members defined new criteria for evaluating near-term potential solutions. Solutions shown in the table for the present and next two nodes must address leading edge requirements in at least two geographic regions, and all infrastructure including resist and mask must be ready for the timing of the node. Solutions for three nodes or more in the future are somewhat more broad ranging and inclusive to encourage continued innovation. With these criteria 193nm wavelength exposure systems, including 193nm immersion systems, became dominant solutions for the next two nodes; in addition, 157-nm wavelength exposure was only listed with immersion as a less likely option. Furthermore, immersion lithography appears as potential solution at the 32-nm and 22-nm nodes. In the difficult challenges tables, stronger emphasis was placed on challenges related to immersion lithography. Continued emphasis was placed on challenges for implementing cost-effective post-optical lithography solutions.

Many individual parameters for masks and resist were evaluated, and colors or values were changed. In the tables of mask requirements, the scaling of data volume requirements was delayed by one year. Manufacturing solutions are also available for mask protection and for achieving phase and transmission control for attenuated phase shift masks in 2007 since the use of 157-nm wavelength technology is not likely before the 45-nm node. Pellicles and phase-shifting materials are mature for use with 193-nm wavelength exposure. Minor changes were made to the EUV and EPL mask tables. In the resist tables, thickness requirements for single layer and ultrathin layer resist strategies were merged since resist thickness will need to be less than 300nm to maintain aspect ratio values where the resist doesn't collapse. The range of resist dose for 193-nm wavelength exposure was increased, and the dose values for electron beam exposure were adjusted to account for sensitivity differences in resist for exposure with low and high beam energies. Furthermore, the definition of line width roughness was adjusted to account for metrology precision.

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Table 76 Lithography Difficult Challenges UPDATED

	Five Difficult Challenges/ ≥ 50 nm Through 2009	*Summary of Issues*
WAS	Optical masks with features for resolution enhancement and post-optical mask fabrication	--Registration, CD control, defectivity, and 157 nm pellicles; defect free multi-layer EUV substrates or EPL membrane masks --Equipment infrastructure (writers, inspection, repair)
IS	Optical masks with features for resolution enhancement and post-optical mask fabrication	**--Registration, CD control, defect control for optical masks** **--Development of defect free multi-layer EUV mask blanks or EPL membrane masks** **--Equipment infrastructure (writers, inspection, repair)** **--Data volume**
WAS	Cost Control and Return on Investment (ROI)	--Achieving constant/improved ratio of tool cost to throughput over time --Cost-effective resolution enhanced optical masks and post-optical masks --Sufficient lifetimes for the technologies --Resources for developing multiple technologies at the same time --High output, cost-effective, EUV light source
IS	Cost Control and Return on Investment (ROI)	**--Achieving constant/improved ratio of exposure related tool cost to throughput over time** **--Cost-effective resolution enhanced optical masks and post-optical masks** **--Sufficient lifetimes for exposure tool technologies** **--Resources for developing multiple technologies at the same time** **--ROI for small volume products**
WAS	Process Control	--Processes to control gate CDs to less than 1.8 nm (3 sigma) --New and improved alignment and overlay control methods independent of technology option to < 19 nm overlay --Accuracy of OPC
IS	Process Control	**--Processes to control gate CDs to less than 4nm (3 sigma)** **--New and improved alignment and overlay control methods independent of technology option to < 19 nm overlay** **--Accuracy of OPC, especially in presence of polarization effects** **--Control of flare in exposure tool** **--Lithography friendly design and design for manufacturability**
WAS	Resists for ArF, Immersion Lithography and F_2	--Outgassing, LER, SEM-induced CD changes, defects ≥ 30 nm.
IS	**Resists for 193nm and 193nm immersion lithography**	**--Outgassing and leaching during immersion** **--Reduction of line edge and line width roughness** **--Finding and eliminating defects >30nm in size** **--Reducing SEM-induced CD changes**
~~**Delete**~~	~~CaF_2~~	~~--Yield, cost, quality~~
IS	**Defect control**	**--Control of defects caused in immersion environment**

Table 76 Lithography Difficult Challenges (continued)

	Five Difficult Challenges/ < 45 nm Beyond 2010	
WAS	Mask Fabrication and Process Control	--Defect-free NGL masks --Equipment infrastructure (writers, inspection, repair) --Mask process control methods
IS	Mask Fabrication and Process Control	**--Defect-free NGL masks, especially for 1X masks for nanoimprint and EUVL mask blanks free of printable defects** **--Timeliness and capability of mask equipment infrastructure (writers, inspection, repair), especially for 1X masks** **--Mask process control methods and yield enhancement** **--Pellicles for 157nm immersion and protection of EUVL masks from defects without pellicles**
WAS	Metrology and Defect Inspection	--Capability for critical dimensions down to 7 nm and metrology for overlay down to 7.2 nm, and patterned wafer defect inspection for defects < 30 nm
IS	Metrology and Defect Inspection	**--Resolution and precision for critical dimension measurement down to 7 nm, including metrology for 2.2nm 3 sigma line width roughness** **--Metrology for overlay down to 7.2 nm** **--Defect inspection for patterned wafers for defects < 30 nm**
WAS	Cost Control and ROI	--Achieving constant/improved ratio of tool cost to throughput --Development of cost-effective post-optical masks --Achieving ROI for industry with sufficient lifetimes for the technologies
IS	**Cost Control and return on investment (ROI)**	**--Achieving constant/improved ratio of exposure related tool cost to throughput** **--Development of cost-effective optical and post-optical masks** **--Achieving ROI for industry with sufficient lifetimes for exposure tool technologies and ROI for small volume products**
WAS	Gate CD Control Improvements, Process Control, Resist Materials	--Development of processes to control gate CDs < 1 nm (3 sigma) with appropriate line-edge roughness --Development of new and improved alignment and overlay control methods independent of technology option to < 7.2 nm overlay
IS	Gate CD Control Improvements, Process Control, Resist Materials	**--Development of processes to control gate CDs < 4 nm (3 sigma) with appropriate line-edge roughness** **--Development of new and improved alignment and overlay control methods independent of technology option to < 7.2 nm overlay, especially for nanoimprint** **--Process control and design for low k1 lithography** **--Resists with high index of refraction, high index fluids and high index optical materials to extend optical immersion to its limits** **--Limits of chemically amplified resist sensitivity for <50-nm linewidths due to acid diffusion length**
WAS	Tools for Mass Production	--Optical and NGL exposure tools capable of meeting requirements of the Roadmap --EUV sources with power sufficient for high throughput
IS	Tools for Mass Production	**--Optical and NGL exposure tools capable of meeting requirements of the ITRS** **--High output, cost-effective EUV sources** **--CaF2 cost, yield, and quantity for 157nm immersion**

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INTERCONNECT

In general the 2004 ITRS Interconnect requirements tables will change very little from the numbers published in 2003. However, there are additions and expansions of some metrics that are intended to clarify specific interconnect issues.

- There has been further clarification of what is meant by "Metal 1" as opposed to "local wiring." In the latest chapter, the deteriorating resistivity of copper wires, as linewidth decreases, is highlighted.
- For Logic, additional Cu resistivity numbers are being added to reflect the effect of surface or sidewall scattering. A model, which incorporates resistivity of copper ρ o = constant 1.9 $\mu\Omega$-cm at 300 K, a mean free path of charge carriers $\lambda = 3.4 \times 10^{-6}$cm (34nm), a wire width W (cm), a probability for reflection of electrons at the grain boundaries of 0.2, and the portion, p, of electrons specularly reflected from the walls (surface or interface), has been used to generate a series of new metrics in the Technology requirements tables (81a and 81b. The new metrics tabulate the impact to line resistivity at; Metal 1, intermediate, and global wiring. In these tables, interconnect delay (ps) is calculated for a one mm copper wire, assuming width dependent scattering (as described above) and a conformal barrier of thickness specified in the table. For the first time in the past 10 years, the low κ portion of the roadmap was unaltered (κ value targets not delayed) with respect to the prior edition. Small changes were made to the shading of the boxes for bulk and effective dielectric constant over the next five years, recognizing that materials that deliver an effective κ =2.7 are in production today, and those material systems that will deliver an effective κ = 2.4 are expected to be available with manufacturable solutions in the next three years.
- The proposed changes for DRAM are relatively minor and center on the contacts. There are some changes in specific via and contact resistivity, with the contact A/R rising to >20 in 2018. This is now a "red" challenge associated with 16 nm DRAM half pitch. Cu has been delayed to 2007. The need to distinguish the requirements for embedded, Flash, and traditional DRAM was identified by the committee, but will not be addressed until the next major revision in 2005.
- In the Interconnect surface cleans tables, the notes clarifying the contributors to damage due to rework, strip, and clean, have been updated.

In assessing the Interconnect roadmap as a whole, however, it still becomes almost entirely "red bricks" (red = "no known solution") by the end of this decade. No new discoveries or major breakthroughs have occurred in the year since closing the 2003 roadmap to change the outlook.

Table 80 Interconnect Difficult Challenges

Five Difficult Challenges ≥45 nm/Through 2009	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures compatible with new materials and processes*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool.
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling and control of failure mechanisms will be key.
Three-dimensional control (3D CD) of interconnect features (with its' associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Five Difficult Challenges <45 nm/Beyond 2009	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control (3D CD) of interconnect features (with its' associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual-Damascene metal structures and DRAM at nano dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address global wiring scaling issues*	Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

* *Top three challenges*

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FACTORY INTEGRATION

The International Technology Roadmap for Semiconductors (ITRS) is a 15 year roadmap that analyzes the industry's difficult challenges and technology requirements and then formulates potential solutions to meet these needs. The pace of technology is governed by the desire to stay on Moore's law, reduce cost per function by 30% per year [historic norms], and deliver new and compelling IC devices that continue our industry's growth.

While most of the ITRS focuses on process technology, the objective of the Factory Integration chapter is to ensure that our factories fully integrate physical and data elements of the factories to enable the development and high volume running of these process technologies so that the right products are made in the right volumes on schedule, while meeting cost targets. Historically, cost per function has been reduced through a technology advances such as device feature size reductions, yield improvement to near 100% and wafer size increases (i.e. 300mm wafers). It is expected that improvements in manufacturing productivity will play an even greater future role in reducing time to money and getting the most out of the factory investment. The need for future break-through technologies and capabilities that radically improve semiconductor factory design and manufacturing has never been greater. The scope of factory integration covers operations, AMHS, information systems, facilities and equipment in the fab area.

The focus for the FI team this year is to review difficult challenges, update technology requirements table, potential solutions table and to identify key focus areas to work on. For year 2004, the difficult challenges remained the same and most of the technology requirements and potential solutions table were unchanged except for small changes. However, the team identified the following 9 focus areas including AMC, 450mm wafer transition, etc.:

2004 ITRS FI focus areas:

- Airborne Molecular Contamination (AMC) Implications at < 45nm process technologies (Now → 2006)
- Implications of Relaxed Fab Facility Cleanliness (Now →)
- Litho EUV: Design for Manufacturability (2006 → 2010?)
- Fab Point of Use vs. Bulk Systems (Now →)
- Rapid Equipment Install and Qualification (Now →)
- Integrated Metrology Guidelines (Now →)
- Wafer and Unit Traceability from Fab through Packaging (Now →)
- "Proactive Visual" manufacturing (Now →)
- 450mm Wafer Size Transition (2005 → 2012)

The team is currently working on selecting top 3-4 focus areas in order to put together sub-teams to define the impact of these focus areas on FI and also on other cross-cut ITRS chapters.

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Table 84a Factory Integration Difficult Challenges—Near-term

Difficult Challenges ≥ 45 nm/Through 2009	*Summary of Issues*
Responding to Rapidly Changing, Complex Business Requirements	Many new and co-existing business models including IDM, Foundry, Joint Ventures, Collaborations, other Outsourcing, etc Increased expectations by customers for faster delivery of new and volume products Need for improve integration of the entire product design and manufacturing process Faster design -> prototype and prototype -> volume production Enhanced customer visibility into outsourced production operations Reduced time to ramp factories, products, and processes to stay competitive within the rapidly changing business environment Building 30+ mask layer System on a Chip (SoC) with long cycle times where needs are rapidly changing Rapid and frequent factory plan changes driven by changing business needs Ability to model factory performance so that output can be optimized Ability to constantly adjust equipment loading to keep the factory profitable Need to run globally disparate factories as single "virtual factory"
Achieving Growth Targets while Margins are Declining	Implications of rising wafer, packaging, and other materials cost on meeting cost targets Meeting high factory yield much faster at startup Addressing increased complexity while keeping costs in check Reducing complexity and waste across the supply chain Inefficiencies introduced by non-product wafers (NPW) competing for resources with production wafers High cost and cycle time of mask sets for manufacturers impacting affordability of new product designs Increasing dedication of masks and equipment causing manufacturing inefficiencies Challenges introduced with sharing of mask sets Difficulty maintaining the historical 0.7× transistor shrink per year for die size and cost efficiency
Managing Ever Increasing Factory Complexity	Quickly and effectively integrating rapid changes in process technologies Managing carriers with multiple lots, wafers with multiple products, or multiple package form factors Comprehending increased purity requirements for process and materials Need to run aluminum and copper back end in the same factory Increasing number of processing steps coupled with process and product complexity Need to concurrently manage new and legacy software systems and systems with increasingly high interdependencies Explosive growth of data collection/analysis requirements driven by process and modeling needs Increased requirements for wafer level tracking and die level tracking
Meeting Factory and Equipment Reliability, Capability or Productivity Requirements per the Roadmap	Process equipment not meeting availability, run rate, and utilization targets out of the box Stand alone and integrated reliability for equipment and systems to keep factories operating Increased impacts that single points of failure have on a highly integrated and complex factory Quality issues with production equipment embedded controllers Lack of good data to measure equipment and factory effectiveness for optimization and improvement programs Factory capacity planning and supply chain management systems are not continuously base lined with actual factory data creating errors Lack of migration paths which inhibit movement from old inefficient systems to new highly productive systems

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Table 84b Factory Integration Difficult Challenges—Long-term

Difficult Challenges ≥ 45 nm/Through 2009	*Summary of Issues*
Meeting the Flexibility, Extendibility, and Scalability Needs of a Cost-effective, Leading-edge Factory	Need to quickly convert factories to new process technologies while reusing equipment, facilities, and skills Minimizing downtime to on-going operations while converting factories to new technologies Scalability implications to meet large 300 mm factory needs [50K WSPM] Continued need to improve both throughput and cycle time Reuse of building, production and support equipment, and factory information and control systems across multiple technology nodes Understanding up-front costs to incorporate EFS Ability to convert 200 mm facilities to 300 mm wafer size Comprehending increased purity requirements for process and materials Accelerating the pace of standardization to meet industry needs
Meeting Process Requirements at 65 nm and 45 nm Nodes Running Production Volumes	Small process windows and tight process targets at 65 nm and 45 nm nodes in many modules make process control increasingly difficult Complexity of integrating next generation lithography equipment into the factory Overall development and volume production timelines continuing to shrink Device and process complexity make the ability to trace functional problems to specific process areas more difficult Difficulty in running different process parameters for each wafer while maintaining control windows and cycle time goals Reducing the impacts of parametric variation
Increasing Global Restrictions on Environmental Issues	Need to meet regulations in different geographical areas Need to meet technology restrictions in some countries while still meeting business needs Comprehending tighter ESH/Code requirements Lead free and other chemical and materials restrictions New material introduction
Difficult Challenges < 45 nm/2010 Through 2018	*Summary of Issues*
Post-conventional CMOS Manufacturing Uncertainty	Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements will have on factory design Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency Need to run CMOS and post CMOS processes in the same factory
Emerging Factory Paradigm and Next Wafer Size Change	Uncertainty about the next wafer size [450 mm] and the conversion timing [See Backup material as a link in the electronic chapter at http://public.itrs.net.] Traditional strategies to scale wafers and carriers for the next wafer size conversion may not work with [450 mm] 25 wafer carriers and drive significant production equipment and material handling changes Uncertainty concerning how to reuse buildings, equipment, and systems to enable the next wafer size conversion [to 450 mm] at an affordable cost

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ASSEMBLY AND PACKAGING

The 2004 Assembly and Packaging Roadmap updates focused on three primary areas; expansion on the difficult challenges, new materials challenges, and changes in the near term package cost roadmap. In the difficult challenges tables focus has been increased on to need to close the gap between on chip interconnect and chip to chip interconnect in packages. This problem is seen as becoming more severe as chip interconnect continues to shrink at a faster rate than package based interconnect limiting the benefits of chip scaling. Longer term the packaging challenge of new MEMS, nanostructure, and emerging device technologies will also become very critical and have been identified as a critical research area for the industry. The materials challenges where expanded to include new lead free requirements, dielectrics for imbedded passives, organics which are compatible with higher temperature lead free solder assembly operations. The projections on future cost reductions in the low end were also modified to reflect the slow down in cost reduction. This is due to increasing material cost and the maturity of many package types. To put packaging industry back on an aggressive cost reduction curve completely new approaches are required which have not yet been identified.

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Table 92a Assembly and Packaging Difficult Challenges—Near-term UPDATED

	Difficult Challenges ≥ 45 nm/Through 2010	Summary of Issues
WAS	Improved Organic Substrates	Tg compatible with Pb free solder processing Increased wireability at low cost Improved impedance control and lower dielectric loss to support higher frequency applications Improved planarity and low warpage at higher process temperatures Low-moisture absorption Low-cost embedded passives Substrate cost is barrier to flip chip wide spread adoption today Increased via density in substrate core Alternative plating finish to improve reliability
IS	**Close gap between Chip and substrate -** Improved Organic Substrates	Tg compatible with Pb free solder processing Increased wireability at low cost Improved impedance control and lower dielectric loss to support higher frequency applications Improved planarity and low warpage at higher process temperatures Low-moisture absorption Low-cost embedded passives, **R. L, C** **Embedded active devices** Substrate cost is barrier to flip chip wide spread adoption today Increased via density in substrate core Alternative plating finish to improve reliability **Solutions for operation temp up to 200C** **Interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology** **Production techniques will require silicon-like production and process technologies after 2005.**
WAS	Improved Underfills for Flip Chip on Organic Substrates	Thermal performance and thermal coupling between parts Materials which enable integration of SMT, varying semiconductors, and substrate types reliably Thin die, stack die, very large and very small die, passives component integration, SAW, shielding interconnect process Narrowing gaps Higher bump densities
Delete	~~Improved Underfills for Flip Chip on Organic Substrates~~	~~Thermal performance and thermal coupling between parts~~ ~~Materials which enable integration of SMT, varying semiconductors, and substrate types reliably~~ ~~Thin die, stack die, very large and very small die, passives component integration, SAW, shielding interconnect process~~ ~~Narrowing gaps~~ ~~Higher bump densities~~
	Coordinated Design Tools and Simulators to address Chip, Package, and Substrate Co-design	Mix signal co-design and simulation environment Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis Electrical (power disturbs, EMI, signal integrity associated with higher frequency/current and lower voltage switching) Commercial EDA supplier support System level co-design is needed now. EDA support for "native" area array is required to meet the Roadmap projections. Educational programs required to train engineers in these technologies/requirements.

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Table 92a Assembly and Packaging Difficult Challenges—Near-term UPDATED (continued)

	Difficult Challenges ≥ 45 nm/Through 2010	Summary of Issues
WAS	Impact of Cu/low κ on Packaging	Direct wirebond and bump to Cu Bump and underfill technology to assure low-κ dielectric integrity Improved mechanical strength of dielectrics Interfacial adhesion Reliability of first level interconnect with low κ Mechanisms to measure the critical properties need to be developed. Probing over copper/low κ due to damage and bonding over probe mark
IS	Impact of **BEOL incl** Cu/low κ on Packaging	Direct wirebond and bump to Cu or improved barrier systems bondable pads Bump and underfill technology to assure low-κ dielectric integrity **including lead free solder bump system** Improved mechanical strength of dielectrics **and other interfaces** Interfacial adhesion Reliability of first level interconnect with low κ Mechanisms to measure the critical properties need to be developed. Probing over copper/low κ due to damage and bonding over probe mark
	High Current Density Packages	Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. Whisker growth Thermal dissipation
Add	**Flexible System Packaging**	**Conformal low cost organic substrates** **Small and thin die assembly** **Handling in low cost operation** **Different carrier materials (organics, silicon, ceramics, glass, laminat core) impact** **Establish infrastructure for new value chain** **Establish new process flows** **Reliability** **Testability** **Different active devices** **Electrical and optical interface integration**
	Wafer Level CSP	I/O pitch between 250um 400um less than 100 I/O solder joint reliability and cleaning processes for low stand-off Wafer thinning and handling technologies Compact ESD structures

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Table 92b Assembly and Packaging Difficult Challenges—Long-term UPDATED

	Difficult Challenges <45 nm/Beyond 2010	*Summary of Issues*
WAS	Package Cost does not follow the Die Cost Reduction Curve	-Margin in packaging inadequate to support investment required to reduce cost
WAS	Small Die with High Pad Count, High Power Density, and/or High Frequency	-Current density, operating temperature, etc for these devices exceed the capabilities of current assembly and packaging technology
IS	Small Die with High Pad Count, High Power Density, and/or High Frequency	-New solder/UBM with improved current density capabilities , operating temperature, etc for these devices exceed the capabilities of current assembly and packaging technology
	High Frequency Die	-Substrate wiring density to support >20 lines/mm '-Lower loss dielectrics—skin effect above 10 GHz" -Hot spot" thermal management needs to be addressed before 2007. There is a "brick wall" at five-micron lines and spaces. Design TWG would like to have an upper bound on thermal management capability of future packages.
WAS	Close Gaps between Substrate Technology and the Chip	-Interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology '-Production techniques will require silicon-like production and process technologies after 2005.
Delete	~~Close Gaps between Substrate Technology and the Chip~~	~~-Interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology~~ ~~'-Production techniques will require silicon-like production and process technologies after 2005.~~
	System-level Design Capability to Integrated Chips, Passives, and Substrates	-Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required. Hardware only '-This is also an issue before 2007.Embedded passives may be integrated into the "bumps" as well as the substrates.
	New Device Types (Organic, Nanostructures, Biological) that require New Packaging Technologies	-Organic device packaging requirements not yet define (will chips grow their own packages) '-Biological interfaces will require new interface types
	Bumpless area array technologies will be needed during this period. Face to face packages and other 3D packages are examples. High frequency, low power and low profile are driving forces	

ENVIRONMENT, SAFETY, AND HEALTH

Elimination of Requirements that are already "ESH Best Practices"

1. Exposure Data
2. Dependency upon Personal Protective Equipment
3. Equipment/Process Risk Assessments
4. Ergonomic Stressor Evaluation
5. Collection of Regulatory Requirements
6. Pollutant Release and Transfer Disclosure

Restructured "Design for ESH" Section

1. Interim solutions are being used for Life Cycle Assessments (LCA) and for Chemical Risk Assessments.
2. Pollutant Release and Transfer Disclosure was dropped.
3. Regulatory requirements were dropped because they are covered by existing Environmental Management Systems*Resource Conservation for Energy and WaterEnergy Conservation (Table 102)*
1. Ratio of Fab Equipment to Facilities energy use was changed from 50/50 to 40/60.

Water Conservation (Tables 102 and 105)

1. Eliminated redundancy by locating data only in Table 102.

Chemical/Materials and Equipment Management (Table 103)

1. Dropped requirements for safe dopant delivery systems (goal achieved) and expanded definition of dopant requirements.
2. Revised high-k materials of concern.

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Table 101a ESH Difficult Challenges—Near-term

Five Difficult Challenges ≥ 50 nm/Through 2009	*Summary of Issues/Needs*
Chemicals, Materials, and Equipment Management	*New Chemical Assessment* Need for quality rapid assessment methodologies to ensure that new chemicals (or those carried over from previous technologies but that now face new restrictions) can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation. *Chemical Data Collection* Need to document and make available environment, safety, and health characteristics of chemicals *Chemical Reduction* Need to develop processes that meet technology demands while reducing impact on human health, safety and the environment, both through replacement of hazardous materials with materials that are more benign, and by reducing chemical quantity requirements through more efficient and cost-effective process management *Environment Management* Need to develop effective management systems to address issues related to disposal of equipment, and hazardous and non-hazardous residue from the manufacturing process
Resource Conservation	*Natural Resource Conservation (Energy, Water)* Need to implement known (from supplier optimization studies, benchmarking surveys and best known methods) energy and water use reduction solutions Continue to design innovative energy and water efficient processing equipment *Chemicals and Materials Use* Need more efficient utilization of chemicals and materials *Resource Recycling* Increase resource reuse and recycling *Sustainable Growth* Continued expansion of semiconductor manufacturing with reduced impact on natural resources
Workplace Protection	*Equipment Safety* Continue to design ergonomically correct and safe equipment Minimize ergonomic stressors and health and safety risks during maintenance activities *Chemical Exposure Protection* Increase knowledge base on health and safety characteristics of chemicals, materials, and process byproducts in the manufacturing and maintenance processes and design out potential for chemical exposures and need for PPE
Climate Change Mitigation	*Reduce Energy Use of Process Equipment* Need to design energy efficient processing equipment *Reduce Energy Use of the Manufacturing Facility* Need to develop energy efficient facilities systems *Reduce High Global Warming Potential (GWP) Chemicals Emission* Need ongoing improvement in methods that reduce emissions from processes using GWP chemicals
Design for Environment, Safety, and Health (DFESH)	*Evaluate and Quantify ESH Impact* Need integrated way to evaluate and quantify ESH impact of process, chemicals, and process equipment, and to make ESH a design parameter in development of new equipment and processes

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Table 101b ESH Difficult Challenges—Long-term

Five Difficult Challenges <50 nm/Beyond 2009	*Summary of Issues/Needs*
Chemicals, Materials and Equipment Management	*Chemical Use Information* Need to understand regulatory requirements that set chemical restrictions Need for comprehensive material life cycle analysis of semiconductor products
Resource Conservation	*Reduce Water, Energy, Chemicals and Materials Use* Need resource efficient processing and facility support equipment driving toward resource sustainability and greener fabs
Workplace Protection	*Equipment Safety* Need more emphasis on safety of fab automation systems/robotics and sub-system isolation (e.g., lock-out, tag-out (LOTO) of components of cluster tools) for tool maintenance
Climate Change Mitigation	*Reduce Energy Use* The importance of reducing energy use to minimize/slow climate change will grow *Reduce High GWP Chemicals Emissions* The international pressures to reduce emissions of GWP chemicals will continue
Design for Environment, Safety, and Health (DFESH)	*Evaluate and Quantify ESH Impact* Need ESH integrated into the design and development of new equipment and processes

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YIELD ENHANCEMENT

The Yield Enhancement community is challenged by the following topics:

- Need for high-speed and cost-effective high aspect ratio inspection tools.
- Achieve testable and diagnosable designs for Integrated circuits.
- Data management and test structures for rapid yield learning.
- Correlation of Impurity level to yield.
- Development of parametric sensitive yield models including new materials and considering the high complexity of integration. The understandings of systematic mechanism limited yield are mandatory for achieving historic yield ramps in the future.
- Detection of ever-shrinking yield critical defects.
- Need for fast and short yield learning cycles at simultaneously increasing process complexity, to achieve historic yield ramps and mature yield levels.
- Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughput.

The priorities are according the listing above. The key changes were at:

- Defect Detection and Characterization
    - The edge exclusion was aligned between YE, FEP, Litho, and Factory Integration
    - Update and new calculation of the cost of ownership for defect inspection tools.

- Wafer Environment Contamination Control
    - Address table 114 to wafer environment as e.g. clean room or mini environment
    - Adjustment of the table values
    - Add new contamination issues within the table

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Table 107 Yield Enhancement Difficult Challenges -- WAS

Difficult Challenge ≥ 45 nm/Through 2010	*Summary of Issues*
Design for Manufacture and Test (DFM and DFT) and Systematic Mechanisms Limited Yield (SMLY)—IC designs must be optimized for a given process capability and must be testable and diagnosable. Understanding SMLY is mandatory for achieving historic yield ramps in the future.	Design to process compatibility, design for manufacturability, design for test, design for diagnosability, systematic mechanisms limited yield (SMLY) model development.
High-Aspect-Ratio Inspection—High-speed, cost-effective tools are needed to rapidly detect defects at 1/2 X ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches and especially defects near or at the bottoms of these features	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
Detection of Ever Shrinking Yield Critical Defects—High throughput, high capture rate detection tools are needed for ever shrinking critical defects of interest.	Line edge roughness, ACLV, subtle process variation. Where does process variation stop and defect start? Need to improve signal to noise to delineate defect from process variation.
Non-visual Defect Sourcing—Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected.	Many defects that cause electrical faults are not detectable inline.
Difficult Challenge <45 nm/Beyond 2010	*Summary of Issues*
Develop Yield Models that include New Materials and Integration—Models must comprehend greater parametric sensitivities, complex integration issues, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Develop test structures for new technology nodes. Address complex integration issues. Model ultra-thin film integrity issues. Improve scaling methods for front-end processes including increased transistor packing density.
Defect Detection—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughput.	Existing techniques trade-off throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size may not exist.
Correlation of Impurity Level to Yield—Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product.	Establish an employment methodology for each material type. Define a standard test for yield/parametric effect.
Yield Ramp and Mature Yields—With increasing process complexity and fewer yield learning cycles with each subsequent technology node, it would be impossible to achieve historic yield ramps and mature yield levels.	Long and complex process will make achieving historic yield ramps challenging. Also, new materials will introduce previously unseen yield problems. Need tools and methods to shorten yield learning cycles

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Table 107 Yield Enhancement Difficult Challenges -- IS

	Difficult Challenge ≥ 45 nm/Through 2010	*Summary of Issues*
IS	High-Aspect-Ratio Inspection—High-speed, cost-effective tools are needed to rapidly detect defects at 1/2 X ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches and especially defects near or at the bottoms of these features	Poor transmission of energy into bottom of via and back out to detection system Large number of contacts and vias per wafer
IS	Design for Manufacture and Test (DFM and DFT) and Systematic Mechanisms Limited Yield (SMLY)—IC designs must be optimized for a given process capability and must be testable and diagnosable. Understanding SMLY is mandatory for achieving historic yield ramps in the future.	Design to process compatibility Design for manufacturability, test, and diagnosability SMLY model development.
IS	Data Management and Test Structures for Rapid Yield Learning to enable the rapid root-cause analysis of yield-limiting conditions.	Development of automated, intelligent structures, analysis, and reduction algorithms that correlate facility, design, process, test, and work-in-process (WIP) data
IS	Detection of Ever-Shrinking Yield Critical Defects - High throughput, cost-effective, high capture rate detection tools are needed for ever-shrinking critical defects of interest. Where does process variation stop and defect start?	Non-visual Defect Sourcing - In-line and end-of-line failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected. Wafer inspection of backside, bevel, edge, nanotopography and geometry Line edge roughness, ACLV, subtle process variation. Need to improve signal to noise ratio to delineate defect from process variation.
	Difficult Challenge <45 nm/Beyond 2010	*Summary of Issues*
IS	Correlation of Impurity Level to Yield— Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and determine required control limits.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product. Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect.
IS	Develop Yield Models that include New Materials and Integration—Models must comprehend greater parametric sensitivities, complex integration issues, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Develop test structures for new technology nodes. Address complex integration issues. Model ultra-thin film integrity issues. Improve scaling methods for front-end processes including increased transistor packing density.
IS	Yield Ramp and Mature Yields—With increasing process complexity and fewer yield learning cycles with each subsequent technology node, it would be impossible to achieve historic yield ramps and mature yield levels. Also, new materials will introduce previously unseen yield problems.	Need of tools and methods for short yield learning cycles. Understanding of Systematic Mechanisms Limited Yield (SMLY) is mandatory for achieving historic yield ramps in the future.
IS	Defect Detection—Detection and simultaneous differentiation of multiple killer defect types is necessary at high capture rates and throughput.	Existing techniques trade-off throughput for sensitivity, but at predicted defect levels, both throughput and sensitivity are necessary for statistical validity. Ability to detect particles at critical size may not exist.

METROLOGY

The changes to the 2003 ITRS Technology Requirements tables come from the Metrology TWG assessments of the state of the art of metrology equipment capability. The requirement values have remained the same. One of the most important new messages is that Critical Dimension measurement technology is now believed to be extendable to ~ the 32 nm Node. CD-SEM and scatterometry are both considered capable of being improved and extended to the 32 nm node. Since in some cases, the equipment will require improvement to meet precision requirements, those areas are now listed by using the color yellow. Previously, all CD measurement requirements were listed in the red color for near term years. Some measurement requirements such as CD for Dense Lines can be met through 2009 by existing technology. Another requirement for CD measurement was added to the Requirements Table. The aspect ratio for trench structures makes CD measurement much more difficult. Values for this requirement can now be found in the table. Some of the values for gate dielectric thickness measurement were refined after inputs from the FEP TWG.

The TWG also found that the Materials Characterization community now has a critical new capability. Aberration corrected TEM is moving from the research labs to the commercialized systems. The first evidence of 3D TEM imaging is being published. Electron energy loss can locate a single atom to one column of atoms in a crystalline sample.

Table 115 Metrology Difficult Challenges

Five Difficult Challenges ≥ 45 nm/Through 2009	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, ion species /energy /dosage (current), and wafer temperature during RTA.
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of high-aspect ratio technologies such as Damascene challenges all metrology methods. Key requirements are dimensional control, void detection in copper lines, and pore size distribution and detection of killer pores in patterned low-κ dielectrics.	New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures in new, low-κ dielectrics. Sidewall roughness impacts barrier integrity and the electrical properties of lines and vias.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new, high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates. The same is true for measurement of barrier layers. High frequency dielectric constant measurements have shown a constant frequency response and are no longer a pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. There is a concern that measurements on test structures located in scribe lines do not correlate with in die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.

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Table 115 Metrology Difficult Challenges (continued)

Five Difficult Challenges < 45 nm/Beyond 2009	
Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for Damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in die properties is becoming more difficult as device shrinks.
Statistical limits of sub-45 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions.	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

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MODELING AND SIMULATION

The most important trend in the 2004 Update of the Modeling and Simulation chapter is the ever increasing need for improved integration between the various areas of simulation, like device and circuit, or interconnect and packaging. Different effects which could in the past be simulated separately will in future need to be treated simultaneously, such as thermal-mechanical, thermodynamic and electronic properties of interconnect materials. Due to the ongoing extension of the PIDS chapter to detail the requirements for high-frequency technologies, the simulation of III/V materials has been added to the short-term challenge on high-frequency device/circuit modeling. Furthermore, various new aspects and additional details were added to the items which explain the challenges and the requirements for Modeling and Simulation.

Concerning the Modeling and Simulation Technology Requirement table, four new features have been added: Full chip lithography simulation, novel memory devices, the impact of processes and materials on electrical performance, and material properties in general. The items which detail the requirements have been considerably extended, and their timing updated.

Table 121 Modeling and Simulation Difficult Challenges UPDATED

	Difficult Challenges ≥45 nm/Through 2010	*Summary of Issues*
WAS	High-frequency circuit modeling for 5–40 GHz applications	Efficient extraction and simulation of full-chip interconnect delay Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters High-frequency circuit models including non-quasi-static, substrate noise and parasitic coupling Parameter extraction assisted by numerical electrical simulation instead of RF measurements
IS	High-frequency device and circuit modeling for 5–100 GHz applications	Efficient extraction and simulation of full-chip interconnect delay Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters Extension of physical device models to III/V materials High-frequency circuit models including non-quasi-static, substrate noise, 1/f noise and parasitic coupling Parameter extraction assisted by numerical electrical simulation instead of RF measurement Scalable active and passive component models for compact circuit simulation Co-design between interconnects and packaging
WAS	Front-end process modeling for nanometer Structures	Diffusion/activation/damage models and parameters including low thermal budget processes in Si-based substrate, i.e., Si, SiGe:C (incl. strain), SOI, and ultra-thin body devices Characterization tools/methodologies for these ultra shallow geometries/junctions and low dopant levels Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
IS	Front-end process modeling for nanometer Structures	Diffusion/activation/damage models and parameters including SPE and low thermal budget processes in Si-based substrate, i.e., Si, SiGe:C, Ge (incl. strain), SOI, and ultra-thin body devices Characterization tools/methodologies for these ultra shallow geometries/junctions and low dopant levels Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces Front-end processing impact on reliability

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Table 121 Modeling and Simulation Difficult Challenges UPDATED (continued)

	Difficult Challenges ≥ 45 nm/Through 2010	*Summary of Issues*
WAS	Modeling of equipment Influences on features generated in deposition and etching processes	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry); reaction mechanisms, and reduced models for complex chemistry Linked equipment/feature scale models CMP (full wafer and chip level, pattern dependent effects) MOCVD, PECVD, and ALD modeling Multi-generation equipment/wafer models
IS	**Integrated modeling of equipment, materials, feature scale processes and influences on devices**	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry **for ULK, photoresists and high-k metal gate)**; reaction mechanisms, and reduced models for complex chemistry Linked equipment/feature scale models **(including high-k metal gate integration, damage prediction)** CMP (full wafer and chip level, pattern dependent effects) MOCVD, PECVD, ALD, **electroplating and electroless deposition** modeling Multi-generation equipment/wafer models
WAS	Lithography simulation including NGL	Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM) Predictive resist models including line-edge roughness, etch resistance and mechanical stability Multi-generation lithography system models
IS	Lithography simulation including NGL	Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM) Predictive resist models **(e.g. mesoscale models)** including line-edge roughness, etch resistance, **adhesion**, and mechanical stability **Methods to easily calibrate resist model kinetic and transport parameters** **Models that bridge requirements of OPC (speed) and process development (predictive)** **Experimental verification and simulation of ultra-high NA vector models, including polarization** **Models and experimental verification of non-optical immersion lithography effects (e.g. topography and change of refractive index distribution)** Multi-generation lithography system models **Simulation of defect influences/defect printing**
WAS	Ultimate nanoscale CMOS simulation capability	Methods and algorithms that contribute to prediction of CMOS limits Quantum based simulators Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS Phenomenological gate stack models for ultra-thin dielectrics Models for device impact of statistical fluctuations in structures and dopant distributions
IS	Ultimate nanoscale CMOS simulation capability	Methods and algorithms that contribute to prediction of CMOS limits Quantum based simulators Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS Gate stack models for ultra-thin dielectrics Models for device impact of statistical fluctuations in structures and dopant distributions **Phenomenological material models for stress engineering**

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Table 121 Modeling and Simulation Difficult Challenges UPDATED (continued)

	Difficult Challenges ≥45 nm/Through 2010	*Summary of Issues*
WAS	Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical and electronic properties of low κ, high κ, and conductors and the impact of processing on these properties Model reliability of packages and interconnects, e.g. stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion
IS	Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical, **thermodynamic** and electronic properties of low κ, high κ, and conductors and the impact of processing on these properties **especially for interfaces and films under 1 micron dimension** Model reliability of packages and interconnects, e.g. stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion. **Models for electron transport in ultra fine patterned conductors.**
	Difficult Challenges <45 nm/Beyond 2010	*Summary of Issues*
WAS	Modeling of processing and electrical properties of new materials	Computational materials science tools to understand materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions
IS	Modeling of **chemical, thermomechanical,** and electrical properties of new materials	Computational materials science tools to **describe** materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, **thermomechanical (including stress effects on mobility), optical properties**, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. **Models for air gap and novel integrations in 3D interconnects including data for ultrathin material properties.**
	Compact modeling including more physical models and statistics	Computer-efficient inclusion of influences of statistics (incl. correlations) before process freeze, quantum/ballistic transport, etc., into compact modeling
WAS	Nano-scale modeling	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes, quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects)
IS	Nano-scale modeling	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes **(incl. doping)** , quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects)
	Optoelectronics modeling	Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling Physical design tools for integrated electrical/optical systems

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For More Information

The 2004 Update is available free online to download at the website *http://public.itrs.net*.

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FOLDER 9

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Overall Roadmap Technology Characteristics

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