



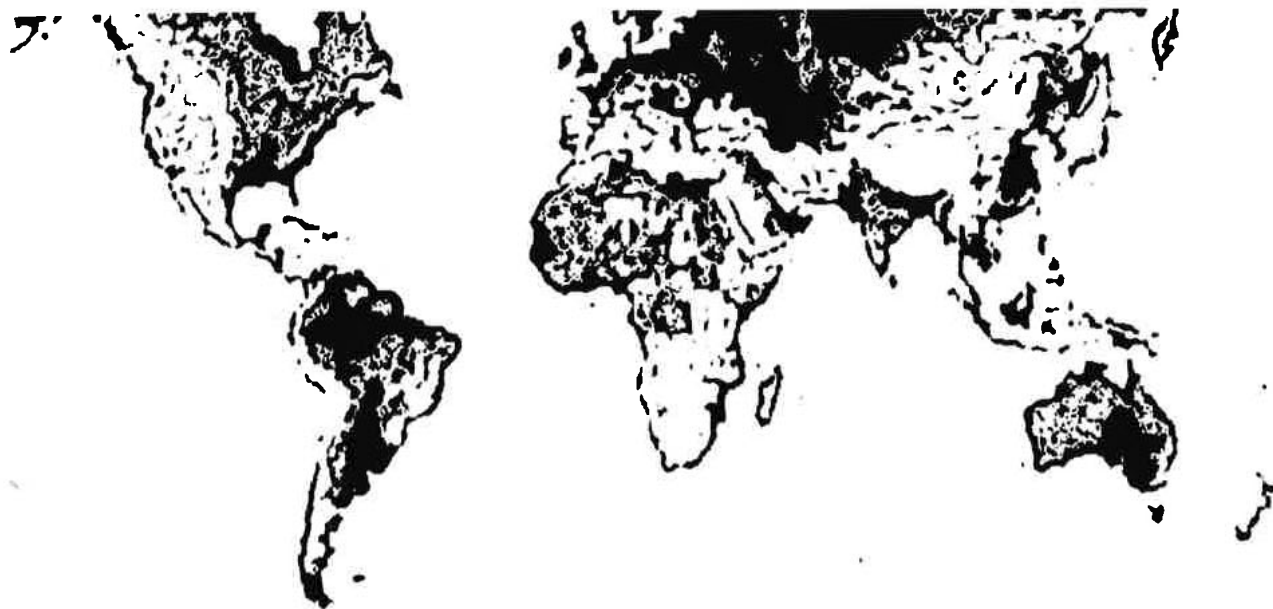
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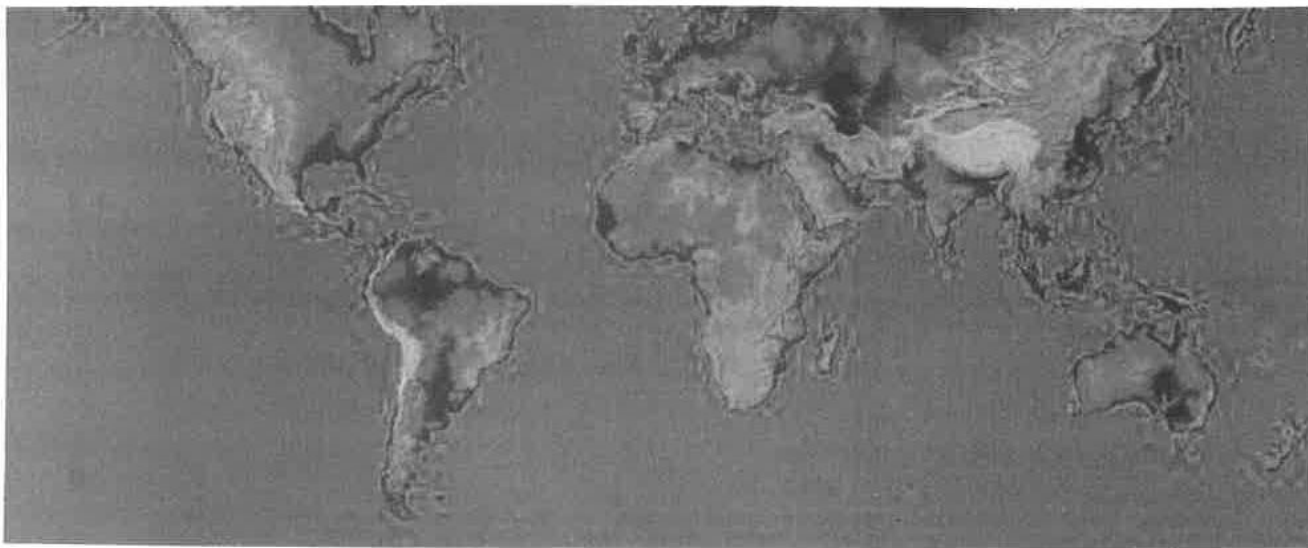
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IEEE Catalog Number	05CH37628 (softbound)
	05CH37628C (CD-ROM)
ISBN	0-7803-8881-X (softbound)
	0-7803-8882-8 (CD-ROM)
ISSN	1097-5659

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Ultra-high Performance, Low-Power, Data Parallel Radar Implementations

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ABSTRACT

Radar involves similar operations applied to large amounts of data. It is thus well suited to data parallel (SIMD) hardware. In the past, large data-parallel machines have been applied to radar with limited success. This has been due to such reasons as programming issues, cost, and the hardware being too big for most embedded applications. Most SIMD machines went away a decade ago.

There is now a new generation of SIMD COTS technology with powerful Processing Elements (PEs) and floating-point hardware. WorldScape is applying these chips to radar processing, and has demonstrated significantly more performance with much lower power dissipation (GFLOPS/Watt). These implementations provide attractive alternatives to traditional FPGA and DSP solutions. Lockheed-Martin has provided benchmark validation testing and support for these implementations.

The current implementation is based on a 64 PE, 25 GFLOP CS-301 chip supplied by ClearSpeed Technology PLC. WorldScape has demonstrated FFT, Pulse Compression, a form of QR factorization, and other applications on this generation of hardware using a mix of C-level programming and optimized assembly. The next generation chip is compatible, but also has several improvements that will significantly enhance I/O performance as well as raw GFLOP throughput.

WorldScape and Lockheed-Martin will present updated demonstrations and discuss a Scalable Processing Platform for embedded radar processing which significantly improves I/O performance and provides a roadmap to government-qualified hardware for technology insertion. Architectures, data parallel coding approaches, additional functionality of the Scalable Processing Platform, and relevance to embedded defense radar applications will be discussed.

1. ARCHITECTURE, CHIPS and BOARDS

The core of the CS301 and CSX600 chip architectures is shown in Figure 1, and some key parameters are in Table 1.

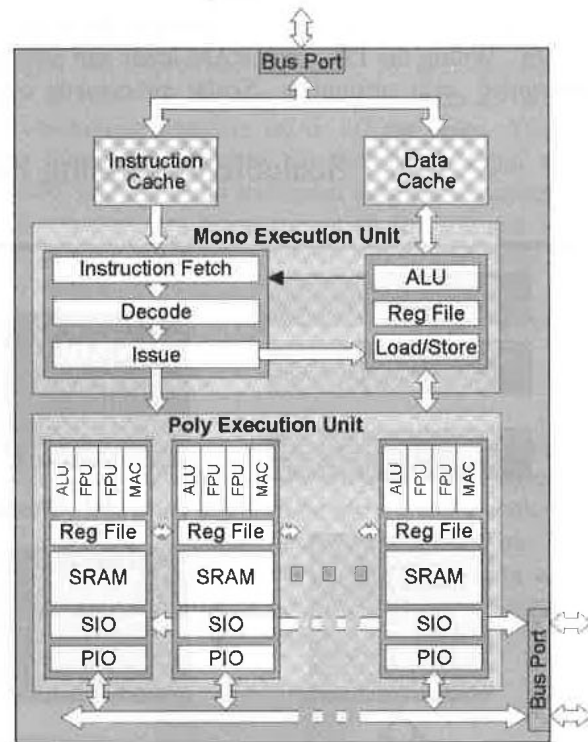


Figure 1. Chip generic core

Table 1

	CS301	CSX600
Number of PEs	64	96
RAM/PE ("poly" RAM)	4 kB	6 kB
MHz	200	250
Registers/PE	64 bytes	128 bytes
Poly RAM to registers ld/st rate	51 GB/s	64 GB/s
On-chip "mono" RAM	128 kB	128 kB
Neighbor connectivity	1D (32-bit)	1D (64-bit)
Floating Point (IEEE)	32-bit	32- and 64-bit
FP pipeline length	4	4
FP units	add & multiply	add & multiply
Peak GFLOPS	25	50
Integer MAC (bits)	8x8 to 16 out	16x16 to 32 out
Other arith unit	sqrt/divide	sqrt/divide
I/O ClearConnect ports (MB/s)	2 x 800 peak	2 x 4000 peak
I/O DDR RAM ports (MB/s)	-	3200 peak
Watts (flat-out processing)	< ~2	< ~5

The PEs have indirect addressing to their poly RAM, ie each PE can use a different address. The I/O is very flexible, with each PE able to specify a different address in external address space ("mono" RAM) for its data. PEs can be disabled for I/O an operation. Even when 16-bit integer is sufficient, it is usually possible to achieve a faster code with 32-bit floating point.

There is also a scalar processor. Broadcasting data is fast, as are global tests that reduce a Boolean array, with an element in every PE, to a scalar Boolean.

There is a lot of parallelism in addition to the SIMD data parallelism. Within the PEs, poly RAM loads and stores can be overlapped with arithmetic. Scalar processing can be

overlapped with SIMD PE processing; for example, this can lead to zero overhead looping. Multithreading enables I/O to be simultaneous with processing.

The CSX600 has some improvements (in addition to those in Table 1) that will enable the peak GFLOPS to be more nearly achieved than in the CS301. More detail on the CSX600 can be found in [1].

1.1 Scalable Processing Platform

WorldScope is developing a Scalable Processing Platform. The first board includes 2 SIMD chips and two large mono DRAMs. A diagram is shown in Figure 2.

Scalable Processing Platform Development Board

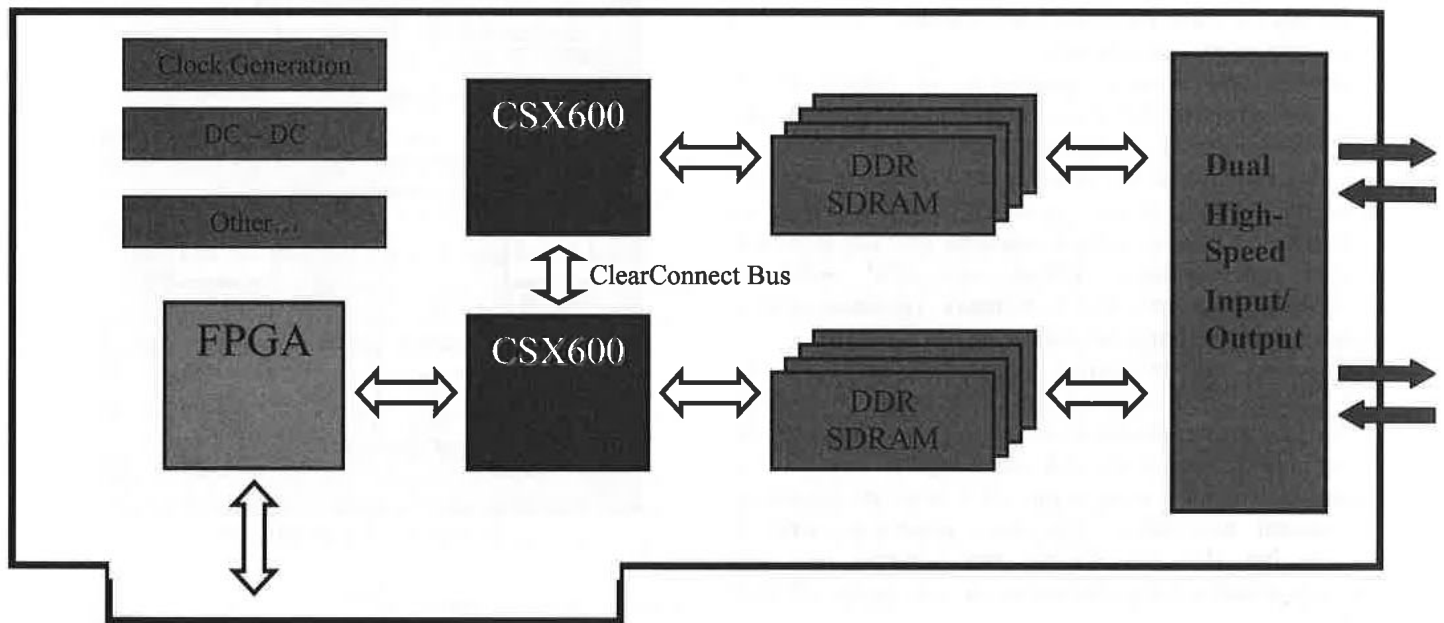


Figure 2. Scalable Processing Platform board

1.2 Programming

The high level programming language is Cn, an extension of ANSI C. The main extension is the declaration and use of poly variables, which have an instance of the variable in every PE. A mono variable can be assigned to a poly variable, which is a broadcast. Global OR or AND can be done to reduce a Boolean poly array to a mono Boolean. There are parallel data movement operations, such as transfers between mono and poly RAM, and neighbor shifting to move data between PEs.

If an IF statement is applied to a poly operation, the code does not branch but those PEs for which the condition does not apply are disabled. This can be a very powerful technique.

The instruction set is extensible, so new instructions can be microcoded. This can be powerful for getting top performance from the pipelined floating point.

Higher performance can be achieved by using assembler code, especially for floating point codes. Cn exploits neither the pipelining possibilities of the floating point units nor the ability to operate the add and multiply units simultaneously. These effects alone effectively reduce the peak GFLOPS by a factor of 8 when using Cn.

A comprehensive Software Development Kit is available, including both functionally accurate and (slower) cycle accurate simulators. Thus code can be developed without access to hardware.

2. DATA PARALLEL IMPLEMENTATIONS

A key to getting high throughput performance is to minimize data movement. Understanding and leveraging the various factors that relate to getting high performance on data parallel functions is important. Some of these factors are:

- Outer loop parallelism (OLP)

- RAM/PE limitations
- Applications latency requirements
- I/O performance
- Processing and I/O overlapping capabilities
- Multi-chip (multi-SIMD processor) architectures

The use of OLP is illustrated in the examples below.

2.1 FFTs

Rather than trying to speedup the inner loops (butterflies and short FFTs) by using the parallelism, it is often better to confine these inner loops to a single PE and get the speedup by doing many of them in parallel. For many applications such as radar, when an FFT is wanted, usually there are many similar FFTs wanted that can be done in parallel.

Using assembly code, WorldScape has implemented eight 1024-point FFTs simultaneously on a CS301 chip using 8 PEs to do each FFT. Twiddle factors are pre-stored in the poly RAM. This enabled 8 FFTs to be performed in parallel. On the CSX600 the 8 FFTs in parallel will become 12. The limit to doing more FFTs in parallel, each in fewer PEs, is the RAM/PE. Confining an FFT to few PEs avoids long distance shifts across the linear neighbor network. It does, however, increase the latency.

In the case of FFTs, microcode was written to do a radix2 butterfly using the floating point hardware in each PE. The floating point multiply and add units are each able to start a FLOP each cycle, but with a pipeline length of 4. The butterfly instruction (10 FLOPs) takes 16 cycles.

Nearly all the loads and stores between the PEs' RAM and registers can be overlapped with the butterfly instructions. With much of the scalar control code overlapped with parallel code, there is little overhead on the butterfly cycles (for within-PE work).

Shifting data within the 8 PEs takes nearly 25% of the time on the CS301.

I/O can be simultaneous with processing, and the above code includes double buffers in the PE RAM for this, as well as space for twiddle factors. If all the input and results for the FFT come from and go to the board's off-chip DRAM, the FFT is I/O limited by a factor of over 2 for a single CS301. For a single CSX600 the I/O and processing should be roughly in balance. Using both chips on a board, there is contention at the DRAM and on the ClearConnect bus. This means that performance potential is impaired, especially for the CS301 board.

On CS301, the time for 8 1024-point FFTs is ~70 usecs, or ~8.8 usecs/FFT (~5.6 GFLOPs). The CS301 dissipates 1.85 Watts when performing this code.

In the future, a wider range of instructions microcoded for FFT will enable substantially faster FFTs.

2.1.1 RAM per PE impact on performance and coding

RAM limitations will sometimes result in a greater need to move data in and out of each PE. FFTs larger than 16K points require 2 "passes" of the data through the chip, due to the CS301 having only 4KB/PE. Big 1D FFTs are similar to

2D FFTs. Thus, a 512x512 2D FFT is similar to a 256K FFT, which can be done by row and column 512-point FFTs joined by a twiddle multiply. A 64k FFT requires two passes, with 8 radix-2 stages processed on each pass. In this case the large number of twiddle factors involved means they cannot be pre-stored in poly RAM but must either be input from DRAM or computed on-the-fly. The latter is preferable, because these FFTs will be I/O limited, especially for the CS301.

An issue that has had prominence for big FFTs is the cost of "corner turning" between the two passes. This involves selecting single data points at regular but widely separated locations, and can be expensive. A feature that is being leveraged for improving efficiency of this operation is the ability of each PE to supply its own external address for packet-switching transfers on or off the chip. This enables corner turning to be done as part of an input or output operation, and not as an additional (expensive) operation. To stop the packet size being too small for efficient I/O, extra step(s) of data movement between PEs can be done before or after transfers.

Big 2D FFTs can be important for SAR processing.

2.2 Pulse Compression

Adjusting the phase of radar transmission during a long transmit pulse enables a lot of energy to be used, and, at the same time, accurate range can be recovered by convolving the echo with the transmit phase pattern. This common processing requirement is best achieved by doing an FFT, a complex multiply of the FFT by the "reference function", and an inverse FFT. This is illustrated in Figure 3.

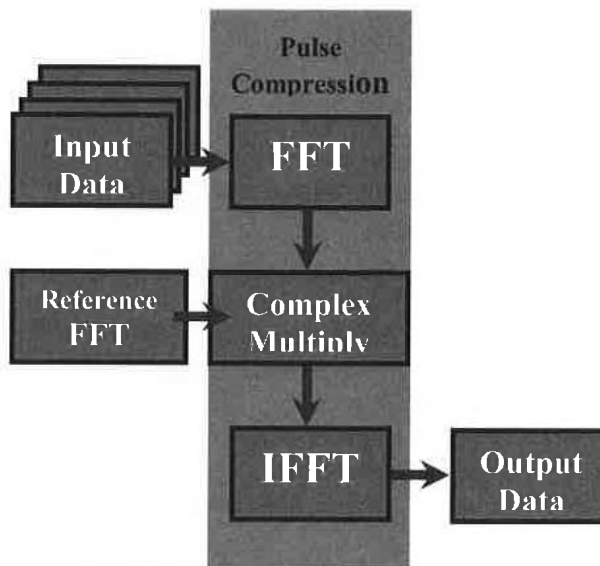


Figure 3. Pulse Compression Algorithm

The implementation approach described above for FFTs can be "mirrored" for IFFTs. For pulse compression, the FFTs are *in situ*, with the results stored in a bit-reversed order. The data format of the reference function must match the *in situ* results. If the reference function is fixed, it can remain in the PE RAM, incurring no extra I/O (I/O is only required at setup time). Thus the I/O for pulse compression is the same as

for the FFT alone, but the processing is more than doubled due to the IFFT and complex multiply. This leads to rough balance between I/O and processing in the CS301 when a single chip is used. The measured time on a single CS301 for pulse compression, including I/O, corresponds to ~3.7 GFLOPS. When both chips on the board are used, contention at the DRAM and on the ClearConnect bus means that I/O dominates and much of the potential for performance increase is not achieved.

The CSX600 will have more than double the GFLOPS per chip, and the large increase in I/O speed will mean that the use of both chips on the board will not make the chips I/O limited. About 15 GFLOPS is expected from the CSX600 board, and the two SIMD chips dissipate about 10 mWatts. Table 2 shows the performance for a Mercury PowerPC 7410 (measured by Lockheed Martin), for a CS301 (measured) and for a CSX600 (projected).

Table 2. 1024-point pulse compression

	Time (usec)	GFLOPS	Watts	GFLOPS per mW	Improvement
Mercury PowerPC 7410	152.2	0.71	8.3	0.086	
CS301	29.1	3.73	1.85	2.02	23.5x
CSX600 (estimated)	7.2	15.1	5.0	3.0	34.9x

If more than one chip is used, an issue is whether to do the FFT in one chip and the IFFT in a second chip, or to have each chip do a complete pulse compression on different pulses. OLP principles indicate the latter, and this gives higher throughput due to less data movement.

This pulse compression work was first presented in [2] and [3].

2.3 Bigger Convolutions

Some applications require quite big convolutions such as 64k. The reference function is too big to remain in poly RAM, so it must be input from DRAM as needed. An outline of the sequence is:

- Input batch of 16 sets of 256 pts
- Process 8 radix-2 stages on batch
- Output batch
- Loop over above 3 bullets (overlap I/O and processing)
- Input "2nd pass" FFT batches
- Process 8 radix-2 stages, incl twiddle compute
- Input batch of reference function
- Complex multiply (bit-reversed order)
- Process 8 radix-2 stages of IFFT
- Output batch
- Loop over above 6 bullets (with overlap)
- Input 2nd pass IFFT batches
- Process 8 radix-2 stages on batch
- Output batch (natural order)
- Loop over above 3 bullets (with overlap)

Performing the 2nd pass of the FFT and the first pass of the IFFT in the same pass means there are only 3 passes in all. Compared with the pulse compression 1024-pt convolution, the I/O per point is up about 3.5x and the processing per point is up about 1.6x. (The latter allows for more radix-2 stages, computing twiddles, complex multiply unchanged and less neighbor shifting.) CS301 will be fully I/O limited. CSX600 should be roughly balanced between I/O and processing, even when processing with 2 chips on a board.

In one case encountered, symmetry means that Sine transforms are beneficial as they halve the length of transform needed. These can be implemented in a fairly similar way to normal FFTs but require some extra processing. Some cases have real data rather than complex. Here again, efficient processing can use half-length transforms, but an extra processing stage is needed.

2.4 QR Factorization

Side lobe cancellation can involve a QR computation. There are many ways of implementing these computations. One approach is to do the bulk of the work by a matrix multiplication of a rectangular matrix by its' Hermitian transpose to generate a symmetric square matrix. Using OLP principles, it is favorable to do many such problems in parallel, with each problem confined to as few PEs as permitted by the PE RAM. The parameter that determines the number of PEs per problem is the smaller dimension, m, of the input matrix. For m up to 25, only one PE per problem is needed, there is no data movement between PEs, and about 20 GFLOPS will be achieved on a CSX600. (40 GFLOPS with 2 on a board.) For larger m, more PEs are needed and some performance is lost to data movement. There is more input than output. However, if care is taken, the input data can be 16-bit and then converted to 32-bit float in the PE, achieving full overlap of the input by processing. The final stage is a form of Cholesky decomposition which is typically a minor part of the computing total.

2.5 Air Traffic Control

Air Traffic Control (ATC) is a demanding application which is largely built on inputs from radars. Existing approaches typically are delivered late, are over budget and perform well below specification. The heart of the application is a real-time database for which multiple standard processor implementations have difficulty meeting all the requirements. An SIMD algorithmic approach is better and simpler, for which SIMD chips are much better

suited than multiple standard processors, which have problems with the synchronizations needed. The use in the ATC application of the chips described here is studied in [4], and real-time operation on much tougher specifications with much less hardware is expected.

3. OTHER APPLICATION AREAS

Outside radar there are many application areas for this type of computing, including:

- Image Processing
- Signal Processing
- Compression/De-compression
- Encryption/Decryption
- Network Processing
- Search Engine
- Supercomputing Applications

.....Matrix Inversion has been implemented in Cn with good performance. Library functions are planned with more optimised code.

4. COMPARISON WITH FPGA

FPGAs are popular for radar processing. Good performance can be achieved when configured for specific algorithms and embedded in a specific board. To do a complete job, a programmable processor usually does later stages of processing. Floating point can be done, but is relatively expensive. Sometimes different algorithms in an application can be catered for by dynamically reconfiguring the FPGA. This is quite quick, but the time is not negligible. Big fast FPGAs dissipate a lot of heat.

The flexibility of a modern SIMD chip means that more of a complete application can be done, and the performance per Watt typically far surpasses FPGAs. The programmability means it is faster to develop applications and quicker and cheaper to make algorithmic changes.

5. COMPARISON WITH DSPS

To date, DSPs have made limited use of SIMD. The new generation of chips discussed in this paper has made a coherent jump into a significant scale of SIMD, backed up by a well developed software development system. While SIMD chips might be viewed as DSPs, it is probably better

to view them as a new breed of processor that embrace the data parallelism that is so widespread in traditional image and signal processing applications.

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BIOGRAPHY

.....**Stewart Reddaway** was born in 1941, did Maths and Physics at Cambridge University and obtained a PhD at Durham University in England.

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