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A.	B. S. Haran, et al.; "22 nm technology compatible fully functional 0.1 μ m ² 6T-SRAM cell", published in 2008 IEEE International Electron Devices Meeting, date of conference December 15 -17, 2008.
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Executed on: 12/19/2022

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Gordon Macpherson
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EXHIBIT A

22 nm Technology Compatible Fully Functional 0.1 μm^2 6T-SRAM Cell

B. S. Haran[†], A. Kumar^a, L. Adam, J. Chang^a, V. Basker, S. Kanakasabapathy, D. Horak, S. Fan, J. Chen, J. Faltermeyer, S. Seo, M. Burkhardt, S. Burns, S. Halle, S. Holmes, R. Johnson, E. McLellan, T. M. Levin, Y. Zhu, J. Kuss, A. Ebert, J. Cummings, D. Canaperi, S. Paparao, J. Arnold, T. Sparks^{**}, C. S. Koay, T. Kanarsky, S. Schmitz, K. Petrillo, R. H. Kim^{*}, J. Demarest, L. F. Edge, H. Jagannathan, M. Smalley, N. Berliner, K. Cheng, D. LaTulipe, C. Koburger, S. Mehta, M. Raymond^{*}, M. Colburn, T. Spooner, V. Paruchuri, W. Haensch^a, D. McHerron, and B. Doris

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Abstract

We demonstrate 22 nm node technology compatible, fully functional 0.1 μm^2 6T-SRAM cell using high-NA immersion lithography and state-of-the-art 300 mm tooling. The cell exhibits a static noise margin (SNM) of 220 mV at $V_{dd}=0.9$ V. We also present a 0.09 μm^2 cell with SNM of 160 mV at $V_{dd}=0.9$ V demonstrating the scalability of the design with the same layout. **This is the world's smallest 6T-SRAM cell.** Key enablers include band edge high- κ metal gate stacks, transistors with 25 nm gate lengths, thin spacers, novel co-implants, advanced activation techniques, extremely thin silicide, and damascene copper contacts.

Introduction

The viability of the planar 6T-SRAM cell at 22 nm node and beyond is a subject of great debate due to extreme process challenges, high variability, and stability issues. State-of-the-art 32 nm node 0.157 μm^2 SRAM cells have 35 nm gate length, 30 nm spacer, and 40 nm contact holes (1). Significant shrink in gate length ($L_g=25$ nm), total spacer thickness ($T_{sp}<20$ nm) and contact size (~ 26 nm) is required to support a 22 nm node 6T-SRAM cell as shown in Fig. 1.

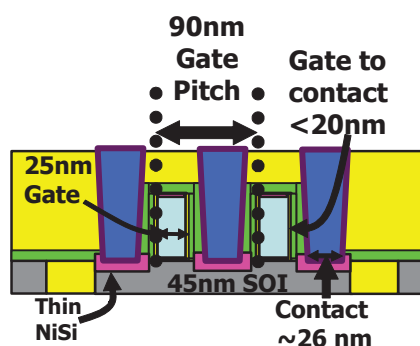


Fig. 1: Cross-section view of 6T-SRAM cell showing that aggressive gate length, spacer and contact scaling are essential at 22 nm node dimensions.

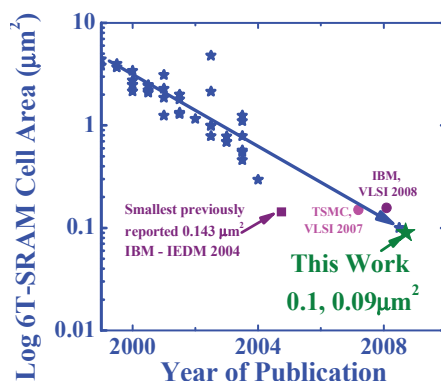


Fig 2: 6T-SRAM cell area scaling trend showing 37% reduction of cell area beyond the smallest previously reported.²

Band edge high- κ metal gate stacks, novel co-implants, and low thermal budget junction annealing techniques enabled gate length and spacer thickness scaling with adequate short channel behavior. Contact scaling has been achieved through innovative image shrink techniques in conjunction with Cu metallization. We integrate and leverage these advanced processes to demonstrate 0.1 and 0.09 μm^2 6T-SRAM cell. These are the smallest functional SRAM cells reported to date (Fig. 2) and the 0.09 μm^2 cell is 37% smaller than the previous smallest cell (2).

Device Fabrication

Ground rules for the aggressively scaled 0.1 μm^2 6T-SRAM cell are shown in Table 1. Each critical level of mask design was iteratively co-optimized for printability and functionality using predictive modeling of the on-wafer patterning contours and was printed on a high numerical aperture immersion scanner. The process flow as shown in Fig. 3 combines a thin spacer scheme, low Dt junction anneals, scaled S/D implants, and thin SOI. Fabrication began with active level printing (Fig. 4) on 45 nm thick SOI substrates using a crossed quadrupole illuminator that provided minimal corner rounding (3).

Table 1: Cell dimensions of the 0.1 μm^2 6T-SRAM cell.

Cell area	0.1	μm^2
Cell Height	0.554	mm
Cell Width	0.180	mm
Min Active Line	52	nm
Min Active Space	50	nm
Min Gate Length	25	nm
Gate Pitch	90	nm
Gate End-to-End Space	40	nm
Min Contact Size (Contact bottom)	26	nm
Min Contact Pitch	90	nm
Min Metal Line	40	nm
Min Metal Space	50	nm
Min Block Level Line	204	nm
Gate-to-Contact Spacing	19.5	nm
N+/P+ Isolation	50	nm
Gate extension beyond active	25	nm

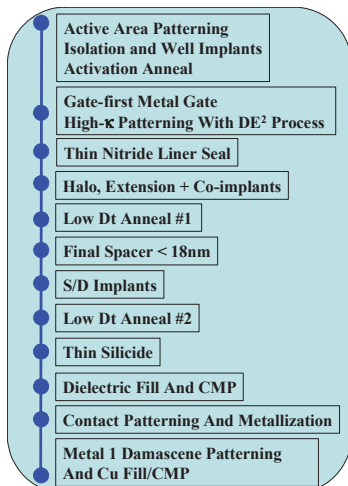


Fig. 3: Thin spacer with low Dt process flow used to fabricate the 0.1 μm^2 6T-SRAM cell.

Isolation was accomplished by using a two-step deposition process capable of filling the small trenches without voids. Band edge high- κ metal gate stacks are created through a novel integration scheme featuring the gate-first approach. The gate level was printed using a double-exposure double-etch (DE²) process (Fig. 5) with a contacted gate pitch of 90 nm (4). A thin Si_3N_4 film was used to seal the gate stack (Fig. 6). The nitride seal also serves as an offset spacer for halo, extension, and co-implants.

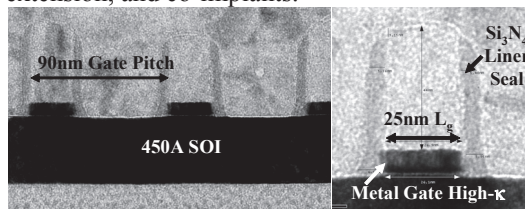


Fig. 6: Cross-section of 90 nm pitch gate stack after patterning and nitride liner seal.

Aggressive gate pitch for 22 nm node technology limits the maximum allowable thickness of the source-drain spacer. The total spacer thickness was kept < 18 nm to enable contacts to be formed between 90 nm pitch gates. An extremely thin composite oxide/nitride film was deposited and etched to form the spacer for source drain implants (Fig. 7). Nickel silicide was significantly scaled to minimize Si consumption and to prevent junction punch-through.

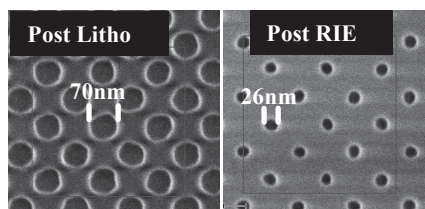


Fig. 8: Top-down SEM image of the contacts within an array after (a) immersion lithography and (b) plasma etch. Novel etches and image shrink techniques are used to reduce the contact size from 70 nm to ~26 nm.

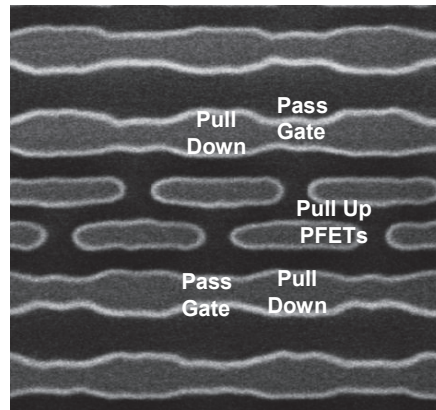


Fig. 4: Top-down SEM image of the 0.1 μm^2 6T-SRAM cell after active area patterning.

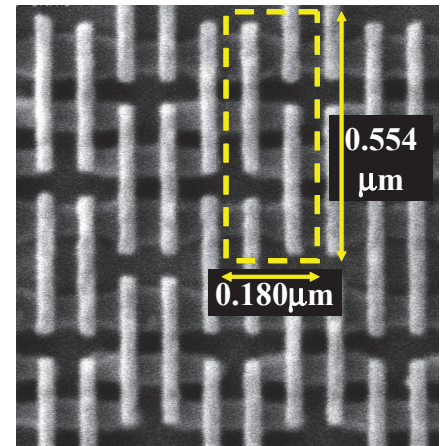


Fig. 5: Top-down SEM image of the 0.1 μm^2 6T-SRAM cell after STI fill and gate-first metal gate patterning.

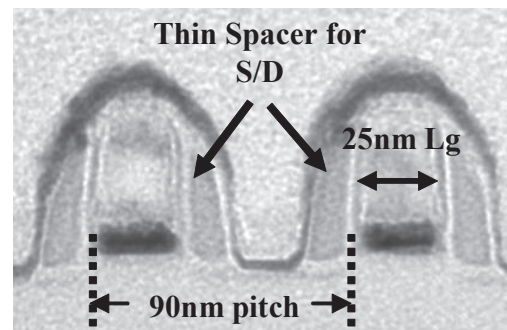


Fig. 7: Cross-sectional TEM image showing thin composite oxide-nitride spacer on 25 nm wide gate at 90 nm pitch.

The contact module was patterned using a pitch-split DE² process. The demanding CD requirements for this technology were achieved with innovative image shrink techniques. Aggressive shrink of a tri-layer organic resist followed by pattern transfer into the underlying inter-level dielectric (Fig. 8 and Fig. 9) enabled a final contact dimension of ~26 nm (5). Small CDs coupled with the high-aspect ratio place significant demands on contact metallization. Traditional W fill leads to seams/voids which increase the external resistance and degrade the device performance. A novel Cu metallization scheme enabled low resistance contacts (Fig. 10) by successfully filling the high aspect ratio contacts without voids (6). Metal levels were

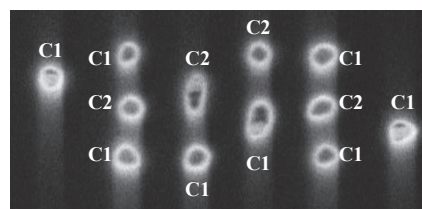


Fig. 9: Top-down SEM image of the contact patterns in the 0.1 μm^2 6T-SRAM single cell test structure post plasma etch. Pitch splitting with double expose patterning (level one - C1, level two - C2) is used to print the 12 contacts.

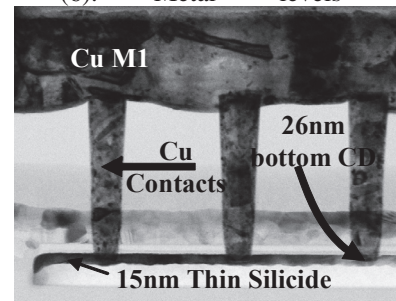


Fig. 10: Cross-sectional TEM image of high-aspect ratio Cu contacts with advanced liners.

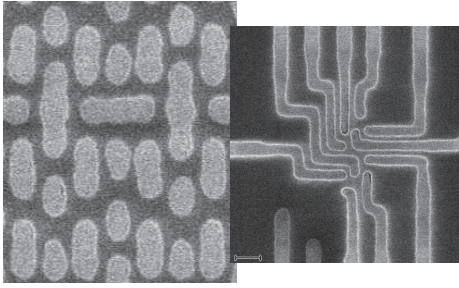


Fig. 11: Top-down SEM image after void-free first metal level fabrication of (a) $0.1 \mu\text{m}^2$ SRAM array and (b) $0.1 \mu\text{m}^2$ 6T-SRAM test structure.

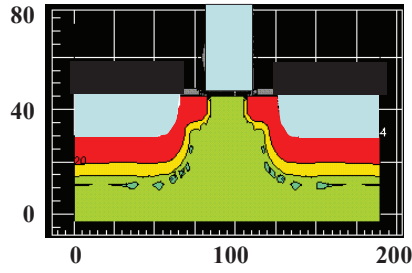


Fig. 12: Contours of net active doping in $L_g=25$ nm nFET (all dimensions are in nm).

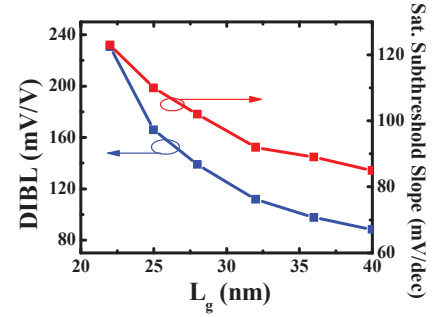


Fig. 13: Simulation of nFET DIBL and subthreshold slope (sat) as a function of L_g , showing feasibility of thin-spacer, low Dt scheme.

printed with double dipole lithography (7). Cu damascene technique was used to pattern and metallize the M1 lines (Fig. 11).

Device Results

The extremely small gate pitch at 22 nm node places significant constraints on device design methodology. In contrast to previous generations of technology, the gate pitch at 22 nm node demands that both the gate length as well as the spacer thickness be aggressively scaled. Scaling trends project that gate length for 22 nm node be 25 nm or below. An equally demanding constraint is also placed on the total spacer thickness (< 18 nm). The optimal process flow for this gate length and spacer thickness (Fig. 3) was determined by multiple iterations of device design experiments in conjunction with TCAD simulations. Preliminary results indicated the need for a low Dt approach to minimize effective diffusion of source/drain and extension implants at $L_g=25$ nm and $T_{sp} \sim 18$ nm. Band edge high- κ metal gate stacks and novel co-implants were also essential to maintain short channel control. TCAD cross-sections and simulation results demonstrating feasibility of the thin-spacer scheme with low Dt are shown in Figs. 12 and 13. In addition to the use of band edge high- κ metal gate stacks (nFET/pFET T_{inv} of 1.25/1.45 nm), further improvement in short channel behavior

was achieved with the novel co-implant design optimized for 22 nm process.

Experimental data demonstrating improvements in device characteristics from (i) low Dt thin spacer process flow, (ii) band edge high- κ metal gate stacks and (iii) novel co-implants are shown in Fig. 14. Excellent short channel characteristics (Fig. 15), with nFET/pFET DIBL of 153/194 mV/V is shown for $L_g=25$ nm. The subthreshold slope (sat) is ~ 100 mV/dec. at $L_{nom}=25$ nm. Short channel integrity at $L_g < L_{nom}$ is also very important for SRAM stability. As shown in Fig 15, good DIBL behavior down to sub nominal $L_g=20$ nm has been obtained. Appropriate sub-threshold characteristics at narrow widths are shown in the I_d-V_g curves in Fig. 16. The tight DIBL distribution of representative SRAM FETs in Fig. 17 demonstrates the robust nature of the low Dt thin spacer process flow.

Successful SRAM operation requires good SCE, low leakage, and a robust contact module. Butterfly curves for a $0.1 \mu\text{m}^2$ 6T-SRAM cell operating at various V_{dd} are shown in Fig. 18. SNM under the worst-case stability condition (word line and both bit lines at V_{dd} , during a read event or write disturb) is 150 mV at $V_{dd}=0.7$ V and reaches 230 mV at $V_{dd}=1.1$ V. Very good symmetry between half cells is also observed.

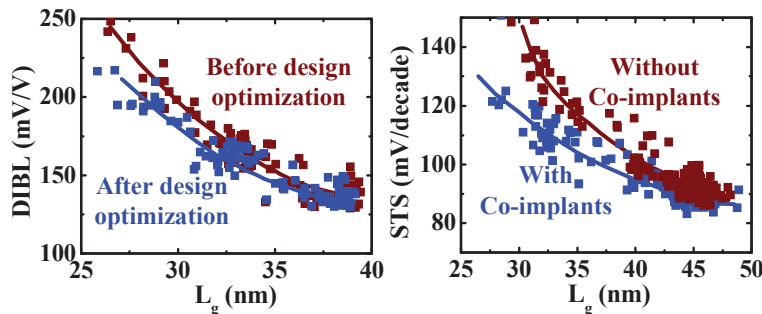


Fig. 14: Experimental results showing gate-length scaling using high-k metal gate stacks, optimized process flow and novel co-implant technology.

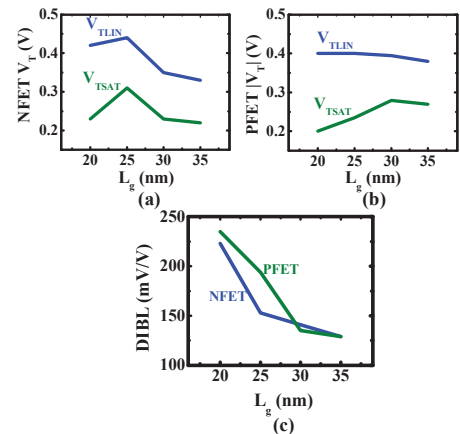


Fig. 15: Short channel characteristics of 90 nm pitch devices - V_T vs. L_g behavior for (a) nFET and (b) pFET. (c) DIBL vs. L_g

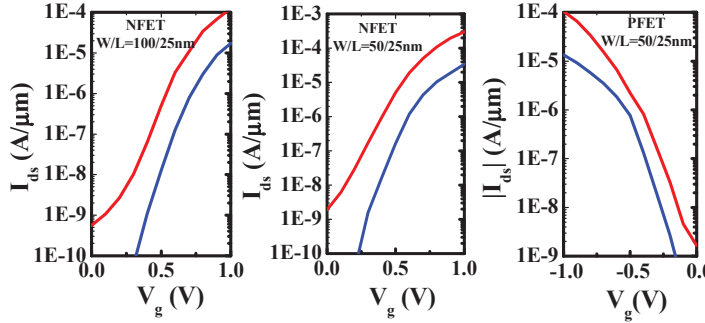


Fig. 16: I_d - V_g curves demonstrating adequate turn-off characteristics on narrow-width devices representative of the $0.1 \mu\text{m}^2$ 6T-SRAM cell.

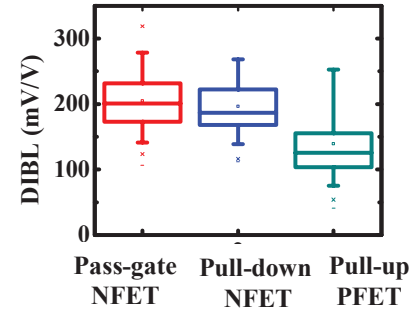


Fig. 17: DIBL distribution from SRAM devices.

As we scale to 22 nm, with the reduction of V_{dd} and increased threshold voltage variation, SRAM cell stability is a big concern. Fig. 19 shows many working cells with good SNM. We have shown enhanced SNM as compared to previous SRAM cell demonstrations (1, 2) by using high- κ metal gates, co-implants and an optimized process flow. We designed and fabricated another cell with similar layout, but with 10% reduction in cell area to demonstrate the extendibility of this approach. Butterfly curve from the $0.09 \mu\text{m}^2$ cell is shown in Fig. 20. The cell exhibits a SNM of 160 mV at $V_{dd}=0.9$ V. Although the SNM of the $0.1 \mu\text{m}^2$ cell is higher, the 10% reduction in cell area did not compromise the functionality of the $0.09 \mu\text{m}^2$ cell. This demonstrates the robust nature of both the process and the device design.

Conclusions

We developed innovative process elements for 22 nm technology on a 300 mm platform including: (i) DE² patterning with high-NA immersion lithography, (ii) dual high- κ metal gate stacks, (iii) co-implants with advanced junction anneal and (iv) novel contact shrink techniques. We integrated these elements with a low Dt process flow to **fabricate the world's smallest fully functional 6T-SRAM cell**. Ground rules and stability metrics are consistent with 22

nm node technology. This work suggests the extendibility of the 6T-SRAM cell on planar SOI.

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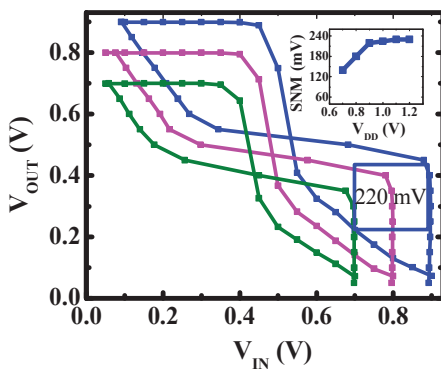


Fig. 18: Butterfly curves for $0.1 \mu\text{m}^2$ 6T-SRAM cell showing SNM of 220 mV, 180 mV and 148 mV at $V_{dd}=0.9, 0.8$ and 0.7 V respectively.

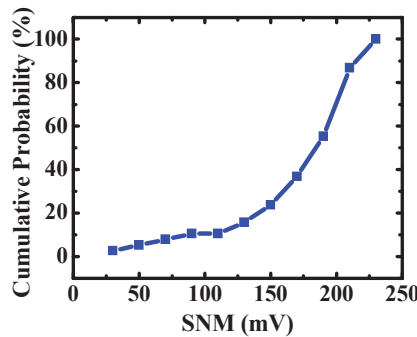


Fig. 19: Static noise margin (SNM) distribution for the $0.1 \mu\text{m}^2$ 6T-SRAM cell showing several working cells with good SNM at $V_{dd}=0.9$ V.

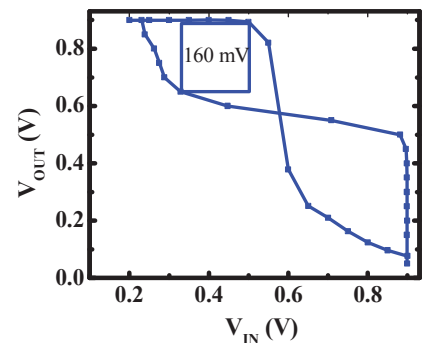


Fig. 20: Butterfly curve for $0.09 \mu\text{m}^2$ 6T-SRAM cell showing SNM of 160 mV at $V_{dd}=0.9$ V. This is the world's smallest SRAM cell.

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 Contents

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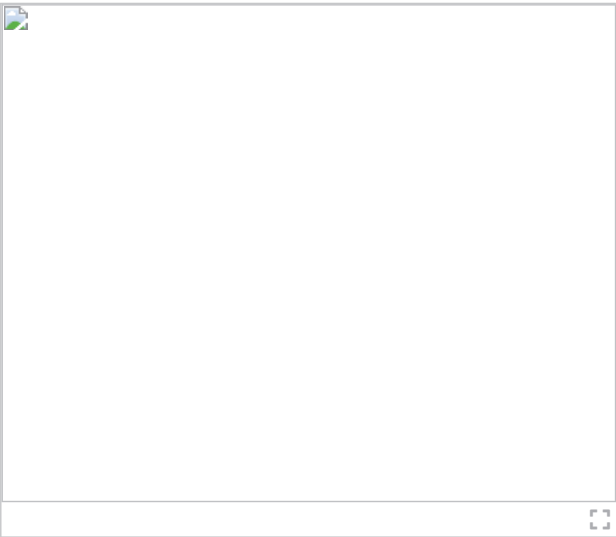


Fig. 1: Cross-section view of 6T-SRAM cell showing that aggressive gate length, spacer and contact scaling are essential at 22 nm node dimensions.

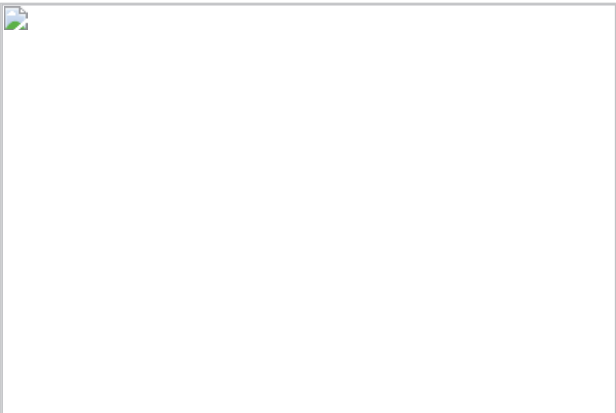




Fig 2: 6T-SRAM cell area scaling trend showing 37% reduction of cell area beyond the smallest previously reported.2

Band edge high- κ metal gate stacks, novel co-implants, and low thermal budget junction annealing techniques enabled gate length and spacer thickness scaling with adequate short channel behavior. Contact scaling has been achieved through innovative image shrink techniques in conjunction with Cu metallization. We integrate and leverage these advanced processes to demonstrate 0.1 and 0.09 μm^2 6T-SRAM cell. These are the smallest functional SRAM cells reported to date (Fig. 2) and the 0.09 μm^2 cell is 37% smaller than the previous smallest cell (2).

Device Fabrication

Ground rules for the aggressively scaled 0.1 μm^2 6T-SRAM cell are shown in Table 1. Each critical level of mask design was iteratively co-optimized for printability and functionality using predictive modeling of the on-wafer patterning contours and was printed on a high numerical aperture immersion scanner. The process flow as shown in Fig. 3 combines a thin spacer scheme, low Dt junction anneals, scaled S/D implants, and thin SOI. Fabrication began with active level printing (Fig. 4) on 45 nm thick SOI substrates using a crossed quadrapole illuminator that provided minimal corner rounding (3).

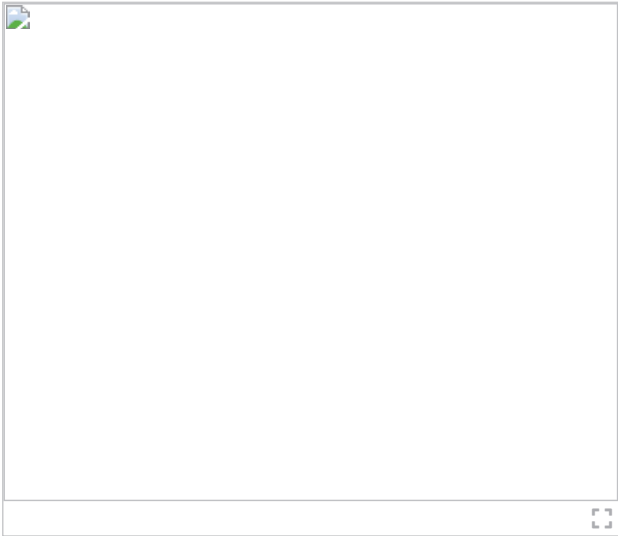
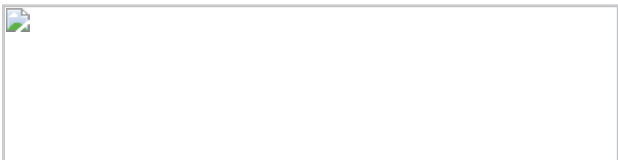


Fig. 3: Thin spacer with low Dt process flow used to fabricate the 0.1 μm^2 6T-SRAM cell.



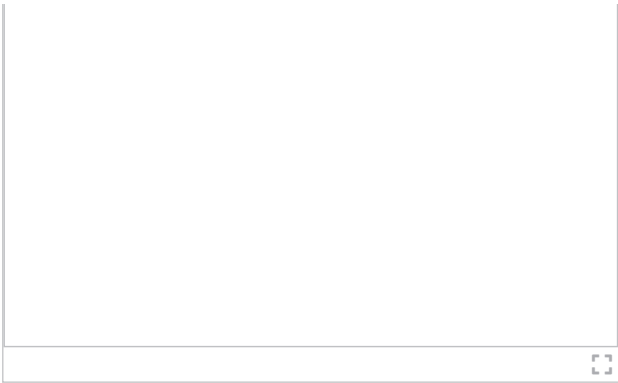


Fig. 4: Top-down SEM image of the 0.1 μm^2 6T-SRAM cell after active area patterning.

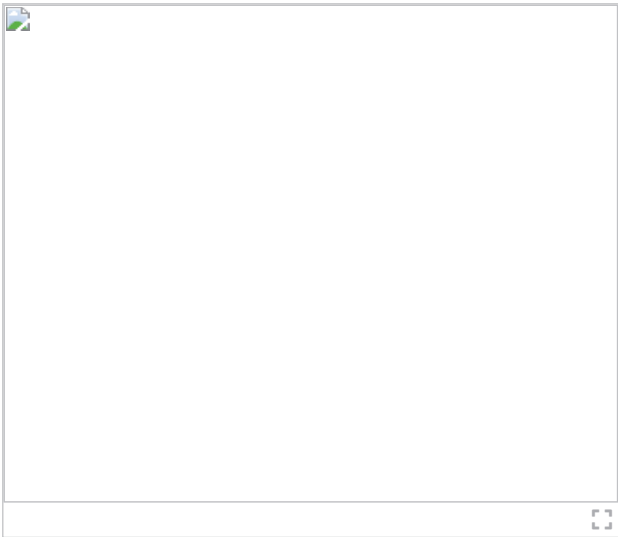


Fig. 5: Top-down SEM image of the 0.1 μm^2 6T-SRAM cell after STI fill and gate-first metal gate patterning.

Table 1: Cell dimensions of the 0.1 μm^2 6T-5RAM cell.

Cell area	0.1	μm^2	▲
Cell Height	0.554	mm	
Cell Width	0.180	mm	
Min Active Line	52	nm	
Min Active Space	50	nm	
Min Gate Length	25	nm	
Gate Pitch	90	nm	
Gate End-to-End Space	40	nm	
Min Contact Size (Contact bottom)	26	nm	
Min Contact Pitch	90	nm	
Min Metal Line	40	nm	
Min Metal Space	50	nm	
Min Block Level Line	204	nm	
Gate-to-Contact Spacing	19.5	nm	
N+/P+ Isolation	50	nm	

Cell area	0.1	μm^2
Gate extension beyond active	25	nm

Isolation was accomplished by using a two-step deposition process capable of filling the small trenches without voids. Band edge high- κ metal gate stacks are created through a novel integration scheme featuring the gate-first approach. The gate level was printed using a double-exposure double-etch (DE²) process (Fig. 5) with a contacted gate pitch of 90 nm (4). A thin Si₃N₄ film was used to seal the gate stack (Fig. 6). The nitride seal also serves as an offset spacer for halo, extension, and co-implants.

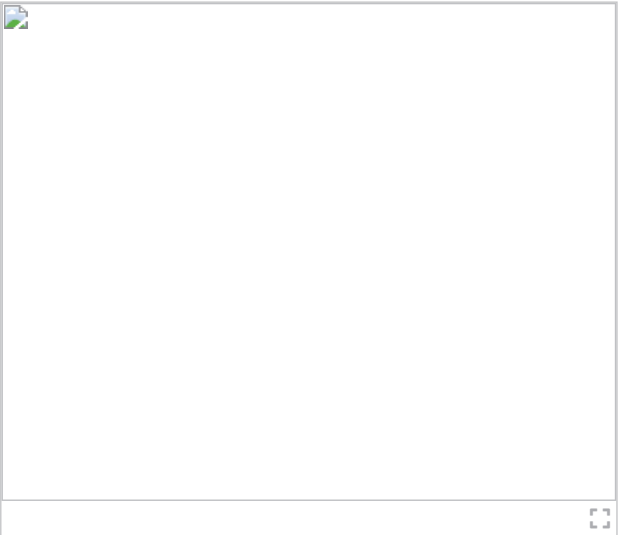


Fig. 6: Cross-section of 90 nm pitch gate stack after patterning and nitride liner seal.

Aggressive gate pitch for 22 nm node technology limits the maximum allowable thickness of the source-drain spacer. The total spacer thickness was kept < 18 nm to enable contacts to be formed between 90 nm pitch gates. An extremely thin composite oxide/nitride film was deposited and etched to form the spacer for source drain implants (Fig. 7). Nickel silicide was significantly scaled to minimize Si consumption and to prevent junction punch-through.

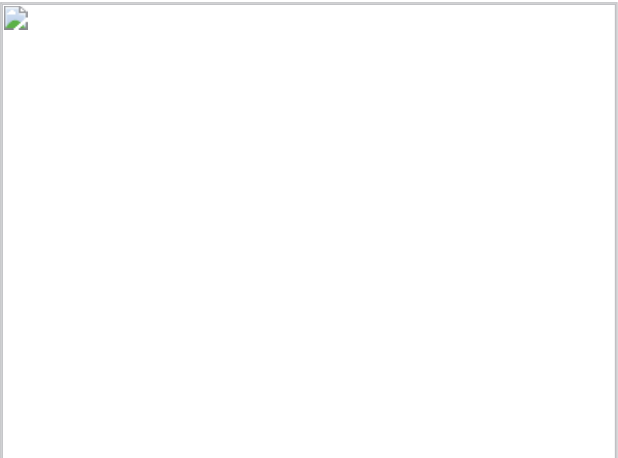




Fig. 7: Cross-sectional TEM image showing thin composite oxide-nitride spacer on 25 nm wide gate at 90 nm pitch.

The contact module was patterned using a pitch-split DE² process. The demanding CD requirements for this technology were achieved with innovative image shrink techniques. Aggressive shrink of a tri-layer organic resist followed by pattern transfer into the underlying inter-level dielectric (Fig. 8 and Fig. 9) enabled a final contact dimension of ~26 nm (5). Small CDs coupled with the high-aspect ratio place significant demands on contact metallization. Traditional W fill leads to seams/voids which increase the external resistance and degrade the device performance. A novel Cu metallization scheme enabled low resistance contacts (Fig. 10) by successfully filling the high aspect ratio contacts without voids (6). Metal levels were printed with double dipole lithography (7). Cu damascene technique was used to pattern and metallize the M 1 lines (Fig. 11).

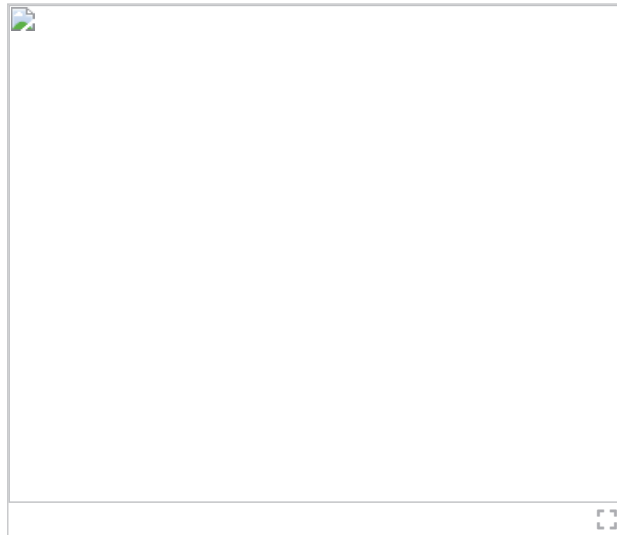


Fig. 8: Top-down SEM image of the contacts within an array after (a) immersion lithography and (b) plasma etch. Novel etches and image shrink techniques are used to reduce the contact size from 70 nm to ~26 nm.

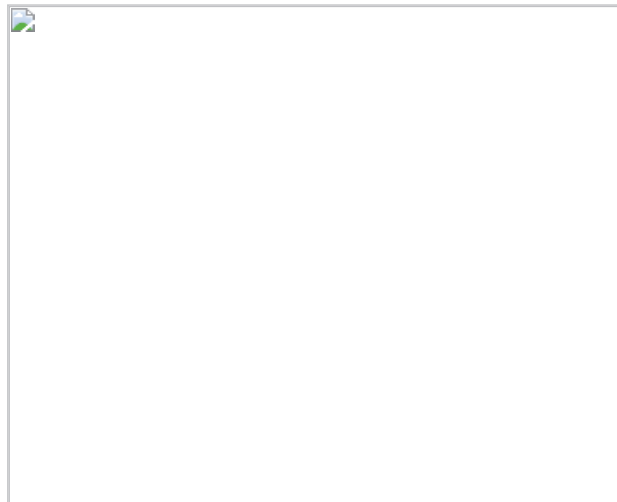




Fig. 9: Top-down SEM image of the contact patterns in the 0.1 μm^2 6T-SRAM single cell test structure post plasma etch. Pitch splitting with double expose patterning (level one - C1, level two - C2) is used to print the 12 contacts.

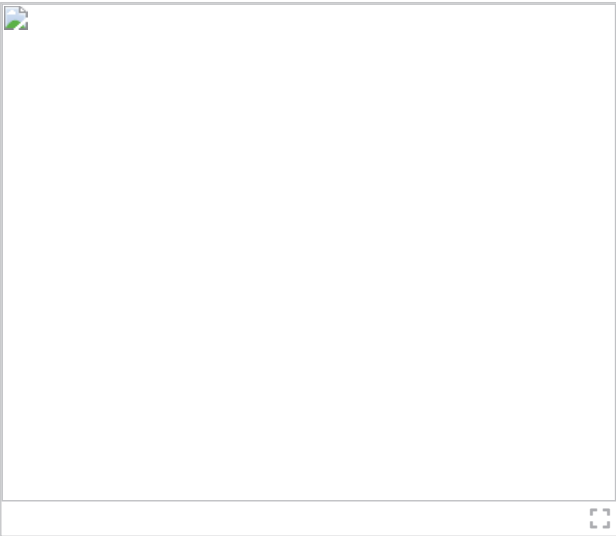


Fig. 10: Cross-sectional TEM image of high-aspect ratio Cu contacts with advanced liners.

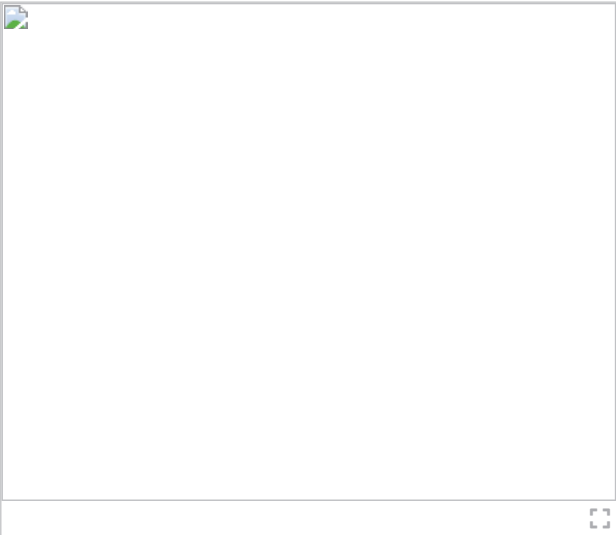


Fig. 11: Top-down SEM image after void-free first metal level fabrication of (a) 0.1 μm^2 SRAM array and (b) 0.1 μm^2 6T-SRAM test structure.

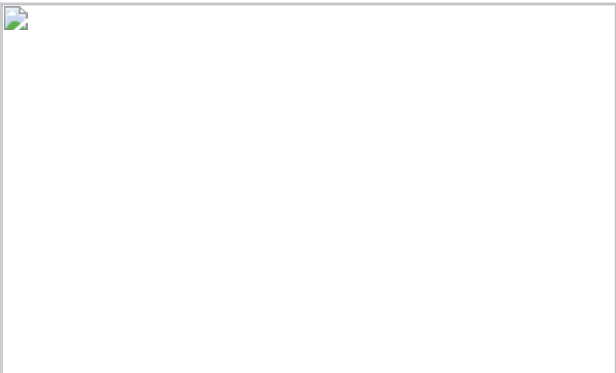




Fig. 12: Contours of net active doping in $L_g = 25$ nm nFET (all dimensions are in nm).

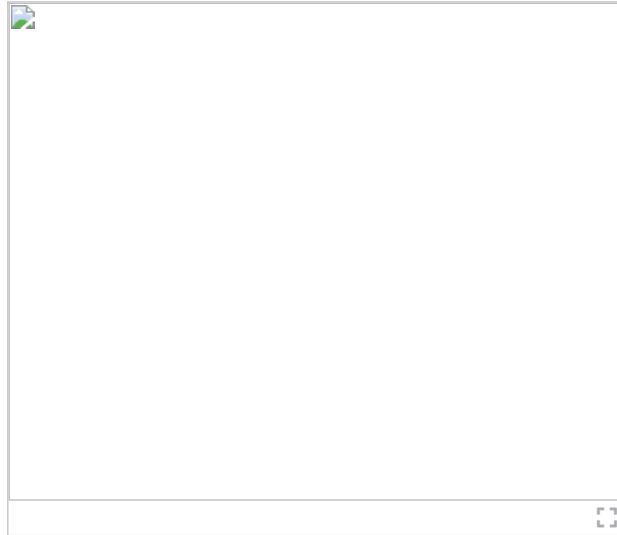
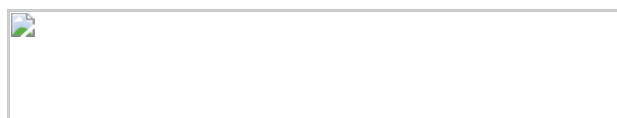


Fig. 13: Simulation of nFET DIBL and subthreshold slope (sat) as a function of L_g , showing feasibility of thin-spacer, low Dt scheme.

Device Results

The extremely small gate pitch at 22 nm node places significant constraints on device design methodology. In contrast to previous generations of technology, the gate pitch at 22 nm node demands that both the gate length as well as the spacer thickness be aggressively scaled. Scaling trends project that gate length for 22 nm node be 25 nm or below. An equally demanding constraint is also placed on the total spacer thickness (<18 nm). The optimal process flow for this gate length and spacer thickness (Fig. 3) was determined by multiple iterations of device design experiments in conjunction with TCAD simulations. Preliminary results indicated the need for a low Dt approach to minimize effective diffusion of source/drain and extension implants at $L_g = 25\text{nm}$ and $T_{sp} \sim 18\text{nm}$. Band edge high- κ' metal gate stacks and novel co-implants were also essential to maintain short channel control. TCAD cross-sections and simulation results demonstrating feasibility of the thin-spacer scheme with low Dt are shown in Figs. 12 and 13. In addition to the use of band edge high-x metal gate stacks (nFET/pFET T_{inv} of 1.25/1.45 nm), further improvement in short channel behavior was achieved with the novel co-implant design optimized for 22 nm process.



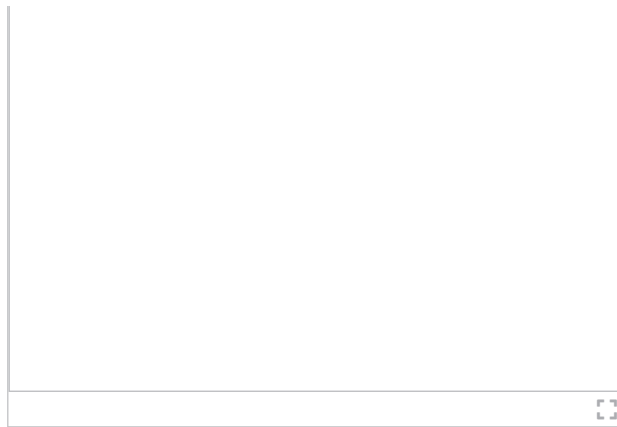


Fig. 14: Experimental results showing gate-length scaling using high-k metal gate stacks, optimized process flow and novel co-implant technology.

Experimental data demonstrating improvements in device characteristics from (i) low Dt thin spacer process flow, (ii) band edge high- κ metal gate stacks and (iii) novel co-implants are shown in Fig. 14. Excellent short channel characteristics (Fig. 15), with nFET/pFET DIBL of 153/194 m V/V is shown for $L_g = 25\text{nm}$. The subthreshold slope (sat) is ~ 100 mV/dec. at $L_{\text{nom}} = 25\text{nm}$ Short channel integrity at $L_g < L_{\text{nom}}$ is also very important for SRAM stability. As shown in Fig 15, good DIBL behavior down to sub nominal $L_g = 20$ nm has been obtained. Appropriate sub-threshold characteristics at narrow widths are shown in the $I_d - V_g$ curves in Fig. 16. The tight DIBL distribution of representative SRAM FETs in Fig. 17 demonstrates the robust nature of the low Dt thin spacer process flow.

Successful SRAM operation requires good SCE, low leakage, and a robust contact module. Butterfly curves for a $0.1\mu\text{m}^2$ 6T-SRAM cell operating at various V_{dd} are shown in Fig. 18. SNM under the worst-case stability condition (word line and both bit lines at V_{dd} , during a read event or write disturb) is 150 mV at $V_{\text{dd}} = 0.7$ V and reaches 230 mV at $V_{\text{dd}} = 1.1$ V. Very good symmetry between half cells is also observed.

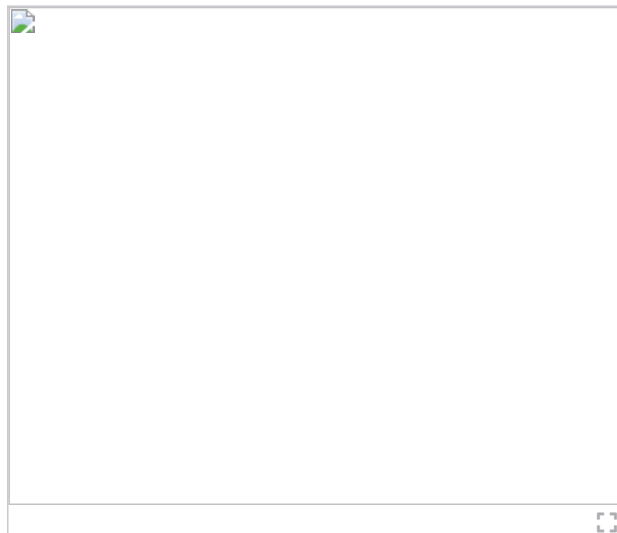


Fig. 15: Short channel characteristics of 90 nm pitch devices- V_T vs. L_g behavior for (a) nFET and (b) pFET. (c) DIBL vs. L_g

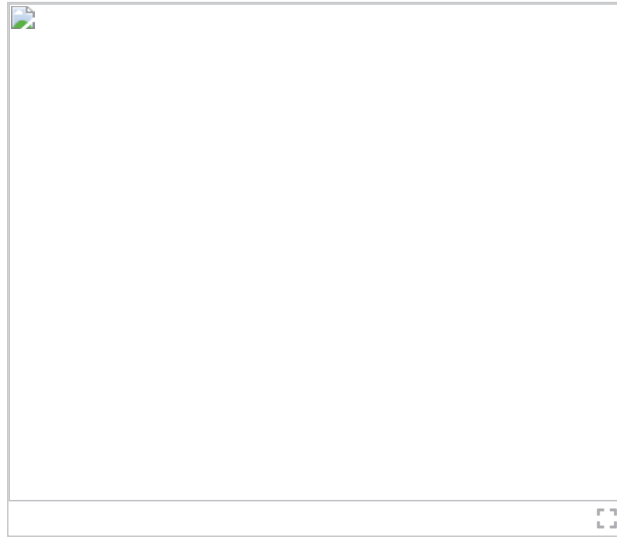
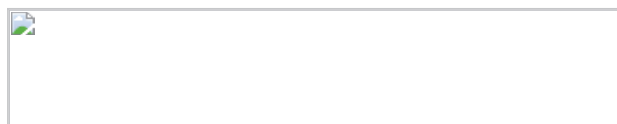


Fig. 16: Id-Vg curves demonstrating adequate turn-off characteristics on narrow-width devices representative of the 0.1 μm^2 6T-SRAM cell.

As we scale to 22 nm, with the reduction of V_{dd} and increased threshold voltage variation, SRAM cell stability is a big concern. Fig. 19 shows many working cells with good SNM. We have shown enhanced SNM as compared to previous SRAM cell demonstrations (1, 2) by using high- κ metal gates, co-implants and an optimized process flow. We designed and fabricated another cell with similar layout, but with 10% reduction in cell area to demonstrate the extendibility of this approach. Butterfly curve from the 0.09 μm^2 cell is shown in Fig. 20. The cell exhibits a SNM of 160 mV at $V_{dd} = 0.9\text{V}$. Although the SNM of the 0.1 μm^2 cell is higher, the 10% reduction in cell area did not compromise the functionality of the 0.09 μm^2 cell. This demonstrates the robust nature of both the process and the device design.

Conclusions

We developed innovative process elements for 22 nm technology on a 300 mm platform including: (i) DE² patterning with high-NA immersion lithography, (ii) dual high- κ metal gate stacks, (iii) co-implants with advanced junction anneal and (iv) novel contact shrink techniques. We integrated these elements with a low FDT process flow to fabricate the world's smallest fully functional 6T-SRAM cell. Ground rules and stability metrics are consistent with 22 nm node technology. This work suggests the extendibility of the 6T-SRAM cell on planar SOI.



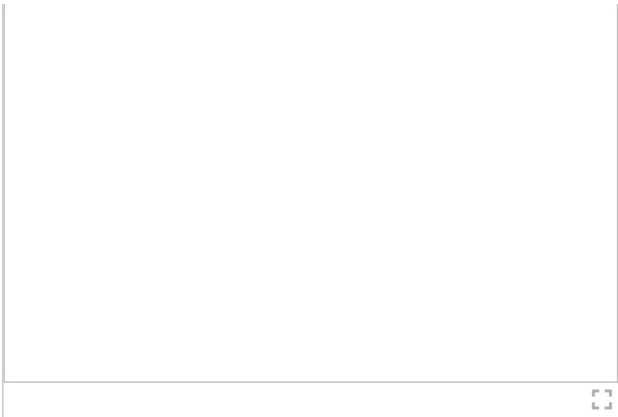


Fig. 17: DIBL distribution from SRAM devices.

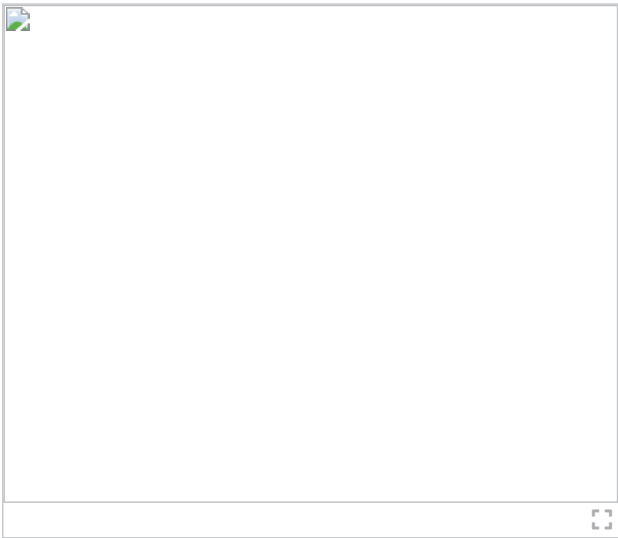


Fig. 18: Butterfly curves for 0.1 μm^2 6T-SRAM cell showing SNM of 220 mV, 180 mV and 148 mV at $V_{\text{dd}} = 0.9, 0.8$ and 0.7 V respectively.

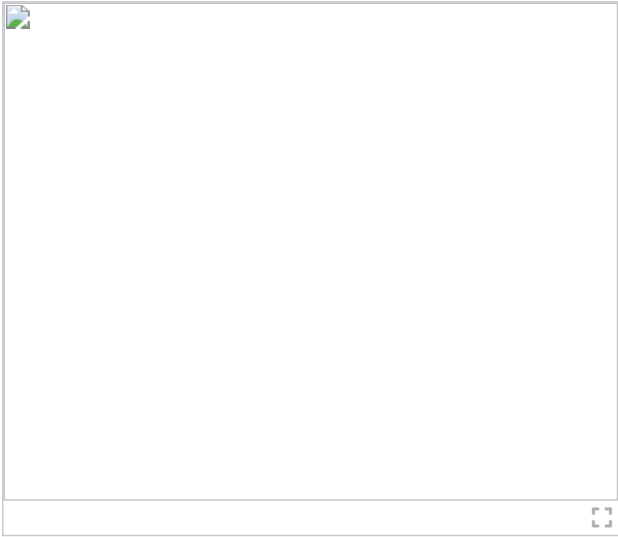
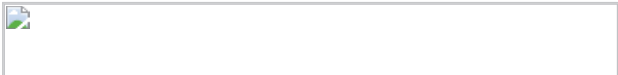


Fig. 19: Static noise margin (SNM) distribution for the 0.1 μm^2 6T-SRAM cell showing several working cells with good SNM at $V_{\text{dd}} = 0.9\text{V}$.



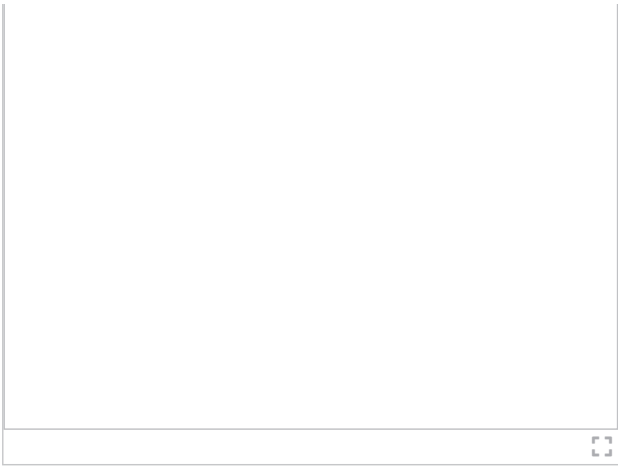


Fig. 20: Butterfly curve for 0.09 μm^2 6T-SRAM cell showing SNM of 160 mV at $V_{\text{dd}} = 0.9\text{V}$. This is the world's smallest SRAM cell.

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