

1999 IEEE

Pacific Rim Conference on Communications, Computers and Signal Processing



IEEE
Networking
the World™

Victoria, BC, Canada
August 22-24, 1999

Google Exhibit 1138
Google v. Singular

1999 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing

Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law, for private use of patrons, those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For other copying, reprint, or republication permission, write to the IEEE Copyrights Manager, Institute of Electrical and Electronics Engineers, Inc. IEEE Operations Center, 445 Hoes Lane, Piscataway, NJ 08855-1331. All rights reserved. Copyright © 1999 by The Institute of Electrical and Electronics Engineers, Inc.

IEEE Catalog Number: 99CH36368

Library of Congress: 90-655140

ISBN
0-7803-5582-2 (Softbound)
0-7803-5583-0 (Casebound)
0-7803-5584-9 (Microfiche Edition)

Additional copies of this publication are available from

IEEE Operations Center
P.O. Box 1331
445 Hoes Lane
Piscataway, NJ 08855-1331 USA

1-800-678-IEEE
1-732-981-1393
1-732-981-9667 (FAX)
833-233 (Telex)
email: customer.services@ieee.org

Kurt F. Wendt Library
University of Wisconsin - Madison
215 N. Randall Avenue
Madison, WI 53706-1688

TABLE OF CONTENTS

Session 1: ATM Networks

1.1	Congestion Control for ATM real-time Service <i>Lichen Zhang, Guangdong University of Technology, Shantou University, P.R.C.; and Peijiang Yuan, Shantou University, P.R.C.</i>	1
1.2	Scalability Issues in Multicast ATM Switching Architectures. Problems and Solutions. <i>Josemaria Malgosa-Sanahuja, Ana Jaulin-Francés, University of Zaragoza, Spain; and Joan Garcia-Haro, Polytechnic University of Catalonia, Spain</i>	5
1.3	A New Approach for ATM Network Traffic Modeling and Simulation <i>David G. Daut, Rutgers, The State University of New Jersey, USA; and Ming Yu, AT&T OTC, USA</i>	9
1.4	An Improved Fast Algorithm for Simulating Self-Similar Traffic with Application in ATM Networks <i>David G. Daut, Rutgers, The State University of New Jersey, USA; and Ming Yu, AT&T OTC, USA</i>	14

Session 2: High-Speed Communications Systems

2.1	Simultaneous Voice and Internet Data on Rural Subscriber Lines <i>David E. Dodds and Lyle Swanson, University of Saskatchewan and TRLabs, Canada</i>	18
2.2	Splitterless DSL at 230 Kb/s for Internet Access <i>David E. Dodds, University of Saskatchewan and TRLabs, Canada; Greg Erker and Jack Hanson, TRLabs, Canada; and Graham Bradley, SaskTel Research and Development, Canada</i>	22
2.3	Look-up Table based Adaptive Predistortion For Dynamic Range Enhancement in a Radio over Fiber Link <i>Xavier N. Fernando and Abu B. Sesay, TRLabs, Canada</i>	26
2.4	Performance Analysis of Indoor Infrared Wireless Systems Using OOK CDMA on Diffuse Channels <i>Ryoko Matsuo, Michihito Matsuo, Keio University, Japan; Tomoaki Ohtsuki, University of Tokyo and TAO Shin-Kawasaki Research Center, Japan; Tomoyuki Udagawa, TAO Shin-Kawasaki Research Center, Japan; and Iwao Sasase, Keio University and TAO Shin-Kawasaki Research Center, Japan</i>	30
2.5	Optical Frequency-Encoding CDMA Systems Using Time-Encoding For MAI Mitigation <i>Toshio Sonoda, Katsuhiko Kamakura, Iwao Sasase, Keio University, Japan; Tomoaki Ohtsuki, University of Tokyo, Japan; and Sinsaku Mori, Nippon Institute of Technology, Japan</i>	34

Session 3: Database and Knowledge base

3.1	A Newspaper Reading Out System with an Adaptive Information Filtering Technology to Support Visually Impaired People <i>Hideyuki Yoshida and Toshiki Kindo, Matsushita Research Institute Tokyo, Inc., Japan</i>	38
3.2	On the Implementation of a Phylogenetic Tree Database <i>Takanobu Yoshikawa, Tomohiro Tabe, Risa Kishinami, Hideo Matsuda and Akihiro Hashimoto, Osaka University, Japan</i>	42
3.3	Inductive Classification of Temporal Objects <i>Takao Miura, Hosei University, Japan; and Isamu Shioya, SANNO College, Japan</i>	46
3.4	Daily Clustering for the Electronic Newspaper Based on the Analysis of Trend <i>Takuo Nakashima and Ryoza Nakamura, Kumamoto University, Japan</i>	51
3.5	An Efficient Management Method of Moving Spatial Objects <i>Yasuaki Nakamura and Hiroyuki Dekihara, Hiroshima City University, Japan</i>	55

Session 4: Real - Time Systems

4.1	HUST_RAID: High Performance RAID in Real-Time System <i>Peng Cheng, Xinrong Zhou, Qiong Chen and Jiangling Zhang, Huazhong University of Science and Technology, P.R.C.; and Hai Jin, University of Hong Kong, P.R.C.</i>	59
-----	---	----

4.2	An Integrated Approach for Real-Time System Design <i>Lichen Zhang, Guangdong University of Technology and Shantou University, P.R.C.; and Peijiang Yuan, Shantou University, P.R.C.</i>	63
4.3	Some Real-Time Requirements in Continuous Multimedia Applications <i>Lichen Zhang, Guangdong University of Technology and Shantou University, P.R.C.; and Peijiang Yuan, Shantou University, P.R.C.</i>	67

Session 5: Wavelets and Applications (I)

5.1	Peak-Constrained Least-Squares Half-Band Filters and Orthogonal Wavelets <i>M. Liu, S. Verma, C. Zarowski and F. Fairman, Queen's University, Canada</i>	71
5.2	Blocking Artifacts Removal with a Successive Structure Analysis Using Wavelet Transform <i>Ngai-Fong Law and Wan-Chi Siu, The Hong Kong Polytechnic University, Hong Kong</i>	75
5.3	Design and Application of an Optimum Orthogonal Wavelet Filter for Echo Cancellation <i>P. Sristi, W.-S. Lu and A. Antoniou, University of Victoria, Canada</i>	79
5.4	Denoising Images Using Wavelet Transform <i>Dadang Gunawan, University of Indonesia, Indonesia</i>	83

Session 6: Image and Video Processing (I)

6.1	Real-Time Image Segmentation for Action Recognition <i>Shawn Arseneau and Jeremy R. Cooperstock, McGill University, Canada</i>	86
6.2	Efficient Color Object Segmentation Using the Dichromatic Reflection Model <i>Vladimir Kravtchenko and James J. Little, University of British Columbia, Canada</i>	90
6.3	Image Expansion Using Segmentation-Based Method <i>Abdul Karim Murad Agha, Rabab Ward and Saif Zahir, University of British Columbia, Canada</i>	95
6.4	Moving Object Velocity Estimation by Appropriately Choosing Spatial Frequencies in the Mixed Domain <i>Shengli Wu and Nozomu Hamada, Keio University, Japan</i>	99
6.5	Robust Algorithm for Scene Analysis on Compressed Video <i>Minsup Lee, Byoungchul Ahn, Yeungnam University, Korea; and Inkyu Kim, Kookmin University, Korea</i>	103

Session 7: ATM Traffic Control

7.1	Performance Analysis of a Wireless Multiple Access Scheme with Network Assisted Diversity and ARQ Control <i>Ruifeng Zhang and Michail K. Tsatsanis, Stevens Institute of Technology, USA</i>	107
7.2	An Adaptive Control Mechanism for the DQDB CO Data Service <i>L. Orozco-Barbosa and X. Tao, University of Ottawa, Canada; and A. Gupta, Nanyang Technological University, Singapore</i>	111
7.3	ABR Rate-based Control Scheme with Background VBR Traffic <i>Xiaojing Yuan, Boon Hee Soong and Liren Zhang, Nanyang Technological University, Singapore</i>	115
7.4	Efficient Time Slot Assignment Algorithms in Variable Bit Rate TDM Switch <i>Tadao Saito, Hitoshi Aida, Udomkiat Bunworasate, Takayuki Muranaka and Terumasa Aoki, University of Tokyo, Japan</i>	119

Session 8: Interference Cancellation

8.1	Analysis of Cochannel Interference in Angle Modulation Systems <i>Jocelyn Chow and Norman C. Beaulieu, Queen's University, Canada</i>	123
8.2	Adaptive Suppression of Skywave Interference in HF Surface Wave Radar Using Auxiliary Horizontal Dipole Antennas <i>Hank W. H. Leong, Defence Research Establishment Ottawa, Canada</i>	128

8.3	Serial Interference Cancellation for Highly Correlated Users <i>P.S. Guinand, R. W. Kerr and M. Moher, Communications Research Centre, Canada</i>	133
8.4	Simulated Optimum Filtering in Digital Wireless Personal Communications <i>Sandor N. Demosthenes, Hughes Space and Communications, USA; and Tai-Wu Kao, Loyola Marymount University, USA</i>	137

Session 9: Parallel Processing

9.1	Computation/Communication Balance-Point Modeling in Multiprocessors <i>V. Carl Hamacher, Queen's University, Canada</i>	141
9.2	Task Scheduling Algorithms Based on Heuristic Search Taking Account of Communication Overhead <i>Munenori Kai and Masanori Shimada, Seikei University, Japan</i>	145
9.3	Design of a Superscalar Processor Based on Queue Machine Computation Model <i>Shusuke Okamoto, Ibaraki University, Japan; Hitoshi Suzuki, Atsui Maeda, and Masahiro Sowa, The University of Electro-Communications, Japan</i>	151
9.4	Fault Tolerance Analysis of Odd-Even Transposition Sorting Networks <i>Salam N. Salloum and Andrew L. Perrie, University of Wisconsin Oshkosh, USA</i>	155
9.5	An Effective Cache Coherence Scheme Using Data Locality <i>Dongkwang Lee and Byoungchul Ahn, Yeungnam University, Korea; Hyekseong Kweon, Kukho Bae and Kiyong Yoon, LG Electronics Inc., Korea</i>	158

Session 10: VLSI

10.1	On Disjoint Covers and ROBDD Size <i>E. V. Dubrova, Royal Institute of Technology, Sweden; and D. M. Miller, University of Victoria, Canada</i>	162
10.2	Application of New Chinese Remainder Theorems to RNS with Two Pairs of Conjugate Moduli <i>Alex Skavantzios, Louisiana State University, USA; and Yuke Wang, Florida Atlantic University, USA</i>	165
10.3	Time-Domain Analysis of Nonuniform Coupled Planar Lines in VLSI Circuits <i>A. Cheldavi, Iran University of Science and Technology, Iran; S. Safavi Naeini, University of Waterloo, Canada; and M. Kamarei, University of Tehran, Iran</i>	169
10.4	Crosstalk in Ultra-High-Speed VLSI Interconnects due to Substrate-Conductivity, Temperature, and Line-Length Effects <i>Settapong Malisuwan, Florida Atlantic University, USA</i>	173

Session 11: Wavelets and Applications (II)

11.1	Low-Complexity Reversible Integer-to-Integer Wavelet Transforms for Image Coding <i>Michael D. Adams, and Faouzi Kossentini, University of British Columbia, Canada</i>	177
11.2	Suppression of Ringing Artifacts with an Adaptive Shrinkage Algorithm <i>Ngai-Fong Law, Wan-Chi Siu and Degan Feng, Hong Kong Polytechnic University, Hong Kong</i>	181
11.3	Interpolation Techniques for a LIDAR Profiler System <i>D. Sasmal, W.-S. Lu, D. Shpak and A. Antoniou, University of Victoria, Canada</i>	185
11.4	Experimental Study of a Parallel Wavelets Compression System for Medical Applications <i>Encarnacion Moyano, Pascual Gonzalez, and Francisco Quiles, Universidad de Castilla La Mancha, Spain; L. Orozco-Barbosa, University of Ottawa, Canada</i>	189
11.5	A Systolic Array Architecture for 2-D Inverse Wavelet Transform <i>J. Singh, A. Antoniou and D. J. Shpak, University of Victoria, Canada</i>	193

Session 12: Image and Video Processing (II)

12.1	A Novel Intelligent System for Defining Similar Symbols <i>Maher Ahmed and Rabab K. Ward, University of British Columbia, Canada</i>	197
------	--	-----

12.2	High Quality Image Restoration by Adaptively Transformed Sampling Function <i>Masakazu Ohira, Koichi Mori, Koichi Wada and Kazuo Toraichi, University of Tsukuba, Japan</i>	201
12.3	Analysis of Telomere Intensities in Human Chromosomes with Application to Classification of Chromosome 16 Homologs <i>Parvin Mousavi and Rabab K. Ward, University of British Columbia, Canada; Elizabeth Chavez, British Columbia Cancer Research Center, Canada; and Peter M. Lansdorp, University of British Columbia and British Columbia Cancer Research Center, Canada</i>	205
12.4	Feature Extraction Algorithm for Beef Marbling <i>Fumito Yoshikawa, Kazuo Toraichi, Koichi Wada, Kazuki Katagishi and Kwan Paul Wing Hing, University of Tsukuba, Japan; Nobuyuki Otsu, University of Tsukuba and ETL, Japan; Hiroyasu Nakai, Tohoku National Agricultural Experiment Station, Japan; and Mitsuru Mitsumoto, National Institute of Animal Industry, Japan</i>	209

Session 13: Cellular Communications Systems

13.1	Performance Analysis of Reuse Partitioning in Cellular Systems <i>Peter H. J. Chong and Cyril Leung, University of British Columbia, Canada</i>	213
13.2	Generalized Paging Schemes for Cellular Communication Systems <i>Tae K. Kim and Cyril Leung, University of British Columbia, Canada</i>	217
13.3	A Secure Communication Architecture for GSM Networks <i>Chi-Chun Lo and Yu-Jen Chen, National Chiao-Tung University, R.O.C.</i>	221
13.4	Network Efficiency for Wireless Internet Access <i>Xiaoyuan Luo, Yuming Jiang and Shengming Jiang, National University of Singapore, Singapore</i>	225
13.5	CCS Network Expansion Technique in the PCS Network <i>Jong-Shik Kim, Min-Jeong Kim, Korea Telcom Freetel, Korea; and Young-Han Kim, Soongsil University, Korea</i>	230
13.6	Forwarding Data Packets in an Integrated Voice and Data Packet Radio Network <i>Ronald D. Bowman and Harlan B. Russell, Techno-Sciences, Inc., USA</i>	234

Session 14: System Design and Implementation

14.1	CDMA Circuit-Switched Data Capacity Analysis <i>Terrence Kwong, Richard S.C. Wong and Parm Sandhu, Telus Mobility, Canada</i>	238
14.2	Multi-channel Multi-point Distribution Service System Transceiver Implementation <i>Anh Dinh, University of Regina and TRILabs, Canada; R. J. Bolton, University of Saskatchewan and TRILabs, Canada; Ralph Mason, Carleton University, Canada; and Ron Palmer, University of Regina, Canada</i>	242
14.3	A Study on Noisy HFC Network Upstream Channel Failure Prediction and Implementation <i>Liang C. Chu, Georgia Institute of Technology, USA</i>	246
14.4	Evaluating Power-Performance Trade-Offs of VLSI Transceiver Architecture for Low-Energy Communication System Design <i>Sangjin Hong and Wayne E. Stark, University of Michigan, USA</i>	250

Session 15: Internet Application Support

15.1	Performance Evaluation of Two Step Locking Protocol for Location Databases in Mobile Environment <i>Budiarto, Kaname Harumoto, Masahiko Tsukamoto and Shojiro Nishio, Osaka University, Japan</i>	254
15.2	A New Method for Maintaining Semi-Structured Data Described in XML <i>Takeya Kasukawa, Hideo Matsuda, Michio Nakanishi and Akihiro Hashimoto, Osaka University, Japan</i>	258
15.3	A Public Key Cryptography-Based Security Enhanced Mail Gateway with the Mailing List Function <i>Kazuki Katagishi, Yoshihiko Ebihara, Kazuo Toraichi and Tetsuo Sugiyama, University of Tsukuba, Japan; and Tohru Asami, KDD R&D Labs., Japan</i>	262
15.4	Cooperative Matchmaking of Requests Among Distributed Change Monitoring Service Agents <i>Santi Saeyor and Mitsuru Ishizuka, University of Tokyo, Japan</i>	266
15.5	Navigational Integration of Autonomous Web Information Sources by Mobile Users <i>Wisut Sae-Tung, Tadashi Ohmori and Mamoru Hoshi, The University of Electro-Communications, Japan</i>	270

Session 16: Image and Video Processing (III)

16.1	Error Concealment Techniques for H.263 Video Transmission <i>David Kwon and Peter Driessen, University of Victoria, Canada</i>	276
16.2	Study of Video Quality Metrics for MPEG2-Based Video Communications <i>Pedro Cuenca, Antonio Garrido and Francisco Quiles, Universidad de Castilla La Mancha, Spain; and Luis Orozco-Barbosa, University of Ottawa, Canada</i>	280
16.3	Scaleable Delivery Mechanism for VBR MPEG-2 Video Streams over the Internet <i>Naresh K. Agarwal and Anil K. Gupta, Nanyang Technological University, Singapore; Wang Bin, JVC Asia Pte. Ltd., Singapore; and Luis Orozco-Barbosa, University of Ottawa, Canada</i>	284
16.4	Reconstruction of Missing Blocks in JPEG Picture Transmission <i>M. Ancis and D. D. Giusto, University of Cagliari, Italy</i>	288

Session 17: VLSI CAD and FPGA

17.1	Embedded Memory in FPGAs: Recent Research Results <i>Steven J. E. Wilton, University of British Columbia, Canada</i>	292
17.2	VHDL Signal Analysis in VALET <i>Claudio Costi and D. Michael Miller, University of Victoria, Canada</i>	297
17.3	Tradeoff Analysis of Integer Multiplier Circuits Implemented in FPGAs <i>M. A. Thornton, Mississippi State University, USA; J. D. Gaiche, Axiom Corporation, USA; and J.V. Lemieux, University of Arkansas, USA</i>	301
17.4	Probabilistic IP Verification <i>Rolf Drechsler and Bernd Becker, Albert-Ludwigs-University, Germany</i>	305

Session 18: Digital Filters

18.1	Stable Recursive Digital Filter Design with a New Parametrization <i>Gang Li and Xiaokai Bai, Nanyang Technological University, Singapore</i>	309
18.2	Noise Reduction in State-Space Digital Filters Using High-Order Error Feedback <i>Takao Hinamoto and Takuya Maeda, Hiroshima University, Japan</i>	313
18.3	An Improved Architecture and Implementation of Cascaded Integrator-Comb Decimation Filters <i>Yonghong Gao, Lihong Jia and Hannu Tenhunen, Royal Institute of Technology, Sweden</i>	317
18.4	Performance Driven Coefficient Optimization for High Throughput Energy Efficient Digital Matched Filter Design <i>Sangjin Hong and Wayne E. Stark, University of Michigan, USA</i>	321
18.5	Convergence Analysis of Complex Adaptive IIR Notch Filters with Colored Noisy Signal <i>Shotaro Nishimura, Shimane University, Japan; Hai-Yun Jiang and Takao Hinamoto, Hiroshima University, Japan</i>	325

Session 19: Coding and Modulation (I)

19.1	New Frequency-Hopping Codes for Multimedia Mobile Communication Systems <i>Wing C. Kwong, Hofstra University, USA; and Guu-Chang Yang, National Chung-Hsing University, Taiwan</i>	329
19.2	On the Solution of Source Matching Problems <i>Laurence Wolfe, U.S. General Services Administration and Hood College, USA</i>	333
19.3	Turbo Code and Star 16-QAM for DS/SSMA Communications <i>Bon-Jin Ku, Ha-Young Yang, Suk-Hyon Yoon and Chang-Eon Kang, Yonsei University, Korea; and Sang-Cheol Han, Shinsegi Telecomm. Inc., Korea</i>	337
19.4	Multiple Input/Multiple Output (MIMO) Equalization for Space-Time Block Coding <i>Won-Joon Choi and John M. Cioffi, Stanford University, USA</i>	341

Session 20: Network Architecture

20.1	Cost and Performance Optimization in IP Switched -Routers <i>Henry C. B. Chan, Hussein M. Alnuweiri and Victor C. M. Leung, University of British Columbia, Canada</i>	345
20.2	Performance Evaluation of a Multicast Packet Switch Employing Dynamic Random Early Detection <i>C. M. Chu and H. M. Alnuweiri, University of British Columbia, Canada</i>	349
20.3	Quality of Service Support over Switched Ethernet <i>A. Pandey and H. M. Alnuweiri, University of British Columbia, Canada</i>	353
20.4	A Queue Growth Rate Based Flow Control Algorithm <i>Zhonghui Yao and Bernard Doray, Nortel Networks, Canada</i>	357
20.5	Flow Initiation and ReSeRvation Tree (FIRST): A New Internet Resource Reservation Protocol <i>Tony W. K. Chung and Henry C. B. Chan, The Hong Kong Polytechnic University, Hong Kong; and Victor C. M. Leung, University of British Columbia, Canada</i>	361

Session 21: Software Engineering

21.1	The Design of Holmes: a Tool for Domain Analysis and Engineering <i>G. Succi, A. Eberlein, J. Yip, K. Luc, M. Nguy and Y. Tan, University of Calgary, Canada</i>	365
21.2	An Object Oriented Approach for the Specification of User Interfaces <i>Maria Dolores Lozano, University of Castilla-La Mancha, Spain; and Isidro Ramos, Technical University of Valencia, Spain</i>	369
21.3	Reverse Engineering Tools in the Reporting and Analysis of the Year 2000 Date Problem <i>Jason Edward Dahmer and Richard Foley, Glasgow Caledonian University, U.K.</i>	373
21.4	Simple Approach to TSP by Permutation of Six Cities and Deletion of Crossover <i>Naoki Matsumoto and Satoshi Yashiki, Meiji University, Japan</i>	377
21.5	SBDD Variable Reordering Based on Probabilistic and Evolutionary Algorithms <i>M. A. Thornton, Mississippi State University, USA; J. P. Williams, NCR Corporation, USA; R. Drechsler and N. Drechsler, University of Freiburg, Germany; and D.M. Wessels, University of Arkansas, USA</i>	381

Session 22: Speech and Audio Processing

22.1	Speech Modification by Selective Fourier-Bessel Series Expansion of Speech Signals <i>Kaliappan Gopalan, Purdue University Calumet, USA</i>	388
22.2	MELP Vocoder Using Lifting Wavelet Transform <i>Naofumi Aoki, Hokkaido University, Japan; and Kunio Takaya, University of Saskatchewan and TRILabs, Canada</i>	392
22.3	Phrase Based Feature Extraction for Musical Information Retrieval <i>Takashi Yanase, University of Tokyo, Japan; Atsuhiko Takasu and Jun Adachi, National Center for Science Information Systems, Japan</i>	396
22.4	Arabic/English Automatic Spoken Language Identification <i>Maged Nofal, Esam Abdel-Reheem and Hadia El Henawy, Ain Shams University, Egypt</i>	400
22.5	Music Retrieval by Humming -- Using Similarity Retrieval over High Dimensional Feature Vector Space -- <i>Naoko Kosugi, Yuichi Nishihara, Seiichi Kon'ya, Masashi Yamamuro and Kazuhiko Kushima, NTT Laboratories, Japan</i>	404

Session 23: Coding and Modulation (II)

23.1	Complexity Reduction of the Viterbi Algorithm Using Doubly Complementary Convolutional Codes <i>David Haccoun and Mehdi Nabli, École Polytechnique de Montréal, Canada; and Mario Caron, Communications Research Center, Canada</i>	408
23.2	Ordered Statistics Decoding of Linear Block Codes on the WSSUS Multipath Channel <i>Wu-hsiang Jonas Chen, Jenq-Neng Hwang and Sumit Roy, University of Washington, USA</i>	412

23.3	Errors and Erasures Decoding of Reed-Solomon Codes for Reduced M-ary Orthogonal Signaling <i>Laurie L. Joiner, University of Alabama in Huntsville, USA; and John J. Komo, Clemson University, USA</i>	416
23.4	Randomly Interleaved Single Parity Check Product Codes <i>David Rankin and T. Aaron Gulliver, University of Canterbury, New Zealand</i>	420

Session 24: Integrated Circuit and Logic Design

24.1	High Speed I/O Circuit Design in Multiple Voltage Domains <i>Jerry Jex, Jed Griffin and David R. Johnson, Intel Corporation, USA</i>	424
24.2	Multi-Mode Single Neuron Arithmetics and Logics <i>C. N. Zhang, Ming Zhao and Meng Wang, University of Regina, Canada</i>	428
24.3	A VHDL Library for Current-Mode CMOS Multiple-Valued Logic <i>Daniel H. Y. Teng, Ron J. Bolton, Renee D. Schmitz and David E. Dodds, University of Saskatchewan, Canada; and Atul K. Jain, Texas Instruments, Inc., USA</i>	432
24.4	A Self-Restored Current-Mode CMOS Multiple-Valued Logic Design Architecture <i>Daniel H. Y. Teng and Ron J. Bolton, University of Saskatchewan, Canada</i>	436
24.5	Highly Testable Finite State Machines Based on EXOR Logic <i>Ugur Kalay, Alan Mishchenko, Douglas V. Hall and Marek A. Perkowski, Portland State University, USA; and Nagesh Venkataramaiah, Integrated Measurement Systems, USA</i>	440

Session 25: Distributed Multimedia

25.1	A WWW Server with Media Scaling Mechanism Based on Page Transmission Latency <i>Kaname Harumoto, Tadashi Nakano, Shinji Shimojo, and Shojiro Nishio, Osaka University, Japan</i>	444
25.2	Dynamic Multimedia Integration with the WWW <i>Koji Sato, Toshihiro Takada, Shigemi Aoyagi, Toshio Hirotsu and Toshiharu Sugawara, Nippon Telegraph and Telephone Corp., Japan</i>	448
25.3	End-System Architecture for Distributed Networked Multimedia Applications: Issues, Trends and Future Directions <i>A.Z.M. Ekram Hossain and Kin F. Li, University of Victoria, Canada</i>	452
25.4	New Resource Reservation Architecture with User Interactions <i>F. Sallabi and A. Karmouch, University of Ottawa, Canada</i>	456
25.5	Using Formal Approach to Specify Distributed Multimedia Systems <i>Lichen Zhang, Guangdong University of Technology and Shantou University, P.R.C.; and Peijiang Yuan, Shantou University, P.R.C.</i>	460

Session 26: VLSI Design and Implementation

26.1	Library Issues in the Implementation of Fast R2W Converters <i>Alberto Macii and Enrico Macii, Politecnico di Torino, Italy</i>	464
26.2	Efficient VLSI Implementation of Radix-8 FFT Algorithm <i>Lihong Jia, Yonghong Gao and Hannu Tenhunen, Royal Institute of Technology, Sweden</i>	468
26.3	Power Simulation Using Test Sets: An Experimental Analysis <i>Alberto Macii and Enrico Macii, Politecnico di Torino, Italy</i>	472
26.4	DSP-RAM: A Logic-Enhanced Memory Architecture for Communication Signal Processing <i>Zixiong Wang, Bruce F. Cockburn, Duncan G. Elliott and Witold A. Krzymien, University of Alberta, Canada</i>	475
26.5	Extending Spectral Synthesis of Binary Streams to Sequential Circuits <i>Alberto Macii, Enrico Macii, Massimo Poncino and Riccardo Scarsi, Politecnico di Torino, Italy</i>	479

Session 27: Intelligent Signal Processing in Communications

27.1	Block Subband Coding and Time-varying Filterbanks <i>Ying Zhang, University of Western Ontario, Canada; and Mehmet Zeytinoglu, Ryerson Polytechnic University, Canada</i>	483
27.2	Improved Lifting Scheme for Block Subband Coding <i>Ying Zhang, University of Western Ontario, Canada; and Mehmet Zeytinoglu, Ryerson Polytechnic University, Canada</i>	487
27.3	A Robust Chaotic Digital Secure Communication Scheme <i>Ke Li, Luxi Yang, and Zhenya He, Southeast University, P.R.C.; and Ju Liu, Southeast University and Shandong University, P.R.C.</i>	491
27.4	An Improved Wavelet-Packet-Division Multiple Access System <i>Joan Monera-Llorca, W.-S. Lu and Vijay K. Bhargava, University of Victoria, Canada</i>	495
27.5	Wavelet-Packet-Based Signatures for Asynchronous CDMA systems <i>Joan Monera-Llorca, W.-S. Lu and Vijay K. Bhargava, University of Victoria, Canada</i>	499
27.6	DS-CDMA Systems with Polyphase Signature Sequences in Multipath Fading Channel <i>So Ryoung Park, Ickho Song, Jooshik Lee, Korea Advanced Institute of Science and Technology, Korea; and Seong Ro Lee, Mokpo University, Korea</i>	503

Session 28: Spatial – Temporal Receiver Techniques

28.1	Predetection Macrodiversity in DS/CDMA Asynchronous Systems <i>Ángel M. Bravo, Universidad de Valladolid, Spain and Vijay K. Bhargava, University of Victoria, Canada</i>	507
28.2	MLSE for CPM Signals in a Fading Multipath Channel <i>Linda M. Zeger, Lucent Technologies, USA; and Hisashi Kobayashi, Princeton University, USA</i>	511
28.3	Capacity and Performance of Multiple-Input Multiple-Output Wireless Systems in a Cellular Context <i>S. Catreux, R. L. Kirlin and P. F. Driessen, University of Victoria, Canada</i>	516
28.4	Performance of a Multicarrier Decorrelating Multiuser Receiver for a DS/CDMA System <i>Jin Young Kim, Princeton University, USA; and Wan Choi, Hansol PCS, Korea</i>	520

Session 29: Distributed Applications

29.1	A Distributed Architecture for Collaborative Applications <i>Bogdan Ionescu, James Binder and Dan Ionescu, University of Ottawa, Canada</i>	525
29.2	Agent Enabled Scenario Language for Production of Interactive TV Program <i>Takeshi Shirai, Makoto Takano, Hideo Miyahara and Shinji Shimojo, Osaka University, Japan; Shunsuke Kodama, Nara Institute of Science and Technology, Japan; Koichi Tajima, Nippon Steel Information & Communications Systems Inc., Japan; and Keishi Kandori, Asahi Broadcasting Company, Inc., Japan</i>	530
29.3	Isochronous Services in Home Multimedia Networks <i>Rajugopal Gubbi, ShareWave, Inc., USA</i>	534
29.4	Service-PlugIn Mechanism for Distributed Application System <i>Yoshihiko Sakashita, Mitsubishi Electric Corporation, Japan; and Tadanori Mizuno, Shizuoka University, Japan</i>	540

Session 30: System/Signal Detection and Interpolation

30.1	New Design Approach for Polynomial-Based Interpolation <i>Ridha Hamila and Markku Renfors, Tampere University of Technology, Finland; and Gudni Gunnarsson, Nokia Telecommunications, Finland</i>	544
30.2	A MDL Approach for Determining the Number of Emitters Using Intra-Pulse Information <i>Yifeng Zhou and Jim P. Y. Lee, Defence Research Establishment Ottawa, Canada</i>	548

30.3	Practical Compactly Supported Sampling Functions of Degree 2 <i>Kazuki Katagishi, Kazuo Toraichi, Shinji Hattori and Kouji Nakamura, University of Tsukuba, Japan; and Seng Luan Lee, The National University of Singapore, Singapore</i>	552
30.4	A Frequency Domain Implementation of the Butler Matrix Direction Finder <i>Y. T. Chan and Q. Yuan, Royal Military College of Canada, Canada; and R. Inkol, Department of National Defence, Canada</i>	556

Session 31: Topics in Communications

31.1	An Adaptive Noise-Predictive Decision-Feedback Equalizer for the Magnetic Recording Channel <i>Michael Q. Le, Paul J. Hurst and Xiaodong Wang, University of California - Davis, USA</i>	560
31.2	A RISC Core Design for an ATM Network Interfaces <i>A. Elkateeb and M. Elbeshti, Acadia University, Canada</i>	564
31.3	Equalization for Partially Bandwidth-Occupied Multicarrier Transceivers <i>X. F. Wang, W.-S. Lu and A. Antoniou, University of Victoria, Canada</i>	568
31.4	Adaptive Equalization for Partially Bandwidth-Occupied ADSL Transceivers <i>X. F. Wang, W.-S. Lu and A. Antoniou, University of Victoria, Canada</i>	572

Session 32: Signal Acquisition Techniques

32.1	A New DS/CDMA Code Acquisition Scheme for Reducing the Effect of Residual Code Phase Offset <i>Seokho Yoon, Ickho Song and Ju Mi Lee, Korea Advanced Institute of Science and Technology, Korea; and Sun Yong Kim, Hallym University, Korea</i>	576
32.2	An Efficient Frequency Offset Estimator for Timing and Frequency Synchronization in OFDM Systems <i>Yun Hee Kim, Hye Jung Jung and Ickho Song, Korea Advanced Institute of Science and Technology, Korea; and Young Kwon Hahm, Electronics and Telecommunications Research Institute, Korea</i>	580
32.3	Impact of Power Control Error on PN Acquisition Performance for a Code-Division-Multiple-Access System <i>Jin Young Kim, Princeton University, USA</i>	584
32.4	A Multi-Channel Digital Receiver for Intrapulse Analysis and Direction-Finding <i>Jim P. Y. Lee, Defence Research Establishment Ottawa, Canada</i>	589

Session 33: Distributed Systems

33.1	Client Mobility and Fault Tolerance in a Distributed Network Data System <i>André P. Schoorl and Nikitas J. Dimopoulos, University of Victoria, Canada</i>	593
33.2	Design and Implementation of Message Passing Library for PC Cluster Maestro <i>Pusit Kulkasem, Burapha University, Thailand; Shinichi Yamagiwa, Naoki Ito, Naoki Yonezawa and Koichi Wada, University of Tsukuba, Japan</i>	597
33.3	Scheduling a Reservation Primitive for Effective Latency Hiding in DSM <i>Masayuki Hirota, Takeshi Yamazaki, Naoki Yonezawa and Koichi Wada, University of Tsukuba, Japan</i>	601
33.4	On Page Blocks in Distributed Virtual Memory Systems <i>A. Fellah and M. Abaza, United Arab Emirates University, United Arab Emirates</i>	605

Session 34: Analysis and Identification of Dynamic Systems

34.1	A Survey of Representations for Multidimensional Linear Systems: the Extra Term <i>Irwin W. Sandberg, The University of Texas at Austin, USA</i>	608
34.2	Neural Network Application in Robot Motion Planning <i>Xianyi Yang and Max Meng, University of Alberta, Canada</i>	611
34.3	Influence of Shear, Rotary Inertia to the Dynamic Characteristics of Flexible Manipulators <i>Dalong Wang, Max Meng and Yan Liu, University of Alberta, Canada</i>	615

Tradeoff Analysis of Integer Multiplier Circuits Implemented in FPGAs

M. A. Thornton

Mississippi State University

J. D. Gaiche

Axiom Corporation

J. V. Lemieux

University of Arkansas

Abstract

Integer multiplication is a necessary operation for performing many tasks relevant to multimedia and telecommunications processes. Here, we discuss the results of an investigation into the effectiveness of automated synthesis tools as related to a sample of modern Programmable Logic Devices (PLDs). Although it is generally accepted that superior results in terms of required area and circuit delay can generally be obtained through manual implementation of such circuits, the exclusive use of automated synthesis tools based upon an original specification in terms of a Hardware Description Language (HDL) is presented here. The results of several different approaches to multiplier architectures are presented.

1 Introduction

Field Programmable Gate Array (FPGA) and Complex Programmable Logic Devices (CPLDs) devices have matured to the point that they present a viable alternative for the implementation of general arithmetic and digital signal processing (DSP) circuitry [4] [2]. DSP processing tasks have traditionally been realized using microprocessors, Application Specific ICs (ASIC) or special purpose DSP processors. However, the logic density and speeds of modern FPGA/CPLDs have now reached levels where they can be competitive with special purpose DSP devices. In terms of custom solutions, the FPGA/CPLD approach offers immediate availability compared to the relatively lengthy development and turn around time for the design and fabrication of an ASIC. As a result of these benefits, many developers are investigating the feasibility of porting DSP applications into FPGA/CPLD based circuitry.

Digital signal processing algorithms are generally multiplication intensive tasks and many different multiplication circuit architectures exist [1] [5] [9]. It is therefore crucial that the particular multiplier circuit employed must make efficient use of the internal FPGA/CPLD architecture for a DSP task to yield acceptable performance. Furthermore, the multiplication architectures which are utilized in ASIC's are not necessarily optimal for a FPGA/CPLD implementation

because of their fixed internal structure. More information is needed to help determine which algorithms are best suited for FPGA/CPLD implementations and to further clarify the division of hardware and software functions in the circuitry being implemented. A survey of various multiplier circuits is presented in [1]. The motivation for this study is that dynamically reconfigurable computing solutions for DSP tasks will require automatically generated multipliers of various sizes and resource requirements. In some cases, throughput is enhanced with the use of many small but slow multipliers versus a large fast one [7].

The suitability of several multiplication algorithms for use in FPGAs is explored by describing the circuit structure using the Hardware Descriptive Language (HDL), *Verilog*, followed by simulation and synthesis runs. Each multiplier in this investigation is capable of multiplying two 16-bit integer numbers. Multiplier circuits that are investigated include a Scaling Accumulator Multiplier, a Addition Array Multiplier, a Computed Partial Product Multiplier, a Wallace Tree Multiplier, and a Partial Product Look-Up Table Multiplier. These particular architectures were chosen since they represent differing resource requirements and all can be scaled to various wordlengths.

The paper is organized as follows. First, a description of example multiplication circuits is presented. Next, the experimental results are presented and analyzed. Finally, conclusions and future efforts are addressed.

2 Multiplier Circuit Architecture

Descriptions of the integer multiplication architectures are provided in this section. As a point of reference, a purely behavioral description of a 16-bit multiplier is synthesized and results are given for the purpose of comparison to the other approaches considered here. An attempt was made to choose candidate architectures that represent diverse approaches. We have included structures that have traditionally yielded the best results in terms of ASIC implementation (addition tree and array based approaches), techniques that are known for speed but require large amounts of circuitry (combinational logic implementations such as the look-up table based approaches), and, word-serial implementations that require

smaller amounts of circuitry but multiple clock cycles.

2.1 Behavioral

The behavioral multiplier is implemented using a *Verilog* statement of the form: `prod = mplier * mcand;`. When the synthesis tools encounter this statement, they default to built in multiplier models for the target device. Thus, these results are useful for comparing against the RTL level multiplier descriptions of the other architectures. The *Verilog* code for this model is shown in Figure 1.

Figure 1: *Verilog* Description of Behavioral Multiplier

```
module behmult(mcand,mplier,prod,clk,
               reset,din_valid,dout_valid);
// I/O Declarations
input  [15:0]  mcand, mplier;
input        clk, rest, din_valid;
output [31:0]  prod;
output        dout_valid;
// Data Type Declarations;
reg  [31:0]  prod;
reg          dout_valid;

always @(posedge clk)
  if (reset == 1'b1)
    begin
      prod = 0;
      dout_valid = 1'b0;
    end
  else
    if (din_valid == 1)
      begin
        prod = mplier * mcand;
        dout_valid = 1'b1;
      end
    end
endmodule
```

2.2 Scaled Accumulator

This is a “shift and add” approach to generating the product. The advantages are a small amount of circuitry, but a number of clock cycles equal to the wordsize of the multiplier operand.

2.3 Computed Partial Product

This circuit stores the multiplicand, twice the multiplicand and three times the multiplicand in three internal registers. These are generated very efficiently through the use of a single-bit left-shift and an adder. The multiplier word is then used two bits at a time to select the appropriate multiple of the multiplicand. As each successive bit pair from the multiplier word is brought in, the final product is accumulated in a shift register. This approach is a generalization of

the scaled accumulator where a digit size of two bits versus a single bit is used. Figure 2 contains a block diagram of the computed partial product multiplier.

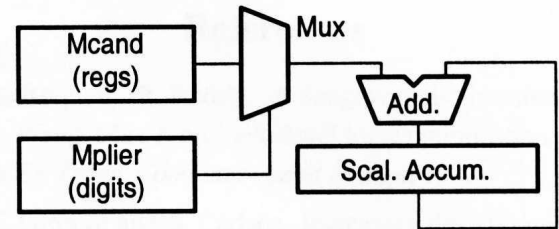


Figure 2: Block Diagram of Parallel Multiplier (array/tree type)

2.4 Addition Array

This is a array based multiplier circuit [6] using full and half single-bit adders. This approach is known for producing fast multipliers with a regular layout pattern and is popular in ASIC designs. It operates by generating all the partial products in parallel and adding them together using a rectangular array of single bit addition circuits. This is a fully parallel approach in that a product is returned at each clock cycle. Figure 3 contains a diagram of this type of multiplier.

2.5 Addition Tree

This approach accumulates the partial products through the use of a tree of 3:2 and 2:2 compressors (or single bit adders) [8] [3]. While these approaches often yield the fastest multipliers in ASIC designs, they are known for large area requirements and usually do not map well to the regular layouts inherent in FPGAs and CPLDs. In terms of operational functionality, this approach is very similar to the array multiplier described above with the difference being that a tree of adders is used to accumulate the partial products. Figure 3 also represents the addition tree multiplier.

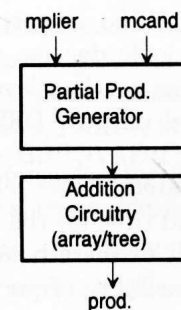


Figure 3: Block Diagram of Parallel Multiplier (array/tree type)

2.6 Memory Based Lookup Table

Here, external memory is used to store the product with the address serving as the concatenation of the multiplier and

multiplicand. To reduce the size of the required memory, four partial products are stored versus the entire 32-bit product and programmable device logic is used to scale (shift) and accumulate the final products. Due to the small amount of logic required, this approach is generally limited in speed due to the memory access times. This approach also places additional demands on FPGA/CPLD I/O requirements since pins are needed to drive the memory device address and to read in the resulting data for scaling and accumulation.

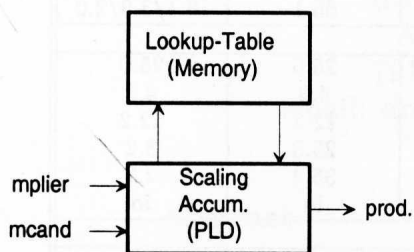


Figure 4: Block Diagram of Memory Based LUT Multiplier

3 Experimental Results

Table 1 contains results that were generated using the place and route tools from Altera MaxPlusII (ver. 9.1.2) and Xilinx Foundation Express (ver. 1.5). The Verilog descriptions were synthesized using the Synopsys FPGA Express tools bundled with MaxPlusII and Foundation, and the Synplicity Synplify tool (ver. 5.1.4). The Verilog models were tested using the PC-based Model Tech and the Unix-based Cadence Verilog-XL simulators. Estimated operating frequencies and logic resource utilization metrics are compiled based on the place and route tool log files. The place route tools were set to place approximately equal emphasis on area and delay. Since the various FPGA/CPLD manufacturers market devices with different internal architectures, each multiplier circuit is synthesized onto a variety of target devices.

In the data presented below, each multiplier type is designated using a three-letter acronym. *beh* is the behavioral multiplier, *aam* is the addition array multiplier, *atm* is the addition tree multiplier, *cpp* is the computed partial product multiplier, *sca* is the scaling accumulator approach, and, *lpp* is the look-up table based circuit. The table entries *io* and *lb* refer to inadequate device resources in terms of required I/O pins and logic blocks respectively. The columns labeled IOB, CLB, IO and LB contain the percentage of the device resources needed to implement the circuit. For those circuits that were implemented as a block of combinational logic with a register for the product, clock speed was computed as the inverse of the critical path delay plus the output register setup time. The frequencies for the *lpp* type circuits are given assuming a 10 ns SRAM, a 40 ns DRAM and a 120 ns EPROM are used for storing the partial products.

4 Conclusion

Various scalable multipliers have been synthesized and analyzed in terms of speed and area for implementation in programmable devices. It should be noted that the purpose here is not to compare the effectiveness of logic synthesis tools or programmable device architectures, but rather to get a feel for the trend in resource requirements given the various approaches. A fair comparison of the synthesis tools would require careful adherence to coding styles required by each tool and the to compare the architectures, details about internal features (such as dedicated carry-ripple logic) would need to be exploited in the HDL descriptions.

These results are useful for researchers in the area of re-configurable computing where tradeoffs between speed and logic usage must be evaluated dynamically. The results can also be of use to designers of dedicated programmable logic circuits in the preliminary phases of resource estimation and the evaluation of candidate designs with respect to functional requirements.

References

- [1] R. Andraka. *Multiplication in FPGAs*. Web Page, <http://users.ids.net/randraka/multipli.htm>, 1999.
- [2] Altera Corporation. Improving fixed-point dsp processor system performance with plds as a dsp coprocessor. *Altera Application Brief*, <http://www.altera.com/document/papers/cpdsp.pdf>, 1999.
- [3] L. Dadda. Some Schemes for Parallel Multipliers. *Alta Freq.*, 34:349–356, 1965.
- [4] S. K. Knapp. Using programmable logic to accelerate dsp functions. *Xilinx Application Brief*, <http://www.xilinx.com/appnotes/dspintro.pdf>, 1995.
- [5] I. Koren. *Computer Arithmetic Algorithms*. Prentice Hall Publishers, Englewood Cliffs, New Jersey, 1993.
- [6] S. D. Pezaris. A 40-ns 17-bit by 17-bit Array Multiplier. *IEEE Transactions on Computers*, C-20:442–447, 1971.
- [7] J. Pihl. Tradeoffs Between Parallel and Serial Architectures in High Performance Digital Signal Processing. *Proceedings of the International Symposium on Integrated Circuits*, 1997.
- [8] C. S. Wallace. A Suggestion for a Fast Multiplier. *IRE Transactions on Electronic Computers*, EC-13:14–17, 1964.
- [9] S. Waser and M. J. Flynn. *Introduction to Arithmetic for Digital Systems Designers*. Holt, Rinehart and Winston, New York, 1982.

Table 1: Results Using Various FPGA/CPLDs

Xilinx		Synopsys Express			Synplicity Synplify		
Arch.	%IOB	% CLB	CLK (MHz)	Rate (MHz)	% CLB	CLK (MHz)	Rate (MHz)
V300PQ240-4 (Virtex)							
beh	40	5	21.4	21.4	4	42.4	42.4
aam	40	12	10.0	10.0	9	9.1	9.1
atm	40	11	18.8	18.8	11	15.8	15.8
cpp	31	5	22.7	2.8	4	42.0	5.3
sca	31	1	57.7	3.6	1	69.7	4.4
lpp	50	2	36.6	14.9/3.7/2.0	1	65.1	18.1/3.9/2.0
S30VQ100-3 (Spartan)							
beh	88	43	10.6	10.6	39	25.6	25.6
aam	88	68	4.7	4.7	86	4.3	4.3
atm	88	60	7.6	7.6	65	12.2	12.2
cpp	70	25	17.2	2.2	22	25.3	3.2
sca	68	12	27.4	1.7	6	35.4	2.2
lpp	109	9	io	io	5	io	io
S05XLPC84-4 (Spartan XL)							
beh	111	250	io,lb	io,lb	214	io/lb	io/lb
aam	111	381	io,lb	io,lb	295	io/lb	io/lb
atm	111	332	io,lb	io,lb	348	io/lb	io/lb
cpp	88	144	lb	lb	116	lb	lb
sca	86	72	44.9	2.8	39	52.4	3.3
lpp	137	54	io	io	32	io	io
4028EXHQ208 ex-2 (4000EX)							
beh	42	24	10.0	10.0	22	23.1	23.1
aam	42	38	4.0	4.0	28	8.2	8.2
atm	42	33	7.9	7.9	35	12.3	12.3
cpp	33	14	22.4	2.8	12	23.2	2.9
sca	33	7	32.0	2.0	3	35.8	2.2
lpp	51	5	22.4	11.8/3.5/1.9	3	38.3	15.1/3.8/2.0
40150XVHQ240 xv-09 (4000XV)							
beh	38	4	8.9	8.9	4	33.0	33.0
aam	38	7	3.4	3.4	5	10.2	10.2
atm	38	6	6.0	6.0	7	15.5	15.5
cpp	30	2	19.2	2.4	2	38.6	4.8
sca	29	1	17.0	1.1	1	61.5	3.8
lpp	46	1	11.4	7.8/3.1/1.8	1	59.2	17.6/3.9/2.0
3020APC68-6 (3000A)							
beh	115	414	io,lb	io,lb	607	io,lb	io,lb
aam	115	525	io,lb	io,lb	576	io,lb	io,lb
atm	115	648	io,lb	io,lb	637	io,lb	io,lb
cpp	91	337	lb	lb	343	lb	lb
sca	89	185	lb	lb	92	135.1	8.4
lpp	143	98	io	io	84	io	io
Altera		Synopsys Express			Synplicity Synplify		
Arch.	%IO	% LC	CLK (MHz)	Rate (MHz)	% LC	CLK (MHz)	Rate (MHz)
EPF10K20TC144-3 (Flex 10k)							
beh	64	71	9.2	9.2	48	26.0	26.0
aam	64	67	6.1	6.1	54	6.1	6.1
atm	64	67	10.4	10.4	lb	lb	lb
cpp	50	52	12.2	1.5	28	33.9	4.2
sca	48	13	20.0	1.3	15	49.5	3.1
lpp	81	10	17.2	10.2/3.4/1.9	8	55.2	17.2/3.9/2.0
EPF81188AQC208-2 (Flex 8k)							
beh	45	81	8.7	8.7	55	23.8	23.8
aam	45	77	5.3	5.3	61	4.7	4.7
atm	45	76	9.6	9.6	80	8.3	8.3
cpp	36	59	10.7	1.3	34	21.6	2.7
sca	35	15	17.5	1.1	14	34.7	2.2
lpp	56	12	16.5	9.9/3.3/1.8	9	41.5	15.6/3.8/2.0
EPF6010ATC100-1 (Flex 6k)							
beh	95	93	12.3	12.3	62	23.0	23.0
aam	95	89	7.1	7.1	lb	lb	lb
atm	95	87	13.4	13.4	lb	lb	lb
cpp	74	68	14.1	1.8	38	33.6	4.2
sca	73	17	25.4	1.6	16	41.3	2.6
lpp	io	io	io	io	io	io	io