

International Technology Roadmap for Semiconductors 2000 Update

Overall Roadmap Technology Characteristics

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OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS & GLOSSARY

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) 2000 Update Tables have been revised from the *International Technology Roadmap for Semiconductors, 1999 edition* (ITRS) ORTC to highlight the current rapid pace of advancement in semiconductor technology. They represent a “snapshot” of the work in progress by the International Roadmap Committee (IRC) and the International Technology Working Groups (ITWGs) as they prepare for the full revision of the ITRS in 2001.

The ORTC tables are used throughout the update and renewal of the ITRS to identify rapidly changing, leading-edge trends and provide synchronization among the ITWGs. In July 2000, the IRC reached consensus on proposing “most aggressive” values for a few high-level ORTC line items that were then used to drive the complete ORTC update. These values represent the most optimistic of three scenarios (see details below) that are still under discussion in preparation for the 2001 edition of the ITRS. Thus, they represent a start toward creating new ORTC tables early in the 2001 ITRS revision/development process.

With respect to the ITWG tables, the activities for the 2000 Update are limited to review and correction as possible considering all tables from the 1999 ITRS. Some ITWG tables do not comprehend this “most aggressive” ORTC 2000 Update. Inconsistencies among the ITWG and ORTC tables are part of this work-in-progress as we move towards the full revision of the ITRS in 2001. Therefore we encourage review of the ITWG tables as a response-to-date.

The 2001 activities focus on a complete revision of the ITRS. Once we have consensus on the 2001 ORTC tables, they will serve as a guide for the activities of the International Technology Working Groups in producing their detailed chapters for the 2001 edition.

The complete 1999 ITRS, along with the latest 2000 Update Tables are available for viewing and printing as an electronic document at the International SEMATECH internet web site <http://public.itrs.net>.

UPDATE OVERVIEW AND OBSERVATION SUMMARY

Please note that the year header on the tables may refer to different points in the development/life cycle of integrated circuits (ICs), depending on the individual line item metric. However, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds 10,000 units per month of ICs from a manufacturing site using “production tooling.” Additional clarification was provided this year by the IRC, requiring a second company to start production within 3 months. To satisfy this definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility.

Furthermore, new IRC guidelines clarified the definition of a Technology Node as the achievement of significant advancement in the process technology. To be explicit, a Technology Node was defined as the achievement of an approximate 0.7x reduction per node (0.5x per two nodes). The period of time in which a new Technology Node is reached is called a “technology-node cycle.” It is acknowledged that continuous improvement occurs between Technology Nodes, and this is reflected by arithmetic interpolation between nodes in the annual columns of the “Near-Term Years” tables. The “Long Term Years” table columns are snapshots at 3-year increments and do not necessarily coincide with Technology Node Years.

In the 1998 ITRS Roadmap Update and the 1999 ITRS Renewal development, a trend was first identified which indicated that the technology node cycle had accelerated by at least one year compared to the 1997 National Technology Roadmap for Semiconductors (NTRS). Additionally, it was discussed that the technology

implementation trend could be moving from a 3-year technology-node cycle to a 2-year rate, and a pull-in of the 130nm node to 2001 was anticipated. However, by the completion of the work on the 1999 ITRS in November, 1999, the 180nm node was pulled in one year to 1999, a 3-year technology node cycle was applied, and the 130nm DRAM half-pitch node target remained in 2002.

During their 2000 ITRS Update activities, the ITWGs and the IRC have concluded that a two-year DRAM half-pitch node cycle rate will indeed be maintained through 2001, pulling in the original 1999 ITRS 130nm node target from 2002 to 2001. Beyond 2001, three possible scenarios were considered for potential technology node (DRAM half-pitch) trends, as summarized below:

Scenario 1 (Sc. 1.0): Pull-in the 130nm DRAM half-pitch to 2001, but then intersect with the original 100nm 1999 ITRS target in 2005. Next, interpolate the annual numbers in-between and extrapolate from the 100nm/2005 point at a 70%/node (0.5×2 nodes) reduction rate.

Scenario 1.5 (Sc. 1.5): Pull-in the 130nm DRAM half-pitch to 2001, but move 100nm to 2004 (a corresponding 1-year pull-in from the original 1999 ITRS point in 2005); then, interpolate the annual numbers in-between, and extrapolate from the new 100nm/2004 point at a 70%/node (0.5×2 nodes) reduction rate.

Scenario 2.0 (also known as the "Best-Case Opportunity" or "Most Aggressive" case) (Sc. 2.0): Pull-in the 130nm DRAM half-pitch to 2001, and also correct the original 100nm, 70nm, 50nm, and 35nm "nodes" to the 70%/node definition (0.5×2 nodes rate): 90nm, 65nm, 33nm, and 23nm, respectively.

Please note in Figure 1 and in Table A the 3-year node cycle is being forecast as a future trend for all scenarios. However, only the new "most aggressive" scenario proposal, Scenario 2.0, includes a correction to the IRC-defined trend rate. The new correction results in a 2-year pull-in of the sub-100-nanometer DRAM half-pitch nodes.

As previously mentioned, for simplification and focus in the 2000 Update publication, only the proposed "most aggressive" Scenario 2.0 was used to develop the complete ORTC Update Tables included in this ORTC 2000 Update document. Scenario 2.0 was also recommended by the IRC for use by the ITWGs as guidance in developing their 2000 Update Tables. The ITWGs responded in their ITWG 2000 Update tables.

For reference and ease of comparison by the reader, the original 1999 ITRS ORTC target roadmap data has been included and identified as **"1999 ITRS"** in the line item labels. The new proposal targets for the 2000 Update "most aggressive" scenario are identified as **"Sc. 2.0"** in the line item identifier, and modified targets are highlighted in **bold blue text**.

Note in Figure 1 that the "printed in resist" MPU Gate Length trend, originally introduced in the 1998/99 ITRS development, remains unchanged from its original trend, but now the leading-edge ASIC and MPU are at the same technology level. New for the 2000 Update is the addition of a trend to track the actual "Physical Bottom Gate Length" of leading-edge MPU and ASIC devices.

ITRS Roadmap Acceleration Continues...

(Including MPU/ASIC "Physical Gate Length" Proposal)

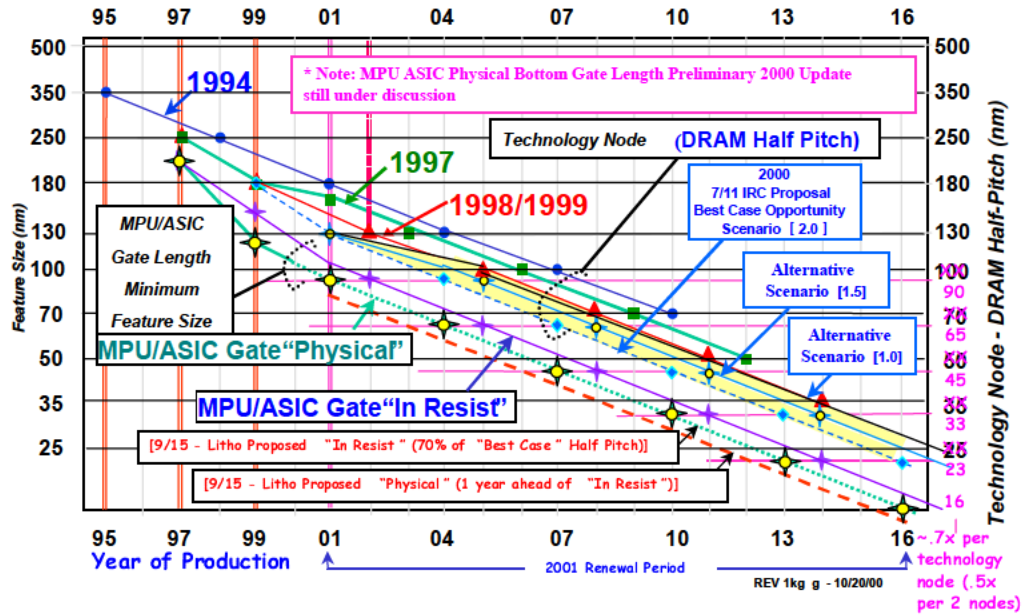


Figure 1 ITRS Roadmap Acceleration Continues...
(Including MPU/ASIC "Physical Gate Length" Proposal and Half-Pitch Trend Correction)

Table A Product Generations and Chip Size Model - **Technology Node Scenarios**

YEAR OF PRODUCTION TECHNOLOGY NODE WAS (1999 ITRS)	1999 180nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
DRAM ½ Pitch (nm) WAS (1999 ITRS)	180	165	150	130	120	110	100	70	50	35
DRAM ½ Pitch (nm) IS [Sc. 1.0] [pull-in 130nm 1 year; 100nm/2005; then .7x/3yrs reduction rate]	180	150	130	120	115	105	100	70	50	35
DRAM ½ Pitch (nm) IS [Sc. 1.5] [pull-in 130nm 1 year; 100nm/2004; then .7x/3yrs reduction rate]	180	150	130	120	110	100	90	65	45	33
DRAM ½ Pitch (nm) IS [Sc. 2.0] [pull-in 130nm 1 year; then .7x/3yrs reduction rate]	180	150	130	115	100	90	80	[60]§	[40]§	[30]§

§ Note that proposed node years for Scenario 2.0 are now 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]

Table 1a Product Generations and Chip Size Model *Technology Nodes*—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
<i>Lithography-Based Characteristics</i>								
DRAM ½ Pitch (nm) (1999)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch (nm) (SC. 2.0)	180	150	130	115	100	90	80	D ½
MPU/ASIC ½ Pitch (nm) (1999)	230	210	180	160	145	130	115	M AND A ½
MPU/ASIC ½ Pitch (nm) (SC. 2.0) [Tied to DRAM]	230	190	160	145	130	115	100	M AND A ½
MPU Gate Length (nm) †† (1999)	140	120	100	85-90	80	70	65	M GATE
ASIC Gate Length (nm) (1999)	180	165	150	130	120	110	100	A GATE
MPU/ASIC Gate Length (In Resist) (nm) †† (SC. 2.0)	140	120	100	90	80	70	65	M AND A GATE
<i>Physical Bottom Gate-Length</i>								
MPU/ASIC Gate Length (nm) †† [NEW]	120	100	90	80	70	65	60	COST/PERFORMANCE

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1b Product Generations and Chip Size Model *Technology Nodes*—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
<i>Lithography-Based Characteristics</i>			
DRAM ½ Pitch (nm) (1999)	70	50	35
DRAM ½ Pitch (nm) (SC. 2.0)	60	40	30
MPU/ASIC ½ Pitch (nm) (1999)	80	55	40
MPU/ASIC ½ Pitch (nm) (SC. 2.0) [Tied to DRAM]	70	50	35
MPU Gate Length (nm) †† (1999)	45	30-32	20-22
ASIC Gate Length (nm) (1999)	70	50	35
MPU/ASIC Gate Length (In Resist) (nm) †† (SC. 2.0)	45	33	23
<i>Physical Bottom Gate-Length</i>			
MPU/ASIC Gate Length (nm) †† [NEW]	40	30	20

†† MPU and ASIC Gate-length (In Resist) node targets refer to most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon", in the 1999 ITRS).

NEW: Trends have been identified, in which the MPU and ASIC "physical bottom" gate lengths may be reduced from the "as-printed" dimension. These "physical bottom" gate-length targets are also included in the FEP, PIDs, and Design TWG Tables as needs which drive device and process technology requirements.

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]

Table 1c **DRAM Production** Product Generations and Chip Size Model—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
DRAM ½ Pitch [f] (nm) (1999)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch [f] (nm) (SC. 2.0)	180	150	130	115	100	90	80	D ½
Cell area factor [A] (1999)	8.0	7.3	6.6	6.0	5.4	4.9	4.4	Market — Cost/Timing
Cell area factor [A] (SC. 2.0)	8.0	8.0	8.0	8.0	8.0	8.0	6.0	Market — Cost/Timing
Cell area [Ca = Af ²] (µm ²) (1999)	0.26	0.20	0.15	0.10	0.08	0.059	0.044	Market — Cost/Timing
Cell area [Ca = Af ²] (µm ²) (SC. 2.0)	0.26	0.18	0.13	0.10	0.082	0.065	0.039	Market — Cost/Timing
Cell array area at production (% of chip size) § (1999)	53%	—	55%	—	53%	—	54%	Market — Cost/Timing
Cell array area at production (% of chip size) § (SC. 2.0)	53.0%	54.0%	54.8%	55.3%	55.7%	56.1%	56.4%	Market — Cost/Timing
Generation at production § (1999)/(SC. 2.0)	256M	—	512M	—	1G	—	2G	Market — Cost/Timing
Functions per chip (Gbits) [NEW]	0.268	0.380	0.537	0.759	1.07	1.52	2.15	Market — Cost/Timing
Chip size at production (mm ²) § (1999)	132	—	145	—	159	—	174	Market — Cost/Timing
Chip size at production (mm ²) § (SC. 2.0)	131	129	127	141	157	175	147	Market — Cost/Timing
Gbits/cm ² at production § (1999)	0.20	—	0.37	—	0.68	—	1.23	Market — Cost/Timing
Gbits/cm ² at production § (SC. 2.0)	0.20	0.29	0.42	0.54	0.68	0.87	1.46	Market — Cost/Timing

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1d **DRAM Production** Product Generations and Chip Size Model—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]
DRAM ½ Pitch [f] (nm) (1999)	70	50	35
DRAM ½ Pitch [f] (nm) (SC. 2.0)	60	40	30
Cell area factor [A] (1999)	3.5	3.0	2.5
Cell area factor [A] (SC. 2.0)	6.0	4.0	4.0
Cell area [Ca = Af ²] (μm ²) (1999)	0.017	0.008	0.003
Cell area [Ca = Af ²] (μm ²) (SC. 2.0)	0.019	0.0064	0.0032
Cell array area at production (% of chip size) § (1999)	52%	56%	57%
Cell array area at production (% of chip size) § (SC. 2.0)	57.3%	57.8%	58.2%
Generation at production § (1999)	[5.7]	16G	[45.2G]
Generation at production § (SC. 2.0)	[66]	16G	[486]
Functions per chip (Gbits) [NEW]	6.1	17.2	48.6
Chip size at production (mm ²) § (1999)	199	229	262
Chip size at production (mm ²) § (SC. 2.0)	205	191	268
Gbits/cm ² at production § (1999)	3.05	7.51	18.5
bits/cm ² at production § (SC. 2.0)	2.97	8.99	18.1

§ DRAM Model—Cell Factor (design/process improvement) targets are: 1999-2004/8x; 2005-2010/6x; 2011-2016/4x. DRAM product generations are usually increased by 4x bits/chip every four years with interim 2x bits/chip generations, except: 1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4x/5years (2x/2-3yrs); and 2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4x/5years (2x/2-3yrs). InTER-generation chip size growth rate varies to maintain 1 chip per 572mm² field at Introduction and 2 chip per 572mm² field at Production. The more aggressive "best case opportunity" technology node trends allow the Production-phase products to remain at 2x bits/chip every 2 years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5x every technology node in-between cell factor reductions.

Note: Long-Term nodes now fall on: 2010/45; 2013/33; 2016/25

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

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YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1e **DRAM Introduction** Product Generations and Chip Size Model—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
DRAM ½ Pitch [f] (nm) (1999)	180	165	150	130	120	110	100	D ½
DRAM ½ Pitch [f] (nm) (SC. 2.0)	180	150	130	115	100	90	80	D ½
Cell area factor [A] (1999)	8.0	7.3	6.6	6.0	5.4	4.9	4.4	Market — Cost/Timing
Cell area factor [A] (SC. 2.0)	8.0	8.0	8.0	8.0	8.0	8.0	6.0	Market — Cost/Timing
Cell area [Ca = Af ²] (μm ²) (1999)	0.26	0.20	0.15	0.10	0.08	0.059	0.044	Market — Cost/Timing
Cell area [Ca = Af ²] (μm ²) (SC. 2.0)	0.259	0.183	0.130	0.103	0.082	0.065	0.039	Market — Cost/Timing
Cell array area at introduction (% of chip size) § (1999)	70%	—	72%	—	70%	—	72%	Market — Cost/Timing
Cell array area at introduction (% of chip size) § (SC. 2.0)	69.5%	70.5%	71.3%	71.8%	72.2%	72.6%	72.9%	Market — Cost/Timing
Generation at introduction § (1999)	1G	—	2G	—	4G	—	8G	—
Generation at introduction § (SC. 2.0)	1G	—	2G	—	4G	—	8G	—
Functions per chip (Gbits) (1999)	1.07	—	2.15	—	4.29	—	8.59	Market — Moore's Law
Functions per chip (Gbits) (SC. 2.0)	1.07	1.52	2.15	3.04	4.29	6.07	8.59	Market — Cost/Timing
Chip size at introduction (mm ²) § (1999)	400	—	438	—	480	—	526	Market — Cost/Timing
Chip size at introduction (mm ²) § (SC. 2.0)	400	395	390	435	485	542	454	Market — Cost/Timing
Gbits/cm ² at introduction § (1999)	0.27	—	0.49	—	0.89	—	1.63	Market — Cost/Timing
Gbits/cm ² at introduction § (SC. 2.0)	0.27	0.38	0.55	0.70	0.88	1.12	1.89	Market — Cost/Timing

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

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YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1f **DRAM Introduction** Product Generations and Chip Size Model—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
DRAM ½ Pitch [f] (nm) (1999)	70	50	35
DRAM ½ Pitch [f] (nm) (SC. 2.0)	60	40	30
Cell area factor [A] (1999)	3.5	3.0	2.5
Cell area factor [A] (SC. 2.0)	6.0	4.0	4.0
Cell area [Ca = Af²] (µm²) (1999)	0.017	0.008	0.003
Cell area [Ca = Af²] (µm²) (SC. 2.0)	0.019	0.0064	0.0032
Cell array area at introduction (% of chip size) \$ (1999)	69%	75%	75%
Cell array area at introduction (% of chip size) \$ (SC. 2.0)	73.3%	74.3%	74.7%
Generation at introduction \$ (1999)	[22.6G]	64G	[181G]
Generation at introduction \$ (SC. 2.0)	[206]	[456]	[1046]
Functions per chip (Gbits) (1999)	24.3	68.7	194
Functions per chip (Gbits) (SC. 2.0)	19.7	45.3	104.2
Chip size at introduction (mm²) \$ (1999)	603	691	792
Chip size at introduction (mm²) \$ (SC. 2.0)	516	392	448
Gbits/cm² at introduction \$ (1999)	4.03	9.94	24.5
Gbits/cm² at introduction \$ (SC. 2.0)	3.82	11.56	23.25

* In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. The subsequent contents of this Table have been tied to update so as to reflect the new TN.

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YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
Process/design annual improvement factor ++ (1999)	0.90	0.90	0.90	0.91	0.92	0.93	0.93	Market — Cost/Timing
(SC. 2.0)	1.00	1.00	1.00	0.93	0.93	0.93	0.93	
Transistor density SRAM at introduction (Mtransistors/cm ²) (1999)/(SC. 2.0)	35	50	70	95	128	173	234	Market — Cost/Timing
Transistor density logic at introduction (Mtransistors/cm ²) (1999)/(SC. 2.0)	6.6	9.4	13	18	24	33	44	Market — Cost/Timing
Generation at introduction * (1999)/(SC. 2.0)	p99c	—	p01c	—	p03c	—	p05c	—
Functions per chip (million transistors [Mtransistors]) (1999)	23.8	—	47.6	—	95.2	—	190	Market — Moore's Law
(1999)/(SC. 2.0)	23.8	33.7	47.6	67.3	95.2	135	190	
Chip size at introduction (mm ²) ‡ (1999)	340	—	340	—	372	—	408	Market — Cost/Timing
(SC. 2.0)	340	340	340	356	372	390	408	
Cost performance MPU (Mtransistors/cm ² at introduction) (including on-chip SRAM) ‡ (1999)	7	—	14	—	26	—	47	M Gate and M and A ½
(SC. 2.0)	7.0	9.9	14.0	18.9	25.6	34.5	46.7	
Generation at production *	p97c	—	p99c	—	p01c	—	P03c	—
Chip size at production (mm ²) §§ (1999)	170	—	170	—	214	—	235	Market — Cost/Timing
(SC. 2.0)	170	170	170	178	186	195	204	
Cost performance MPU (Mtransistors/cm ² at production, including on-chip SRAM) ‡ (1999)	7	—	14	—	22	—	41	M Gate and M and A ½
(SC. 2.0)	7.0	9.9	14.0	18.9	25.6	34.5	46.7	

++ The MPU Process/design improvement factor is an estimate of the additional annual functional area reduction required beyond the area reduction contributed by the MPU metal half-pitch reduction. Note that this additional area reduction for transistor density plays a role generally analogous to the "cell area factor" for DRAMs. It has been achieved historically through a combination of many factors, for example: use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout.

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All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Process/design improvement factor (1999)	0.93	0.93	0.93
(SC. 2.0)	0.93	0.93	0.93
Transistor density SRAM at introduction (Mtransistors/cm ²) (1999)/(SC. 2.0)	577	1,423	3,510
Transistor density logic at introduction (Mtransistors/cm ²) (1999)/(SC. 2.0)	109	269	664
Generation at introduction *	—	p11c	—
Functions per chip (million transistors (Mtransistors) (1999)/(SC. 2.0)	539	1,523	4,308
Chip size at introduction (mm ²) ‡ (1999)	468	536	615
(SC. 2.0)	468	536	615
Cost-performance MPU Mtransistors/cm ² at introduction (including on-chip SRAM) ‡ (1999)	115	284	701
(SC. 2.0)	115	284	701
Generation at production *	—	p09c	—
Chip size at production (mm ²) § (1999)/(SC. 2.0)	269	308	354
(SC. 2.0)	234	268	307
Cost performance MPU Mtransistors/cm ² at production (including on-chip SRAM) ‡ (1999)	100	247	609
(SC. 2.0)	115	284	701

* p is processor, numerals reflect year of introduction, c is cost-performance product.

** p is processor, numerals reflect year at ramp, h is high-performance product.

† MPU Cost-performance Model—Cost-performance MPU includes small level 1 (L1) on-chip SRAM (32Kbyte/1999), but consists primarily of logic transistor functionality; both SRAM and Logic functionality doubles every two years.

‡ MPU High-performance Model—High-performance MPU includes large level 2 (L2) on-chip SRAM (2MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + 98Mtransistors (2048 bytes × 8 bits/byte × 6 transistors/bit) L2 SRAM = 110Mtransistors/1999); both SRAM and Logic functionality doubles every two years.

‡ MPU High-performance Model—High-performance MPU includes large level 2 (L2) on-chip SRAM (1MByte/1999) added to ramp-level cost-performance core functionality shrunk from 2-year-prior generation (P99h = 11.9M transistor (Mtransistors) (shrunk P97 core) + 49Mtransistors (1024 bytes × 8 bits/byte × 6 transistors/bit) L2 SRAM = 61Mtransistors/1999); both SRAM and Logic functionality doubles every two years.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates can be kept flat through 2001, due to the more aggressive MPU/ASIC half-pitch technology node trend; but beyond 2001, the target growth rate is 1.2× growth every four years. The InTRA-generation chip size shrink model is 0.5× every two years through 2001, then 0.5× every three years after 2001.

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2000 UPDATE

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]

Table 1i *High-Performance MPU and ASIC Product Generations and Chip Size Model—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	DRIVER
Logic (Low-volume Microprocessor) High-performance ‡								
Generation at production ** (1999)/(SC. 2.0)	p99h	—	p01h	—	p03h	—	p05h	—
Functions per chip (million transistors) (1999)	110	—	220	—	441	—	882	Market — Moore's Law
(SC. 2.0)	61	86	122	173	244	345	488	
Chip size at production (mm ²) § (1999)	450	—	450	—	567	—	622	Market — Cost/Timing
(SC. 2.0)	310	310	310	325	340	356	372	
High-performance MPU Mtransistors/cm ² at production (including on-chip SRAM) ‡ (1999)	24	—	49	—	78	—	142	M Gate and M and A ½
(SC. 2.0)	19.7	27.8	39.4	53.2	71.9	97.1	131	
ASIC								
ASIC usable Mtransistors/cm ² (auto layout) (1999)	20	28	40	54	73	99	133	M Gate and M and A ½
(SC. 2.0)	19.7	27.8	39.4	53.2	71.9	97.1	131	
ASIC max chip size at production (mm ²) (maximum lithographic field size) (1999)	800	800	800	800	800	800	800	Lithographic Field Size
(SC. 2.0)	800	800	800	800	572	572	572	
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size) (1999)	160	224	320	432	584	800	1064	Market — Performance/ Timing
(SC. 2.0)	157	223	315	426	411	556	751	

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All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 1j *High-Performance MPU and ASIC Product Generations and Chip Size Model—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Logic (Low-volume Microprocessor) High-performance ‡			
Generation at production ‡ (1999)/(SC. 2.0)	—	p11h	—
Functions per chip (million transistors) (1999)	2,494	7,053	19,949
(SC. 2.0)	1,381	3,907	11,052
Chip size at production (mm ²) § (1999)	713	817	937
(SC. 2.0)	427	489	561
High-performance MPU Mtransistors/cm ² at production (including on-chip SRAM) ‡ (1999)	350	863	2,130
(SC. 2.0)	324	799	1,970
ASIC			
ASIC usable Mtransistors/cm ² (auto layout) (1999)	328	811	2,000
(SC. 2.0)	324	799	1,970
ASIC maximum chip size at production (mm ²) (maximum lithographic field size) (1999)	800	800	800
(SC. 2.0)	572	572	572
ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size) (1999)	2,624	6,488	16,000
(SC. 2.0)	1,852	4,568	11,269

Since only the 2011 odd-year product generation data column is available in the Long Term table format, interpolated numbers were calculated and included in the 2008 and 2014 node columns. The extended market-need-based product trends for the product generation two-year-cycle years (1999, 2001, 2003, 2005, 2007, 2009, 2011, 2013) are forecast to follow patterns established in Near Term Table 1a.

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OTHER ORTC TABLES, TWG LINE ITEMS/OWNERS

Table	Line Item	TWG Owner
♦ Table 2a,b	Litho Field Size	Lithography
♦	Wafer Size	Front End Processes, Factory Integration
♦ Table 3a,b	# of Chip I/O's	Test, Design
♦	# of Package Pins/Balls	Test, Assembly & Packaging
♦ Table 4a,b	Chip Pad Pitch	Assembly & Packaging
♦	Cost-Per-Pin	Assembly & Packaging
♦ Table 4c,d	Chip Frequency	Design
♦	Chip-to-Board Freq.	Assembly & Packaging
♦	Max # Wire Levels	Interconnect
♦ Table 5a,b	Electrical Defects	Defect Reduction
♦ Table 6a,b	P.Supply Volt.	Process Integration, Devices, Structures
♦	Max. Power	Design, Process Integration, Devices, Structures
♦ Table 7a,b	Affordable Cost	Economic (Alan Allan acting)
♦	Test Cost	Test

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 2a ~~Chip Size~~, Lithographic-Field and Wafer-Size Trends—Near Term Years*

(Note: 1999 Lithographic field sizes represent current capability)

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Lithography Field Size							
Maximum lithographic field size — area (mm ²) (1999)	800	800	800	800	800	800	800
Lithography Field Size—area (mm ²) (SC. 2.0)	800	800	800	800	800	572	572
Maximum lithographic field size — length (mm) (1999)	32	32	32	32	32	32	32
Maximum lithographic field size — width (mm) (1999)	25	25	25	25	25	25	25
Lithographic field size (width X length [mm ²]) (SC. 2.0)	25x32	25x32	25x32	25x32	25x32	22x26	22x26
Maximum Substrate Diameter (mm) — High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer (1999)	200	200	300	300	300	300	300
(SC. 2.0)	200	200	300	300	300	300	300

Table 2b ~~Chip Size~~, Lithographic-Field and Wafer Size Trends—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Lithography Field Size			
Maximum lithographic field size—area (mm ²) (1999)	800	800	800
Lithography Field Size—area (mm ²) (SC. 2.0)	572	572	572
Maximum lithographic field size—length (mm) (1999)	32	32	32
Maximum lithographic field size—width (mm) (1999)	25	25	25
Lithographic field size (width X length [mm ²]) (SC. 2)	22x26	22x26	22x26
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)			
Bulk or epitaxial or SOI wafer (1999)	300	300	450
(SC. 2.0)	300	450	450

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2000 UPDATE

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90 nm	2005
Number of Chip I/Os (Number of Total Chip Pads) — Maximum							
Total pads—MPU (1999)	2,304	2,560	3,042	3,042	3,042	3,042	3,042
Signal I/O—MPU (1/3 of total pads) (1999)	768	1,024	1,024	1,024	1,024	1,024	1,024
Power and ground pads—MPU (2/3 of total pads) (1999)	1,536	1,536	2,018	2,018	2,018	2,018	2,018
Total pads—ASIC high-performance (1999)	1,400	1,800	2,200	2,600	3,000	3,400	3,800
Signal I/O pads—ASIC high-performance (1/2 of total pads) (1999)	700	900	1,100	1,300	1,500	1,700	1,900
Power and ground pads—ASIC high-performance (1/2 of total pads) (1999)	700	900	1,100	1,300	1,500	1,700	1,900
Chip-to-package pads (Peripheral) (1999)	368	397	429	464	501	541	584
Number of Total Package Pins/Balls—Maximum							
Microprocessor/controller, cost-performance (1999)	740	821	912	1,012	1,123	1,247	1,384
ASIC (high-performance) (1999)	1,600	1,792	2,007	2,248	2,518	2,820	3,158

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (Sc. 2.0)	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]
Number of Chip I/Os (Number of Total Chip Pads)—Maximum			
Total pads—MPU (1999)	3,840	4,224	4,416
Signal I/O pads—MPU (1/3 of total pads) (1999)	1,280	1,408	1,472
Power and ground pads—MPU (2/3 of total pads) (1999)	2,560	2,816	2,944
Total pads—ASIC high-performance (1999)	4,600	5,400	6,000
Signal I/O pads—ASIC high-performance (1/2 of total pads) (1999)	2,300	2,700	3,000
Power and ground pads—ASIC high-performance (1/2 of total pads) (1999)	2,300	2,700	3,000
Chip-to-package pads (Peripheral) (1999)	736	927	1,167
Number of Total Package Pins/Balls—Maximum			
Microprocessor/controller, cost-performance (1999)	1,893	2,589	3,541
ASIC (high-performance) (1999)	4,437	6,234	8,758

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 4a Performance and Package Chips: Pads, Cost, and Frequency—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Chip Pad Pitch (micron)							
Pad pitch—ball bond (1999)	50	48	47	45	43	42	40
(2000)	50	50	45	35	30	25	20
Pad pitch—wedge bond (1999)	45	43	42	40	39	38	35
(2000)	45	45	40	35	30	25	20
Package cost (cents/pin) (cost-performance)—minimum (1999)	200	200	200	200	182	165	150
(2000)	200	200	175	175	150	150	130
Pad Pitch—area array (handheld, low-cost, harsh) NEW	180	165	150	130	120	110	100
Cost-Per-Pin							
Package cost (cents/pin) (cost-performance)—maximum (1999)	1.90	1.81	1.71	1.63	1.55	1.47	1.40
(2000)	1.90	1.40	1.33	1.26	1.20	1.14	1.08
Package cost (cents/pin) (cost-performance)—minimum (1999)/(2000)	0.90	0.86	0.81	0.77	0.73	0.70	0.66
Package cost (cents/pin) (Memory)—maximum (1999)/(2000)	1.90	1.71	1.54	1.39	1.25	1.12	1.01
Package cost (cents/pin) (Memory)—minimum (1999)/(2000)	0.40	0.38	0.36	0.34	0.33	0.31	0.29

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2000 UPDATE

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 4b Performance and Package Chips: Pads, Cost, and Frequency—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Chip Pad Pitch (micron)			
Pad pitch—ball bond (1999)	40	40	40
(2000)	20	20	20
Pad Pitch—wedge bond (1999)	35	35	35
(2000)	20	20	20
Pad Pitch—area array (cost-performance, high-performance) (1999)	150	150	150
(2000)	115	100	80
Pad Pitch—area array (handheld, low-cost, harsh) NEW	70	50	35
Cost-Per-Pin			
Package cost (cents/pin) (cost-performance)—maximum (1999)	1.20	1.03	0.88
(2000)	1.03	0.98	0.93
Package cost (cents/pin) (cost-performance)—minimum (1999)/(2000)	0.57	0.49	0.42
(1999)/(2000)	0.74	0.54	0.39
Package cost (cents/pin) (memory)—minimum (1999)/(2000)	0.25	0.22	0.19

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All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 4c Performance and Package Chips: ~~Pads, Cost, and Frequency,~~
*On-Chip Wiring Levels—Near Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90 nm	2005
Chip Frequency (MHz)							
On-chip local clock, (high-performance) (1999)	1,250	1,486	1,767	2,100	2,490	2,952	3,500
(2000)		1,620	2,100	2,490	2,952	3,500	4,150
On-chip, across-chip clock (high-performance) (1999)	1,200	1,321	1,454	1,600	1,724	1,857	2,000
(2000)		1,386	1,600	1,724	1,857	2,000	2,155
On-chip, across-chip clock, high-performance ASIC (1999)	500	559	626	700	761	828	900
(2000)		592	700	761	828	900	980
On-chip, across-chip clock (cost-performance) (1999)	600	660	727	800	890	989	1,100
(2000)		693	800	890	989	1,100	1,225
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus) (1999)	1,200	1,321	1,454	1,600	1,724	1,857	2,000
(2000)		1,386	1,600	1,724	1,857	2,000	2,155
Chip-to-board (off-chip) speed (high-performance, for peripheral buses) (1999)	480	589	722	885	932	982	1,035
(2000)	480	693	800	862	929	1000	1078
Maximum number wiring levels—maximum (1999)/(2000)	7	7	7	8	8	8	9
Maximum number wiring levels—minimum (1999)/(2000)	6	6	7	7	8	8	8

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All the items and/or numericals modified from the 1999 ITRS are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]

Table 4d Performance and Package Chips: ~~Pads, Cost, and Frequency,~~
*On-Chip Wiring Levels—Long Term Years**

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (Sc. 2.0)	2008 [60 nm]	2011 [40 nm]	2014 [30 nm]
Chip Frequency (MHz)			
On-chip local clock, (high-performance) (1999)	6,000	10,000	13,500
(2000)	7,115	11,050	14,920
On-chip, across-chip clock (high-performance) (1999)	2,500	3,000	3,600
(2000)	2,655	3,190	3,825
On-chip, across-chip clock (high-performance ASIC) (1999)	1,200	1,500	1,800
(2000)	1,295	1,595	1,913
On-chip, across-chip clock (cost-performance) (1999)	1,400	1,800	2,200
(2000)	1,522	1,925	2,350
Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus) (1999)	2,500	3,000	3,600
(2000)	2,655	3,190	3,825
Chip-to-board (off-chip) speed (high-performance, for peripheral buses) (1999)	1,285	1,540	1,800
(2000)	1328	1595	1913
Maximum number wiring levels—minimum (1999)/(2000)	9	10	10
Maximum number wiring levels—minimum (1999)/(2000)	9	9	10

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Table 5a Electrical Defects—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Defect Reduction							
DRAM at production electrical D_0 chip size at 85% yield (d/m^2) § (1999)	1,249	1,193	1,140	1,089	1,040	994	950
(2000)	1,259	1,282	1,302	1,170	1,050	942	1126
MPU at production electrical D_0 chip size at 75% yield (d/m^2) §§ (1999)	1,742	1,742	1,742	1,552	1,383	1,321	1,262
(2000)	1,742	1,742	1,742	1,664	1,590	1,519	1,452
ASIC first year electrical D_0 at 65% yield (d/m^2) (1999)	562	562	562	562	562	562	562
(2000)	562	562	562	562	787	787	787
Minimum, mask count—maximum (1999)	24	24	24	24	25	25	26
(2000)	24	24	24	25	25	26	26
Minimum, mask count—minimum (1999)	22	23	23	24	24	24	24
(2000)	22	23	24	24	24	24	24

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YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 5b Electrical Defects—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Defect Reduction			
DRAM at production electrical D_0 chip size at 85% yield (d/m^2) § (1999)	828	723	630
(2000)	807	865	660
MPU at production electrical D_0 chip size at 75% yield (d/m^2) §§ (1999)	1,101	960	837
(2000)	1,266	1,104	963
ASIC first year electrical D_0 at 65% yield (d/m^2) (1999)	562	562	562
(2000)	787	787	787
Minimum, mask count—maximum (1999)	28	28	30
(2000)	28	28	30
Minimum, mask count—minimum (1999)	26	28	29
(2000)	26	28	29

D_0 —defect density

§ DRAM Model—Cell Factor (design/process improvement) targets are: 1999–2004/8x; 2005–2010/6x; 2011–2016/4x. DRAM product generations are usually increased by 4x bits/chip every four years with interim 2x bits/chip generations, except: 1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4x/5years (2x/2–3yrs); and 2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4x/5years (2x/2–3yrs). InTER-generation chip size growth rate varies to maintain 1 chip per 572mm² field at Introduction and 2 chip per 572mm² field at Production. The more aggressive “best case opportunity” technology node trends allow the Production-phase products to remain at 2x bits/chip every 2 years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5x every technology node in-between cell factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates can be kept flat through 2001, due to the more aggressive MPU/ASIC half-pitch technology node trend; but beyond 2001, the target growth rate is 1.2x growth every four years. The InTRA-generation chip size shrink model is 0.5x every two years through 2001, then 0.5x every three years after 2001.

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Table 6a Power Supply and Power Dissipation—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Power Supply Voltage (V)							
Minimum logic V_{dd} (V)—maximum (for maximum performance) (1999)	1.8	1.8	1.5	1.5	1.5	1.2	1.2
(2000)	1.8	1.8	1.5	1.5	1.2	1.2	1.1
Minimum logic V_{dd} (V)—minimum (for lowest power) (1999)	1.5	1.5	1.2	1.2	1.2	0.9	0.9
(2000)	1.5	1.5	1.2	1.2	0.9	0.9	0.8
Maximum Power							
High-performance with heatsink (W)	90	100	115	130	140	150	160
(2000)	90	108	130	140	150	160	170
Battery (W)—(hand-held) (1999)	1.4	1.6	1.7	2.0	2.1	2.3	2.4
(2000)	1.4	1.7	2.0	2.1	2.3	2.4	2.6

Table 6b Power Supply and Power Dissipation—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Power Supply Voltage (V)			
Minimum logic V_{dd} (V)—maximum (for maximum performance) (1999)	0.9	0.6	0.60
(2000)	0.9	0.6	0.60
Minimum logic V_{dd} (V)—minimum (for lowest power) (1999)	0.6	0.5	0.30
(2000)	0.6	0.5	0.30
Maximum Power			
High-performance with heatsink (W) (1999)	170	174	183
(2000)	171	177	186
Battery (W)—(hand-held) (1999)	2.0	2.2	2.4
(2000)	2.1	2.3	2.5

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Table 7a Cost—Near Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction (1999)/(SC. 2.0)	42	—	21	—	11	—	5.3
DRAM cost/bit at (packaged microcents) at production \$ (1999)/(SC. 2.0)	15	—	7.6	—	3.8	—	1.9
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction \$\$ (1999)/(SC. 2.0)	1,735	—	868	—	434	—	217
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production \$\$ (1999)/(SC. 2.0)	1,050	—	525	—	262	—	131
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production \$\$ (1999)/(SC. 2.0)	245	—	123	—	61	—	31
Cost-Per-Pin (see Table 4) (1999)/(SC. 2.0)	—	—	—	—	—	—	—
Test							
Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—maximum (1999)/(SC. 2.0)	8	7	7	6	6	5	5
Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—minimum (1999)/(SC. 2.0)	4	3	3	3	3	2	2
Volume tester cost/pin (\$K/pin) (cost-performance MPU) (1999)/(SC. 2.0)	8	8	7	7	6	6	5

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Table 7b Cost—Long Term Years*

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]
Affordable Cost per Function ++			
DRAM cost/bit (packaged microcents) at samples/introduction (1999)/(SC. 2.0)	—	0.66	—
DRAM cost/bit (packaged microcents) at production § (1999)/(SC. 2.0)	—	0.24	—
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§ (1999)/(SC. 2.0)	—	27	—
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	—	16	—
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§ (1999)/(SC. 2.0)	—	3.8	—
Cost-Per-Pin (see Table 4) (1999)/(SC. 2.0)	—	—	—
Test			
Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—maximum (1999)/(SC. 2.0)	5	5	5
Volume tester cost per high-frequency signal pin (\$K/pin) (high-performance ASIC)—minimum (1999)/(SC. 2.0)	N/A	N/A	N/A
Volume tester cost/pin (\$K/pin) (cost-performance MPU) (1999)/(SC. 2.0)	4	2	2

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5x/two years inTER-generation reduction rate model used; .55x/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically 7–8 years after introduction; MPU unit volume life-cycle peak occurs typically after four years, when the next generation processor enters its ramp phase (typically two years after introduction).

§ DRAM Model—Cell Factor (design/process improvement) targets are: 1999–2004/8x; 2005–2010/6x; 2011–2016/4x. DRAM product generations are usually increased by 4x bits/chip every four years with interim 2x bits/chip generations, except: 1) at the Introduction phase, after the 8Gbit interim generation, the introduction rate is 4x/5years (2x/2–3yrs); and 2) at the Production phase, after the interim 32Gbit generation, the introduction rate is 4x/5years (2x/2–3yrs). InTER-generation chip size growth rate varies to maintain 1 chip per 572mm² field at Introduction and 2 chip per 572mm² field at Production. The more aggressive “best case opportunity” technology node trends allow the Production-phase products to remain at 2x bits/chip every 2 years and still fit within the target of two DRAM chips per 572mm² field size, through the 32Gbit interim generation. The InTRA-generation chip size shrink model is 0.5x every technology node in-between cell factor reductions.

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ITRS TABLE DEFINITIONS/GUIDELINES

Proposal Rev1, 7/11/00

- Technology Requirements Perspective
 - Near-Term Years : First Yr. Ref.+ 6 yr\$'cast (ex. 1999 through 2005), annually
 - Long-Term Years : Following 9 years (ex.: 2008, 2011, and 2014), every 3 year
 - Technology Node :
 - General indices of technology development.
 - Approximately 70% of the preceding node, 50% of 2 preceding nodes.
 - Each step represents the creation of significant technology progress
 - Example: DRAM half pitches (2000 ITRS) of 180, 130, 90, 65, 45 and 33nm
 - *Year 2000 : Smallest 1/2 pitch among DRAM, ASIC, MPU, etc
 - Year of Production:
 - The volume = *10K units (devices)/month. ASICs manufactured by same process technology are granted as same devices
 - Beginning of manufacturing by *a company and another company starts production within 3 months
 - Technology Requirements Color:
 - Red : ManufacturableSolutions are NOT known
 - Yellow : ManufacturableSolutions are known
 - White : ManufacturableSolutions exist, and they are being optimized
- *Year 2000 : Red cannot exist in next 3 years (2000, 2001, 2002)*
 *Year 2000 : Yellow cannot exist in next 1 year (2000)

** Exception: Solution NOT known, but does not prevent Production manufacturing

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GLOSSARY – ORTC 2000 UPDATE EDITION

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

TECHNOLOGY NODE (nm)—

Each technology node step represents the creation of significant technology progress - approximately 70% of the preceding node, 50% of 2 preceding nodes. Example: DRAM half pitches (2000 ITRS) of 180, 130, 90, 65, 45 and 33 nm. The ground rules of process governed by the smallest feature printed. The half-pitch of first-level interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. For logic, such as microprocessors (MPUs), **physical bottom gate length** is most representative of the leading-edge technology level required for maximum performance. MPU and ASIC logic interconnect half-pitch processing requirement **typically refers to the first metal layer** and lags behind DRAM half-pitch, **which may refer either first layer polysilicon or metal**. For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

“MOORE’S LAW”—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a “self-fulfilling” prophecy, “Moore’s Law” has been a consistent macro trend, and key indicator of successful leading-edge semiconductor products and companies, for the past 30 years.

“COST-PER-FUNCTION” MANUFACTURING PRODUCTIVITY IMPROVEMENT DRIVER—In addition to “Moore’s Law”, there is a historically-based “corollary” to the “law,” which suggests that, to be competitive, manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every two years, as suggested by consensus DRAM and MPU models of the 1999 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

“Affordable” Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by **Functions/Chip**. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market “top-down” needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership (CoO); 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

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DRAM Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration, Introduction, Sample, Production, Ramp, Peak).

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction, Ramp, Peak, Embedded).

Cost-Performance MPU—MPU product optimized for lowest cost by minimizing on-chip SRAM to level-one (L1) cache only (32Kbytes/1999). Logic functionality and L1 cache typically double every 2-year generation. This typically has a 6-year (introduction plus ramp plus peak) computer-market-application life-cycle before being replaced by the next generation cost-performance MPU, then continues on in embedded applications.

High-performance MPU—MPU product optimized for maximum system performance by using a shrunk cost-performance ramp-level MPU core combined with a large (1Mbyte/1999) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two-year generation. Typically has only a 4-year (ramp and peak) life cycle in the relatively low-volume, higher-priced, high-performance computer market. There is no classic “embedded” application for the high-SRAM-content MPU, but that may change as future market demand develops for multiple-MPU-per box internet server and communication processor applications emerge. Those applications will provide increased demand for more cost-effective inTRA generation shrinks of the high-performance MPU, thus extending the life-cycles of future generations.

PRODUCT INTER-GENERATION—Product generation-to-generation targets for periodically increasing on-chip functionality and allowable chip size. The targets are set to maintain “Moore’s Law,” while preserving economical manufacturability. The 1999 ITRS consensus target for the rate of increase of DRAM and MPU inTER-generation functionality is 2×/chip every two years. The allowable inTER-generational chip size growth for DRAMs was 1.2× every four years in the 1999 ITRS, but is now limited by the maximum available lithography field size and also the cell shrink limitations imposed by the achievable cell area factor targets. For MPUs, the allowable chip size growth is flat through 2001, then grows at 1.2× every four years. To add only 20% in area every four years, while quadrupling functionality, requires an inTER-generation design productivity which further reduces chip size by an additional minus 7–8 % per year. This design-related productivity reduction is in addition to the basic lithography-provided area reduction of -11% per year.

PRODUCT INTRA-GENERATION—Within a given product generation. The consensus-based targets reduce chip size (by shrinks and “cut-downs”) utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS consensus targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node. For DRAM, this reduction of minus 50% occurs every three years, or minus 37% every two years. For MPU, the 50% reduction occurs every two years through 2001, then slows to minus 37% per two years (same as DRAM).

YEAR OF DEMONSTRATION—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration-level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three years at the leading-edge process technology node, typically 2–3 years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be “stitched” together via multiple-exposure

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techniques that are feasible only for very small quantities of laboratory samples.

Example: 1997/ISSCC/1Gb DRAM.

YEAR OF INTRODUCTION (DRAM)—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, DRAM products will be introduced at 2× functionality per chip every two years. In addition, manufacturers will delay introduction until a chip-size shrink or “cut-down” level is achieved which limits the inTER-generation chip-size growth to 1.2× every 4 years, or approximately 1.1× every 2-year generation in the 1999 ITRS, but is now limited by the maximum available lithography field size and also the cell shrink limitations imposed by the achievable cell area factor targets Example: 1999/1Gb DRAM.

YEAR OF PRODUCTION (DRAM)—Year in which leading chip manufacturers begin shipping volume quantities (10K/month) of product manufactured with qualified production tooling and processes and is followed within three months by a second manufacturer. This product typically contains one-fourth (1/4) the bits per chip of the introduction-level generation design, from which it is “cut-down.” Example: 1999/256Mb DRAM.

YEAR OF INTRODUCTION (MPU)—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. The introduction cost-performance MPU may be combined in a multi-chip module, along with L2 cache, in low-volume computer applications which demand high performance.

YEAR OF PRODUCTION (MPU)—Year in which leading chip manufacturers begin shipping volume quantities (10K/month) of product manufactured with qualified production tooling and processes and is followed within three months by a second manufacturer. As demand increases, the tooling and processes are being quickly “copied” into multiple modules of manufacturing capacity. Lower-volume, high-performance MPUs are also ramping concurrently as its co-existing cost-performance MPU core, but the L2 cache is now included on-chip but with twice the memory as its high-performance-generation predecessor.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs, application-specific integrated circuits [ASICs]) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm²)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS analyst consensus models).

Functions/cm²—The density of functions in a given square centimeter = **Functions/Chip** on a single monolithic chip divided by the **Chip Size**. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. Most typical ASIC designs will be slightly less dense than the high-performance MPUs, which are mostly SRAM.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe

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2000 UPDATE

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
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area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 55% at the production level, and less than 50% at the ramp level).

DRAM Cell Area (μm^2)—The measure of the maximum allowable DRAM memory bit cell area specified by the requirement to meet the target chip size and cell array area percentage requirements. May also be expressed as the cell area factor – number of equivalent units of area of a square of the DRAM half-pitch. Minimizing the area for the cell is in conflict with the desire to maximize the capacitance storage capability of the continuously shrinking cell. This creates a conflict between the technical feasibility of the cell area required to meet the economic constraints of the maximum allowable chip size.

DRAM Cell Area Factor—The measure of the maximum allowable DRAM memory bit cell area, expressed as the number of equivalent units of area of a square of the DRAM half-pitch.

Example: 1999: square of the half-pitch = $(180\text{ nm})^2 = .032\text{ }\mu\text{m}^2$; maximum cell area for 1Gb DRAM to be < 70% of total chip area = $0.26\text{ }\mu\text{m}^2$; therefore, the maximum cell area factor = $0.26/0.32 = 8$. The cell factor is also often expressed by equivalent aspect ratios of the half-pitch units ($2\times 4 = 8$, $2\times 3 = 6$, $2\times 2 = 4$, $1.6\times 1.6 = 2.5$, etc.).

Usable Transistors/cm² (High-performance ASIC, Auto Layout)—Number of transistors per cm² designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os – Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os – Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package cost (cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

Chip Frequency (MHz)

On-chip, local clock, high-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

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On-chip, across-chip clock—On-chip clock frequency of microprocessors and ASICs for interconnect signals that run across the full width of the chip (Typically, this is lower than the localized clock performance due to capacitance loading of the long cross-chip interconnect.).

Chip-to-board (off-chip) speed (high-performance, reduced-width, multiplexed bus)—Maximum signal I/O frequency to specialized board reduced-width, multiplexed buses.

Chip-to-board (off-chip) speed (high-performance, peripheral buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

Other Attributes

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. **The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.**

Maximum Number Of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration Technology Working Group, are based on the first 20K wafer-starts-per-month manufacturing facility, versus the first-pilot-line timing target of the 1997 NTRS.

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ELECTRICAL DESIGN AND TEST METRICS

Power Supply Voltage (V)

Minimum Logic V_{dd} —Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power

High-performance with heat sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin (\$K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

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International Technology Roadmap for Semiconductors 2000 Update

Process Integration, Devices, and Structures

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PROCESS INTEGRATION, DEVICES, & STRUCTURES

SUMMARY

Since the publication of the 1999 ITRS, it has become clear that some of the forecast trends were too conservative. In particular, both the MPU transistor gate length scaling and the technology node timing keyed mainly to the DRAM half pitch are proceeding faster than predicted. Also, the ASIC gate length scaling is no longer trailing the MPU scaling. In response, the PIDS TWG has accelerated the scaling of MPU transistor gate length and associated specifications in the 2000 Roadmap update and has set the ASIC gate length equal to the MPU gate length at all nodes. The changes are in Table 28a, Memory and Logic Technology Requirements—Near Term. In the table, for each year through 2001, the MPU gate length is moved forward by one year in the 2000 update compared to the 1999 ITRS, but the gate lengths are left unchanged from 2002 on. Other key specifications such as equivalent T_{ox} , V_{dd} , maximum I_{off} , etc., are also moved forward by one year, following the gate length. The acceleration is halted with the year 2002 because the TWG is concerned about the “red brick wall” in equivalent T_{ox} that appears in 2005 in the 1999 ITRS. The equivalent T_{ox} is small enough in 2005 to perhaps require high K material for the gate dielectric to keep the gate leakage within acceptable limits, but the industry has no solution in hand. Furthermore, prospects of such a solution by 2005 are highly uncertain. Moving the gate length and thus the equivalent T_{ox} forward by one year for the 2002 node and beyond could result in requiring high K gate dielectric earlier than 2005, which the TWG found unrealistic. The issue of accelerating the gate length and other parameters for 2002 and beyond requires careful analysis of scaling issues.

Other changes are relatively minor, to correct minor errors, update several values in the tables, and clarify explanations in the notes. In Table 28, the changes include an improved definition of the gate delay metric in Rows 9 and 13, making the S/D extension junction depth values and colors in Row 16 the same as those in the Front End Processing Table 34, and recognition of special difficulty, starting in 2002, in meeting the gate leakage requirements for low power transistors (see Note 11). In Table 29, many of the values have been updated.

Currently, there is not a consensus amongst the TWGs and the IRC on the acceleration in scaling trends for DRAM half pitch and MPU/ASIC gate length, especially in 2002 and beyond. It is vitally important to come to consensus early in 2001 regarding the appropriate scaling trend to use. A major challenge for the PIDS TWG will be to then analyze in detail the resulting impact on device and DRAM scaling and characteristics, including especially the accelerated development and integration of high K gate dielectric. Another key challenge will be to work with the FEP TWG to add flash and FERAM characteristics to the tables, and to expand the logic low power requirements. Other key challenges will be to work with the Design TWG to resolve linked device, circuit, and system issues, such as the impact of gate leakage on logic circuitry, the impact of V_{dd} and I_{off} specifications on circuit and system power, etc. Finally, updating and improving the novel devices table will be a major focus.

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2000 UPDATE TABLES

MEMORY AND LOGIC

Table 28a Memory and Logic Technology Requirements—Near Term**

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
1	DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	
2	MPU/ASIC Physical Gate Length	120	100	90	85-90	80	70	65	
3	MPU / ASIC ½pitch (nm)	230	210	180	160	145	130	115	
4									
5	Minimum logic V _{dd} (V) (desktop)	1.5–1.8	1.2–1.5	1.2–1.5	1.2–1.5	1.2–1.5	0.9–1.2	0.9–1.2	
6	T _{ox} equivalent (nm)	1.9–2.5	1.5–1.9	1.5–1.9	1.5–1.9	1.5–1.9	1.2–1.5	1.0–1.5	M GATE
7	Nominal I _{on} at 25 °C (µA/µm) [NMOS/PMOS] high-performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	M GATE
8	Maximum I _{off} at 25 °C (nA/µm) (For minimum L device) high performance	7	8	10	10	13	16	20	M GATE
9	Gate delay metric CV/I (ps) high- performance	12.5	11.4	10.3	9.7	9.1	8.1	7.5	
10	Percent static power reduction necessary due to innovative circuit/system design	0	48	55	55	71	77	81	M GATE M & A ½
11	Nominal I _{on} at 25 °C (µA/µm) [NMOS/PMOS] low power	490/230	490/230	490/230	490/230	490/230	490/230	490/230	A GATE
12	Maximum I _{off} at 25 °C (pA/µm) (For minimum L device) low power	7	8	10	10	13	16	20	A GATE
13	Gate delay metric CV/I (ps) low power	20.9	17.6	15.9	15.0	14.1	12.9	11.6	
14	Percent static power reduction necessary due to innovative circuit/system design	0	55	65	65	80	85	88	A GATE M & A ½
15	V _t 3σ variation (±mV) (for nominal L _g device)	50	42	42	42	42	33	33	M GATE
16	S/D extension junction depth, nominal (nm)	36–60	30–50	25–43	25–43	24–40	20–35	20–33	M GATE

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2000 UPDATE										
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YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 28a Memory and Logic Technology Requirements—Near Term (continued)**

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
1	DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	
2	MPU/ASIC Physical Gate Length	120	100	90	85-90	80	70	65	
3	MPU / ASIC ½pitch (nm)	230	210	180	160	145	130	115	
17	Gate sheet resistance (Ω/sq) at minimum dimension	4-6	4-6	4-6	4-6	4-6	4-6	4-6	M Gate
18	Interconnect levels	6-7	6-7	7	7-8	8	8	8-9	M & A ½
19	Short wire <i>minimum</i> pitch (nm)	360-460	330-420	300-360	260-320	240-290	220-260	200-230	M & A ½, <i>D ½</i>
20	Maximum wire length <i>for local levels</i> , Lm (μm)	2243	2036	1828	1621	1468	1315	1162	M & A ½
21	DRAM cell size (μm^2)	0.26	0.22	0.18	0.10	0.08	0.065	0.044	D ½
22	DRAM cell dielectric T_{ox} equivalent (nm)	3	2.40	1.80	0.95	0.80	0.65	0.45	
23	DRAM retention time (ms)	250	250	250	250	250	250	250-500	
24	DRAM soft error rate (fits)	1000	1000	1000	1000	1000	1000	1000	
25	Nonvolatile data retention (Years)	10	10	10	10	10	10	10	
26	NOR cell size (μm^2)	0.34	0.29	0.24	0.17	0.15	0.13	0.1	M & A ½
27	+/- V_{pp} (V)	8-10	8-10	8-9.5	8-9.5	8-9.5	7-9	7-9	
28	Tunnel oxide (nm)	8-10	8-10	8-9.5	8-9.5	8-9.5	8-9	8-9	
29	NVM endurance (erase/write cycles)	100K	100K	100K	100K	100K	100K	100K	
30	ESD protection voltage (V/ μm)	7.5	7.5	10.5	10.5	10.5	12	12	
31	(V/ μm^2)	2.5	2.5	3.0	3.0	3.0	3.5-4.0	3.5-4.0	

Solutions Exist ☐Solutions Being Pursued ☐No Known Solutions ☐

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Table 28b Memory and Logic Technology Requirements—Long Term**

	Year Technology Node	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
[1]	DRAM ½ Pitch (nm)	70	50	35	
[2]	MPU Gate Length (nm)	45	32	22	
[3]	MPU / ASIC ½ Pitch (nm)	80	55	40	
[4]	ASIC Gate Length (nm)	70	50	35	
[5]	Minimum logic V _{dd} (V) (desktop)	0.6–0.9	0.5–0.6	0.3–0.6	M Gate
[6]	T _{ox} equivalent (nm)	0.8–1.2	0.6–0.8	0.5–0.6	M Gate
[7]	Nominal I _{on} at 25 °C (µA/µm) [NMOS/PMOS] high performance	750/350	750/350	750/350	M Gate
[8]	Maximum I _{off} at 25 °C (nA/µm) (For minimum L device) high-performance	40	80	160	M Gate
[9]	Gate delay metric CV/I (ps) high-performance	4.9	3.4	3.0	
[10]	Percent static power reduction necessary due to innovative circuit/system design	91	97	98	M Gate M & A ½
[11]	Nominal I _{on} at 25 °C (µA/µm) [NMOS/PMOS] low power	490/230	490/230	490/230	A Gate
[12]	Maximum I _{off} at 25 °C (pA/µm) (For minimum L device) low power	40	80	160	A Gate
[13]	Gate delay metric CV/I (ps) low power	7.4	5.7	2.8	
[14]	Percent static power reduction necessary due to innovative circuit/system design	95	98	99	A Gate M & A ½
[15]	V _T 3σ variation (±mV) (for nominal L _g device)	25	17	17	M Gate
[16]	S/D extension junction depth, nominal (nm)	16-26	11-19	8-13	
[17]	Gate sheet resistance (Ω/sq) at minimum dimension	4–6	4–6	4–6	M Gate

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Table 28b Memory and Logic Technology Requirements—Long Term (continued)**

	Year Technology Node	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
[1]	DRAM ½ Pitch (nm)	70	50	35	
[2]	MPU Gate Length (nm)	45	32	22	
[3]	MPU / ASIC ½ Pitch (nm)	80	55	40	
[4]	ASIC Gate Length (nm)	70	50	35	
[18]	Interconnect levels	9	9–10	10	M & A ½
[19]	Short wire <i>minimum</i> pitch (µm)	140-160	100-110	70-80	M & A ½, D ½
[20]	Maximum wire length <i>for local levels</i> , Lm (µm)	697	325	201	M & A ½
[21]	DRAM cell size (µm²)	0.018	0.0075	0.0031	D ½
[22]	Cell dielectric T _{ox} equivalent (nm)	0.15	0.06	0.043	
[23]	DRAM retention time (ms)	250–500	250–500	250–500	
[24]	Soft error rate (fits)	1000	1000	1000	
[25]	Nonvolatile data retention (Years)	10	10	0.1–10	
[26]	NOR cell size (µm²)	0.05	0.025	0.012	M & A ½
[27]	+/- V _{pp} (V)	7–8.5	6.5–8.5		
[28]	Tunnel oxide (nm)	7.5–8.5	2–8	2–7	
[29]	NVM endurance (erase/write cycles)	100K	0.1–1M	0.1–10M	
[30]	ESD protection voltage (V/µm)	13.5	15	17.5	
[31]	(V/µm²)	4.5–5.0	5.5–6.0	7.5–10	

Solutions Exist ☐Solutions Being Pursued ☐No Known Solutions ☐

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(PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)										

Notes for Table 28a and b Memory and Logic Requirements

General Notes:

[A] The power supply voltage control is $\pm 10\%$.

[B] Control of L_{gate} is $\pm 10\%$ and $\pm 20\%$ for L_{eff}

[C] The total series resistance of the S/D is expected to be $< 10\%$ of the channel "ON" resistance, $R_{on} = V_{dd}/I_{on}D$. Flash products will not make use of a technology node at the time it is introduced for microprocessor or DRAM usage.

Explanatory Notes for each row of Table 28a and b:

[1] These DRAM half pitch numbers are unchanged from the 1999 ITRS. However, developments since the publication of the 1999 ITRS strongly suggest that the scaling trend here is too conservative. A proposal has been made to accelerate this trend (see ORTC tables), and this proposal will be carefully evaluated and its impact analyzed in preparing the 2001 ITRS.

[2] This is the final, as-etched length at the bottom of the gate electrode. These numbers have been changed from those in the 1999 ITRS because developments since the publication of that document strongly suggest that scaling is proceeding faster than expected. Furthermore, the ASIC gate length scaling no longer trails the MPU scaling, so the ASIC gate length has been set equal to the MPU gate length. In this updated table, for each year through 2001 the gate length value is moved to the left by one year (i.e., one year earlier) compared to the 1999 ITRS, but the gate length values are left unchanged from 2002 on. Other key specifications such as equivalent T_{ox} , V_{dd} , maximum I_{off} , nominal I_{on} , etc., are linked to the gate length, and hence are also moved to the left by one year through 2001 and left unchanged for 2002 and beyond.

The accelerated scaling is not extended beyond 2001 mainly because of concerns about the equivalent T_{ox} specification. In the 1999 ITRS, the equivalent T_{ox} is small enough in 2005 to perhaps require high K material for the gate dielectric in order to keep the gate leakage within acceptable limits. However, the industry has no solution in hand for such a high K gate dielectric, and prospects of implementing such a solution in production by 2005 are highly uncertain. Accelerated scaling of the gate length and thus the equivalent T_{ox} for 2002 and beyond could result in requiring high K gate dielectric earlier than 2005, which is unrealistic. There are proposals (see the ORTC tables) for accelerated scaling of the gate length in 2002 and beyond, and these will be evaluated in preparing the 2001 ITRS. Such accelerated scaling will require re-evaluation of the equivalent T_{ox} scaling and resolution of difficult overall transistor scaling, CD control, and other issues

[3] From ORTC table

[4] Row 4 was for the ASIC Gate Length in the 1999 ITRS. However, as explained in Note 2 above, the ASIC gate length scaling has matched the MPU gate length scaling, so ASIC gate length has been set equal to the MPU gate length in the 2000 update. Hence, for the 2000 ITRS, Row 2 covers both MPU and ASIC gate length, and Row 4 is unnecessary.

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE											
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm	
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]	

- [5] Power supply voltage is based on controlling the active power dissipation (see linked spreadsheet) and keeping the field in the gate dielectric at reasonable levels per reliability concerns. Generally, the higher values in the range will be used for high-performance applications, while the lower values in the range will be used for low-power applications.
- [6] This is the equivalent effective physical SiO_2 thickness. (Note that the electrically determined oxide thickness from C-V measurements would be larger than the thickness in this line because of polysilicon depletion and quantum effects.) *The values here are the same as those in Table 34 in the Front End Processes chapter.* Generally, as with V_{dd} , the higher values in the range will be used for high-performance applications, while the lower values in the range will be used for low-power applications. For the 180 through the 110 nm nodes, the range of equivalent T_{ox} is chosen to keep $V_{dd}/T_{ox} \leq 8 \text{ MV/cm}$ because of oxide reliability concerns, where V_{dd}/T_{ox} is a metric for the electric field in the oxide. At the 100 nm technology node, there is a distinct likelihood that high κ materials other than SiO_2 or oxynitride will be used for the gate dielectric. For such materials, the gate leakage current is much smaller than for oxide dielectric with the same equivalent T_{ox} , allowing smaller T_{ox} and hence higher I_{on} for the high κ case. Also, the $V_{dd}/T_{ox} \leq 8 \text{ MV/cm}$ requirement may not hold for the high κ materials, and hence from a reliability point of view, T_{ox} can be scaled further for these materials. Thus, at the 100 nm node, the wide range of 1.0–1.5 nm for equivalent T_{ox} comprehends the uncertainty of what dielectric material will be used, with the high end of the range appropriate for SiO_2 or oxynitride and the very bottom end of the range appropriate for high κ materials. Beyond the 100 node, the use of high κ material for the gate dielectric becomes much more likely, and the $V_{dd}/T_{ox} \leq 8 \text{ MV/cm}$ requirement is no longer followed.
- [7] The device I_{on} value is expected to remain relatively constant for succeeding technology generations. *The white, yellow, and red coloring here follows that of T_{ox} in Line 6.*
- [8] The device I_{off} value is projected to increase with successive technology generations to maintain I_{on} constant per Line 7. I_{off} is measured with $V_s = V_g = V_{\text{substrate}} = 0$ and $V_d = V_{dd}$. I_{off} is the difference between the drain current and the gate (leakage) current (I_{off} is the sum of the subthreshold current [the current in the source lead] and the junction leakage current [the current in the substrate lead]). The requirements on the gate leakage current are listed in the Front End Processes (FEP) chapter in Table 34. *This row is colored white throughout because through adjustment of the threshold voltage implant (and perhaps use of other techniques such as optimized halo implants), meeting the I_{off} specification should be achievable. What will be difficult is to simultaneously meet the I_{off} requirement and other key device requirements, especially for I_{on} , at the later technology nodes. The coloring of Row 7 captures this difficulty for I_{on} .*
- [9] *The gate delay metric for high-performance devices is calculated using the approach in Taur and Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998, pp. 228 - 230. We assume a CMOS inverter with $W_p = (I_{on,n}/I_{on,p}) * W_n = (750/350) * W_n$, where W_n and W_p are the widths of, respectively, the NMOS and PMOS transistors, and the inverter is driven by an ideal square wave at its input. Also, the inverter's load is an identical inverter. Under those circumstances, the CV/I gate delay metric equals the switching delay, τ , in Taur and Ning, where $\tau = (\tau_n + \tau_p)/2$, and τ_n and τ_p are defined, respectively, in Equations 5.3 and 5.4 in Taur and Ning. The highest values of V_{dd} from Row 5 are used in this analysis, along with the largest T_{ox} equivalent values from Row 6. It is assumed that the channel width scales with the channel length. The MPU gate length is used for L . Since the gate delay metric is only a calculated number using transistor characteristics such as T_{ox} , V_{dd} , etc., the coloring here is white.*

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All modifications of the items and/or numerals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

- [10] For each technology node, maximum system-imposed limits for total chip leakage current, $I_{L,SYS}$, were estimated by assuming a static power dissipation limit of 10% of the maximum heat-sink limit, and dividing this static power dissipation by V_{dd} . Given the projected device I_{off} value from Line 8, the total projected static leakage current for the chip was calculated based on the total number of transistors and an assumed W/L ratio of 3. This projected chip static leakage current was increased by a factor of 100 to account for the leakage current increase due to device self heating ($T=100^{\circ}\text{C}$). If this projected $T=100^{\circ}\text{C}$ chip static leakage current value is greater than $I_{L,SYS}$, then the excess percentage of static power dissipation is listed in Line 9. This excess must be eliminated through innovative circuit or system design techniques such as using dynamic or multi- V_t techniques to reduce the effective I_{off} of the chip or by turning off sections of the chip temporarily. System values of the heat-sink dissipation limit, the power-supply voltage, chip size and transistor density were obtained from the ORTC tables.
- [11] For successive technology generations, the device I_{on} value is expected to remain relatively constant. The low-power device performance is a calculated percentage of the high-performance I_{on} value; this calculated value takes into account the loss in current drive due to the higher required threshold voltage necessary in order to satisfy more stringent I_{off} requirements. *The color is yellow at the 130 nm node (2002) because of difficulty in meeting the gate leakage specification of $\leq 10 \text{ pA}/\mu\text{m}$ at 100°C , and the color is red for 2004 and beyond because of the greater difficulty of meeting the gate leakage specifications with the increasingly thin equivalent T_{ox} values at those nodes.*
- [12] The device I_{off} value is set to three orders of magnitude less than the I_{off} for the high-performance chips (Line 8), and is similarly projected to increase with succeeding technology generations. I_{off} is the difference between the drain current and the gate (leakage) current (I_{off} is the sum of the subthreshold current [the current in the source lead] and the junction leakage current [the current in the substrate lead]). The requirements on the gate leakage current are listed in the Front End Processes chapter in Table 34.
- [13] *The gate delay metric for the low-power devices is calculated using the approach in Yuan and Taur, similarly to calculating the gate delay metric for high-performance devices (see Note 9 above). The only difference from the high-performance case is that the smallest values of V_{dd} from Row 5 and the smallest T_{ox} equivalent values from Row 6 are used in the analysis, and the I_{on} values are those for low-power devices.*
- [14] For each technology node, maximum system-imposed limits for total chip leakage current, $I_{L,SYS}$, were estimated by assuming a static power dissipation limit of 10% of the maximum chip power dissipation, and dividing this static power dissipation by V_{dd} . A reasonable value for the maximum dissipation for high density, battery-operated chips is $100 \mu\text{W}$, in order to preserve battery life. Given the projected device I_{off} value from Line 11, the total projected static leakage current for the chip was calculated based on the total number of transistors and an assumed W/L ratio of 3. If this projected chip static leakage current value is greater than $I_{L,SYS}$, then the excess percentage of static power dissipation is listed in Line 12. This excess must be eliminated through innovative circuit or system design techniques such as using dynamic or multi- V_t techniques to reduce the effective I_{off} of the chip or by turning off sections of the chip temporarily.

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2000 UPDATE											
YEAR OF PRODUCTION TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm	
(1999 ITRS)											
YEAR OF PRODUCTION TECHNOLOGY NODE	1999 180 nm	2000	2001	2002	2003	2004	2005	2008	2011	2014	
(PROPOSED NODE YEARS ARE NOW 2007/65nm; 2010/45nm; 2013/33nm; 2016/23nm) (SC. 2.0)			130 nm			90nm		[60 nm]	[40 nm]	[30 nm]	

- [15] The V_t 3-sigma variation was scaled proportionately with the reduction in the midrange power supply voltage. *The V_t 3-sigma variation here is the total statistical variation in V_t , including the effects of statistical variation in T_{ox} , L_g , implant dose and energy, etc.*
- [16] A range of junction depths can be used depending on the drain and channel engineering used (such as pocket implants versus shallow drain extensions). *The values and the white, yellow, and red coloring here are the same as those in Table 34 in the Front End Processes chapter.*
- [17] Difficult to obtain gate sheet resistance targets with silicide at 70 nm and beyond.
- [18] The number of interconnect levels is driven by high-performance microprocessor.
- [19] The short wire pitch is equal to two times the half pitch.
- [20] For the metal layers with the smallest pitch, this is the calculated value of the maximum wire length for the propagation delay to be $0.9 \cdot f_{\max, \text{local}}$ where $f_{\max, \text{local}}$ is the maximum local frequency from the ORTC tables. The gates are three-input NAND gates, with a W_n/L ratio of 5. (The formula used in calculating the delay as a function of maximum wire length is in P.D. Fisher, et al.⁶) Also refer to the linked spreadsheet.
- [21] The cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Processes chapter Table 34b. The capacity and chip size numbers used by FEP are from the Overall Roadmap Technology Characteristics (ORTC) Tables 1a and 1b, and reflect the "generation at introduction" option. (This is for the DRAM chip that is just being introduced and sampled, having the highest DRAM capacity and most aggressive but still quite large chip size. Note that the "Generation at production" option in the ORTC tables has one quarter the DRAM capacity of the generation at introduction option, and correspondingly smaller chip size that allows the chip price to be affordable.) Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled very aggressively. The difficulty will lie in reducing the value of the cell size factor, a , where $a = \text{cell size}/F^2$ and F is the DRAM half pitch. The required values for a are 8 for the 180 nm node, 6 for the 130 nm node, and 4.4 for the 100 nm node. $a = 8$ is probably achievable with current techniques, but $a = 6$ will require innovative solutions, as indicated by the yellow coloring of the 130 nm node for this line, while $a = 4.4$ has no known solution, as indicated by the red coloring of the 100 nm node and beyond.

⁶ P. D. Fisher, et al., "The Test of Time," *IEEE Circuits and Devices Magazine*, vol. 14, pp. 37–44 (March 1998).

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

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2000 UPDATE

YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

- [22] Cell dielectric T_{ox} equivalent thickness is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Processes chapter, Table 34b. The capacity and chip size numbers used by FEP are from the Overall Roadmap Technology Characteristics (ORTC) Tables 1a and 1b, and reflect the "generation at introduction" option. (This is for the DRAM chip that is just being introduced and sampled, having the highest DRAM capacity and most aggressive but still quite large chip size. Note that the "generation at production" option in the ORTC tables has one quarter the DRAM capacity of the Generation at introduction option, and correspondingly smaller chip size that allows the chip price to be affordable.) Since the FEP DRAM capacity and chip size numbers are quite aggressive, the equivalent T_{ox} must also be scaled very aggressively. For the 180 nm–150 nm nodes, the dielectric is based on ONO/Ta_2O_5 . For the 130 nm node and beyond, breakthroughs are needed to utilize MIM structures and eventually BST, while for the 70 nm node and beyond, there are no known solutions. The actual T_{ox} equivalent requirement for each node depends on factors such as area enhancement (by height and 3D structures), film leakage, and contact formation. Trench capacitors may have different requirements for the cell dielectric material, but the trends should be valid.
- [23] Retention time is the minimum time without refreshing a row that the data from memory is still sensed correctly at 85°C. This is the measure of the combined interaction of device leakage, signal strength, and the sense amplifier circuit's sensitivity. This requirement can vary with operating frequency and temperature, and also depending on the application specifics.
- [24] Soft error: This is a typical FIT rate and can vary with cycle time and other quality/reliability testing conditions.
- [25] Retention requirements will remain at ten years in the near term, but future alternative technologies will exploit retention-endurance tradeoffs.
- [26] The need for high electric fields will complicate scaling and eventually force use of alternative NVM technology.
- [27] The meaning of V_{pp} has become uncertain because it is no longer an external supply. In this table it is intended to indicate the highest voltage relative to ground seen in the cell array.
- [28] Tunnel oxides must be thin enough to allow ease of program/erase, but thick enough to assure retention. Scaling difficulties will force consideration of alternative cell structures.
- [29] Endurance of 100K cycles is a minimum need, and in emerging nodes the possibility of higher endurance and lower retention will be explored.
- [30] ESD $V/\mu m$ in terms of NMOS capability per micron width, **based on the Human Body Model**. Particularly critical in NMOS ESD circuits and self-protected circuits.
- [31] ESD $V/\mu m^2$ in terms of protection circuit effectiveness per unit area of the protection circuit including guard ring, **based on the Human Body Model**.

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

ANALOG, MIXED-SIGNAL, AND RF

Table 29a Analog, Mixed-signal, and RF Technology Requirements—Near Term**

[1]	YEAR TECHNOLOGY NODE		1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
	DRAM ½ Pitch (nm)		180	165	150	130	120	110	100	D
	MPU Gate Length (nm)		140	120	100	85	80	70	65	M Gate
	MPU/ASIC ½ Pitch (nm)		230	210	180	160	145	130	115	M & A
	ASIC Gate Length (nm)		180	165	150	130	120	110	100	A Gate
[2]	Minimum Digital Supply Voltage (V)		1.8–1.5		1.5–1.2			1.2–0.9		M Gate
[3]	Minimum Analog Supply Voltage (V)		3.3–2.5	3.3–1.8			2.5–1.8			
[4]	RF Frequency (GHz)		0.9–2.5	0.9–10						
[5]	Analog Frequency (GHz)		<0.1	0.1–5						
[6]	RF Transistor	Current (µA)	100	100	100	100	75	75	75	M Gate
[7]		f _{max} (GHz)	25	28	32	35	40	45	50	
[8]		f _t (GHz)	20	20	25	30	30	35	40	
[9]		Noise figure (dB)	1.5	1.5	1.5	1.5	1.2	1.2	1.2	
[10]		1/f Noise (V ² -µm ²)	1 × 10 ⁻¹¹	1 × 10 ⁻¹¹	1 × 10 ⁻¹¹	5 × 10 ⁻¹²	5 × 10 ⁻¹²	5 × 10 ⁻¹²	1 × 10 ⁻¹⁰	
[11]	Analog	Current (µA)	75	70	65	60	55	50	50	
[12]		1/f Noise (V ² -µm ²)	1 × 10 ⁻¹¹	1 × 10 ⁻¹¹	1 × 10 ⁻¹¹	5 × 10 ⁻¹²	5 × 10 ⁻¹²	5 × 10 ⁻¹²	2 × 10 ⁻¹⁰	
[13]		Gate oxide leakage (A/cm ²)	—	—	—	—	—	—	1 × 10 ⁻¹⁰	
[14]		Current matching (Δ% ±3σ)	≤1	≤1	≤1	≤1	≤1	≤1	≤1	
[15]	RF Coupling	Density (fF/µm ²)	1	1.2	1.4	1.5	1.7	1.9	2	
[16]		Q	≥15	≥18	≥22	≥25	≥27	≥29	≥30	
[17]	Filter	Density (fF/µm ²)	2.5	2.8	3.2	3.5	3.7	3.8	4	
[18]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	
[19]	RF Bypass	Density (fF/µm ²)	5	6	7	7.5	8	9	10	
[20]		Linearity (ppm/V)	≤1000	≤1000	≤1000	≤1000	≤1000	≤1000	≤1000	
[21]		Q	≥15	≥18	≥22	≥25	≥27	≥29	≥30	

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 29a Analog, Mixed-signal, and RF Technology Requirements—Near Term (continued)**

[1]	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	DRIVER
	DRAM ½ Pitch (nm)	180	165	150	130	120	110	100	D
	MPU Gate Length (nm)	140	120	100	85	80	70	65	M Gate
	MPU/ASIC ½ Pitch (nm)	230	210	180	160	145	130	115	M & A
	ASIC Gate Length (nm)	180	165	150	130	120	110	100	A Gate
[22]	Analog Density (fF/μm ²)	1	1	1	1.5	1.5	1.5	2	
[23]	Linearity (ppm/V)	≤100	≤100	≤100	≤100	≤100	≤100	≤100	
[24]	Leakage (pA/pF-V)	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	≤0.001	
[25]	Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	≤0.1	
[26]	RF Resonator Q	<50	<50	<50	50–1000				
[27]	Analog Matching (Δ% ±3σ)	≤1	≤1	≤1	≤0.1	≤0.1	≤0.1	≤0.1	
[28]	1/f Noise (A ² -μm ²)	1 × 10 ⁻¹⁸	1 × 10 ⁻¹⁸	1 × 10 ⁻¹⁸	1 × 10 ⁻¹⁸	1 × 10 ⁻¹⁸	1 × 10 ⁻¹⁸	1 × 10 ⁻¹⁸	
[29]	TC (ppm/°C)	≤100	≤100	≤100	≤10	≤10	≤10	≤10	
[30]	Inductor Q	≥15	≥15	≥25	≥25	≥25	≥25	≥30	
[31]	Signal Isolation S ₂₁ (dB)	≤-100	≤-100	≤-100	≤-100	≤-100	≤-100	≤-120	
[32]	Benchmark Gain (dB)	≥20	≥20	≥20	≥20	≥20	≥20	≥20	
[33]	IIP3 (dBm)	-4	-4	-4	-3	-3	-3	-2.5	
[34]	Noise figure (dB)	1.5	1.5	1.5	1.3	1.3	1.3	1.2	
[35]	Noise (dB)	4	4	4	3.5	3.5	3.5	3	
[36]	Resolution (Bits)	8–14			8–14				

Solutions Exist ☐Solutions Being Pursued ☐No Known Solutions ☐

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numerals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.

2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 29b Analog, Mixed-signal, and RF Technology Requirements—Long Term**

[1]	YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
	DRAM ½ Pitch (nm)	70	50	35	D
	MPU Gate Length (nm)	45	32	22	M Gate
	MPU / ASIC ½ Pitch (nm)	80	55	40	M & A
	ASIC Gate Length (nm)	70	50	35	A Gate
[2]	Minimum Digital Supply Voltage (V)	0.9–0.6	0.6–0.5	0.5–0.3	M Gate
[3]	Minimum Analog Supply Voltage (V)	1.8–1.5		1.5	
[4]	RF Frequency (GHz)	0.9–10	0.9–100		
[5]	Analog Frequency (GHz)	0.1–5	0.1–10		
[6]	RF Transistor Current (μA)	50	50	50	M Gate
[7]	f _{max} (GHz)	60	150	175	
[8]	f _t (GHz)	50	120	140	
[9]	Noise figure (dB)	≤1	≤1	≤1	
[10]	1/f Noise (V ² -μm ²)	5 × 10 ⁻¹¹	2 × 10 ⁻¹¹	1 × 10 ⁻¹¹	
[11]	Analog Current (μA)	40	30	20	
[12]	1/f Noise (V ² -μm ²)	1 × 10 ⁻¹⁰	1 × 10 ⁻¹⁰	5 × 10 ⁻¹¹	
[13]	Gate oxide leakage (A/cm ²)	1 × 10 ⁻⁰⁸	1 × 10 ⁻⁰⁸	1 × 10 ⁻⁰⁵	
[14]	Current matching (Δ% ±3σ)	≤1	≤1	≤1	
[15]	RF Coupling Density (fF/μm ²)	3	4	6	
[16]	Q	≥35	≥40	≥40	
[17]	Filter Density (fF/μm ²)	5	7	10	
[18]	Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	
[19]	RF Bypass Density (fF/μm ²)	15	20	30	
[20]	Linearity (ppm/V)	≤1000	≤1000	≤1000	
[21]	Q	≥35	≥40	≥40	

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2000 UPDATE										
YEAR OF PRODUCTION TECHNOLOGY NODE (1999 ITRS)	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm
YEAR OF PRODUCTION TECHNOLOGY NODE (PROPOSED NODE YEARS ARE NOW 2007/65NM; 2010/45NM; 2013/33NM; 2016/23NM) (SC. 2.0)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90nm	2005	2008 [60 NM]	2011 [40 NM]	2014 [30 NM]

Table 29b Analog, Mixed-signal, and RF Technology Requirements—Long Term (continued)**

[1]	YEAR TECHNOLOGY NODE		2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
	DRAM ½ Pitch (nm)		70	50	35	D
	MPU Gate Length (nm)		45	32	22	M Gate
	MPU / ASIC ½ Pitch (nm)		80	55	40	M & A
	ASIC Gate Length (nm)		70	50	35	A Gate
[22]	Analog	Density (fF/μm ²)	3	4	6	
[23]		Linearity (ppm/V)	≤100	≤50	≤50	
[24]		Leakage (pA/pF-V)	≤0.001	≤0.001	≤0.001	
[25]		Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.1	
[26]	RF	Q	50–1000		≥1000	
[27]	Analog	Matching (Δ% ±3σ)	≤0.1	≤0.1	≤0.01	
[28]		1/f noise (A ² -μm ²)	1 × 10 ⁻¹⁸	1 × 10 ⁻¹⁸	1 × 10 ⁻¹⁸	
[29]		TC (ppm/°C)	≤10	≤10	≤1	
[30]	Inductor	Q	≥50	≥75	≥75	
[31]	Signal Isolation	S ₂₁ (dB)	≤-120	≤-120	≤-120	
[32]	Benchmark	Gain (dB)	≥20	≥20	≥20	
[33]		IIP3 (dBm)	-1.5	-1	-1	
[34]		Noise figure (dB)	1.0	1.0	1.0	
[35]		Noise (dB)	2.5	2	2	
[36]		Resolution (Bits)	8–14		≥24	

Solutions Exist Solutions Being Pursued No Known Solutions

Notes for Table 29a and b Analog, Mixed-signal, and RF Requirements

Explanatory Notes for each row of Tables 29

[1] Year of first digital product for a given technology generation. Lithographic drivers for key technologies at each node are indicated. Year of first analog, RF, and mixed-signal product at the same technology may lag by one generation.

[2] Digital (logic V_{dd}) supply voltage, driven by MPU gate length (M Gate), is repeated here for reference.

[3] Analog supply voltage is expected to lag digital by two or more generations. Additional voltage headroom is needed to avoid excessive power dissipation under reduced signal swing conditions. Analog CMOS designs may use thick gate oxide and low V_t techniques. The analog power supply reduction trend may lag digital backward compatibility trend for I/O such that a common thick gate oxide solution is not feasible.

[4] RF applications will focus on the 0.9–2.5 GHz, 5–6 GHz, 17–20 GHz, 40–45 GHz, and 60–65 GHz frequency spectrums. Design of applications at the lower frequencies will continue throughout the duration of the roadmap (lower frequency bands are not “obsoleted” and will continue to be used). Higher frequency bands will drive performance requirements.

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- [5] General purpose analog frequency (such as DSP, audio/video, ADC) trend is in parallel with RF. Very clean, jitter-free, clock frequency generation is required. Transistors: It is expected that speed $\times$ power characteristics favor use of bipolar for $W_e < 180$ nm. MOS speed $\times$ power may be favorable relative to bipolar at $L_{eff} > 180$ nm. Bipolar device assumed through 110 nm (see Potential Solutions Figure 14) followed by MOS device.
- [6] Absolute current (independent of device geometry) at which these key RF transistor parameters are measured.
- [7] Assumes a "rule of thumb" of approximately $10\times$ the transmit/receive frequency.
- [8] Assumes that f_t generally follows the progression of f_{max} .
- [9] Measured at the specified current (Row 5) and at the application transmit/receive frequency (Row 4).
- [10] Bipolar device assumed **up to and including the 110 nm node** (see Potential Solutions Figure 14) followed by MOS device. Assume SPICE model for MOS device: $SVG = Kf / (C_{ox}^2 \times W \times L \times f)$. Values scaled assuming t_{ox}^2 relationship. $1/f$ spectral density is normalized to active device area = $1 \mu m^2$, frequency = 1Hz. RF MOS device assumed to be realized with the thinnest gate oxide and shortest L_{eff} available at a given node. For this reason, the minimum MPU gate length (M Gate) is indicated as a driver for this device. Although the effects are acute at baseband, $1/f$ noise can be "mixed up" to RF if present in RF devices. The effect is prominent in MOS devices due to carrier recombination in traps at the insulator-semiconductor interface (surface effect).
- [11] Absolute current (independent of device geometry) at which these key analog transistor parameters are measured.
- [12] Bipolar device assumed **upto and including the 110 nm node** (see Potential Solutions Figure 14) followed by MOS device. Assume SPICE model for MOS device: $SVG = Kf / (C_{ox}^2 \times W \times L \times f)$. Values scaled assuming t_{ox}^2 relationship. $1/f$ spectral density is normalized to active device area = $1 \mu m^2$, frequency = 1Hz. Analog MOS device assumed to use the thicker or analog gate oxide available at a given node. The effect is prominent in MOS devices due to carrier recombination in traps at the insulator-semiconductor interface (surface effect). Vertical devices (bipolar) or sub-surface devices (JFETs) are superior in this regard.
- [13] Bipolar device assumed **up to and including the 110 nm node** (see Potential Solutions Figure 14) followed by MOS device. Hence, gate oxide leakage has no meaning until the 110 nm node (2004), and the boxes for the previous nodes are left with just a dash in them. For CMOS, analog power supply constrains minimum gate oxide thickness (and therefore leakage). $T_{ox} = 4$ nm (100 nm node); $T_{ox} = 3.5$ nm (70–50 nm nodes); $T_{ox} = 3$ nm (35 nm node).
- [14] Matching specification assumes "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity are required.
- [14] Bipolar device assumed **up to and including the 110 nm node** (see Potential Solutions Figure 14) followed by MOS device. Matching specification assumes "near neighbor" devices at minimum practical separation. Careful layout and photolithographic uniformity are required. Bipolar values specified for an emitter area of $20 \mu m^2$, CMOS values specified at a gate overdrive, $V_{gs} - V_{th}$, of 200mV and an area of $250 \mu m^2$.

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- [15] RF coupling capacitors are not expected to drive density. Linearity is not driven by this capacitor.
- [16] Q is the most important parameter for this type of capacitor. Low series R and low parasitics are key.
- [17] Analog filter implementations will drive density to $7 \text{ fF}/\mu\text{m}^2$. As digital filter solutions dominate beyond 2003, bypass capacitor applications will drive density. As digital content increases, chip size decreases, and capacitors occupy a larger percentage of a chip. Choice of implementation is driven by complexity/chip size tradeoff (cost). microelectromechanical systems (MEMS) implementation for filter applications may be favorable at density $=7 \text{ fF}/\mu\text{m}^2$. Voltage linearity and leakage are not driven by this capacitor.
- [18] Matching important for this capacitor. Specified at a value of 1 pF.
- [19] As digital filter solutions dominate beyond 2003, bypass capacitor applications will drive density. High κ dielectrics may be cost-effective as chip size decreases in the 5–15 year timeframe. Density is driven by low frequency requirements and chip size considerations.
- [20] Voltage linearity not driven by this capacitor.
- [21] Q is important for this capacitor to provide bypass response at high frequency. Massively parallel, parasitic implementations are expected to dominate for the next five years.
- [22] Analog capacitors do not drive density.
- [23] Voltage linearity is driven by switched capacitor applications. Low series R is key.
- [24] Leakage is driven by feedback capacitor applications where a long time constant is required. Requirement is relaxed with increasing analog clock frequency. Highest quality dielectric is suggested.
- [25] Matching is key for analog capacitors. Specified at a value of 1 pF.
- [26] Q is important for this resonator. Low RF parasitic structures such as MEMS polysilicon structures are long-term solutions (see Potential Solutions Figure 14).
- [27] Matching is important for the analog resistor. Careful layout and photolithographic uniformity are required. Minimum dimensions assumed to be larger than minimum technology dimensions. **Specified at a value of 1 M Ω .**
- [28] 1/f noise requirement is most important for the analog resistor. It is assumed that low 1/f solutions other than polysilicon coincide with high Q RF resistor solutions. **1/f spectral density is normalized to resistor area=1 μm^2 , frequency=1 Hz.**
- [29] Temperature coefficient is important for the analog resistor. Low TC films or TC canceling techniques may be utilized
- [30] Q is most important for the inductor. Low series R implementations such as thick copper is assumed for the next five years. CMOS trend toward increasing substrate doping conflicts with inductor integration. Solutions that mitigate the CMOS conflict and maintain Q are assumed.

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- [30] *Q* is most important for the inductor. Low series *R* implementations such as thick copper is assumed for the next five years. CMOS trend toward increasing substrate doping conflicts with inductor integration. Solutions that mitigate the CMOS conflict and maintain *Q* are assumed. **Specified at $L = 1$ nH and $f = 1$ GHz.**
- [31] Signal isolation is best defined as the transmission efficiency (*S*₂₁ in dB) between a noise source and a noise sensor. Transient sensitivity (in V peak-to-peak) is also an important measure of signal isolation but is not quantified due to its dependence on layout and package. System partitioning, metal interconnect scheme, substrate resistivity, and package design have significant impact on the signal isolation performance. Final result is dependent on application and design tradeoffs.
- [32] Gain for low-noise amplifier and mixer benchmark circuits
- [33] IIP3 for low-noise amplifier and mixer benchmark circuits
- [34] Noise figure for a low-noise amplifier benchmark circuit
- [35] Noise for a mixer benchmark circuit
- [36] Resolution for A/D, D/A benchmark circuits required for audio/video applications

Several trends have been identified for analog, RF and mixed-signal requirements that will lead to higher levels of integration with logic: raw speed of the logic process will enable more signal processing in the digital realm and the implementation of some RF functions; use of dual-gate oxides for higher voltage logic I/O's will support analog requirements for signal headroom; continued focus on 1/*f* noise, capacitor density and component matching will be required for power and area efficient design.

Modularity of process features will be desirable in order to adapt the technology to specific SoC architectures. Optimization of the logic process to meet analog transistor specifications may add process complexity, but will be required to achieve mixed-signal integration goals. CMOS will continue to be the technology of choice except for applications where Si or SiGe BiCMOS offers a clear performance or area advantage in high-speed circuits.

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RELIABILITY*Table 30a Reliability Technology Requirements—Near Term*

YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm
<i>Customer Reliability Expectations (at 85° C Junction Temperature)</i>							
[1] Early failures (ppm) (First 4000 operating hours)	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
[2] Long term reliability (5–10 Years) (FITs = failures in 1E9 hours)	10–100	10–100	10–100	10–100	10–100	10–100	10–100
[3] Soft error rate (FITs)	1000	1000	1000	1000	1000	1000	1000
[4] Relative failure rate per transistor (normalized to 180 nm)	1	1	1	.62	.62	.62	.34
[5] Relative failure rate per m of Interconnect (normalized to 180 nm)	1	1	1	.51	.51	.51	.34
[6] System-on-a-Chip reliability prediction	Logic and Memory			MicroMachine			Micro Optics
[7] Failure analysis cycle time (days)	1–12	1–12	1–12	1–10	1–10	1–10	1–10

Solutions Exist Solutions Being Pursued No Known Solutions 

Note: Reliability requirement includes chip and package failures. Additional parameters (such as temperature cycling and humidity) need to be specified for package reliability.

Table 30b Reliability Technology Requirements—Long Term

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
<i>Customer Reliability Expectations (at 85° C Junction Temperature)</i>			
[1] Early failures (ppm) (First 4000 operating hours)	50–2000	50–2000	50–2000
[2] Long term reliability (FITs = Failures in 1E9 hours) (5–10 Years)	10–100	10–100	10–100
[3] Soft error rate (FITs)	1000	1000	1000
[4] Relative failure rate per transistor (normalized to 180 nm)	.16	.07	.03
[5] Relative failure rate per m of interconnect (normalized to 180 nm)	.18	.10	
[6] System-on-a-Chip reliability prediction	Micro Biological		
[7] Failure analysis cycle time (days)	1–10	1–10	1–10

Solutions Exist Solutions Being Pursued No Known Solutions *Notes for Table 30a and b Reliability Requirements*

- [1, 2, 3, 5] Reliability requirements vary with application. For many mainstream customers it will be sufficient to hold current reliability levels steady during this period of rapid technological change. However, other customers would like reliability levels to improve. Degradation of current reliability levels is not acceptable.
- [1] Early failures are generally associated with defects.
- [3, 4] Inverse of number of transistors per generation (3) or meters of interconnect per generation (4). For the reliability levels of the chip to remain constant (1,2) the failure rate per transistor or per meter of interconnect must be reduced.
- [6] Need to develop the capability to predict the reliability of advanced technologies then will be integrated onto advanced Systems-on-a-Chip. Dates when technologies will be inserted are approximate.
- [7] The time to complete the determination of the cause of a yield, field or design failure.

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BEYOND CMOS / NOVEL DEVICES

Non – Bulk CMOS Devices Table

Device	INSERTION NODE (NM)	APPLICATION DRIVER (PERFORMANCE, POWER, COST)	INSERTABILITY (SYSTEM)	INSERTABILITY (INFRASTRUCTURE)	ADVANTAGES	CHALLENGES
SOI (PD)	180	Low Power especially. Performance	OK	OK	Low power, high speed, low voltage operation, reduced SER	Cost, Dynamic body charge
SOI (FD)	130	"	"	"	Low power, high speed, low voltage operation, reduced SER	Cost, Control of very thin Si layer
Multi-Vt Logic MOS	180	Performance	OK	OK	High system speed @ relatively low power	Cost
Multi-value logic	≤100	Cost	Very Difficult	Difficult	Density	V t control, speed.
Dynamic Vt logic (gate tied to body)	≤100 (0.6V restriction on Vdd drives this choice.)	"	". (Note: 0.6V restriction on Vdd is less than ITRS's Vdd for 100 nm node.)	"	High speed @ relatively low power	Cost, Junction leakage. Restricted to Vdd≤0.6 V. For bulk, isolation is an issue.
Vertical MOSFET	≤130 (DRAM) ≤70 (logic)	Performance	Issues. (Only one Lg =>no good for analog.)	Difficult Issues	Litho independence, high Idrive	Processing, Process integration. Standard CMOS needed on same chip.
Double Gate SOI	≤70	Performance	"	Difficult Issues	Improved short channel, high Idrive	Cost, how to fabricate self- aligned double gate
Epi channels, including SiGe	≤70	Performance	OK	OK	High mobilities for electrons and holes	Process complexity, novel materials and processes

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Non-Bulk MOS Technology Descriptions

TECHNOLOGY	DESCRIPTION
SOI (PD)	Partially depleted SOI MOSFETs
SOI (FD)	Fully depleted SOI MOSFETs
Multi-Vt Logic	Multiple threshold voltages provided by a second gate fabricated as a mirror image of the control gate
Multi-Value Logic	Logic gates/primitives providing 3 or more logic states
Dynamic-Vt Logic	Second gate is connected to the body providing high Vt in the off-state and low Vt in the on-state
Vertical MOSFET	MOSFETs fabricated with the source/gate/drain vertically aligned providing for either horizontal or vertical current flow
Double Gate SOI	SOI MOSFETs fabricated with 2 gates providing charge control on the two channel interfaces between the source/drain
Epi Channels	MOSFETs containing group IV alloy (SiGe, SiGeC, etc.) epitaxially grown channels
Delta-Type MOSFET	MOSFET in which the channel has a spiked or delta doping
MEM(D)S	Micro-Electro-Mechanical devices/structures fabricated in silicon (e.g., electrical and optical switches, RF resonators, imagers, etc.)

Novel Logic Devices Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
MEMS	100 (dependent on solving difficult problems, not on 100 nm node CDs)	-Cost, Sys on Chip (RF resonators, imaging, sensors) -ULSI switching (open and close) -Microelectronic chem. Sensors	Difficult issues	Difficult issues	Great SOC flexibility, possible speed, lower power, and low crosstalk (optical interconnect)	Integration of MEMS and Si systems; reliability
Resonant Tunneling IC	≤35	Performance, RF	Difficult issues	Difficult issues	Density, performance, RF	Entirely new IC device
3D Stack Structures	≤35	Cost, power	Issues, especially with interconnect	Difficult issues	Very high density & Short interconnects	Process complexity, Heat dissipation
Organic Transistors (could be on plastic substrate)	≤35	Cost, power	Difficult issues	Difficult issues	Cost, power	Entirely new IC device. Temperature limitations during processing
CHINTS (chan. hot electron injection transistor)	≤35	Performance, power	Difficult issues	Issues	Density, power, performance (multi-value logic)	Entirely new IC device
Carbon Nanotube transistor	≤35	Performance, power	Difficult issues	Difficult issues	Density, power	New device & system

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Novel Logic Device Tables (continued)

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
Single Electron Transfer	≤ 35	Cost	Difficult Issues	Difficult Issues	Desity	New devices & system, Room temp operation questionable, noise (offset charge). Lack of drive current
Carbon Nanotube Transistor	≤ 35	Performance, Power	Difficult Issues	Difficult Issues	Desity, Power	New Devices & System

Novel Logic Device Technology Descriptions

TECHNOLOGY	DESCRIPTION
3D Stack Structures	CMOS gates fabricated with the p-channel MOSFET stacked on top the n-channel MOSFET. Also, ICs fabricated with 2 or more active layers (containing CMOS gates with interconnect layers) stacked Resonant
Tunnel Diode (RTD) IC	An IC fabricated solely using resonant tunneling diodes (negative differential resistance diodes whose conduction state depends upon energetic coincidence of an electrode Fermi energy with a quantum state formed between 2 high-energy barrier potentials). The IC may also consist of RTDs combined with CMOS gates.
Organic Transistors	Transistors fabricated in polymer materials, perhaps, using plastic substrates
CHINTS	Channel hot electron injection transistor - Channel charge density is supplied by the injection of hot electrons from an electrode
Carbon Nanotube Transistor	A transistor fabricated using amphoteric carbon nanotube technology
Single Electron Transistor	A 3-terminal device based on the Coulomb blockade where the number of electrons on an island or a dot is an integer number controlled by a gate

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Novel Storage Devices Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
FERAM	180	Cost, performance for nonvolatile	OK	OK	high capacitance, nonvolatile, low voltage and power (nonvolatile)	Cost, fab., reliability, esp. for highly scaled technology
Multi level Flash	180	Cost	OK	OK	High density - ==>cost reduction	Accurately placing charge on gate, process control, material and reliability
MRAM	≤ 100	Cost	Issues	Difficult Issues	Density, power, performance, nonvolatility	Reliability and integration. Material quality.
Quantum Dot Memories, including single electron	<35	Cost	Difficult Issues	Difficult Issues	Density, power, , nonvolatile capability	New device & system. Room temperature operation difficult.

Novel Storage Device Technology Descriptions

TECHNOLOGY	DESCRIPTION
FERAM	Ferroelectric RAM
Multi-Level Flash	A flash memory cell containing two or more addressable floating gates for charge storage
MRAM	An array of ultra-small magnetic sensors with hysteresis forming the bits. The bits are set by a magnetic field generated by 2 crossed conductors carrying a current, with a bit consisting of magnetic thin multilayers exhibiting magnetoresistance, the conductance of which is based on the spin state of the bit
Quantum Dot	A memory device in which the storage element consists of 2-terminal Memories quantum dot for storage of multiple or single electrons

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Novel Systems Table

Device	Insertion Node (nm)	Application driver (performance, power, cost)	Insertability (system)	Insertability (Infrastructure)	Advantages	Challenges
Cryoelectronics, esp. device optimization for reduced temp. operation	180 (modest cooling); ≤ 50 ($\leq$ Liq. Nitrogen temp.)	Performance	OK (180 nm) -Packaging and cooling issues	Some Issues	Speed, power	Cost
Molecular Electronics	<35	Cost	Difficult Issues	Difficult Issues	Density	Entirely new device, system.
DNA and Biological Computing	<35	Cost, performance	Difficult Issues	Difficult Issues	Density, power, performance	Entirely new device, system.
Quantum Computing -Spin State Structures - Tunneling Phase Logic	<35	Performance, power	Difficult Issues	Difficult Issues	Density, power, performance	Entirely new device, system (NMR readout?)
Quantum devices: Josephson Junction Tunneling devices	<35	Performance	Difficult Issues	Difficult Issues	Speed and relatively low power	Entire new device, system. Room temp. operation.
All-optical integrated computing and swithing	<35	Performance	Difficult Issues	Difficult Issues	Performance crosstalk reduction	Entirely new device and system.

Novel Systems Technology Descriptions

TECHNOLOGY	DESCRIPTION
Cryoelectronics	CMOS technology cooled for special, high performance applications
Molecular Electronics	Electronic logic and memory elements that function as voltage-operated switches fabricated in single molecules
DNA & Biological Computing	DNA Computing: Computational functions performed by a DNA molecule; DNA molecules more likely will guide fabrication of nano-structures via self assembly techniques Biological Computing: Biological cells containing intelligent genes that can add numbers, store bits, keep time and execute programs
Quantum Computing	Performance of computational functions using quantum effects realized in systems utilizing the spin states of atomic nuclei or, alternatively, of electrons. Each atom or electron provides two basis functions (spin-up & spin-down) that define the eigenstates of the system; these coupled (or entangled) eigenstates define quantum bits or qubits as a superposition of the eigenstates. Calculations are based on the controlled coherent interaction between the two qubits (entanglement).
Josephson Junction	Also known as Rapid Single Flux Quantum Logic (RSFQ) Logic Tunneling Devices where a flux quantum is used as a bit. The switching elements are Josephson Junctions formed of a semiconductor-insulator-semiconductor structure.

** In response to the observed acceleration of the Technology Nodes (TN) represented by DRAM half-pitch, the IRC proposes a new TN called Scenario 2 (SC. 2.0) for the year 2001 Renewal. However, due to the lack of time the subsequent contents of this Table are not updated to reflect the new TN.

All modifications of the items and/or numericals modified from the 1999 ITRS are based on the TN of ITRS 1999 and are highlighted in bold blue text.