INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2010 UPDATE

OVERVIEW

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2010 Process Integration, Devices, and Structures (PIDS)Tables Update file	2009 Process Integration, Devices, and Structures (PIDS)
2010 Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (RF A/MS) Tables Update file	2009 Radio Frequency and Analog/Mixed-Signal Technologies for Wireless Communication
Emerging Research Devices (ERD) and Emerging Research Materials (ERM) 2010 Memory Assessment Workshop Summary	2009 Emerging Research Devices
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OVERVIEW

For more than four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles roughly every 24 months). The most significant trend is the decreasing cost-per-function, which has led to significant improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor throughput**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last three decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for Semiconductors (NTRS), which had 1992, 1994, and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of the Roadmap and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999. Since then, the ITRS has been updated in even-numbered years and fully revised in odd-numbered years. The overall objective of the ITRS is to present industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, universities, governments, and other research providers or funders. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that most need research breakthroughs.

The ITRS is a dynamic process, evident by the evolution of the ITRS documents. The ITRS reflects the semiconductor industry migration from geometrical scaling to equivalent scaling. Geometrical scaling [such as Moore's Law] has guided targets for the previous 30 years, and will continue in many aspects of chip manufacture. Equivalent scaling targets, such as improving performance through innovative design, software solutions, and innovative processing, will increasingly guide the semiconductor industry in this and the subsequent decade. Since 2001 the ITRS has responded by introducing new chapters on System Drivers (2001), Emerging Research Devices and Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (2005), and, in 2007, Emerging Research Materials, to better reflect this evolution of the semiconductor industry. The ITRS 2010 Update will also begin to address the subject of Energy.

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of electronics would further reduce the cost per function (historically, ~25–29% per year) and promote market growth for integrated circuits (historically averaging ~17% per year, but maturing to slower growth in more recent history). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?"

In order to properly represent the continuously evolving facets of the semiconductor industry as it morphs into new and more functional devices in response to the broadening requirements of new customers, the 2010 ITRS has addressed the concept of Functional Diversification ("More than Moore"). This new definition (MtM) addresses and emerging category of devices that incorporate functionalities that does not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution and ultimately into Stacked Chip SoC (SCS).

It is forecasted that by the end of the next decade it will be necessary to augment the capabilities of the CMOS process by introducing multiple new devices that will hopefully realize some properties beyond the ones of CMOS devices. However, it is believed that most likely these new devices will not have all the properties of CMOS devices and therefore it is anticipated that heterogeneous integration either at the chip level or at the package level will integrate these new capabilities around a CMOS core.

The participation and continued consensus of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. ensure that the 2010 ITRS remains the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The complete ITRS 2010 Update and past editions of the ITRS are available for viewing and printing as electronic documents at the Internet web site ***http://www.itrs.net***.

Link to 2009 Executive Summary.

SPECIAL TOPICS

ENERGY

Energy consumption has become an increasingly important topic of public discussion in recent years due, in part, to concerns regarding global CO_2 emission. Since semiconductor electronics are broadly applicable to energy collection, conversion, storage, transmission, and consumption/usage, it is not surprising that the ITRS addresses many factors of significance to energy issues. In general, the ITRS documents the impressive trends and, more importantly, sets aggressive targets for future electronics energy efficiency, for example, computational energy/operation (per logic and per memory-bit state changes). The most detailed targets relate directly to semiconductor materials, process, and device technologies, which form the bases of integrated-circuit manufacturing and components, respectively.

At the next level, the ITRS addresses integrated circuit design and its system-level drivers. In both the ITRS Design and the ITRS System Driver chapters, there is increasingly direct influence of energy factors on design technologies, which started a number of years ago. Power consumption is now one of the major constraints in chip design, and the ITRS has identified it as one of the top three overall challenges for the last seven years. Leakage power consumption, including its variability, has been identified as a clear long-term threat and a focus topic for design technology in the next 15 years. The connection with the energy challenge is based on the increasing worldwide usage of information technology devices.

In addition to improved efficiency of the basic components (i.e., switches, wires, and memory bits) and of the circuits they compose, the major favorable impact on energy usage of advancing semiconductor technology is in the applications of the circuits themselves, which are often designed specifically to improve the energy efficiency of end-equipment systems which they control. For example, microcontrollers, signal processors, and power/battery management circuits are key to the efficiency of communications systems, household appliances, transportation (e.g., cars), industrial machines, etc.

The ITRS also addresses the minimization of energy usage in semiconductor manufacturing. In particular, the Factory Integration and the Environmental, Safety, and Health (ESH) chapters present goals for further reducing the amount of energy and other resources required to produce integrated circuits and to generally increase the environmental friendliness of IC fabrication.

The ITRS will continue to focus diligently on energy-related issues along the directions outlined above, and to make important contributions to the energy challenges facing the world. In particular, near its 15-year horizon, the ITRS Emerging Research Devices (ERD) and Emerging Research Materials (ERM) chapters are tracking developments for potential beyond-CMOS devices that may greatly extend the energy efficiency of information technologies.

TECHNOLOGY PACING

The ORTC Technology Pacing Trends drivers for the 2010 Update are unchanged from the published 2009 ITRS tables, except for some corrections on Tables ORTC-2C and 2D. The corrections to ORTC -2C, and 2D do not affect the ITWG table update drivers for the ITRS 2010 Update (See additional detail in the *2010 ITRS ORTC section* below.)

However, the ITRS International Roadmap Committee (IRC) and the PIDS ITWG Team felt it was important for the 2010 Update readers to also be aware of recent 2011 technology pacing update proposals, which are based on real-time changes in the manufacturing technology environment, and to know that the ITRS is responding to the industry pacing with a preview of several key changes, with more details provided in the next ITRS 2011 edition..

The PIDS survey team has made proposals to change the memory technology pacing drivers, which will affect the overall effort of ITWG work in the 2011 ITRS edition. , The preparation for the 2011 edition work began with a "Kick-off" workshop meeting on December 1–2, 2010 ITRS meetings in Tsukuba, Japan.

The PIDS projections for the 2011 proposed technology trend changes are identified below; and are also summarized as data in ORTC table form, Figure 1 and portrayed in graphical and overlay form, Figure 2. The projections are also included in the ***2010 ITRS PIDS update tables***. The remaining ITRS ITWGs will review and respond to these proposals in their tables and text during the 2011 ITRS edition effort. The following is a brief summary of the PIDS ITWG proposals:

PIDS DRAM Metal 1 (M1) Contacted Half-Pitch Proposal:

1. ~1-year pull-in to 2010/42 nm
2. Then 3-year technology cycle (.5× per 2 cycles) out to 2024
3. Design Factor $4f^2$ delayed until 2013

PIDS Flash Poly Un-contacted Half-Pitch Proposal:

1. ~2-year pull-in to 2010/26 nm
2. Then ~4-year cycle to 2017/14 nm
3. Then back on 2009 Trend at 3-year cycle to 2022/8 nm
4. Then flat through end of roadmap at 8 nm due to physics limits of voltage and electron storage
5. The multi-level-cell (MLC) 4 bits/cell is delayed to 2019

The 2010 ORTC Update MPU M1 half-pitch and gate length trends remain unchanged from the 2009 ITRS; however, new surveys are underway and new proposals will be considered for possible changes during the 2011 ITRS work, including:

1. Evaluation of the "Two-company" ITRS rule for the M1 contacted half-pitch and other key trends;
2. Evaluation of the alignment of industry published "nodes" trends and the relationship between "Moore's Law" high-density and high-performance drivers with low-power needs in both high-performance and mobile applications
    a. Consideration will also be given in the 2011 ORTC and ITWG tables to possible technology pacing driver segment convergence—MPU high performance, MPU/ASIC low operating power (LOP), and MPU/ASIC low standby power (LSTP) into two segments.
3. Alignment and trade-off with the "equivalent scaling" technology roadmap trends (see also the "Equivalent Scaling" special topic below)

4 Overview

Table ORTC-1 ITRS Technology Trend Targets **[including PIDS 2011 Roadmap Flash and DRAM Trend Driver Proposals]**

	Year of Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
2010 ORTC	*Flash ½ Pitch (nm) (un-contacted Poly)(f)[A]*	38	32	28	25	23	20	18	15.9	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3	N/A
2010 PIDS Projection based on survey data	*Flash ½ Pitch (nm) (un-contacted Poly)(f) [B]*	N/A	26	24	22	20	19	18	16	14	13	12	11	9	8	8	8	N/A
2010 WAS	*DRAM ½ Pitch (nm) (contacted)[C]*	52	45	40	36	32	28	25	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	N/A
2010 PIDS Projection based on survey data	*DRAM ½ Pitch (nm) (contacted) [D]*	N/A	42	36	31	28	25	24.0	21.0	18.0	16.0	14.0	13.0	12.0	10.0	9.0	8.0	N/A
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)[1,2]	54	45	38	32	27	24	21	18.9	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5	N/A
	MPU Printed Gate Length (GLpr) (nm) ††[1]	47	41	35	31	28	25	22	19.8	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9	N/A
	MPU Physical Gate Length (GLph) (nm)[1]	29	27	24	22	20	18	17	15.3	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	N/A
	ASIC/Low Operating Power Printed Gate Length (nm) ††[1]	54	47	41	35	31	25	22	19.8	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9	N/A
	ASIC/Low Operating Power Physical Gate Length (nm)[1]	32	29	27	24	22	18	17	15.3	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	N/A
	ASIC/Low Standby Power Physical Gate Length (nm)[1]	38	32	29	27	22	18	17	15.3	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	N/A
	MPU Etch Ratio GLpr/GLph (nm)[1]	1.6039	1.5296	1.4588	1.4237	1.3895	1.3561	1.3235	1.2917	1.2607	1.2304	1.2008	1.1720	1.1438	1.1163	1.0895	1.0633	N/A

Figure 1 ORTC Table 1 with PIDS update proposals for 2011 ITRS effort)

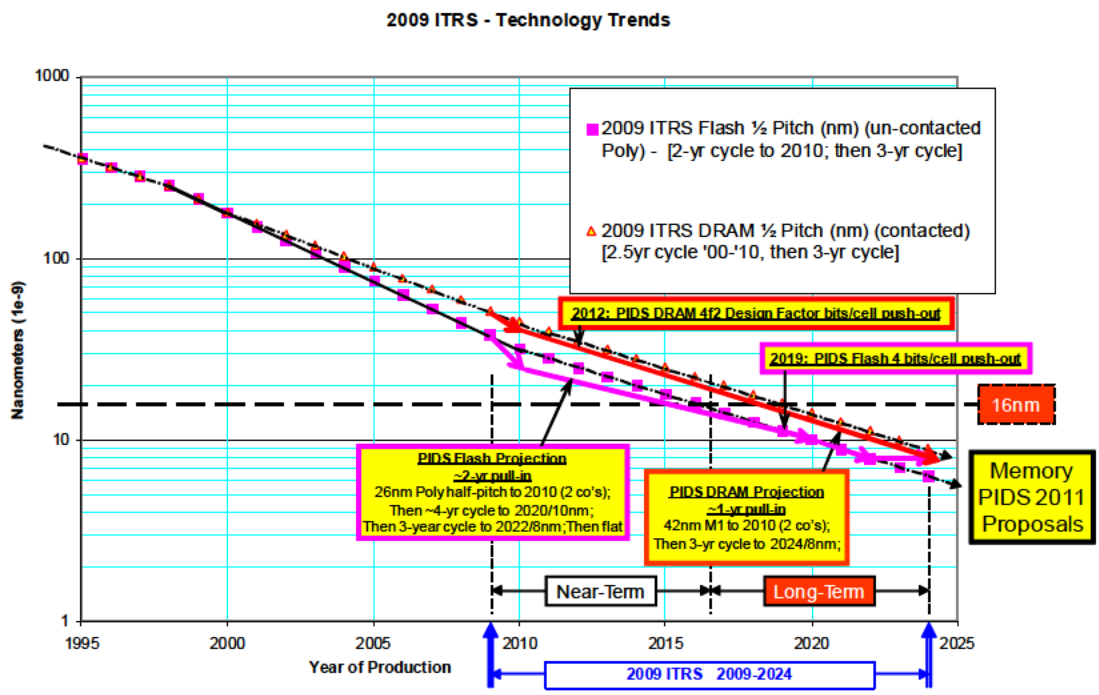

Figure 2 ORTC Table 1 Graphical Trends (including overlay of PIDS update proposals for 2011 ITRS effort)

Link to Overall Roadmap Technology Characteristics section

EQUIVALENT SCALING

The ORTC Technology Pacing Trends drivers for the 2010 ITRS Roadmap Update also include "equivalent scaling" technology introductions, along with the classical "Moore's Law" dimensional trends (***Refer to the Glossary for additional definition detail).*** Also see examples of "equivalent scaling" technology included in Figure 3.

Individual companies are on different technology implementation timing paces for differing reasons, based on their product market needs, competitive position, and their company technology roadmap differences. During the 2010 ITRS update work, the ITRS IRC determined that clarification and flexibility were needed to properly communicate the ITRS vision for various equivalent scaling pathways. These "Equivalent Scaling Roadmap" pathways were first shown in the Figure 8c of the 2009 Executive summary and needed to be updated to current industry status.

In particular, the pathways for bulk CMOS and SOI needed to be separated, and the grouping of associated technologies aided the simplification of the graphic. This clarification and simplification was in preparation for the ITRS 2011 edition work, which would do the following:

1. Reposition the technology insertion timing for the possible relationship with "mix and match" trade-offs between "equivalent scaling" technology and dimensional technology progressions (for "Moore's Law" density requirements versus power and performance management trade-offs). This is especially true when taking into account the impact of recent memory technology pacing proposals and anticipated proposals on logic technology pacing
2. Prepare the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) ITWGS for their cross-TWG negotiations with the Process and Integrated Devices (PIDS) and Front-End Processes (FEP) ITWGs to transfer responsibility for new high-mobility gate channel materials (i.e., Germanium channel and III/V materials) and new logic switch and memory storage candidates from the "Beyond CMOS" region.

The work of clarification and simplification of the "Equivalent Scaling Technology Roadmap" resulted in a preliminary consensus represented in Figure 3. That figure will receive additional consensus-building during the 2011 ITRS work, including the development of agreement on additional timing shifting of the 3-dimensional multi-gate transistor technology insertion. See Figure 3.

The dimensional industry "node" and ITRS technology pacing targets are also shown in Figure 3, not necessarily to suggest an absolute relationship/linkage between the equivalent scaling and dimensional scaling timing. Rather it is shown for convenience of the reader to view what is in fact the present timing of the latest dimensional and technology pathways to date. Please note that the dimensional pacing is based on the 2009 ITRS and does not yet include the proposals for the memory DRAM and Flash proposals under consideration for the 2011 ITRS edition work.

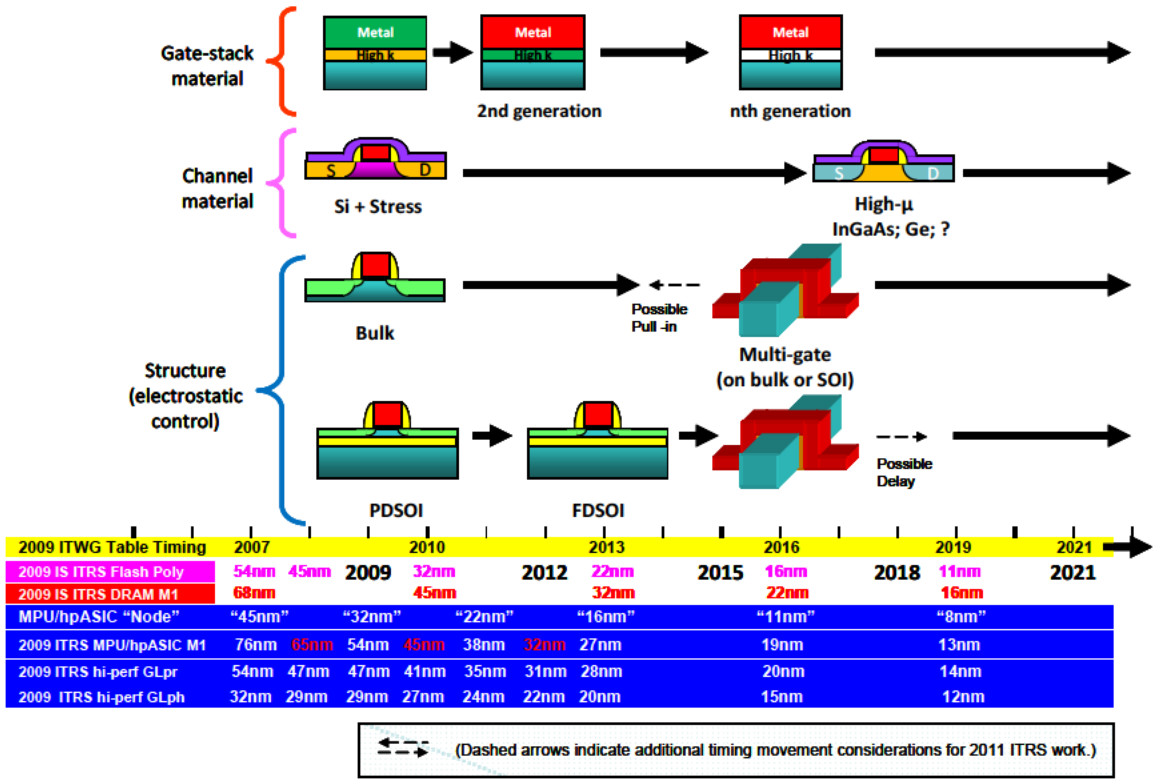

Figure 3 ORTC Table 1 Graphical Trends (including overlay of 2009 industry logic "nodes" and ITRS trends for comparison)

Please see the PIDS, FEP, ERD, and ERM chapters' text and tables for additional details.

MORE THAN MOORE

Link to More than Moore white paper

During the year 2010, the ITRS community has been continuing its active engagement in the investigation of the "More than Moore" (MtM) concept, which was first introduced in the 2005 ITRS.

Given the benefits that roadmapping has brought to the semiconductor industry so far, the International Roadmap Committee clearly wants to include more significant parts of the "More-than-Moore" domain in the work of the ITRS community. In particular, it has tackled the difficult question of how to build a roadmap (or several roadmaps) for the various "More than Moore" technologies. Indeed, in the absence of a single law of expected progress such as Moore's law for the many devices and technologies that enable the "More than Moore" trends, a different methodology is needed to identify and guide roadmap efforts in the MtM domain.

The ITRS has therefore elaborated ***a white paper, available at this link on the ITRS website,*** to propose a methodology that helps the ITRS community to identify those MtM technologies for which a roadmapping effort is feasible and desirable. It departs from the traditional "technology push" approach that the ITRS has followed for roadmapping the continuation of Moore's law (i.e., linear scaling), and requires to collect both technical and market data, thus implying the involvement of many actors beyond the ITRS historical membership, and representing the application domains. In particular, the ITRS has been actively engaging with other entities involved in roadmapping, such as ***the International Electronics Manufacturing Initiative (iNEMI).***

It should be stressed here that the white paper is not intended to be the "final words" on MtM roadmapping methodology, but rather a way to collect more inputs and advices on what promises to be a very challenging task.

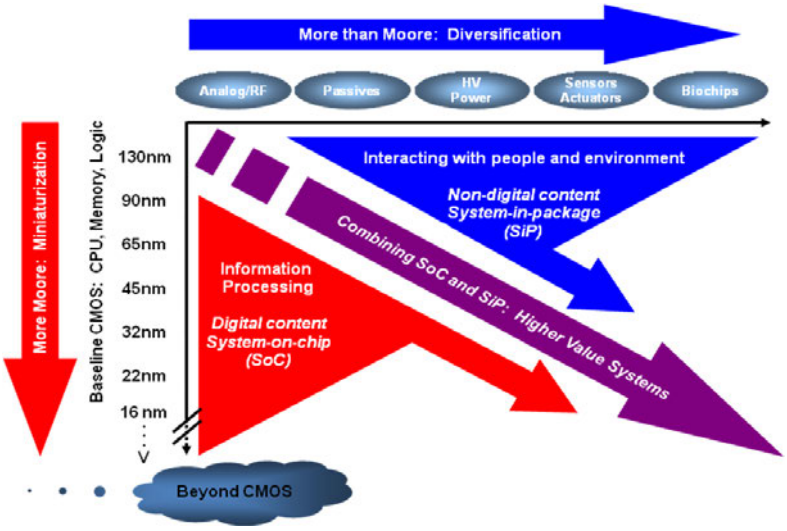

Figure 4 The Concept of Moore's Law and More

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS —2010 UPDATE

SUMMARY

The ITRS Overall Roadmap Technology Characteristics (ORTC) section provides both originating guidance from ORTC Product Models and also consolidates items from other ITRS International Technology Working Group (ITWG) tables.

The metric values of the ORTC tables can be found throughout the 2010 Update Roadmap in greater detail in each technology working group update section. The information in this section is intended to highlight the current rapid pace of advancement in semiconductor technology. It represents a completion of the revision update work that began in 2010, and summarizes the major changes to the ORTC Tables. This 2010 Update version of the ORTC summary is abbreviated from the 2009 ITRS edition Executive Summary, which can be viewed online at ***www.itrs.net***. Additionally, the ORTC Glossary has been included in this 2010 Overview from 2009 ITRS Executive Summary.

There continues to be confusion in the industry regarding individual company public press announcements of their "node" progress and timing, which may or may not align with the ITRS definitions and specific targets. Industry technology progress alignment and communication continues to be a challenge for the ITRS and is further complicated by the recent trends to trade off historical dimensional scaling with technology solutions known as "equivalent scaling" (examples: copper interconnect, strained silicon, metal gate, high-κ gate dielectric, fully-depleted SOI; multi-gate transistors; etc.).

There will also be added complication to the technology progression tracking issue as the market and company public and media relations attempt to describe and connect "design equivalent scaling" and the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) "Beyond CMOS "potential solutions to their chapters and their cross-ITWG modeling with Process Integration, Devices, and Structures (PIDS) and Front End Processes (FEP). New "design equivalent scaling" definitions had been added to the ITRS definitions for "More Moore Geometrical and Equivalent Scaling;" and "More than Moore Functional Diversification" to the Glossary in the ITRS 2009 edition to continue to address the subtleties and for needed clarification of the definitions of the new "More Moore" and "More than Moore" solutions.

2010 UPDATE NOTES

The following notes highlight the key updates for each table set. ***To download or review the 2010 Update ORTC tables , select this link.***

TABLE 1—"PRODUCT GENERATIONS AND CHIP SIZE MODEL TECHNOLOGY TREND TARGETS"

For the 2010 Update version, the ORTC 2009 tables remain unchanged in guiding the 2010 TWG table update work. Flash Un-contacted Poly Half Pitch is unchanged from the 2009 ITRS, and after accelerating in the 2009 version one year to 2010/32 nm, the Flash technology pacing trend goes forward from 2010 at a 3-year cycle pace. The DRAM M1 Contacted half-pitch also remains unchanged for the 2010 update, and based on the 2007 PIDS TWG survey recommendations, is on a 2.5-year cycle through 2010/45 nm, then returns (unchanged) to a 3-year cycle. (See Figures 5a and 5b.)

However, it must be noted that the PIDS ITWG has updated their survey in 2010 and have included their proposals for revision of the 2011 tables in their 2010 Update tables (see the Technology Pacing in the Special Topics section above). This is atypical of ITRS Update work (due to the potential for confusion), but was done in order to make the ITRS 2010 Update readers aware of the dramatic changes that have occurred this year. This will also allow the other TWGs dependent on these changes to prepare for the 2011 ITRS Full Renewal work that will kick off in December in Tokyo.

A preview of these proposed-for 2011-work PIDS changes is noted above in Figures 1 and 2, which include preliminary 2011 ORTC Table 1 line items, and also proposal trend graphics overlaid on the 2009 and 2010 unchanged trends.

The MPU Contacted M1 Half Pitch is also unchanged from the 2009 ITRS, and continues on a 2-year cycle until 2013/29 nm, when the trend shifts to a 3-year cycle through the remainder of the ITRS timeframe (2024);

The most significant impact to the 2008 and 2009 ITRS editions was due to revisions of the ORTC Table 1 physical and printed gate length trends. Data from surveys in 2008 and 2009 by the PIDS and FEP and Design TWGs indicated that

the final physical gate length reduction had slowed dramatically from past anticipated trends, resulting in revisions that affected many of the 2009 ITRS Update tables, and are used as drivers again for the 2010 ITWG Update tables:

- MPU Physical Gate Length (GLph) is now calculated based on a 3.8-year cycle after 2007 to align on a best-fit with the PIDS survey data;
- MPU Printed (Lithography) Gate Length (GLpr) is based on the Lithography TWG Proposal, and is unchanged in the 2009 and 2010 editions. It should be noted as an important reminder to the reader that the gate length trends are no longer based on a parallel relationship to the MPU/DRAM Half Pitch; therefore, the 1.6818 GLpr/GLph past constant ratio is a variable shrinking ratio throughout the roadmap period*.
- ASIC Low Operating Power Printed Gate Length is unchanged and was adjusted in the 2009 version for consistency with the 3.8-year-cycle MPU High Performance Printed Gate Length and also with the new Litho TWG variable GLpr/GLph etch ratio*;
- ASIC Low Standby Power Physical Gate Length was added in the 2009 edition as a new ORTC Line Item and also remains unchanged in 2010;
- *The MPU High Performance variable GLpr/GLph etch ratio (versus fixed ratio) continues as a new ORTC Line Item in the 2009 and 2010 version;
- The impact of the physical and printed gate length changes are included with additional table detail and notes in the PIDS and FEP and Lithography section tables and notes.
    - Included in the 2009 ITRS edition and continued unchanged in the 2010 Update edition is a more robust FEP, PIDS, and Design model impact update; including the relationship with "equivalent scaling" (next generation metal gate and gate high-κ dielectrics, FDSOI, multi-gate transistors, etc.) trade-offs and the timing placement for future "equivalent scaling" technologies as potential solutions for performance and power management.

Please read the Equivalent Scaling special topic above and make note of 2010 revision proposals of the Equivalent Scaling Technology Roadmap graphic, Figure 3.

TABLES 2A THROUGH 2D—"PRODUCT GENERATIONS (DRAM, FLASH, MPU/ASIC) AND CHIP SIZE MODEL TECHNOLOGY TRENDS"

In 2010, there were no changes to the 2009 ORTC DRAM and Flash technology trend and product models. As a result, the memory product tables, ORTC -2A and 2B, which are sourced from those models, remain unchanged. (See Figures 6 and 7a.)

However, in the 2011 ITRS work, begun in December 2010, these ORTC product models will be updated to reflect the impact of the new PIDS memory DRAM and Flash projection proposals noted in the Technology Pacing special topic above.

The MPU product models in Tables ORTC-2C and 2D underwent some corrections which affected the introduction-level trends, but did not impact the work of the 2010 Update of the ITWG Tables, since the ITWG tables are driven by the ORTC production-level model trends. The production-level trends remained unchanged from the 2009 ITRS. See Figures 7a and 7b. (The previous ITRS graphics of combined memory and logic half-pitch and gate-length trends were replaced in the 2009 ITRS edition by separate Figures 5a and 5b and, similarly, the previously combined memory and logic functions per chip and chip sizes trends graphics were updated in the 2009 ITRS edition, too, as shown in Figures 7a and 7b.)

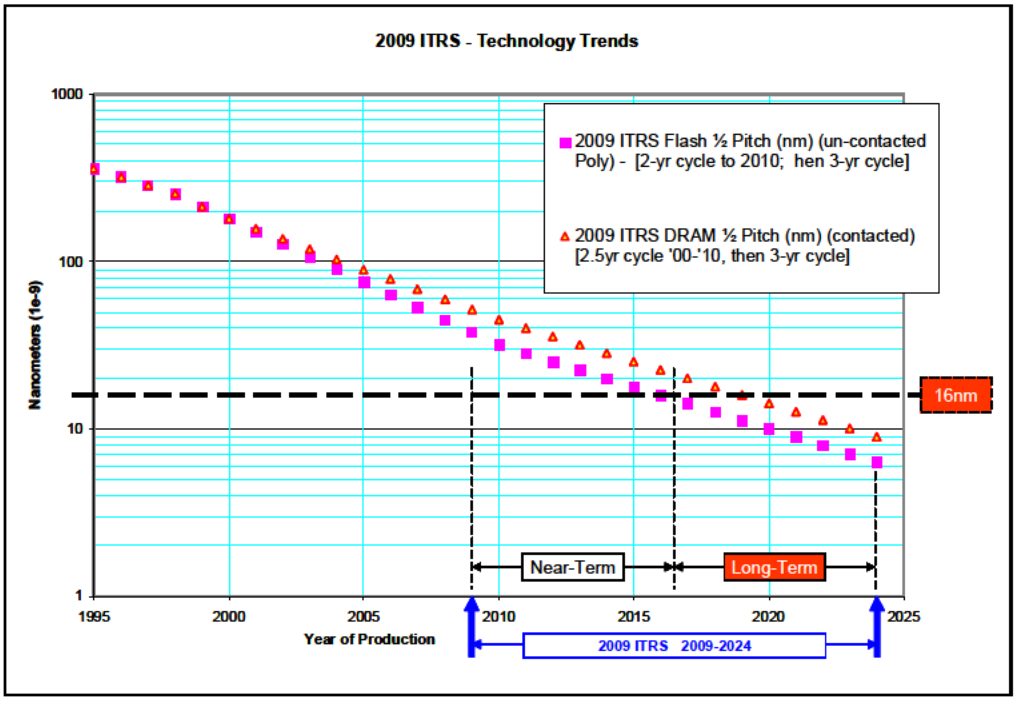

Figure 5a DRAM and Flash Memory Half Pitch Trends

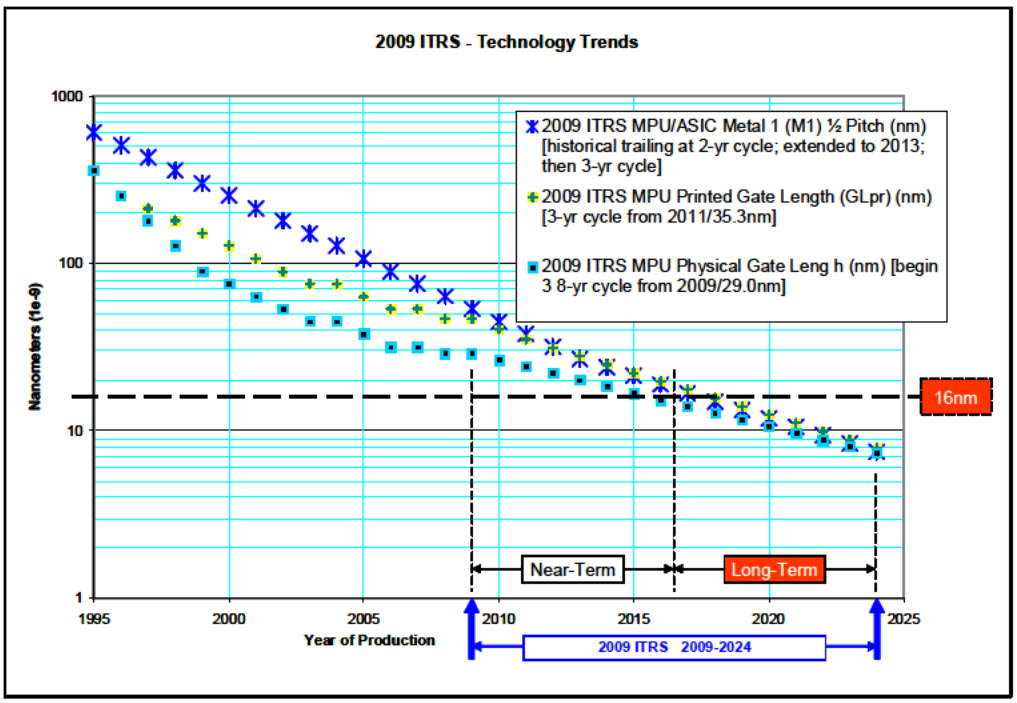

Figure 5b MPU/high-performance ASIC Half Pitch and Gate Length Trends

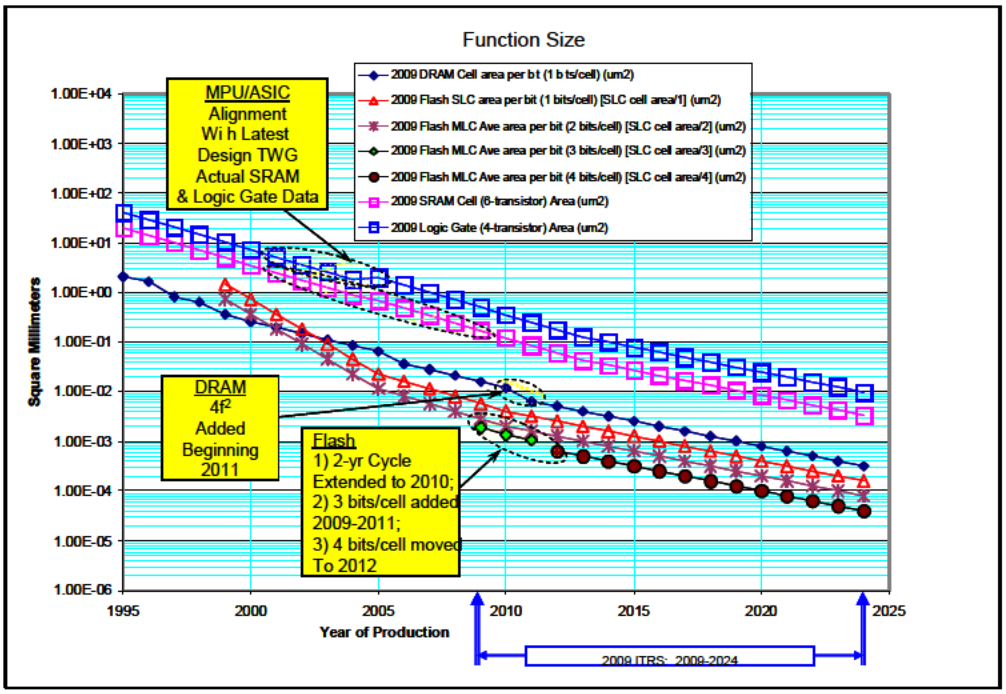

Figure 6 2009 ITRS Product Function Size Trends:
MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)]

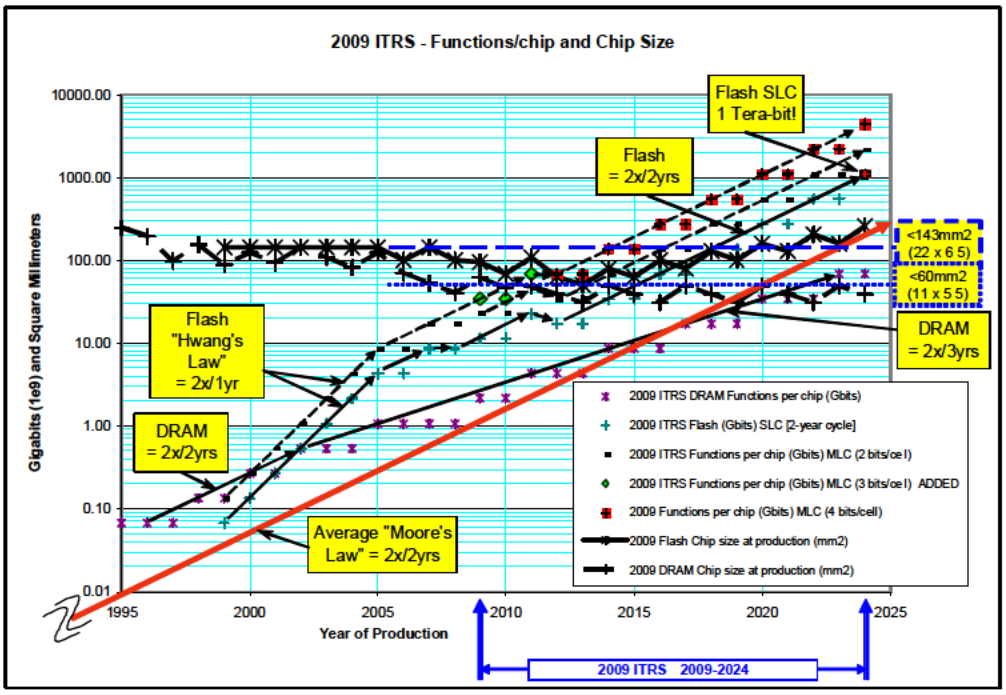

Figure 7a 2009 ITRS Product Technology Trends:
Memory Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

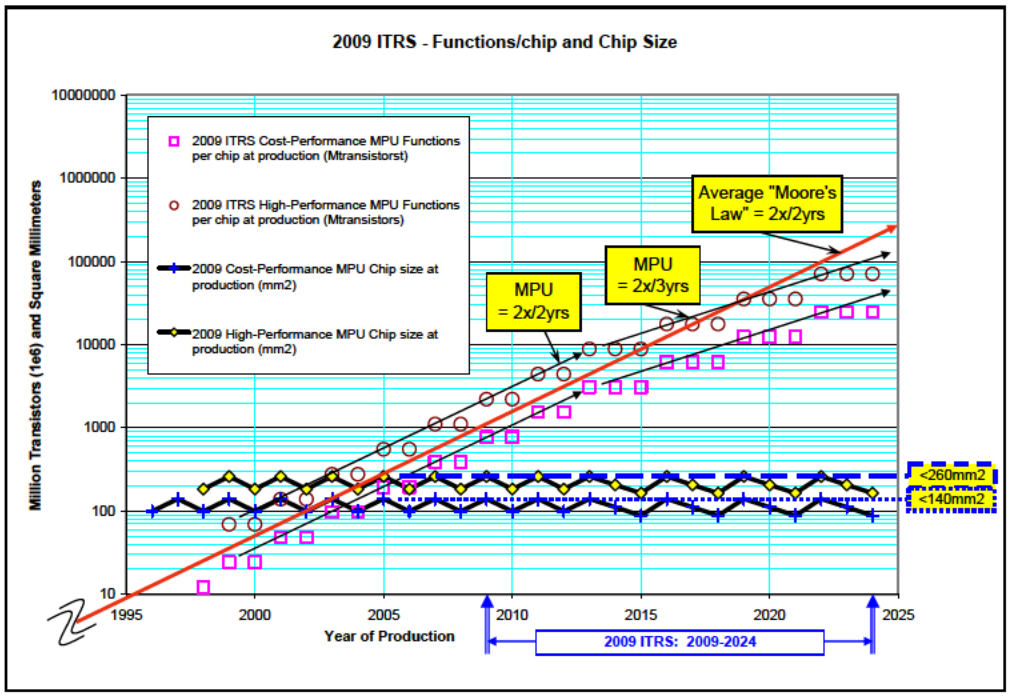

Figure 7b 2009 ITRS Product Technology Trends:
MPU Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

The remaining changes to Tables ORTC-3 through ORTC-7 for the 2010 Update are derived from corresponding changes to ITWG tables, which are used as the various source line items for consolidation in the ORTC. A review of these ITWG-related ORTC tables is included below.

TABLE 3—"LITHOGRAPHIC-FIELD AND WAFER-SIZE TRENDS"

Lithography field size trends are unchanged from the 2009 ITRS document. The 2010 update wafer generation timing targets for the 450 mm generation also remain unchanged from the 2009 ITRS. The 450 mm targets were revised in the 2009 ITRS to begin production in the 2014–2016 timeframe on a delayed 12–14-year cycle).The International Roadmap Committee (IRC) had originally commented in 2008 that the 450 mm volume production ramp by product group "could range at different rates from 2012–2016," but that range was narrowed to 2014–16 in the 2009 and 2010 editions, and will undergo re-evaluation for possible updating during the 2011 ITRS work.

Significant progress by consortia is ongoing, as is dialogue between semiconductor manufacturers and suppliers to assess standards and productivity improvement options on 300mm and 450 mm generations. Economic analysis of option scenarios also continues to examine the required R&D cost, benefits, return-on-investment, along with funding mechanism analysis and proposals from companies, and different regional consortia and governments. See Figure 8 for the timing targets for 450 mm, which were added to the 2009 ITRS Executive Summary, and continue unchanged in the 2010 edition.

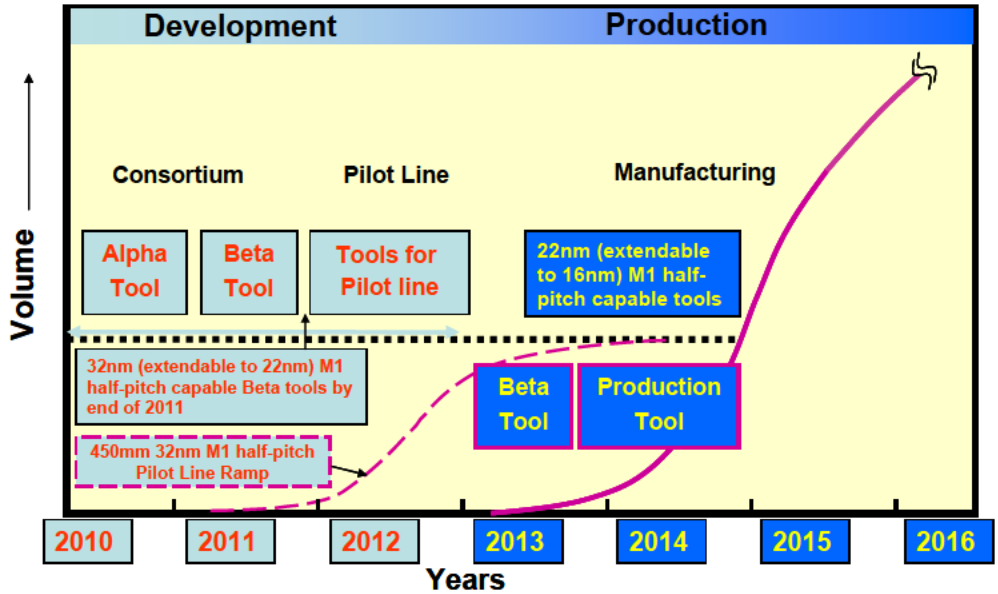

Figure 8 A Typical Wafer Generation Pilot Line and Production "Ramp" Curve applied to Forecast Timing Targets of the 450 mm Wafer Generation

TABLE 4—"PERFORMANCE AND PACKAGE CHIPS TRENDS":

The 2010 update for internal chip pad counts for both I/O and power and ground remain unchanged (2:1 ratio I/O-to-power/ground for high-performance MPU; 1:1 ratio for high-performance ASIC). And numerical targets and trends for the maximum pin counts and packaging costs also remain unchanged from the 2009 ITRS,

The Assembly and Packaging ITWG has made adjustments to their targets for pad pitch. Cost-per-pin targets are unchanged by Assembly and Packaging (A&P) and reflect that ITWG's estimates and response to cost challenges.

In the 2007 ITRS edition, the chip-to-board (off-chip) frequency was removed from the ORTC to avoid confusion with the Design/Process Integration (PIDS) targets for on-chip frequency (see the A&P ITWG tables for off-chip frequency). The Design and PIDS ITWG recommended targets for maximum on-chip frequency remain unchanged from the 2009 ITRS target of 8% average annual growth trend. The 8% growth trend forecast, was derived from the 2007 Design ITWG surveys and Product Performance Models. The PIDS ITWG has maintained a 13% intrinsic transistor speed growth target, which provides significant designer "headroom" compared to the 8% Design ITWG chip frequency trend drivers.

The maximum chip frequency in actual product is running lower than the ITRS targets, and it is likely that the models from both PIDS and Design will be revised during the 2011 ITRS work. The Interconnect ITWG has left the number of on-chip wiring levels unchanged, as reflected in the 2009 and 2010 ORTC line item tracking that trend.

TABLE 5—"ELECTRICAL DEFECTS"

Due to the unchanged product models, the ORTC defect density targets remain unchanged from the 2009 ITRS edition. The number of mask levels, provided by the Lithography ITWG, also remains unchanged, but is under evaluation by the Lithography ITWG to determine the impact of recent trends of increasing mask levels; especially due to the growth trend of double-masking to extend optical lithography until the anticipated arrival of EUV solutions.

TABLE 6—"POWER SUPPLY AND POWER DISSIPATION"

The targets for V_{dd} for both high performance and low operating power voltage remain unchanged from the 2009 Roadmap. However, the A&P ITWG is re-evaluating the approach for modeling maximum power, which is based on per square centimeter targets alone. The A&P ITWG approach takes into account "hot spots" on the chip and the need for cross-TWG potential solutions from both the Interconnect ITWG and the packaging roadmap which would mitigate those power dissipation challenges. In the meantime the ORTC maximum Watts targets in the 2010 tables continue to be calculated for specific product maximum production start chip sizes, which are unchanged from the targets in the 2009 ORTC chip size models (See Tables ORTC-2A through 2D and Figures 7a and 7b).

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TABLE 7—"COST"

The "tops-down" semiconductor market driver models for cost-per-function remain unchanged from the 2009 ITRS. The cost table targets for both memory and logic represent the need to preserve the historical economic semiconductor device productivity trend for continuous reduction of the cost-per-function by -29% compound annual reduction rate (CARR) throughout the roadmap timeframe.

Preserving this cost-per-function productivity trend in view of increasing packaging costs, plus the slowing of product function densities due to slower technology cycles (three-year versus two-year) and design factor improvements, represent the over-arching economic grand challenge for the industry; and the major driver of the Factory Integration ITWG productivity improvement grand challenges and potential solutions

Link to 2009 Executive Summary

Link to 2010 Update ORTC tables' file

2010 UPDATE: WORKING GROUP SUMMARIES

SYSTEM DRIVERS AND DESIGN

Link to the 2010 Update file for System Drivers.

Link to the 2010 Update file for Design.

Link to the 2009 System Drivers Chapter.

Link to 2009 Design chapter.

In the 2010 Update of the ITRS Design and System Drivers chapters, focus is on a few selected key messages and updates described below.

Key messages continue to be delivered by these chapters. First, design productivity continues to be center focus of our design technology roadmap, as scaling depends fundamentally on time to market for electronic products. Accurate design productivity and cost models are crucial. Second, power consumption has become the key technical parameter that controls feasible semiconductor scaling. As a result, the device roadmap has become power-driven, and frequency is being pushed to a flat trend. Third, More than Moore has become a necessary component of semiconductor product scaling. Mixed SiP-SoC analog-digital drivers also need to be roadmapped.

Although this year's design technology roadmap does not feature any major changes, the following workflows are worth mentioning. First, the Design chapter's productivity and cost models are being improved. Second, a "Power Chart" that mimics our well-known productivity chart is being developed, given the critical importance of power to design. Third, 3D/TSV content continues to be made consistent with other chapters, even if there is not a separate section for it within the Design and System Drivers ITWG chapters, due to the breadth of impact of these technologies. Finally, several sections continue to be improved, including the Design for Manufacturing (DFM)—e.g., adding quantifiable Design for Reliability (DFR) requirements)—, Verification, and Logic-Circuit-Physical sections. Finally, for 2010, a refresh of the well-known design cost figure has been provided, with the recognition that the beyond-CMOS part of the curve will require more work as device structures and their design impact are all but unknown in the most distant years.

For the System Drivers chapter, the MPU frequency roadmap is being updated to reflect a flatter trend that has been confirming itself over the last few years—a change whose impact will be reflected beyond these two chapters. Other drivers are being improved not dissimilarly from prior years, including the SoC-CP and SoC-CS models, the RF and Analog/Mixed-signal fabric drivers (in coordination with the Wireless chapter), and an extended/new More-Than-Moore RF andAnalog/Mixed-signal SoC (based on the SoC-Portable driver). All of them will be more accurate integration realities as the roadmap moves to its next 15 years. In the very short term, for 2010, it has been ensured that minimal consistency exists with other chapters such as PIDS by flowing known changes through the key consumer system driver models. This is reflected in Figures DESN5-7 and DESN9-11.

Cooperation with other groups is also being reflected in these two chapters. Additionally, input from the 2nd ITRS-driven EDA Roadmap Workshop at the IEEE/ACM DAC Conference is being incorporated.

Table ITWG1 Major Product Market Segments and Impact on System Drivers

Market Drivers	*SOC*	*Analog/MS*	*MPU*
I. Portable/consumer			
1. Size/weight ratio: peak in 2004 2. Battery life 3. Function: 2×/2 years 4. Time-to-market: ASAP	Low power paramount Need SOC integration (DSP, MPU, I/O cores, etc.)	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
II. Medical			
1. Cost: slight downward pressure (~1/2 every 5 years) 2. Time-to-market: >12 months 3. Function: new on-chip functions 4. Form factor often not important 5. Durability/safety 6. Conservation/ ecology	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SOC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
III. Networking and communications			
1. Bandwidth: 4×/3–4 years 2. Reliability 3. Time-to-market: ASAP 4. Power: W/m^3 of system	Large gate counts High reliability More reprogrammability to accommodate custom functions	Migrating on-chip for MUX/DEMUX circuitry MEMS for optical switching.	MPU cores, FPGA cores and some specialized functions
IV. Defense			
1. Cost: not prime concern 2. Time-to-market: >12 months 3. Function: mostly on SW to ride technology curve 4. Form factor may be important 5. High durability/safety	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
V. Office			
1. Speed: 2×/2 years 2. Memory density: 2×/2 years 3. Power: flat to decreasing, driven by cost and W/m^3 4. Form factor: shrinking size 5. Reliability	Large gate counts; high speed Drives demand for digital functionality Primarily SOC integration of custom off-the-shelf MPU and I/O cores	Minimal on-chip analog; simple A/D and D/A Video i/f for automated camera monitoring, video conferencing Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-position resolution	MPU cores and some specialized functions Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
VI. Automotive			
1. Functionality 2. Ruggedness (external environment, noise) 3. Reliability and safety 4. Cost	Mainly entertainment systems Mainly ASSP, but increasing SOC for high end using standard HW platforms with RTOS kernel, embedded software	Cost-driven on-chip A/D and D/A for sensor and actuators Signal processing shifting to DSP for voice, visual Physical measurement (“communicating sensors” for proximity, motion, positioning); MEMS for sensors	

A/D—analog to digital ASSP—application-specific standard product D/A—digital to analog DEMUX—demultiplexer DSP—digital signal processing FPGA—field programmable gate array i/f—interface I/O—input/output HW—hardware MEMS—microelectromechanical systems MUX—multiplexer RTOS—real-time operating system

Table ITWG2 Overall Design Technology Challenges

Challenges ≥ 22nm	*Summary of Issues*
Design productivity	System-level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation Verification: executable specification, ESL formal verification, intelligent test bench, coverage-based verification Logic/circuit/physical: analog circuit synthesis, multi-objective optimization Logic/circuit/physical: SiP and 3D (TSV-based) planning and implementation flows Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	Logic/circuit/physical: dynamic and static, system- and circuit-level power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Reliability	Logic/circuit/physical: MTTF-aware design, BISR, soft-error correction
Interference	Logic/circuit/physical: signal integrity analysis, EMI analysis, thermal analysis
Challenges <22nm	*Summary of Issues*
Design productivity	Verification: complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage Tools specific for SOI and non-static logic, and emerging devices Cost-driven design flow
Power consumption	Logic/circuit/physical: SOI power management Logic/circuit/physical : Reliability- and temperature-constrained 3D physical implementation flows
Manufacturability	Uncontrollable threshold voltage variability Advanced analog/mixed signal DFT (digital, structural, radio), “statistical” and yield-improvement DFT Thermal BIST, system-level BIST
Reliability	Autonomic computing, robust design, SW reliability
Interference	Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.)

ATE—automatic test equipment BISR—built-in self repair BIST—built-in self test DFT—design for test EMI—electromagnetic interference ESL—Electronic System-Level HW/SW—hardware/software MTTF—mean time to failure SOI—silicon on insulator

TEST AND TEST EQUIPMENT

Link to the 2010 Test and Test Equipment update file.

Link to 2009 Test and Test Equipment chapter.

The 2010 test and test equipment roadmap contains minor updates to table trends, but contains some significant changes to the overall test drivers that reflect the implications of More than Moore trends and the proliferation of multi-core and fault tolerant devices. CPU clock rates have not significantly changed in the last few years and are forecasted to be on a much slower growth curve than forecasted five years ago, but communication and other devices in the >20 Gigahertz range are on the fast change track to higher frequencies and present challenges to traditional test methods.

TEST DRIVERS

The trend toward system in a package solutions to obtain higher performance, lower cost, and reduced power consumption remains, but is being enhanced with a focus on the test challenges for 3D multi-die and multi-layer implementations which either use multiple die connected with TSVs or a single base silicon where a second, third or N layers are added to the previously completed circuit layer by forming a new silicon (or other material) base layer and forming new circuits in the added layer. The use of TSV (through silicon via) or TLV (through layer via) solutions will add complexities to the test and design for test processes to ensure the overall quality and reliability of the connections, while at the same time not increasing the test cost by a non-similar scaling factor over the cost of testing individual pieces of silicon. Cost containment will require concurrent or phase shift concurrent testing of similar logical block or cores.

Circuits are becoming more fault tolerant through the use of error detection, which then reacts to the error by disabling and replacing the faulty block, correcting the information, or throttling the system in some manner to achieve reliable and continuing operation. These non-deterministic but algorithmic methods to keep functionality further add to the complexity of determining whether a device is shippable. Improving yield and reducing cost via adaptive test adds the requirement of reliable unit and die-level tracking to take full advantage of the benefits of intelligent test.

High gigahertz frequency radio devices will require innovative solutions that do not depend on the traditional insertion of a device into a socket. These may bring wireless testing of units into mainstream high-volume product along with the added complexity of signal and interference management.

LOOKING TO 2011

The next year will examine the impacts of the key drivers changes made in this 2010 revision. Memory testing has become more type specific and this will be reflected in future tables by replacing the combined memory trends with specific sections for DRAM and NAND. Further focus will be on DFT and testing of 3D structures. Greater than 100GHz testing, concurrent testing, test data volume reduction, and test cost control will also be included in development of the 2011 roadmap.

Table ITWG3 Summary of Key Test Drivers, Challenges, and Opportunities—Updated

Key Drivers (not in any particular order)	
Device trends	Increasing device interface bandwidth and data rates Increasing device integration (SoC, SiP, MCP, 3D packaging) Integration of emerging and non-digital CMOS technologies Device characteristics beyond the deterministic stimulus/response model Fault Tolerant architectures and protocols 3 Dimensional silicon - multi-die and Multi-layer Multiple Power modes and Multiple time domains
Test process complexity	Adaptive test and Feedback data Concurrent test within a DUT Maintaining unit level test traceability Device customization / configuration during the test process
Economic scaling of test	Physical limits of packaged test parallelism Test data volume Managing interface hardware and (test) socket costs Multiple Insertions and System test
Difficult Challenges (in order of priority)	
Test for yield learning	Critically essential for fab process and device learning below optical device dimensions
Detecting Systemic Defects	Testing for local non-uniformities, not just hard defects Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects
Screening for reliability	Effectiveness and Implementation of burn-in, IDDQ, and Vstress testing Detection of erratic, non deterministic, and intermittent device behavior
Future Opportunities (not in any order)	
Test program automation (not ATPG)	Automation of generation of entire test programs for ATE
Majority of effort on mixed-signal and RF tests	Digital tests are just "data" Mixed signal and RF tests tend to be hand coded.
Simulation and modeling	Seamless Integration of simulation and modeling of test interface hardware and instrumentation into the device design process
Convergence of test and system reliability solutions	Re-use and fungibility of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMs—micro-electromechanical systems

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

Link to the 2010 Process Integration, Devices, and Structures update file.

Link to 2009 PIDS chapter.

SUMMARY

The changes made in this update fall into two categories: reduction of power supply voltages V_{dd} for low-power logic technologies, both LSTP and LOP, and incorporation of the latest observations and projections on the fast-moving memory technologies, both DRAM and NVM.

For low-power technologies, the supply voltages are lowered to reduce the dynamic power component. The trade-off is lower speed (I/CV) which is sufficient to meet their performance requirements. The specific changes for each low-power device type are detailed below:

Table PIDS3A: Low Standby Power Technology Requirements

- Off-current I_{off} is reduced from 50 pA/µm to 10 pA/µm to decrease the static power.
- Power supply voltages V_{dd} are lowered to similar values as those of high performance technology to reduce the dynamic power.
- From these changes, the speed I/CV values are reduced by the amounts ranging 20–57% from those of 2009. These speeds are considered to be adequate for their functions.

Table PIDS3B: Low Operating Power Technology Requirements

- Power supply voltages V_{dd} are lowered to reduce the dynamic power.
- From this change, the speed I/CV values are reduced by amounts ranging 14–34% from those of 2009. These speeds are considered adequate.

For memories, the Japan PIDS sub-group had recently finished another survey on future scaling. Together with the latest public product announcements, PIDS has decided to incorporate the latest projections in this update. However, time does not allow the ITRS ORTC tables to propagate such changes across the board to all working groups' tables during the 2010 Update. It has been agreed that PIDS should still go ahead with the latest projections in this 2010 update, and the new projections will be adopted, to be adjusted if necessary per later information, by the rest of ITRS in the 2011 ITRS technology pacing work. Specific changes for each memory device type in the 2010 PIDS tables are listed below:

Table PIDS4: DRAM Technology Requirements

- Half-pitch scaling is accelerated by one year for the next five years.
- Structure transition from RCAT to FinFET is delayed by two years to 2012.
- Vertical channel transistor (VCT) will be launched in 2013 and continue till end of roadmap.
- Cell size factor of $4F^2$ will be delayed by two years.
- Support PMOS gate electrode transition to TiN metal gate is delayed by two years.

Table PIDS5: Non-Volatile Memory Technology Requirements

- Half-pitch scaling is accelerated by one year.
- Product total bit size (in Gb) is accelerated by one year.
- Introduction of 3-D stacking is delayed by one year to 2015.
- 4 bit/cell is delayed by seven years to 2019.

All other tables remain unchanged from the 2009 ITRS chapter:

Table PIDS1: Process Integration Difficult Challenges.
Table PIDS2: High-performance Logic Technology Requirements.
Table PIDS5A: Requirements for Spin-Torque Transfer (STT) MRAM.
Table PIDS6 Reliability Technology Requirements.

Table ITWG4 Process Integration Difficult Challenges

Difficult Challenges for $L_g \geq 16$ nm	*Summary of Issues*
1. Scaling of logic MOSFETs	Scaling planar bulk CMOS Implementation of fully depleted SOI and multi-gate (MG) structures Controlling source/drain series resistance within tolerable limits Further scaling of EOT with higher κ materials (κ > 30) Threshold voltage tuning and control with metal gate and high-κ stack Inducing adequate strain
2. Scaling of DRAM and SRAM	DRAM— Adequate storage capacitance with reduced feature size; implementing high-κ dielectric Low leakage in access transistor and storage capacitor Low resistance for bit and word lines to ensure desired speed Improve bit density and to lower production cost in driving toward $4F^2$ cell size SRAM— Maintain adequate noise margin and control key instabilities and soft-error rate Difficult lithography and etch issues
3. Scaling high-density non-volatile memory	Endurance, noise margin, and reliability requirements Non-scalability of tunnel dielectric and interpoly dielectric in flash Difficult lithography and etch issues with pitch scaling Maintain high gate coupling ratio in floating-gate flash
4. Reliability due to material, process, and structural changes	Threshold voltage shifts due to traps, carrier injection, and program/erase cycling in memory cells Mobility degradation due to mechanical stress relaxation or interface states New or changed failure mechanisms resulting from high-κ/metal gate and new doping/activation processes New failure mechanism resulting from fundamental length scales or new device structures Process variability
Difficult Challenges for $L_g < 16$ nm	*Summary of Issues*
1. Implementation of advanced non-classical CMOS structures	Advanced non-planar multi-gate MOSFETs below 10 nm gate length Control of short-channel effects Drain engineering to control parasitic resistance Strain enhanced thermal velocity and quasi-ballistic transport
2. Implementation of non-classical CMOS channel materials	Identification and demonstration of alternate channel materials New issues from materials, devices, and processing Integration of alternate channel materials on Si platform
3. Identification and implementation of new memory structures	Density and voltage scaling of NVM 3-D integration of NVM Implementing non-charge-storage type of NVM Scaling storage capacitor for DRAM DRAM and SRAM replacement solutions
4. Reliability of novel devices, structures, materials, and applications	Reliability characterization of new devices Dealing with fluctuations and statistical process variations Impact of microscopic physical effects Need for Design for Reliability tools
5. Power scaling	V_{dd} scaling Controlling subthreshold current
6. Beyond CMOS	Identification and implementation of non-CMOS devices and architectures Integration onto Si-CMOS platform See ***ERD*** and ***ERM chapters*** for more discussions and details

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

Link to the 2010 Wireless update file.

Link to 2009 Wireless chapter.

Radio frequency (RF) and analog/mixed-signal (A/MS) technologies serve the rapidly growing wireless communications market and represent essential and critical technologies for the success of many semiconductor manufacturers. Communications products are becoming key drivers of volume manufacturing. Consumer products now account for over half of the demand for semiconductors.[1] For example, third generation (3G) cellular phones now have a much higher semiconductor content and now are 50 % of the cellular phone market compared to only 5 % of the market a few years ago. The consumer portions of wireless communications markets are very sensitive to cost. With different technologies capable of meeting technical requirements, time to market and overall system cost will govern technology selection.

The scope of the RF and A/MS ITWG remains the same as in the 2009 ITRS. The requirements for wireless transceiver ICs are technology drivers that contribute substantially to the recent ITRS-defined More than Moore thrust. This 2010 ITRS RF and A/MS chapter update is divided into applications for less than 10 GHz and mm-wave applications. The RF and A/MS ITWG has five technology subgroups. Four of the subgroups cover applications below 10 GHz: CMOS, bipolar, passives, power amplifiers (PAs) and MEMS. The fifth subgroup on mm-wave applications focuses on power and low-noise requirements of both III-V compound semiconductor and silicon-based devices used in transceiver ICs.

Some portions of the RF and A/MS technology roadmap pertain more to prototype capabilities rather than usual CMOS volume production of most of the other ITRS chapters. Production implies applications and markets. But emerging mm-wave connectivity and imaging applications that are part of the RF and A/MS ITWG currently lag technology capabilities. Also, collaborations with the International Electronics Manufacturing Initiative (iNEMI) are ongoing to generate a matrix of applications versus technologies that cover emerging applications such as ultra low-power, medical, security, and the like.

For CMOS, the 2010 technology requirements tables continue the link of Performance-RF to low standby power (LSTP) CMOS with a one-year lag and mm-wave CMOS to high performance (HP) CMOS with a two-year lag as reflected in the 2009 table. Three adjustments were made for 2010; matching is dramatically lowered to reflect published data for high-κ/metal-gate technologies; f_{MAX} was lowered to better reflect recent publications, and the fact the analog-friendly FETs are now commonly available is reflected in the Precision Analog table.

For bipolar, only the figures of the HS PNP transistor, newly introduced in 2009, have been updated. BV_{CEO} reduction is delayed at the expense of a slower increase in f_T over time in order to better fit to the key applications that are more BV_{CEO} driven than f_T driven today. f_T and f_{MAX} colors have been updated for the HS PNP and PA NPN bipolar transistors in agreement with published data. The key driving forces for the bipolar roadmap continue to include speed, power consumption, noise, and breakdown voltages.

For passive devices, the density and leakage for the on-chip MOS capacitor lag one year behind those for CMOS active devices as shown in the 2010 tables. Inductors with Q factor values of 35 are expected to be manufactured at high volumes in 2012 according to a 2010 publication. However, the technology of 3D IC interposer is expected to enable, higher Q factors in the near future. RF capacitors with densities near 1.5 $fF/\mu m^2$ are now available from some vendors of III-V compound semiconductor PAs. In the table on off-chip inorganic substrate capacitors, the leakage current density tends to be in the range of nA which is reflected in the reliability data of some publications. In the table on potential solutions for 0.4 GHz to 10GHz applications, materials for thinner layers with higher dielectric constants used in decoupling capacitors would require one more year of R&D activities. And, the high-μ materials that are needed in inductors with greater Q factors for use in analog or power devices and circuits would require two more years of R&D activities.

For power amplifiers, Handset Devices—The battery requirements are expected to remain at current levels for at least few more years. The MEMS adoption seems to be happening more slowly than expected, but remains an active area of development. It is also likely to be going directly toward an integrated solution. Base-Station Devices—The tables show that 48V LDMOS is likely to be introduced into the cellular infrastructure market in 2011. This introduction is primarily due to increased demand for higher power parts for Doherty PAs, and, due to the possibility that for the longer term, it

[1] *P. H. Singer, "Dramatic Gains in Performance on the Horizon," editorial in* Semiconductor International*, Vol. 29, No. 8, 29, July 2006, page 15.*

may serve as an envelope tracking or drain modulation solution to achieve higher efficiencies than can be achieved with Doherty PAs alone. In addition, the increased focus on efficiency is reflected in both the P1dB drain efficiency and peak drain efficiency. The goals for high efficiency architecture and drain efficiency have increased for both LDMOS and GaN.

For MEMS, we have no changes to the 2009 ITRS tables. Because MEMs is a very broad and diverse area, we are having ongoing discussions with other ITRS working groups and with iNEMI working group about the optimum way in which to do technology roadmaps for MEMs.

For millimeter wave applications, we have assumed "production" implies that at least one company offers products with "data sheets" or that the technology is available for custom designs from one or more companies as a foundry service. The main changes in the technology requirements table from 2009 are manifested as a delay in the trend to smaller critical dimensions in HBT and HEMT technologies. Because InP HBTs are not moving as fast as predicted to smaller dimensions, increases in f_t and f_{MAX} are slowing-down. For GaN HEMTs, technology challenges of maintaining breakdown voltage are delaying shrinking gate lengths. Nevertheless, we still predict that GaAs and InP will begin to be replaced by GaN as early as 2012 and 2014, respectively, for new applications. Power MHEMT is also likely to eventually be replaced by GaN HEMTs. As predicted in 2009, LN MHEMT at 70 nm is now available. However, continued progress in shrinking dimensions and higher frequency performance will be driven by market applications. Volume markets will be very cost sensitive, and SiGe and RF CMOS will be utilized in applications where their performance is adequate, resulting in possible further delay in transitioning III-V R&D advances into production.

DIFFICULT CHALLENGES

Table ITWG5 RF and Analog Mixed-Signal (RF and AMS) Technologies for Wireless Communications Difficult Challenges

Difficult Challenges	*Summary of Issues*
CMOS	New materials (e.g., high-permittivity gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes) make predicting trends uncertain for transistor mismatch and for 1/f noise.
Bipolar HS-NPNs and HS-PNPs transistors	Increasing f_T by more aggressive vertical profiles and still maintaining acceptable figures of merit, manufacturing control, and punch-through margins
Bipolar Power Amplifiers	Improving the trade-off between f_T/f_{MAX} and breakdown voltages to provide acceptable voltage handling and power densities at performance levels that can effectively complete with alternative technologies.
On-Chip Passive Devices	Integrating new materials in a cost-effective manner to realize compact and high quality factor (Q) inductors and high-density metal-insulator-metal (MIM) capacitors demanded by the roadmap for increased RF performance.
Off-Chip Passive Devices	The large number of options for embedded passives increases complexity and cost. And accurate models for process tolerance and parasitic effects and computer assisted design (CAD) tools.
Handset Power Amplifiers	Increasing functionality in terms of operating frequency and modulation schemes and simultaneously meeting increasingly stringent linearity requirements at the same or lower cost.
Base-station Power Amplifiers	Enhancing performance with continual product-price pressure. And Improving amplifier efficiency.
mm-Wave Devices	Thermal management for high power density circuits, multi-level integration and E/D mode transistors. And reduction of leakage current and understanding of failure mechanisms, particularly for GaN materials which are piezoelectric in nature.
MEMS	Incorporating the great process diversity of MEMS into specific ITRS processes. And developing design tools, packaging, performance drivers, and cost drivers for each MEMS device type.

EMERGING RESEARCH DEVICES

Link to the 2010 ERD and ERM Memory Workshop file.

Link to 2009 ERD chapter.

The ITRS Emerging Research Devices (ERD) International Technical Working Group (ITWG), in collaboration with the Emerging Research Materials (ERM) ITWG and co-sponsored by the National Science Foundation, evaluated and updated their information on several new technologies proposed for beyond CMOS information processing, memory, and storage technologies. In particular, the ERD and ERM ITWGs thoroughly assessed eight of the most promising emerging memory technologies to determine whether one or more has high potential and is sufficiently mature to justify its accelerated research and technology development toward commercialization. To be considered, a memory technology was required to have demonstrated good performance with at least a partially understood storage mechanism and be scalable multiple generations beyond the 16 nm technology generation. Further, it should be ready for manufacturing within the next five to ten years.

This study was initiated for two reasons. First, current memory technologies, such as DRAM, SRAM, and NAND Flash, are approaching very difficult issues related their continued scaling to and beyond the 16 nm generation. Second, research over the past ten to fifteen years has led to discovery of several promising new non-volatile memory technologies, many in the category of resistive RAMs. These emerging research memory technologies include the ferroelectric-gate FET, nanoelectromechanical RAM, spin transfer torque (STT) MRAM, nanoionic or redox memory (including the fuse/antifuse memory and related electrochemical metallization, programmable metal cell and the atomic switch), nanowire phase change memory, electronic effects memory (i.e., charge trapping, mott transition, ferroelectric barrier effects), macromolecular memory, and molecular memory. Research has provided some clarification and insight to the physical storage mechanisms and the limits of several of these approaches; this information was used to establish a basis for judging their long-term potential, The ERD and ERM ITWGs reviewed white papers and listened to arguments presented by advocates and challenged by "friendly critics" for each of the eight technologies. Following considerable discussion, these work groups recommended to the IRC that STT-MRAM and redox RAM receive additional attention in research and development to accelerate progress toward commercialization of one or both of these technologies. The IRC approved communication of these recommendations to the research community and to funding agencies**.** A subsequent workshop will be held to identify specific materials and process research needed to enable critical progress on these technologies.

An ERD Logic Device workshop, also co-sponsored by the National Science Foundation, was conducted in 2010 to evaluate progress and potential of emerging research spin-based and graphene-based logic devices. This workshop followed up an intensive evaluation of several candidate beyond CMOS logic technologies, in July 2008, which resulted in "carbon-based nanoelectronics" being identified as promising candidate information processing by the ERD and ERM ITWGs. Another objective of this workshop was to gather material on selected research areas in order to have current information the 2011 ERD chapter rewrite.

Table ITWG6 Emerging Research Devices Difficult Challenges

Difficult Challenges ≥ 16 nm and < 16 nm	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile and non-volatile memory technologies to and beyond the 16 nm technology generation.	SRAM and FLASH scaling will reach definite limits within the next several years (see PIDS Difficult Challenges). These are driving the need for new memory technologies to replace SRAM and FLASH memories. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in the technology development
Scale CMOS to and beyond the 16 nm technology generation.	Develop new materials to replace silicon as an alternate channel and source/drain to increase the saturation velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation for technology scaled to 16 nm and beyond. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in t
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and a primitive-level architecture to provide special purpose optimized functional cores heterogeneously integrable with silicon CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and develop a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. Bridge a knowledge gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in the technology development

EMERGING RESEARCH MATERIALS

Link to the 2010 ERD and ERM Memory Workshop file.

Link to 2009 ERM chapter.

The 2010 Emerging Research Materials (ERM) chapter is unchanged from the 2009 chapter. In 2010, the ERM Technology Working Group held meetings and workshops to prepare for the rewrite of the ERM chapter in 2011 and worked with other ITWGs to define materials that should be added to the ERM chapter or transitioned to other ITWGs. Workshops and e-workshops were held for the topics of nanowires for devices, carbon nanotube device materials, memory materials, directed self assembly (DSA) for lithography, deterministic doping, "native" interconnects, and ultrathin barrier layers for extending copper interconnects. Meetings were also planned for early 2011 to review progress on carbon nanotubes and graphene for interconnects; directed self assembly for lithography extension, and assembly and package materials. The ERM also participated with ERD, PIDS, and FEP in development of a critical assessment of the maturity of III-V and Ge as alternate channel materials for their potential transition to FEP and PIDS in 2011. The ERM also participated in several meetings with the Assembly and Package and Interconnect ITWGs to identify potential ERM needed to support future 3D interconnect technologies.

The workshops and planning in 2010 were focused on determining the scope of the 2011 ERM chapter and identifying progress and research needed on promising materials. The nanowire workshop reviewed performance of silicon and III-V nanowires and assessed whether the performance of grown nanowires was better than patterned and etched structures. The carbon nanotube (CNT) workshop reviewed progress on the ability to grow CNTs in desired locations with controlled directions and bandgaps. The memory material workshop focused on materials and interfaces to reduce write energy in spin transfer torque (STT) devices and also materials physical mechanisms that enable operation of the Redox RAM. A workshop, organized by SEMATECH, at Kobe, Japan reviewed progress in DSA to determine whether there were any intermediate applications that could be used in integrated circuit manufacturing. The "native" interconnect review assessed the speed of signal propagation and power dissipation of several alternate state variables (i.e., spin, plasmons, etc.) to determine whether signals in beyond CMOS devices can be transmitted between devices without converting to electrical signals. The ultrathin barrier layer workshop reviewed progress of ruthenium based alloys and self assembled layers of organic molecules being scaled to sub 5 nm thicknesses to preventing diffusion of copper. For 3D interconnect technologies, it was determined that ERM should focus on materials to enable a thermal hierarchy for chip attach, stress management polymers that also spread heat and have required mechanical, electrical properties, and moisture resistance properties.

Additional workshops have been planned for early 2011 to get updates on ERM for devices, lithography, interconnects, and assembly and package. An update on graphene is being planned for alternate channel applications and this will be completed prior to the Alternate Channel Material Critical Assessment. A second workshop on DSA will be held on March 4, 2011 at the SPIE conference to assess the state of defect control and identify the potential for defects being reduced to levels compatible with integrated circuit processing. An e-workshop is being planned for February 2011 to review progress of carbon nanotubes and graphene for interconnect and via applications. Multiple e-workshops will be held to review progress in Assembly and Packaging materials including low-temperature chip-to-package or chip-to-chip interconnect materials, polymers to manage stress, thermal, and moisture, and high performance thermal interface materials.

The ERM is also working with other ITWGs to potentially transition more mature materials to their ITWGs. In 2010, the ERM, ERD, PIDS, and FEP held workshops and conducted a critical assessment survey to determine whether Ge and III-V materials were mature enough to transition into the PIDS and FEP roadmaps. ERM is working with the Lithography ITWG to potentially transition evolutionary resist materials into the Lithography roadmap. ERM is also working with the Interconnect ITWG to potentially transition evolutionary copper barrier layers into their chapter in 2011.

Table ITWG7 Emerging Research Material Technologies Difficult Challenges

Difficult Challenges ≤16 nm	*Summary of Issues*
Integration of alternate channel materials with high performance	III-V has high electron mobility, but low hole mobility Germanium has high hole mobility, but electron mobility is not as high as III-V materials Demonstration of high mobility n and p channel alternate channel materials co-integrated with high κ dielectric Demonstration of high mobility n and p channel carbon (graphene or carbon nanotubes) FETs with high on-off ratio co-integrated with high κ dielectric and low resistance contacts Selective growth of alternate channel materials in desired locations with controlled properties and directions on silicon wafers (III-V, Graphene, Carbon nanotubes and semiconductor nanowires) Achieving low contact resistance to sub 16 nm scale structures (graphene and carbon nanotubes) Ge dopant thermal activation is much higher than III-V process temperatures Growth of high κ dielectrics with unpinned Fermi Level in the alternate channel material
Control of nanostructures and properties	Ability to pattern sub 16 nm structures in resist or other manufacturing related patterning materials (resist, imprint, self assembled materials, etc.) Control of CNT properties, bandgap distribution and metallic fraction Control of stoichiometry, disorder and vacancy composition in complex metal oxides Control and identification of nanoscale phase segregation in spin materials Control of surfaces and interfaces Control of growth and heterointerface strain Control of interface properties (e.g., electromigration) Ability to predict nanocomposite properties based on a "rule of mixtures" Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability
Controlled assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components Control of line width of self-assembled patterning materials Control of registration and defects in self-assembled materials
Characterization of nanostructure-property correlations	Correlation of the interface structure, electronic and spin properties at interfaces with low-dimensional materials Characterization of low atomic weight structures and defects (e.g., carbon nanotubes, graphitic structures, etc.) Characterization of spin concentration in materials Characterization of vacancy concentration and its effect on the properties of complex oxides 3D molecular and nanomaterial structure property correlation
Characterization of properties of embedded interfaces and matrices	Characterization of the roles of vacancies and hydrogen at the interface of complex oxides and the relation to properties Characterization of transport of spin polarized electrons across interfaces Characterization of the structure and electrical interface states in complex oxides Characterization of the electrical contacts of embedded molecule(s)
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures Device structure-related properties, such as ferromagnetic spin and defects Dopant location and device variability

FRONT END PROCESSES

Link to the 2010 Front End Processes update file.

Link to 2009 FEP chapter.

SUMMARY

The 2010 FEP updates are minimal. Changes to the FEP tables in an update year are typically minor changes or a result of adjustments in the ORTC scaling numbers that impact the models that feed into the FEP tables. In 2010, one parameter so modified is the physical gate length—which impacts scaling for high performance (HP), low operating power (LOP), and low standby power (LSTP) logic devices, and DRAM ½-pitch scaling—these changes further impact defect and yield numbers in starting materials and surface preparation. This year the ORTC elected not to make any changes to the tables so the FEP tables were not significantly modified. The 2010 update changes focused on Table FEP13 for etch and Figure FEP16 for surface preparation.

The most significant updates for FEP occur in Table FEP13, "Etching Process Technology Requirements." The changes in FEP13 are driven by the many new etch challenges with advanced CMOS technologies. Through-pitch gate CD variations (gate linewidth roughness, across chip variation, and across wafer variation), are changing for gate CD targeting because of the critical effect of etch micro-loading. Micro-loading among various patterns, such as single gate transistor, multiple-finger transistor, array transistor, minimum-pitch transistor, and isolated transistor, becomes more critical as gate CD shrinks. OPC model optimization is critical to minimize gate CD variation among various patterns. Etch-induced loading effect should be included into the OPC model to further improve OPC model accuracy. Similarly, dense versus isolated pattern etch micro-loading effect is critical for SiGe recess etch because the SiGe to gate distance which is critical for transistor performance is strongly dependent on the SiGe etch micro-loading effect. Transistor gate CD control for 3D interconnect technology will also be challenging. Through silicon via (TSV), a key component for the TSV technology may have a transistor exclusion zone due to the high stress of TSV. CD control adjacent to the TSV excluded zone will be challenging due to the low local gate density. The line width roughness (LWR) budget remains constant at 2.28 nm between 2010 and 2011 because recent advanced lithography tools greatly improve across chip line width variation. However, LWR now becomes the largest portion of gate CD variation and resist improvement is urgently needed to further reduce this value. Further reductions in lot-to-lot and wafer-to-wafer gate CD variation will require the development of in-situ CD metrology in the etch tools, possibly with dynamic feed forward correction.

Updates were made to the Surface Preparation Potential Solutions table. As the industry moves toward materials requiring low temperature processing, controlling the interface prior to film deposition will become more critical. Controlled environments (FOUPS, clustered cleans) aqueous and subcritical solvent cleans, and advanced passivants and formulations are all potential method for accomplishing interface control. New materials and technologies will require new photoresist techniques and challenges for photoresist and residue removal. These include multilevel resists, fluorocarbon based residues, and, accomplished with low material loss, no structural damage, no impact to V_t, or work function while being potentially metal gate/high-κ compatible.

An issue of concern to the FEP working group has been the status of high-κ gate dielectric as a volume manufacturing solution. By the spirit of the ITRS guidelines of achieving sufficient volume to be considered in high volume manufacturing, it has done so. In 2011 we will change the coloration of this part of the Technology Requirement tables and of the Potential Solutions tables to indicate this. At the same time, we acknowledge that this solution has not achieved the expected number of implementations at time of writing this to fully fit the high volume definition, although a second manufacturer has just announced high volume implementation of high-κ metal gates for 32 nm technology.

In 2010 FEP worked closely with the Design and PIDS ITWGs to converge on a V_{cc} scaling roadmap for HP, LP, and LSTP. Along with V_{cc} scaling, FEP/PIDS/Design will work together in 2011 towards device metrics including I_{on}, I_{off}, CV/I, which will then guide the roadmap for module metrics (Gate stack, junctions, contacts, etc). The associated Thermal and Thin Films tables will be updated accordingly, with NMOS and CMOS requirements listed separately.

Looking toward 2011, FEP will work with other sub-groups to refine the timelines (and tables) associated with ERM and ERD ITWGs. The timing of MUGFET (ERD) and III-V /heterogeneous (ERM) integration will move two to three years ahead to address industry needs for advanced logic—necessitating changes to the tables to account for the corresponding infrastructure and FEOL module needs. The FEP high-mobility III-V (InGaAs and Ge) substrates identified for ERM will have a wide range of issues. Some of those identified include high throughput CVD epi processes, damage-free doping strategies, resist removal without III-V damage, low D_{it} high-κ dielectrics, defect and surface passivation, barriers and contact metal technologies.

Table ITWG8 Front End Processes Difficult Challenges

Difficult Challenges ≥ 16 nm (Metal 1 1/2-pitch)	*Summary of Issues*
	Strain Engineering - continued improvement for increasing device performance - application to FDSOI and Multi-gate technologies
	Achieving DRAM cell capacitance with dimensional scaling - finding robust dielectric with dielectric constant of ~60 - finding electrode material with high work function
	Achieving clean surfaces free of killer defects - with no pattern damage - with low material loss (<0.2 A)
	High-k/Metal Gate - introduction to full scale manufacturing for HP, LOP, and LSTP - scaling equivalent oxide thickness (EOT) below 0.8 nm
	450 mm wafers - meeting production level quality and quantity
Difficult Challenges < 16 nm (Metal 1 1/2-pitch)	*Summary of Issues*
	Continued scaling of HP multigate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation.
	Lowering required DRAM capacitance by 4F2 cell scheme or like, while continuing to address materials challenges
	Continued achievement of clean surfaces while eliminating material loss and surface damage and sub-critical dimension particle defects
	Continued EOT scaling below 0.7 nm with appropriate metal gates
	Continued charge retention with dimensional scaling and introduction of new non-charged based NVM technologies

LITHOGRAPHY

Link to the 2010 Lithography update file.

Link to 2009 Lithography chapter.

It is becoming increasingly more difficult to extend optical lithography as we know it today. In 2010, Flash devices are being manufactured using 32 nm half-pitch double patterning (DP) as a way of extending the half-pitch while keeping the NA and wavelength constant. This approach will be pushed harder as DRAM and MPU drive down to the 32 nm half pitch and Flash starts to test the limits of optical solutions at the 22 nm half-pitch node in 2013. But it is at this point that an alternative next generation lithography (NGL) must be introduced into manufacturing to ensure a smooth transition into the lithography approaches beyond 22 nm.

At 22 nm, the international community that contributes to the ITRS saw possible divergence between Flash and DRAM/MPU products. Flash will continue using 193 nm immersion as the lithography technology of choice due to the high volume requirement in manufacturing. DRAM and MPU have four possible technologies that could be used and that could extend the roadmap out to 11 nm half-pitch. These were all ranked at each year for their desirability and feasibility as solutions. EUV lithography is the lead candidate because of its lower cost of ownership (COO). Second is extending 193 immersion double patterning down to a k1 of 0.15 for 22 nm half-pitch, followed by maskless lithography (ML2) and imprint lithography. Alpha and soon beta tools are being delivered to the semiconductor industry for evaluation and further development using all of these approaches. In many cases, the technology is not limited by the lithography tool, but rather by the supporting technologies.

DIFFICULT CHALLENGES < 16 NM VERSUS TECHNOLOGY

The difficult challenges moving into the NGL regime are many and are not just incremental improvements in the technologies that we know and understand. The technology options are still vast, and in many cases the technology and the supporting infrastructure technologies need significant inventions to approach the manufacturing stage. The Difficult Challenges table for ≤16 nm shows the major challenges that must be solved to bring NGL technologies to the manufacturing stage. These challenges are listed in the order of perceived difficulty. For EUV lithography at 16 nm, defect free masks, sources brightness, and optimal resist system are key components needing substantial improvements. All three components will be further challenged as requirements for <16 nm will be tightened. In addition, the NA for the exposure system will be required to be increased which will bring a different set of challenges. The incidence angles may be required to be increased which will require thinner absorber thicknesses and flare mitigation. It is not clear how much the increase in the source power may cause additional challenges to the substrate in term of thermal management. Any other lithography enhancement techniques such as double pattern may be considered for deep sub 16 nm nodes.

EUV printing defect can derive not only from the traditional opaque defect in the patterning layer but also from small phase defects on the EUV substrate or a phase defect generated in the multilayer of the reflective blank. These phase defects are beyond the limits of today's metrologies and as such are very difficult to observe and improve upon. Currently, the infrastructure inspection equipment (substrate, blank, patterned mask, AIMs) needed for EUV mask manufacturing at the 16 nm node does not exist.

Maskless lithography is another NGL technology that must overcome major challenges before being considered a manufacturing technology. Foremost is the system throughput combined with the resist sensitivity that will also provide adequate LWR and resolution. This is both a system issue with respect to the e-beam flux and a resist material issue. ML2 is listed as possible lithography option for <16 nm DRAM/MPU and Flash. There is significantly higher throughput to price challenge for Flash than logic due to its high volume requirement in manufacturing. The second most pressing concern for ML2 is the inability to inspect wafer images at the same capability that we now have for 4× mask patterns. Inspection involves two issues: the resolution of the wafer inspection (at sufficient speed) and die-to-database inspection to ensure no systematic recurring defects are present.

Imprint lithography has three major needs: 1× masks, imprint materials, and imprint systems. The 1× mask has many areas contributing to difficult obstacles. First is mask inspection. The mask must be inspected to find defects in the 1× pattern that are just 10% of the width of the feature. An e-beam system might be able to do this but not at the speeds needed for manufacturing. Second is the write time to expose the slower speed e-beam resists to meet the LWR and CD specifications for 1× patterning. Third, 1× defect sizes are 4× smaller than what current 4× optical mask processes require; therefore, imprint template and e-beam resist patterning processes need to be developed to match these specifications. Another challenge is that the imprint materials must be of sufficiently low viscosity to be applied quickly for sufficient throughput. The last major challenge is with the imprint system. The lithography community believes that

throughput; defect levels, and overlay all need a significant improvement for the technology to be accepted in manufacturing.

Although there are many near-term challenges, the industry is addressing them. Lithographic systems are being made to run at throughputs that are about 2× the throughput of older steppers, thus addressing some of the COO issues associated with double patterning. Registration and overlay issues with lithographic mask patterning systems are also being addressed to move double patterning into manufacturing. The industry is likewise addressing the fundamental challenges associated with the NGL technologies, in particular the EUV lithography and the mask infrastructure that is needed. With these gains, the lithography industry will be back on course for improving ROI into the future.

Table ITWG9A Lithography Difficult Challenges ≥ 16 nm—Updated

Difficult Challenges > 16 nm	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features Registration, CD, and defect control for masks Eliminating formation of progressive defects and haze during exposure Understanding and achieving the specific signature and specifications for a Double Patterned mask Establishing a stable process so that signatures can be corrected.
Double and multiple patterning	Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs Availability of high productivity scanner, track, and process to maintain low cost-of-ownership Photoresists with independent exposure of multiple passes Fab logistics and process control to enable low cycle time impact that efficient scheduling of multiple exposure passes.
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time ROI for small volume products Resources for developing multiple technologies at the same time Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume 450 mm diameter wafer infrastructure if at 16 nm
Process control	New and improved alignment and overlay control methods independent of technology option to <5.7 nm 3σ overlay error Controlling LER, CD changes induced by metrology, and defects < 10 nm in size Greater accuracy of resist simulation models Accuracy of OPC and OPC verification, especially in presence of polarization effects Lithography friendly design and design for manufacturing (DFM)
EUV lithography	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components Cost control and return on investment Resist with < 1.5 nm 3s LWR, < 10 mJ/cm2 sensitivity and < 20 nm ½ pitch resolution Fabrication of Zero Printing Defect Mask Blanks Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection) Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs) Controlling optics contamination to achieve > five-year lifetime Protection of EUV masks from defects without pellicles Fabrication of optics with < 0.10 nm RMS figure error and < 7% intrinsic flare

Table ITWG9B Lithography Difficult Challenges <16 nm—Updated

Difficult Challenges <16 nm	*Summary of Issues*
EUV lithography—extendibility	Increased in NA
	Higher source power is needed to meet the throughput requirement
	Possible double patterning needed.
	Possibly new resist needed.
	Change of incident angle
	Different LTEM and absorber material to deal with high source power and heating
	Flare
Resist materials	Limits of chemically amplified resist sensitivity for <16 nm half pitch due to acid diffusion length
	Materials with improved dimensional and LWR control add (limits)
	Resist and antireflection coating materials composed of alternatives to PFAS compounds
	Low defects in resist materials (size <10 nm)
	Line width roughness <1.4 nm 3 sigma
Mask fabrication	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair)
	Increasingly long mask write and cycle time
	Mask process control methods and yield enhancement
	Cost control and return on investment
	Required degree of complexity with computational Lithography
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
	Development of cost-effective post-optical masks
	Cost effective 450 mm lithography systems
	Achieving ROI for small volume products
193 nm immersion multilple patterning	Cost control and return on investment
	Wafer processing to tighter overlay and CD controls
	Mask fabrication to tighter specifications
	Required degree of complexity with computational Lithography
	Increasing numbers of masks required.
Metrology and defect inspection	Defect inspection on patterned wafers for defects <20 nm
	Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3s
	Metrology for achieving <2.8 nm 3s wafer overlay error
	Template inspection for 1× Imprint Patterned Masks
	Phase shifting masks for EUV
CD control improvements and process control	Development of litho and post litho processes to control gate CD <1.5 nm 3s with <1.4 nm 3s line width roughness. Printed, post print process reduction, and final roughness
	Development of new and improved alignment and overlay control methods independent of technology option to achieve total <2.8 nm 3s overlay error on products.
Maskless lithography	Wafer throughput
	Cost control and return on investment
	Die-to-database inspection of wafer patterns written with maskless lithography
	Pattern placement—ncluding stiching
	Controlling variability between beams in multibeam systems
Imprint lithography	Defect-free Imprint templates at 1× dimensions
	Infrastructure for 1× technology templates (write, inspection, and repair)
	Template fabrication to tighter specifications
	Protection of imprint templates from defects without pellicles
	Throughput
	Cost control and return on investment
	Overlay
	Process control methods to compensate for systematic CD and overlay errors

INTERCONNECT

Link to the 2010 Interconnect update file.

Link to 2009 Interconnect chapter.

The Interconnect chapter of the ITRS addresses the wiring system that distributes clock and other signals to the various functional blocks of the integrated circuit, along with providing necessary power and ground connections. For 2008, the scope has been expanded to include the contact level and continues up through the device from metal 1 through to the global wiring levels. Traditionally, global wiring delay has been the "Grand Challenge" and tackling delay generally, is still a primary focus.

The current approach of the 2010 Interconnect TWG for addressing delay is to enable high-bandwidth low-power signaling solutions and a new table, INTC6 "High Density Through Silicon Via Specification" has been added. The group continues to project the use of copper as the primary conductor in a dual-damascene architecture; however, much of the work in progress focuses on the latest challenges and trends related to 3D integration and emerging technology.

- The Technology Requirements Table (INTC2) has been substantially revised and reorganized and divided into
  - general requirements – e.g., bulk resistivity and dielectric constant
  - level specific requirements determined by the nature of the wire or via geometry – e.g., barrier thickness or effective resistivity
- Low-k roadmap – small slowdown
  - New range for bulk κ
  - Air gaps moved out of emerging sections – considered mainstream
  - Air gaps expected to be the solution for $\kappa_{bulk} < 2.0$
- Atomic layer deposition (ALD) barrier processes and metal capping layers for Cu are lagging in introduction – needed to meet sub 1 nm specifications
  - Hybrid barriers containing ruthenium are proliferating
- J_{max} current limit model show a width dependence – a new reliability concern
- Technology drivers expanded to support both traditional geometric scaling and equivalent scaling
  - Requirements for CMOS-compatible equivalent scaling are highlighted in an expanded *Emerging Interconnect Properties* section along with a new first principle consideration of interconnect properties for new (non-FET) switches
- Design and processing of three-dimensional chip stacking through the use of high-density through silicon vias (TSVs) is a key focus area to address delay and power concerns and a new TSV table has been introduced

DIFFICULT CHALLENGES

Table ITWG10 Interconnect Difficult Challenges--Updated

Five Most Critical Challenges ≥ 16 nm	*Summary of Issues*
Material Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Manufacturable Integration Engineering manufacturable interconnect structures, processes and new materials	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Reliability Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Metrology Three-dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Cost & Yield for Manufacturability Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Five Most Critical Challenges < 16 nm	*Summary of Issues*
Material Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Metrology Three-dimensional control of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Process Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Complexity in Integration Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Practical Approach for 3D Identify solutions which address 3D structures and other packaging issues	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

CMP—chemical mechanical planarization DRAM—dynamic random access memory

FACTORY INTEGRATION

Link to 2010 Factory Integration update file.

Link to 2009 Factory Integration chapter.

The Factory Integration (FI) ITWG identifies needed operational factory services and relevant technologies, and it updates the near term and longer term technology requirements and potential solutions to meet these requirements. The Factory Integration ITWG has five thrust teams and their technology focuses are shown in the following table.

Functional Area	*Key technology focuses and issues*
Factory Operations (FO)	1) Systematic productivity improvement methodology prior to 450 mm insertion 2) Systematic factory waste visualization of cycle times and factory output losses
Production Equipment (PE)	1) 450 mm production tool development 2) Reliable and predictable equipment availability improvement 3) Energy conservation/management in process tools
Material Handling Systems (MHS)	1) Reduction in average material delivery times 2) More interactive control with FICS and PE for accurate scheduled delivery
Factory Information and Control Systems (FICS)	1) Increased FICS reliability performance for more complex factory control 2) Enhanced system extendibility
Facilities	1) Enhanced extendibility for 450 mm and facility cost reduction 2) AMC management, electric static control on masks, wafers, and facility surfaces

NGF TECHNOLOGY REQUIREMENTS INCLUSION

The FI focus areas activity concluded that a significant productivity improvement as NGF is to be promoted before 450 mm introduction. NGF is best described as systematic waste reduction approach that should facilitate comprehensive productivity improvement with the aid of proactive service visibility. NGF can be loaded with the so-called 300 mm Prime mission as well. The industry can focus on common technology development for the current wafer diameters and 450 mm.

WASTE REDUCTION MANAGEMENT

Waste reduction approach has been identified as the effective NGF driver. The ultimate goal for waste reduction is that all the technology requirements tables in the ITRS roadmap adopt waste reduction scheme, i.e., as a new driving axis in addition to the historic Si scaling cost reduction. Two high-level waste metrics have been introduced to promote this approach into Factory Operation technology requirements table. They are factory wait time waste (WTW) defined as a total sum of wait time for a wafer to go through all the process and factory equipment output waste (EOW) defined as opportunity loss of production calculated as normalized difference between instantaneous throughput and averaged throughput.

CROSS CUT ISSUES

Green fab initiatives, advanced process control (APC), fab temperature and humidity control, single wafer versus batch processing for thermal processes and 450 mm cross-cut issues are reflected to the requirements and solutions tables.

2010 HIGHLIGHTS

The FI team continues to focus on factory issues that are driven by cost, quality, productivity, and speed. Good progress has been made in developing the metrics and identifying potential solutions for these key drivers.

A major initiative in 2010 for the FI team was a focused effort on energy conservation and management. Energy consumption has become an increasingly important topic of public discussion in recent years because of global CO_2 emission and to reduce cost. An energy workshop was held in July 2010 to map and study the energy-related issues. The output of this workshop was a better understanding the challenges and an initial definition of the scope of work for the FI team in 2010/11. Working with other ITWGs, FI will start defining the metrics, challenges, key focus areas, and potential solutions, including more efficient process flows, reducing waste and improving energy use at the equipment level.

A logical progression might be: (i) baseline existing fab energy consumption at whatever level of granularity seems reasonable; (ii) identify challenges, potential solutions, and key focus areas and hence potential scope for energy reduction, and (iii) map this into technology tables for future years. The team also decided to start development of baseline process for generating metrics. Specifically, this will be used for the following:

- Define a generic process flow
- Benchmarking/data quality
- Development of 300 mm/450 mm fab model for energy and related modeling/simulation

Table ITWG10 Factory Integration Difficult Challenges—Updated

Difficult Challenges through 2017	*Summary Of Issues*
1. Responding to rapidly changing, complex business requirements	• Increased expectations by customers for faster delivery of new and volume products (design → prototype and pilot → volume production)
	• Rapid and frequent factory plan changes driven by changing business needs
	• Ability to load the fab within manageable range under changeable market demand
	• Enhancement in customer visibility for quality assurance of high reliability products
2. Managing ever increasing factory complexity	• Quickly and effectively integrating rapid changes in process technologies
	• Increased requirements for high mix factories. Examples are (1) significantly short life cycle time of products that calls frequent product changes, (2) the complex process control as frequent recipe creations and changes for process tools and frequent quality control criteria due to small lot sizes
	• Manufacturing knowledge and control information need to be shared as required among factory operation steps and disparate factories
	• Need to concurrently manage new and legacy FICS software and systems with increasingly high interdependencies
	• Ability to model factory performance to optimize output and improve cycle time for high mix factories
	• Need to manage clean room environment for more environment susceptible processes, materials, and, process and metrology tools
	• Comprehending increased purity requirements for process and materials
3. Achieving growth targets while margins are declining	• Ability to visualize cost and cycle time for systematic waste reduction from all aspects.
	• Reducing complexity and waste across the supply chain; reducing white space in cycle times
	• Minimize the cost of new product ramp up against the high cost of mask sets and product piloting
4. Meeting factory and equipment reliability, capability and productivity requirements per the Roadmap	• Increased impacts that single points of failure have on a highly integrated and complex factory
	• More equipment reliability, capability and productivity visualization that can be used bidirectionally between equipment suppliers and users for more efficient task sharing
	• Design-in of equipment capability visualization in production equipment; design-in of APC to meet quality requirements
	• Equipment supplier roadmap for equipment quality visualization and improvement, and, reduction of Equipment Output Waste.
	Reduction of equipment driven NPW (non-product wafers) operations that compete for resources with production wafers and Dandori operations[1]
	• Moving from reactive to predictive paradigm for scheduling, maintenance and yield management
5. Emerging factory paradigm and next wafer size change	• Uncertainty about 450 mm conversion timing and ability of 300 mm wafer factories to meet historic 30% cost effectiveness.
	• Uncertainty concerning how to reuse buildings, equipment, and systems to enable 450 mm wafer size conversion at an affordable cost

Table ITWG10 Factory Integration Difficult Challenges (continued)—Updated

Difficult Challenges Beyond 2017	*Summary of Issues*
1. Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	• Ability to utilize task sharing opportunities to keep the manufacturing profitable such as manufacturing outsourcing
	• Enhanced customer visibility for quality assurance of high reliability products including manufacturing outsourcing business models
	• Scalability implications to meet large 300 mm factory needs [40K–50K WSPM]
	• Cost and task sharing scheme on industry standardization activity for industry infrastructure development
2. Managing ever increasing factory complexity	• Higher resolution and more complications in process control due to smaller process windows and tighter process targets in many modules
	• Complexity of integrating next generation lithography equipment into the factory
	• More comprehensive traceability of individual wafers to identify problems to specific process areas
	• Comprehensive management that allows for automated sharing and re-usages of complex engineering knowledge and contents such as process recipes, APC algorithms, FD and C criteria, equipment engineering best known methods
	• Linking yield and throughput prediction into factory operation optimization
	• Real-time simulation in lock-step with production for operations prediction
3. Increasing global restrictions on environmental issues	• Need to meet regulations in different geographical areas
	• Need to meet technology restrictions in some countries while still meeting business needs
	• Comprehending tighter ESH/Code requirements
	• Lead free and other chemical and materials restrictions
	• New material introduction
4. Post-conventional CMOS manufacturing uncertainty	• Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements on factory design
	• Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition
	• Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency

Notes for Table ITWG10
[1] Dandori operations Peripheral equipment related operations that are in parallel or in-line and prior to or following to the main thread PE operations. So-called in-situ chamber cleaning is another good example than NPW operations.

ASSEMBLY AND PACKAGING

Link to the 2010 Assembly and Packaging update file.

Link to 2009 Assembly and Packaging chapter.

The 2010 update of the Assembly and Packaging Chapter incorporates into our tables the major addition to the contained in the 2009 Edition. Many changes in the text and tables were driven by the rapid changes in three dimensional electronics and System in Package (SiP) architecture. The work for 2010 was focused on preparation for major changes to be incorporated in the 2011 edition, which will include expanded coverage of automotive electronics, optical component packaging including optical fiber data paths, LED packaging, and photovoltaic packaging requirements.

The materials used in packaging have had a major change in this decade with 100% of the packaging materials undergoing significant change. This will be followed in the next decade with half of the materials changing again as we adopt new nano-materials, new molecules, and complex composite materials. The section on materials will provide expanded coverage to address these new materials.

The expansion of 3D architectures for packaging poses unique challenges that are not encountered in conventional 2D packaging. These include:

- Thinning wafers and die, and the handling of these thinned wafer and die
- Thermal management when several layers of semiconductor devices are stacked
- Power delivery and the maintenance of power integrity as the operating voltages are dropped to near the threshold voltage
- Testing for 3D structures when test access is a challenge

These and other challenges are reflected in our Difficult Challenges table. There were no major changes in other tables for 2010. Minor changes to existing tables will be included in our 2011 edition. The Assembly and Packaging is also in the process of updating our System in Package paper which should be complete in early 2011. This update will reflect the significant changes made in SiP technology since the original publication of the paper. The growth of SiP and 3D integration results in a greater dependence on the cross-TWG interactions. This will be reflected in the major rewrite for 2011 which will include:

- Joint efforts with the Design ITWG to address the needs for design and simulation tools to address needs of 3D and deep sub-micron package requirements. The goal will be to perform the development cycles in the computer and avoid the cost and time required for multiple physical prototypes of each new product.
- Joint efforts with the Emerging Research Materials and Emerging Research Devices ITWGs to meet the materials properties required for new packaging and accommodate the packaging requirements for new device types as replacements for conventional CMOS are introduced.
- Joint efforts with the Test ITWG to define package architectures and test solutions that will satisfy the requirements to ensure quality and reliability for these new packages types particularly in 3D and for very high frequencies.
- Joint efforts with the Interconnect ITWG to ensure that we coordinate the interface between the global interconnect architecture and package interconnect architecture and identify a consistent set of challenges and potential solutions in the overlap areas.

DIFFICULT CHALLENGES

Innovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices. Near-term difficult challenges exist in all phases of the assembly and packaging process from design through manufacturing, test, and reliability.

Many critical technology requirements are yet to be met and they are listed in Table ITWG11 below. Meeting these requirements will demand significant investment in research and development.

Table ITWG11 Assembly and Packaging Difficult Challenges ≥16 nm—Updated

Difficult Challenges ≥16 nm	*Summary of Issues*
Impact of BEOL including Cu/low κ on packaging	-Direct wire bond and bump to Cu or improved barrier systems bondable pads - Dicing for ultra low k dielectric -Bump and underfill technology to assure ultra low-κ/ air gap dielectric integrity -Improved fracture toughness of dielectrics -Interfacial adhesion -Reliability of first level interconnect (increasing with decreasing contact pitch) -Mechanisms to measure the critical properties (particularly for thin layers and interfaces)
Wafer level Packaging	-Redistribution processing for pad pitch below 50 μm -Thermal management (for high power devices used in automotive and other areas) -Wafer thinning and handling technologies -TCE mismatch compensation for large die
Coordinated design tools and simulators to address chip, package, and substrate co-design	-Models for Reliability prediction -Rapid turn around modeling and simulation -Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis -Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) -System level co-design(cm to nm) is needed now (including mixed signal and simulation). -EDA for "native" area array is required to meet the Roadmap projections.
Embedded components	-Low cost embedded passives: R, L, C -Embedded active devices -Quality levels required not attainable on chip -Die size for high C, low L integrated circuit matching die size -Wafer level embedded components
Thinned die packaging	-Wafer/die handling for thin die (must address die warpage) -Reliability -stress impact on device performance and assembly yield -Interconnect thickness and bonding for die stacking -Testability (ohmic contacts without damage)

The Difficult Challenges for <16nm reflect the fundamental changes associated with continued scaling. The list is relatively short but the challenges are complex and will require substantial innovation.

Table ITWG11 Assembly and Packaging Difficult Challenges<16nm—Updated

Difficult Challenges < 16 nm	*Summary of Issues*
Close gap between chip and substrate	-Increased wireability at low cost -Improved impedance control and lower dielectric loss to support higher frequency applications -Improved planarity and low warpage at high process temperatures -Low-moisture absorption -Increased via density in substrate core -Production techniques will require silicon-like production and process technologies
High current density packages	-Electromigration will become a more limiting factor. -Thermal dissipation
Post CMOS switch devices	-The structures and materials employed will present serious challenges for packaging that will need to be addressed during this Roadmap period. The specifics of the requirements and challenges are not known at this time.

ENVIRONMENT, SAFETY, AND HEALTH

Link to the 2010 Environment, Safety, and Health update file.

Link to 2009 ESH chapter.

The four basic ITRS ESH chapter strategies in 2010 remain as they were in the previous edition; namely:

1) Understand (characterize) processes and materials during the development phase;

2) Use materials that are less hazardous or whose by-products are less hazardous;

3) Design products and systems (equipment and facilities) that consume less raw material and resources and,

4) Make the factory safe for employees.

The significant new element added in 2009 was retained in 2010 for further validation, which is the addition of ESH Categories. Previous ESH chapter tables presented a requirements set that related ESH concerns to the technical thrusts (e.g., Interconnect, Front End Processes, etc.). They also identified ESH concerns that are broader and more general than those pertaining to a single technology thrust (referred to as "intrinsic").

To focus available resources toward those areas of greatest added benefit, in addition to the ESH improvements gained, all ESH requirements have now been placed in one of three Categories:

1. *Critical*—Any requirement in this category is an essential item for technology success/implementation as well as ESH benefits. If not addressed, it could compromise the ability to insert the technology into manufacturing.
2. *Important*—Any requirement in this category is a key item for process success as well as ESH benefits. If not addressed, it could compromise the cost of ownership (CoO) of the technology in manufacturing, based on factors such as throughput, yield, and chemical/material and/or tool costs.
3. *Useful*—Any requirement in this category is a key item for ESH benefits ("best practices"), but without any clear additional factors that would place it in either of the above two categories. If not addressed, it could compromise the ability to achieve the lowest ESH impact for the technology when inserted into manufacturing.

Some minor corrections to the tables were made in the 2010 revision, which include some simple word changes to add clarity to the intent of ESH technical requirements and correction of errors found in metric definitions so they match the associated values in technology requirements.

For 2011 two critical areas, both focused on materials, will be where efforts are concentrated. The first is defining research needs that decrease polarization of public/government policy expectations versus future technology needs, where critical materials are needed or new materials required to assure future technology. The second area is determining how to specify technology requirements in non-quantifiable or non-data supported terms where data do not exist, are not representative, or do not have granularity for defining a technical objective—while the objective remains important for ESH.

Table ITWG12 ESH Difficult Challenges ≥16 nm—Updated

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials can be utilized (without delay) in manufacturing, while protecting human health, safety, and the environment. Given the global movement possible for R&D, pre-manufacturing, and full commercialization, these methodologies must recognize regional regulatory /policy differences and the overall trends towards lower exposure limits and increased monitoring. • *Chemical Data Availability*: There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use In addition, methods for anticipating and forecasting such future requirements are not well developed.. • *Chemical Exposure Management*: There is incomplete information on how chemicals/materials are used and the process by-products formed. Also, while methods used to obtain such information are becoming more standardized, their availability varies depending on the specific issue being addressed, and can use improvement.
Process and equipment management	• *Process Chemical Optimization* There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). • *Environment Management* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations (including the capability for component isolation in waste streams) for such hazardous and non-hazardous emissions and by-products can be addressed. Global Warming Emissions Reduction: There is a need to limit emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Water and Energy Conservation* There is a need for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization* There is a need for more efficient chemical/material utilization, with improved reuse/recycling/reclaiming of them and their process emissions and byproducts. • *Byproducts Management*: There is a need for improved metrology for byproduct speciation. • *Chemical Exposure Management* There is a need to design-out chemical exposure potentials and the requirements for personal protective equipment (PPE) • *Design for Maintenance* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities use, and for more efficient cleanrooms' and facilities systems' thermal management. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics* There is a need for methodologies to define and measure a technology generation's sustainability. • *Design for ESH* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes and products. • *End-of-Life Reuse/Recycle/Reclaim* There is a need to design facilities, equipment and products to facilitate these end-of-life issues

Table ITWG12 ESH Difficult Challenges <16 nm—Updated

Difficult Challenges < 16 nm	*Summary of Issues*
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials can be utilized (without delay) in manufacturing, while protecting human health, safety, and the environment. • *Chemical Data Availability*: There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use • *Chemical Exposure Management*: There is incomplete information on how chemicals/materials are used and the process by-products formed.
Process and equipment management	· Chemical Reduction: There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). There is a need to limit emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Environment Management* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations for such hazardous and non-hazardous emissions and by-products can be addressed. • *Water and Energy Conservation* There is a need to reduce water and energy consumption, and for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization* There is a need for more efficient chemical/material utilization, with their increased reuse/recycle/reclaim (and of their process emissions and byproducts). • *Chemical Exposure Management* There is a need to design-out chemical exposure potentials and personal protective equipment (PPE) requirements. • *Design for Maintenance* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities use, and for more efficient cleanrooms' and facilities systems' thermal management. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics* There is a need for methodologies to define and measure a technology generation's sustainability, and also sustainability at a factory infrastructure level. • *Design for ESH* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes and products, with methodologies to holistically evaluate and quantify the ESH impacts of facilities operations, processes, chemicals/materials, consumables, and process equipment for the total manufacturing flow. • *End-of-Life Reuse/Recycle/Reclaim*: There is a need to design facilities, equipment and products to facilitate these end-of-life issues

YIELD ENHANCEMENT

Link to 2010 Yield Enhancement update file.

Link to 2009 Yield Enhancement chapter.

The key challenges were adapted to latest developments and challenges recognized by the 2010 Yield Enhancement ITWG. Currently, the most important key challenge will be "detection and identification of small yield limiting defects from nuisance." It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership, and high throughput. Furthermore, it is a challenge to identify yield-relevant defects under a vast amount of nuisance and false defects. In the long term the requirements for next generation inspection were identified.

Other topics challenging the yield enhancement community are prioritized as follows in the near term:

- *Detection and identification of small yield limiting defects from nuisance*—Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.
- *Non-visual defects and process variations*–Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.
- *3D inspection*—For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases.
- *Process stability versus absolute contamination level including the correlation to yield test structures*—Methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water, and substrate surface cleanliness.

In the long term the following key challenges are currently identified:

- *Next generation inspection*—As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm. Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy; near-field scanning optical microscopy; interferometry; scanning capacitance microscopy, and e-beam. This path finding exercise needs to assess each technique's ultimate resolution, throughput, and potential interactions with samples (contamination or degree of mechanical damage) as key success criteria.
- *In-line defect characterization and analysis*—Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and energy dispersive x-ray spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.
- *Development of model-based design-manufacturing interface*—Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.

The Yield Enhancement chapter consists of two active subchapters—"Defect Detection and Characterization," and "Wafer Environment and Contamination Control (WECC)." Two subchapters are currently not active for "Defect Budget" and "Yield Model and Yield Learning." The major work during 2010 was the control and update of the tables. The changes summarizes as follows.

- Defect Budget and Yield Model
  - In 2010 a new initiative collecting data from a defect budget survey of manufacturing sites in Japan, United States, and Europe was started. The aim of the survey is to supply defect density data for processes and equipment.
- Defect Detection and Characterization
  - The tables YE 4, YE5 and YE6 were checked carefully against latest developments for defect inspection and detection.
- Wafer Environment and Contamination Control
  - The table YE 7 was extended and checked carefully.

Table ITWG14 Yield Enhancement Difficult Challenges ≥ 16 nm—Updated

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Detection and identification of Small Yield Limiting Defects from Nuisance - Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.	Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. Reduction of inspection costs and increase of throughput is crucial in view of CoO. Detection of line edge roughness due to process variation. Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. Reduction of background noise from detection units and samples to improve the sensitivity of systems. Improvement of signal to noise ratio to delineate defect from process variation. Where does process variation stop and defect start?
Non-Visual Defects and Process Variations – Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.	Systematic Mechanisms Limited Yield (SMLY), resulting from unrecognized models hidden in the chip, should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. It is required to manage the above models at both the design and manufacturing stage. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis runs time per die. d) Statistical methodology to analyze results of logic diagnosis for denoising influence of random defects and building a layout-dependent systematic yield model. Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic yield loss, and has to improve their coverage.
3D Inspection – For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases.	Detection of non visible defects e.g. voids, embedded defects, and sub surface defects in the structures. The demand for high-speed and cost-effective inspection is crucial. Large number of contacts and vias per wafer E-beam inspection seems not to be the solution for all those tasks any more. Sensitivity of the inspection tool to process variation and definition of maximum process variation (control limits).
Process Stability vs. Absolute Contamination Level – Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect.
Wafer Edge and Bevel Monitoring and Contamination Control – Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems.	Currently, the monitoring and contamination control methods require intensive development.

Table ITWG14 Yield Enhancement Difficult Challenges <16 nm—Updated

Difficult Challenges < 16 nm	*Summary of Issues*
Next Generation Inspection - As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm node.	Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This path finding exercise needs to assess each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.
In - line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality. [1]	Data volume + quality: strong increase of data volume due to miniaturization The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. It will be recommended to supply information on chemical state and bonding especially of organics. Small volume technique adapted to the scales of technology generations. Capability to distinguish between the particle and the substrate signal.
Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	A lot of models should be operated at the design stage. For example, Optical Proximity Correction, Well Proximity, Stress Proximity, CMP and so on The Amount of models seems to be rapidly increasing. Not only accuracy of models, but also optimization of trade-off between models might be requested. Development of test structures for new technology generations

METROLOGY

Link to 2010 Metrology update file.

Link to 2009 Metrology chapter.

2009 SUMMARY

Metrology requirements continue to be driven by advanced lithography processes, new materials, and Beyond CMOS materials, structures, and devices. The introduction of dual patterning and double exposure lithography add the complexity of measuring two distributions of linewidth, sidewall angle, and line width roughness inside the same measurement area. Another key challenge to critical dimension metrology is tool matching. Precision requirements for the next several years can be met using single tools. There are many gaps in metrology for EUV lithography especially for mask metrology. The entire mask fabrication process needs advances in capability especially for actinic patterned mask inspection and aerial imaging. Overlay metrology capability lags behind the need for improved overlay control. Front end processes continue to drive metrology to provide measurements for new higher dielectric constant materials, dual work function metal gates, and new ultra shallow junction doping processes. The sub 1 nm EOT gate stacks require greatly improved film thickness and composition control during manufacturing. Interconnect structures continue the cycle of new materials. The need for porosity control for low k materials has driven a renewed interest in porosity measurements. 3D interconnect metrology requirements are largely driven by the activity in through silicon vias (TSV) R&D. Bonded wafer overlay control for next generation TSV now has potential solutions that are under investigation. In the area of metrology for Beyond CMOS R&D, graphene measurements have advanced in the areas of microscopy and electrical characterization. In addition, there are now several means of determining the number of graphene layers in a sample. The need for understanding large area graphene uniformity is driving both physical and electrical metrology. In addition, metrology R&D is working with other Beyond CMOS materials.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 22 nm technology generation. Metrology needs after 2015 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table ITWG15 presents the ten major challenges for metrology.

Table ITWG15 Metrology Difficult Challenges

Difficult Challenges ≥16 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of new process technology such as Dual Patterning Lithography, complicated 3D structures such as capacitors and contacts for memory, and 3D Interconnect are not ready for their rapid introduction.	Overlay measurements for Dual Patterning have tighter control requirements. Overlay defines CD. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures including capacitors, devices, and contacts.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges <16 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks. Sampling plan optimization is key to solve these issues.
Statistical limits of sub-32 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for *beyond CMOS.*	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

* *SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

MODELING AND SIMULATION

Link to 2010 Modeling and Simulation update file.

Link to 2009 Modeling and Simulation chapter.

SUMMARY

Modeling and Simulation software tools span the entire semiconductor world. These tools are being used daily with increasing efficiency. The Modeling and Simulation (M&S) chapter of the ITRS presents specific needs to increase this effectiveness and to provide impact on the semiconductor industry in the future. Similar to the other chapters of the ITRS, in the Modeling and Simulation chapter only the tables have been revised in the 2010 Update. Besides this, the preparations for the next full version of the ITRS, the 2011 edition, have been started. Again in 2010, much effort has been spent on the analysis of the requirements of the other chapters towards the Modeling and Simulation chapter, based on face-to-face meetings with other ITWGs in the ITRS and the extraction of relevant material from their documents This analysis has on one hand been used as background and input for the discussions on the 2010 update of the Modeling and Simulation tables, and on the other hand will be further updated throughout 2010 and until the edit deadline of the 2011 ITRS, to serve as a key input to the 2011 Modeling and Simulation chapter.

Concerning the *Modeling and Simulation Difficult Challenges*, mainly the scope of the challenge on integrated modeling from equipment through devices was extended. It now reads "Integrated modeling of equipment, materials, feature scale processes and influences on device and circuit performance and reliability, including random and systematic variability". Especially, it now additionally includes "Pattern/microloading effects in radiative annealing or plasma processing" and "Propagation of process variations into circuit block simulation". Besides this, several details were updated in the other challenges, among others due to the selection of favourable options for beyond CMOS devices by the ERD ITWG.

The table *"Modeling and Simulation Technology Requirements: Capabilities—Near-term Years"* again summarizes the needs in the areas of process, device, circuit and package simulation, and includes premier general requirements on tools. The most important changes are as follows: Concerning *lithography simulation*, "Innovative 193 nm immersion multiple patterning" was included, due to the prioritization of technological options by the Lithography ITWG. In the requirements *for numerical device modeling*, the simulation of random device variability was added as a new requirement for device modeling in 2010, especially concerning the efficient inclusion in commercial simulation tools. Several items have been delayed by one year due to the state-of-the-art not yet meeting the needs.

Compared to this the M&S table on "*Modeling and Simulation Technology Requirements: Capabilities—Long-term Years*" is far less detailed, because long-tem technology options are so far only partly defined or prioritized in the other parts of the ITRS. Generally, this long-term requirements table contains a majority of "*red" items* for which so far no solutions are known. Partly this is due to the fact that the technological options are not yet known or prioritized, and in turn also simulation approaches can not yet be developed or selected. Another problem is the inherent difficulty to develop models and tools to meet the ambitious requirements—in turn, the success of the development work required from M&S cannot be predicted ten or more years in advance.

The table on *"Modeling and Simulation Technology Requirements: Accuracy—Near-term Years"* is quite similar to the other requirement tables grouped into lithography modeling, front end process modeling, topography modeling, numerical device modeling, circuit element modeling/ECAD, and package modeling. Here, the estimate of about one third, given for the cost and time reduction from use of TCAD in best practice cases reported by industry, is based on an industrial survey already discussed in the 2008 ITRS. In this table, accuracy refers to models and tools calibrated to a certain technology (at a company), <u>not</u> to a certain experiment. Most accuracy specifications are given as percent of the respective nominal value or of some top-level parameter of the respective technology node, e.g., the physical gate length. A key issue in the preparation of this table has been how to define the accuracy of simulation when comparing with experiment which themselves have a significant inaccuracy or uncertainty. Detailed definitions made are listed in the footnotes of the table, e.g., "compared with median value of statistically meaningful samples". Furthermore, the table does not only specify the required accuracy in the simulation of nominal values like a junction depth, but also the accuracy of the sensitivity of such values with respect to changes in process conditions. This is important for tracing the impact of process variations through a simulation sequence, as requested in M&S subchapter on "Modeling for Design Robustness, Manufacturing and Yield" of the 2009 ITRS. In the 2010 Update, some details were changed in the definition of the items specified, compared with the 2009 ITRS. Furthermore, the specification for *gate 2D/3D topography accuracy* has been identified as somewhat duplicating the other topography specifications, and has therefore been skipped. For the error of the output characteristics of devices, in the 2010 Update no more difference is made between the saturation and the linear region. Some changes compared to the 2009 ITRS in the absolute accuracies specified are due to slight modifications of top-level ITRS specifications, like printed gate length, late in the 2009 process.

Table ITWG16 Modeling and Simulation Difficult Challenges—Updated

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Lithography simulation including EUV	Models and experimental verification of optical and non-optical immersion lithography effects (e.g., topography and change of refractive index distribution)
	Simulation of multiple exposure/patterning including database splitting
	Multi-generation lithography system models
	Simulation of defect influences/defect printing in EUV. Mask optimization including defect compensation
	Optical simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including extensions for inverse lithography
	Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects
	Predictive and separable resist models (e.g., mesoscale models) including line-edge roughness, accurate profiles, topcoat interactions, etch resistance, adhesion, mechanical stability, leaching, and time-dependent effects in in single and multiple exposure
	Resist model parameter calibration methodology (including kinetic and transport parameters)
	Fast, predictive simulation of ebeam mask making (single-beam and multibeam)
	Simulation of directed self-assembly of sublithography patterns
	Modeling lifetime effects of equipment and masks, including lens and mirror heating effects
	Predictive coupled deposition-lithography-etch simulation (incl. double patterning, self-aligned patterning)
	Modeling metrology equipment for enhancing its accuracy
Front-end process modeling for nanometer structures	Coupled diffusion/activation/damage/stress models and parameters including SPER and millisecond processes in Si-based substrate, that is, Si, SiGe, SiGe:C, Ge-on-Si, III/V-on-Si, SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers
	Diffusion in advanced gate stacks
	Predictive segregation and dose loss models
	Modeling of interface and dopant passivation by hydrogen or halogens
	Modeling of cluster or cocktail implants
	Modeling of plasma doping, e.g. for FinFETs. Predictive modeling of de-activation of dopants.
	Modeling of epitaxially grown layers: Shape, morphology, stress, defects, doping, diffusion, activation
	Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
	Efficient and robust 3D meshing for moving boundaries
	Modeling the impact of front-end processing-induced damage to devices on their leakage, noise and reliability bahavior during operation
Integrated modeling of equipment, materials, feature scale processes and influences on device and circuit performance and reliability, including random and systematic variability	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-) products, rates ...) , and simplified but physical models for complex chemistry and plasma reaction.
	Linked equipment/feature scale models (including high-κ metal gate integration, damage prediction)
	Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
	Spin-on-dielectrics (stress, poriosity, dishing, viscosity, …) for high aspect ratio fills
	Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
	Pattern/microloading effects in radiative annealing or plasma processing
	Propagation of process variations into circuit block simulation
	Simulation of polishing, grinding and wafer thinning in backend processes
	Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulations
Nanoscale device simulation capability: Methods, models and algorithms	General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra
	Efficient models and tools for-analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
	Models (incl. material models) to investigate new memory devices like STT-MRAM, nanoionic memories, PCM/PRAM, etc
	Gate stack models for ultra-thin/high-k dielectrics with respect to electrical permittivity, built-in charges, influence on workfunction by interface interaction with metals, reliability, tunneling currents and carrier transport

Difficult Challenges ≥ 16 nm	*Summary of Issues*
	Modeling of salicide/silicon contact resistance and engineering (e.g. Fermi-level depinning to reduce Schottky barrier height)
	Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure and dopant variations in order to assess the impact of variations on statistics of device performance
	Physical models for novel channel materials, e.g., Ge and compound III/V channels …: Band structure, defects/traps, ...
	Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation
	Reliability modeling for ultimate CMOS
	Device simulators (software) for STT and nanoionic memories
	Physical models for stress induced device performance
Electrical-thermal-mechanical-modeling for interconnect and packaging	Model thermal-mechanical, thermodynamic and electrical properties of low κ, high κ, and conductors for efficient on-chip and off-chip incl. SIP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension
	Thermal modeling for 3D ICs and assessment of modeling and CAD tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keepout regions, …). Size effects (microstructure, surfaces, ...) and variability of thinned wafers.
	Signal integrity modeling for stacked die
	Identify effects and apply/extend models which influence reliability of interconnects/packages incl. 3D integration (e.g., stress voiding, electromigration, fracture initiation, dielectric breakdown, piezoelectric effects)
	Physical models and simulation tools to predict adhesion and fracture toughness on interconnect-relevant interfaces (homogeneous and heterogeneous), packages and die interfaces
	Dynamic simulation of mechanical problems of flexible substrates and packages
	Models for electron transport in ultra fine patterned interconnects
Circuit element and system modeling for high frequency (up to-300 GHz) applications	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package: - possibly consisting of different technologies, - covering and combining different modelling and simulation levels as well as different simulation domains
	Scalable active component circuit models [1] including non-quasi-static effects, substrate noise and coupling, high-frequency RT and 1/f noise, temperature and stress layout dependence and parasitic coupling
	Scalable passive component models [1] for compact circuit simulation, including interconnect, transmission lines, …
	Scalable circuit models [1] for More-than-Moore devices including switches, filters, accelerometers, …
	Physical circuit element models for new memory devices, such as PCM, and standardization of models for III/V devices
	Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently
	Computer-efficient assessment of building block/circuit-level using process/device/circuit simulation, including process variations

Notes for Table ITWG16
[1] In More than Moore, scalability refers to the ability to model litho-defined device variations.

Table ITWG16 Modeling and Simulation Difficult Challenges <16nm—Updated

Difficult Challenges < 16 nm	*Summary of Issues*
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: 1) Layer stacks for gates, junctions and channels: Predictive modeling of dielectric constant, bulk polarization charge, ferroelectric/-magnetic properties, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. 2) Models for novel integrations in 3D interconnects including data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties 3) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. 4) Accumulation of databases for semi-empirical computation.
Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials	Ab-initio modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping, quantum dots, atomic electronics, multiferroic materials and structures, strongly correlated electron materials)
	Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …). Modeling impact of geometry, interfaces and bias on transport for carbon-based nanoelectronics
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, fast and efficient optical interconnect models of larger domains, semiconductor laser modeling
	Physical design tools for integrated electrical/optical systems
	Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects & impact on LER); heating and charging effects), including impact on device characteristics (e.g. due to local crystal damage by electron scattering or charging effects)
NGL simulation	Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

Notes for Table ITWG16
[1] In More than Moore, scalability refers to the ability to model litho-defined device variations.

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (ALSO WITH OBSERVATIONS AND ANALYSIS)

Moore's Law—An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that device affordability must be taken into account and also performance. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been recently acknowledged and celebrated as a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 40 years.

Scaling ("More Moore")—

- *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)* refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)* refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
    - "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures."
    - Addresses the need for quantifiable, specific Design Technologies that address the power and performance trade-offs associated with meeting "More Moore" functionality needs, and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—The incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

- Design technologies enable new functionality that takes advantage of More than Moore technologies.
- "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology."
- Addresses the need for design technologies which enable functional diversification

Beyond CMOS—emerging research devices, focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switch, NEMS switches, etc.

CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle

timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets.

MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

As defined above, additional "Equivalent Scaling" process technologies can be combined with transistor gate dimensional scaling technology advancement to further advance the performance and power-management characteristics of a device. The "Equivalent Scaling" technologies can also be "mix-and-matched" by companies within their specific product fabs. In some cases the most recent ITRS ITWG surveys have indicated that dimensional scaling (both gate length and gate material thickness) reduction can be slowed and still meet power management and performance requirements, when traded off with "equivalent scaling" process insertion.

Some (not comprehensive or complete) examples of "equivalent scaling" process and transistor design technology are: copper interconnect; low-K interconnect materials; strained silicon; high-K/metal gate; fully depleted silicon-on-insulator (FDSOI); multiple-gate 3-D transistors, III-V gate material; etc.

It should be noted that the timing of availability and implementation of "equivalent scaling" process insertion may not be as regular as dimensional cycles. See the Interconnect and process integration and device structures (PIDS) chapters for additional technology description and timing details.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to the "Moore's Law" driver of functions/chip doubling every two years , there has been a historically-based "corollary" to the "law," which suggests that, to be affordable and competitive, manufacturing productivity improvements must also enable the cost-per-function (micro-cents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 2 years, cost per function must also reduce by half every 2 years (-29%/year average). On average then cost-per-chip (packaged unit) , for affordability, could remain approximately constant (requires both flat chip cost targets and flat back-end packaging targets to remain constant), If functionality doubles only every three years, then the manufacturing cost per chip (packaged unit) can remain flat if the cost per function reduction rate slows to one-half every 3 years.(-21%/year average). It should be noted that this simplistic manufacturing cost affordability model, used as a first-order driver for the ITRS, does not take into account the economic supply and demand market complexity of actual external market environments.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A Flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two to four bits of data in the same physical area.

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two and level-three (L2 and L3) cache. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation.

High-performance MPU[2]—MPU product optimized for maximum system performance by combining a single or multiple CPU cores with large level-two and level-3 (L2 and L3) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory. Recently the typical pattern among MPU products is to keep the number of cores constant within a generation and double the number of transistors within each core, and the latest ITRS ORTC modeling reflects this trend in the table targets.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip had increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is still maintained, although the latest consensus ITRS forecast of cell-area-factor improvement to 4 by 2011, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate. Therefore, the latest ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The latest ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology generation processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology generation, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples.

Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2005 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (typically <1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

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[2] *Note: The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.*

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, 10K/month or higher, depending upon die size and wafer generation size) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 2a in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: .5 Gb/production, 4 G/introduction, plus 256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2009 ITRS, the typical high-performance ASIC (hpASIC) design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 74% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 56% at the production level, and also for shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=74% of total chip area, the $C_{AVE} = C/E = 0.35\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.35e-6 mm^2/bit = 376 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two to four bits in the same cell area, creating a multi-level-cell (MLC)

"virtual" per-bit size that is one-half to one-fourth the size of an SLC product cell size and will also have a "virtual area factor" that is half to one-fourth of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 10–15 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2–3 times greater than an SRAM 6t cell area factor, and 30–40 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology generation. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology generation. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology generation, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first production-qualified development manufacturing facilities. Additional clarification was added by the IRC in 2009 to differentiate the new 450 mm wafer generation early consortia pilot line equipment readiness from the timing of anticipated production readiness and ramp.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

APPENDIX—ITRS TABLES LISTING

Link to the 2010 Update webpage.

SYSTEM DRIVERS

	Table SYSD1	Major Product Market Segments and Impact on System Drivers
	Table SYSD2	SOC Consumer Driver Design Productivity Trends
	Table SYSD3	Projected Mixed-Signal Figures of Merit for Four Circuit Types
	Table SYSD4	Embedded Memory Requirements
	The System Drivers chapter did not have table updates. The following figures were updated for 2010:	
Updated	Figure SYSD5	SOC Consumer Portable Design Complexity Trends
Updated	Figure SYSD6	SOC Consumer Portable Power Consumption Trends
Updated	Figure SYSD7	SOC Consumer Portable Processing Performance Trends
Updated	Figure SYSD9	SOC Consumer Stationary Design Complexity Trends
Updated	Figure SYSD10	SOC Consumer Stationary Performance Trends
Updated	Figure SYSD11	SOC Consumer Stationary Power Consumption Trends

DESIGN		
	Design Chapter section update	Analog, Mixed-Signal and RF Specific DT Trends and Challenges
	Table DESN1	Overall Design Technology Challenges
	Table DESN2	System-Level Design Requirements
	Table DESN3	Correspondence Between System-Level Design Requirements and Solutions
	Table DESN4	Logical/Circuit/Physical Design Technology Requirements
	Table DESN5	Correspondence Between Logical/Circuit/Physical Requirements and Solutions
	Table DESN6	Design Verification Requirements
	Table DESN7	Correspondence Between Design Verification Requirements and Solutions
	Table DESN8	Design for Test Technology Requirements
	Table DESN9	Design for Manufacturability Technology Requirements
	Table DESN10	Correspondence Between Design for Manufacturability Requirements and Solutions
	Table DESN11	Design Technology Improvements and Impact on Designer Productivity
	The Design chapter did not have table updates. The following figure was updated for 2010:	
Updated	Figure DESN1	Impact of Design Technology on SoC SOC Consumer Portable Implementation Cost

TEST AND TEST EQUIPMENT		
Updated	Table TST1	Summary of Key Test Drivers, Challenges, and Opportunities
Updated	Table TST2	Multi-site Test for Product Segments
	Table TST3	"Stages" of Adaptive Test
	Table TST4	Implications of Adaptive Test

Test and Test Equipment		
Updated	Table TST5	System on Chip Test Requirements
Updated	Table TST6	Logic Test Requirements
	Table TST7	Vector Multipliers
Updated	Table TST8	Memory Test Requirements
	Table TST9	Mixed-signal Test Requirements
Updated	Table TST10	RF Test Requirements
	Table TST11	Burn-in Requirements
	Table TST12	Test Handler and Prober Difficult Challenges
	Table TST13	Prober Requirements
	Table TST14	Handler Requirements
Updated	Table TST15	Probing Difficult Challenges
Updated	Table TST16	Wafer Probe Technology Requirements
	Table TST17	Test Socket Technology Requirements

RF and AMS for Wireless		
Updated	Table RFAMS1	RF and Analog Mixed-Signal CMOS Technology Requirements
Updated	Table RFAMS2	RF and Analog Mixed-Signal Bipolar Technology Requirements
	Table RFAMS3	On-Chip Passives Technology Requirements
	Table RFAMS4	Off-Chip Passives Technology Requirements
Updated	Table RFAMS5	Power Amplifier Technology Requirements
Updated	Table RFAMS6	Base Station Devices Technology Requirements
Updated	Table RFAMS7	Millimeter Wave 10 GHz–100 GHz Technology Requirements
	Table RFAMS8	RF and Analog Mixed-Signal RFMEMS
Updated	Figure RFAMS2	0.4 GHz–10 GHz Potential Solutions
Updated	Figure RFAMS3	10 GHz–100 GHz Potential Solutions

Process Integration, Devices, and Structures (PIDS)		
	Table PIDS1	Process Integration, Devices, and Structures Difficult Challenges
	Table PIDS2	High-performance Logic Technology Requirements
Updated	Table PIDS3A	Low Standby Power Technology Requirements
Updated	Table PIDS3B	Low Operating Power Technology Requirements
Updated	Table PIDS4	DRAM Technology Requirements
Updated	Table PIDS5	NAND Flash Technology Requirements
	Table PIDS5A	Requirements for Spin-Torque Transfer (STT) MRAM
	Table PIDS6	Reliability Technology Requirements

Emerging Research Devices	
	Please refer to the ERD summary in the 2010 Update Overview with respect to the Future Memory Devices Workshop

EMERGING RESEARCH MATERIALS	
	Please refer to the ERM summary in the 2010 Update Overview with respect to the Future Memory Devices Workshop

FRONT END PROCESSES		
	Table FEP1	Front End Processes Difficult Challenges
	Table FEP2	High Performance Device Technical Requirements
	Table FEP3	Low Operating Power Device Technical Requirements
	Table FEP4	Low Standby Power Devices Techical Requirements
	Table FEP5	DRAM Stacked Capacitor Technology Requirements
	Table FEP6	Floating Gate FLASH Non-volatile Memory Technology Requirements
	Table FEP7	Charge Trapping FLASH Non-volatile Memory Technology Requirements
	Table FEP8	Phase Change Memory (PCM) Technology Requirements
	Table FEP9	FeRAM Technology Requirements
	Table FEP10	Starting Materials Technology Requirements
	Table FEP11	Front End Surface Preparation Technology Requirements
	Table FEP12	Thermal, Thin Film, Doping Process Technology Requirements
Updated	Table FEP13	Etching Process Technology Requirements
	Table FEP14	Shallow Trench Isolation CMP Process Technology Requirements
Updated	Figure FEP16	Surface Preparation Potential Solutions

LITHOGRAPHY		
	Table LITH1	Various Techniques for Achieving Desired CD Control and Overlay with Optical Projection Lithography for MPU and DRAM
Updated	Table LITH2A	Lithography Difficult Challenges >16nm
Updated	Table LITH2B	Lithography Difficult Challenges ≤16nm
Updated	Table LITH3	Lithography Technology Requirements
Updated	Table LITH4A	Resist Requirements
	Table LITH4B	Resist Sensitivities
Updated	Table LITH5A	Optical Mask Requirements
Updated	Table LITH5B	Double Patterning / Spacer Requirements
Updated	Table LITH5C	EUVL Mask Requirements
Updated	Table LITH5D	Imprint Template Requirements
	Table LITH6	Maskless Lithography Technology Requirements
Updated	Figure LITH3	DRAM and MPU Potential Solutions—Updated
NEW	Figure LITH4	Flash Potential Solutions—New for 2010

INTERCONNECT		
	Table INTC1	3D Interconnect Technologies Based on the Interconnect Hierarchy
	Table INTC2	3D-WLP Via Pitch Requirements Based on Table ORTC-4 Chip Pad Pitch Trend (µm)
Updated	Table INTC3	Global interconnect level 3D-SIC/3D-SOC roadmap
Updated	Table INTC4	Intermediate interconnect level 3D-SIC roadmap

INTERCONNECT		
Updated	Table INTC5	2009 Interconnect Difficult Challenges
Updated	Table INTC6	MPU Interconnect Technology Requirements
	Table INTC7	DRAM Interconnect Technology Requirements
	Table INTC8	Interconnect Surface Preparation Technology Requirements
	Table INTC9	Advantages and Concerns for Cu Extensions, Replacements and Native Device Interconnects.
	Table INTC10	Minimum Density of Metallic SWCNTs Needed to Exceed Minimum Cu Wire Conductivity
Updated	Figure INTC15	Planarization Applications and Equipment Potential Solutions
Updated	Figure INTC16	Planarization Consumables Potential Solutions

FACTORY INTEGRATION		
Updated	Table FAC1	Factory Integration Difficult Challenges
Updated	Table FAC2	Key Focus Areas and Issues for FI Functional Areas Beyond 2009
Updated	Table FAC3	Factory Operations Technology Requirements
Updated	Table FAC4	Context Data Importance for Good Equipment Visibility
Updated	Table FAC5	Production Equipment Technology Requirements
Updated	Table FAC6	Material Handling Systems Technology Requirements
Updated	Table FAC7	Factory Information and Control Systems Technology Requirements
Updated	Table FAC8	Facilities Technology Requirements
Updated	Table FAC9	Crosscut Issues Relating to Factory Integration

ASSEMBLY AND PACKAGING		
Updated	Table AP1	Difficult Challenges
	Table AP2	Single-chip Packages Technology Requirements
	Table AP3	Chip-to-package Substrate Technology Requirements
	Table AP4	Package Failure Modes
	Table AP5	Substrate to Board Pitch
	Table AP6	Package Warpage at Peak Processing Temperature
	Table AP7	Package Substrates: Low Cost (PBGAs
	Table AP8	Package Substrates: Hand-held (FBGA)
	Table AP9	Package Substrates: Mobile Products (SiP, PoP)
	Table AP10	Package Substrates: Cost performance (CPU, GPU,Game Processor)
	Table AP11	Package Substrates: High Performance (High End)
	Table AP12	Package Substrates: High Performance (LTCC)
	Table AP13	Wafer Level Packaging
	Table AP14	Key Technical Parameters for Stacked Architectures Using TSV
	Table AP15	System in Package Requirements
	Table AP16	Difficult Challenges for SiP
	Table AP17	TSV Interconnect Methods
	Table AP18	Comparison of SoC and SiP Architecture

ASSEMBLY AND PACKAGING		
	Table AP19	Some Common Optoelectronic Packages and Their Applications
	Table AP20	Telecommunications: Long Haul (100's of Km) to Metro (>1Km)
	Table AP21	Datacom Receivers: Short range LAN, FTTX, Active Optical Cable (AOC), Backplane, On-circuit Board and On-to and Off-of chip Data Transfer Applications
	Table AP22	Difficult Challenges for Optical Packaging
	Table AP23	Technology Requirements for Optical Packaging
	Table AP24	Potential Solutions for Optical Packaging
	Table AP25	Cross TWG Issues for Optoelectronics
	Table AP26	High Brightness LEDs
	Table AP27	MEMS Packaging Methods
	Table AP28	MEMS Packaging Examples
	Table AP29	Automotive Operating Environment Specifications
	Table AP30	Multiple-Sun Photovoltaic Cell Packaging Issues
	Table AP31	Thinned Silicon Wafer Thickness 200 mm/300 mm
	Table AP32	Challenges and Potential Solutions in Thinning Si Wafers
	Table AP33	Materials Challenges
	Table AP34	Packaging/Gaps/Technology Needs Summary
	Table AP35	Consortia and Research Institutes in Packaging Technology

ENVIRONMENT, SAFETY, AND HEALTH		
Updated	Table ESH1a	ESH Difficult Challenges—Near- and Long-term Years
	Table ESH2	ESH Requirements by Domain and Category
Updated	Table ESH3a	ESH Intrinsic Requirements—Near-term Years
Updated	Table ESH3b	ESH Intrinsic Requirements—Long-term Years
	Table ESH4a	Chemicals and Materials Management Technology Requirements—Near-term Years
	Table ESH4b	Chemicals and Materials Management Technology Requirements—Long-term Years
	Table ESH5a	Process and Equipment Management Technology Requirements—Near-term Years
	Table ESH5b	Process and Equipment Management Technology Requirements—Long-term Years
	Table ESH6a	Facilities Technology Requirements—Near-term Years

YIELD ENHANCEMENT		
Updated	Table YE1	Definitions for the Different Interface Points
Updated	Table YE2	Yield Enhancement Difficult Challenges
	Table YE3	Defect Budget Technology Requirement Assumptions
Updated	Table YE4	Defect Inspection on Pattern Wafer Technology Requirements
Updated	Table YE5	Defect Inspection on Unpatterned Wafers: Macro, and Bevel Inspection Technology Requirements
Updated	Table YE6	Defect Review and Automated Defect Classification Technology Requirements
Updated	Table YE7	Technology Requirements for Wafer Environmental Contamination Control

METROLOGY*		
***ONLY A FEW COLOR CHANGES WERE MADE TO A FEW TABLES FOR 2009; AS SUCH THESE TABLES ARE NOT INDICATED AS UPDATED. (SOME 2010 CELLS WERE CHANGED FROM YELLOW TO WHITE.)*		
	Table MET1	Metrology Difficult Challenges
	Table MET2	Metrology Technology Requirements
	Table MET3	Lithography Metrology (Wafer) Technology Requirements
	Table MET4a	Lithography Metrology (Mask) Technology Requirements: Optical
	Table MET4b	Lithography Metrology (Mask) Technology Requirements: EUV
	Table MET5	Front End Processes Metrology Technology Requirements
	Table MET6	Interconnect Metrology Technology Requirements

MODELING AND SIMULATION		
Updated	Table MS1	Modeling and Simulation Difficult Challenges
Updated	Table MS2A	Modeling and Simulation Technology Requirements: Capabilities—Near-term Years
Updated	Table MS2B	Modeling and Simulation Technology Requirements: Capabilities—Long-term Years
Updated	Table MS3	Modeling and Simulation Technology Requirements: Accuracy [1] —Near-term Years

Link to the 2010 Update webpage.