OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

Link to the 2003 ITRS Executive Summary

ORTC TABLES

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
ASIC/Low Operating Power Printed Gate Length (nm) ††	90	75	65	53	45	40	35
ASIC/Low Operating Power Physical Gate Length (nm)	65	53	45	37	32	28	25

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	ASIC/Low Operating Power Printed Gate Length (nm) ††	32		25	22		18	16		13
IS	ASIC/Low Operating Power Printed Gate Length (nm) ††	32	28	25	22	20	18	16	14	13
WAS	ASIC/Low Operating Power Physical Gate Length (nm)	22		18	16		13	11		9
IS	ASIC/Low Operating Power Physical Gate Length (nm)	22	20	18	16	14	13	11	10	9

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2 Overall Roadmap Technology Characteristics

Notes for Tables 1a and 1b

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "physical" gate lengths may be reduced from the "as-printed" dimension. These "physical" gate-length targets are driven by the need for maximum speed performance in logic Microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design ITWG Tables as needs that drive device design and process technology requirements.

In addition, during the 2003 ITRS development, an attempt has been made to reconcile the many published press releases by Logic manufacturers referencing "90 nm" technology node manufacturing in 2003. Since the metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that the public citations were in reference to an "indexed" technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance).

The IRC has decided that the best way to minimize confusion between the ITRS and individual company public announcements is to identify the ITRS table header node with the industry's most aggressive half-pitch targets, and to label these targets as hpXX (i.e., hp90, hp65, hp45, etc.). Currently the industry's most aggressive half pitch is the DRAM cell metal half-pitch.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1c DRAM Production Product Generations and Chip Size Model—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Cell area factor [a]	8	8	7.5	7	7	6	6
Cell area [Ca = af^2] (mm^2)	0.082	0.065	0.048	0.036	0.028	0.019	0.015
Cell array area at production (% of chip size) §	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%
Generation at production §	1G	1G	1G	2G	2G	4G	4G
Functions per chip (Gbits)	1.07	1.07	1.07	2.15	2.15	4.29	4.29
Chip size at production (mm^2)§	139	110	82	122	97	131	104
Gbits/cm^2 at production §	0.77	0.97	1.31	1.76	2.22	3.27	4.12

Table 1d DRAM Production Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Cell area factor [a]	6		6	6		6	5		5
IS	Cell area factor [a]	6	6	6	6	6	6	5	5	5
WAS	Cell area [Ca = af^2] (mm^2)	0.012		0.0077	0.0061		0.0038	0.0025		0.0016
IS	Cell area [Ca = af^2] (mm^2)	0.012	0.0096	0.0077	0.0061	0.005	0.0038	0.0025	0.002	0.0016
WAS	Cell array area at production (% of chip size) §	63.00%		63.00%	63.00%		63.00%	63.00%		63.00%
IS	Cell array area at production (% of chip size) §	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%	63.00%
WAS	Generation at production §	4G		8G	8G		16g	32G		32G
IS	Generation at production §	4G	8G	8G	8G	16g	16g	32G	32G	32G
WAS	Functions per chip (Gbits)	4.29		8.59	8.59		17.18	34.36		34.36
IS	Functions per chip (Gbits)	4.29	8.59	8.59	8.59	17.18	17.18	34.36	34.36	34.36
WAS	Chip size at production (mm^2)§	83		104	83		104	138		87
IS	Chip size at production (mm^2)§	83	131	104	83	131	104	138	110	87
WAS	Gbits/cm^2 at production §	5.19		8.23	10.37		16.46	24.89		39.51
IS	Gbits/cm^2 at production §	5.19	6.53	8.23	10.37	13.07	16.46	24.89	31.36	39.51

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Notes for Tables 1c and 1d
§ DRAM Model—Cell Factor (design/process improvement) targets are as follows
1999-2004/8× 2005/7.5×; 2006-2007/7×; 2008-2015/6×; 2016–2018/5×. The delay of the "6" DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.
DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except
1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).
InTER-generation chip size growth rate model target for Production-phase DRAMs is now "flat" at less than 140 mm^2, similar to the MPU model. This new flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Table 1c,d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63% , which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above).The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.
Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
DRAM ½ Pitch (nm)	**100**	**90**	**80**	**70**	**65**	**57**	**50**
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Cell area factor [a]	**8**	**8**	**7.5**	**7**	**7**	**6**	**6**
Cell area [Ca = af^2] (mm^2)	**0.082**	**0.065**	**0.048**	**0.036**	**0.028**	**0.019**	**0.015**
Cell array area at introduction (% of chip size) §	**72.23%**	**72.61%**	**72.95%**	**73.25%**	**73.52%**	**73.76%**	**73.97%**
Generation at introduction §	**4G**	**4G**	**8G**	**8G**	**16G**	**16G**	**16G**
Functions per chip (Gbits)	**4.29**	**4.29**	**8.59**	**8.59**	**17.18**	**17.18**	**17.18**
Chip size at introduction (mm^2) §	**485**	**383**	**568**	**419**	**662**	**449**	**356**
Gbits/cm^2 at introduction §	**0.88**	**1.12**	**1.51**	**2.05**	**2.59**	**3.82**	**4.83**

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Cell area factor [a]	6		6	6		6	5		5
IS	Cell area factor [a]	6	6	6	6	6	6	5	5	5
WAS	Cell area [Ca = af2] (mm^2)	0.012		0.0077	0.0061		0.0038	0.0025		0.0016
IS	Cell area [Ca = af2] (mm^2)	0.0120	0.01	0.0077	0.0061	0.005	0.0038	0.0025	0.0020	0.0016
WAS	Cell array area at introduction (% of chip size) §	74.16%		74.47%	74.61%		74.83%	74.93%		75.09%
IS	Cell array area at introduction (% of chip size) §	74.16%	74.30%	74.47%	74.61%	74.70%	74.83%	74.93%	75.00%	75.09%
WAS	Generation at introduction §	32G		32G	64G		64G	128G		128G
IS	Generation at introduction §	32G	32G	32G	64G	64G	64G	128G	128G	128G
WAS	Functions per chip (Gbits)	34.36		34.36	68.72		68.7	137.4		137.4
IS	Functions per chip (Gbits)	34.36	34.36	34.36	68.72	68.72	68.7	137.4	137.4	137.4
WAS	Chip size at introduction (mm^2) §	563		353	560		351	464		292
IS	Chip size at introduction (mm^2) §	563	458	353	560	456	351	464	378	292
WAS	Gbits/cm2 at introduction §	5.2		8.2	10.4		16.5	24.9		39.5
IS	Gbits/cm2 at introduction §	6.10	7.71	9.73	12.3	15.5	19.6	29.6	37.3	47.1

Notes for Tables 1e and 1f

§ DRAM Model—Cell Factor (design/process improvement) targets are as follows 1999-2004/8× 2005/7.5×; 2006-2007/7×; 2008-2015/6×; 2016–2018/5×. The delay of the "6" DRAM Cell design improvement Factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a 3-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation/2007, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation/2003, the introduction rate is 4×/five years (2×/two–three years).

The original 2001 ITRS InTER-generation chip size growth rate was targeted to fit one chip per 572 mm^2 field at Introduction and two chips per 572 mm^2 field at Production. Due to the delay of the cell area factor reductions, Introduction chip sizes increased, but the new 704 mm^2 maximum affordable Litho field allows the Introduction chip to double bits per chip every two years through the 16 Gbit generation (660 mm^2/2007). Slowing the "Moore's Law" bits per chip of the Introduction-phase DRAM model to an average of 2× per 2.5 years enables the Introduction DRAMs to remain under the original 572 mm^2 affordable target after 2007. The InTRA-generation chip size shrink model remains at 0.5× every technology node in-between cell factor reductions, and eventually (ranging from five to six years), the Introduction-phase DRAMs shrink below the 140 mm^2 Production-phase chip size target.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

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Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	SRAM Cell (6-transistor) Area factor ++	120.3	117.8	115.6	113.7	111.9	110.4	109
	Logic Gate (4-transistor) Area factor ++	320	320	320	320	320	320	320
	SRAM Cell (6-transistor) Area efficiency ++	0.63	0.63	0.63	0.63	0.63	0.63	0.63
	Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50	0.50	0.50	0.50	0.50
ADD	SRAM Cell (6-transistor) Area ++	1.23	0.95	0.74	0.58	0.45	0.35	0.28
	SRAM Cell (6-transistor) Area w/overhead ++	2.0	1.5	1.2	0.93	0.73	0.57	0.45
ADD	Logic Gate (4-transistor) Area ++	3.27	2.59	2.06	1.63	1.30	1.03	0.82
	Logic Gate (4-transistor) Area w/overhead ++	6.5	5.2	4.1	3.3	2.6	2.1	1.6
	Transistor density SRAM (Mtransistors/cm^2)	305	393	504	646	827	1,057	1,348
	Transistor density logic (Mtransistors/cm^2)	61	77	97	122	154	194	245
	Generation at introduction *	--	p07c	--	--	p10c	--	--
WAS	Functions per chip at introduction (million transistors [Mtransistors])	180	226	285	360	453	571	719
IS	Functions per chip at introduction (million transistors [Mtransistors])	307	386	487	614	773	974	1227
	Chip size at introduction (mm^2) ‡	280	280	280	280	280	280	280
	Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	110	138	174	219	276	348	438
	Generation at production *	--	p04c	--	--	p07c	--	--
	Functions per chip at production (million transistors [Mtransistors])	153	193	243	307	386	487	614
	Chip size at production (mm^2) §§	140	140	140	140	140	140	140
	Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	110	138	174	219	276	348	438

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	SRAM Cell (6-transistor) Area factor ++	107.8		105.7	104.8		103.4	102.8		101.7
IS	SRAM Cell (6-transistor) Area factor ++	107.8	106.7	105.7	104.8	104.1	103.4	102.8	102.2	101.7
WAS	Logic Gate (4-transistor) Area factor ++	320		320	320		320	320		320
IS	Logic Gate (4-transistor) Area factor ++	320	320	320	320	320	320	320	320	320
WAS	SRAM Cell (6-transistor) Area efficiency ++	0.625		0.625	0.625		0.625	0.625		0.625
IS	SRAM Cell (6-transistor) Area efficiency ++	0.625	0.625	0.625	0.625	0.625	0.625	0.625	0.625	0.625
WAS	Logic Gate (4-transistor) Area efficiency ++	0.5		0.5	0.5		0.5	0.5		0.5
IS	Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50
ADD	SRAM Cell (6-transistor) Area	0.22	0.17	0.13	0.11	0.084	0.066	0.052	0.041	0.032
WAS	SRAM Cell (6-transistor) Area w/overhead ++	0.22		0.13	0.11		0.066	0.052		0.032
IS	SRAM Cell (6-transistor) Area w/overhead ++	0.35	0.27	0.22	0.17	0.13	0.106	0.083	0.07	0.052
ADD	Logic Gate (4-transistor) Area	0.65	0.51	0.41	0.32	0.26	0.20	0.16	0.13	0.10
WAS	Logic Gate (4-transistor) Area w/overhead ++	1.3		0.82	0.65		0.41	0.32		0.2
IS	Logic Gate (4-transistor) Area w/overhead ++	1.30	1.03	0.82	0.65	0.51	0.41	0.32	0.26	0.20
WAS	Transistor density SRAM (Mtransistors/cm^2)	1,718		2,781	3,532		5,687	7,208		11,558
IS	Transistor density SRAM (Mtransistors/cm^2)	1,718	2,187	2,781	3,532	4,484	5,687	7,208	9,130	11,558
WAS	Transistor density logic (Mtransistors/cm^2)	309		490	617		980	1,235		1,960
IS	Transistor density logic (Mtransistors/cm^2)	309	389	490	617	778	980	1,235	1,555	1,960

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Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Generation at introduction *	p13c		--	p16c		--	p19c		--
IS	Generation at introduction *	p13c	--	--	p16c	--	--	p19c	--	--
WAS	Functions per chip at introduction (million transistors [Mtransistors])	1,546		2,454	3,092		4,908	6,184		9,816
IS	Functions per chip at introduction (million transistors [Mtransistors])	1,546	1,948	2,454	3,092	3,896	4,908	6,184	7,791	9,816
WAS	Chip size at introduction (mm^2) ‡	280		280	280		280	280		280
IS	Chip size at introduction (mm^2) ‡	280	280	280	280	280	280	280	280	280
WAS	Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	552		876	1,104		1,753	2,209		3,506
IS	Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	552	696	876	1,104	1,391	1,753	2,209	2,783	3,506
WAS	Generation at production *	p10c		--	p13c		--	p16c		--
IS	Generation at production *	p10c	--	--	p13c	--	--	p16c	--	--
WAS	Functions per chip at production (million transistors [Mtransistors])	773		1,227	1,546		2,454	3,092		4,908
IS	Functions per chip at production (million transistors [Mtransistors])	773	974	1,227	1,546	1,948	2,454	3,092	3,896	4,908
WAS	Chip size at production (mm^2) §§	140		140	140		140	140		140
IS	Chip size at production (mm^2) §§	140	140	140	140	140	140	140	140	140
WAS	Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	552		876	1,104		1,753	2,209		3,506
IS	Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	552	696	876	1,104	1,391	1,753	2,209	2,783	3,506

Notes for Tables 1g and 1h

++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p01c, was introduced in 1999, but not ramped into volume production until 2001; similarly, the p04c, is introduced in 2001, but is targeted for volume production in 2004.*

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/1999), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years
UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	Logic (Low-volume Microprocessor) High-performance ‡							
WAS	Generation at production **	p03h	--	p05h	--	p07h	--	p09h
IS	Generation at production **	--	p04h	--	--	p07h	--	--
	Functions per chip (million transistors)	439	553	697	878	1,106	1,393	1,756
	Chip size at production (mm^2) §§	310	310	310	310	310	310	310
	High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	142	178	225	283	357	449	566
	ASIC							
	ASIC usable Mtransistors/cm^2 (auto layout)	142	178	225	283	357	449	566
	ASIC max chip size at production (mm^2) (maximum lithographic field size)	572	572	572	572	572	572	572
	ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	810	1,020	1,286	1,620	2,041	2,571	3,239

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Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years
UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Logic (Low-volume Microprocessor) High-performance ‡									
WAS	Generation at production **	--		--	p13h		p15h	--		--
IS	Generation at production **	p10h	--	--	p13h	--	--	p16h	--	--
WAS	Functions per chip (million transistors)	2,212		3,511	4,424		7,022	8,848		14,045
IS	Functions per chip (million transistors)	2,212	2,787	3,511	4,424	5,574	7,022	8,848	11,147	14,045
WAS	Chip size at production (mm^2) §§	310		310	310		310	310		310
IS	Chip size at production (mm^2) §§	310	310	310	310	310	310	310	310	310
WAS	High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	714		1,133	1,427		2,265	2,854		4,531
IS	High-performance MPU Mtransistors/cm^2 at production (including on-chip SRAM) ‡	714	899	1,133	1,427	1,798	2,265	2,854	3,596	4,531
	ASIC									
WAS	ASIC usable Mtransistors/cm^2 (auto layout)	714		1,133	1,427		2,265	2,854		4,531
IS	ASIC usable Mtransistors/cm^2 (auto layout)	714	899	1,133	1,427	1,798	2,265	2,854	3,596	4,531
WAS	ASIC maximum chip size at production (mm^2) (maximum lithographic field size)	572		572	572		572	572		572
IS	ASIC maximum chip size at production (mm^2) (maximum lithographic field size)	572	572	572	572	572	572	572	572	572
WAS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081		6,479	8,163		12,958	16,326		25,915
IS	ASIC maximum functions per chip at ramp (Mtransistors/chip) (fit in maximum lithographic field size)	4,081	5,142	6,479	8,163	10,284	12,958	16,326	20,569	25,915

Notes for Tables 1i and 1j
*** p is processor, numerals reflect year of production; h indicates high-performance product. Examples—the high-performance processor, p99h, was ramped into volume production in 1999; similarly, the p01h, is introduced in 2001, the p03h in2003, and so forth.*
‡ MPU High-performance Model—High-performance MPU includes large L2 and L3 on-chip SRAM (2MByte/1999) plus a larger logic core (P99h core = 25M transistor (Mtransistors) both SRAM and Logic functionality doubles every technology node cycle.
§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.
Refer to the Glossary for definitions

Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Lithography Field Size							
Lithography Field Size—area (mm^2)	**704**	**704**	**704**	**704**	**704**	**704**	**704**
Lithographic field size—length (mm)	**32**	**32**	**32**	**32**	**32**	**32**	**32**
Lithographic field size—width (mm)	**22**	**22**	**22**	**22**	**22**	**22**	**22**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	**300**	**300**	**300**	**300**	**300**	**300**	**300**

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years UPDATED

	Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
	Technology Node	*hp45*			*hp32*			*hp22*		
WAS	*DRAM ½ Pitch (nm)*	*45*		*35*	*32*		*25*	*22*		*18*
IS	*DRAM ½ Pitch (nm)*	*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
WAS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**	-	**42**	**38**	-	**30**	**27**	-	**21**
IS	*MPU/ASIC Metal 1 (M1) ½ Pitch (nm)*	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
WAS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**	-	**35**	**32**	-	**25**	**22**	-	**18**
IS	*MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)*	**45**	**40**	**35**	**32**	**28**	**25**	**22**	**20**	**18**
WAS	*MPU Printed Gate Length (nm) ††*	**25**	-	**20**	**18**	-	**14**	**13**	-	**10**
IS	*MPU Printed Gate Length (nm) ††*	**25**	**22**	**20**	**18**	**16**	**14**	**13**	**11**	**10**
WAS	*MPU Physical Gate Length (nm)*	**18**	-	**14**	**13**	-	**10**	**9**	-	**7**
IS	*MPU Physical Gate Length (nm)*	**18**	**16**	**14**	**13**	**11**	**10**	**9**	**8**	**7**
	Lithography Field Size									
WAS	*Lithography Field Size—area (mm^2)*	**704**		**704**	**704**		**704**	**704**		**704**
IS	*Lithography Field Size—area (mm^2)*	**704**	**704**	**704**	**704**	**704**	**704**	**704**	**704**	**704**
WAS	*Lithographic field size—length (mm)*	**32**	-	**32**	**32**	-	**32**	**32**	-	**32**
IS	*Lithographic field size—length (mm)*	**32**	**32**	**32**	**32**	**32**	**32**	**32**	**32**	**32**
WAS	*Lithographic field size—width (mm)*	**22**	-	**22**	**22**	-	**22**	**22**	-	**22**
IS	*Lithographic field size—width (mm)*	**22**	**22**	**22**	**22**	**22**	**22**	**22**	**22**	**22**
	Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)									
WAS	*Bulk or epitaxial or SOI wafer*	**300**		**450**	**450**		**450**	**450**		**450**
IS	*Bulk or epitaxial or SOI wafer*	**300**	**300**	**450**	**450**	**450**	**450**	**450**	**450**	**450**

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Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	Number of Chip I/Os (Number of Total Chip Pads)—Maximum							
WAS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,328	3,584
IS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072
WAS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,109	1,195
IS	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,024	1,024
WAS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,219	2,389
IS	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,048	2,048
WAS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,600	4,800
IS	Total pads—ASIC high-performance	3,400	3,600	4,000	4,200	4,400	4,400	4,600
WAS	Signal I/O pads—ASIC high-performance	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Signal I/O pads—ASIC high-performance	1700	1800	2000	2100	2200	2200	2300
WAS	Power and ground pads— ASIC high-performance (½ of total pads)	1,700	1,800	2,000	2,100	2,200	2,300	2,400
IS	Power and ground pads— ASIC high-performance (½ of total pads)	1700	1800	2000	2100	2200	2200	2300
	Number of Total Package Pins—Maximum [1]							
WAS	Microprocessor/controller, cost-performance	500–1,452	500–1,600	550–1,760	550–1,936	600–2,140	660–2,354	720–2,568
IS	Microprocessor/controller, cost-performance	--	500–1600	550–1760	550–1936	600–2140	600–2400	660–2800
WAS	Microprocessor/controller, high-performance	1,452	1,600	1,760	1,936	2,140	2,354	2,568
IS	Microprocessor/controller, high-performance	--	1,600	1,760	1,936	2,140	2,400	2,800
WAS	ASIC (high-performance)	2,400	3,000	3,400	3,800	4,000	4,400	4,600
IS	ASIC (high-performance)	--	3,000	3,400	3,800	4,000	4,400	4,600

Notes for Tables 3a and 3b
[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by PWB technology and system cost. The highest pin count applications will as a result use larger pitches and larger package sizes. The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2 1 to 1 4.

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Number of Chip I/Os (Number of Total Chip Pads)—Maximum									
WAS	Total pads—MPU	3,840		4,096	4,224		4,352	4,416		4,544
IS	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072
WAS	Signal I/O—MPU (1/3 of total pads)	1,280		1,365	1,408		1,451	1,472		1,515
IS	Signal I/O—MPU (1/3 of total pads)	1024	1024	1024	1024	1024	1024	1024	1024	1024
WAS	Power and ground pads—MPU (2/3 of total pads)	2,560		2,731	2,816		2,901	2,944		3,029
IS	Power and ground pads—MPU (2/3 of total pads)	2048	2048	2048	2048	2048	2048	2048	2048	2048
WAS	Total pads—ASIC high-performance	4,800		5,200	5,400		5,800	6,000		6,400
IS	Total pads—ASIC high-performance	4,800	4,800	5,000	5,400	5,400	5,600	6,000	6,000	6,200
WAS	Signal I/O pads—ASIC high-performance	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Signal I/O pads—ASIC high-performance	2,400	2,400	2,500	2,700	2,700	2,800	3,000	3,000	3,100
WAS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	-	2,600	2,700		2,900	3,000		3,200
IS	Power and ground pads—ASIC high-performance (½ of total pads)	2,400	2,400	2,500	2,700	2,700	2,800	3,000	3,000	3,100
	Number of Total Package Pins—Maximum [1]									
	Microprocessor/controller, cost-performance	780–2,782		936–3,338	1014–3,616		1217–4,340	1318–4,702		1521–5,426
	Microprocessor/controller, high-performance	2,782		3,338	3,616		4,340	4,702		5,426
	ASIC (high-performance)	4,009		4,810	5,335		6,402	7,042		8,450

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Table 4a Performance and Package Chips: Pads, Cost—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	Chip Pad Pitch (micron)							
WAS	Pad pitch—ball bond	40	35	30	25	25	20	20
IS	Pad pitch—ball bond	40	40	35	35	30	30	25
WAS	Pad pitch—wedge bond	30	25	20	20	20	20	20
IS	Pad pitch—wedge bond	30	30	30	25	25	25	20
	Pad Pitch—area array flip-chip (cost-performance, high-performance)	150	150	130	130	120	110	100
	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	60	60	40	40	30	30	20
	Cost-Per-Pin							
	Package cost (cents/pin) (cost-performance)—minimum-maximum	.75–1.30	.71–1.24	.67–1.17	.64–1.11	.61–1.05	.58–1.00	.55–.96
WAS	Package cost (cents/pin) (Memory)—minimum–maximum	0.30–0.56	0.29–.53	.27–.50	,26–.48	,25–.45	.23–.43	.22–.41
IS	Package cost (cents/pin) (Memory)—minimum–maximum	0.30–0.56	0.30–.53	.27–.50	.26–.48	.25–.45	.23–.43	.22–.41

Table 4b Performance and Package Chips: Pads, Cost—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Chip Pad Pitch (micron)									
WAS	Pad pitch—ball bond	20		20	20		20	20		20
IS	Pad pitch—ball bond	25	25	25	25	25	25	25	25	25
WAS	Pad Pitch—wedge bond	20		20	20		20	20		20
IS	Pad Pitch—wedge bond	20	20	20	20	20	20	20	20	20
WAS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	100		90	90		80	80		70
IS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	90	--	90		--	80	--	--	70
WAS	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	20		20	20		15	15		15
IS	Pad Pitch—peripheral flip-chip (handheld, low-cost, harsh)	20	20	20	20	--	15	15	15	15
	Cost-Per-Pin									
	Package cost (cents/pin) (cost-performance)— minimum–maximum	0.52–0.94		0.5–.86	0.5–.77		0.5–0.69	0.5–0.65		0.5–0.59
	Package cost (cents/pin) (Memory)— minimum–maximum	.22–.41		0.22–0.36	0.22–0.35		0.22–0.31	0.22–0.29		0.22–0.27

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Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Chip Frequency (MHz)							
On-chip local clock	2,976	4,171	5,204	6,783	9,285	10,972	12,369
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	2,000	2,500	3,125	3,906	4,883	6,103	7,629
Maximum number wiring levels—maximum	13	14	15	15	15	16	16
Maximum number wiring levels—minimum	9	10	11	11	11	12	12

Table 4d Performance and Package Chips: Frequency, On-chip Wiring Levels—Long-term Years
UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	-	35	32	-	25	22	-	18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25	-	20	18	-	14	13	-	10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18	-	14	13	-	10	9	-	7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Chip Frequency (MHz)									
	On-chip local clock	15,079		20,065	22,980		33,403	39,683		53,207
	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	9,536		14,901	18,626		29,103	36,379		56,843
WAS	Maximum number wiring levels—maximum	16		16	16		17	18		18
IS	Maximum number wiring levels—maximum	16	16	16	16	17	17	18	18	18
WAS	Maximum number wiring levels—minimum	12		12	12	-	13	14	-	14
IS	Maximum number wiring levels—minimum	12	12	12	12	13	13	14	14	14

Note for Tables 4c and 4d
[1] The off-chip frequency is expected to increase for a small number of high-speed pins that will be used in combination with a large number of lower speed pins
[2] In 2001, high-speed serial communications transceiver devices are achieving chip-board frequencies of 3.125 GHz using CMOS, and 10 GHz using SiGe. In 2002 it is expected that 10 GHz transceivers will be fabricated using CMOS. 40 GHz SiGe devices are expected in 2003. The roadmap for higher levels of integration with wider bus widths, is shown in the High Frequency Serial Communications section in the Test chapter.
[3] The minimum number of wiring levels represents the interconnect metal levels, and the maximum number of interconnect wiring levels includes the Minimum number of wiring levels plus additional optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

Table 5a Electrical Defects—Near-term Years

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	2,216	2,791	3,751	2,532	3,190	2,345	2,954
MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	1,395	1,395	1,395	1,395	1,395	1,395	1,395
# Mask Levels—MPU	29	31	33	33	33	35	35
# Mask Levels—DRAM	24	24	24	24	24	24	24

Table 5b Electrical Defects—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §	3,722		2,954	3,722		2,954	2,233		3,545
IS	DRAM Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §	3,722	2,353	2,954	3,722	2,353	2,954	2,233	2,803	3,545
WAS	MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§	1,395		1,395	1,395		1,395	1,395		1,395
IS	MPU Random Defect D_0 at production chip size and 89.5% yield (faults/ m^2) §§	1,395	1,395	1,395	1,395	1,395	1,395	1,395	1,395	1,395
WAS	# Mask Levels—MPU	35		35	35		37	39		39
IS	# Mask Levels—MPU	35	35	35	35	37	37	39	39	39
WAS	# Mask Levels—DRAM	26		26	26		26	26		26
IS	# Mask Levels—DRAM	26	26	26	26	26	26	26	26	26

Notes for Tables 5a and 5b

D_0 — defect density

§ DRAM Model—Cell factor (design/process improvement) targets are as follows

1999–2004/8× 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the "6" DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2×.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

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Table 6a Power Supply and Power Dissipation—Near-term Years UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm) ††	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
	Power Supply Voltage (V)							
	V_{dd} (high-performance)	1.2	1.2	1.1	1.1	1.1	1	1
	V_{dd} (Low Operating Power, high V_{dd} transistors)	1	0.9	0.9	0.9	0.8	0.8	0.8
	Allowable Maximum Power [1]							
WAS	High-performance with heatsink (W)	149	158	167	180	189	200	210
IS	High-performance with heatsink (W)	149	158	167	180	189	198	198
	Cost-performance (W)	80	84	91	98	104	109	114
	Battery (W)—(low-cost/hand-held)	2.1	2.2	2.3	2.4	2.5	2.6	2.7

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 6b Power Supply and Power Dissipation—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Power Supply Voltage (V)									
WAS	Vdd (high-performance)	1		0.9	0.9		0.8	0.8		0.7
IS	Vdd (high-performance)	1	1	0.9	0.9	0.9	0.8	0.8	0.7	0.7
WAS	Vdd (Low Operating Power, high Vdd transistors)	0.7		0.7	0.6		0.6	0.5		0.5
IS	Vdd (Low Operating Power, high Vdd transistors)	0.7	0.7	0.7	0.6	0.6	0.6	0.5	0.5	0.5
	Allowable Maximum Power [1]									
WAS	High-performance with heatsink (W)	218		240	251		270	288		300
IS	High-performance with heatsink (W)	198	198	198	198	198	198	198	198	198
	Cost-performance (W)	120		131	138		148	158		168
	Battery (W)—(hand-held)	2.8		3	3		3	3		3

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 7a Cost—Near-term Years

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	**120**	**107**	**95**	**85**	**76**	**67**	**60**
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	**107**	**90**	**80**	**70**	**65**	**57**	**50**
MPU Printed Gate Length (nm) ††	**65**	**53**	**45**	**40**	**35**	**32**	**28**
MPU Physical Gate Length (nm)	**45**	**37**	**32**	**28**	**25**	**22**	**20**
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	**10.5**	**7.4**	**5.3**	**3.7**	**2.6**	**1.9**	**1.3**
DRAM cost/bit at (packaged microcents) at production §	**3.8**	**2.7**	**1.9**	**1.4**	**0.96**	**0.7**	**0.5**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**88**	**62**	**44**	**31**	**22**	**15.6**	**11.0**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**53**	**38**	**27**	**19**	**13.3**	**9.4**	**6.7**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**49**	**34**	**24**	**17**	**12**	**8.6**	**6.1**
Cost-Per-Pin							
Test Cost							
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	**1**	**1**	**1**	**1**	**1**	**1**	**2**

Notes for Tables 7a and 7b

++ Affordable packaged unit cost per function based upon Average Selling Prices (ASPs) available from various analyst reports less Gross Profit Margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two to four years after introduction).

§ DRAM Model—Cell factor (design/process improvement) targets are as follows

1999–2004/8× 2005/7.5×; 2006–2007/7×; 2008–2015/6×; 2016–2018/5×. The delay of the "6" DRAM cell design improvement factor [a] by five years, from 2003 to 2008, requires the slowing of the addition of "Moore's Law" bits/chip from 2× every 1.5–2 years to 2× every 2.5–3 years in the 2003 ITRS DRAM Chip Size Model, which remains on a three-year DRAM half-pitch node cycle after 2004.

DRAM product generations are usually increased by 4× bits/chip every four years with interim 2× bits/chip generations, except

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 1 Gbit generation, the introduction rate is 4×/five years (2×/two–three years).

InTER-generation chip size growth rate model target for Production-phase DRAMs is now "flat" at less than 140 mm^2, similar to the MPU model. This new flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAMs to increase the time for doubling bits per chip to an average of 2×/2.5 years by alternating between 2×/2 years and 2×/3 years (see ORTC Tables 1c and d). In addition, the Cell Array Efficiency (Array % of total chip area) was increased to 63%, which also assists in the achievement of the target flat-chip-size model for the Production-phase product chip size, even under the slower design improvement factor contribution (see note above). The InTRA-generation chip size shrink model is 0.5× every technology node in-between cell factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation chip size growth rates are targeted to be flat through 2018 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size model is made possible by doubling the on-chip functionality every technology node cycle. The InTRA-generation chip size shrink model was 0.5× every two-year technology node through 2001, and is now 0.5× every three-year technology node cycle after 2003.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

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Table 7b Cost—Long-term Years UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
WAS	DRAM ½ Pitch (nm)	45		35	32		25	22		18
IS	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54		42	38		30	27		21
IS	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
WAS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45		35	32		25	22		18
IS	MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	45	40	35	32	28	25	22	20	18
WAS	MPU Printed Gate Length (nm) ††	25		20	18		14	13		10
IS	MPU Printed Gate Length (nm) ††	25	22	20	18	16	14	13	11	10
WAS	MPU Physical Gate Length (nm)	18		14	13		10	9		7
IS	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
	Affordable Cost per Function ++									
WAS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93		0.46	0.33		0.16	0.12		0.06
IS	DRAM cost/bit (packaged microcents) at samples/introduction	0.93	0.66	0.46	0.33	0.23	0.16	0.12	0.08	0.06
WAS	DRAM cost/bit (packaged microcents) at production §	0.34		0.17	0.12		0.06	0.042		0.021
IS	DRAM cost/bit (packaged microcents) at production §	0.34	0.24	0.17	0.12	0.08	0.06	0.04	0.03	0.02
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78		3.89	2.75		1.38	0.97		0.49
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	7.78	5.50	3.89	2.75	1.94	1.38	0.97	0.69	0.49
WAS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71		2.35	1.66		0.83	0.59		0.29
IS	Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.71	3.33	2.35	1.66	1.18	0.83	0.59	0.42	0.29
WAS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.305		2.15	1.52		0.76	0.54		0.27
IS	High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	4.30	3.04	2.15	1.52	1.08	0.76	0.54	0.38	0.27
	Cost-Per-Pin									
	Test Cost									
WAS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	4		4	4		4	4		4
IS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—maximum	4	4	4	4	4	4	4	4	4
WAS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	2		2	3		3	4		4
IS	Volume tester cost per high-frequency signal pin ($K/pin) (high-performance ASIC)—minimum	2	2	2	3	3	3	4	4	4

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

Technology Node—The minimum half-pitch of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated circuits and is selected to define an ITRS Technology Node. For each Node, this defining metal half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other parameters are also important for characterizing IC technology. For example, in the case of microprocessors (MPUs), physical bottom gate length is most representative of the leading-edge technology level required for maximum performance. Each technology node step represents the creation of significant technology progress in metal half-pitch — approximately 70% of the preceding node, 50% of two preceding nodes.

Example: DRAM half pitches of 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, and 22 nm.

For cost reasons, high-volume, low-cost ASIC gate-length requirements will typically match DRAM half-pitch targets, but the low-volume leading-edge high-performance ASIC gate-length requirements will track closely with MPUs.

An official *2003 ITRS* metal half-pitch node indicator, "hpXX," has been added to differentiate the ITRS definition from commercial technology generation numbers .

Moore's Law—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore's Law, there is a historically-based "corollary" to the "law," which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every three years, as suggested by consensus DRAM and MPU models of the *2003 ITRS*, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated Microprocessor Unit (MPU) product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

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Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1Mbytes/2001). Logic functionality and L2 cache typically double every three-year generation.

High-performance MPU—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example two cores at 25Mt cores in 2001) with a large (example 4Mbyte/2001) level-two (L2) SRAM. Logic functionality and L2 cache typically double every three-year technology generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology-node scaling (.7× linear, .5× area) is every three years, an additional device/process design improvement of .8× per two years must be achieved. This requirement represents a design-related (cell-area-factor) area-reduction improvement of at least -11% per year, and this design-related productivity improvement is in addition to the basic lithography-based area reduction of -21% per year (three-year node cycle).

The present *2003 ITRS* consensus target for the rate of increase of DRAM bits/chip has increased from 2× bits/chip every two years to 2×/chip every two and half years average. This slower bits/chip growth is required due to the new consensus *2003 ITRS* forecast of cell-area-factor improvement of only negative 4–6% per year on average rather than the *2001 ITRS* target of -7% per year average. This results in an average DRAM inTER-generation approximately flat chip-size growth. Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the *2003 ITRS* MPU inTER-generation functionality model target is 2× transistors/chip every technology node, in order maintain a flat chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The *2003 ITRS* consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The *ITRS* targets for both DRAM and MPU reduce chip size within a generation by minus 50% per technology node.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every four years at the leading-edge process technology node, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples. Example: 1997/ISSCC/1Gb DRAM, versus *ITRS* 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every two years (every technology node, in the case of MPUs). In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturer begins shipping volume quantities (initially, at least 10K/month) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume

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production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready 12–24 months prior to Production Ramp "Time Zero" [see Figure 2 in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1Gb/production, 4G/introduction, plus 512Mb/256Mb/128Mb/64Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the *ITRS* consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the *2003 ITRS*, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 63% at the production level, and less than 50–55% for smaller previous generation shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified *ITRS*-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 1999: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E = 0.37\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.37e-6 mm^2/bit = 397 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, 1.6×1.6=2.5, etc.).

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density

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calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board.). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The *ITRS* timing targets, contributed by the Factory Integration ITWG, are based on the first 20K wafer-starts-per-month manufacturing facility.

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ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

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FOLDER 10

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Design

Jointly Sponsored
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DESIGN

2004 UPDATE HIGHLIGHTS

This update includes (a) a revised "General" design technology requirements (revised), with some new rows, and new explanations as footnotes for each row, but no changes in the values of existing rows, (b) a new design technology solutions table after the requirements table, which includes a definition of each row, (c) a new Design For Manufacturability (DFM) section with completely new content, and (d) an update of the verification section.

Link to the 2003 ITRS Design chapter

WORKING GROUP SECTION UPDATES

DESIGN FOR MANUFACTURABILITY [NEW SECTION ADDED]

Increasing variability, mask cost and data explosion, and lithography hardware limitations, are posing significant design challenges for the manufacturability of integrated circuits:

1. Architecture challenges—architectural redundancy will be required due to the difficulty in making circuits yield. It will be hard to do much more at this level of abstraction.

2. Logic and circuit challenges—digital and mixed-signal adaptive circuits will be increasingly necessary. Statistical design, including power and timing convergence will be fundamental. But it will be hard to make work without addressing two primary challenges: characterization and modeling inputs to statistical design tools; and the evolution from statistical analysis to optimization with the subsequent increase in computation complexity. Finally, statistical timing tools and statistical optimization methods must model actual variations rather than crude and inaccurate abstractions. The composition of variations during statistical analyses and optimizations should match the methods used for initial decomposition via statistical metrology techniques during process characterization. A mismatch between composition and decomposition will introduce unnecessary error and impart dubious value to the computationally costly results.

3. Layout and physical design challenges— First, the complexity of design rules checking is increasing (include graph). Rules have evolved to a two-tier system (required versus suggested rules) and may need to evolve either to a three-tier system or to a no-tier system (where rules are not pass-fail but provide a point in a curve and the designer needs to apply criteria for tape-out). All this will need to be done without increasing designer-perceived complexity. Second, the limitation in lithography hardware resolution will require design flows to more explicitly account for the impact of Resolution Enhancement Techniques (RET). RET tools, such as OPC and CMP fill, must become explicitly aware of circuit metrics such as timing and power. Such awareness aligns the tools to overall product goals and enables yield enhancements, manufacturing cost reductions, and mask data preparation time. As an example, OPC would be applied only to features in critical timing paths. This entails a tighter flow integration to communicate circuit intent downstream, and to avoid independent modifications by several tools leading to incorrect results.

4. Yield prediction and optimization as design challenge— The ground rules as specified are not longer ‘hard numbers’, where designer and EDA tools used to consider as strict ‘hard’ numbers. To archive reasonable mature yields and steep ramp capability a strategy for meaningful relaxation have to be used. These ‘recommended’ rules have been derived from the interaction of the design layout and wafer process requirements, such as alignment tolerances, optical proximity corrections, RET enhancements and many other constrains. DFM measures acts different for each design because it impacts power, area and speed as you tune for yield. During design process the mutual interaction off yield, area, power and speed must be analyzed and a commercial useful trade off must be found. This involvement of DFM measures effecting the functional yield and parametric yield must be integrated as a new optimization feature into the design flow and tools, not as post processing that allows only limited results and is time consuming. That means that yield prediction has to be integrated into design tools for Synthesis and Place & Route to consider all design targets to optimize simultaneously yield, performance, power, signal integrity and area (Yield as explicit new design target).

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Table A Design For Manufacturability Challenges ADDED

Challenges ≥50 nm/Through 2009	*Summary Of Issues*
Mask cost	ALL—CAD tools that explicitly account for mask cost in their algorithms
Data explosion	ALL—RET tools that are explicitly aware of circuit metrics (timing, power)
Limitations of lithography hardware resolution	ALL—RET-aware CAD tools, radically-restricted design rules, including yield prediction and optimization
Voltage supply and threshold variability	ALL—Statistical analysis tools and flows that account for this variability, including yield prediction and optimization
BEOL Planarization and dimensional variability	ALL—Statistical design tools and flows that account for this variability; including yield prediction and optimization
Heterogeneous components (analog, MEMS, eRAM)	
Leakage as a limiter of manufacturability	ALL—Statistical leakage analysis and optimization tools
Additional Challenges <50 nm/Beyond 2009	
Leakage as a limiter of manufacturability	ALL—Statistical leakage optimization tools
Uncontrollable CD and doping variability	ALL—Statistical parametric optimization tools
Extreme device and circuit variability	ALL—Architectures fundamentally resistant to variability (redundancy, ECC)
Critical need to integrate RET into design	ALL—RET-aware CAD tools
Package, system, and software variability	ALL—adaptable and redundant circuits that can adapt to these variations
BEOL planarization and dimensional variability	ALL—post-tapeout RET that interacts with synthesis, timing, and P&R

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

VARIABILITY MODELING AND ROADMAP

Since variability is expected to be the source of multiple critical DFM challenges, a systematic method to roadmap required and/or desired variability trends will become a crucial component of the overall Design roadmap. It may also allow for design-manufacturing "co-roadmapping", which may help gather indications of whether our industry should invest in variability reduction or in design productivity improvements. The requirement for such a framework is underlined by the sensitivity of variability-related information for industry participants. Since the design community needs to view variability from their parameter-based perspective, such a variability framework needs to be multi-level, i.e., it needs to cover multiple levels of design abstraction.

A Variability Roadmap Framework (VRF) is being developed by the Design TWG as illustrated in Figure 19. In this Framework the following three levels of abstraction have initially been considered:

- *Circuit/chip level*: this is the abstraction level most relevant to designers. Ideally, timing and power consumption variability for a given circuit would be road-mapped at this level, based on lower-level parametric variations.
- *Device level*: since circuits are composed of devices, at this level device-related parameters are roadmapped, such as the threshold voltage V_t, or the off-current I_{off}.
- *Physical level*: this is the level closest to the design-manufacturing interface, where parameters such as CD or effective device length (L_e), and actual doping level (N_A) are road-mapped. These parameters' variability stems from some of challenging issues enumerated above, including lithography hardware resolution limitations, and the inability to control the exact number of dopants in a channel.

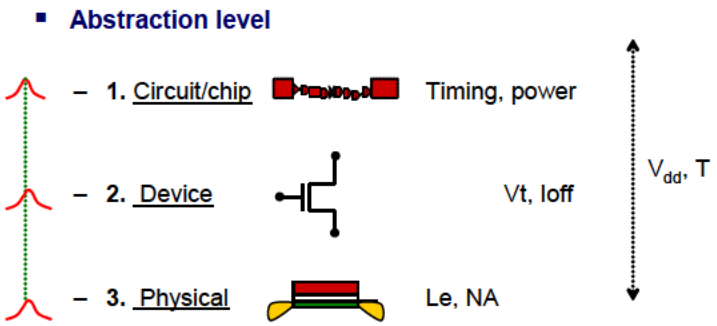


Figure a Possible variability abstraction levels ADDED

In this framework, the modeling process can be symbolically described as

$$\Delta \text{ outputs} = \text{model } (\Delta \text{ inputs}) \qquad [1]$$

Based on published approximated models, this model is based on a simplified gate + wire circuit slice where parameters are decomposed into gate-related and wire-related parameters. Performance is analytically modeled in the current model as total delay, which in turn is decomposed into gate delay and wire delay. Delay variability is modeled as a delta that is statistically computed from a statistical distribution of individual delay values that stems from "simulating" distributions of the input parameters in a Monte Carlo style. Model inputs include gate channel length and width, and oxide thickness; wire width, length, and thickness; ILD thickness, and wire sheet resistance.

Among other applications, this framework will be used for circuit performance variability trending. For example, estimated delay variability will be estimated over time for two possible scenarios: 10% required CD (actual channel feature length) variation, and 20% required CD variation. In this particular illustration, the model could indicate that circuit performance variability does not seem to vary very significantly with the CD tolerance requirement, which might suggest the possibility of a relaxation of the requirement.

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Table 13 Near-term Breakthroughs in Design Technology for AMS

Field Of Breakthrough	*2003*	*2004–2005*	*2006–2007*
Specification, validation	**Mixed-signal description languages**	**Multi-language support**	**Complete specification-driven design flow**
Architectural design	**Algorithm-oriented design**	**Language-based performance evaluation**	**Synthesizable AMS description**
Mixed A/D and RF physical design	**Procedural layout generation**	**Design centering, performance estimation**	**Constraint-driven synthesis: behavior to layout**
Parasitic extraction, modeling, simulation	**EMI simulation**	**2D/3D modeling, order reduction**	**Fault-tolerant circuit architectures, robustness**

Table 14 Design Process Challenges

Challenges ≥50 nm/Through 2009	*Summary Of Issues*
Silicon Complexity: devices and interconnects	All—Exponential increase in leakage power S, P, A—Power density and distribution All—Technology and library characterization S, P, A—High-frequency noise analysis S, P, A—Transmission-line interconnects All—eDRAM, eFPGA, SiGe, optical, MEMS
System Complexity: number of states, design diversity	S, P—Verifying systems with exploding number of states S, P, A—Concurrent multi-factor analysis and optimization S, P—Scalable algorithms S, A—Design and test of mixed analog and digital designs All—Complex package analysis S, A—Integrating A/D tools
Design Productivity	S—Integrating third party components S, P—Design tool interoperability S, P—Early analysis and verification methods
Time-to-Market	S, A—Support for platform-based design S, P, A—Exploiting parallel processing
Challenges <50 nm/Beyond 2009	
Manufacturability	All—Cross-chip variability All—Sub-wavelength mask correction (AltPSM, OPC, RET) All—Design for yield and manufacturability All—Standards for sharing design and manufacturing data
System-level Design	S—Common hardware/software (HW/SW) representation S—SW synthesis, HW/SW optimization

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

Table 14 summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S = SOC, P = MPU, A = AMS, M = Memory). The remainder of this section gives explanatory comments.

Table 15 System-level Design Challenges

Challenges ≥50 nm/Through 2009	*Summary Of Issues*
System complexity	S—Higher-level abstraction and specification S—Dynamism and softness S, A—System-level reuse S, A, P—Design space exploration and system-level estimation S—Efficiency of behavioral synthesis and software compilation S—Automatic interface synthesis
System power consumption	P, S—Energy-performance-flexibility trade-offs P, S—Novel data transfer and storage techniques
Integration of heterogeneous technologies	S, P, A—Codesign (HW–SW, chip-package-board, fixed-reprogrammable) A, S—Non-scalability of analog circuits; analog behavioral modeling and synthesis P, S, A—Top-down implementation planning with diverse fabrics (digital, AMS, RF, MEMS, EO, SW)
Embedded software	S—SW–SW codesign onto highly programmable platforms S—System capture and abstraction S—New automation from high level description to HW–SW implementations, including SW synthesis S—Formal verification for SW S—HW–SW coverification
Links to verification, test and culture	S—Integration-oriented verification and test architectures S, P, A—Divergent design practices and cultures
Additional Challenges <50 nm/Beyond 2009	
System complexity	S, P—Communication-centric design and network-based communications on chip All—Design robustness
System power consumption	P—Non-scaling of centrally organized architectures S—Building large systems from heterogeneous SOCs
Integration of heterogeneous technologies	S—Total system integration including new integrated technologies (MEMS, electro-optical, electro-chemical, electro-biological or organic)

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

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Table 16 Logical, Circuit, and Physical Design Challenges

Challenges ≥50 nm/Through 2009	*Summary Of Issues*
Efficient and predictable implementation	P—Scalable, incremental analyses and optimizations P, S—Unified implementation/interconnect planning and estimation/prediction P, S—Synchronization and global signaling S, A, P—Heterogeneous system composition P, S—Links to verification and test
Variability and design-manufacturing interface	P, S, A—Uncertainty of fundamental chip parameters (timing, skew, matching) due to manufacturing and dynamic variability sources All—Process modeling and characterization P, S—Cost-effective circuit, layout and reticle enhancement to manage manufacturing variability
Silicon complexity, non-ideal device scaling and power management	P, S—Leakage and power management All—Reliability and fault tolerance, soft error P, S—Analysis complexity and consistent analyses / synthesis objectives
Circuit design to fully exploit device technology innovation	P—Support for new circuit families that address power and performance challenges P, S—Implementation tools for SOI A, S—Analog synthesis
Additional Challenges <50 nm/Beyond 2009	
Efficient and predictable implementation	S—Reliable, predictable fabric- and application-specific silicon implementation platforms S—Cost-driven implementation flows
Variability and design-manufacturing interface	P, S, A—Increasing atomic-scale variability effects
Silicon complexity, non-ideal device scaling and power management	P—Recapture of reliability lost in manufacturing test
Circuit design to fully exploit device technology innovation	P, A—Increasing atomic-scale effects P, S, A—Adaptive and self-repairing circuits A, S—Low-power sensing and sensor interface circuits; micro-optical devices

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

DESIGN VERIFICATION UPDATED

Design verification is the task of establishing that a given design accurately implements the intended behavior. The prevailing view by much of the semiconductor industry is that design verification plays a relatively minor supporting role to the design process. (Possibly, such a view is reflected in the very structure of this document.) Current reality, however, is markedly different. Verification has become the dominant cost in the design process. On current projects, verification engineers outnumber designers, with this ratio reaching two or three to one for the most complex designs. Design conception and implementation are becoming mere preludes to the main activity of verification.

This unfortunate situation is the result of two processes. First, the functional complexity of modern designs is increasing at a breathtaking pace. Design size is growing exponentially with Moore's Law. In the worst case, functional complexity, as measured by the number of distinct states of the system that must be verified, can grow exponentially in the size of the design, producing a doubly exponential blow-up.[1] Second, the historically greater emphasis on other aspects of the design process has produced enormous progress (automated tools for logic synthesis, place-and-route, and test pattern generation, etc.), leaving verification as the bottleneck. Without major breakthroughs, verification will be a non-scalable, show-stopping barrier to further progress in the semiconductor industry.

The overall trend from which these breakthroughs will emerge is the shift from ad-hoc verification methods to more structured, formal processes. The mainstream methodology used in industry today attempts to verify the functionality of a system design by repeatedly building models, simulating them on an ad hoc selection of vectors, and then patching any bugs that happen to be triggered. However, such a trial-and-error verification methodology lacks the metrics that make the verification process predictable and repeatable. More structured approaches relay on planning the verification effort, modeling and measuring coverage as verification tasks are being executed. This deliberate verification strategy makes use of simulation engines at the unit, chip and system level as well as formal engines at the unit level.[2] Formal verification techniques are starting to gain momentum and they are complementing simulation methods in the process of verification. Formal methods span multiple aspects of verification: from a formalized verification process, to a formal notation for specification and verification and formal solvers and proof techniques.

In tackling the complexity of very complex systems, and in particular, systems-on-a-chip, a "hierarchical" verification methodology seems to be needed, along with the development of specific methods and tools associated with each level of the hierarchy. In this context, the design and implementation pyramid can be summarized roughly as follows: 1) Module level (structural, dataflow and behavioral module description and synthesis) where the verification tools must prove the correctness of systems in the range of 10K to 500K logic gates. 2) Sub-System level (for the most part, this is the result of structural composition of modules) producing systems with 100k to 10M logic gates. 3) System/Full chip level (obtained by composing sub-systems) producing designs of 1M to more than 100M logic gates. In a hierarchical verification approach different verification techniques would be used at each design level: At the module level, the goal is to produce high-quality modules through the formal verification of properties and assertions. For sub-systems, verification would entail a mix of property verification for the interface and simulation with constrained random pattern generation. Property verification at the sub-system level could be achieved in the future, for instance, through the definition of aggressive automatic design-abstraction techniques, and of automatic techniques for the refinement of such abstractions, driven by counter-examples, which would allow proving sub-system properties while posing a minimum demand on the verification engineering resources. At the system level, simulation-based assertion checking paired with coverage metrics seem the most appropriate among the techniques available. Technological progress depends on developing rigorous and efficient methods to achieve these verification goals (the bulk of formal and semi-formal verification research today), and eventually codifying reliable, predictable engineering practices that simplify many verification challenges. Tables 17 and 18 summarize the main challenges in design verification. The remainder of this section provides explanatory comments.

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[1] There are many variations that arrive at this conclusion. For example, a new design that requires doubling the number of transistors on a chip is likely to also double the number of latches on the chip, which likely means roughly squaring the number of reachable states of the design. This analysis assumes that the correct behavior can be verified by examining the set of reachable states of the system, or a similar computation. If verifying correct behavior requires reasoning over sequences of states, the computational challenge will be even worse.

[2] This argument applies to hardware emulation as well as to conventional simulation. Hardware emulation buys several orders of magnitude improvement in "simulation" speed, providing an invaluable aid to verification. It also often allows an earlier start to system integration and software development. An emulation system, however, still runs vectors one-at-a-time, so it cannot possibly provide a scalable, long-term solution to the verification problem.

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Table 17a Design Verification Challenges—Near-term UPDATED

Challenges ≥50 nm/Through 2009	*Summary Of Issues*
Increased verification capacity	S, P, A—Verification complexity is double-exponential in design size S, P, A—Need high coverage as well as capacity to handle large designs S, P, A—Semi-formal techniques
Robust verification tools	S, P, A—Highly unpredictable verification algorithms demand improved heuristics and characterizations of problem difficulty
Verification metrics	S, P, A—Code, structural and functional coverage S, P, A—Realistic bug models are needed, along with algorithms to determine bug coverage
Software verification	S—Software intrinsically more difficult to verify S—Traditional software verification techniques inapplicable S—Integrated hardware/software systems S—Design for verifiability
Verification reuse	S—Must allow reuse of verification of IP blocks S—Specify abstract behavior of IP blocks S—Specify environmental constraints of IP blocks S—Hierarchical verification algorithms
Verification methodology	S, P—Different cost-benefit trade-off (higher cost acceptable) S, P—Need exceptionally high capacity S, P—Must be very predictable due to long design cycle and pipelined development teams
Design for verifiability	S,P—Will be necessary sooner than for other system drivers; specialized techniques are likely
Greater concurrency	S,P—Far more concurrency in new processors greatly increases verification complexity

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

DESIGN VERIFICATION CHALLENGES—NEAR TERM (>50 nm)

Many of the most important challenges for verification are relevant to most or all system drivers. In the near-term, eight primary issues (1–8 below) center around making formal and semi-formal verification techniques more reliable and controllable. In particular, major advances in the capacity and robustness of formal verification tools are needed, as well as meaningful metrics of the quality of verification. In the longer term, four primary issues (9–12 below) center around raising the level of abstraction and broadening the scope of formal verification. These longer-term issues are actually relevant now, but the near-term challenges are already crises. In general, all of the verification challenges apply to SOC. In addition, the following near term challenges are especially important for SOC. MPUs present a distinct verification challenge, both because of their leading-edge complexity, and because of the unique economics of an incredibly complex design that is produced in incomparably high volumes. As a result, different, domain-specific verification challenges and opportunities exist, both near- and long-term.

1. Capacity—Figure 19 relates the current landscape of available verification tools and design granularity. The horizontal axis presents increasing design complexity, from module components, to sub-systems, multiple modules connected together providing some high-level functionality, to systems, complete systems-on-a-chip integrating multiple functionalities on a single die, and to the application software running on the system; the vertical axis indicates the verification techniques available. Conventional simulation-based methods[3] span a large range; they are practically used

[3] *"Conventional simulation" here refers to verification techniques based on simulating possible behaviors of the system one-at-a-time. "Formal verification" refers to any techniques, such as symbolic simulation, symbolic trajectory evaluation, model checking, and theorem proving, that provide the effect of an exhaustive analysis of all possible behaviors of the system. An occasionally useful distinction can be drawn between theorem-proving approaches, which tend to provide the greatest expressive and analytical power at the expense of requiring substantial human expertise, versus the other approaches, which tend to trade off theoretical power for greater automation. "Semi-formal" refers to a broad range of techniques that attempt to handle larger designs by sacrificing complete, formal coverage, usually by blending techniques from formal verification and conventional simulation.*

for anything from module to full-system verification. However, the quality of the results varies: For small modules it is possible to run many simulation vectors in a short time and thus achieve a fairly good coverage of the design under verification. At the system level the performance of simulation is very low, since the complexity of the algorithms involved is linear on the design size and the number of simulation vectors. Thus, for very complex systems, only a few simulation vectors can be run within a reasonable amount of time, and the fraction of design coverage they provide is even much smaller considering the complexity of the system that is being simulated. Formal verification can achieve very high coverage, granted that a broad set of properties are in place, targeting the various aspects of the system. The downside of these techniques is their limited scalability that usually cannot go above the module level. Semi-formal verification attempts to blend formal and simulation-based techniques. As the Figure shows, they present generally better capacity, sometimes at the cost of lower design coverage. For very complex systems and when the project involves software development, software tools are insufficient to provide any confidence in the correctness in the system. Solutions used at this level include FPGA-based rapid prototyping and/or a silicon production of the hardware. The challenge is to create new solutions that together provide high coverage at all levels of complexity. The two orthogonal methodologies of formal verification and simulation in use today have both important downsides: while formal tools can only handle small to medium size designs, simulation-based tools can simulate designs of almost arbitrary complexity, but they provide a vanishingly small coverage even with extremely long simulation times. Emulation and rapid hardware prototyping perform several orders of magnitude faster than software logic simulators, thus providing the ability to achiever higher coverage. However, the improvement is only a constant factor and does not scale at the same rate as design complexity.

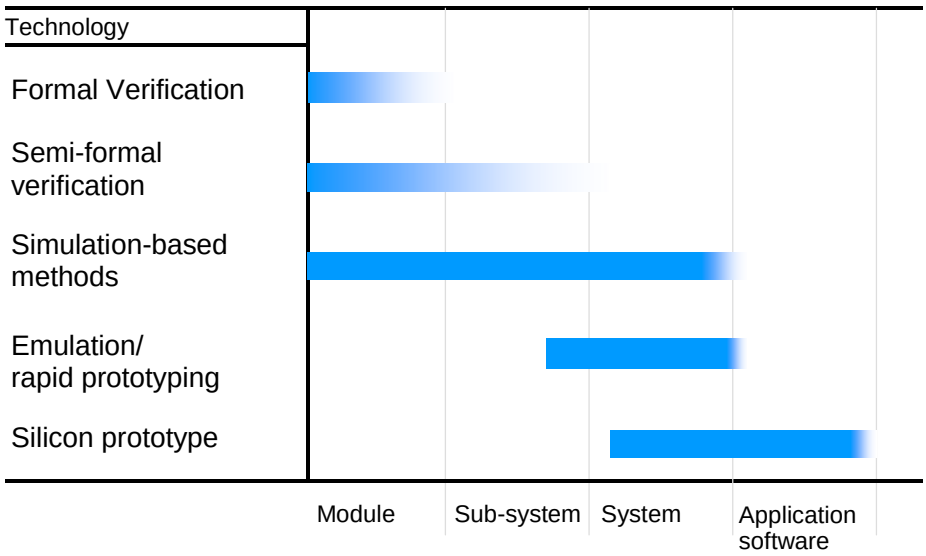


Figure b Current Verification Tool Landscape ADDED

2. Robustness— A crucial aspect of current verification solutions that is not shown in Figure 19 is their reliability. On one hand, simulation-based methods are fairly predictable, because their execution time per simulation vector scales linearly with design complexity. Their performance, thus, will linearly decrease as we move towards the most complex design levels. Emulation techniques present a similar trend, while silicon prototypes are consistently reliable. On the other hand, formal verification techniques depend on highly temperamental heuristics, in order to cope with the complexity of the verification problem. For any given pair of design and verification algorithm, even an expert can be hard-pressed to determine whether the verification algorithm will complete. Common measures of problem size, such as transistor, gate, or latch counts, correlate only vaguely with formal verification complexity; it is easy to find designs with less than one hundred latches that defy all known verification methods, as well as designs with thousands of latches that can be verified easily. Such unpredictability is not acceptable in a production environment. A crucial verification challenge is to make the verification process more robust. This can take the form of either improved heuristics for the verification algorithms, or improved characterization of the difficulty of verifying a given design, leading to methodologies for easy-to-verify design.

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3. Verification metrics— An important near-term verification challenge is the need to quantify the quality of the verification effort. In particular, a meaningful notion of coverage is needed. Multiple types of coverage metrics are available, each with their own benefits and limitations:

- Code coverage is concerned with measuring which fraction of the design source code has been stimulated during simulation (for example, lines of code, expression coverage). Variants of line coverage are concerned with covering all components of expressions in the code, or all cases in switch statements, etc…The limitation of line coverage is in its projecting a dynamic simulation execution to a static source code, thus missing many potential problems that could be still present because of all the possible paths of execution available during simulation.

- Structural coverage, such as state or pair arc coverage. State coverage focuses on the finite state machines of the design and measures which states have been covered by simulation. However, it is generally not possible to consider the whole design as a single finite state machine, rather only a few machines are considered by coverage. The downside is that while the coverage provides good results for single machines, combinations of states resulting from products of multiple machines are not considered.

- Functional coverage targets each of the design's functionalities. Since these differ for each distinct design, the specific definition needs to be provided by the verification team based on the design's specification. The quality of the result is thus dependent also on the quality of the coverage definition.

Code and structural coverage metrics quantify aspects of the designs that do not necessarily imply its correctness. Functional coverage potentially could achieve this goal of measuring the fraction of a design's functionality that has been verified. However, the challenge is in the definition of a good functional coverage. In the current landscape, there is a lack and a need for a common foundation metric for functional coverage in a unified environment, so that achieving a certain level of coverage in a design could have a meaning beyond the specific functional coverage used in that particular design. Moreover, there is no general methodology in designing the functional coverage units; an abstract fundamental model to use as a guideline during the development is needed and could support the development methodology. Ultimately, there is a need for a defect model for functional bugs, much like there is a defect model for testing, to support the development of coverage and a unified metric for verification.

4. Software— The verification of complex systems, such as systems-on-a-chip (SOC) entails the verification of the hardware components, of the hardware/software interface and of the application software running on the system. The software components of an SOC can be divided into application software, running over an operating system, or, in general, a layer that is hardware-independent, and a lower-level hardware-dependent software, such as drivers, etc. Because in these systems the software layer could provide much of the functionality, a major challenge in SOC verification is how to verify software and the hardware/software interface. Presently, software development is not as rigorous as hardware development in terms of design reviews, analysis tools, and testing. Software is intrinsically harder to verify: it has more complex, dynamic data and an enormous state space. Techniques used today include "on-chip-verification", that is, running the software on a production version of the hardware components to verify the software. While this technique is required by the intrinsic complexity of software, and allows very fast simulation, its downside is that software verification can only happen very late in the design cycle. Classical formal techniques for software verification are still too labor-intensive to be widely applicable for SOC, to attack systems with such large state spaces, and require very aggressive abstraction techniques. The verification of the hardware/ software interface is a challenge on its own, since it requires verifying the two domains together, a task of enormous complexity. To make this task manageable, there is a need for techniques that provide a proper abstraction of the interface activity, verification techniques to check the correctness of the abstracted driver layers, and assertion checking for drivers' invariants at the non-abstract level. The near-term challenge will be to develop techniques that allow verification of even elementary and low-level pieces of software. The longer-term challenge will be to develop robust verification methods for software, and hardware/ software interfaces, as well as an understanding of design-for-verifiability as applied to software.

5. Reuse—Pre-designed IP blocks promise to allow assembling SOCs of unprecedented complexity in a very short time. The major challenge is to develop the corresponding verification methodology to allow rapid verification of a system assembled from pre-designed (and pre-verified) blocks. Key issues are how to rigorously and completely describe the abstract behavior of an IP block, how to describe the environmental constraints assumed by the IP block, and how to exploit the hierarchy to simplify verification. Some IP components have started to ship with associated verification IPs, from standard protocols verification IPs, to abstract models for general IP blocks, protocol checkers to check environmental constraints surrounding the block, to transaction generators. However, these are still preliminary attempts,

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while there is a need for consistent availability of verification IPs associated with any IP block in order to develop a reuse methodology. Besides verification components associated with IP blocks, there is some availability of independent verification IPs, such as environment generators for specific protocols. Near-term progress will most likely occur for standardized IP interconnects, such as on-chip buses, but the general problem for arbitrary IP block interfaces must be eventually solved.

6. Specialized verification methodology— The biggest issue in design verification is that all currently known algorithmic solutions are running out of capacity with respect to the designs being developed today. The only foreseeable way to overcome this issue in the short term is with an adequate verification methodology. Current trends in this direction include coverage-driven verification, both for simulation-based verification and semi-formal verification, more in use today than in the past; specification documents in formal notation, that make easily available the set of formal properties to be verified in the implementation; coverage model templates. Many challenges are still to be solved to obtain a sufficiently robust and complete methodology. For instance, there is a need for ways to obtain consistent abstraction techniques of design components, interfaces, etc. that do not drop key aspects of the design in the abstraction, and, obviously, these aspects depend on the context where the abstraction is used. Formal specifications are starting to be developed; however, a major challenge is the completeness of such specifications, a challenge that becomes even more compelling in a world where different IP components in the same system are developed by completely unrelated design teams. The acceptance of new verification methodologies is progressing slowly, even the basic deployment of formal properties in a design is a challenge since it often requires a global understanding of some specific aspect of a design, which involves additional effort on the development team. Finally, verification methodology is ultimately an evolving target that can only provide a risk reduction to the development, not a guarantee of correctness through a well-defined recipe.

7. Specialized design-for-verifiability— To enable more effective verification, a few specialized activities in design for verifiability are already foreseeable. For instance, facilities for software and/or hardware debug can be put in silicon. In this direction there is preliminary work being done on self-checking processors, in which a small watchdog processor verifies the correct execution of the main processor. For mixed-signal designs, the insertion of loop-back modes to bypass the analog portion of the design allows to verify the system as a fully digital design. The use of synchronizers, in particular at the software level forces tasks not to proceed independently past the synchronization points, creating checkpoints for verification and reducing the searchable state space. In MPU designs synchronizers would reduce the complexity of verifying speculative execution systems. The challenges in this area will be the development and the adoption of design-for-verifiability techniques for a few major domains. Efforts are also made in developing design methodologies by incremental refinement to produce systems that are correct-by-construction; however, it is not clear how automatic the refinement process can be made, while, on the other hand, manual intervention is a potential source of design errors.

8. New kinds of concurrency—As MPU designs become more complex, new kinds of concurrency become important. Already, many of the bugs that elude verification relate to cache coherence and other concurrency issues. New designs greatly complicate the verification process by increasing the level of concurrency via techniques such as chip-level multiprocessing and on-chip cache coherence protocols, and simultaneous multithreading. In the future, new kinds of concurrency both at the intra-processor level and in multi-processor systems, or in other hardware context will present difficult challenges to verification. There is a need for new models of failure to grasp this additional level of complexity. The solution will probably require a mix of hardware and software techniques to reduce the complexity of the interactions and make the concurrent protocols verifiable.

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Table 17b Design Verification Challenges—Long-term UPDATED

Additional Challenges <50 nm/Beyond 2009	
Design for verifiability	S, P, A—New methodology needed S, P, A—Characterize and minimize performance and area impact
Higher levels of abstraction	S, P, A—New algorithms needed S, P, A—Complexity of designs enabled by higher-level design S, P, A—Equivalence checking vs. RTL
Specification for verifiability	S, P, A—Specifications of correctness will become unmanageable S, P, A—Need to understand what kinds of specifications are most understandable S, P, A—Need to consider how to make specifications modular and modifiable
Verification in the presence of non-digital effects	S, P, M, A—Hybrid systems verification for analog effects S, P, M, A—Hybrid systems verification for analog properties S, P, M, A—Verification of probabilistic systems
Heterogeneous systems	A, S—How to model, analyze, and verify MEMS, EO devices, and electro-biological devices
Analog-Mixed signal	A—Extremely primitive state-of-the-art forces difficult hybrid-systems issues into near term
Soft failures	S, P, M—Reliable systems in face of soft errors
Verification of redundancy	S, P, M—Sufficient reliability in face of soft errors

This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

DESIGN VERIFICATION CHALLENGES—LONG TERM (<50 nm)

1. Design for verifiability— As the solutions to the near-term challenges produce understandings of what is easy or hard to verify and how design errors occur, the longer-term challenge arises of how to codify that understanding into producing easy-to-verify designs. Without design-for-verifiability, it is unlikely that verification will be tractable for the designs envisioned beyond 2007. Major changes in methodology may be required, and some performance degradation is likely. A useful analogy is to sequential testability, where the computational intractability of sequential ATPG has resulted in near-universal adoption of scan-based testing.

2. Higher levels of abstraction— As design moves to a level of abstraction above RTL, verification will have to keep up. The challenges will be to adapt and develop verification methods for the higher-levels of abstraction, to cope with the increased system complexity made possible by higher-level design, and to develop means to check the equivalence between the higher-level and lower-level models. This longer-term challenge will be made much more difficult if decisions about the higher-level of abstraction are made without regard for verification (e.g., languages with ill-defined or needlessly complex semantics, or a methodology relying on simulation-only models that have no formal relationship to the RTL model).

3. Specification for verifiability—A continuing challenge for design verification is how to specify the desired behavior of a design. Current available notations for specification are not powerful enough to approach this problem in a generalized way. A deeper understanding of what makes a specification clear or opaque, modifiable or intractable will be needed to guide development of languages that are used to specify ever more complex designs. For instance, there is a need for automatic ways to check the self-consistency of a specification document, so that different specifications don't state conflicting requirements. In addition, specific training is needed for designers to use these specification notations and to be able to develop formal specifications consistently.

4. Verification in presence of non-digital effects— To date, design verification has mainly focused on the discrete behavior of digital systems. The dual challenges of silicon complexity and system complexity will force future verification efforts to analyze a broader class of aspects. The complexity of silicon integrated circuit systems is making the clean, digital abstraction of a VLSI system increasingly precarious. Analog electrical effects will impact performance and, eventually, functionality. The existing simulation methodology (SPICE) for analyzing these effects is too slow, and

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may become unreliable as smaller devices become increasingly sensitive to process variations. In this direction there is preliminary work being done on architectural simulation of microprocessors, in which the high-level architectural simulator, interacts with a low-level context-specific simulator to acquire metrics such as timing and voltage, which are then fed back for overall system evaluation with minimal performance impact. In the long term, formal techniques will be needed to verify these issues at the boundary of analog and digital, treating them as hybrid systems.[4] Similarly, at the highest-levels of design, system complexity dictates that future verification tasks will likely require specifying and verifying analog and probabilistic behaviors (such as quality of service guarantees in a network processor). Thus, there will be the challenges of hybrid systems and probabilistic verification.

5. Heterogeneous systems— The development of new technologies that are placed side-by-side to a digital design in a silicon die presents a whole set of new challenges. Examples are MEMS, electro-optical devices, and electro-biological devices. These new components will require modeling of both the interface between the digital portion and the non-digital components and a proper abstraction of the non-digital system behavior in order to still be able to verify the digital portion of the system.

6. Analog-Mixed signal— Today analog systems are mostly verified through classic systems analysis tools for continuous systems, through system modeling and analysis in the frequency domain. The bulk of verification happens in the post-design phase, by verifying test dies with analog lab equipment. Mixed-signal designs undergo separate verification activities for the digital and analog portions. In the future, mixed-signal systems will become a more relevant fraction of all silicon developments, bringing the development of proper verification methodologies in this arena to a critical level. The challenge in this area is in tying the verification of the analog portion of a system with its digital counterpart. One of the requirements in achieving this goal is in bridging the current performance gap between digital and analog simulation.

7. Soft failures— In the long term there is a need to develop verification techniques that can provide information on a system's reliability in presence of soft errors.

8. Verification of redundancy— The quantifiable evaluation of the reliability of a redundant system, and the estimation of the level of redundancy needed to achieve a certain level of reliability is particularly important for safety-critical application. In the future, the increased complexity of electrical effects in a system performance and correctness will make these evaluations even more important, even for non safety-critical designs.

[4] *Hybrid systems have both complex discrete behavior (e.g., finite-state machines) as well as complex continuous behavior (e.g., differential equation models). The discipline borrows techniques from both discrete formal verification as well as classical control theory.*

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Table 18 Design Test Challenges

Challenges ≥50 nm/Through 2009	*Summary Of Issues*
Effective speed test with increasing core frequencies and widespread proliferation of multi-GHz serial I/O protocols	P, S—Continuation (avoidance) of at-speed functional test with increased clock frequencies
	P, S—At-speed structure test with increased clock frequencies
	P, S, A—DFT, test and on-chip measurement techniques for multi-gigahertz serial I/Os and non-deterministic interfaces
Capacity gap between DFT/test generation/fault grading tools and design complexity	P, S—Better EDA tools for advanced (open, delay, etc.) fault models
	P, S—DFT to enable low-cost ATE
	P, S—Non-intrusive logic BIST (including advanced fault models)
	A—AMS DFT/BIST, especially at beyond-baseband frequencies
Quality and yield impact due to test process and diagnostic limitations	P, S—Power and thermal management during test
	P, S—Fault diagnosis and design for diagnosability
	S—Yield improvement and failure analysis tools and methods
	All—Increasing difficulty to fault isolate and root cause yield limiting defects
Signal integrity testability and new fault models	P, S—Signal integrity (noise, interference, capacitive/inductive coupling, etc.) testability
	A—Fault models for analog (parametric) failures
SOC and SIP test	S—Integration of SOC test methods into chip-level DFT
	S—Integration of multiple fabric-specific test methodologies in cost-effective manufacturing flows
	A—DFT, BIST and test methods compatible with core-based SOC environment and constraints
	M—Embedded memory (DRAM, SRAM, Flash) built-in self-diagnosis and self-repair
	All—Test reuse in context of higher integration
Additional Challenges <50 nm/Beyond 2009	
Integrated self-testing for heterogeneous SOCs and SIPs	A—Test of multi-gigahertz RF front ends on chip
	S—Use of on-chip programmable resources for SOC and SIP self-test
	S, A—Dependence on self-test solutions for SOC (including RF and analog)
	A— (Analog) signal integrity test issues caused by interference from digital to analog circuitry
	S—Test methods for heterogeneous SOC and SIP including MEMS and EO components
Diagnosis, reliability screens, and yield improvement	A—Diagnosis and failure analysis for AMS parts
	P, S—Electrical automated fault isolation techniques below gate level
	P, S—Design for efficient and effective burn-in to screen out latent defects
	P, S—Quality and yield impact due to test equipment limits
	P, S—New timing-related fault models for defects/noise
Fault tolerance and on-line testing	P, S—DFT and fault tolerant design for logic soft errors
	S—Logic self-repair using on-chip reconfigurability
	S—System-level on-line testing

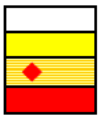
This table summarizes challenges to the design process advances implied by the above four trends. Each challenge is labeled with a list of the most relevant system drivers (S—system on chip, P—microprocessor, A—analog/mixed-signal, M—memory).

Table 19 Additional Design Technology Requirements UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009	2012	2015	2018	Driver
	Technology Node		hp90			hp65						
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50	35	25	18	
	MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50	35	25	18	
	MPU Printed Gate Length (nm)	65	53	45	40	35	32	28	20	15	10	
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	14	10	7	
Add	Complexity --> (system) % of memory		47%	50%	53%	55%	58%	61%	65%	65%	65%	
WAS	SOC new design cycle (months)	12	12	12	12	12	12	11	11	10	9	SOC
IS	Productivity --> design cycle (mo) [1]	12	12	12	12	12	12	11	11	10	9	SOC
WAS	SOC logic Mtx per designer-year (10-person team)	1.9	2.5	3.3	4.3	5.4	7.4	10.6	24.6	73.4	113	SOC
IS	Productivity --> Logic Mtx per designer-year (10-person team [2]	1.9	2.5	3.3	4.3	5.4	7.4	10.6	24.6	73.4	113	SOC
Add	Productivity --> % software in design cycle (mo[3])	---	60%	60%	60%	60%	60%	60%	60%	60%	60%	SOC
WAS	SOC dynamic power reduction beyond scaling (X)	0	0.1	0.1	0.2	0.2	0.2	0.2	6	4.7	8.1	SOC
IS	SOC dynamic power reduction beyond scaling (X) [4]	0	0.1	0.1	0.2	0.2	0.2	0.2	6	4.7	8.1	SOC
WAS	SOC standby power reduction beyond scaling (X)	0.37	1.4	2.4	3.4	5.1	6.4	8.73	18.8	44.4	232	SOC
IS	SOC standby power reduction beyond scaling (X) [5]	0.37	1.4	2.4	3.4	5.1	6.4	8.73	18.8	44.4	232	SOC
WAS	%Test covered by BIST	20	20	25	30	35	40	45	60	75	90	MPU, SOC
IS	Manufacturing interface --> %logic Test covered by BIST [6]	20	20	25	30	35	40	45	60	75	90	MPU, SOC
Add	Design cost --> improvement, normalized[7]	---	100%	86%	120%	56%	78%	105%	143%	149%	155%	SOC
Add	Area density --> increase (X) [8]	---	1	1.4	2	2.8	4	5.6	15.6	43.8	122.8	SOC
Add	Area density --> increase beyond scaling (X) [9]	---	0	0	0	0	0	0	0	0	0	SOC

Mtx—Million transistors

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Added Notes for Table 19:

[1] Number of months from design requirements definition to tape-out.
[2] Number of logic transistors in a chip divided by the number of person-years in a design team, for a 10-person team.
[3] % of software design effort as the number of software development person-years versus the total number of person-years.
[4] % of dynamic power savings on top of the % of active power savings derived from technology scaling..
[5] % of leakage power savings on top of the % of leakage power savings derived from technology scaling.
[6] % of the logic gates' stuck-at faults covered by BIST.
[7] % improvement in design cost per year for low-power PDA SoC driver. It accounts for all design technology improvements.
[8] Increase in absolute area density (number of gates per unit chip area.
[9] Increase in area density on top of density improvement coming from technology scaling (feature reduction).

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Table 20 Design Technology Improvements and Impact on Designer Productivity

DT Improvement	*Year*	*Productivity Delta*	*Productivity (Gates/Desn-Year)*	*Cost of Component Affected*	*Description of Improvement*
None	1990		4K		
In-house place and route	1993	+38.9%	5.55K	PD Integration	Automated block placement and routing.
Engineer	1995	+63.6%	9.09K	Chip/circuit/PD Verification	Engineer than can pursue all required tasks to complete a design block, from RTL to GDSII.
Reuse—small blocks	1997	+340%	40K	Circuit/PD Verification	Blocks from 2,500–74,999 gates.
Reuse—large blocks	1999	+38.9%	56K	Chip/circuit/PD Integration Verification	Blocks from 75,000–1M gates.
IC implementation suite	2001	+63.6%	91K	Chip/circuit/PD Integration EDA support	Tightly integrated tool set that goes from RTL synthesis to GDS II through IC place and route.
Intelligent testbench	2003	+37.5%	125K	SW development Verification	RTL verification tool ("cockpit") that takes an ES-level description and partitions it into verifiable blocks, then executes verification tools on the blocks, while tracking and reporting code coverage.
Electronic system-level (ES-level) methodology	2005	+60%	200K	SW development Verification	Level above RTL, including both HW and SW design. It consists of a behavioral (where the system function has not been partitioned) and an architectural level (where HW and SW are identified and handed off to design teams).
Very large block reuse	2007	+200%	600K	Chip/circuit/PD Verification	Blocks >1M gates; intellectual-property cores
TOTAL		+15,000%			

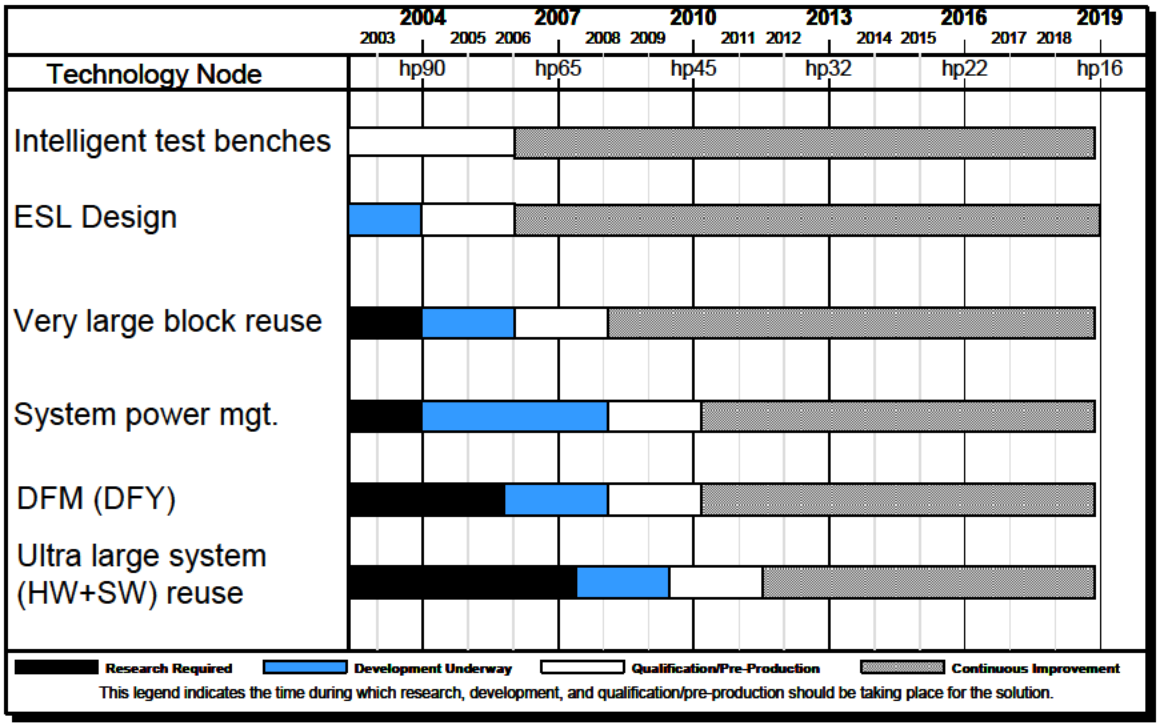


Figure c General Design Potential Solutions ***ADDED DEFINITIONS***

Intelligent test benches—RTL verification tool that takes ES-level description, partitions it, verifies blocks, and tracks code coverage

ESL design—Level above RTL, includes HW and SW design. It consists of a behavioral (before HW/SW partitioning) and architectural level (after)

Very large block reuse—Blocks >1M gates; intellectual-property cores

System power management—Automated design of power management features applied at the system level

DFM (DFY)—Design-For-Manufacturability and Design For Yield automation

Ultra large system (HW+SW) reuse—Reuse of ultra-large blocks, including massively parallel processing HW and SW units (>10M "gates")

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FOLDER 11

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2004 UPDATE

Process Integration, Devices, and Structures

Jointly Sponsored
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PROCESS INTEGRATION, DEVICES, AND STRUCTURES

2004 UPDATE HIGHLIGHTS

The 2004 update for the Process Integration, Devices and Structures (PIDS) section of the ITRS has minor changes and corrections from the 2003 edition. The most notable change is that in the long-term technology requirements tables, the years 2011, 2014, and 2017 have been added, so that all years from 2010 through 2018 are now included. As expected, the parameter values for these added years are generally close to midway between the values for the previous and succeeding years. In Figure 23, which is for low standby power logic, the curve for maximum allowed gate leakage current density (labeled "Jg,limit") has been corrected. In the 2003 edition, this curve was low by a factor of 2 to 3. Even with the correction, the implication of the figure is unchanged, that oxynitride gate dielectric is projected to be unable to meet the gate leakage current limits by 2006.

Link to the 2003 ITRS Process Integration, Devices, and Structures chapter

WORKING GROUP TABLES

Table 46a Process Integration Difficult Challenges—Near-term

Difficult Challenges ≥ 45 nm/Through 2010	*Summary of Issues*
1. High-performance applications: meeting performance and power dissipation requirements for highly scaled MOSFETs	Cost effectiveness, process control, and reliability of very thin oxy-nitride gate dielectrics, especially considering the high gate leakage Difficulty in controlling short-channel effects for highly scaled devices Negative impact of high channel doping needed for highly scaled devices. Also, the difficulty in controlling threshold voltage due to statistical fluctuations in the doping Need to reduce series S/D parasitic resistance Controlling static power dissipation in the face of rapidly increasing leakage: architecture and circuit design improvement and innovation will be needed.
2. Low-power applications: meeting performance and leakage requirements for highly scaled MOSFETs	Early availability of manufacturing-worthy high-κ gate dielectrics is necessary to meet stringent gate leakage and performance requirements. Slow scaling of V_{dd} for low standby power logic will make overall device scaling difficult. Rapid scaling of V_{dd} for low operating power logic will make overall device scaling difficult.
3. Assuring the reliability and implementing into manufacturing of multiple material, process, and structural changes in a relatively short period of time	Multiple material changes projected: high-κ gate dielectric, metal gate electrodes, strained Si, nickel silicide by 2008 or so Elevated S/D (selective epi) Ultra-thin body (UTB) SOI by 2008 or so, followed by multiple-gate structures. Near mid-gap metal gate electrodes will be desirable to set the threshold voltage for UTB SOI. Difficulty in ensuring reliability of all these new materials, processes, and structures in a timely manner

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Table 46a Process Integration Difficult Challenges—Near-term (continued)

4. Implementation of DRAM, SRAM, and high-density nonvolatile memory (NVM) for scaled technologies	DRAM main issues—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities with scaling. Also, difficult lithography and etch issues with scaling NVM, flash—Scaling of tunnel dielectric and interpoly dielectric involves many complex tradeoffs. Dielectric material properties and dimensional control are key issues NVM, FeRAM—Ferroelectric material properties and dimensional control. Sensitivity to IC processing temperatures and conditions NVM, SONOS—ONO stack dimensions and material properties, including nitride layer trap distribution in space and energy NVM, MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions
5. High-performance and low-cost RF and analog/mixed-signal solutions	Signal isolation Optimizing RF/analog CMOS devices with scaled technologies: mismatch, 1/f noise, and leakage with high-κ gate dielectrics High density integrated passive element scaling and use of new materials: Q-factor value for inductors; matching and linearity for capacitors Reduced power supply voltages: degradation in SNR (signal-to-noise ratio) and signal distortion performance Reduced device breakdown voltage in scaled technologies High-frequency devices with increased operating voltage for base station applications Compound semiconductor substrates with good thermal dissipation and process equipment for fabrication at low cost See section on RF and A/MS Technologies for Wireless Communications for detailed discussion of these issues

Table 46b Process Integration Difficult Challenges—Long-term

Difficult Challenges < 45 nm/Beyond 2010	*Summary of Issues*
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate, ultra-thin body [UTB] MOSFETs) with lightly doped body will be needed to effectively scale MOSFETs to well under 20 nm gate length (L_g). Most likely, advanced material solutions such as strained Si (enhanced mobility) channels, elevated source/drain, high-κ gate dielectric, metal gate electrode, etc., will be utilized along with the advanced non-classical CMOS Particularly for the highly scaled UTB MOSFETs required towards the end of the Roadmap, with body thickness well under 10 nm, electrical performance and the impact of quantum effects are not well understood To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced carrier saturation velocity appears to be needed See Emerging Research Devices section for more detail.
7. Dealing with atomic-level fluctuations and statistical process variations in sub-20 nm MOSFETs	Fundamental issues of atomic-level statistical fluctuations for sub-20 nm MOSFETs are not completely understood, including the impact of quantum effects.
8. Identifying, selecting, and implementing new memory structures	Highly scaled, dense, fast, non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness, attaining the very low leakage currents that will be required, and reducing the cell area factor All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc,) are currently unclear.
10. Toward the end of the Roadmap or beyond, identification, selection, and implementation of advanced, beyond-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of beyond-CMOS devices need to extend well beyond CMOS limits. Beyond-CMOS devices need to integrate into a CMOS platform. Integration of the two may be difficult, especially for mixed signal. See Emerging Research Devices sections for more discussion and detail.

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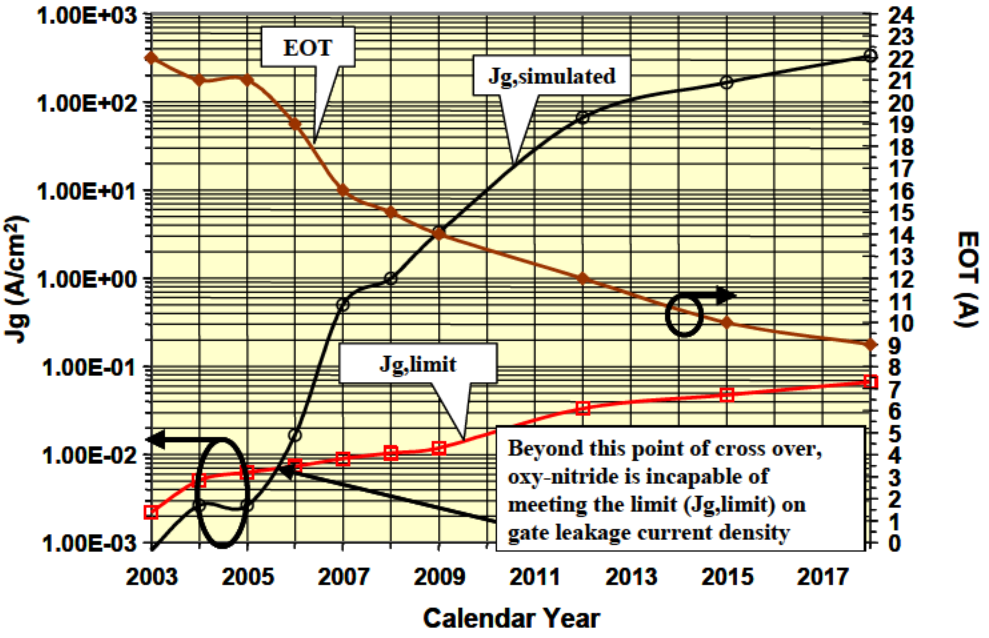


Figure 23 LSTP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling WAS

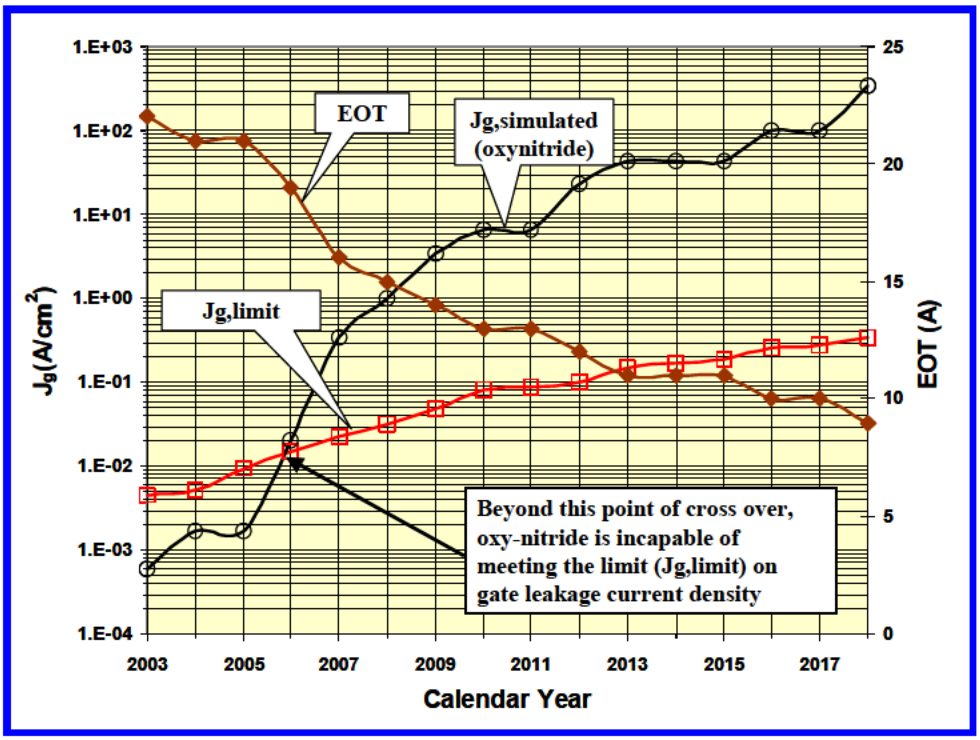


Figure 23 LSTP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling UPDATED

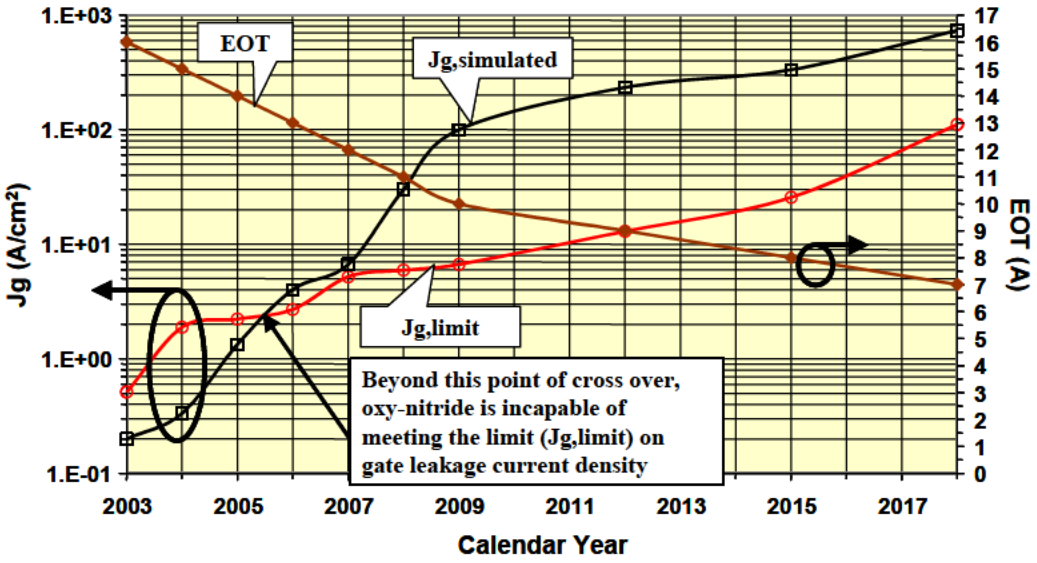


Figure 24 LOP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling WAS

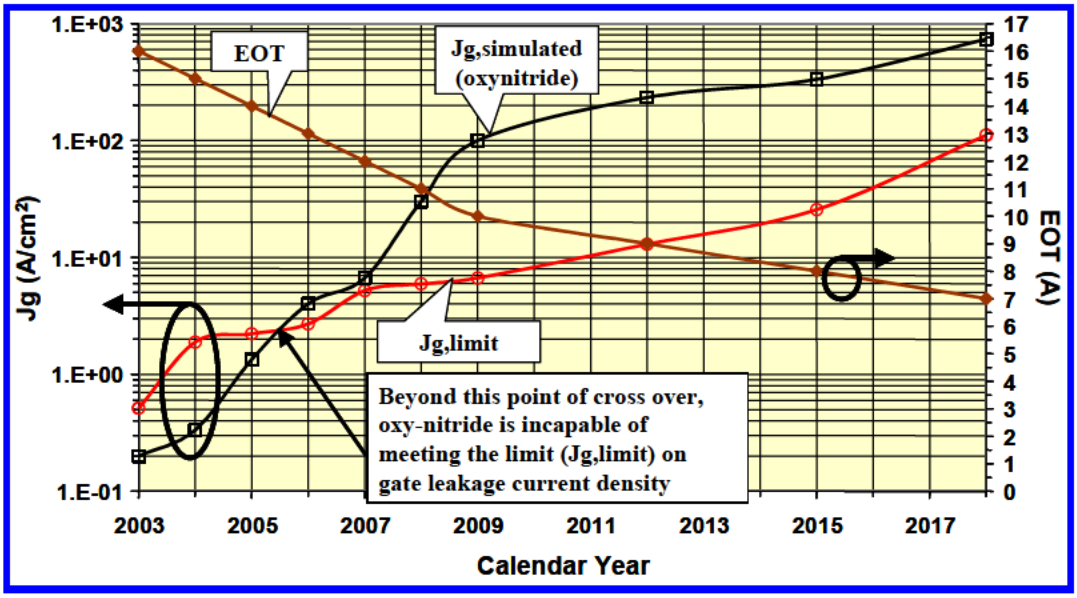


Figure 24 LOP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling UPDATED

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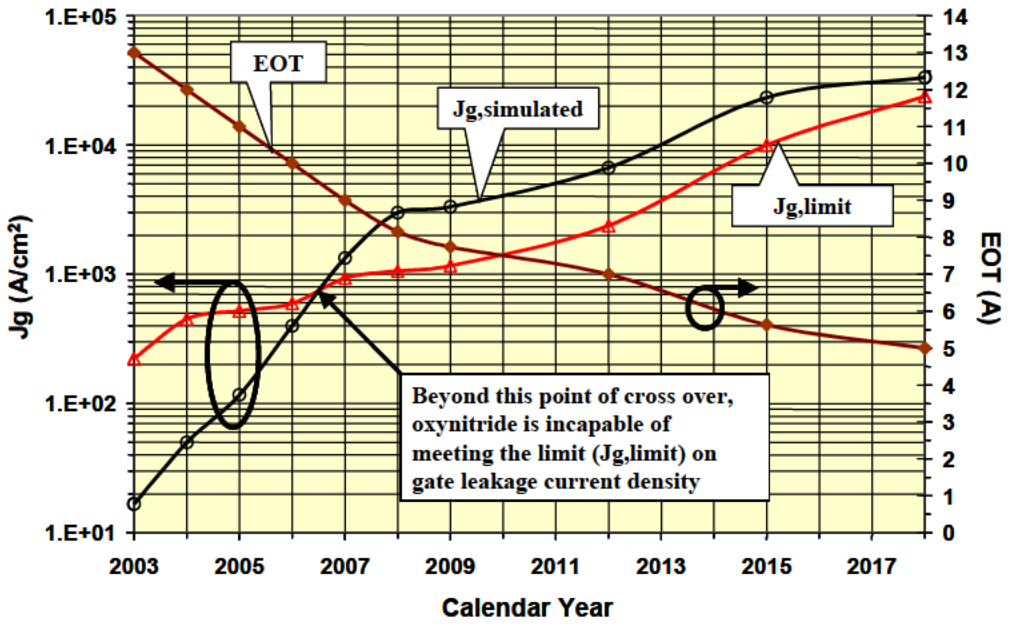


Figure 25 High-performance Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling WAS

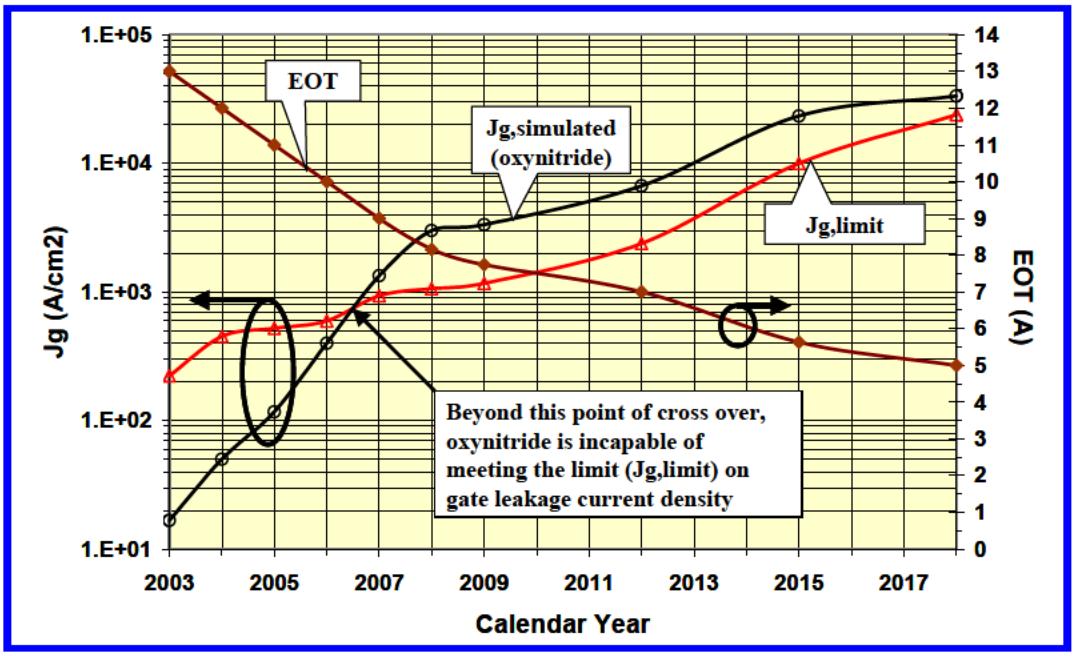


Figure 25 High-performance Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling UPDATED

Table 47a High-performance Logic Technology Requirements—Near-term

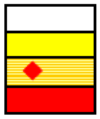
Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Physical gate length high-performance (HP) (nm) [1]	45	37	32	28	25	22	20
EOT equivalent oxide thickness (physical) for high-performance (nm) [2]	1.3	1.2	1.1	1.0	0.9	0.8	0.8
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.4	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	2.1	2.0	1.8	1.7	1.3	1.2	1.2
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	2.2E+02	4.5E+02	5.2E+02	6.0E+02	9.3E+02	1.1E+03	1.2E+03
Nominal power supply voltage (V_{dd}) (V) [6]	1.2	1.2	1.1	1.1	1.1	1.0	1.0
Saturation threshold voltage (V) [7]	0.21	0.20	0.20	0.21	0.18	0.17	0.16
Nominal high-performance NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (µA/µm) [8]	0.03	0.05	0.05	0.05	0.07	0.07	0.07
Nominal high-performance NMOS saturation drive current, $I_{d,sat}$ (at V_{dd}, at 25°C) (mA/mm) [9]	◆ 980	1110	1090	1170	1510	1530	1590
Required "mobility/transconductance improvement" factor [10]	1.0	1.3	1.3	1.4	2.0	2.0	2.0
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	1.0	1.0	1.0	1.0	1.0	0.8	0.7
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]	◆ 180	180	180	171	162	153	144
Ideal NMOS device gate capacitance (F/µm) [14]	7.40E-16	6.39E-16	6.14E-16	5.69E-16	6.64E-16	6.33E-16	5.76E-16
Parasitic fringe/overlap capacitance (F/µm) [15]	2.40E-16	2.40E-16	2.40E-16	2.30E-16	2.20E-16	2.00E-16	1.90E-16
High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	◆ 1.20	0.95	0.86	0.75	0.64	0.54	0.48
Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	◆ 1.00	1.26	1.39	1.60	1.86	2.20	2.49
Nominal logic gate delay (NAND Gate) (ps) [18]	◆ 30.24	23.94	21.72	18.92	16.23	13.72	12.13
NMOSFET power-delay product (J/µm) [19]	1.41E-15	1.27E-15	1.03E-15	9.66E-16	1.07E-15	8.33E-16	7.66E-16
NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	3.96E-07	6.60E-07	6.05E-07	6.05E-07	8.47E-07	7.70E-07	7.70E-07

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known ◆
Manufacturable solutions are NOT known

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Table 47b High-performance Logic Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Physical gate length high-performance (HP) (nm) [1]	18		14	13		10	9		7
IS	Physical gate length high-performance (HP) (nm) [1]	18	16	14	13	11	10	9	8	7
WAS	EOT equivalent oxide thickness (physical) for high-performance (nm) [2]	0.7		0.7	0.6		0.6	0.5		0.5
IS	EOT equivalent oxide thickness (physical) for high-performance (nm) [2]	0.7	0.7	0.7	0.6	0.6	0.6	0.5	0.5	0.5
WAS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4		0.4	0.4		0.4	0.4		0.4
IS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
WAS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.1		1.1	1		1	0.9		0.9
IS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.1	1.1	1.1	1	1	1	0.9	0.9	0.9
WAS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	1.90E+03		2.40E+03	7.70E+03		1.00E+04	1.90E+04		2.40E+04
IS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	1.90E+03	2.08E+03	2.40E+03	7.70E+03	9.09E+03	1.00E+04	1.90E+04	2.08E+04	2.40E+04
WAS	Nominal power supply voltage (V_{dd}) (V) [6]	1		0.9	0.9		0.8	0.8		0.7
IS	Nominal power supply voltage (V_{dd}) (V) [6]	1	1	0.9	0.9	0.9	0.8	0.8	0.7	0.7
WAS	Saturation threshold voltage (V) [7]	0.15		0.14	0.11		0.12	0.1		0.11
IS	Saturation threshold voltage (V) [7]	0.15	0.15	0.14	0.11	0.11	0.12	0.1	0.1	0.11
WAS	Nominal high-performance NMOS sub-threshold leakage current, Isd,leak (at 25°C) (µA/µm) [8]	0.1		0.1	0.3		0.3	0.5		0.5
IS	Nominal high-performance NMOS sub-threshold leakage current, Isd,leak (at 25°C) (µA/µm) [8]	0.1	0.1	0.1	0.3	0.3	0.3	0.5	0.5	0.5



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Table 47b High-performance Logic Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Nominal high-performance NMOS saturation drive current, $I_{d,sat}$ (at Vdd, at 25°C) (mA/μm) [9]	1900		1790	2050		2110	2400		2190
IS	Nominal high-performance NMOS saturation drive current, Id,sat (at Vdd, at 25°C) (μA/μm) [9]	1900	1940	1790	2050	2230	2110	2400	2120	2190
WAS	Required "mobility/transconductance improvement" factor [10]	2		2	2		2	2		2
IS	Required "mobility/transconductance improvement" factor [10]	2	2	2	2	2	2	2	2	2
WAS	Sub-threshold slope adjustment factor (Full depletion/multiple-gate effects) (0–1) [11]	0.6		0.5	0.5		0.5	0.5		0.5
IS	Sub-threshold slope adjustment factor (Full depletion/multiple-gate effects) (0–1) [11]	0.6	0.6	0.5	0.5	0.5	0.5	0.5	0.5	0.5
WAS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.1		1.1	1.1		1.3	1.3		1.3
IS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.1	1.1	1.1	1.1	1.2	1.3	1.3	1.3	1.3
WAS	Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	135		116	107		88	79		60
IS	Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	135	125	116	107	98	88	79	70	60
WAS	Ideal NMOS device gate capacitance (F/μm) [14]	5.65E-16		4.39E-16	4.49E-16		3.45E-16	3.45E-16		2.69E-16
IS	Ideal NMOS device gate capacitance (F/μm) [14]	5.65E-16	5.02E-16	4.39E-16	4.49E-16	3.76E-16	3.45E-16	3.45E-16	3.07E-16	2.69E-16
WAS	Parasitic fringe/overlap capacitance (F/μm) [15]	1.80E-16		1.50E-16	1.40E-16		1.20E-16	1.00E-16		8.00E-17
IS	Parasitic fringe/overlap capacitance (F/μm) [15]	1.80E-16	1.65E-16	1.50E-16	1.40E-16	1.30E-16	1.20E-16	1.00E-16	9.00E-17	8.00E-17
WAS	High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.39		0.3	0.26		0.18	0.15		0.11
IS	High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.39	0.34	0.3	0.26	0.21	0.18	0.15	0.13	0.11

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

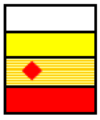
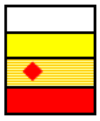


Table 47b High-performance Logic Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	3.06		4.05	4.64		6.8	8.08		10.77
IS	Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	3.1	3.5	4.1	4.6	5.7	6.8	8.1	9.2	10.8
WAS	Nominal logic gate delay (NAND gate) (ps) [18]	9.88		7.47	6.52		4.45	3.74		2.81
IS	Nominal logic gate delay (NAND gate) (ps) [18]	9.88	8.67	7.47	6.52	5.19	4.45	3.74	3.30	2.81
WAS	NMOSFET power-delay product (J/μm) [19]	7.45E-16		4.77E-16	4.77E-16		2.98E-16	2.85E-16		1.71E-16
IS	NMOSFET power-delay product (J/μm) [19]	7.45E-16	6.67E-16	4.77E-16	4.77E-16	4.10E-16	2.98E-16	2.85E-16	1.95E-16	1.71E-16
WAS	NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	1.10E-06		9.90E-07	2.97E-06		2.64E-06	4.40E-06		3.85E-06
IS	NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	1.1E-06	1.1E-06	9.9E-07	3.0E-06	3.0E-06	2.6E-06	4.4E-06	3.9E-06	3.9E-06

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 47a and 47b

A Microsoft Excel file containing the worksheet in which the details of the model-based scaling are described is located in the electronic version of this chapter at http //public.itrs.net, including the formulas used in the MOSFET modeling. All the entries in this High-performance Logic Technology Requirements Table are from the worksheet. Please refer to this Excel file for detailed questions about the table.

WAS *The scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goal for high-performance logic, 17% per year average improvement in the NMOS intrinsic switching speed (see Note [16]), while delaying as long as feasible the projected need for major innovations. These include innovations such as metal gate electrode, high-κ gate dielectric, and novel doping and annealing techniques to reduce the value of the parasitic series source/drain resistance. However, there are numerous parameters (such as EOT, V_{dd}, $I_{sd,leak}$, etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters (see text for more detail on this point).*

IS *The scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goal for high-performance logic, 17% per year average improvement in the NMOS intrinsic switching speed (see Note ~~[16]~~ [17]), while delaying as long as feasible the projected need for major innovations. These include innovations such as metal gate electrode, high-κ gate dielectric, and novel doping and annealing techniques to reduce the value of the parasitic series source/drain resistance. However, there are numerous parameters (such as EOT, V_{dd}, $I_{sd,leak}$, etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters (see text for more detail on this point).*

[1] This is the final, as-etched length of the bottom of the gate electrode. Values set by ORTC. Gate dimensional control is set by the Lithography and FEP Etch ITWGs, and is assumed to have a three-sigma value of ± 10% × L_g. It is expected that meeting this 10% requirement will become increasingly difficult with scaling (refer to the Lithography chapter and the FEP chapter). Gate length variation is assumed to be a primary factor responsible for driving device parameter variation.

[2] For a gate dielectric of thickness T_d and relative dielectric constant κ, EOT is defined by EOT = T_d / (κ/3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide. For a MOSFET with the gate dielectric of thickness T_d, the ideal gate capacitance per unit area is the same as that of a similar MOSFET, but with a gate dielectric made up of thermal silicon dioxide with a thickness of EOT. Yellow coloring in 2006 is set by FEP TWG projections of difficulties in achieving adequate thickness control and reliability capability for thin silicon oxy-nitride gate dielectrics. Red coloring for 2007 and beyond is due to projected inability of oxy-nitride gate dielectric to meet the gate leakage current density limits (see Note [5], and see text as well as Figure 25 for detail). Utilization of high-κ gate dielectric is a potential solution. Measurement of EOT is complicated, and is usually done via sophisticated MOS capacitor-voltage (CV) measurements on MOS capacitors or via optical measurements.

[3] Accounts (approximately) for gate electrode depletion and inversion-layer effects, including quantum effects. The portion of the electrical thickness adjustment due to inversion-layer effects is assumed to remain constant at 0.4 nm. For polysilicon gate electrodes, the portion of the electrical thickness adjustment due to gate electrode depletion is dependent on the polysilicon doping. The yellow coloring for 2005 and 2006 reflects the FEP TWG assessment of difficulty in adequately doping polysilicon (particularly

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for the P^+, boron-doped electrodes) to meet the gate depletion thickness adjustment requirements. The red coloring for 2007 and beyond reflects the projected inability to adequately dope polysilicon gate electrodes to meet the gate depletion thickness adjustment requirements. Introduction of metal-gate electrodes, which reduce the gate depletion effect to zero, is a potential solution.

[4] Sum of EOT and electrical thickness adjustment (see Notes [2] and [3] above). For MOSFETs in inversion, ideal gate capacitance per unit area (see Note [14]) is ε_{ox} / (equivalent electrical oxide thickness), where ε_{ox} is the dielectric constant of thermal silicon dioxide. The equivalent electrical oxide thickness in inversion is used in calculations of the CV/I intrinsic delay (see Note [16]) and of the CV^2 dynamic switching energy (see Note [19]). Red/yellow coloring follows that of EOT and Electrical Thickness Adjustment (see Notes [2] and [3] above).

[5] This is the maximum allowed gate leakage at 25°C, and is related to $I_{sd,leak}$, the nominal subthreshold leakage current per micron device width (see Note [8] below). Specifically, gate leakage current density limit = [$I_{sd,leak}$ / (physical gate length)] × [temp. factor] / [stack and overlap factor]. "Temp factor" = 10, and it accounts for the high operating temperature expected for high-performance logic, by adjusting for both the rapid increase in $I_{sd,leak}$ with temperature and the insensitivity of gate leakage current (since it is due to direct tunneling) to temperature. Stack and overlap factor=3, and accounts for the different effects on $I_{sd,leak}$ and gate leakage current of stacked transistors in logic gates and of transistor gate overlap. The values of both temp factor and stack and overlap factor are rough order of magnitude estimates. The yellow and red coloring follows that of EOT (see Note [2] above).

[6] Nominal power supply voltage has been chosen to maintain sufficient voltage over-drive [V_{dd} – saturation threshold voltage (see Note 7)] in order to meet the required saturation current drive values (see Note 9), while still maintaining reasonable vertical gate dielectric electric field strengths. Target power supply voltage values for actual ICs may vary ± 10% (or more) from the values in this table, depending on the particular circuit design application or technology optimization.

[7] Calculated threshold voltage for minimum nominal gate length transistor with drain bias set equal to V_{dd} (see Note [6]). The threshold voltage values and the corresponding subthreshold leakage current values (see Note [8]) have been chosen to maintain sufficient voltage over-drive (V_{dd} – saturation threshold voltage) in order to meet the required saturation current drive values (see Note [9]). Since control of short-channel effects for scaled MOSFETs is a key issue here, the yellow/red coloring follows that of the subthreshold slope adjustment factor (see Note [11] below).

[8] Nominal subthreshold leakage current is defined as the NMOSFET source current per micron of device width, at 25°C, with the drain bias set equal to V_{dd} (see Note [6]) and with the gate, source, and substrate biases set to zero volts. All MOSFET device dimensions are assumed to be at their nominal/target values. Total NMOS off-state current is the NMOSFET drain current per micron of device width at 25°C, and is the sum of the NMOS subthreshold, gate, and junction leakage current components. The subthreshold leakage current is assumed to be larger than the junction leakage current component at either 25°C or high-temperature conditions, but see Note [5] for the relation between $I_{sd\,leak}$ and gate leakage current density. Yellow and red coloring follows that of the subthreshold slope adjustment factor, which takes account of the impact of using advanced devices ultra-thin body, fully depleted MOSFETs and multiple-gate MOSFETs (see Note [11] below). The above subthreshold, gate, and junction leakage current scaling scenario also applies to PMOS devices. Note that subthreshold current values here apply to the fastest MOSFETs only; slower/lower-leakage MOSFETs will also be available, since current and future chips consist/will consist of a mix of both high and lower-leakage devices (see text for further discussion).

WAS

[9] Nominal saturation current drive, $I_{d,sat}$, is defined as the NMOSFET drain current per micron device width, at 25°C, with the gate bias and the drain bias set equal to V_{dd} (see Note [6]) and the source and substrate biases set to zero; all MOSFET device dimensions are assumed to be at their nominal/target values. The saturation drive current values have been chosen to continue the historical approximate 17% per year device performance scaling (see Note [17] below). Nominal PMOS saturation current-drive value is assumed to be (40–50)% of the nominal NMOS saturation current-drive value. Yellow/red coloring follows that of three items the parasitic source/drain series resistance, R_{sd} (see Note [13] below), the equivalent electrical oxide thickness in inversion (see Note [4]), and the required mobility/transconductance improvement factor (see Note [10]). Note that saturation current drive values here apply to the fastest MOSFETs only; lower saturation current drive/lower-leakage MOSFETs will also be available, since current and future chips consist/will consist of a mix of both high and lower-leakage devices (see text for further discussion).

IS

[9] Nominal saturation current drive, $I_{d,sat}$, is defined as the NMOSFET drain current per micron device width, at 25°C, with the gate bias and the drain bias set equal to V_{dd} (see Note [6]) and the source and substrate biases set to zero; all MOSFET device dimensions are assumed to be at their nominal/target values. The saturation drive current values have been chosen to continue the historical approximate 17% per year device performance scaling (see Note [17] below). Nominal PMOS saturation current-drive value is assumed to be (40–50)% of the nominal NMOS saturation current-drive value. Yellow/red and striped coloring follows that of three items the parasitic source/drain series resistance, R_{sd} (see Note [13] below), the equivalent electrical oxide thickness in inversion (see Note [4]), and the required mobility/transconductance improvement factor (see Note [10]). Note that saturation current drive values here apply to the fastest MOSFETs only; lower saturation current drive/lower-leakage MOSFETs will also be available, since current and future chips consist/will consist of a mix of both high and lower-leakage devices (see text for further discussion).

[10] Fundamental device mobility/transconductance improvement (strained Si channel is the current implementation choice) is captured by a factor multiplying the carrier mobility. Such improvement is projected to be needed by 2004 in order to meet the required saturation current drive values (see Note [9]). Yellow coloring in 2004 and beyond reflects projected implementation of strained Si channel devices. Red coloring in 2007 and beyond reflects the difficulty in optimizing this mobility enhancement to a factor of 2.0, and the difficulty of implementing enhanced mobility channels for advanced, ultra-thin body devices.

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[11] Subthreshold slope adjustment factor takes account of the impact of using advanced, single-gate, ultra-thin body, fully depleted SOI MOSFETs and eventually, ultra-thin body, multiple-gate MOSFETs, which are needed to control short-channel effects for highly scaled transistors. Specifically, this is a multiplying factor for the subthreshold slope, reducing it towards its minimum ideal value of 60 mV/decade. The factor ranges from 1.0 for classical, planar bulk MOSFETs, to 0.7 to 0.8 for single-gate, ultra-thin body MOSFETs, to 0.6 to 0.5 for ultra-thin body, multiple-gate MOSFETs. These numbers are rough estimates of the impact of these advanced devices. (See Non-Classical CMOS tables in the Emerging Research Devices section for further discussion of the ultra-thin body MOSFETs.) The yellow coloring reflects the projected introduction of the single-gate, ultra-thin body MOSFET in 2008, and the red coloring reflects the projected introduction of the multiple-gate MOSFET in 2010.

[12] This is a multiplying factor for carrier saturation velocity, reflecting quasi-ballistic transport in highly scaled, ultra-thin body MOSFETs, particularly multi-gate MOSFETs. The red coloring in 2010 and beyond reflects the projected need for saturation velocity enhancement in order to meet the required saturation current drive values (see Note [9]).

WAS

[13] Rsd is the maximum allowable parasitic series source plus drain resistance for a MOSFET of one micron width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow/red coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.

IS

*[13] Rsd is the maximum allowable parasitic series source plus drain resistance for a MOSFET of one micron width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow/red **and striped** coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling.*

[14] This is $C_{g,ideal}$, the ideal gate capacitance per micron device width, in inversion. $C_{g,ideal} = [\varepsilon_{ox} / (EOT_{inv})] \times L_g$, where ε_{ox} is the dielectric constant of thermal silicon dioxide, EOT_{inv} is the equivalent electrical oxide thickness in inversion (see Note [4]), and L_g is the physical gate length (see Note [1]). The red/yellow coloring follows that of EOT_{inv} (see Note [4]).

[15] This is the parasitic gate overlap/fringing capacitance per micron device width [3× the overlap/fringing capacitance value per side, including the Miller effect]. These values are assumed to be independent of bias conditions.

WAS

[16] τ is the intrinsic transistor delay for NMOS devices at 25°C. $\tau = (C_{gate} \times V_{dd}) / I_{d,sat}$, where C_{gate} is the sum of the ideal device gate capacitance per micron device width (Note 14) and the parasitic gate overlap/fringing capacitance per micron device width (see Note [15]). τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat} \sim (0.4–0.5) \times$ (NMOS $I_{d,sat}$) (see Note [9]). τ is a good metric for the intrinsic switching delay of the device, while $1/\tau$ is a good metric for the intrinsic switching speed of the device. Red/yellow coloring follows that of both saturation current-drive (see Note [9]) and ideal gate capacitance (see Note [14]).

IS

*[16] τ is the intrinsic transistor delay for NMOS devices at 25°C. $\tau = (C_{gate} \times V_{dd}) / I_{d,sat}$, where C_{gate} is the sum of the ideal device gate capacitance per micron device width (Note 14) and the parasitic gate overlap/fringing capacitance per micron device width (see Note [15]). τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat} \sim (0.4–0.5) \times$ (NMOS $I_{d,sat}$) (see Note [9]). τ is a good metric for the intrinsic switching delay of the device, while $1/\tau$ is a good metric for the intrinsic switching speed of the device. Red/yellow **and striped** coloring follows that of both saturation current-drive (see Note [9]) and ideal gate capacitance (see Note [14]).*

WAS

[17] NMOS performance metric ($1/\tau$, NMOS intrinsic switching speed--see Note [16]), normalized to the year 2003. Maintenance of the historical approximate 17% per year device performance improvement scaling trend is the key scaling goal for high-performance logic. Red/yellow coloring follows that of τ (see Note [16]).

IS

*[17] NMOS performance metric ($1/\tau$, NMOS intrinsic switching speed--see Note [16]), normalized to the year 2003. Maintenance of the historical approximate 17% per year device performance improvement scaling trend is the key scaling goal for high-performance logic. Red/yellow **and striped** coloring follows that of τ (see Note [16]).*

WAS

[18] This is the calculated nominal delay for a 2-input, fan-out of 3, NAND gate, which is chosen to represent a typical logic gate (for details of the calculation, see link provided in the electronic version, online at http //public.itrs.net.). Red/yellow coloring follows that of τ (see Note [16]).

IS

*[18] This is the calculated nominal delay for a 2-input, fan-out of 3, NAND gate, which is chosen to represent a typical logic gate (for details of the calculation, see link provided in the electronic version, online at http //public.itrs.net.). Red/yellow **and striped** coloring follows that of τ (see Note [16]).*

[19] This is the energy dissipated per micron of MOSFET width during a full switching cycle, defined as $C_{gate} \times V_{dd}^2$, where C_{gate} is the sum of the ideal device gate capacitance per micron width (Note [14]) and the parasitic gate overlap/fringing capacitance per micron width (see Note [15]). (This is the same C_{gate} used in calculating τ [see Note [16]). The dynamic power dissipation is directly related to this power-delay product. Red/yellow coloring follows that of $C_{g,ideal}$ (see Note [14]).

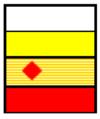
[20] This is the static power dissipation per micron of MOSFET width, defined as $V_{dd} \times [\{I_{sd,leak}$ (see Note 8)$\} + \{$ maximum gate leakage current per micron device width (defined as $L_g \times$ gate leakage current density limit, from Note 5)$\}]$. (The junction leakage current is assumed to be much smaller than either the source/drain subthreshold leakage current or the gate leakage current). Yellow/red coloring follows that of nominal gate leakage current density limit (see Note [5]).

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Table 48a Low Operating Power (LOP) Logic Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
Physical gate length low operating power (LOP) (nm) [1]	65	53	45	37	32	28	25
EOT equivalent oxide thickness (physical) for LOP (nm) [2]	1.6	1.5	1.4	1.3	1.2	1.1	1.0
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.7	0.4	0.4
Equivalent electrical oxide thickness in inversion (nm) [4]	2.4	2.3	2.1	2.0	1.9	1.5	1.4
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	0.51	1.89	2.22	2.70	5.21	5.95	6.67
Nominal LOP power supply voltage (V_{dd}) (V) [6]	1.0	0.9	0.9	0.9	0.8	0.8	0.8
Saturation threshold voltage (V) [7]	0.31	0.26	0.27	0.28	0.26	0.25	0.25
Nominal LOP NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (μA/μm) [8]	1.0E-03	3.0E-03	3.0E-03	3.0E-03	5.0E-03	5.0E-03	5.0E-03
Nominal LOP NMOS saturation drive current, $I_{d,sat}$ (at V_{dd} at 25°C) (μA/μm) [9]	520	530	580	610	570	730	770
Required "mobility/transconductance improvement" factor [10]	1.0	1.0	1.0	1.0	1.0	1.3	1.3
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	180	180	180	180	180	180	180
Ideal NMOS device gate capacitance (F/μm) [14]	9.35E-16	7.96E-16	7.40E-16	6.39E-16	5.82E-16	6.45E-16	6.17E-16
Parasitic fringe/overlap capacitance (F/μm) [15]	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16	2.40E-16
LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	2.26	1.76	1.52	1.30	1.15	0.97	0.89
Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	1.00	1.29	1.49	1.74	1.96	2.33	2.54
Nominal logic gate delay (NAND gate) (ps) [18]	57.0	44.3	38.3	32.7	29.1	24.4	22.4
NMOSFET power-delay product (J/μm) [19]	1.18E-15	8.39E-16	7.94E-16	7.12E-16	5.26E-16	5.66E-16	5.48E-16
NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	2.0E-09	5.4E-09	5.4E-09	5.4E-09	8.0E-09	8.0E-09	8.0E-09

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



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Table 48b Low Operating Power (LOP) Logic Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Physical gate length low operating power (LOP) (nm) [1]	22		18	16		13	11		9
IS	Physical gate length low operating power (LOP) (nm) [1]	22	20	18	16	14	13	11	10	9
WAS	EOT equivalent oxide thickness (physical) for LOP (nm) [2]	0.9	-	0.9	0.8	-	0.8	0.7	-	0.7
IS	EOT equivalent oxide thickness (physical) for LOP (nm) [2]	0.9	0.9	0.9	0.8	0.8	0.8	0.7	0.7	0.7
WAS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	-	0.4	0.4	-	0.4	0.4	-	0.4
IS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
WAS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.3	-	1.3	1.2	-	1.2	1.1	-	1.1
IS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.3	1.3	1.3	1.2	1.2	1.2	1.1	1.1	1.1
WAS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	11	-	13	21	-	26	91	-	111
IS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	11	12	13	21	24	26	91	100	111
WAS	Nominal LOP power supply voltage (V_{dd}) (V) [6]	0.7	-	0.7	0.6	-	0.6	0.5	-	0.5
IS	Nominal LOP power supply voltage (V_{dd}) (V) [6]	0.7	0.7	0.7	0.6	0.6	0.6	0.5	0.5	0.5
WAS	Saturation threshold voltage (V) [7]	0.22	-	0.23	0.21	-	0.19	0.16	-	0.17
IS	Saturation threshold voltage (V) [7]	0.22	0.22	0.23	0.21	0.2	0.19	0.16	0.16	0.17
WAS	Nominal LOP NMOS sub-threshold leakage current, Isd,leak (at 25°C) (µA/µm) [8]	0.007	-	0.007	0.01	-	0.01	0.03	-	0.03
IS	Nominal LOP NMOS sub-threshold leakage current, Isd,leak (at 25°C) (µA/µm) [8]	0.007	0.007	0.007	0.01	0.01	0.01	0.03	0.03	0.03
WAS	Nominal LOP NMOS saturation drive current, Id,sat (at V_{dd} at 25°C) (µA/µm) [9]	770	-	830	780	-	900	920	-	950
IS	Nominal LOP NMOS saturation drive current, Id,sat (at V_{dd} at 25°C) (µA/µm) [9]	770	800	830	780	840	900	920	935	950

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

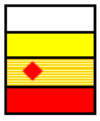


Table 48b Low Operating Power (LOP) Logic Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Required "mobility/transconductance improvement" factor [10]	1.3	-	2	2	-	2	2	-	2
IS	Required "mobility/transconductance improvement" factor [10]	1.3	1.3	2	2	2	2	2	2	2
WAS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8	-	0.8	0.8	-	0.5	0.5	-	0.5
IS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8	0.8	0.8	0.8	0.8	0.5	0.5	0.5	0.5
WAS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1	-	1	1.1	-	1.1	1.3	-	1.3
IS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1	1	1	1.1	1.1	1.1	1.3	1.3	1.3
WAS	Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]	160	-	135	126	-	107	98	-	80
IS	Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]	160	148	135	126	117	107	98	89	80
WAS	Ideal NMOS device gate capacitance (F/µm) [14]	5.84E-16	-	4.78E-16	4.60E-16	-	3.74E-16	3.45E-16	-	2.83E-16
IS	Ideal NMOS device gate capacitance (F/µm) [14]	5.84E-16	5.31E-16	4.78E-16	4.60E-16	4.03E-16	3.74E-16	3.45E-16	3.14E-16	2.83E-16
WAS	Parasitic fringe/overlap capacitance (F/µm) [15]	2.20E-16	-	1.80E-16	1.60E-16	-	1.40E-16	1.30E-16	-	1.10E-16
IS	Parasitic fringe/overlap capacitance (F/µm) [15]	2.20E-16	2.00E-16	1.80E-16	1.60E-16	1.50E-16	1.40E-16	1.30E-16	1.20E-16	1.10E-16
WAS	LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.73	-	0.56	0.48	-	0.34	0.26	-	0.21
IS	LOP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.73	0.64	0.56	0.48	0.39	0.34	0.26	0.23	0.21
WAS	Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	3.1	-	4.1	4.7	-	6.6	8.7	-	10.9
IS	Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	3.1	3.54	4.1	4.7	5.72	6.6	8.7	9.75	10.9
WAS	Nominal logic gate delay (NAND Gate) (ps) [18]	18.4	-	14	12	-	8.6	6.5	-	5.2
IS	Nominal logic gate delay (NAND Gate) (ps) [18]	18.4	16.1	14	12	9.9	8.6	6.5	5.8	5.2
WAS	NMOSFET power-delay product (J/µm) [19]	3.94E-16	-	3.22E-16	2.23E-16	-	1.85E-16	1.19E-16	-	9.81E-17
IS	NMOSFET power-delay product (J/µm) [19]	3.94E-16	3.58E-16	3.22E-16	2.23E-16	1.99E-16	1.85E-16	1.19E-16	1.08E-16	9.81E-17
WAS	NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	9.80E-09	-	9.80E-09	1.20E-08	-	1.20E-08	3.00E-08	-	3.00E-08
IS	NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	9.80E-09	9.80E-09	9.80E-09	1.20E-08	1.20E-08	1.20E-08	3.00E-08	3.00E-08	3.00E-08

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

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Table 48c Low Standby Power (LSTP) Technology Requirements—Near-term

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Technology Node		*hp90*			*hp65*		
DRAM ½ Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*120*	*107*	*95*	*85*	*76*	*67*	*60*
MPU/ASIC ½ Pitch (nm)	*107*	*90*	*80*	*70*	*65*	*57*	*50*
MPU Printed Gate Length (nm)	*65*	*53*	*45*	*40*	*35*	*32*	*28*
MPU Physical Gate Length (nm)	*45*	*37*	*32*	*28*	*25*	*22*	*20*
Physical gate length low standby power (LSTP) (nm) [1]	**75**	**65**	**53**	**45**	**37**	**32**	**28**
EOT equivalent oxide thickness (physical) for LSTP (nm) [2]	**2.2**	**2.1**	**2.1**	**1.9**	**1.6**	**1.5**	**1.4**
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.4**	**0.4**
Equivalent electrical oxide thickness in inversion (nm) [4]	**3**	**2.9**	**2.8**	**2.6**	**2.3**	**1.9**	**1.8**
Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	**4.4E-03**	**5.1E-03**	**9.4E-03**	**1.5E-02**	**2.3E-02**	**3.1E-02**	**4.8E-02**
Nominal LSTP power supply voltage (V_{dd}) (V) [6]	**1.2**	**1.2**	**1.2**	**1.2**	**1.1**	**1.1**	**1.1**
Saturation threshold voltage (V) [7]	**0.50**	**0.50**	**0.51**	**0.52**	**0.50**	**0.47**	**0.47**
Nominal LSTP NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) (μA/μm) [8]	**1.0E-05**	**1.0E-05**	**1.5E-05**	**2.0E-05**	**2.5E-05**	**3.0E-05**	**4.0E-05**
Nominal LSTP NMOS saturation drive current, $I_{d,sat}$ (at V_{dd}, at 25°C) (μA/μm) [9]	**410**	**440**	**470**	**510**	**510**	**670**	**700**
Required "mobility/transconductance improvement" factor [10]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.3**	**1.3**
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**	**1.0**
Parasitic source/drain series resistance (R_{sd}) (Ohm-μm) [13]	**180**	**180**	**180**	**180**	**180**	**180**	**180**
Ideal NMOS device gate capacitance (F/μm) [14]	**8.63E-16**	**7.74E-16**	**6.54E-16**	**5.98E-16**	**5.55E-16**	**5.82E-16**	**5.37E-16**
Parasitic fringe/overlap capacitance (F/μm) [15]	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**	**2.40E-16**
LSTP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	**3.23**	**2.77**	**2.28**	**1.97**	**1.72**	**1.35**	**1.22**
Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	**1.00**	**1.17**	**1.42**	**1.64**	**1.88**	**2.39**	**2.64**
Nominal logic gate delay (NAND Gate) (ps) [18]	**81.4**	**69.7**	**57.5**	**49.7**	**43.2**	**34.0**	**30.8**
NMOSFET power-delay product (J/μm) [19]	**1.6E-15**	**1.5E-15**	**1.3E-15**	**1.2E-15**	**9.6E-16**	**9.9E-16**	**9.4E-16**
NMOSFET static power dissipation due to drain and gate leakage (W/μm) [20]	**2.4E-11**	**2.4E-11**	**3.6E-11**	**4.8E-11**	**5.5E-11**	**6.6E-11**	**8.8E-11**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

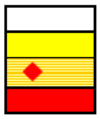


Table 48d Low Standby Power (LSTP) Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Physical gate length low standby power (LSTP) (nm) [1]	25		20	18		14	13		10
IS	Physical gate length low standby power (LSTP) (nm) [1]	25	23	20	18	16	14	13	12	10
WAS	EOT equivalent oxide thickness (physical) for LSTP (nm) [2]	1.3		1.2	1.1		1.1	1		0.9
IS	EOT equivalent oxide thickness (physical) for LSTP (nm) [2]	1.3	1.3	1.2	1.1	1.1	1.1	1	1	0.9
WAS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4		0.4	0.4		0.4	0.4		0.4
IS	Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
WAS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.7		1.6	1.5		1.5	1.4		1.3
IS	Equivalent electrical oxide thickness in inversion (nm) [4]	1.7	1.7	1.6	1.5	1.5	1.5	1.4	1.4	1.3
WAS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	8.00E-02		1.00E-01	1.48E-01		1.90E-01	2.56E-01		3.33E-01
IS	Nominal gate leakage current density limit (at 25°C) (A/cm^2) [5]	0.08	0.09	0.10	0.15	0.17	0.19	0.26	0.28	0.33
WAS	Nominal LSTP power supply voltage (V_{dd}) (V) [6]	1		1	0.9		0.9	0.8		0.8
IS	Nominal LSTP power supply voltage (V_{dd}) (V) [6]	1	1	1	0.9	0.9	0.9	0.8	0.8	0.8
WAS	Saturation threshold voltage (V) [7]	0.39		0.43	0.34		0.38	0.36		0.4
IS	Saturation threshold voltage (V) [7]	0.39	0.42	0.43	0.34	0.36	0.38	0.36	0.39	0.4
WAS	Nominal LSTP NMOS sub-threshold leakage current, Isd,leak (at 25°C) (µA/µm) [8]	6.00E-05		6.00E-05	8.00E-05		8.00E-05	1.00E-04		1.00E-04
IS	Nominal LSTP NMOS sub-threshold leakage current, Isd,leak (at 25°C) (µA/µm) [8]	6.00E-05	6.00E-05	6.00E-05	8.00E-05	8.00E-05	8.00E-05	1.00E-04	1.00E-04	1.00E-04
WAS	Nominal LSTP NMOS saturation drive current, Id,sat (at V_{dd}, at 25°C) (µA/µm) [9]	760		790	880		870	860		990
IS	Nominal LSTP NMOS saturation drive current, Id,sat (at V_{dd}, at 25°C) (µA/µm) [9]	760	750	790	880	870	870	860	880	990

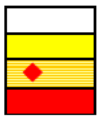
Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

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Table 48d Low Standby Power (LSTP) Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Required "mobility/transconductance improvement" factor [10]	1.3		1.3	1.3		1.3	2		2
IS	Required "mobility/transconductance improvement" factor [10]	1.3	1.3	1.3	1.3	1.3	1.3	2	2	2
WAS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8		0.8	0.5		0.5	0.5		0.5
IS	Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	0.8	0.8	0.8	0.5	0.5	0.5	0.5	0.5	0.5
WAS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1		1	1		1	1.1		1.3
IS	Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1	1	1	1	1	1	1.1	1.2	1.3
WAS	Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]	180		144	135		116	107		88
IS	Parasitic source/drain series resistance (R_{sd}) (Ohm-µm) [13]	180	160	144	135	125	116	107	97	88
WAS	Ideal NMOS device gate capacitance (F/µm) [14]	5.08E-16		4.32E-16	4.14E-16		3.22E-16	3.21E-16		2.66E-16
IS	Ideal NMOS device gate capacitance (F/µm) [14]	5.08E-16	4.67E-16	4.32E-16	4.14E-16	3.68E-16	3.22E-16	3.21E-16	2.96E-16	2.66E-16
WAS	Parasitic fringe/overlap capacitance (F/µm) [15]	2.40E-16		1.90E-16	1.70E-16		1.50E-16	1.40E-16		1.20E-16
IS	Parasitic fringe/overlap capacitance (F/µm) [15]	2.40E-16	2.15E-16	1.90E-16	1.70E-16	1.60E-16	1.50E-16	1.40E-16	1.30E-16	1.20E-16
WAS	LSTP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.98		0.79	0.6		0.49	0.43		0.31
IS	LSTP NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{d,sat}$ (ps) [16]	0.98	0.90	0.79	0.6	0.55	0.49	0.43	0.39	0.31
WAS	Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	3.28		4.1	5.4		6.61	7.54		10.36
IS	Relative NMOS intrinsic switching speed, 1/τ, normalized to 2003 [17]	3.28	3.58	4.1	5.4	5.91	6.61	7.54	8.34	10.36
WAS	Nominal logic gate delay (NAND gate) (ps) [18]	24.8		19.83	15.06		12.31	10.8		7.85
IS	Nominal logic gate delay (NAND gate) (ps) [18]	24.8	22.78	19.83	15.06	13.71	12.31	10.8	9.73	7.85
WAS	NMOSFET power-delay product (J/µm) [19]	7.48E-16		6.22E-16	4.73E-16		3.83E-16	2.95E-16		2.47E-16
IS	NMOSFET power-delay product (J/µm) [19]	7.48E-16	6.82E-16	6.22E-16	4.73E-16	4.28E-16	3.83E-16	2.95E-16	2.73E-16	2.47E-16
WAS	NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	1.20E-10		1.20E-10	1.44E-10		1.44E-10	1.60E-10		1.60E-10
IS	NMOSFET static power dissipation due to drain and gate leakage (W/µm) [20]	1.20E-10	1.20E-10	1.20E-10	1.44E-10	1.44E-10	1.44E-10	1.60E-10	1.60E-10	1.60E-10

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



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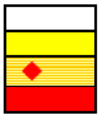
Table 49a DRAM Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm) [1]	100	90	80	70	65	57	50
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
DRAM cell size (μm^2) [2]	0.082	0.065	0.048	0.036	0.028	0.019	0.015
DRAM storage cell dielectric equivalent physical oxide thickness, EOT (nm) [3]	3.5	2.3	1.8	1.3	0.8	0.8	0.8
Minimum DRAM retention time (ms) [4]	64	64	64	64	64	64	64
DRAM soft error rate (FITs) [5]	1000	1000	1000	1000	1000	1000	1000

Table 49b DRAM Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm) [1]	45		35	32		25	22		18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	DRAM cell size (μm^2) [2]	0.0122		0.0077	0.0061		0.0038	0.0025		0.0016
IS	DRAM cell size (μm^2) [2]	0.0122	0.0096	0.0077	0.0061	0.0048	0.0038	0.0025	0.0020	0.0016
WAS	DRAM storage cell dielectric equivalent physical oxide thickness, EOT (nm) [3]	0.70		0.58	0.53		0.42	0.37		0.25
IS	DRAM storage cell dielectric equivalent physical oxide thickness, EOT (nm) [3]	0.70	0.64	0.58	0.53	0.48	0.42	0.37	0.31	0.25
WAS	Minimum DRAM retention time (ms) [4]	64		64	64		64	64		64
IS	Minimum DRAM retention time (ms) [4]	64	64	64	64	64	64	64	64	64
WAS	DRAM soft error rate (FITs) [5]	1000		1000	1000		1000	1000		1000
IS	DRAM soft error rate (FITs) [5]	1000	1000	1000	1000	1000	1000	1000	1000	1000

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 49a and 49b

[1] From ORTC (Overall Roadmap Technology Characteristics) Table 1a and b. These DRAM half pitch numbers are the same as those in the 2002 ITRS due to no further speed up in the pace of DRAM half pitch scaling during 2002 and the early part of 2003.

[2] The DRAM cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and chip size numbers used by FEP are based on the ORTC Tables 1a and 1b. Since the FEP DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled aggressively. The difficulty will lie in reducing the value of the cell size factor "a", where "a" equals (cell size /F^2). and F is the DRAM half pitch. The required values of "a" are 8 for the 90 nm node, real 6 for the 55 nm DRAM half pitch in 2008, and 5 (need $4F^2$ layout) for the 32 nm node. The reason for the introduction delay of "a" value of 6 is due to no clear solutions, as illustrated with yellow zone in this line. The "a" value of 5 has no known solution for 32 nm node and beyond, as illustrated with red zone.

[3] The EOT is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and the chip size numbers used by FEP are from ORTC Tables 1a and 1b. Since the values of DRAM capacity and chip size from FEP are quite aggressive, the EOT must also be scaled very aggressively. Up to the 90 nm nodes, the dielectric material is based on Al_2O_3 or Ta_2O_5 with MIS structure, and hence the color is white. Beyond the 90 nm node, breakthroughs such as MIM structure and higher κ material are needed, so the color is yellow. Finally, for the 65 nm node and beyond, there are no known solutions with demonstrated credibility, and hence the color is red. The actual EOT required for each node also depends on the other factors such as cell height and/or 3D structure, film leakage current and contact formation. Trench capacitors have other requirements for the cell dielectric material.

[4] Retention time is defined at 85ºC, and is the minimum time during which the data from memory can still be sensed correctly without refreshing a row bit line. The 64 ms specified here is the value needed for PC applications. The retention time depends on the combined interaction of device leakage current, signal strength and signal sensing circuit sensitivity, and also depends on operational frequency and temperature.

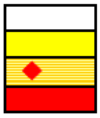
[5] This is a typical FIT rate and depends on cycle time and the quality of cell capacitor and sensing circuits.

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Table 50a Non-Volatile Memory Technology Requirements—Near-term UPDATED

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	120	107	95	85	76	67	60
	MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50
	MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
	MPU Physical Gate Length (nm)	45	37	32	28	25	22	20
WAS	Flash technology node – F (nm) [1]	107	90	80	70	65	55	50
IS	Flash technology node – F (nm) [1]	107	90	80	70	65	57	50
	Flash NOR cell size – area factor a in multiples of F^2 [2]	10–12	11–14	11–14	11–14	11–14	12–14	12–15
	Flash NAND cell size – area factor a in multiples of F^2 SLC/MLC [3]	5.5	5.5	5.5	5.5	4.5	4.5	4.5
WAS	Flash NOR typical cell size (μm^2) [4]	0.135	0.101	0.08	0.061	0.053	0.039	0.034
IS	Flash NOR typical cell size (μm^2) [4]	0.135	0.101	0.08	0.061	0.053	0.042	0.034
	Flash NOR L_g-stack (physical – µm) [5]	0.22–0.24	0.2–0.22	0.2–0.22	0.19–0.21	0.19–0.21	0.18–0.20	0.18–0.20
	Flash NOR highest W/E voltage (V) [6]	8–10	7–9	7–9	7–9	7–9	7–9	7–9
	Flash NAND highest W/E voltage (V) [7]	18–20	17–19	17–19	17–19	15–17	15–17	15–17
	Flash NOR I_{read} (µA) [8]	34–42	31–39	29–37	28–36	27–35	26–34	25–33
	Flash coupling ratio [9]	0.65–0.75	0.65–0.75	0.65–0.75	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
WAS	Flash NOR tunnel oxide thickness (nm) [10]	9–10	8.5–9.5	8.5–9.5	8.5–9.5	8–9	8–9	8–9
IS	Flash NOR tunnel oxide thickness EOT (nm) [10]	9–10	8.5–9.5	8.5–9.5	8-9	8–9	8–9	8–9
WAS	Flash NAND tunnel oxide thickness (nm) [11]	7–8	7–8	7–8	7–8	6–7	6–7	6–7
IS	Flash NAND tunnel oxide thickness EOT (nm) [11]	7–8	7–8	7–8	6–7	6–7	6–7	6–7
WAS	Flash NOR interpoly dielectric thickness (nm) [12]	11–13	10–12	9–11	9–11	8.5–10.5	8.5–10.5	8.5–10.5
IS	Flash NOR interpoly dielectric thickness EOT (nm) [12]	13-15	11-13	11-13	11-13	10-12	10-12	10-12
	Flash NAND interpoly dielectric thickness (nm) [13]	13–15	13–15	13–15	13–15	10–13	10–13	10–13
	Flash endurance (erase/write cycles) [14]	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05	1.00E+05
	Flash nonvolatile data retention (years) [15]	10–20	10–20	10–20	10–20	10–20	10–20	10–20
	Flash maximum number of bits per cell (MLC) [16]	2	2	4	4	4	4	4

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



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Table 50a Non-Volatile Memory Technology Requirements—Near-term UPDATED (continued)

	Year of Production	2003	2004	2005	2006	2007	2008	2009
	Technology Node		hp90			hp65		
	DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
WAS	FeRAM technology node – F (nm) [17]	250	180	180	150	130	120	110
IS	FeRAM technology node – F (nm) [17]	250	180	130	130	120	110	110
WAS	FeRAM cell size – area factor a in multiples of F^2 [18]	24	16	12	12	12	10	10
IS	FeRAM cell size – area factor a in multiples of F^2 [18]	15	15	12	12	12	10	10
WAS	FeRAM cell size (μm^2) [19]	1.5	0.518	0.389	0.27	0.203	0.144	0.121
IS	FeRAM cell size (μm^2) [19]	0.937	0.486	0.203	0.203	0.173	0.121	0.121
WAS	FeRAM cell structure [20]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
IS	FeRAM cell structure [20]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
WAS	FeRAM capacitor structure [21]	stack	stack	stack	stack	3D	3D	3D
IS	FeRAM capacitor structure [21]	stack	stack	stack	stack	3D	3D	3D
WAS	FeRAM capacitor footprint (μm^2) [22]	0.5	0.26	0.13	0.09	0.07	0.06	0.05
IS	FeRAM capacitor footprint (μm^2) [22]	0.44	0.23	0.12	0.12	0.086	0.081	0.076
WAS	FeRAM capacitor active area (μm^2) [23]	0.5	0.26	0.13	0.09	0.09	0.09	0.08
IS	FeRAM capacitor active area (μm^2) [23]	0.44	0.23	0.12	0.12	0.058	0.048	0.04
WAS	FeRAM cap active area/footprint ratio [24]	1	1	1	1	1.29	1.5	1.6
IS	FeRAM cap active area/footprint ratio [24]	1	1	1	1	1.48	1.67	1.89
WAS	Ferro capacitor voltage (V) [25]	2.5	1.8	1.5	1.5	1.2	1.2	1.2
IS	Ferro capacitor voltage (V) [25]	2.5-3	1.8	1.5	1.5	1.2	1.2	1.2
WAS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	11.2	17.2	34.5	34.5	40	40	40
IS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	12.8	19.8	30.5	30.5	40	40	40
	FeRAM endurance (read/write cycles) [27]	1.00E+13	1.00E+14	1.00E+15	>1E16	>1E16	>1E16	>1E16
	FeRAM nonvolatile data retention (years) [28]	10	10	10	10	10	10	10

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

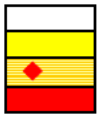


Table 50a Non-Volatile Memory Technology Requirements—Near-term UPDATED (continued)

Year of Production	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
SONOS/NROM technology node – F (nm) [29]	130	115	100	90	70	65	55
SONOS/NROM cell size – area factor a in multiples of F^2 [30]	5	5	5.5	5.5	6	6	6
SONOS/NROM typical cell size (mm^2) [31]	0.085	0.066	0.055	0.045	0.029	0.025	0.018
SONOS/NROM maximum number of bits per cell (MLC) [32]	2	2	2	2	2	2	2
SONOS/NROM area per bit (mm^2) [33]	0.042	0.033	0.028	0.022	0.015	0.013	0.009
SONOS L_g-stack (physical – μm) [34]	0.18	0.18	0.17	0.17	0.16	0.16	0.16
SONOS highest W/E voltage (V) [35]	6.0–7.0	6.0–7.0	5.0–6.0	5.0–6.0	5.0–5.5	5.0–5.5	5.0–5.5
SONOS/NROM I_{read} (μA) [36]	35–45	33–43	31–41	29–39	27–37	25–35	25–35
SONOS/NROM tunnel oxide thickness (nm) [37]	5	5	4.5	4	3.5	3.5	3.5
SONOS/NROM nitride dielectric thickness (nm) [38]	6	5	5	4.5	4	4	4
SONOS/NROM blocking (top) oxide thickness (nm) [39]	5	5	4.5	4.5	4	4	4
SONOS/NROM endurance (erase/write cycles) [40]	1.00E+06	1.00E+06	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07
SONOS/NROM nonvolatile data retention (years) [41]	10–20	10–20	10–20	10–20	10–20	10–20	10–20
MRAM technology node F (nm) [42]	180	130	90	90	65	55	50
MRAM cell size area factor a in multiples of F^2 [43]	24.7	23.7	24.7	22.2	22.2	22.2	22.2
MRAM typical cell size ($μm^2$) [44]	0.8	0.4	0.2	0.18	0.09	0.07	0.06
MRAM switching field (Oe) [45]	50	60	80	70	90	100	110
MRAM write energy (pJ) [46]	150	100	70	70	50	45	40
MRAM active area per cell ($μm^2$) [47]	0.28	0.2	0.11	0.1	0.05	0.04	0.03
MRAM resistance-area product (Kohm-$μm^2$) [48]	3	2.5	2	1.7	1.5	1.3	1.2
MRAM magnetoresistance ratio(%) [49]	45	45	50	50	60	60	60
MRAM nonvolatile data retention (years) [50]	>10	>10	>10	>10	>10	>10	>10
MRAM write endurance (read/write cycles) [51]	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15
MRAM endurance – tunnel junction reliability (years at bias) [52]	>10	>10	>10	>10	>10	>10	>10

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

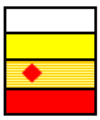


Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	48	42	38	34	30	27	24	21
	MPU/ASIC ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
	MPU Printed Gate Length (nm)	25	22	20	18	16	14	13	11	10
	MPU Physical Gate Length (nm)	18	16	14	13	11	10	9	8	7
WAS	Flash technology node – F (nm) [1]	50		39	35		28	25		20
IS	Flash technology node – F (nm) [1]	45	40	35	32	28	25	22	20	18
WAS	Flash NOR cell size – area factor a in multiples of F^2 [2]	12–15		12–15	13–16		14–17	14–17		15–18
IS	Flash NOR cell size – area factor a in multiples of F^2 [2]	12–15	12–15	12–15	13–16	13-16	14–17	14–17	15-18	15–18
WAS	Flash NAND cell size – area factor a in multiples of F^2 SLC/MLC [3]	4.5/2.3		4.5/2.3	4.5/2.3		4.5/2.3	4.5/2.3		4.5/2.3
IS	Flash NAND cell size – area factor a in multiples of F^2 SLC/MLC [3]	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3	4.5/2.3
WAS	Flash NOR typical cell size (μm^2) [4]	0.034		0.021	0.018		0.012	0.01		0.007
IS	Flash NOR typical cell size (μm^2) [4]	0.027	0.022	0.017	0.017	0.011	0.01	0.008	0.007	0.005
WAS	Flash NOR L_g-stack (physical – μm) [5]	0.17–0.19		0.15–0.17	0.14–0.16		0.13–0.15	0.12–0.14		0.11–0.13
IS	Flash NOR L_g-stack (physical – μm) [5]	0.17–0.19	0.16-0.18	0.15–0.17	0.14–0.16	0.14-0.16	0.13–0.15	0.12–0.14	0.12-0.14	0.11–0.13
WAS	Flash NOR highest W/E voltage (V) [6]	7–9		7–9	7–9		7–9	7–9		7–9
IS	Flash NOR highest W/E voltage (V) [6]	7–9	7-9	7–9	7–9	7-9	7–9	7–9	7-9	7–9
WAS	Flash NAND highest W/E voltage (V) [7]	15–17		15–17	15–17		15–17	15–17		15–17
IS	Flash NAND highest W/E voltage (V) [7]	15–17	15-17	15–17	15–17	15-17	15–17	15–17	15-17	15–17
WAS	Flash NOR I_{read} (μA) [8]	27–33		26–32	25–31		23–29	22–28		20–26
IS	Flash NOR I_{read} (μA) [8]	27–33	27–33	26–32	25–31	24-30	23–29	22–28	21-27	20–26
WAS	Flash Coupling Ratio [9]	0.6–0.7		0.6–0.7	0.6–0.7		0.6–0.7	0.6–0.7		0.6–0.7
IS	Flash Coupling Ratio [9]	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
WAS	Flash NOR tunnel oxide thickness (nm) [10]	8–9		8–9	8		8	8		8
IS	Flash NOR tunnel oxide thickness (nm) [10]	8–9	8–9	8–9	8–9	8	8	8	8	8
WAS	Flash NAND tunnel oxide thickness (nm) [11]	6–7		6–7	6–7		6–7	6–7		6–7
IS	Flash NAND tunnel oxide thickness (nm) [11]	6–7	6–7	6–7	6–7	6–7	6–7	6–7	6–7	6–7
WAS	Flash NOR interpoly dielectric thickness (nm) [12]	8–10		7–9	6–8		5–7	4–6		3–5
IS	Flash NOR interpoly dielectric thickness (nm) [12]	8–10	8–10	8–10	8–10	7-9	6-8	6-8	6-8	6-8
WAS	Flash NAND interpoly dielectric thickness (nm) [13]	10–13		10–13	9–10		9–10	9–10		9–10
IS	Flash NAND interpoly dielectric thickness (nm) [13]	10–13	10–13	10–13	9–10	9–10	9–10	9–10	9–10	9–10

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

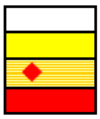


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Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	Flash endurance (erase/write cycles) [14]	1.00E+06		1.00E+06	1.00E+06		1.00E+06	1.00E+07		1.00E+07
IS	Flash endurance (erase/write cycles) [14]	1.E+06	1.E+06	1.E+06	1.E+06	1.E+06	1.E+06	1.E+07	1.E+07	1.E+07
WAS	Flash nonvolatile data retention (years) [15]	10–20		10–20	20		20	20		20
IS	Flash nonvolatile data retention (years) [15]	10–20	10–20	10–20	20	20	20	20	20	20
WAS	Flash maximum number of bits per cell (MLC) [16]	8		8	8		8	8		8
IS	Flash maximum number of bits per cell (MLC) [16]	8	8	8	8	8	8	8	8	8
WAS	FeRAM technology node – F (nm) [17]	100		80	70		57	50		45
IS	FeRAM technology node – F (nm) [17]	100	90	80	70	64	57	50	48	45
WAS	FeRAM cell size – area factor a in multiples of F^2 [18]	8		8	8		8	8		8
IS	FeRAM cell size – area factor a in multiples of F^2 [18]	8	8	8	8	8	8	8	8	8
WAS	FeRAM cell size (μm^2) [19]	0.08		0.051	0.039		0.026	0.02		0.016
IS	FeRAM cell size (μm^2) [19]	0.08	0.065	0.051	0.039	0.033	0.026	0.02	0.018	0.016
WAS	FeRAM cell structure [20]	1T1C		1T1C	1T1C		1T1C	1T1C		1T1C
IS	FeRAM cell structure [20]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
WAS	FeRAM capacitor structure [21]	3D		3D	3D		3D	3D		3D
IS	FeRAM capacitor structure [21]	3D	3D	3D	3D	3D	3D	3D	3D	3D
WAS	FeRAM capacitor footprint (μm^2) [22]	0.03		0.019	0.015		0.01	0.0075		0.0061
IS	FeRAM capacitor footprint (μm^2) [22]	0.071	0.065	0.06	0.057	0.052	0.048	0.045	0.042	0.038
WAS	FeRAM capacitor active area (μm^2) [23]	0.076		0.065	0.06		0.052	0.048		0.045
IS	FeRAM capacitor active area (μm^2) [23]	0.024	0.02	0.015	0.013	0.01	0.008	0.0061	0.005	0.0037
WAS	FeRAM cap active area/footprint ratio [24]	2.53		3.42	4		5.2	6.4		7.38
IS	FeRAM cap active area/footprint ratio [24]	2.9	3.25	4	4.4	5.2	6	7.4	8.4	10.3
WAS	Ferro capacitor voltage (V) [25]	1		1	0.7		0.7	0.7		0.7
IS	Ferro capacitor voltage (V) [25]	1	1	1	0.7	0.7	0.7	0.7	0.7	0.7
WAS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	40		40	40		40	40		40
IS	FeRAM minimum switching charge density ($\mu C/cm^2$) [26]	40	40	40	40	40	40	40	40	40

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

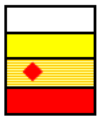


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Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	FeRAM endurance (read/write cycles) [27]	>1E16		>1E16	>1E16		>1E16	>1E16		>1E16
IS	FeRAM endurance (read/write cycles) [27]	>1E16	>1E16	>1E16	>1E16	>1E16	>1E16	>1E16	>1E16	>1E16
WAS	FeRAM nonvolatile data retention (years) [28]	10		10	10		10	10		10
IS	FeRAM nonvolatile data retention (years) [28]	10	10	10	10	10	10	10	10	10
WAS	SONOS/NROM technology node – F (nm) [29]	50		40	35		28	25		20
IS	SONOS/NROM technology node – F (nm) [29]	50	45	40	35	32	28	25	23	20
WAS	SONOS/NROM cell size – area factor a in multiples of F^2 [30]	6		6	6.5		6.5	7		7
IS	SONOS/NROM cell size – area factor a in multiples of F^2 [30]	6	6	6	6.5	6.5	6.5	7	7	7
WAS	SONOS/NROM typical cell size (mm^2) [31]	0.015		0.01	0.008		0.005	0.004		0.003
IS	SONOS/NROM typical cell size (mm^2) [31]	0.015	0.012	0.01	0.008	0.007	0.005	0.004	0.0037	0.003
WAS	SONOS/NROM maximum number of bits per cell (MLC) [32]	4		4	4		4	4		4
IS	SONOS/NROM maximum number of bits per cell (MLC) [32]	4	4	4	4	4	4	4	4	4
WAS	SONOS/NROM area per bit (mm^2) [33]	0.0038		0.0024	0.002		0.0013	0.0011		0.0007
IS	SONOS/NROM area per bit (mm^2) [33]	0.0038	0.003	0.0024	0.002	0.0018	0.0013	0.0011	0.0009	0.0007
WAS	SONOS L_g-stack (physical – μm) [34]	0.16		0.16	0.15		0.15	0.14		0.14
IS	SONOS L_g-stack (physical – μm) [34]	0.16	0.16	0.16	0.15	0.15	0.15	0.14	0.14	0.14
WAS	SONOS highest W/E voltage (V) [35]	5.0–5.5		5.0–5.5	5.0–5.5		5.0–5.5	4.5.–5.0		4.0–4.5
IS	SONOS highest W/E voltage (V) [35]	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	5.0–5.5	4.5.–5.0	4.5.–5.0	4.0–4.5
WAS	SONOS/NROM I_{read} (μA) [36]	25–35		24–34	23–33		22–32	21–31		20–30
IS	SONOS/NROM I_{read} (μA) [36]	25–35	25–35	24–34	23–33	23–33	22–32	21–31	21–31	20–30

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

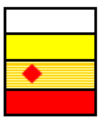


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Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	SONOS/NROM tunnel oxide thickness (nm) [37]	3		3	2.5		2.5	2		2
IS	SONOS/NROM tunnel oxide thickness (nm) [37]	3	3	3	2.5	2.5	2.5	2	2	2
WAS	SONOS/NROM nitride dielectric thickness (nm) [38]	4		4	4		4	3.5		3.5
IS	SONOS/NROM nitride dielectric thickness (nm) [38]	4	4	4	4	4	4	3.5	3.5	3.5
WAS	SONOS/NROM blocking (top) oxide thickness (nm) [39]	4		4	4		4	4		4
IS	SONOS/NROM blocking (top) oxide thickness (nm) [39]	4	4	4	4	4	4	4	4	4
WAS	SONOS/NROM endurance (erase/write cycles) [40]	1.00E+08		1.00E+08	1.00E+08		1.00E+08	1.00E+09		1.00E+09
IS	SONOS/NROM endurance (erase/write cycles) [40]	1.E+08	1.E+08	1.E+08	1.E+08	1.E+08	1.E+08	1.E+09	1.E+09	1.E+09
WAS	SONOS/NROM nonvolatile data retention (years) [41]	10–20		10–20	10–20		10–20	10–20		10–20
IS	SONOS/NROM nonvolatile data retention (years) [41]	10–20	10–20	10–20	10–20	10–20	10–20	10–20	10–20	10–20
WAS	MRAM technology node – F (nm) [42]	45		35	32		25	22		18
IS	MRAM technology node – F (nm) [42]	45	40	35	32	28	25	22	20	18
WAS	MRAM cell size – area factor a in multiples of F^2 [43]	22.2		22.2	22.2		22.2	22.2		22.2
IS	MRAM cell size – area factor a in multiples of F^2 [43]	22.2	22.2	22.2	22.2	22.2	22.2	22.2	22.2	22.2
WAS	MRAM typical cell size (μm^2) [44]	0.04		0.03	0.02		0.01	0.01		0.01
IS	MRAM typical cell size (μm^2) [44]	0.045	0.036	0.027	0.023	0.017	0.014	0.01	0.009	0.007
WAS	MRAM switching field (Oe) [45]	120		120	120		120	120		120
IS	MRAM switching field (Oe) [45]	120	120	120	120	120	120	120	120	120
WAS	MRAM write energy (pJ) [46]	35		30	25		23	20		18
IS	MRAM write energy (pJ) [46]	35	33	30	25	24	23	20	19	18
WAS	MRAM active area per cell (μm^2) [47]	0.03		0.02	0.01		0.01	0.01		0.01
IS	MRAM active area per cell (μm^2) [47]	0.03	0.025	0.02	0.01	0.01	0.01	0.01	0.01	0.01

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



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Table 50b Non-Volatile Memory Technology Requirements—Long-term UPDATED (continued)

	Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018
	Technology Node	hp45			hp32			hp22		
	DRAM ½ Pitch (nm)	45	40	35	32	28	25	22	20	18
WAS	MRAM resistance-area product (Kohm-μm^2) [48]	1.1		0.95	0.8		0.7	0.6		0.55
IS	MRAM resistance-area product (Kohm-μm^2) [48]	1.1	1	0.95	0.8	0.75	0.7	0.6	0.6	0.55
WAS	MRAM magnetoresistance ratio(%) [49]	60		65	70		70	70		70
IS	MRAM magnetoresistance ratio(%) [49]	60	65	65	70	70	70	70	70	70
WAS	MRAM nonvolatile data retention (years) [50]	>10		>10	>10		>10	>10		>10
IS	MRAM nonvolatile data retention (years) [50]	>10	>10	>10	>10	>10	>10	>10	>10	>10
WAS	MRAM write endurance (read/write cycles) [51]	>1e15		>1e15	>1e15		>1e15	>1e15		>1e15
IS	MRAM write endurance (read/write cycles) [51]	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15	>1e15
WAS	MRAM endurance – tunnel junction reliability (years at bias) [52]	>10		>10	>10		>10	>10		>10
IS	MRAM endurance – tunnel junction reliability (years at bias) [52]	>10	>10	>10	>10	>10	>10	>10	>10	>10



Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

Notes for Tables 50a and 50b

[1] In the past Flash devices tended to lag behind the current CMOS technology node, but that delay no longer exists. This entry provides the F value for designs in the indicated time period.

[2] The area factor "a" = cell area/F^2, so this entry presents the expected range for Flash NOR cell area in multiples of the implementation technology node F^2. Note the lack of long term scaling.

[3] The area factor "a" = cell area/F^2, so this entry presents the Flash NAND cell area in multiples of F^2 the implementation technology node. Flash NAND enjoys a small cell size because much of the cell structure is shared among a group of cells. (SLC single level cell, MLC multilevel cell.)

[4] A typical Flash NOR cell size in micrometers squared is estimated using the midrange area factor "a."

[5] This is the physical length of the control gate of Flash NOR devices.

[6, 7] This is the highest voltage relative to ground seen in the cell array. It is not usually an external supply.

*[8] The current reduces with scaling at a rate higher than W/(L*Cox) to reduce the voltage overdrive factor.*

[9] The coupling ratio is the (control gate to floating gate capacitance)/(total floating gate to source, drain and substrate capacitance).

[10, 11] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This difficult trade off problem hinders scaling.

[12, 13] Interpoly dielectric must be thick enough to assure retention but thin enough to assure an almost constant coupling ratio. Charge retention when the dielectric is scaled downward is the major issue.

[14] E/W endurance requirements vary with the specifics of an application, but 1E5 cycles have been accepted as the historical minimum acceptable level for a useful product. It is expected that emerging technology will allow both tradeoffs of endurance for retention as well as increases in the specified minimum endurance capability as device design options.

[15] Retention is a defect related parameter rather than an intrinsic device characteristic. Improvement in defect control and accumulation of device history is expected to eventually allow specification of 20 years retention. Also, it should become possible to accept a reduced retention specification as a tradeoff for increased E/W endurance.

[16] Cell read out distinguishes between four levels of charge storage to provide two storage bits. Progression to 16 and 256 levels is anticipated. (MLC multilevel cell).

[17] This entry is the critical dimension "F" within the FeRAM cell for stand-alone memory devices (not embedded devices).

[18] This is the area factor "a" = cell size/F^2. FeRAM cell size is presented in terms of F^2 multiples of the FeRAM implementation technology node.

[19] FeRAM cell size is presented in terms of micrometers squared. It is the product $a \times F^2$.

[20] FeRAM cell structures have migrated to one transistor, one capacitor (1T1C) formats. Other alternative configurations are under investigation such as Chain-FeRAM.

[21] The geometry of the capacitor is a key factor in determining cell size. Stacked planar films are expected to be replaced by more efficient 3D structures.

[22] This is the footprint of the capacitor in micrometers squared. It is this area that constitutes the capacitor area contribution to the cell size. For 2003–2004 $8F^2$, for 2005–2009 $4F^2$, and for 2010–2018 F^2 are assumed.
[23] This is the actual effective area of the capacitor. It can be larger than the footprint because of the utilization of area in the third dimension.
[24] This ratio of the effective area to the footprint gives a measure of the impact of utilization of the third dimension.
[25] This is the operating voltage (V_{op}) applied to the capacitor. Low voltage operation is a difficult key design issue.
[26] The minimum switching charge density in $\mu C/cm^2$ is a useful design parameter. It is equal to the cell minimum switching charge divided by the capacitor actual effective area. The capacitor voltage is taken as V_{op}.
[27] FeRAM is a destructive read-out technology, so every read is accompanied by a write to restore the data. Endurance cycles are taken as the sum of all read and all write cycles. For FeRAM to compete with DRAM and SRAM the cycle endurance should be about 1E15. Test time is a serious concern. Note that operation at 100 MHz for 10 years would accumulate 1E16 cycles.
[28] This is the data retention requirement while the device is disconnected from power. It is usually specified at 85ºC.
[29] SONOS/NROM devices have recently been introduced into the commercial market and will tend to lag the current CMOS technology node by one year; however, similar to Flash floating-gate technology, this gap will close rapidly due to low programming voltages combined with CMOS compatibility (i.e. single-level polysilicon). This entry provides the F value for designs in the indicated time period.
[30] The area factor "a" = cell area/F^2. This entry depicts the expected SONOS/NROM NOR cell area in multiples of the implementation technology node F^2. The reduced ONO gate stack thickness and low programming voltages should permit long range scaling of this technology.
[31] The expected "typical" SONOS/NROM NOR cell size is presented in terms of micrometers squared.
[32] MBC signifies "multiple bit storage," while MLC signifies "multiple level storage." The SONOS/NROM cell stores charge in two distinct locations – in the nitride over the source and drain junctions. Thus, in the simplest case there are two distinct bits within each cell; however, each charge location may be partitioned into multiple levels, thereby, increasing the bit storage per cell.
[33] The expected "typical" SONOS/NROM NOR area per bit is presented in terms of micrometers squared.
[34] This is the physical length of the gate of SONOS/NROM devices in micrometers as there is only a single gate, similar to a MOSFET.
[35] This is the highest voltage relative to ground seen in the cell array. It is not usually an external supply.
*[36] Reduction rate is higher than (W/L)*Cox) to reduce the voltage overdrive factor.*
[37] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This offers a challenge to scaling.
[38] The nitride dielectric provides the charge storage medium and its thickness is a compromise between program/erase voltages, erase/write window, retention, process control and endurance. This offers a challenge to scaling.
[39] The blocking (top) oxide thickness isolates the charge storage region (nitride) from the gate electrode. Its thickness is a compromise between program/erase voltages and retention. This offers a challenge to scaling.
[40] E/W endurance (erase/write cycles) requirements vary with the specifics of an application, but 1E5cycles has been accepted as the historical minimum acceptable level for a useful product. It is expected that emerging technology will allow both tradeoffs of endurance for retention as well as increases in the specified minimum endurance capability as device design options.
[41] Retention is a defect related parameter rather than an intrinsic device characteristic. Improvement in defect control and accumulation of device history is expected to eventually allow specification of 20 years retention. Also, it should become possible to accept a reduced retention specification as a tradeoff for increased E/W endurance.
[42] MRAM devices are expected to lag the CMOS current technology node up until the 65 nm node in 2007. This entry provides the F value for designs in the indicated time period.
[43] The area factor "a" = cell area/F^2. This entry is the expected MRAM cell area in multiples of the implementation technology node F^2.
[44] The expected "typical" MRAM cell size is presented in micrometers squared.
[45] The MRAM switching field is the magnetic intensity H required to change the direction of magnetization of the cell.
*[46] MRAM switching energy per bit is calculated as (write current * power supply voltage * write time). It is preferred to use the median value of switching energy measured on a multi-megabit array. A good estimate of power drain is (switching energy * number of writes per second).*
*[47] MRAM active bit area is the area of the magnetic material stack within the cell. It represents the "A" in the R*A product.*
*[48] MRAM resistance-area product (i.e., the R*A product) is an intrinsic property of the magnetic material stack that provides a convenient basis for comparing cells of different sizes. The R*A product can be computed by measuring the effective low state resistance (R_{low}) of the magnetic tunnel junction and multiply it by the active bit area of the magnetic stack.*
[49] MRAM magnetoresistive ratio is calculated as $100*(R_{high} - R_{low})/R_{low}$. This ratio summarizes the difference between a logic ONE and a logic ZERO, and as such it represents the intrinsic capability of the magnetic stack. The magnetic tunnel junction resistance values are to be measured at low currents.
[50] MRAM devices are required to retain data while unpowered. This entry states the retention requirement in years.
[51] This entry is the required number of read/write cycles that an MRAM device must be able to endure without degradation that impacts the ability of the device to pass all operating specifications.
[52] An MRAM device is required to meet this minimum life requirement when the magnetic material stack is continuously under bias.

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Table 51 Reliability Difficult Challenges

Difficult Challenges ≥45 nm/ Through 2010	*Summary of Issues*
High-κ Gate Dielectrics	Dielectric breakdown characteristics (hard and soft breakdown) Influence of charge trapping and NBTI on threshold voltage stability Stability and number of fixed charges
Metal Gate	Impact of metal-ion drift and/or diffusion on gate dielectric reliability Work function control and stability Metal susceptibility to oxidation Thermo-mechanical issues due to large thermal expansion mismatch Impact of implantation
Copper/Low-κ Interconnects	Stress migration of Cu vias and lines Cu via and line electromigration performance Thermal-mechanical stability of the interfaces between metals, barriers and interlevel dielectrics and resulting line-to-line leakage Time Dependent Dielectric Breakdown (TDDB) of the Cu/low-κ system Reliability impact of lower thermal conductivity of low-κ dielectric Reliability issues due to the porous nature of the low-κ dielectrics and moisture Reliability impact of the lower mechanical strength in the Cu/low-κ system, including the impact of packaging
Packaging	Ability of bumps to withstand thermal and mechanical stresses while providing sufficient current carrying capability Solder joints fracture at 1st and 2nd level interconnects Electromigration in package traces, vias and bumps Impact of increasing Coefficient of Thermal Expansion (CTE) mismatch between low-κ, silicon and organic packages
Design and Test for Reliability	Simulation tools for concurrent optimization of circuit performance and reliability Tools to simulate electromigration, thermal-mechanical stress and process induced charging Soft error detection and correction at chip and system level, including random logic faults Screens for resistive and capacitively coupled interconnect defects Alternative screens for decreasing burn-in effectiveness

Table 52a Reliability Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009	
Technology Node		hp90			hp65			
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50	
Early failures (ppm) (First 4000 operating hours)** [1]	50–2000	50–2000	50–2000	50–2000	◆50–2000	◆50–2000	◆50–2000	Customer needs; new materials (High κ in 2004)
Long term reliability (FITS = failures in 1E9 hours) [2]	10–100	10–100	10–100	10–100	◆10–100	◆10–100	◆10–100	Customer needs; new materials (High κ in 2004)
Soft error rate (FITs)	1000	1000	1000	1000	◆1000	◆1000	◆1000	Scaling
Relative failure rate per transistor (normalized to 130 nm) [3]	1	0.8	0.63	0.5	◆ 0.4	TBD	TBD	Number of transistors
Relative failure rate per m of interconnect (normalized to 130 nm node) [4]	1	0.84	0.64	0.58	◆ 0.52	◆ 0.41	◆ 0.37	Customer needs; J11 length of interconnect

Table 52b Reliability Technology Requirements—Long-term

Year of Production	2010	2012	2013	2015	2016	2018
Technology Node	hp45		hp32		hp22	
DRAM ½ Pitch (nm)	45	35	32	25	22	18
Early failures (ppm) (First 4000 operating hours)**[1]	◆50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
Long term reliability (FITS = failures in 1E9 hours) [2]	◆10–100	10–100	10–100	10–100	10–100	10–100
Soft error rate (FITs)	◆ 1000	1000	1000	1000	1000	1000
Relative failure rate per transistor (normalized to 130 nm) [3]	◆ 0.2		0.1		0.04	
Relative failure rate per m of interconnect (normalized to 130 nm) [4]	◆ 0.36	0.26	0.25	0.16	0.17	0.11

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known ◆
Manufacturable solutions are NOT known

Notes for Tables 52a and 52b
Reliability requirements vary with different applications. For many mainstream customers it will be sufficient to hold current reliability levels steady during this period of rapid technological change. However, other customers would like reliability levels to be improved. Degradation of current reliability levels is not acceptable. Reliability requirements are for the packaged device and include both chip and package related failure modes.
A reliability qualification can always be attempted with available knowledge. The better the knowledge the less risk in the qualification and vice versa. Yellow coloring indicates some risk. Striped indicates a greater risk (due to changed and possible new failure mode 0. Finally, red indicates an unspecified solution (e.g., what technology will be used for post-CU) for which the reliability risk cannot be assessed until details about the solution are provided.
[1] Failures during the first 4000 hours of operation (~1 year's use at 50% duty cycle). Early failures are associated with defects.
[2] Long term reliability rate applies for the specified lifetime of the IC.
[3] While the overall IC failure rate does not change with time, as the number of transistors increase [from ORTC], the relative failure rate per transistor must decrease.
[4] As the length of interconnect increases [from Interconnect Technology Requirements Tables], the failure rate per m of interconnect must decrease. Even more important for reliability is the increase in the number of vias.

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FOLDER 12

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2007 EDITION

EXECUTIVE SUMMARY

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

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INTRODUCTION

OVERVIEW

For more than four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles roughly every 24 months). The most significant trend is the decreasing cost-per-function, which has led to significant improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor throughput**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last three decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for Semiconductors (NTRS), which had 1992, 1994, and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of the Roadmap and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999. Since then, the ITRS has been updated in even-numbered years and fully revised in odd-numbered years. The overall objective of the ITRS is to present industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, universities, governments, and other research providers or funders. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that most need research breakthroughs.

The ITRS is a dynamic process, evident by the evolution of the ITRS documents. The ITRS reflects the semiconductor industry migration from geometrical scaling to equivalent scaling. Geometrical scaling [such as Moore's Law] has guided targets for the previous 30 years, and will continue in many aspects of chip manufacture. Equivalent scaling targets, such as improving performance through innovative design, software solutions, and innovative processing, will increasingly guide the semiconductor industry in this and the subsequent decade. Since 2001 the ITRS has responded by introducing new chapters on System Drivers (2001), Emerging Research Devices and Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (2005), and most recently in 2007, Emerging Research Materials, to better reflect this evolution of the semiconductor industry.

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of electronics would further reduce the cost per function (historically, ~25–29%% per year) and promote market growth for integrated circuits (historically averaging ~17% per year, but maturing to slower growth in more recent history). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?"

It is forecasted that by the end of the next decade it will be necessary to augment the capabilities of the CMOS process by introducing multiple new devices that will hopefully realize some properties beyond the ones of CMOS devices. However, it is believed that most likely these new devices will not have all the properties of CMOS devices and therefore it is anticipated that heterogeneous integration either at the chip level or at the package level will integrate these new capabilities around a CMOS core.

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The participation and continued consensus of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. ensures that the 2007 ITRS remains the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The complete 2007 ITRS and past editions of the ITRS are available for viewing and printing as electronic documents at the Internet web site *http://www.itrs.net*.

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each sponsoring region (Europe, Japan, Korea, Taiwan, and the U.S.A.). The principal IRC functions include the following:

- Providing guidance/coordination for the International Technology Working Groups (ITWGs)
- Hosting the ITRS Workshops
- Editing the ITRS

The International Technology Working Groups write the corresponding technology-area chapters of the ITRS. The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points.

For the 2007 ITRS, the Focus ITWGs are the following:

- System Drivers
- Design
- Test and Test Equipment
- Process Integration, Devices, and Structures
- RF and Analog / Mixed-signal Technologies for Wireless Communications
- Emerging Research Devices
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging

Crosscut ITWGs are the following:

- Emerging Research Materials
- Environment, Safety, and Health
- Yield Enhancement
- Metrology
- Modeling and Simulation

The ITWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. The demographics per ITWG reflect the affiliations that populate the technology domains. For example, with a longer-term focus area such as Emerging Research Devices, the percentage of research participants is higher than suppliers. In the process technologies of Front End Processes, Lithography, and Interconnect, the percentages of suppliers reflect the equipment/materials suppliers' participation as much higher due to the near-term requirements that must be addressed.

For the 2007 edition, three ITRS meetings were held worldwide as follows: Annecy, France (sponsored by the ESIA and hosted by STMicroelectronics); San Francisco, U.S.A., sponsored by the SIA, organized by SEMATECH and co-hosted with SEMI/North America; and Chiba, Japan (sponsored and co-hosted by JEITA and SEMI Japan). These meetings provided the main forums for face-to-face discussions among the members of each ITWG and coordination among the

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different ITWGs. In addition, the ITRS teams hold public ITRS conferences bi-annually to present the latest Roadmap information and to solicit feedback from the semiconductor industry at-large.

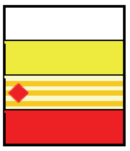
The ITRS is released annually, with updates and corrections to data tables each even-numbered year (such as 2000, 2002, 2004, 2006) while complete editions are released each odd-numbered year (2001, 2003, 2005, 2007). This ITRS process thus ensures continual assessment of the semiconductor industry's near and long-term needs. It also allows the teams to correlate in a timely fashion the ITRS projections to most recent research and development breakthroughs that may provide solutions to those needs.

ROADMAP CONTENT

The ITRS assesses the principal technology needs to guide the shared research, showing the "targets" that need to be met. These targets are as much as possible quantified and expressed in tables, showing the evolution of key parameters over time. Accompanying text explains and clarifies the numbers contained in the tables where appropriate.

The ITRS further distinguishes between different maturity or confidence levels, represented by colors in the tables, for these targets:

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



The first situation, "Manufacturable solutions exist, and are being optimized," indicates that the target is achievable with the currently available technology and tools, at production-worthy cost and performance. The yellow color is used when additional development is needed to achieve that target. However, the solution is already identified and experts are confident that it will demonstrate the required capabilities in time for production start. The situation "Interim Solutions are Known" means that limitations of available solutions will not delay the start of production, but work-arounds will be initially employed in these cases. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity. The fourth and last situation is highlighted as "red" on the Roadmap technology requirements tables and has been referred to as the "Red Brick Wall" since the beginning of ITRS. (The "red" is officially on the Roadmap to clearly warn where progress might end if tangible breakthroughs are not achieved in the future.) Numbers in the red regime, therefore, are only meant as warnings and should not be interpreted as "targets" on the Roadmap. For some Roadmap readers, the "red" designation may not have adequately served its *sole* purpose of highlighting significant and exciting challenges. There can be a tendency to view *any* number in the Roadmap as "on the road to sure implementation" regardless of its color. To do so would be a serious mistake.

"Red" indicates where there are no "known manufacturable solutions" (of reasonable confidence) to continued scaling in some aspect of the semiconductor technology. An analysis of "red" usage might classify the "red" parameters into two categories:

1. where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which the industry doesn't have much confidence in any currently proposed solution(s), or
2. where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end)

To achieve the red parameters of the first category, breakthroughs in research are needed. It is hoped that such breakthroughs would result in the "red" turning to "yellow" (manufacturable solutions are known) and, ultimately "white" (manufacturable solutions are known and are being optimized) in future editions of ITRS.

As indicated in the overview, the Roadmap has been put together in the spirit of defining what technical capabilities the industry needs to develop in order to stay on Moore's Law and the other trends, and when. So the ITRS is not so much a forecasting exercise as a way to indicate where research should focus to continue Moore's law. In that initial "challenge" spirit, the Overall Roadmap Technology Characteristics (ORTC) team updates key high-level technology needs, which establish some common reference points to maintain consistency among the chapters. The high-level targets expressed in the ORTC tables are based in part on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies.

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Over the years, however, the Roadmap has sometimes been seen as a self-fulfilling prophecy. To a certain extent this is also a valid view, as companies have benchmarked each other against the Roadmap, and it proved very effective in providing thrust for research. So it is not unreasonable to use the Roadmap targets, when manufacturing solutions or acceptable workarounds are known, as guidelines to forecasting exercises.

What these targets should never be used for, however, is as basis for legal claims in commercial disputes or other circumstances. In particular, the participation in the ITRS roadmapping process does not imply in any way a commitment by any of the participating companies to comply with the Roadmap targets. We recall that the ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual product or equipment.

TECHNOLOGY CHARACTERISTICS

As mentioned above, a central part of the IRC guidance and coordination is provided through the initial creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics (ORTC) tables. Each ITWG chapter contains several principal tables. They are individual ITWGs' technology requirements tables patterned after the ORTC tables. For the 2007 ITRS, the ORTC and technology requirements tables are fully annualized and in both the "Near-term Years" (2005, 2006… through 2015) and "Long-term Years" (2016, 2017 … through 2022) This format is illustrated in Table B, which contains a few key rows from lithography-related ORTC Table 1a and 1b, including the new Flash product uncontacted polysilicon half-pitch technology trend line item. In the previous 2005 Roadmap editions, the DRAM stagger-contacted M1 half pitch line item was used as a standard header for all the ITRS ITWG tables; however, beginning with the 2007 edition, the IRC has requested that only the year of first production be required as a standard header. At the discretion of the ITWGs, other product technology trend driver line items may be selected from ORTC Table 1a and 1b for use in their ITWG tables as overall headers indicating key drivers for their tables.

Table B ITRS Table Structure—Key Lithography-related Characteristics by Product

Near-term Years

YEAR OF PRODUCTION	2007	2008	2009	2010	2011	2012	2013	2014	2015
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	65	57	50	45	40	36	32	28	25
MPU/ASIC stagger-contacted Metal 1 (M1)½ Pitch (nm)	68	59	52	45	40	36	32	28	25
Flash Uncontacted Poly Si ½ Pitch (nm)	54	45	40	36	32	28	25	23	20
MPU Printed Gate Length (nm)	42	38	34	30	27	24	21	19	17
MPU Physical Gate Length (nm)	25	23	20	18	16	14	13	11	10

Long-term Years

YEAR OF PRODUCTION	2016	2017	2018	2019	2020	2021	2022
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	22	20	18	16	14	13	11
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	22	20	18	16	14	13	11
Flash Uncontacted Poly Si ½ Pitch (nm)	18	16	14	13	11	10	9
MPU Printed Gate Length (nm)	15	13	12	11	9	8.4	7.5
MPU Physical Gate Length (nm)	9	8	7	6.3	5.6	5.0	4.5

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. Please refer to the Glossary *for detailed definitions for Year of Introduction and Year of Production.*

TECHNOLOGY PACING

In previous editions of the ITRS, the term "technology node" (or "hpXX node") was used in an attempt to provide a single, simple indicator of overall industry progress in integrated circuit (IC) feature scaling. It was specifically defined as the smallest half-pitch of contacted metal lines on any product. Historically, DRAM has been the product which, at a given time, exhibited the tightest contacted metal pitch and, thus, it "set the pace" for the ITRS technology nodes. However, we are now in an era in which there are multiple significant drivers of scaling and believe that it would be misleading to continue with a single highlighted driver, including DRAM

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For example, along with half-pitch advancements, design factors have also rapidly advanced in Flash memory cell design, enabling additional acceleration of functional density. Flash technology has also advanced the application of electrical doubling of density of bits, enabling increased functional density independent of lithography half-pitch drivers. A second example is given by the MPU/ASIC products, for which the speed performance driver continues to be the gate-length isolated feature size, which requires the use of leading-edge lithography and also additional etch technology to create the final physical dimension.

Significant confusion relative to the historical ITRS node definition continues to be an issue in many press releases and other documents that have referred to "node acceleration" based on other, frequently undefined, criteria. Of course, we now expect different IC parameters to scale at different rates, and it is certainly legitimate to recognize that many of these have product-specific implications. In the 2007 ITRS, we will continue the practice of eliminating references to the term "technology node." As mentioned above, the IRC has recommended that the only standard header will be year of first production, and DRAM M1 half-pitch is just one among several historical indicators of IC scaling. With this latest change to standard ITRS table format policy, it is hoped that the ITRS will not contribute to industry confusion related to the concept of "technology node." Of course, "node" terminology will continue to be used by others. Hopefully, they will define their usage within the context of the application to the technology of a specific product.

For reference on the 2005 ITRS common definition of M1 half-pitch for all products, as well as the definition of polysilicon half-pitch for FLASH memory, see Figure 1.

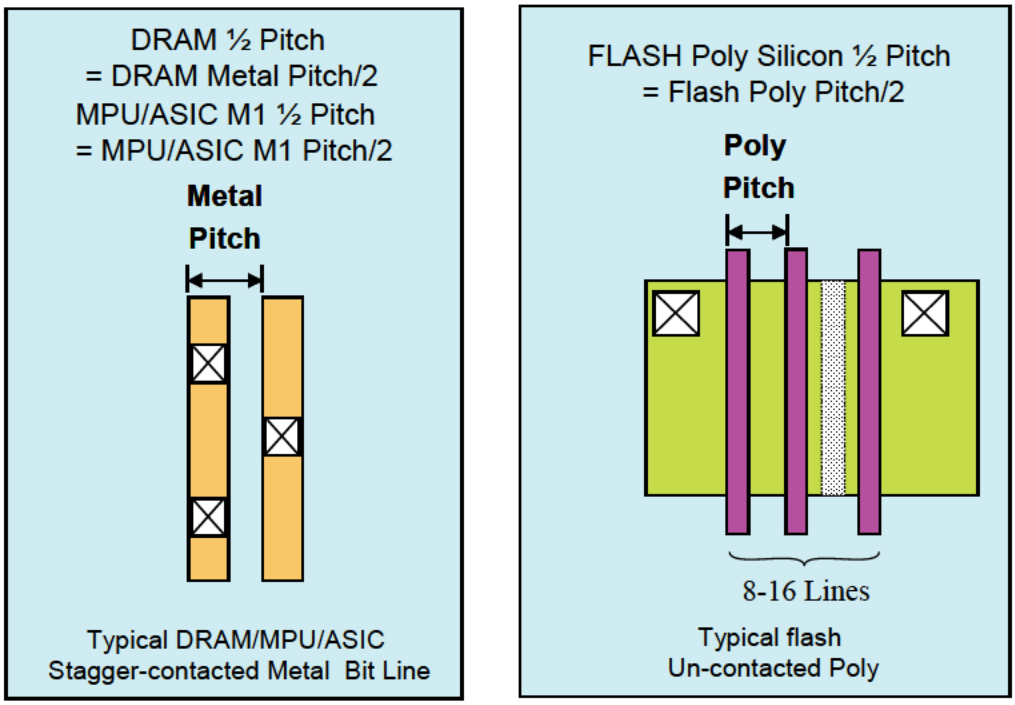


Figure 1 2005 Definition of Pitches

MEANING OF ITRS TIME OF INTRODUCTION

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "Time of Introduction" in the ITRS is the "Year of Production," which is defined in Figure 2.

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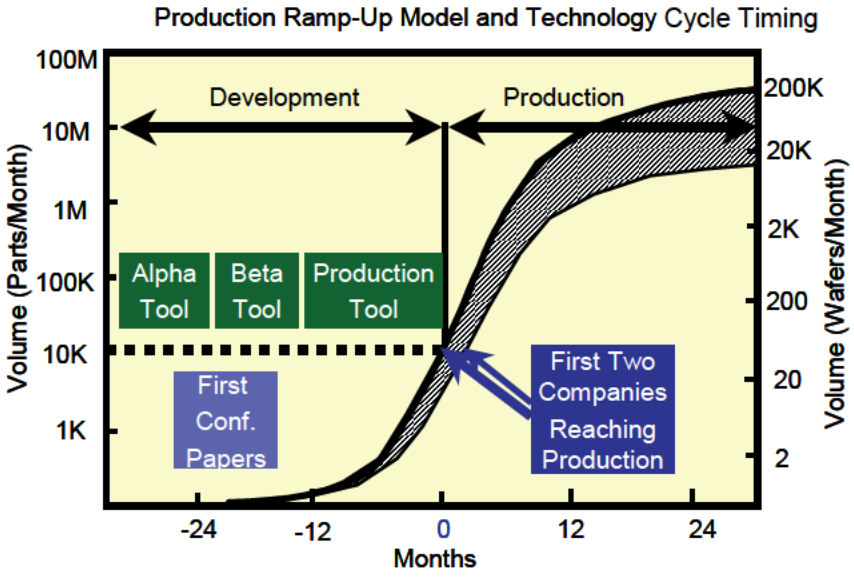


Figure 2 A Typical Production "Ramp" Curve

The "Production" time in the ITRS refers to the time when the first company brings a technology to production and a second company follows, typically within three months. Production means the completion of both process and product qualification. The product qualification means the approval by customers to ship products, which may take one to twelve months to complete after product qualification samples are received by the customer. Preceding the production, process qualifications and tool development need to be completed. Production tools are developed typically 12 to 24 months prior to production. This means that alpha and succeeding beta tools are developed preceding the production tool.

Also note that the Production "time zero (0)" in Figure 2 can be viewed as the time of the beginning of the ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (WSPM) capacity or more, the time to ramp from 20 WSPM to full capacity can take nine to twelve months. This time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month if the chip size were 140 mm^2 (430 gross die per 300 mm wafer × 20K WSPM × 70% total yield from wafer starts to finished product = 6M units/month).

In addition, note that the ITRS ramp timing in this example is in reference to the ramp of a technology cycle within a given wafer generation. Now that the time for a new wafer generation transition, 450mm, is nearly upon us, additional scrutiny must be given to the historical ramp rate for a technology cycle that may be ramped in two wafer generations of the first leading companies at the same time. It is during that transition of a technology cycle coexisting within two wafer generations that the economic productivity gain modeling is also examined.

2007 SICAS Industry Manufacturing Technology Capacity Update

It is noted that the ITRS, by its definition, focuses on forecasting the earliest introduction of the leading-edge semiconductor manufacturing technologies, which support the production of selective leading-edge driver product markets, such as DRAM, Flash, MPU, and high-performance ASICs. It is, however, true that many companies, for a variety of reasons, may choose to introduce a leading-edge technology later than the earliest introduction of the leading-edge technology; hence, there is a wide variation of the technologies in actual production status from leading edge to trailing edge.

Figure 3 shows, in horizontal bar graph format (each bar width is proportional to silicon processing capacity), the actual, annual worldwide wafer production technology capacity distributions over different process feature sizes. The distributions of the overall industry technology capacity segments are tracked by feature-size splits, which are quite widespread.

The ITRS technology cycle, as measured by DRAM metal 1 (M1) half-pitch, is shown as yellow marks (for the historical actual timing), as reported by the industry surveys conducted by ITRS TWGs. The surveys conducted in 2003, 2005, and 2007 have indicated that first production of the leading-edge DRAM M1 half-pitch has been on a two-year cycle (for 0.71× reduction), from 250 nm in 1998 through 90 nm in 2004. However, the most recent survey update is indicating that the DRAM historical trend is tracking closer to the ITRS MPU trend. This will be investigated further in 2007 and reported in the 2008 Update. Details are included in the 2007 PIDS chapter.

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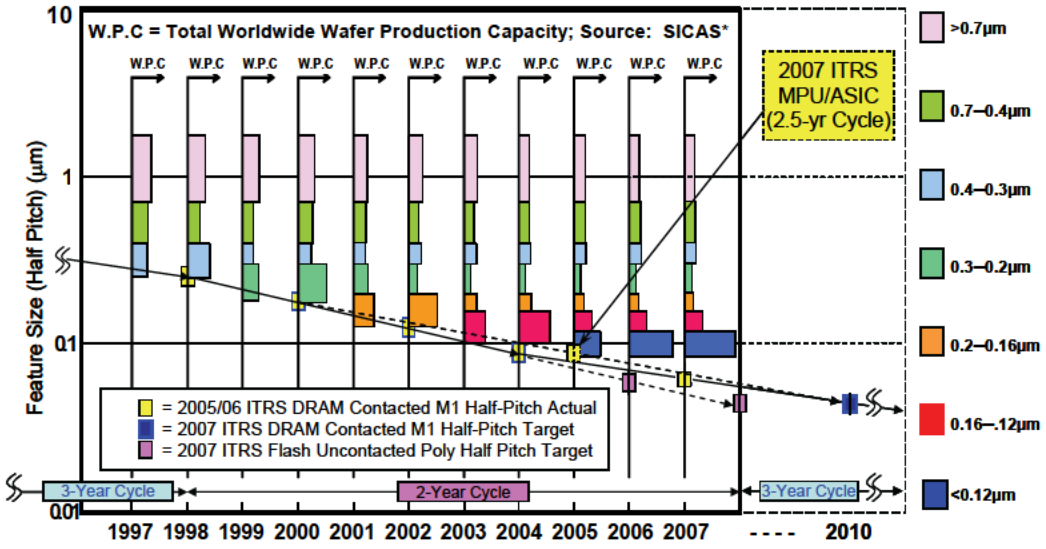
The blue mark indicates the timing for the next 2007 ITRS target for the 45 nm technology in 2010. Subsequent targets for 0.71× reduction of the DRAM M1 half-pitch are placed on a three-year cycle through the present ITRS roadmap horizon in 2022. Also included is the tracking of the Flash technology capacity trend for uncontacted poly; which has grown rapidly in market demand, and now contributes significantly to the industry capacity.

Note that the first production of the leading-edge feature size has historically ramped into a 20–30% industry capacity share within one year, and the timing of that 20–30% capacity share has been on the same cycle as the timing for first production. Furthermore, the relative percentage of the most leading-edge technology capacity has been rapidly growing. The combined capacity of the most recent two technology generations has typically grown to nearly half the capacity of the industry within two to three years after their introduction. The 2007 ITRS has updated the Flash technology trend to continue on a two-year cycle until 2008, which should add even more capacity at the most leading edge.

It should be noted that the capacity for the most leading edge technology (65 nm) is presently only available within the SICAS "<0.12" capacity split. The availability of the "<0.08 μ" split survey data, which would include the rapidly ramping 65 nm Flash technology cycle capacity, has been delayed from SICAS until late in 2007, therefore the actual analysis of the two-year or three-year technology demand cycle (to 20–30% of total MOS capacity) will not be available until the 2008 Update of the ITRS.

It is also notable that relative share of trailing edge capacity continues to appear to not decline as rapidly as might be expected (migrate upward to leading-edge); and the leading-edge capacity split shares should be expected to continue to "crowd" as products migrate to the most leading-edge capacity ("<0.08 μ" capacity data, when available). This phenomenon continues to hold significant implication for the markets and business models of the materials and equipment suppliers that ultimately develop and deliver the required solutions to the ITRS technology "Grand Challenges."

Suppliers must support not only longer-lasting trailing edge factories, but also many diverse technology factories at the leading edge. In addition, suppliers must deliver alpha and beta tools and materials two to three years ahead of the first production requirement, and then they must be prepared to ramp into production with overlapping technology demand capacities. These scenarios present both a market opportunity and also an R&D and support resource challenge to both suppliers and manufacturers, especially with the looming probability of 450 mm wafer generation investments.



Note The wafer production capacity data are plotted from the Semiconductor Industry Association (SIA) Semiconductor Industry Capacity Statistics (SICAS) 4Q data for each year, except 2Q data for 2007. The width of each of the production capacity bar corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.

Figure 3 Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution[1]

[1] *The data for the graphical analysis were supplied by the Semiconductor Industry Association (SIA) from their Semiconductor Industry Capacity Statistics (SICAS). The SICAS data is collected from worldwide semiconductor manufacturers (estimated >90% of Total MOS*

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ROADMAP SCOPE

Traditionally, the ITRS has focused on the continued scaling of CMOS (Complementary Metal-Oxide-Silicon) technology. However, since 2001, we have reached the point where the horizon of the Roadmap challenges the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths below 9 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, the ITRS must address post-CMOS devices. The Roadmap is necessarily more diverse for these devices, ranging from more familiar non-planar CMOS devices to exotic new devices such as spintronics. Whether extensions of CMOS or radical new approaches, post-CMOS technologies must further reduce the cost-per-function and increase the performance of integrated circuits. In addition, product performance increasingly does not scale only with the number of devices, but also with a complex set of parameters given by design choices and technology. Thus new technologies may involve not only new devices, but also new manufacturing and design paradigms.

Microprocessors, memories, and logic devices require silicon-based CMOS technologies. The downscaling of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. The essential functions on such a system-on-chip (SoC) are data storage and digital signal processing. However, many quantitative requirements, such as power consumption and communications bandwidth (e.g., RF), and many functional requirements, such as the functions performed by passive component, sensors and actuators, biological functions, and even embedded software functions, do not scale with Moore's Law. In many of these cases, non-CMOS solutions are employed. In the future, the integration of CMOS- and non-CMOS based technologies within a single package (or system-in-package, (SiP)) will become increasingly important. In terms of functionality, SoC and SiP can be complementary, and hence are not necessarily competing with each other. Functions initially fulfilled by non-CMOS dedicated technologies may eventually be integrated onto a CMOS SoC, using mixed technologies derived from core CMOS. Consequently, the partitioning of system-level functions between *and within* SoC and SiP is likely to be dynamic over time. This will require innovations in cross-disciplinary fields, such as nano-electronics, nano-thermomechanics, nano-biology, extremely parallel software, etc. For SiP applications, packaging will be a functional element and a key differentiator. This trend is represented graphically in Figure 4.

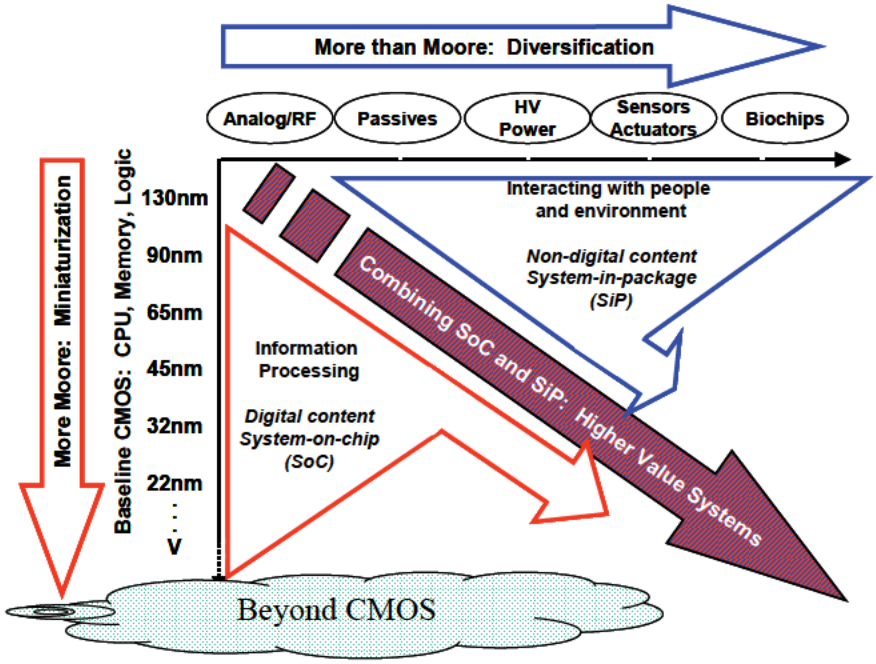


Figure 4 Moore's Law and More

Capacity) and published by the Semiconductor Industry Association (SIA), as of August, 2007. The detailed data are available to the public online at the SIA website, http://www.sia-online.org/pre_stat.cfm .

This concept of "More than Moore," introduced in the 2005 roadmap, has been further discussed and refined for the 2007 edition of the roadmap. In particular, a consensus has been reached on the following definitions. (Refer to Figure 4):

1. Scaling ("More Moore," vertical axis)

> 1a. *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
>
> 1b. *Equivalent Scaling* which occurs in conjunction with, and also enables, continued Geometrical Scaling, refers to (a) 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the performance of the chip; (b) novel design techniques and technology such as multi-core design. The objective of Equivalent Scaling is the continuation of "Moore's Law."

2. Functional Diversification ("More than Moore", horizontal axis)

Functional Diversification refers to the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board level into a particular package-level (SiP) or chip-level (SoC) implementation. In addition, the increasingly intimate integration of complex embedded software into SoCs and SiPs means that software might also need to become a fabric under consideration that directly affects performance scaling. The objective of "More than Moore" is to incorporate digital and non-digital functionality into compact systems.

It is expected that the relative weight of the "More than Moore" component of the industry evolution will increase over time. This increase leads to a growing diversity of the scientific fields that the research must cover in order to sustain the pace of innovation, while the financial constraints are becoming tighter. The question of the guidance of the research efforts, in which the ITRS is playing a pivotal role, is therefore crucial. Taking this into consideration, various working groups of the ITRS have been investigating the consequences of the "More than Moore" trend in their field of expertise. The results of that work, which will further gain momentum in the coming years, can be found in their respective chapters.

The scope of the 2007 ITRS specifically includes detailed technology requirements for all CMOS integrated circuits, including wireless communication and computing products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to design and manufacture CMOS ICs are also used for other products such as compound semiconductor, discrete, optical, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most IC-technology-based micro/nanotechnologies, even though that is not the explicit purpose of the Roadmap.

2007 ITRS SPECIAL TOPICS

EMERGING RESEARCH MATERIALS

Many of the new device and memory concepts that are being discussed in the ERD chapter will employ new materials, for example, for the device itself as well as for interconnect and passivation. The requirements for these new materials are critically dependant on the properties and specifications of the new devices and memories. This led in 2005 to the creation, within the ERD chapter, of a sub-group for Emerging Research Materials (ERM). In this edition of the roadmap, this subgroup has now become a full-fledged working group, and the results of this work are published in a dedicated Emerging Research Materials (ERM) chapter.

TRANSITION TO 450 MM

In the 2005 edition of the Roadmap, 2012 was adopted as the year of introduction of 450 mm wafers in volume production. This date of introduction depends not only on the mastering of all technical issues, associated with the transition of 450 mm, but also on the preparedness of the industry. Accordingly, during the past two years, the ITRS working groups and the IRC have been further collecting data to evaluate the timing of the introduction of 450 mm in production.

The rationale for a transition to 450 mm diameter wafer is productivity, one of the enablers of Moore's law. This is the ability—everything else staying the same—to decrease the manufacturing cost of each mm² of IC by the use of larger diameter wafers. Based on economic considerations, the International SEMATECH Manufacturing Initiative (ISMI) () has determined that to stay on this productivity curve, the industry needs to achieve 30% cost reduction and 50% cycle time improvement in manufacturing by 2012, which in their opinion is achievable only via a transition to 450 mm (while

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the cost reduction goal has been achieved through previous wafer generation changes, the cycle time goal is new). This opinion was reinforced by the conclusions of an analysis of potential 300 mm improvements, which showed that the so-called "300 mm Prime" program has cycle time opportunity but falls short of the traditional cost reduction required to stay on Moore's Law. This realization prompted ISMI to kick-off the 450 mm initiative in July 2007.

There are, however, several arguments to question this 2012 timing:

- On the equipment suppliers' side, having production equipments available in 2012 means that alpha tools must be available by 2009. So far no key suppliers have announced plans for a prototype tool by 2012.
- On the manufacturers' side, an important question is related to the initial investment "step function": the promises for productivity gains in 300 mm Fabs have proved to become true for very large investments, in the range of $4B or beyond. One might expect that the minimal economical size of a 450 mm Fab will be even larger, putting it beyond the reach of many companies. Furthermore, while an economic model which takes into consideration the industry as a whole may conclude that 2012 is the right time for transition to 450 mm, decision of individual companies may differ. So both the initial rate of growth of the 450 mm equipment market and its size at maturity can be questioned, which could lead equipment suppliers to delay their investment in the development of this new generation.
- Finally, readiness of wafer manufacturers is unclear: The Front-End Processes working group is now estimating that wafer suppliers will move the work on 450 mm wafers from research to development in 2009. For 300 mm, this transition occurred approximately seven years before 300 mm was used by IC manufacturers in production. So this would indicate a transition date for IC manufacturers to start moving to 450 mm in 2016.

Given all of the above, the ITRS is proposing a target range of 2012 to 2016 for the introduction of 450 mm wafers in production.

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GRAND CHALLENGES

IN THE NEAR-TERM (THROUGH 2015) AND LONG-TERM (2016 AND BEYOND)

OVERVIEW

The continued research and development efforts in our industry have brought about reacceleration and diversification of scaling. Flash device's scaling continues a two-year cycle until 2008, MPU is a 2.5-year cycle until 2010, and DRAM is a three-year cycle. The word "node" cannot define technology trend clearly anymore. In the chapter on PIDS, it is observed that there are many choices to improve MOSFET performance, which we call "Parallel Paths" of planer bulk metal-oxide semiconductor field effect transistor (MOSFET), fully depleted, silicon-on-insulator (FD-SOI) MOSFET, and multiple gate [e.g., field effect transistor structures (Fin-FET)]. The ITRS is entering a new era as the industry begins to address the theoretical limits of CMOS scaling. There remain many technological challenges in patterning, advanced materials, strain engineering particularly in non-planar device structures, junction leakage, process control, and manufacturability. Challenges also span SoC and SiP integration of CMOS with new types of memory devices. All these will be essential elements for the continuous growth of the semiconductor industry.

Each ITWG identified and listed "Difficult Challenges", which are included in this Executive Summary. In this section of "Grand Challenges," major "Difficult Challenges" are selected and described. This section is intended to help readers grasp an overall picture concerning major technological issues.

These "Grand Challenges" are classified into two categories: "Enhancing Performance" and "Cost-effective Manufacturing." They are also described according to the "near term" (2007 through 2015) and the "long term" (2016 through 2022) timeframes of the Roadmap.

IN THE NEAR TERM (THROUGH ~ 2015)

ENHANCING PERFORMANCE

LOGIC DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, FRONT END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

Scaling planar CMOS will face significant challenges. The conventional path of scaling, which was accomplished by reducing the gate dielectric thickness, reducing the gate length, and increasing the channel doping, might no longer meet the application requirements set by performance and power consumption. Introduction of new material systems as well as new device architecture, in addition to continuous process control improvement are needed to break the scaling barriers.

Reduction of the equivalent gate oxide thickness (EOT) has emerged as the most difficult challenge associated with the future device scaling, which is required for performance improvement. For low-power (LP) applications, oxynitride will no longer meet the strict leakage current requirement. For high-performance (HP) applications, EOT of less than 1 nm with adequate reliability is needed. Therefore, introduction of higher dielectric constant (high-κ) material in which tunneling current can be suppressed without sacrificing current drive will be necessary. The complete gate stack material systems need to be optimized together for best device characteristics and cost. These material changes pose a great challenge in MOSFET technology, where silicon dioxide/poly Si has long played a central role as the most reliable gate stack system.

Planar MOSFET requires high-channel doping to control short-channel effects, the trade-offs are mobility degradation and increased leakage power consumption. Using doping to control threshold voltage in scaled device also causes increasing variation of the threshold voltage, posing difficulty in circuit design while scaling the supply voltage. New device architecture such as ultra-thin body, FD-SOI, and multiple-gate MOSFETs (e.g., finFETs) are expected. A particularly challenging issue is the control of the thickness, including its variability, of these ultra-thin MOSFETs. The solutions for these issues should be pursued concurrently with circuit design and system architecture improvements.

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MEMORY DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FRONT-END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

The continued research and development efforts in the industry have brought about reacceleration and diversification of scaling. The baseline memories now includes both stand-alone and embedded DRAM, SRAM, and both NAND and NOR Flash. The new prototype memories table includes silicon/oxide/nitride/oxide/silicon (SONOS), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase-change memory (PCM).

The challenges for DRAM devices are adequate storage capacitance with reduced feature size, high-κ dielectrics implementation, low leakage access device design, and low sheet resistance materials for bit and word lines. For stand-alone DRAM, high-κ materials are currently being used in an SIS structure for trench capacitors. Metal top electrode will be needed by 2007 and a full MIM structure with high-κ dielectric may be needed by 2009, when a dielectric constant greater than 60 is required for beyond 50 nm. Embedded DRAM in SOC applications will drive additional integration challenges. One such key challenge is the matching between the ground rules required for the deep contacts around the stacked capacitor with the contact ground rules for the logic devices.

The need for advanced capacitor materials in trench DRAM are postponed relatively to the stacked capacitor by a few years; however the cell size factor for stack capacitor DRAM is 6, while that for the trench DRAM remains at 8. Novel cell concepts for the trench capacitor, depending upon the replacement of the conventional planar transfer device by 3D array transistor structures, are envisaged for 65 nm in order to alleviate device scaling issues.

The rapid expansion of the market for Flash memories brings more focus on the material and process challenges for these devices. With this acceleration, Flash memory is becoming a new technology driver for both critical dimension scaling and material technology. The effective dimension, F, of Flash NAND device now appears to lead the DRAM half pitch.

The key challenges in Flash memory device are non-scalability of tunnel dielectrics, non-scalability of interpoly dielectrics, dielectric material properties, and dimensional control. In Flash memory devices, continuous scaling and the reduction in write voltage requires the use of a thinner inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. It is no longer feasible for the control gate poly Si to overlap the sides of the floating gate as the space between adjacent poly Si gates shrink. Thus, by 2010 high-κ interlayer dielectrics will be required to maintain an acceptable coupling ratio. Flash memory challenges also include the inception into mainstream manufacturing and the scaling of new memory types and storage concepts such as MRAM, phase-change memory, and FeRAM, for example. MRAM scalability of cell-size and write-power reduction needs solutions as early as 2008. FeRAM critical issues relate to cell endurance, scalability of power supply and cell-size.

HIGH-PERFORMANCE, LOW-COST RF AND ANALOG/MIXED-SIGNAL SOLUTIONS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS]

Fundamental changes in materials and device structures will be required to sustain continued performance, power management, and density improvements. The introduction of new materials such as high-permittivity (high-κ) gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes poses clear challenges to attain equivalent levels of threshold voltage, current mismatch, and for 1/f noise. The electrical characteristics of non-classical CMOS, such as dual-gate, fully depleted SOI devices, are fundamentally different from that of conventional CMOS. Thus, the fabrication of conventional precision analog/RF driver devices, resistors, and varactors may require separate process steps with the attendant increase in die cost. Furthermore, the steady reduction in analog supply voltage poses a significant circuit design challenge.

Signal isolation, especially between the digital and analog regions of the chip, is another important challenge for scaled technologies and for increased integration complexity. Noise coupling may occur through the power supply, ground, and shared substrate. The difficulty of integrating analog and high-performance digital functions on a chip increases with scaling in both device geometry and supply voltage. Signal isolation is critical for success in co-integrating high-performance analog circuits and highly complex digital signal processing (DSP) functions on the same die or substrate. Such co-integration is required in many modern communication systems to reduce size, power, and cost.

NEW GATE STACK PROCESSES AND MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND FRONT END PROCESSES]

Reduction of the equivalent gate oxide thickness has emerged as the most difficult challenge associated with the future device scaling. Higher dielectric constant (high-κ) and metal gate electrode will be required beginning in ~2008. Timely implementation will involve dealing with numerous challenging issues, including appropriate tuning of metal gate work

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function, ensuring adequate channel mobility, and gate stack integrity. High-κ scalability in integrated devices below 5 angstroms also remains a critical challenge due to interfacial layer control and availability of higher-κ materials. Impact on mobility and gate dielectric leakage are key issues to be addressed in this highly scaled EOT regime. Furthermore, reliability requirements for high-κ, including dielectric breakdown characteristics (hard and soft breakdown), transistor instability (charge trapping, work function stability, metal ion drift, or diffusion), etc., must be resolved.

Continued DRAM scaling requires construction of memory capacitors in ever-smaller cell area, while maintaining the memory capacitance of 25–35 fF to ensure reliability of stored data. This has resulted in the introduction of dielectric materials with a high dielectric constant (high-κ), such as aluminum oxide, aluminates (for example, HfAlOx) and tantalum oxide, along with a 3D memory structure. Capacitor dielectric thickness scalability for stacked DRAM and trench DRAM need resolution by year 2010 and 2014, respectively. The aspect ratio of stacked DRAM structures also needs resolution by year 2010.

In Flash memory devices, on the other hand, continuous scaling and the reduction in write voltage requires the use of a thinner inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. This difficult trade-off problem hinders scaling, suggesting the need to introduce high-κ material and 3D structure devices into Flash memory processing. Along with scaling issue of ferroelectric material in FeRAM, new process integration and 3D capacitors will continue to pose major challenges in the development of memory applications.

32 AND 22 NM HALF PITCH [LITHOGRAPHY]

32 nm half pitch is a crucial turning point for lithography imaging scheme. The 193 nm water immersion process is limited with NA to resolve this pitch, unless tight pitches are split into larger ones by double pattering or exposure; however the lithography cost will almost double. Single exposure requires higher-index immersion fluid and lens material. These technologies are still in development. Similarly, high-power sources, fast resists, masks, and related infrastructures are under development for EUV lithography, which also can use single exposures. Multiple-e-beam maskless lithography, which has the potential to bypass mask difficulties and provide manufacturing flexibility, is in an early-stage of development. Timing, cost, defects, critical dimension uniformity (CDU), overlay accuracy, and resists are other increasing issues.

For 22 nm half-pitch lithography, water-immersion 193 nm scanners and double patterning will be severely stretched with extremely large mask error factor, wafer line edge roughness, and design rule restrictions. High-index fluid and lens material will relieve these just a little, if they become available in time. The numerical aperture of EUV systems will have to be raised to more than 0.35 to have the k_1 factor comparable to NA 0.25 for 32 nm half pitch. There is a likelihood of increasing the number of mirrors in the imaging lens, thus leading to requirement of even higher power source while limiting throughput loss, thus less favorable economy. Multiple-e-beam maskless lithography will be better developed by that time but it has to support a high writing rate or more parallelism to maintain the increased pixel count within the same field size. If the potential is realized to keep the per-pass exposure and processing cost as well as the footprint similar to that of mask-based exposure tools, then it will be the most economical and sought-after solution for logic and memory applications.

MASKS [LITHOGRAPHY]

The mask technology is becoming very expensive and challenging. Mask cost has escalated each generation. Increased resolution plus larger mask error enhancement factor (MEEF), due to higher levels of reticle enhancement technology (RET), make the mask CDU and placement accuracy difficult to meet. Mask feature sizes becoming sub-resolution coupled with finite absorber thickness and polarized illumination worsen the problem. Extreme ultraviolet (EUV) masks have further stringent requirements of defect-free ultra-flat substrate and exposure without a pellicle. Inspecting advanced masks is expensive and time consuming. The inspection resolution is reaching limits with practical inspection wavelengths.

RESISTS [LITHOGRAPHY]

Line edge roughness (LER) of photoresist has substantially sustained the same absolute value and therefore has attained an even larger percentage of CD. As pattern geometry shrinks, shot noise starts to become an issue. Resist collapse after development limits its height-to-width aspect ratio to between 2.5 and 3, thus reducing the absolute resist thickness at each technology generation advancement. With immersion lithography, resist material development has to ensure low resist-induced defectivity, further restricting material choices.

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CD AND L_{EFF} CONTROL [FRONT END PROCESSES, LITHOGRAPHY AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

With the aggressive scaling of gate length, control of CD has been one of the most difficult issues in lithography and etching. In particular, resist slimming and profile-control of the sidewall, which are commonly utilized to minimize the dimension of effective gate length (L_{eff}), have made CD control far more difficult. Although the acceptable 3-sigma variation of the gate length is shared by lithography and etching at an optimum ratio, the tolerances in both technologies are approaching their limits. In addition, it is becoming very difficult to suppress LER, which depends on gate material, photoresist type, and etch chemistry, even by the optimum control of resist printing and etching. CD control and LER measurement also pose challenges to metrology in terms of accuracy and efficiency. Since off-current between source and drain may be affected by the LER, targets for controlling LER should be set with understanding the impact of LER on device performance. Moreover, the introduction of new gate materials and non-planar transistor structure requires many more challenges in selective etch processes, and improved anisotropy with the controlled sidewall features.

With the aggressive scaling of gate length, control of CD in lithography and etching continues to be a critical bottleneck. In particular, 1) resist slimming 2) gate pitch scaling 3) annealing uniformity, 4) offset spacers, and 5) new gate stack material (metal/high-κ) have made CD and effective gate length control more difficult. Controls of self-aligned doping profile in tight poly pitch and thermal activation uniformity (pattern/layout dependencies) are critical to achieve well-controlled L_{eff}. Gate patterning (lithography and etch) to attain 3-sigma variation of the physical gate below 12% may require the inception of restrictive design rules posing corresponding constraints and challenges to strain engineering and design. Furthermore suppression of LER, critical to minimize device variability, challenges gate materials and integration schemes, as well as etch chemistry processes. Moreover, the introduction of multiple gate and non-planar transistor structure requires many more challenges in selective etch processes, and improved anisotropy, and is limited with the controlled sidewall features.

INTRODUCTION OF NEW MATERIALS TO MEET HIGH CONDUCTIVITY AND LOW DIELECTRIC PERMITTIVITY REQUIREMENTS [INTERCONNECT]

To minimize signal propagation delay and power consumption, the industry has introduced high-conductivity metal and low-permittivity dielectric through damascene processes at 130 nm. The continued scaled-down interconnect poses increasing challenges to technology development and manufacturing. To meet the acceleration of MPU product introduction to a two and a half-year cycle for the next two technology generations (2007 and 2009, and then revision to a three-year cycle after 2009), the fast introduction of new metal/dielectric systems becomes critical. Today, the metal challenges include the fast rising resistivity of narrow Cu wires due to electron scattering at the Cu/barrier metal or dielectric interfaces and the grain boundary. In addition, a very thin and conformal low-resistivity barrier metal is required to integrate with Cu to achieve low resistivity and good reliability. For low-κ dielectrics, good mechanical, chemical, thermal, and physical properties are needed for manufacturable integration with other processes that may induce damage, in particular dry and wet etching, ashing, sputtering, and polishing. Furthermore, low-κ material must have sufficient mechanical strength to survive dicing, packaging, and assembling.

ENGINEERING MANUFACTURABLE INTERCONNECT [INTERCONNECT]

The integration of conductive and low-κ material must meet material, geometrical, planarity, and electrical requirements. Defect, variability, and cost must be engineered to ensure a manufacturable process. The advancement of interconnect should address performance, power, and reliability issues for traditional scaling or equivalent scaling with functional diversity. Since material solutions with traditional scaling cannot deliver performance, new technology has been proposed in recent years including 3D (including tight pitch through silicon vias (TSV)) or air gap structures, different signaling methods, novel design and package options, emerging interconnect using different physics and radical solutions, etc. The realization of these innovative technologies challenges new material systems, process integration, CMOS compatibility, metrology, predictive modeling, and optimization tools for interconnect/packaging architecture design.

POWER MANAGEMENT [DESIGN]

Cost-effective heat removal from packaged chips remains almost flat in the foreseeable future. In addition with the 2× increase in transistor count per generation, power management is now the primary issue across most application segments. Power management challenges need to be addressed across multiple levels, especially system, design, and process technology. Circuit techniques to contain system active and leakage power include multiple V_{dd} domains, clock distribution optimization, frequency stepping, interconnect architectures, multiple V_t devices, well biasing, block shutdowns among others. The implementation challenges of these approaches expand upwards into system design requirements, the continuous improvements in CAD design tools for power optimization (including design robustness against process variability), and downwards into leakage and performance requirements of new device architectures.

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CIRCUIT ELEMENT AND SYSTEM MODELING FOR HIGH FREQUENCY (UP TO 160 GHZ) APPLICATIONS

Accurate and efficient compact modeling of non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling will be of prime importance. Computer-efficient inclusion of statistics (including correlations) before process freeze into circuit modeling is necessary, treating local and global variations consistently. To support concurrent optimization of devices and circuits, efficient building block/circuit-level assessment using process/device/circuit simulation must be supported. Compact models are needed for III-V-, CMOS- and HV- devices. Compact scalable models for passive devices are needed for varactors, inductors, high-density capacitors, transformers, and transmission lines. The parameter extraction for RF compact models preferably tries to minimize RF measurements. Parameters should be extracted from standard I-V and C-V measurements with supporting simulations, if needed. Extreme RF applications like 77 GHz car radar approach the 100 GHz range. Third harmonic distortion for 40 GHz applications implies modeling of harmonics up to 120 GHz. Modeling of effects that have a more global influence gains in importance. Examples are cross talk, substrate return path, substrate coupling, EM radiation, and heating. CAD-tools must be further enhanced to support heterogeneous integration (SoC+SiP) by simulating mutual interactions of building blocks, interconnect, dies and package dealing with possibly different technologies while covering and combining different modeling and simulation levels as well as different simulation domains.

FRONT-END PROCESS MODELING FOR NANOMETER STRUCTURES [MODELING AND SIMULATION]

This is the key challenge for the prediction of result from device fabrication. It overlaps to some extent with the challenge "Ultimate nanoscale CMOS simulation capability", which also includes materials and device simulation. Most important and challenging in the area of front-end process modeling is the modeling of ultra-shallow junction formation, which starts from very low energy implant and especially focuses on the thermal annealing and diffusion of dopants. As an alternative the formation of doped epitaxial layers must be simulated, including their shape and morphology, defect status, and stress. Due to the strongly reduced thermal budgets needed for shallow junctions, that process is highly transient and is governed by the diffusion and reaction of dopant atoms and defects, and especially by the dynamics of clusters of these two. Implantation damage, amorphization, re-crystallisation, and silicidation must be accurately simulated. Anisotropy in models and parameters potentially introduced by thin layers must be investigated. In view of the need to increase carrier mobilities in the channel, the modeling of stress and strain and their influence on diffusion and activation has become vital, especially for strained silicon, SiGe, and for SOI structures. Moreover, stress history and memorization during process sequences is important and must be simulated. Model development, calibration, and evaluation as well as process characterization require numerous experimental activities and large progress in the metrology for dopants, defects, and stress, especially regarding two- and three-dimensional measurements. To enable efficient and accurate three-dimensional simulation, meshing for moving boundaries needs to be strongly enhanced. This challenge is being addressed below in the subchapter on Front-End Process Modeling.

COST-EFFECTIVE MANUFACTURING

DESIGN PRODUCTIVITY AND DESIGN FOR MANUFACTURING [DESIGN]

The number of available transistors double every technology cycle, increasing design complexity as well. In order to maintain design quality even after process technologies advance, design implementation productivity must be improved to the same degree as design complexity is scaled. Improving design productivity and IP reuse are key considerations for this issue. Challenges at high-level abstraction, platform-based design, multiprocessor programmability, design verification, analog and mixed-signal circuit synthesis are critical to secure design productivity scaling at a pace consistent with process technology cycles. Cost-effective product manufacturing also requires continuous improvements in the area of design for manufacturability, specifically areas such as design for minimization of performance/power sensitivity to device variability and layout styles, lithography-friendly designs, and design for testability and reliability.

TEST COMPLEXITY [TEST AND TEST EQUIPMENT]

Several device trends present great challenges to test. Increasing device in/out (IO) bandwidth requirements are rapidly driving the proliferation of faster and wider high-speed interfaces challenging test socket controlled impedance contact limits. Increasing integration of previously disparate semiconductor technologies in SOC or SiP present test challenges in management of per core design for test (DFT), test standardization of SOC core "wrappers" and SiP for example. Emerging technologies such as RF, analog, optical and microelectromechanical systems (MEMs) present some unique test challenges and will require significant improvements in test methods as they become more pervasive or integrated with digital CMOS technologies. Several device architecture trends such as more sophisticated power management or self-repair mechanisms could lead to departure from the longstanding deterministic stored stimulus and response test models and adding higher order dimensionality of test conditions (for example, adding multi-power, multi-voltage, multi-frequency topologies as opposed to single-valued temperature, voltage, and frequency). Test for yield learning is already

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critical and is expected to become more so with the introduction of new semiconductor processes and device structures and architectures. Testing for local non-uniformities and detecting symptoms and effects of line width variations, finate dopant distributions, and systematic process defects, are also key challenges to test complexity.

CONTINUED ECONOMIC SCALING OF TEST [TEST AND TEST EQUIPMENT]

The ever-improving economies of scale predicted by Moore's Law may not translate to test naturally. Design for test innovations, widespread use of structural test techniques such as scan testing, and the enabling of higher levels of test parallelism have been very successful in keeping test costs in check to date. However, new test requirements for increasingly complex devices, testing for yield learning, increasing quality requirements, and practical limits on parallel testing continue to present great challenges to test cost. In particular, test tooling cost including probe cards are not scaling and threaten to dominate the total test cost if present trends continue. Accelerating the test learning curve for new device architectures or integration schemes is critical to maintain test cost scaling curve in sync with overall technology cost-scaling goals. Product cost optimization should strike a balance between design, manufacturing, yield learning, and test while securing overall quality of shipped products. Automation of generation entire test programs for automatic test equipment (ATE), convergence of test and system reliability solutions, integration of simulation and modeling of test interfaces hardware and instrumentation into the device design process are challenging opportunities for test cost scaling reduction.

RESPONDING TO RAPIDLY CHANGING COMPLEX BUSINESS REQUIREMENTS [FACTORY INTEGRATION]

Wide ranging business models beyond the integrated device manufacturer (IDM) such as the fabless and foundry model, joint venture, and the variety of task sharing and out-sourcing scenarios have become pervasive in response to customers' rapidly changing complex business requirements. Furthermore, diversified customers' requirement on SoC devices have placed strong demand on manufacturing environments to rapidly and efficiently adapt to high-mix and low-volume product runs. These requirements pose critical near-term challenges in several areas such as integration of larger numbers and different types of equipment, software applications, and fully featured software systems to manage the factory complexity while enabling decreasing time to ramp high volume production.

Development of information exchange/control platform covering all the relevant operation fields, extending from design, mask, front-end-of-line (FEOL), and back-end-of-line (BEOL) to testing, packaging, etc., is also a crucial challenge. Continuous improvements to model factory capacity and performance to optimize output, improve cycle time, and reduce cost are key to successful high-mix factory operations.

IMPROVEMENT IN TRADE-OFF BETWEEN MANUFACTURING COST AND CYCLE TIME [FACTORY INTEGRATION]

Enhanced tool availability, improvements in material handling automation and systems for operational flexibility and control; single-wafer manufacturing; and the reduction/elimination of non product wafers (NPW); are representative areas for continuous improvement in 300 mm lines to meet the challenges of cycle time and cost reduction. The transition from 300 mm to the next wafer size (i.e., 450 mm) is another critical challenge for the semiconductor industry in the 2012–2016 time frame. This transition is considered critical to simultaneously meet the 30% cost/die reduction and a 50% improvement in cycle time.

MEET THE CHANGING COST AND PERFORMANCE REQUIREMENT OF THE MARKET [ASSEMBLY AND PACKAGING]

Many new materials will be introduced in IC packages in the next few years in order to meet requirements of environmental regulations; to improve package performance; and to be compatible with low-κ dielectrics used in Cu interconnects with 45 nm half pitch and beyond. Nano-materials present significant opportunities for the packaging community. The ICs front-end progress is based upon a high level of investment in material and process technology and equipment. There is no corresponding investment in the back-end for materials, process, and equipment. Low-cost opportunities for flip-chip to meet mobile application requirements are challenging and essential, likely requiring new combinations of process and materials. 3D integration (including low-density TVS and via-fill process TVS) and wafer-level packaging, have promises of dramatic cost performance and form factor improvement. The industry will require investment and knowledge of infrastructure to perfect these technologies for high-volume production. The changing marketplace by consumerization of electronic products presents the tremendous opportunity for the packaging industry in implementing 3D integration technologies to fill the gap created by physical limit of Moore's law scaling. Thermal management, thin die handling, signal integrity, and test (as well as environmental issues) are near-term critical challenges for SiP.

SOLUTIONS FOR INTEGRATION OF OFF-CHIP COMPONENTS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS, ASSEMBLY AND PACKAGING]

System-in-package solutions have been developed to meet different applications and system requirements especially in the rapidly changing and increasing market of portable wireless communication devices. The integration of these SiP solutions to construct a universal design platform is increasingly important. High Q RF devices by MEMS or other processes are usually off-chip and need to be made as integrated passive devices (IPD). Three-dimensional stacking and embedded components are two major methodologies to address off-chip components. Forming passive component (as opposed to inserting discrete components) into substrates often involves additional materials such as high-κ dielectric for capacitors, resistive films or paste for resistors, and high permeability (μ) material for inductors. Devising process simplification for this variety of embedded passives is a key challenge to enable a cost-effective alternative. Testing and tuning also pose significant challenges, especially after packaging or assembly processes. Accurate models that include process tolerances as well as circuit and tester parasitic elements are needed for designers to simulate circuit performance with embedded passives before the manufacturing process. Lack of CAD tools for embedded passives also needs to be resolved.

CHEMICAL AND MATERIAL ASSESSMENTS [ESH]

The rapid introduction of new chemicals, materials, and processes requires new rapid assessment methodologies to ensure that new chemicals and materials can be utilized in manufacturing without inducing new hazardous impacts on human health, safety, and the environment. Although methodologies are needed to meet the evaluation and quantification demands for ESH impacts, the focus is currently on expediting process implementation. As such, near-term challenges should include the reduction of emissions from processes using global warming potential (GWP) chemicals.

RESOURCE CONSERVATION [ESH]

As the industry grows and its technology advances toward finer patterning and larger wafer sizes, the natural tendency is toward increased use of water, energy, chemicals, and materials. Resource conservation is becoming a major concern with respect to availability, cost reduction, manufacturing location, sustainability, and waste disposal. Thus, it is necessary to develop diverse process equipment capable of utilizing resources efficiently. Continuous improvement is needed in chemicals and materials utilization and energy consumption reduction in facilities and processing equipment, as well as in efficient thermal management of clean rooms.

DETECTION OF MULTIPLE KILLER DEFECTS AND SIGNAL-TO-NOISE RATIO [YIELD ENHANCEMENT]

Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes required by technology cycles. Inspection sensitivity can be increased to address defect size trends; however challenges arise in terms of efficiently and cost-effectively differentiating defects of interest (DOI) from a vast amount of nuisance and false defects. Reduction of background noise from detection units and samples are key challenges to enhance signal to noise ratio for defect delineation.

LAYOUT STYLE AND SYSTEMATIC YIELD LOSS: HIGH THROUGHPUT LOGIC DIAGNOSIS CAPABILITY [YIELD ENHANCEMENT]

The irregularity of features makes logic areas very sensitive to systematic yield loss mechanisms such as patterning marginalities across the lithographic process window. Solutions exist but need continuous improvements. Before reaching random-defect limited yields, the systematic yield loss mechanisms should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different automatic test pattern generation (ATPG) flows accommodation; ATE architecture that lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die.

WAFER EDGE AND BEVEL CONTROL AND INSPECTION [YIELD ENHANCEMENT]

Defects and process problems around wafer edge and wafer bevel are known to cause yield problems. Development and continuous improvement in terms of defect detection, throughput, and cost of ownership (CoO) of wafer edge and bevel defect inspection tools are increasingly critical to yield enhancement in advance device technologies.

FACTORY-LEVEL AND COMPANY-WIDE METROLOGY INTEGRATION [METROLOGY]

Metrology areas should be carefully chosen and sampling must be statistically optimized for process control based on cost of ownership (CoO). *In situ* and inline metrology has become requisite for both tight process control and throughput. Information from all metrology (i.e., online and offline), associated with advanced process control (APC), fault detection and classification (FDC), and other systems should be integrated into an efficient database for determining process control

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parameters and key correlations to drive yield enhancement. Such efficient and seamless integration requires that standards for process controllers and interfaces, data management and the database structure be established. Continuous improvement of sensors, including calibration, sensing method, and data processing is clearly expected. Development of new sensors must also be concurrently done with the development of advanced process modules.

MEASUREMENT OF COMPLEX MATERIAL STACKS, INTERFACIAL PROPERTIES, AND STRUCTURES [METROLOGY]

Metal-gate high-κ gate stacks, advanced strain and mobility enhancement techniques, as well as advanced interconnect and low-κ dielectric structures require novel or continuous improvement of measurement methodologies and standards in terms of critical dimensions, and physical and electrical properties including interface characteristics. Metrology of film stacks for both front-end and back-end generally provide average physical or electrical property behavior from large area test structures. Therefore, new metrology techniques capable of characterizing stack structures at near nominal dimensions are also needed in the near term. These techniques should be compatible with bulk or SOI substrates. Critical dimension metrology including line edge roughness plays an increasing critical role in process control and variability reduction efforts.

FRONT END PROCESS METROLOGY [METROLOGY]

The device community has shown that CMOS-like transistors, which are referred to as non-classical CMOS, are likely to be the switching device that will be manufactured over the next fifteen years. The process and device design architecture dictate the final selection of metrology requirements. Metrology development is challenged to meet the requirements posed by the accelerated introduction of new technology generations. This requires accelerated advancement of metrology for transistor development and fabrication. Process integration issues such as variability, the need to control leakage current, and the reduction in threshold voltage and gate delay and their tolerances will interact with the reality of process control ranges for gate dielectric thickness doping profiles, junctions, and doses to device metrology needs. Modeling studies of manufacturing tolerances continue to be a critical tool for transistor metrology strategy. CD control and LER measurement also pose challenges to metrology in terms of accuracy and efficiency. Since off-current between source and drain may be affected by the LER, targets for controlling LER should be set with understanding the impact of LER on device performance.

CRITICAL METROLOGY CONSIDERATION—PRECISION AND UNCERTAINTY [METROLOGY]

When comparing measurements with numbers in the roadmap, there are several important considerations. The validity of the comparison is strongly dependent upon how well those comparisons are made. The conventional interpretation of the ITRS precision has been in terms of the single tool reproducibility. The term "precision" is best understood in broader terms as *uncertainty*. Measurement error is a complex function of time (reproducibility), tool (tool-to-tool matching) and sample (sample-to-sample bias variation). The measurement uncertainty is thus defined by the total bias variation with measurement-to-measurement, tool-to-tool and sample-to-sample components. These components may be of varying importance depending on the instrument and the application.

LITHOGRAPHY METROLOGY [METROLOGY]

Lithography metrology continues to be challenged by rapid advancement of patterning technology. A proper control of the variation in transistor gate length starts with mask metrology. Indeed, larger values for mask error factor (MEF) might require a tighter process control at mask level, too; hence, a more accurate and precise metrology has to be developed. Mask metrology includes measurements that determine that the phase of the light correctly prints. Both on-wafer measurement of critical dimension and overlay are also becoming more challenging. The metrology needs for process control and product disposition continue to drive improvements in precision, relative accuracy, and matching. Acceleration of research and development activities for CD and overlay are essential if to provide viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability which is another important metrology challenge.

IN THE LONG TERM (~2016 THROUGH 2022)

ENHANCING PERFORMANCE

MANAGEMENT OF LEAKAGE POWER CONSUMPTION [DESIGN]

While power consumption is an urgent challenge, its leakage or static component will become a major industry crisis in the long term, threatening the survival of CMOS technology itself, just as bipolar technology was threatened and eventually disposed of decades ago. Leakage power varies exponentially with key process parameters such as gate length, oxide thickness and threshold voltage; this presents severe challenges in light of both technology scaling and variability.

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Off-currents in low-power devices increase by a factor of 10 per generation, with emphasis on a combination of drain and gate leakage components. Therefore design technology must be the key contributor to maintain constant or at least manageable static power.

IMPLEMENTATION OF ADVANCED, NON-CLASSICAL CMOS DEVICE WITH ENHANCED DRIVE CURRENT [PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

To continue MOSFET scaling to less than $L_g = 9$ nm, it is quite likely that the device structure will change to advanced non-classical CMOS such as multiple-gate. In these devices, various "technology boosters," such as mobility enhancement by strained Si, elevated source source/drain, high-κ gate dielectric, and metal gate electrode, will likely be simultaneously implemented with the new device structure. Toward the end of the Roadmap timeframe, devices will increasingly be operated in the quasi-ballistic mode, where the current gain will be enhanced by parameters different from those currently known. Eventually, nanowires, carbon nanotubes, and other high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed. Choice of the optimum device structures, their physical characterization, and construction of cost-effective processing flows will become very important along with construction of their circuit architecture.

SCALING OF MOSFET [FRONT END PROCESSES]

Continued CMOS scaling trend forecasts the introduction of new materials and new device structures in conjunction with booster technologies such as strain, hybrid-orientation-technique. Non-classical CMOS structure (multi-gate) must be prepared together with advanced FEP processes such as gate stack, junction and silicide. High-κ dielectric EOT must be continuously scaled below 1.0 nm for metal gates while maintaining high reliability with an acceptable leakage current. Both low sheet resistance and process productivity must be retained, while junction depth will be aggressively scaled. Parasitic resistance must be controlled by introducing a new silicide metal or a new structure such as a Schottky junction. Gate CD variation must be suppressed by process optimization of lithography, photoresist trim, and gate etch.

SHIFTING FROM TRADITIONAL SCALING TOWARD EQUIVALENT SCALING AND FUNCTIONAL DIVERSITY THROUGH UNCONVENTIONAL APPROACHES [INTERCONNECT]

Even with the projected improvements in materials and processes, traditional scaling alone is deemed to be insufficient to meet interconnect performance requirements in the long term. The challenge will be to achieve equivalent scaling by adopting nontraditional technologies as well as new design and architectures. Among the technologies nearing production, 3D integration by the use of TSVs would enable construction of highly complex systems without making global interconnects unduly long. Wireless signaling with passive devices might broaden design and integration options. Looking further into the future, innovative materials and/or wiring schemes, such as carbon nanotubes and/or optical wiring, could significantly raise the performance limits set by metal/dielectric interconnects. Also along the lines of departure from simple scaling, the possibility of adding functional diversity using novel interconnects needs to be explored. Possible technologies in this direction include, for example, embedded repeaters, variable-resistor vias, and integrated back-end memory. In implementing these new technologies, use of unconventional materials such as compound semiconductors should not be precluded. However, it is most desirable to realize functional integration by developing CMOS-compatible interconnect processes and the necessary metrology.

GATE CD CONTROL IMPROVEMENTS AND PROCESS CONTROL [LITHOGRAPHY]

With aggressive scaling of devices, the required gate CD control comes down to 0.92 nm in 3σ with a line width reduction (LWR) of less than 1.2 nm in 3σ in 2016 for every lithography potential solution. (Please note that Si-Si lattice distance is 0.235 nm.) Furthermore, resolution and precision measurements for CD down to 4.5 nm, including LWR metrology of 0.36 nm in 3σ is very challenging, along with the required overlay accuracy of 2.2 nm in 3σ or better in 2022. The maximum permissible defect size on patterned wafer is reduced to smaller than 6.6 nm in 2022. Without metrology and inspection tools having sufficient accuracy and resolution, CD control improvements and process control will be difficult to achieve.

NON-DESTRUCTIVE PRODUCTION MEASUREMENTS [METROLOGY]

Non-destructive (without charging or contaminating the surface) and high-resolution wafer/mask level microscopy for measuring the critical dimensions of 3D structures is required. The relationship between the physical object and the waveform analyzed by the instrument should be understood to improve CD measurement including physical feature measurement. Surface charging and contamination need to be improved as well as sensor and sensing method. New design of optics with aberration correction is required for high resolution and better throughput. Ion microscopy is also one of the candidate technologies to cope with this subject. The combination of high-resolution optics, waveform

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analysis, and non-charging technique enables precise grasp of 3D structures for CD measurement. At the same time, CD metrology tool must be calibrated by using standard reference material or structure for reliable and stable measurement.

CONTINUOUS CMOS SCALING, HETEROGENEOUS INTEGRATION, AND BEYOND CMOS [EMERGING RESEARCH DEVICES]

There are three technological approaches for continuous functional scaling of information processing technologies to the 16 nm generation and beyond. The continuous CMOS scaling is attained by developing new materials to replace silicon as an alternate channel to increase the saturation velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation. The heterogeneous integration is aiming at developing practice new device technologies and primitive-level architectures to provide special purpose optimized functional cores heterogeneously integrated with silicon CMOS. The "beyond CMOS" approach will invent and develop a new information processing technology eventually to replace CMOS.

CONTROL OF NANOSTRUCTURES AND PROPERTIES [EMERGING RESEARCH MATERIALS]

One of Emerging Research Materials's (ERM's) most difficult challenges is to deliver material options with controlled and desired properties. These material options must exhibit the potential to enable high density emerging research devices, lithographic technologies, and interconnect fabrication and operation at the nanometer scale. This challenge requires not only the control of nanostructure properties such as size, bandgap etc., but also placement of nanostructures, such as carbon nanotubes (CNTs), nanowires, or quantum dots, in precise locations for devices and interconnects. To improve the control of material properties for nanometer (nm) scale applications, collaboration and coordination within the research community are required.

COST-EFFECTIVE MANUFACTURING

TEST FOR YIELD LEARNING [TEST]

Test's peripheral role as a feedback loop for understanding underlying defect mechanisms, process marginalities, and as an enabler for rapid fabrication process yield learning and improvement has traditionally been considered a secondary role to screening hard defects. With the increasing reduction in feature (and defect) sizes well below optical wavelengths, rapidly increasing failure analysis throughput times, reduction in failure analysis efficacy, and approaching practical physical limits to other physical techniques (pica, laser probes), the industry is reaching a strategic inflection point for the semiconductor business where the criticality of DFT and test-enabled diagnostics and yield learning becomes paramount.

EMERGING NEW PACKAGING [ASSEMBLY AND PACKAGING]

In 2016 integrated circuits will see M1-half pitch of 23 nm in MPU/ASIC, core voltage of 0.5 V, and I/O frequency of 35 GHz for high performance applications. These device characteristics will rely on advanced packaging technology and new packaging materials for incorporation into electronic systems. Potential solutions for high heat generation and hot spot phenomena include advanced fluidic cooling systems and new generation of high thermal conductive materials such as carbon nanotubes based material. Broad band data transfer may require guided wave optical interconnects or some other high speed electrical interface built into the package. Organic or biological devices emerging in the market will require biological interfaces. From the system design view point, the integration of a wide variety of devices in SiP will require improved design tools and methodology to achieve optimal partitioning.

MEETING PROCESS REQUIREMENTS AT 32 NM AND BEYOND GENERATIONS RUNNING PRODUCTION VOLUMES [FACTORY INTEGRATION]

Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory continues to be a primary challenge. Small process windows and tight process targets at 32 nm generations in many modules force decision makings in process control increasingly complex and difficult that will have a large impact to the factory information and control system. Especially quality tracking and control in even higher mix with smaller lot size operations will become one of the primary production efficiency limiters.

MODELING OF CHEMICAL, THERMOMECHANICAL, AND ELECTRICAL PROPERTIES OF NEW MATERIALS [MODELING AND SIMULATION]

Increasingly new materials need to be introduced in technology development due to physical limits that otherwise would prevent further scaling. This introduction is required especially for gate stacks, interconnect structures, and photoresists, and furthermore for Emerging Research Devices. In consequence, equipment, process, device, and circuit models must be extended to include these new materials. Furthermore, computational material science needs to be developed and applied to contribute to the assessment and selection of new materials in order to reduce the experimental effort, and to contribute to the databases required for semi-empirical calculations.

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DEVELOPMENT OF MODEL-BASED DESIGN-MANUFACTURING INTERFACE [YIELD ENHANCEMENT]

In the future it will be necessary to develop model-based design-manufacturing interfaces. Due to optical proximity correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc. It will be necessary to develop test structures that address complex integration issues of new technology generations. Statistical methodology should also be incorporated with the interface to cope with ever increasing transistor counts.

CHEMICAL AND FACILITY MANAGEMENT BY ESH DESIGN AND MEASUREMENT METHODS [ESH]

Equipment design engineers and equipment users require timely information regarding ESH characteristics of potential new process chemicals and materials and method. This information is essential to the proper selection of optimal chemicals and materials and methods for minimization of ESH impact. Chemical data availability and chemical assessment is essential to the proper evaluation for new process. And the conservation of facilities energy and water and material is essential to the minimization of global environmental impact. To minimize the ESH impact without delaying process implementation, integrated ESH design and measurement and evaluation methods needs to be developed.

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WHAT IS NEW FOR 2007— THE WORKING GROUP SUMMARIES

SYSTEM DRIVERS

WHAT'S NEW?

The 2007 System Drivers Chapter continues to evolve to include market-driven drivers that reflect the demands of a 21st-century roadmap. These driver segments include the following:

- *Networking*: NEW for 2007, this driver represents the class of chips that are used in high bandwidth communications applications. Power efficiency and multi-core design are increasingly used in this application.
- *Consumer stationary driver*: Introduced in the 2006 update, this driver represents a high-performance version of the increasingly important consumer electronics market.
- *Consumer mobile driver*: Existing since the 2005 version, this driver represents a huge class of chips that rely on extremely power efficient techniques for battery-powered devices.
- *Office / MPU*: An "old" existing driver, it has been updated in its modeling of clock frequency growth and growth in the number of cores on chip to reflect current realities in power-limited microprocessor design.
- *Other* existing drivers have been reviewed to ensure the direction is appropriate.
- *Additional* drivers are being examined for inclusion in future roadmaps, including medical and automotive drivers.

A complete set of market-driven drivers is thus being formed for the System Drivers roadmap, to fully align the ITRS with other chapters; the electronic industry, and with other system-level roadmaps such as iNEMI.

An analysis of "More than Moore" aspects has also been pursued, focusing on the consumer portable driver and compared with "*emulators"* in the iNEMI system level roadmap. The long-term goal is to match system-level and chip-level requirements on a driver basis. This analysis is shown in the chapter as well.

Table ITWG1 Major Product Market Segments and Impact on System Drivers

Market Drivers	*SOC*	*Analog/MS*	*MPU*
I. Portable/consumer			
1. Size/weight ratio: peak in 2004 2. Battery life: peak in 2004 3. Function: 2×/2 years 4. Time-to-market: ASAP	Low power paramount Need SOC integration (DSP, MPU, I/O cores, etc.)	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
II. Medical			
1. Cost: slight downward pressure (~1/2 every 5 years) 2. Time-to-market: >12 months 3. Function: new on-chip functions 4. Form factor often not important 5. Durability/safety 6. Conservation/ ecology	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SOC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
III. Networking and communications			
1. Bandwidth: 4×/3–4 years 2. Reliability 3. Time-to-market: ASAP 4. Power: W/m^3 of system	Large gate counts High reliability More reprogrammability to accommodate custom functions	Migrating on-chip for MUX/DEMUX circuitry MEMS for optical switching.	MPU cores, FPGA cores and some specialized functions

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IV. Defense			
1. Cost: not prime concern 2. Time-to-market: >12 months 3. Function: mostly on SW to ride technology curve 4. Form factor may be important 5. High durability/safety	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
V. Office			
1. Speed: 2×/2 years 2. Memory density: 2×/2 years 3. Power: flat to decreasing, driven by cost and W/m^3 4. Form factor: shrinking size 5. Reliability	Large gate counts; high speed Drives demand for digital functionality Primarily SOC integration of custom off-the-shelf MPU and I/O cores	Minimal on-chip analog; simple A/D and D/A Video i/f for automated camera monitoring, video conferencing Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-position resolution	MPU cores and some specialized functions Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
VI. Automotive			
1. Functionality 2. Ruggedness (external environment, noise) 3. Reliability and safety 4. Cost	Mainly entertainment systems Mainly ASSP, but increasing SOC for high end using standard HW platforms with RTOS kernel, embedded software	Cost-driven on-chip A/D and D/A for sensor and actuators Signal processing shifting to DSP for voice, visual Physical measurement ("communicating sensors" for proximity, motion, positioning); MEMS for sensors	

A/D—analog to digital ASSP—application-specific standard product D/A—digital to analog DEMUX—demultiplexer DSP—digital signal processing FPGA—field programmable gate array i/f—interface I/O—input/output HW—hardware MEMS—microelectromechanical systems MUX—multiplexer RTOS—real-time operating system

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DESIGN

WHAT'S NEW?

After going through a major revision in the 2005 edition, the 2006 design chapter update featured a full quantitative design technology roadmap. The 2007 Design chapter focuses on providing meaningful updates of some of the figures, dates, and challenges, including moderate revisions of the System-Level, Verification, DFM, and Logic/Circuit/Physical Design sections.

Most sections now include a table that relates challenges and solutions. Although a one-on-one relationship is usually not warranted, it is quite helpful in certain parts of the design flow. The 2008 version of this chapter will continue in this direction while increasingly accounting for alternative integration methods that add on to Moore's Law (heterogeneous systems, system-in-package (SIP), etc.).

Indeed, an "inventory" analysis of "More than Moore" design technology aspects has also been pursued, looking at the design technology solutions aligned with each design technology section (system level, logic/circuit/physical, verification, DFT, DFM). This analysis is shown in the chapter as well.

DIFFICULT CHALLENGES

While the 2007 Design chapter still lists five overall design technology challenges, design productivity, closely linked to system and design process complexity, and of course affecting design cost, is the most massive and critical challenge, both in the short and long term, and is affected by the other four challenges. The second through fifth challenges are narrower in scope, and mostly address silicon complexity issues. From those challenges, the most critical are power consumption and manufacturability:

- Power consumption is an urgent, short-term challenge, quickly shifting from a performance-driven active power crisis to a variability-driven leakage power crisis in the long term. Power consumption is classified as an "enhancing performance" type challenge in the ITRS Executive summary.
- Manufacturability, i.e., the ability to produce a chip in large quantities at acceptable cost and according to an economically feasible schedule, has been affecting the industry primarily due to lithography hardware limitations but will become a major crisis in the long term as variability in its multiple forms invades all aspects of a design. Manufacturability is classified as a "cost-effective manufacturing" type challenge in the ITRS Executive Summary.

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Table ITWG2 Overall Design Technology Challenges

Challenges ≥ 32 nm	*Summary of Issues*
Design productivity	System level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation Verification: executable specification, ESL formal verification, intelligent test bench, coverage-based verification Logic/circuit/layout: analog circuit synthesis, multi-objective optimization
Power consumption	Logic/circuit/layout: dynamic and static (leakage), system and circuit, power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Reliability	Logic/circuit/layout: MTTF-aware design, BISR, soft-error correction
Interference	Logic/circuit/layout: signal integrity analysis, EMI analysis, thermal analysis
Challenges <32 nm	*Summary of Issues*
Design productivity	Complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage Tools specific for SOI and non-static logic, and emerging devices Cost-driven design flow Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	SOI power management
Manufacturability	Uncontrollable threshold voltage variability Advanced analog/mixed signal DFT (digital, structural, radio), "statistical" and yield-improvement DFT Thermal BIST, system-level BIST
Reliability	Autonomic computing, robust design, SW reliability
Interference	Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.)

ATE—automatic test equipment BISR—built-in self repair BIST—built-in self test DFT—design for test
EMI—electromagnetic interference ESL—Electronic System-level Design HW/SW—hardware/software
MTTF—mean time to failure SOI—silicon on insulator

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TEST AND TEST EQUIPMENT

WHAT'S NEW?

The 2007 Test chapter was originally planned as a refinement of the 2005 Test chapter, but has evolved into including major changes. The 2005 chapter contained some overlapping information in various sections and every effort has been made in the 2007 chapter to eliminate overlap in sections. As an example, the SoC table was completely redefined to only refer to issues pertaining to testing integrations of cores. Core specific requirements are covered in the Logic, Memory, Mixed signal, etc, tables. This resulted in an increase of readability and usability of the SoC table and further drove the need for each of the core tables to be self contained. Consumer logic has been added to the 2007 Logic table whereas the 2005 Logic table focused on only high volume microprocessors and omitted consumer requirements.

In other changes for 2007, DRAM, Flash, and Embedded memory tables have now been combined into a single memory table and embedded SRAM, which was identified as a gap in the 2005 roadmap, and has been added for 2007. The DRAM portion of the memory table is based on a new model and shows significant increases in the I/O data rate over the 2005 information. I/O data rates on commodity DRAM devices will increase to over 8 Gb/s by 2022.

There are significant additions in 2007. RF and test socket tables have been added. The three handler tables of the 2005 roadmap for logic, communication devices, and memory have been combined into a single table, but divided into three areas based upon DUT power consumption. The prober table now represents the needs for all device types versus the logic only focus of the 2005 tables. A new section has been added for specialty devices such as LCD display drivers, imaging devices and other high-volume devices that are required for consumer and mobile applications but are not covered in the other sections. Specialty devices can drive requirement that are beyond the requirements specified in the other tables.

Finally, many table colors have been changed for 2007 based upon a new method of determining colors and table value entries. The value in the each of the table cells was determined by the requirements of the silicon manufacturers based upon the expected needs of the devices. The colors of the cell are the equipment supplier response to the stated need.

KEY TEST DRIVERS, DIFFICULT CHALLENGES, AND OPPORTUNITIES

Table ITWG3 Summary of Key Test Drivers, Challenges, and Opportunities

Key Drivers (not in any particular order)	
Device trends	Increasing device interface bandwidth (# of signals and data rates)
	Increasing device integration (SoC, SiP, MCP, 3D packaging)
	Integration of emerging and non-digital CMOS technologies
	Complex package electrical and mechanical characteristics
	Device characteristics beyond one sided stimulus/response model
	Multiple I/O types and power supplies on same device
	Multiple digital I/O types on same device
Increasing test process complexity	Device customization during the test process
	"Distributed test" to maintain cost scaling
	Feedback data for tuning manufacturing
	Dynamic test flows via "Adaptive Test"
	Higher order dimensionality of test conditions
Continued economic scaling of test	Physical limits of test parallelism
	Managing (logic) test data and feedback data volume
	Defining an effective limit for performance difference for HVM ATE versus DUT
	Managing interface hardware and (test) socket costs
	Trade-off between the cost of test and the cost of quality
	Multiple insertions due to system test and BIST
Difficult Challenges (in order of priority)	
Test for yield learning	Critically essential for fab process and device learning below optical device dimensions
Detecting Systemic Defects	Testing for local non-uniformities, not just hard defects
	Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects

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Screening for reliability	Implementation challenges and efficacies of burn-in, IDDQ, and Vstress
	Erratic, non deterministic, and intermittent device behavior
	Tester inaccuracies (timing, voltage, current, temperature control, etc)
	Over testing (e.g., delay faults on non-functional paths)
	Mechanical damage during the testing process
Potential yield losses	Defects in test-only circuitry or spec failures in a test mode e.g., BIST, power, noise
	Some IDDQ-only failures
	Faulty repairs of normally repairable circuits
	Decisions made on overly aggressive statistical post-processing
Future Opportunities (not in any order)	
Test program automation (not ATPG)	Automation of generation of entire test programs for ATE
Simulation and modeling	Seamless Integration of simulation and modeling of test interface hardware and instrumentation into the device design process
Convergence of test and system reliability solutions	Re-use and fungibility of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMs—micro-electromechanical systems

PROCESS INTEGRATION, DEVICES AND STRUCTURES

WHAT'S NEW?

The *Process Integration, Devices, and Structures (PIDS)* chapter addresses overall IC process flow integration, with the main IC devices and structures, and with the reliability trade-offs associated with new options. Physical and electrical requirements and characteristics are emphasized within PIDS, encompassing parameters such as physical dimensions, key device electrical parameters, including device electrical performance and leakage, and reliability criteria. The focus is on nominal targets, although statistical tolerances are discussed as well. Key technical challenges facing the industry in this area are addressed, and some of the best-known potential solutions to these challenges are discussed. The chapter is subdivided into the following major subsections: logic, memory (including both DRAM and non-volatile memory [NVM]), and reliability.

Key aims of the ITRS include both identifying key technical requirements and challenges critical to sustaining the historical scaling of CMOS technology per Moore's Law and stimulating the needed research and development to meet the key challenges. The objective of listing and discussing potential solutions in this chapter is to provide the best current guidance about approaches that address the key technical challenges. However, the potential solutions list is not comprehensive, nor are the solutions in the list necessarily the most optimal ones. Given these limitations, the potential solutions in the ITRS are meant to stimulate and not limit research exploring new and different approaches.

LOGIC

A major portion of semiconductor device production is devoted to digital logic. In this section, both high-performance and low-power logic (typically for mobile applications) are included, and detailed technology requirements and potential solutions are considered for both types. Key considerations are performance, power, and density requirements and goals. One key theme is continued scaling of the MOSFETs for leading-edge logic technology in order to maintain historical trends of improved device performance. This scaling is driving the industry toward a number of major technological innovations, including material and process changes such as high-κ gate dielectric, metal gate electrodes, etc., and in the long term, new structures such as ultra-thin body, multiple-gate MOSFETs (such as FinFETs). These innovations are expected to be introduced at a rapid pace, and hence understanding, modeling, and implementing them into manufacturing in a timely manner is expected to be a major issue for the industry

MEMORY

Logic and memory together form the predominant majority of semiconductor device production. The types of memory considered in this chapter are DRAM and non-volatile memory (NVM). The emphasis is on commodity, stand-alone chips, since those chips tend to drive the memory technology. However, embedded memory chips are expected to follow the same trends as the commodity memory chips, usually with some time lag. For both DRAM and NVM, detailed technology requirements and potential solutions are considered

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The NVM discussion in this chapter is limited to devices that can be written and read many times; hence read-only memory (ROM) and one-time-programmable (OTP) memory are excluded. The current mainstream types of NVM currently is Flash, both NAND and NOR. There are serious issues with scaling that are dealt with at some length in the chapter. Other, non-charge-storage types of NVM are also considered, include ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase change RAM. For DRAM type memory, the key issue is dealing with increasing scaling difficulties, especially with ensuring very low levels of leakage.

RELIABILITY

Reliability is a critical aspect of process integration. Emerging technology generations require the introduction of new materials and processes at a rate that exceeds current capabilities for gathering information and generating the required database and models on new failure regimes and defects. Because process integration must then be performed without the benefit of extended learning, it will be difficult to maintain current reliability levels. Uncertainties in reliability can also lead to unnecessary performance, cost, and time-to-market penalties. These issues place difficult challenges on testing and wafer level reliability (WLR). Packaging interface reliability is particularly vulnerable to reliability problems because of new materials and processes, form factors, tighter lead and bond spacing, severe environments, adhesion, and customer manufacturing capability issues.

DIFFICULT CHALLENGES

Table ITWG3 Process Integration Difficult Challenges—Near-term Years

Difficult Challenges ≥ 22 nm	*Summary of Issues*
1. Scaling of MOSFETs to the 22 nm technology generation	Scaling planar bulk CMOS will face significant challenges due to the high channel doping required, band-to-band tunneling across the junction and gate-induced drain leakage (GIDL), random doping variations, and difficulty in adequately controlling short channel effects. Also, keeping parasitics, such as series source/drain resistance with very shallow extensions and fringing capacitance, within tolerable limits will be significant issues. Implementation into manufacturing of new structures such as ultra-thin body fully depleted silicon-on-insulator (SOI) and multiple-gate (e.g., FinFET) MOSFETs is expected at some point. This implementation will be challenging, with numerous new and difficult issues. A particularly challenging issue is the control of the thickness and its variability for these ultra-thin MOSFETs, as well as control of parasitic series source/drain resistance for very thin regions.
2. With scaling, difficulties in inducing adequate strain for enhanced mobility.	With scaling, it is critically important to maintain (or even increase) the current significantly enhanced CMOS channel mobility attained by applying strain to the channel. However, the strain due to current process-induced strain techniques tends to decrease with scaling.
3. Timely assurance for the reliability of multiple and rapid material, process, and structural changes	Multiple major changes are projected over the next seven years, such as.: Material: high-κ gate dielectric, metal gate electrodes, lead-free solder Process: elevated S/D (selective epi) and advanced annealing and doping techniques Structure: ultra-thin body (UTB) fully depleted (FD) SOI, multiple-gate MOSFETs, multi-chip package modules It will be an important challenge to ensure the reliability of all these new materials, processes, and structures in a timely manner.
4. Scaling of DRAM and SRAM to the 22 nm technology generation	DRAM main issues with scaling—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs. SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities and soft error rate with scaling. Also, difficult lithography and etch issues with scaling.
5. Scaling high-density non-volatile memory to the 22 nm technology generation	Flash—Non-scalability of tunnel dielectric and interpoly dielectric. Dielectric material properties and dimensional control are key issues. FeRAM—Continued scaling of stack capacitor is quite challenging. Eventually, continued scaling in 1T1C configuration. Sensitivity to IC processing temperatures and conditions. MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions

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Table ITWG3 Process Integration Difficult Challenges—Long-term Years

Difficult Challenges<22 nm	*Summary of Issues*
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate MOSFETs) with ultra-thin, lightly doped body will be needed to scale MOSFETs to 10 nm gate length and below effectively. Control of parasitic resistance and capacitance will be critical. To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, nanowires, carbon nanotubes, or other high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed.
7. Dealing with fluctuations and statistical process variations in sub-11 nm gate length MOSFETs	Fundamental issues of statistical fluctuations for sub-10 nm gate length MOSFETs are not completely understood, including the impact of quantum effects, line edge roughness, and width variation.
8. Identifying, selecting, and implementing new memory structures	Dense, fast, low operating voltage non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness and attaining the very low leakage currents and power dissipation that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc.) are currently unclear. For detail, refer to ITRS Interconnect chapter.
10. Eventually, identification, selection, and implementation of advanced, non-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of non-CMOS devices need to extend well beyond CMOS limits. Non-CMOS devices need to integrate physically or functionally into a CMOS platform. Such integration may be difficult. See Emerging Research Devices sections for more discussion and detail.

[1] Scaling of MOSFETs to the 22 nm technology generation—With scaling of planar bulk MOSFETs, the channel doping will need to be increased to undesirably high levels in order to gain adequate control of short-channel effects and to set the threshold voltage properly. As a result of the high channel doping, the mobility of holes and electrons will be reduced and the junction leakage due to band-to-band tunneling and gate-induced drain leakage will increase. Furthermore, due to the small total number of dopants in the channel of extremely small MOSFETs, the percent stochastic (random) variation in the number and location of the dopants will increase sharply, and this will sharply increase the statistical variability of the threshold voltage. Another challenge for highly scaled MOSFETs is reducing the parasitic series source/drain resistance (R_{sd}) to tolerable values with very shallow source and drain junction depth.

Due to the challenges with scaling planar bulk MOSFETs, advanced devices such as ultra-thin body fully depleted SOI MOSFETs and multiple-gate, particularly double-gate (DG) MOSFETs (e.g., FinFETs) are expected to be eventually implemented. Since such devices will typically have lightly doped channels and the threshold voltage will be controlled by the metal gate electrode's work function, the challenges associated with high channel doping and stochastic dopant variation in planar bulk MOSFETs will be avoided, but numerous new challenges are expected. Amongst the most critical of such challenges will be controlling the body thickness and its variability for these ultra-thin structures, and setting the metal gate electrode work function to its desired value. As with the planar bulk MOSFET, it will be highly challenging to reduce the parasitic series source/drain resistance (R_{sd}) to tolerable values, but here the ultra-thin body is an added difficulty.

With scaling, a common issue for both planar bulk and advanced MOSFETs is expected to be increased line edge roughness as a percentage of the gate length.

For high-performance logic, in the face of increased chip complexity and increasing transistor leakage current with scaling, chip static power dissipation is expected to become particularly difficult to control while at the same time meeting aggressive targets for performance scaling. Innovations in circuit design and architecture for performance management, as well as utilization of multiple transistors on chip, are needed to design chips with both the desired performance and power dissipation. The multiple transistors have different threshold voltages (V_t), with the low V_t, high

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leakage devices used mainly in the critical paths, and higher V_t, lower leakage devices used in the rest of the chip. For low-power logic, control of static power dissipation with scaling is the critical goal. To meet this goal, the transistor leakage current is projected to be much lower than for high-performance logic, and circuit and architectural innovations as well as multiple transistors on the chip will be needed, similarly to high-performance logic.

[2] With scaling, difficulties in inducing adequate strain for enhanced mobility—Currently enhanced channel mobility due to applied strain to the channel is a major contributor to meeting the MOSFET performance requirements. With scaling, it is critically important to maintain (or even increase) the significantly enhanced CMOS channel mobility to continue to meet the performance requirements. However, the strain due to current process-induced strain techniques tends to decrease with scaling, and solutions to maintain the strain in scaled structures are needed. (For more detail, see Logic Potential Solutions section.)

[3] Timely assurance for the reliability of multiple and rapid material, process, and structural changes—In order to successfully scale ICs to meet performance, leakage current, and other requirements, it is expected that numerous major process and material innovations, such as high-κ gate dielectric, metal gate electrodes, elevated source/drain, advanced annealing and doping techniques, new low-k materials, lead-free solders, multi-chip packages, etc., will need to be implemented in well under a decade. Also, it is projected that new MOSFET structures, starting with ultra-thin body SOI MOSFETs and moving on to ultra-thin body, multiple-gate MOSFETs, will need to be implemented. Understanding and modeling the reliability issues for all these innovations so that their reliability can be ensured in a timely manner is expected to be particularly difficult.

[4] Scaling of DRAM and SRAM to the 22 nm technology generation—For DRAM, a key issue is implementation of high-κ dielectric materials and eventually MIM structures in order to get adequate storage capacitance per cell even as the cell size is shrinking. Also important is controlling the total leakage current, including the dielectric leakage, the storage junction leakage, and the access transistor source/drain subthreshold leakage, in order to preserve adequate retention time. The requirement of low leakage currents causes problems in obtaining the desired access transistor performance. Finally, deploying of low sheet resistance materials for word and bit lines to ensure acceptable speed for scaled DRAMs is critically important.

For SRAM, difficulties with scaling are expected, particularly in maintaining both acceptable noise margins and controlling instability, especially hot electron instability and negative bias temperature instability (NBTI). Also, there are difficult lithography and etch issues with scaling, and difficult issues with keeping the leakage current within tolerable targets for highly scaled SRAMs. Solving these SRAM challenges is critical to system performance, since SRAM is typically used for fast, on-chip memory.

[5] Scaling high-density non-volatile memory (NVM) to the 22 nm technology generation—Inherent in the nature of available nonvolatile semiconductor memory are two challenges. The first is that the memory element structure for each NVM technology differs from the underlying CMOS technology in some way, and accommodating those differences while attempting to scale the memory cell poses some difficult issues. These issues vary depending on which NVM technology is being considered, and specific issues are listed for each NVM type in the table. The second challenge is that the normal operating process used to set and to reset the state of the memory cell generally stresses the materials, and degradation of cell characteristics can be expected. Degradation is usually associated with a defect related mechanism rather than with an intrinsic device characteristic. Endurance and retention requirements provide the user with guidance as to the probable capability of the device and define a "safe" range of use. For both parameters it is a continuous challenge to be able to realistically predict this long-term behavior. Failure causes are difficult to identify and real-time testing is not feasible.

[6] Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs—For the long-term years, when the transistor gate length is projected to become 10 nm and below, ultra-thin body, multiple-gate MOSFETs with lightly doped channels are expected to be utilized to effectively scale the device, and particularly, to control short-channel effects for such highly scaled devices. The other material and process solutions mentioned above, such as high-κ gate dielectric, metal gate electrodes, strained silicon channels, elevated source/drain, etc., are expected to be incorporated along with the non-classical CMOS structures. For 10 nm gate length and below, body thicknesses well below 10 nm are projected, and the impact of quantum and surface scattering effects on such thin devices are not well understood. Finally, for these advanced, highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal carrier velocity and injection at the source end appears to be necessary. Eventually, high transport channel materials, such as germanium or III-V channels on silicon, or carbon nanotubes or nanowires, may be utilized.

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[7] Dealing with fluctuations and statistical process variations in sub-11 nm gate length MOSFETs—For such devices, the impact of statistical variations is not well understood, including the impact of quantum effects, line edge roughness, and variation in the ultra-thin body width.

[8] Identifying, selecting, and implementing new memory structures—In the long term, increasing difficulty is expected in scaling both DRAMs and NVMs, as discussed for each of these memory types in the table. The need for high density, fast, and new non-volatile memory structures is expected to increase, particularly to reduce power dissipation. Implementing such advanced, non-volatile structures will be a major challenge.

[9] Identifying, selecting, and implementing novel interconnect schemes—The resistivity of copper increases somewhat with scaling for widths under ~100 nm, and at κ ~1–1.5, the limits of low-κ dielectric will be reached. At that point, further interconnect performance improvements will require novel architectural and/or materials solutions

[10] Eventually, identification, selection, and implementation of advanced, non-CMOS devices and architectures for advanced information processing—Eventually, toward the end of the Roadmap or beyond, scaling of MOSFETs is likely to become ineffective and/or very costly, and advanced non-CMOS solutions will need to be implemented to continue to improve performance, power, density, etc. It is expected that such solutions will be integrated either functionally or physically with a CMOS baseline technology that takes advantage of the high-performance, cost-effective, and very dense CMOS logic that will have been developed and implemented by then.

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RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

WHAT'S NEW?

RF AND AMS CMOS

- RF CMOS requirements for millimeter-wave that are linked to the high-performance CMOS roadmap with a two-year lag.
- RF parameters for F_t, F_{max}, and noise figures at 24 GHz and 60 GHz

RF AND AMS BIPOLAR DEVICES

- Considered three separate bipolar devices—high voltage for typical low-cost bipolar devices, high speed for millimeter-wave applications, and power amplifiers.
- The focus is on high speed and power amplifiers as drivers.
- High speed device F_t scaling is less aggressive. Delayed 300 GHz by one year and 500 GHz by five years and adjusted F_{max}, J_C and BV_{CEO} scaling accordingly.
- Revised power amplifier NPN parameters and aligned them to power amplifier battery voltages
- Added noise figures at 60 GHz

ON CHIP AND EMBEDDED PASSIVES FOR RF AND ANALOG

- Added the three applications of analog, RF, and power amplifier
- Included such devices as capacitors, resistors, inductors, and varactors
- Added the metal-oxide-metal capacitor

POWER AMPLIFIERS (0.8 GHZ–10 GHZ)

- Handset—For HBT and FET based handsets that use III-V compounds and Si, added end-of-life battery voltage, FET-HBT integration for integrated bias circuit designs, and on-chip switch integration for by-passing intermediate frequency stages. The emerging markets are demanding that power amplifiers be either cost/performance driven or cost-only driven applications. Cost-only markets are driving silicon single chip alternatives.
- Base Station**—**Included cellular and the emerging worldwide interoperability for microwave access (WiMAX) that require relatively high RF power and LDMOS and III-V FET devices.
- Removed SiC devices because they are being displaced by GaN devices.

MILLIMETER WAVE (10 GHZ–100 GHZ)

- Now dominated by III-V devices (GaAs PHEMT, InP HEMT, GaAs MHEMT, GaN HEMT, InP HBT) and SiGe HBT and RF CMOS.
- Emphasized low noise amplifiers and power devices

MORE THAN MOORE FOCUS OF WIRELESS - MULTI-STANDARD APPLICATIONS

- Addressed multi-band, multi-mode, portable applications
- Because the device roadmap alone does not enable the software defined radio (SDR), added the needs to address digital radio design requirements by using a hybrid approach with wideband amplifiers and matching, filtering, and switching networks
- Added two new tables on embedded passives requirements and RFMEMS requirements.

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DIFFICULT CHALLENGES

Table ITWG4 RF and Analog Mixed-Signal (RF and AMS) Technologies for Wireless Communications Difficult Challenges

Difficult Challenges	*Summary of Issues*
Radio Integration	Performance and cost trade-offs for SoC versus SiP solutions Signal isolation and integrity are challenges to technologists, designers, and EDA tool providers for both analog and digital domains CAD solutions for integrated radio SiP designs (chip, passive, MEMS, package, tool compatibility, and model accuracies)
Device Technology	Optimizing analog/RF CMOS devices with scaled technologies. Fundamental changes in CMOS device structure may lead to the need for separate process/chip to support conventional precision analog/RF devices Increasing Ft of silicon bipolar devices by more aggressive vertical profiles Managing higher current and power densities that result from aggressive vertical profiles in silicon bipolar devices Performance and cost trade-offs for integrating passive devices Predictability of battery technology (end-of-life) and its impact on PA roadmap Compound semiconductor substrate quality, reliability, thermal management, particularly for GaN Low-cost processing equipment for compound semiconductors
Design	Design approach for wider range of supply voltages Digitizing analog functions in the software define radio (SDR) Non-linear and 3D Electromagnetic models for accurate design and simulation Computationally efficient physical models for compound semiconductors Thermal modeling and simulations that are integrated with RF and digital design tools.

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EMERGING RESEARCH DEVICES

WHAT'S NEW?

The new 2007 Emerging Research Devices (ERD) chapter has been changed and broadened compared to the 2005 ERD chapter. The section on Emerging Research Materials, prominent in 2005, has been expanded to include new materials for lithography, assembly and packaging, FEP, and interconnect in addition to Emerging Research Devices to form a separate new chapter on Emerging Research Materials (ERM). Materials research issues related to emerging devices are summarized in this ERD chapter and treated more fully in the new ERM chapter. The other major change is increased focus on emerging research device technologies that can be integrated with a CMOS platform technology to extend CMOS further into existing markets and to open new applications.

This possibility motivates an expansion in scope and content of the Emerging Research Devices chapter for 2007. The chapter evaluates emerging new research technologies for memory and information processing or logic devices and nano-architectures applied to two different approaches to realizing integrated electronic functions. One is heterogeneous integration of these new technologies with the CMOS platform, i.e., "enhanced CMOS" or "Functional Diversification". The second addresses the exciting but daunting challenge to invent one or more fundamentally new approaches to information and signal processing. This theme will require discovery and exploitation of a new means to physically represent, process, store, and transport information via new materials, process, device, nano-architecture, and systems innovations.

In the Memory section, Nanofloating Gate Memory has been removed from ERD and recommended to PIDS, and the Resistance-based Memory has been replaced with the Fuse/Antifuse Memory, the Ionic Memory, the Electronic Effects Memory, and the Macromolecular Memory (formerly the Polymer Memory). A new entry for Nanomechanical Memory has also been added.

In addition to broadening the scope of the Logic section to include alternative information processing device structures for supplementing/complementing CMOS, this section also expands the technology entry for 1D structures into a new category entitled "FET Extension". This category includes a new technology entry on "Channel Replacement" materials. These materials are proposed to replace silicon in the channel to enhance carrier mobility and velocity to enable scaling CMOS to the end of the Roadmap. Examples of channel replacement materials are Ge, SiGe, and III-V compound semiconductor materials. Development of graphene ribbon material for MOSFET application has also been added to the 1D or low dimensional category for enhanced FETs.

Finally, the Architecture section has been broadened and re-structured to include emerging research architectures utilizing, for special purposes, novel devices other than CMOS to perform unique functions. Here we use the term *architecture* to refer to a functional arrangement on a single chip of interconnected devices that includes embedded computational components. Implicit in this formulation is the assumption that these devices can be integrated with CMOS structures that will continue to perform many of the generic computational and Input/Output functions required of the implementation. This section explores device and architectural trends to give visibility to architectural options and attempt to establish criteria for weighing alternative approaches.

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DIFFICULT CHALLENGES

Table ITWG5 Emerging Research Device Technologies Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile and non-volatile memory technologies to and beyond 22 nm	SRAM and FLASH scaling will reach definite limits within the next several years (see PIDS chapter for Difficult Challenges). These are driving the need for new memory technologies to replace SRAM and FLASH memories. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM
Difficult Challenges <22 nm	
Scale CMOS to and beyond the 16 nm technology generation.	Develop new materials to replace silicon as an alternate channel to increase the saturation velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation for technology scaled to 16 nm and beyond. Candidate materials include Ge, SiGe, III-V compound semiconductors, and graphene. Develop 1D (nanowire or nanotube) structures to scale MOSFETs and CMOS gates beyond the 16 nm technology generation. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.)
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and a primitive-level architecture to provide special purpose optimized functional cores heterogeneously integrable with silicon CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and develop a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. Bridge a knowledge gap that exists between materials behaviors and device functions.

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EMERGING RESEARCH MATERIALS

WHAT'S NEW

The 2007 Emerging Research Materials (ERM) chapter is a new addition to the ITRS (previously a section in the 2005 and 2006 ERD chapter). The scope of ERM 2005–2006 was materials to support ERD, but the ERM chapter now also assesses ERM for lithography, front end process, interconnects, and assembly and package applications. The ERM chapter also identifies metrology, modeling, and environmental safety and health research needed to support these materials for their potential applications. While these ERMs have properties that make them attractive as potential solutions to future technology needs, significant progress is required for them to be used in future technologies.

Low dimensional materials, such as nanotubes, nanowires, and other nanoparticles, and macromolecules, have properties that could provide solutions for emerging research devices, lithography, front end process, interconnects, and assembly and packaging. Self-assembled materials have potential for applications in lithography, to enable high charge density capacitors, and for selective deposition or etching processes in front end processes. Spin materials are of primary interest for emerging research device applications. Complex metal oxides have potential for applications as emerging research memory and logic devices. A special set of the complex metal oxides, strongly correlated electron state materials, and their heterointerfaces may have potential to enable new logic devices with coupled spin and charge properties. The challenges for these materials the required metrology, modeling, and environmental safety and health research needed are highlighted in the difficult challenges table.

DIFFICULT CHALLENGES

The current set of sub-22 nm ERM Difficult Research Challenges is summarized in Table 1. Perhaps ERM's most difficult challenge is to deliver material options, with controlled and desired properties, in time to impact insertion decisions. These material options must exhibit the potential to enable high density emerging research devices, lithographic technologies, and interconnect fabrication and operation at the nanometer scale. This challenge, to improve the control of material properties for nanometer (nm) scale applications, requires collaboration and coordination within the research community. Accelerated synthesis, metrology, and modeling initiatives are needed to enhance targeted material-by-design capabilities and enable viable emerging material technologies. Improved metrology and modeling tools also are needed to guide the evolution of robust synthetic methods for these emerging nanomaterials. The success of many ERMs depend on robust synthetic methods that yield useful nanostructures, with the required control of composition, morphology, an integrated set of application specific properties, and compatibility with manufacturable technologies.

To achieve high density devices and interconnects, ERMs must assemble in precise locations, with controlled orientations. Another critical ERM factor for improving emerging device, interconnect, and package technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties. For novel nanometer scale materials emerging within the research environment, methodologies and data also must be developed that enable the hierarchical assessment of potential environment, safety, and health impact of new nanomaterials and nanostructures.

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Table ITWG6 Emerging Research Material Technologies Difficult Challenges

Difficult Challenges ≤ 22 nm	*Summary of Issues*
Control of nanostructures and properties	Ability to pattern sub 20nm structures in resist or other manufacturing related patterning materials (resist, imprint, self assembled materials, etc.) Control of surfaces and interfaces Control of CNT properties, bandgap distribution and metallic fraction Control of stoichiometry and vacancy composition in complex metal oxides Control and identification of nanoscale phase segregation in spin materials Control of growth and heterointerface strain Ability to predict nanocomposite properties based on a "rule of mixtures" Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability Control of interface properties (e.g., electromigration)
Control of self assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components Control of line width of self-assembled patterning materials Control of registration and defects in self-assembled materials
Characterization of nanostructure-property correlations	Correlation of the interface structure, electronic and spin properties at interfaces with low-dimensional materials Characterization of low atomic weight structures and defects (e.g., carbon nanotubes, graphitic structures, etc.) Characterization of spin concentration in materials Characterization of vacancy concentration and its effect on the properties of complex oxides 3D molecular and nanomaterial structure property correlation
Characterization of properties of embedded interfaces and matrices	Characterization of the electrical contacts of embedded molecule(s) Characterization of the roles of vacancies and hydrogen at the interface of complex oxides and the relation to properties Characterization of transport of spin polarized electrons across interfaces Characterization of the structure and electrical interface states in complex oxides
Compatibility with CMOS processing	Integration for device extensibility Material compatibility and process temperature compatibility
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures Device structure-related properties, such as ferromagnetic spin and defects Dopant location and device variability

The difficult challenges listed in Table 6 may gate the progress of the emerging research materials considered in this chapter. Significant methodology development is needed that enables material optimization and projected performance analysis in different device structures and potential application environments. Hence, the importance of significant collaboration between the synthesis, characterization, and modeling communities cannot be over stated. Material advances require an understanding of the interdependent relationships between synthetic conditions, the resulting composition and structure, and their impact on the material's functional performance. Thus, characterization methods must be sufficient to establish a quantitative relationship between composition, structure, and functional properties. Furthermore, it must enable model validation and help to accelerate the optimization of the required materials properties. This implies the need for strong alignment between experimentalists and theorists, when establishing a knowledge base to accelerate the development of ERM related models and potential applications.

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FRONT END PROCESSES

WHAT'S NEW?

Continued performance improvement through equivalent scaling has manifested itself in Front End Processes as "material-limited device scaling." Traditional transistor and capacitor formation materials, silicon, silicon dioxide, and polysilicon have been pushed to fundamental material limits and continued scaling has required the introduction of new materials. In addition, new approaches to device structure, such as non-planar multi-gate devices, will be needed for future performance scaling

Material-limited device scaling has placed new demands on virtually every front end material and unit process, starting with the silicon wafer substrate and encompassing the fundamental planar CMOS building blocks and memory storage structures. In addition, the end of planar bulk CMOS is becoming visible within the next several years. As a consequence we must be prepared for the emergence of CMOS technology that uses non-conventional MOSFETs or alternatives such as planar fully depleted SOI (FDSOI) devices and dual- or multi-gate devices either in a planar of vertical geometry. Projections for the manufacturing introduction of non-conventional MOSFET devices are 2010 for FDSOI and 2011 for multi-gate. The challenges associated with integration of these diverse new materials and structures are the central theme of the FEP difficult challenges.

Combined with the extension of silicon oxynitride gate dielectric materials and the introduction of strain-enhanced-mobility channels, the need for high-κ had been delayed, but is now upon us. It is expected that leading manufacturers will start production of high-κ gate dielectrics in 2008. Mobility enhancement and channel-length scaling, which requires accelerated scaling of junctions to control short channel effects, will continue to provide enhanced device performance. It is also expected that dual metal gates, having appropriate work functions, will be put in production by leading manufacturers in 2008 to replace the dual doped polysilicon gates, currently the mainstay of CMOS technology.

The introduction of new materials is also expected to impose added challenges to the methods used to dope and activate silicon. In addition to the scaling imposed need for producing very shallow highly activated junctions, the limited thermal stability of most high-κ materials is expected to place new boundaries on thermal budgets associated with dopant activation. In a worst-case scenario, the introduction of these materials could have a significant impact on the overall CMOS process architecture.

In the memory area, high-κ materials are now in use for both stacked and trench DRAM capacitors. DRAM stacked capacitors are also now using metal-insulator-metal (MIM) structures with trench capacitors projected to move to MIM by 2010. It is expected that high-κ materials will be required for the Floating Gate Flash memory interpoly dielectric by 2010 and for tunnel dielectric by 2013. FeRAM will make a significant commercial appearance where ferroelectric and ferromagnetic storage materials would be used. The introduction of these diverse materials into the manufacturing mainstream is viewed as important, difficult challenges. In addition, phase-change memory (PCM) devices are expected to make a commercial appearance by 2010.

In the starting wafer area, it is expected that alternatives to bulk silicon such as silicon-on-insulator substrates will proliferate. Additionally, various forms of strained silicon technology may be incorporated although these have been and continue to be principally achieved through value-added modifications to the IC manufacturing process. Also, an important difficult challenge expected to emerge within the Roadmap horizon is the potential need for the next generation 450 mm silicon substrate. Based upon historical diameter change cycles, the industry is already several years behind the pace necessary to allow the next generation 450mm silicon substrate to be ready for device manufacture in the year 2012.

Front end cleaning processes will continue to be impacted by the introduction of new front end materials such as high-κ dielectrics, metal gate electrodes and mobility-enhanced channel materials. Scaled devices are expected to become increasingly shallow, requiring that cleaning processes become completely benign in terms of substrate material removal and surface roughening. Scaled and new device structures will also become increasingly fragile, limiting the physical aggressiveness of the cleaning processes that may be employed. Also, there is a challenge for particle scanning technology to reliably detect particles smaller than 28nm on a wafer surface for characterization of killer defect density and to enable yield learning.

DIFFICULT CHALLENGES

Table ITWG7 Front End Processes Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Starting Materials	1.5 mm edge exclusion FDSOI Si and buried oxide thickness control SOI defectivity levels Full production of 450 mm wafer size
Surface Preparation	Critical surface particle size below 28 nm not measurable on wafer Ability to achieve clean surfaces while controlling material loss and surface damage
Thermal/Thin Films/Doping/Etch	Introduction of high-κ/metal gate into high performance (HP) and low operating/low standby power (LOP/LSTP) and equivalent oxide thickness (EOT) scaling below 0.8 nm Increasing device performance with strain engineering and applying it to FDSOI and multi-gate technologies Scaling extension junction depths below 10 nm while achieving high dopant activation Achieving manufacturable interfacial contact resistivities below 10^{-7} Ω-cm^2 to meet parasitic series resistance requirements Si thickness and control for FDSOI and Multi-gate Gate critical dimension control for physical gate length < 20 nm Introduction of new channel materials with high interface quality and low processing thermal budget
DRAM	Improvement of oxide etching capability for high aspect ratio (>40) storage node formation in stack capacitor and for oxide hardmask for high aspect ration trench capacitor. Improvement of Si etching capability for high A/R (>90) trench capacitor formation. Continued scaling of stacked and trench capacitor dielectric Teq below 0.5 nm Continued scaling of physcial dielectric thickness (tphys) while maintaining high dielectric constant (>90) and low leakage current of dielectric
Non-volatile Memory	Scaling of IPD Teq to <6Å for NAND and NOR Scaling of tunnel oxide thickness to <8Å for NOR Scaling of STI fill aspect ratio to >9 starting for NAND PCM material conformality of ≥90% PCM minimum operating temperature of 125 C PCM resistivity change and reset current density Integration and scaling of FeRAM ferroelectric materials Continued scaling of FeRAM cell structure
Difficult Challenges < 22 nm	*Summary of Issues*
Starting Materials	1.5 mm edge exclusion FDSOI Si and buried oxide thickness control SOI defectivity Surface particles
Surface Preparation	Surface particles not measurable Ability to achieve clean surfaces while controlling material loss and surface damage Metrology of surfaces that may be horizontally or vertically oriented relative to the chip surface Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface Achievement and maintenance of structural, chemical, and contamination control of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface
Thermal/Thin Films/Doping/Etch	Continued scaling of HP multigate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation. Continued EOT scaling below 0.7 nm with appropriate metal gates Gate CD Control
DRAM	Continued scaling of capacitor structures for both stacked and trench type as well as continued scaling of dielectric thickness
Non-volatile Memory	Floating gate Flash technology considered unscalable beyond 22 nm—new Flash NVM technology will be required Continued scaling of phase change memory technology Continued scaling of FeRAM technology

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LITHOGRAPHY

DIFFICULT CHALLENGES

Table ITWG8 Lithography Difficult Challenges

*Difficult Challenges ≥ 32 nm**	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Registration, CD, and defect control for masks
	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features
	Understanding polarization effects at the mask and effects of mask topography on imaging and optimizing mask structures to compensate for these effects
	Eliminating formation of progressive defects and haze during exposure
	Determining optimal mask magnification ratio for <32 nm half pitch patterning with 193 nm radiation and developing methods, such as stitching, to compensate for the potential use of smaller exposure fields
	Development of defect free 1× templates
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time
	Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume
	Sufficient lifetime for exposure tool technologies
	Resources for developing multiple technologies at the same time
	ROI for small volume products
	Stages, overlay systems and resist coating equipment development for wafers with 450 mm diameter
Process control	Processes to control gate CDs to < 1.3 nm 3σ
	New and improved alignment and overlay control methods independent of technology option to <5.7 nm 3σ overlay error
	Controlling LER, CD changes induced by metrology, and defects < 10 nm in size
	Greater accuracy of resist simulation models
	Accuracy of OPC and OPC verification, especially in presence of polarization effects
	Control of and correction for flare in exposure tool, especially for EUV lithography
	Lithography friendly design and design for manufacturing (DFM)
Immersion lithography	Control of defects caused in immersion environment, including bubbles and staining
	Resist chemistry compatibility with fluid or topcoat and development of topcoats
	Resists with index of refraction > 1.8
	Fluid with refractive index > 1.65 meeting viscosity, absorption, and fluid recycling requirements
	Lens materials with refractive index >1.65 meeting absorption and birefringence requirements for lens designs
EUV lithography	Low defect mask blanks, including defect inspection with < 30 nm sensitivity and blank repair
	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components
	Resist with < 3 nm 3σ LWR, < 10 mJ/cm2 sensitivity and < 40 nm ½ pitch resolution
	Fabrication of optics with < 0.10 nm rms figure error and < 10% intrinsic flare
	Controlling optics contamination to achieve > five-year lifetime
	Protection of masks from defects without pellicles
Double patterning	Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures
	Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs
	Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
	Photoresists with independent exposure of multiple passes
	Fab logistics and process control to enable low cycle time impact that include on-time availability of additional reticles and efficient scheduling of multiple exposure passes

**Lithography challenges ≥32nm versus the convention of the 2007 ITRS for challenges of ≥22nm will be reviewed in the 2008 Update.*

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Table ITWG8 Lithography Difficult Challenges (continued)

*Difficult Challenges < 32 nm**	*Summary of Issues*
Mask fabrication	Defect-free masks, especially for 1× masks for imprint and EUVL mask blanks free of printable defects
	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair), especially for 1× masks
	Mask process control methods and yield enhancement
	Protection of EUV masks and imprint templates from defects without pellicles
	Phase shifting masks for EUV
Metrology and defect inspection	Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3σ
	Metrology for achieving < 2.8 nm 3σ overlay error
	Defect inspection on patterned wafers for defects < 30 nm, especially for maskless lithography
	Die-to-database inspection of wafer patterns written with maskless lithography
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
	Development of cost-effective optical and post-optical masks
	Achieving ROI for industry with sufficient lifetimes for exposure tool technologies and ROI for small volume products
Gate CD control improvements and process control	Development of processes to control gate CD < 0.9 nm 3σ with < 1.2 nm 3σ line width roughness
	Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3σ overlay error, especially for imprint lithography
	Process control and design for low k1 optical lithography
Resist materials	Resist and antireflection coating materials composed of alternatives to PFAS compounds
	Limits of chemically amplified resist sensitivity for < 32 nm half pitch due to acid diffusion length
	Materials with improved dimensional and LWR control

**Lithography challenges <32nm versus the convention of the 2007 ITRS for challenges of <22nm will be reviewed in the 2008 Update.*

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INTERCONNECT

WHAT'S NEW?

Over the past four decades the primary drivers for conventional metal dielectric interconnects have been technology scaling and the desire for increased performance. During this timeframe, interconnect wiring has evolved from a single level of Al/SiO_2 wiring to eleven levels of Cu/low-κ interconnect in the current generations. In the near term, the most difficult challenge for interconnect is the introduction of new materials that meet the wire conductivity requirements and reduce the dielectric permittivity. Future effective κ requirements preclude the use of a trench etch stop for dual damascene structures. This is an additional impediment to achieving tight control of pattern, etch and planarization of metal wires to reduce RC variability. At < 22 nm, feature size effects, such as electron scattering from grain boundaries and interfaces, will continue to increase the effective Cu resistivity. Ultra low-κ dielectrics may be replaced by air gaps in selective areas. The accelerated scaling of MPU pitch has aggravated the copper electromigration problem. J_{max} limits for current dielectric cap technologies for copper will be exceeded by 2010. Modification of the Cu surface to form CuSiN, use of alloys such as Cu-Al or implementation of a selective metal cap technology, such as CoWP, will be necessary.

However, even with material changes to improve performance, the difficulties for interconnect technology resulting from scaling can be noted by observing that older 1.0 μm Al/SiO_2 technology had a transistor delay of ~20 ps and the RC delay of a 1 mm line was ~ 1.0 ps, while in a projected 35 nm Cu/low-κ technology, the transistor delay will be ~1.0 ps, and the RC delay of a 1 mm line will be ~250 ps. In addition, at 130 nm half-pitch , approximately 51% of microprocessor power was consumed by interconnect, with a projection that without changes in design philosophy, in the next five years up to 80% of microprocessor power will be consumed by interconnect. In recognition of the increasing importance of the dynamic power dissipated in the interconnect structure, a new power metric was added to the MPU and ASIC Technology Requirements Tables in 2006. The power metric is the power (measured in Watts) dissipated per Ghz of frequency and cm^2 of metal layer. Although the power metric is seen to plateau for the long-term years due to aggressive introduction of low-κ dielectrics, the power dissipated in the interconnect structure will still increase dramatically due to higher frequencies and increases in the number of metal layers.

This dramatic increase of the interconnect impact on performance and power shows clearly the challenges created by the scaling of the conventional metal/dielectric system. In the last few years IC manufacturers have recognized the difficulty of addressing interconnect performance and power issues by technology means alone. In response, they have implemented design and architecture improvements to address interconnect limitations; however, even with these advances, interconnect remains a critical bottleneck for many applications. This creates an ever increasing opportunity for developing and introducing alternative interconnect solutions. In addition to resolving some of the power and performance problems associated with conventional metal/dielectric systems, alternative interconnect technologies offer the potential of increased product functional diversity. For example, optical interconnects might be used with multiple wavelengths in a single waveguide (wavelength-division multiplexing (WDM)) to provide not only higher bandwidth density for global interconnects, but also in combination with on-chip, voltage variable gratings to provide selective routing possibilities that can be used for radically different signal processing functions than those currently available. In recognition of these significant opportunities, the 2007 Interconnect ITRS roadmap includes expanded sections on the status and challenges of three dimensional chip and wafer stacking (3DIC), optical interconnect and carbon nanotubes (CNT).

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DIFFICULT CHALLENGES

Table ITWG9 Interconnect Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures, processes and new materials*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Three-dimensional control of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Difficult Challenges < 22 nm	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address 3D structures and other packaging issues*	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

** Top three challenges*

CMP—chemical mechanical planarization DRAM—dynamic random access memory

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FACTORY INTEGRATION

DIFFICULT CHALLENGES

Difficult challenges associated with factory integration span multiple technology generations and cut across the five factory thrust areas. Responses to these challenges are often linked to the technology introductions as a matter of industry convenience to minimize disruptions to operating factories. Near-term difficult challenges for the factory include business, technical, and economic issues that must be addressed.

Table ITWG10 Factory Integration Difficult Challenges

Difficult Challenges ≥22 nm	*Summary Of Issues*
Responding to rapidly changing, complex business requirements	Many new and co-existing business models including IDM, foundry, fabless, joint ventures, collaborations, other outsourcing, etc., need to be considered in the Factory Integration Increased expectations by customers for faster delivery of new and volume products Need for improve integration of the entire product design and manufacturing process Faster design → prototype and pilot → volume production Enhanced customer visibility into outsourced production operations Reduced time to ramp factories, products, and processes to stay competitive within the rapidly changing business environment Building 30+ mask layer System on a Chip (SoC) with high-mix manufacturing as the model in response to diversified customers' requirement Rapid and frequent factory plan changes driven by changing business needs Ability to model factory performance to optimize output and improve cycle time for high mix factories Ability to constantly adjust equipment loading to keep the factory profitable Manufacturing knowledge and control information need to be shared as required among disparate factories
Achieving growth targets while margins are declining	Implications of rising wafer, packaging, and other materials cost on meeting cost targets Meeting high factory yield much faster at startup Addressing increased complexity while keeping costs in check Reducing complexity and waste across the supply chain Inefficiencies introduced by non-product wafers (NPW) competing for resources with production wafers High cost and cycle time of mask sets for manufacturers impacting affordability of new product designs Increasing dedication of masks and equipment causing manufacturing inefficiencies Challenges introduced with sharing of mask sets Difficulty in maintaining the historical 0.7× transistor shrink per year for die size and cost efficiency
Managing ever increasing factory complexity	Quickly and effectively integrating rapid changes in process technologies Managing carriers with multiple lots, wafers with multiple products, or multiple package form factors Comprehending increased purity requirements for process and materials Need to run aluminum and copper back end in the same factory Increasing number of processing steps coupled with process and product complexity Need to concurrently manage new and legacy software and systems with increasingly high interdependencies Explosive growth of data collection/analysis requirements driven by process and modeling needs Increased requirements for high mix factories. Examples are complex process control as frequent recipe creation and changes at process tools and frequent quality control due to small lot sizes
Meeting factory and equipment reliability, capability or productivity requirements per the Roadmap	Process equipment not meeting availability, run rate, and utilization targets out of the box Stand alone and integrated reliability for equipment and systems to keep factories operating Increased impacts that single points of failure have on a highly integrated and complex factory Quality issues with production equipment embedded controllers to improve equipment process performance instability and NPW requirements Lack of good data to measure equipment and factory effectiveness for optimization and improvement programs Factory capacity planning and supply chain management systems are not continuously base lined with actual factory data creating errors Small process windows and tight process targets at >45 nm (DRAM contacted half pitch)in many modules make process control increasingly difficult Lack of migration paths which inhibit movement from old inefficient systems to new highly productive systems

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Table ITWG10 Factory Integration Difficult Challenges (continued)

Difficult Challenges <22 nm	*Summary of Issues*
Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	Need to quickly convert factories to new process technologies while reusing equipment, facilities, and skills Minimizing downtime to on-going operations while converting factories to new technologies Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] Continued need to improve both throughput and cycle time Reuse of building, production and support equipment, and factory information and control systems across multiple technology generations Understanding up-front costs to incorporate EFS (Extendibility, Flexibility and Scalability) Comprehending increased purity requirements for process and materials Accelerating the pace of standardization to meet industry needs
Meeting process requirements at 65 nm and 45 nm generations running production volumes	Small process windows and tight process targets at 32 nm generations in many modules make process control increasingly difficult Complexity of integrating next generation lithography equipment into the factory Overall development and volume production timelines continuing to shrink Device and process complexity make the ability to trace functional problems to specific process areas difficult Difficulty in running different process parameters for each wafer while maintaining control windows and cycle time goals Reducing the impacts of parametric variation
Increasing global restrictions on environmental issues	Need to meet regulations in different geographical areas Need to meet technology restrictions in some countries while still meeting business needs Comprehending tighter ESH/Code requirements Lead free and other chemical and materials restrictions New material introduction
Post-conventional CMOS manufacturing uncertainty	Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements will have on factory design Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency Need to run CMOS and post CMOS processes in the same factory
Emerging factory paradigm and next wafer size change	Uncertainty about 450 mm conversion timing and ability of 300 mm wafer factories to meet historic 30% cost effectiveness. Traditional strategies to scale wafers and carriers for the 450 mm wafer size conversion may not work with [450 mm] 25 wafer carriers and drive significant production equipment and material handling changes Uncertainty concerning how to reuse buildings, equipment, and systems to enable 450 mm wafer size conversion at an affordable cost

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ASSEMBLY AND PACKAGING

DIFFICULT CHALLENGES

Innovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices. Near term difficult challenges exist in all phases of the assembly and packaging process from design through manufacturing, test and reliability.

Many critical technology requirements are yet to be met and they are listed in Table ITWG11 below. Meeting these requirements will demand significant investment in research and development.

Table ITWG11 Assembly and Packaging Difficult Challenges

Difficult Challenges ≥22 nm	*Summary of Issues*
Impact of BEOL including Cu/low κ on packaging	-Direct wire bond and bump to Cu or improved barrier systems bondable pads - Dicing for ultra low k dielectric -Bump and underfill technology to assure low-κ dielectric integrity including lead free solder bump system -Improved fracture toughness of dielectrics -Interfacial adhesion -Reliability of first level interconnect with low κ -Mechanisms to measure the critical properties need to be developed. -Probing over copper/low κ
Wafer level CSP	-I/O pitch for small die with high pin count -Solder joint reliability and cleaning processes for low stand-off -Wafer thinning and handling technologies -Compact ESD structures -TCE mismatch compensation for large die
Coordinated design tools and simulators to address chip, package, and substrate co-design	-Mix signal co-design and simulation environment -Rapid turn around modeling and simulation -Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis -Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) -System level co-design is needed now. -EDA for "native" area array is required to meet the Roadmap projections. -Models for reliability prediction
Embedded components	-Low cost embedded passives: R, L, C -Embedded active devices -Quality levels required not attainable on chip -Wafer level embedded components
Thinned die packaging	- Wafer/die handling for thin die - Different carrier materials (organics, silicon, ceramics, glass, laminate core) impact -Establish infrastructure for new value chain -Establish new process flows -Reliability -Testability -Different active devices -Electrical and optical interface integration

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Table ITWG11 Assembly and Packaging Difficult Challenges (continued)

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Close gap between chip and substrate Improved organic substrates	-Increased wireability at low cost -Improved impedance control and lower dielectric loss to support higher frequency applications -Improved planarity and low warpage at higher process temperatures -Low-moisture absorption -Increased via density in substrate core -Alternative plating finish to improve reliability -Solutions for operation temp up to C5-interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology -Production techniques will require silicon-like production and process technologies after 2005 -Tg compatible with Pb free solder processing (including rework at260 C)
High current density packages	-Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. -Whisker growth -Thermal dissipation
Flexible system packaging	-Conformal low cost organic substrates -Small and thin die assembly -Handling in low cost operation
3D packaging	-Thermal management -Design and simulation tools -Wafer to wafer bonding -Through wafer via structure and via fill process -Singulation of TSV wafers/die - Test access for individual wafer/die -Bumpless interconnect architecture
Difficult Challenges <22 nm	*Summary of Issues*
Package cost does not follow the die cost reduction curve	-Margin in packaging is inadequate to support investment required to reduce cost -Increased device complexity requires higher cost packaging solutions
Small die with high pad count and/or high power density	These devices may exceed the capabilities of current assembly and packaging technology requiring new solder/UBM with: -Improved current density capabilities -Higher operating temperature
High frequency die	-Substrate wiring density to support >20 lines/mm -Lower loss dielectrics—skin effect above 10 GHz -“Hot spot” thermal management There is currently a “brick wall” at five-micron lines and spaces.
System-level design capability to integrated chips, passives, and substrates	-Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. -Complex standards for information types and management of information quality along with a structure for moving this information will be required. -Embedded passives may be integrated into the “bumps” as well as the substrates.
Emerging device types (organic, nanostructures, biological) that require new packaging technologies	-Organic device packaging requirements not yet defined (will chips grow their own packages) -Biological interfaces will require new interface types

TSV—through silicon via

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ENVIRONMENT, SAFETY, AND HEALTH

WHAT'S NEW?

- ESH Tables have been completely rewritten
- 2007/8 requirements are primarily focused on setting ESH metric baseline and replace the sliding scale of relative improvements
- Chemical/Materials table and process table are now reflective of ESH goals for initial chemical selection and process parameters respectively (the Process Table is new from 2005).
- Additions for 2007 include ERM requirements and a New Equipment Design section
- All metrics have been evaluated and updated where appropriate
- Potential Solutions Tables have incorporated the elements which are solution oriented but previously contained in the technical requirements tables

DIFFICULT CHALLENGES

Table ITWG12 Environment, Safety, and Health Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Chemicals and materials management	*Chemical Assessment* Evaluation and refinement of quality, rapid assessment methodologies to ensure that new materials such as nanomaterials can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation Regional differences in regulations for chemicals; given regional movement for R&D, pre-manufacturing, and full commercialization Trend towards lowering exposure limits and more monitoring
	Chemical Data Availability Inability to forecast/anticipate future restrictions or bans on materials, especially nanomaterials Lack of comprehensive ESH data for new, proprietary chemicals and materials to respond to the increasing external and regional requirements on the use of chemicals
	Chemical Exposure Management Lack of information on how the chemicals and materials are used and what process by-products are formed Method to obtain information on how the chemicals and materials are used and what process by-products are formed
Process and equipment management	*Process Chemical Optimization* Need to develop equipment and processes that meet technology demands while reducing impact on human health, safety and the environment, both through the use of more benign materials, and by reducing chemical quantity requirements through more efficient and cost-effective process management
	Environment Management Capability for component isolation in waste streams Need to understand ESH characteristics of process emissions and by-products to identify the appropriate mitigation Need to develop effective management systems to address issues related to hazardous and non-hazardous residues from the manufacturing processes
	Global Warming Emissions Reduction Need to reduce emissions from processes using high GWP chemicals
	Water and Energy Conservation Need for innovative energy- and water-efficient processes and equipment

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Table ITWG12 Environment, Safety, and Health Difficult Challenges (continued)

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Process and equipment management	*Consumables Optimization* Need for more efficient utilization of chemicals and materials, and increased reuse and recycling
	Byproducts Management Development of improved metrology for byproduct speciation.
	Chemical Exposure Management Need to design-out potential for chemical exposures and the necessity for personal protective equipment (PPE) Design for Maintenance Need to design equipment so that commonly serviced components and consumable items are easily and safely accessed Need to design equipment so that maintenance and service may be safely performed by a single person Need to minimize health and safety risks during maintenance activities.
	Equipment End-of-Life Need to develop effective management systems to address issues related to re-use and disposal of equipment
	Conservation Need to reduce use of energy, water and other utilities Need for more efficient thermal management of clean rooms and facilities systems
Facilities technology requirements	*Global Warming Emissions Reduction* Need to design energy efficient manufacturing facilities Need to reduce total CO_2 equivalent emissions
	Sustainability Metrics Need to identify the elements for defining and measuring the sustainability of a technology generation
Sustainability and product stewardship	*Design for ESH* Need to make ESH a design parameter at the design stage of new equipment, processes and products
	End-of-Life Disposal/Reclaim Need to design facilities, equipment and products to facilitate re-use/disposal at end of life
Difficult Challenges < 22 nm	*Summary of Issues*
Chemicals and materials management	*Chemical Assessment* Evaluation and refinement of quality, rapid assessment methodologies to ensure that new materials such as nanomaterials can be utilized in manufacturing, while protecting human health, safety, and the environment without delaying process implementation
	Chemical Data Availability Lack of comprehensive ESH data for new, proprietary chemicals and materials to respond to the increasing external and regional requirements on the use of chemicals
	Chemical Exposure Management Lack of information on how the chemicals and materials are used and what process by-products are formed
	Chemical Reduction Need to develop processes that meet technology demands while reducing impact on human health, safety, and the environment, both through the use of more benign materials, and by reducing chemical quantity requirements through more efficient and cost-effective process management Need to reduce emissions from processes using high GWP chemicals
Process and equipment management	*Environment Management* Need to understand ESH characteristics of process emissions and by-products to identify the appropriate mitigation Need to develop effective management systems to address issues related to hazardous and non-hazardous residues from the manufacturing processes
	Water and Energy Conservation Need to reduce water and energy consumption Need for innovative energy and water-efficient processes and equipment

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Table ITWG12 Environment, Safety, and Health Difficult Challenges (continued)

Difficult Challenges < 22 nm	*Summary of Issues*
Process and equipment management	*Consumables Optimization* Need for more efficient utilization of chemicals and materials, and increased reuse and recycling
	Chemical Exposure Management Need to design-out potential for chemical exposures and need for personal protective equipment (PPE)
	Design for Maintenance Need to design equipment so that maintenance and service may be safely performed by a single person Need to design equipment so that commonly serviced components and consumable items are easily accessed Need to minimize health and safety risks during maintenance activities
	Equipment End-of-Life Need to develop effective management systems to address issues related to re-use and disposal of equipment
	Conservation Need to reduce use of energy, water and other utilities Need for more efficient thermal management of clean rooms and facilities systems
Facilities technology requirements	*Global Warming Emissions Reduction* Need to design energy efficient facilities support equipment and manufacturing facilities. Need to reduce emissions from processes using high GWP chemicals
	Sustainability Metric Need to identify the elements for defining and measuring the sustainability of a technology generation Need to identify the elements for defining and measuring sustainability at a factory infrastructure level Design for ESH Need method to holistically evaluate and quantify the ESH impacts of processes, chemicals, and process equipment for the total manufacturing process Need to make ESH a design parameter in development of new equipment, processes and products End-of-Life Disposal/Reclaim Need to design facilities, equipment, and products to facilitate re-use/disposal at end of life
Sustainability and product stewardship	

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YIELD ENHANCEMENT

DIFFICULT CHALLENGES

The difficult challenges for the Yield Enhancement chapter are summarized in Table ITWG13. The detection of multiple killer defect types and simultaneous differentiation at high capture rates, low cost of ownership, and throughput were identified by the community as the most important challenge for yield enhancement. Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes defined by technology generations. The need of higher sensitivity of in-line inspections is leading to a dramatic increase of defect counts. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects. At the same time, a low Cost of Ownership (CoO) of the tools demands for high throughput of the inspection. This is in conflict with the issue of improving the signal-to-noise ratio. The key of successful inspection results are both a high sensitivity and a high capture rate for Defects of Interest (DOI).

The wafer edge and bevel control have a top priority on the list of key challenges. Defects and process problems around wafer edge and wafer bevel were identified to impact yield. It is a key challenge to find the appropriate inspection of wafer edge, bevel, and apex on the wafer front and backside. Defect inspection concepts or technologies are either under development or have to be realized within the next few years.

Data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and to determine the required control limits. The issues for this challenge are to define the relative importance of different contaminants to wafer yield, a standard test for yield/parametric effect, and a maximum process variation (control limits). The fundamental challenge is to understand the correlation between impurity concentration in key process steps and device yield, reliability, and performance. This correlation will determine whether further increases in contamination limits are truly required. The challenge increases in complexity as the range of process materials widens and selection of the most sensitive processes for study will be required for meaningful progress.

It is a challenge to effectively identify Systematic Mechanisms Limited Yield (SMLY). The tackling through logic diagnosis capability designed into products and systematically incorporated in the test flow is crucial. The irregularity of features makes logic areas very sensitive to SMLY such as patterning marginalities across the lithographic process window. Before reaching random-defect limited yields, the SMLY should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different Automatic Test Pattern Generation (ATPG) flows to accommodate, Automatic Test Equipment (ATE) architecture that can lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die, and statistical aggregation of diagnosis results for building a layout-dependent systematic yield model.

The use of Scanning Electron Microscope (SEM) Energy Dispersive X-ray (EDX) for in-line chemical analysis has inherent limitations that are magnified, as defects of interest become smaller than 100 nm. Sampling volume is the primary limitation, followed by insufficient bonding information and possible e-beam damage. So tools/techniques are needed for elemental analysis in-line. The focus of required developments is on light elements and small amount of samples, as the need to analyze smaller particle increases with shrinking geometries. This challenge is a crosscut of yield enhancement and metrology issues.

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Table ITWG13 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Detection of multiple killer defect types / signal to noise ratio – The detection of multiple killer defect types and simultaneous differentiation at high capture rates, low cost of ownership and throughput is required. The need of higher sensitivity of in-line inspections is leading to a dramatic increase of defect counts. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.	Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. Reduction of inspection costs and increase of throughput is crucial in view of CoO. Detection particles at critical size may not exist. Detection of line edge roughness due to process variation. Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. Filtering and use of Automatic Defect Classification (ADC) is a potential solution for reduction of noise. Reduction of background noise from detection units and samples to improve the sensitivity of systems. Improvement of signal to noise ratio to delineate defect from process variation. Where does process variation stop and defect start?
Wafer edge and bevel control and inspection — Defects and process problems around wafer edge and wafer bevel are identified to cause yield loss.	Find a for production suitable inspection of wafer edge, bevel and apex on the wafer front and backside.
Process stability versus absolute contamination level including the correlation to yield — Test structures, methods, and data are needed for correlating process fluid contamination types and levels to yield and determine required control limits.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect. Definition of maximum process variation (control limits).
Linking systematic yield loss to layout attributes — The irregularity of features makes logic areas very sensitive to Systematic Mechanisms Limited Yield (SMLY) such as patterning marginalities across the lithographic process window.	SMLY should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis run time per die. d) Statistical aggregation of diagnosis results for building a layout-dependent systematic yield model. Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic yield loss, and has to improve their coverage.
High aspect ratio inspection (HARI) — The requirement for high-speed and cost-effective high aspect ratio inspection tools remains as the work around using e-beam inspection does not at all meet requirement for throughput and low cost. Sensitivity requirements are leading to a dramatic increase of defect counts. The major challenge is to find the yield relevant defect types under the vast amount of defects.	Poor transmission of energy into bottom of via and back out to detection system. Rapid detection of defects at ½× Ground Rule (GR) associated with high-aspect-ratio contacts, vias, and trenches, and especially defects near or at the bottoms of these features Large number of contacts and vias per wafer
Difficult Challenges < 22 nm	*Summary of Issues*
In-line defect characterization and analysis — Alternatives to Energy Dispersive X-ray (EDX) analysis systems are required for in-line defect characterization and analysis for defects smaller 100 nm [1]. The focus has to be on light elements, small amount of samples due to particle size following the miniaturization, and microanalysis.	The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. It will be recommended to supply information on chemical state and bonding especially of organics. Small volume technique adapted to the scales of technology generations. Capability to distinguish between the particle and the substrate signal.
Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	Development of test structures for new technology generations Address complex integration issues Model ultra-thin film integrity issues Improve scaling methods for front-end processes including increased transistor packing density

[1] Cross-link to Metrology chapter

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METROLOGY

WHAT'S NEW?

Metrology is defined as the science of measurement. For the past several years, the ITRS has provided an industry consensus look into the extension of CMOS and the nano-scale technology beyond CMOS. The nanoscale nature of today's transistor and interconnect features results in new materials properties that alter many basic assumptions in measurement and its associated models. The 2007 ITRS Metrology Roadmap discusses the status of key measurements such as critical dimension metrology, overlay, front end and interconnect film and process metrology. It also discusses measurement needs for Emerging Materials and Devices.

The ITRS Metrology TWG found that existing CD metrology methods can be enhanced to extend them to the 32 nm ½ pitch and possibly the 22 nm ½ pitch. Overlay metrology faces new issues if dual patterning and dual exposure processes are quickly moved into manufacturing. Although high k and metal gates have been moved forward into volume manufacturing in 2009, metrology requirements remain process dependent. One key example is nitrogen concentration and profile control in the high k and its interfaces. Stress metrology for process enhanced mobility is explored in greater detail in the 2007 Metrology Roadmap, and the TWG found that the variety of processes used to stress the channel mean a lack of consensus on the best approach. Interconnect Metrology and Frond End Process Metrology both have unmet need of in-line measurement of sidewall film thickness. FinFETs and interconnect trenches are just two examples of structures requiring sidewall metrology. Some future needs for Interconnect Metrology require a coordinated effort including 3D Interconnect and carbon nanotubes metrology.

Gaps in measurement technology require emphasis. Gaps can be found in both CMOS extension and beyond CMOS. *One gap is the ability to measure properties of materials such as thickness on the sidewalls of densely patterned features such as gates, FINS, and trenches.* Another gap is meeting the fundamental challenge for materials characterization of imaging and measurement of materials properties at atomic dimensions. Here, the most often mentioned goal is to provide 3D, atomic resolution measurements. The fact that some materials properties are not localized to atomic dimensions is noteworthy. The fundamental challenge for factory metrology will be the measurement and control of atomic dimensions while maintaining profitable high volume manufacturing.

The Metrology roadmap has repeated the call for a proactive research, development, and supplier base for many years. The relationship between metrology and process technology development needs fundamental restructuring. In the past the challenge has been to develop metrology ahead of target process technology. Today we face major uncertainty from unresolved choices of fundamentally new materials and radically different device designs. *Understanding the interaction between metrology data & information and optimum feed back, feed forward, and real-time process control are key to restructuring the relationship between metrology and process technology.*

A new section has been added to the Metrology Roadmap that covers metrology needs for emerging technology paradigms such as spintronics and molecular electronics. The wide variety of materials and devices described in the Emerging Research Materials and Emerging Research Devices sections provides a challenge to both resources and measurement technology. For example, imaging and measuring soft materials found in molecular electronics is considerably different from the materials used for nanowires, nanotubes, and spintronics. The impact of quantum confinement and quantum size effects as well as surface states alters the optical and electrical properties of materials. A diverse set of measurement needs is described here and in the Emerging Research Materials and Emerging Research Devices sections.

Metrology tool development requires access to new materials and structures if it is to be successful. It requires the availability of state-of-the-art capabilities to be made available for fabrication of necessary standards and development of metrology methodologies in advance of production. This requires a greater attention to expanding close ties between metrology development and process development. When the metrology is well matched to the process tools and processes, ramping times for pilot lines and factories are reduced. An appropriate combination of well-engineered tools and appropriate metrology is necessary to maximize productivity while maintaining acceptable cost of ownership.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 22 nm technology generation. Metrology needs after 2015 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table ITWG14 presents the ten major challenges for metrology.

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Table ITWG14 Metrology Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of new process technology such as Dual Patterning Lithography, complicated 3D structures such as capacitors and contacts for memory, and 3D Interconnect are not ready for their rapid introduction.	Overlay measurements for Dual Patterning have tighter control requirements. Overlay defines CD. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures including capacitors, devices, and contacts.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 22 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks. Sampling plan optimization is key to solve these issues.
Statistical limits of sub-32 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for *beyond CMOS.*	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

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MODELING AND SIMULATION

WHAT'S NEW?

In 2007, the same approach as in the preceding years has been followed in the Modeling and Simulation chapter:

As a cross-cut chapter it again started from a through analysis of the requirements of the other ITWGs, especially regarding the technological options chosen and the time schedules estimated by them. This resulted both in elaborate crosscut texts with each of these ITWGs and directed the preparation of the 2007 Modeling and Simulation text and tables, which took these requirements on board and complemented them with the assessment of the technical state-of-the-art and possibilities. In turn, the text of the 2007 Modeling and Simulation chapter was rewritten or updated in order to capture these developments, although its structure consisting of ten topical subchapters was left unchanged.

In 2007 there have been two major changes in the Modeling and Simulation Difficult Challenges. Most apparent, two challenges have been replaced: The former short-term challenge "High-frequency device and circuit modeling for 5-100 GHz applications" has been replaced by the new short-term challenge "Circuit element and system modeling for high frequency (up to 160 GHz) applications." The reason for this was that some requirements of that 2005/2006 challenge have in the meantime been met, and on the other hand side the importance of extending simulation up to system level (e.g., SoC, SiP) has strongly increased. Furthermore, the impact of process variations up to circuit level had to be included. These and some other new aspects lead to a considerable shift in scope between the old and the new challenge. Second, the 2005/2006 long-term challenge "Prediction of dispersion of circuit parameters" has been pulled in to short-term, and its various aspects been extended and distributed there across the short-term challenges "Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability" (where variability is now explicitly included), "Ultimate nanoscale device simulation capability," and as already mentioned "Circuit element and system modeling for high frequency (up to 160 GHz) applications." The reason was that the impact of variability and fluctuations has in the meantime developed to a problem to be tackled quickly in order to provide solutions in time for the upcoming technology generations which could be critically effected by these effects. Linked with this, the former short-term challenge on "Lithography simulation including NGL" has been separated into a short-term one "Lithography simulation including EUV" and its long-term counterpart "NGL simulation," which deals with the favorite non-optical and non-EUV techniques. Besides this, some updates were implemented on several other challenges, and the short-term challenges were put in a logical order which starts with lithography simulation and extends until circuit element and system modeling, without prioritizing among these six challenges.

The development of the technological capabilities and the requirements of the focus ITWGs, especially PIDS, FEP, Lithography and interconnect have resulted in many changes in the details of the Modeling and Simulation requirements, see the respective tables. Furthermore, during the preparation of these tables several topics where identified where results were already requested for 2005 or 2006, but sufficient research could not be carried out around the world due to lack of resources. In turn, were still needed these topics again show up in the current requirement tables. Concerning the main research areas requested, for Front End Process Modeling both continuum diffusion and activation models on one hand side and atomistic modeling for activation and diffusion on the other hand side are now separate main items, where etching and deposition has been combined into one line. The requirements for the modeling of novel devices have been extended beyond memories. Large area lithography simulation now includes TCAD-based inverse lithography modeling.

The development of new modeling capability generally requires long-term research, and increasingly interdisciplinary activities, which can be carried out best in an academic or a laboratory setting. For this reason, a vigorous research effort at universities and independent research institutes is a prerequisite for success in the modeling area, together with a close cooperation with industry, along the simulation food chain mentioned above. Because the necessary basic work generally needs significant development time, it is vital that adequate research funds will be made available in a timely manner in order to address the industry's future critical needs.

DIFFICULT CHALLENGES

The difficult challenges highlighted in Table ITWG15 are those Modeling and Simulation requirements which on one hand must be met in time to support the high-level progress of the roadmap and on the other hand are most critical to fulfill due to their technical difficulty and the R&D resources needed. Additionally, it should be noted that a key difficult challenge present across all the modeling areas is that of experimental validation. This challenge is especially difficult because for most processes many physical effects interact with each other and must be appropriately separated by well-selected experiments, in order to be able to develop predictive models and not simply fit experimental data. As devices shrink and new materials are introduced into the technology arena, new and enhanced analytical techniques are vital that can extract the necessary information for this model development and evaluation validation from the experiments. This critical need is mentioned as a cross-cut item with the Metrology ITWG.

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Table ITWG15 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Lithography simulation including EUV	Experimental verification and simulation of ultra-high NA vector models, including polarization effects from the mask and the imaging system
	Models and experimental verification of non-optical immersion lithography effects (e.g., topography and change of refractive index distribution)
	Simulation of multiple exposure/patterning
	Multi-generation lithography system models
	Simulation of defect influences/defect printing
	Optical simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including extensions for inverse lithography
	Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects and ultra-high NA effects (oblique illumination)
	Predictive resist models (e.g., mesoscale models) including line-edge roughness, etch resistance, adhesion, mechanical stability, and time-dependent effects in multiple exposure
	Resist model parameter calibration methodology (including kinetic and transport parameters)
	Simulation of ebeam mask making
	Simulation of directed self-assembly of sublithography patterns
	Modeling lifetime effects of equipment and masks
Front-end process modeling for nanometer structures	Diffusion/activation/damage/stress models and parameters including SPER and millisecond processes in Si-based substrate, that is, Si, SiGe:C, Ge, SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers
	Modeling of epitaxially grown layers: Shape, morphology, stress
	Modeling of stress memorization (SMT) during process sequences
	Characterization tools/methodologies for ultra shallow geometries/junctions, 2D low dopant level, and stress
	Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
	Efficient and robust 3D meshing for moving boundaries
	Front-end processing impact on reliability
Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-)products, rates ...), and simplified but physical models for complex chemistry and plasma reaction
	Linked equipment/feature scale models (including high-κ metal gate integration, damage prediction)
	Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
	Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
	Efficient extraction of impact of equipment- and/or process induced variations on devices and circuits, using process and device simulation
Ultimate nanoscale device simulation capability	Methods, models and algorithms that contribute to prediction of CMOS limits
	General, accurate, computationally efficient and robust quantum based simulators including fundamental parameters linked to electronic band structure and phonon spectra
	Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
	Models (including material models) to investigate new memory devices like MRAM, PRAM, etc.
	Gate stack models for ultra-thin dielectrics
	Models for device impact of statistical fluctuations in structures and dopant distribution
	Efficient device simulation models for statistical fluctuations of structure and dopant variations and efficient use of numerical device simulation to assess the impact of variations on statistics of device performance
	Physical models for novel materials, e.g., high-k stacks, Ge and compound III/V channels …: Morphology, band structure, defects/traps...
	Reliability modeling for ultimate CMOS
	Physical models for stress induced device performance

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Table ITWG15 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical, thermodynamic and electronic properties of low κ, high κ, and conductors for efficient on-chip and off-chip including SIP layout and power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension Model effects which influence reliability of interconnects/packages including 3D integration (e.g., stress voiding, electromigration, fracture, piezoelectric effects) Models to predict adhesion on interconnect-relevant interfaces Simulation of adhesion and fracture toughness characteristics for packaging and die interfaces Models for electron transport in ultra fine patterned interconnects
Circuit element and system modeling for high frequency (up to 160 GHz) applications	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies and package: - possibly consisting of different technologies, - covering and combining different modeling and simulation levels as well as different simulation domains Scalable active component circuit models including non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling Scalable passive component models for compact circuit simulation, including interconnect, transmission lines, RF MEMS switches, … Physical circuit element models for III/V devices Computer-efficient inclusion of variability including its statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently Efficient building block/circuit-level assessment using process/device/circuit simulation, including process variations
Difficult Challenges < 22 nm	*Summary of Issues*
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: 1) Gate stacks: Predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. 2) Models for novel integrations in 3D interconnects including airgaps and data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties 3) Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. Modeling-assisted metrology. 4) Accumulation of databases for semi-empirical computation.
Nano-scale modeling for Emerging Research Devices including Emerging Research Materials	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), quantum dots, molecular electronics, multiferroic materials and structures, strongly correlated electron materials) Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …)
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling. Physical design tools for integrated electrical/optical systems
NGL simulation	Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects and impact on LER); heating and charging effects), including impact on device characteristics (e.g., due to local crystal damage by electron scattering or charging effects) Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

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OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) tables are created early in the Roadmap process and are used as the basis for initiating the activities of the International Technology Working Groups in producing their detailed chapters. These tables are also used throughout the renewal effort of the Roadmap as a means of providing synchronization among the TWGs by highlighting inconsistencies between the specific tables. The process to revise the tables includes increasing levels of cross-TWG and international coordination and consensus building to develop underlying models of trends and to reach agreement on target metrics. As a result, the ORTC tables undergo several iterations and reviews.

The metric values of the ORTC tables can be found throughout the Roadmap in greater detail in each Technology Working Group chapter. The information in this section is intended to highlight the current rapid pace of advancement in semiconductor technology. It represents a completion of the revision update and renewal work that began in 2006. Additionally, the ORTC Glossary has been updated in 2007.

OVERVIEW OF 2007 REVISIONS

DEFINITIONS

As noted above, the Overall Roadmap Technology Characteristics tables provide a consolidated summary of the key technology metrics. Please note that, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds 10,000 units per month of ICs from a manufacturing site using "production tooling." Furthermore, a second company must begin production within three months (see Figure 2). To satisfy this timing definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility.

It was mentioned in the Introduction section of the ITRS Executive Summary, but it is worth repeating, that there continues to be confusion in the industry regarding individual company public press announcements of their "node" progress and timing, which may or may not align with the ITRS definitions and specific targets.

During the 2003 ITRS development, an attempt was made to reconcile the many published press releases by Logic manufacturers referencing "90 nm" technology "node" manufacturing in 2003. Since the contacted metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM stagger-contacted M1 half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that some of the public citations were in reference to an "indexed" technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance). Some companies also referenced the timing for doubling of functionality on a given product (for example the doubling of logic gates or memory bits) as a measure of "node" advancement. This approach of measuring technology progress complicates the "node" relationship, because density improvements can be accomplished by design improvements added along with linear lithographic feature size reduction.

Additional confusion has developed due to the technology "node" references in Flash memory product announcements, and Flash technology is receiving increased emphasis in both the 2005 and 2007 ITRS. For example, Flash product cell density is defined by the un-contacted poly-silicon (poly) interconnect half-pitch, rather than a metal 1 (M1) half-pitch (the key feature which drives density in DRAM and MPU and ASIC products). Also, very aggressive Flash memory Cell Area Factor (see Glossary) improvements have been added by Flash cell designers in order to aggressively reduce costs and meet the rapidly ramping demand for non-volatile memory (NVM) storage.

The International Roadmap Committee (IRC) decided in the 2007 ITRS roadmap that the best way to minimize confusion between the ITRS and individual company public announcements is to continue the separate tracking of the various technology trend drivers by product—DRAM, MPU/ASIC, and Flash. As mentioned earlier, the MPU/ASIC and DRAM product half-pitches are now both defined by a common reference to the M1 stagger-contact, while the Flash NVM

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product is referenced to un-contacted poly dense parallel lines (refer to Figure 1). Individual TWG tables will utilize the product table header line items that are most representative of the technology trend drivers for each table.

Due to the new emphasis on separate product trend tracking, no common product technology header is required – only the year of production of the referenced technology line item. In the 2007 ITRS, the technology trends and the functional (transistors, bits, logic gates) or characteristic (speed, power) performance associated with the individual product groups (DRAM, Flash, MPU, ASIC) will be emphasized. Individual company references that wish to compare to the ITRS must now reference the specific product technology trend line item, as further defined by the ITRS Executive Summary and Glossary.

Individual product technology trends continue to be monitored, and the most recent TWG survey update is indicating that the DRAM historical trend may be tracking closer to the ITRS MPU trend. However, the 2007 DRAM M1 half-pitch targets were left unchanged in the 2007 ORTC Tables. The DRAM trends and M1 targets will be investigated further in 2007 and reported in the 2008 Update, but additional details from the latest survey are included in the 2007 PIDS chapter. Some minor inconsistencies may appear in the 2007 and 2008 years, and the 2007 ITRS targets for those years are may be slightly more aggressive than actual industry performance. All targets from 2009 and beyond, the timing which influences the Grand Challenges and Potential Research and Development solutions are consistent with the latest survey results.

In the most recent Flash technology survey, the overall lithography resolution now appears to be driven at the most leading edge by a feature size trend from Flash product. For example, as is described in additional detail below, the uncontacted polysilicon half-pitch of FLASH memories is now projected to be ahead of DRAM stagger-contacted M1 half-pitch by two years by 2008. A two-year lead by the Flash uncontacted polysilicon half-pitch is considered equivalent (in lithographic processing difficulty) to a one-year lead of the DRAM stagger-contacted M1 half-pitch, and this additional timing lead increase is therefore causing Flash memory technology to drive leading-edge lithography. Please see the Glossary section for additional detail on the "Year of Production" timing definition.

The 2007 ITRS table technology trend targets have now been completely annualized from 2007 through the 15-year Roadmap horizon in 2022. However, per previously established IRC guidelines, the 2007 ITRS retains the definition of a technology trend cycle time as the period of time to achieve a significant advancement in the process technology. To be explicit, a technology trend cycle time advancement continues to be defined as the period of time to achieve an approximate 0.71× reduction per cycle (precisely 0.50× per two cycles). Refer to Figures 5 and 6.

Please note from the 2007 ITRS ORTC Table 1a and 1b, that the timing of a technology cycle remains different for a particular product. For example, the DRAM stagger-contact half-pitch M1 in the 2007 ITRS is still forecast to be on a 0.71×/3-years (0.50×/6-years) timing cycle from the historical 2004/90 nm actual (after being on a two-year timing cycle pace from the 2000/180 nm actual through 2004/90nm). The DRAM 3-year cycle is presently forecast to continue on a 3-year cycle through the 2022/11 nm target. The annual multiplier for the three-year cycle timing is 0.8909×/year, which is used to calculate the interim annual trend targets (examples: 2009/50 nm, 2020/14 nm).

After taking into account the available industry data and ITWG and IRC inputs, consensus was reached on the new Flash product technology timing model, based on the uncontacted polysilicon half-pitch definition. The Flash uncontacted polysilicon half-pitch is now set on a two-year cycle timing pace from 2000/180 nm through 2008/45 nm. At this point, it was determined by the Lithography ITWG that the Flash uncontacted polysilicon half-pitch, numerically two years "ahead" of the DRAM stagger-contacted M1 half-pitch, is now driving the technology process equipment being used to achieve that target. After 2008/45 nm, the Flash uncontacted polysilicon half-pitch is expected to turn to a three-year timing cycle, two years ahead of the DRAM trend, and would extend to 2022/9 nm on an annual basis.

As noted above, the MPU (and high-performance ASIC) Product Trend cycle timing was changed in the 2005 ITRS to be based on the same stagger-contact M1 half-pitch definition as DRAM. After analysis of historical data and consensus agreement by the ITWGs and IRC, the MPU M1 half-pitch was set on a 2.5-years (0.50×/5-years) cycle timing pace from the historical 2000/180 nm actual point through 2010/45 nm. At the 2010/45 nm point, it was decided that the MPU M1 targets would "catch up" and become equal to the DRAM M1 cycle timing targets (3-year timing cycle) through the end of the roadmap in 2022.

The MPU (and high-performance ASIC) final physical gate-length (phGL) targets remain unchanged from the 2003 ITRS, in which the timing was set at a two-year cycle (0.5×/4-years; 0.8409×/year) from 1999 through the 2005/32 nm point, and then the trend targets revert to a three-year timing (0.5×/6 years; 0.8909/year) cycle through the end of the Roadmap to 2022/4.5 nm. The Lithography and FEP ITWGs continue with their agreement on a new ratio (1.6818× multiplier above the physical gate length) between the final physical gate length, which includes etch, and the printed gate length targets.

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The low-operating-power ASIC gate length targets were established by the PIDs ITWG, and were placed two years behind the MPU (and high-performance ASIC) printed gate length and physical gate length targets.

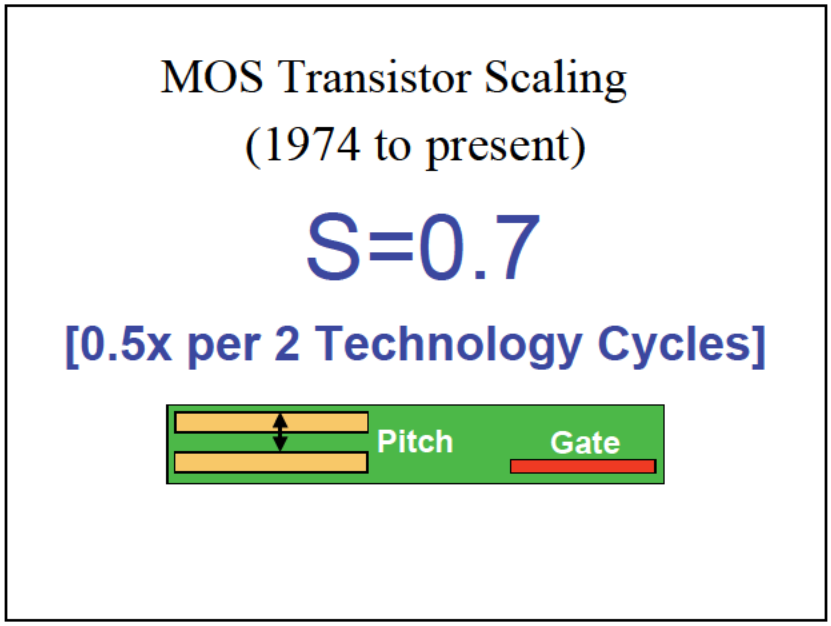


Figure 5 MOS Transistor Scaling—1974 to present

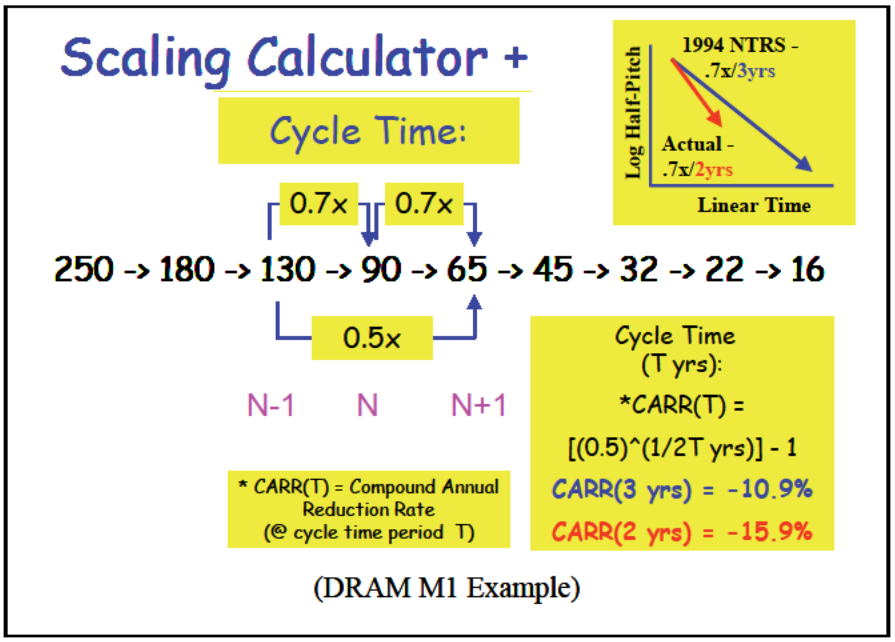


Figure 6 Scaling Calculator

ROADMAP TIMELINE

The 2007 edition of the Roadmap maintains a 15-year projection, from 2007 as a reference year and through 2022. The timing trends of the future technology pace of the DRAM product still represents the leading edge for stagger-contacted M1 half-pitch, and is forecast to return to the three-year cycle (three years between 0.71× reduction of the feature size)

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after 90nm/2004, unchanged from the 2003 edition. From surveys updates by the PIDS TWG, the 90 nm DRAM half-pitch began production ramp in 2004, on the completion of customer product qualification, which was made an explicit requirement of the "Production" definition for DRAM product for the 2003 ITRS.

In the 2001 ITRS, the 130 nm DRAM product M1 half-pitch was pulled in an additional year (from 2002 in the 1999 ITRS to 2001), anticipating a continuation of an observed historical two-year technology cycle calculated from 350 nm/1995, 250 nm in 1997, 180 nm in 1999). Data provided by DRAM manufacturers in 2003, which was based upon the more rigorous customer-product-qualified production ramp, indicated that the actual production ramp timing was as follows: 350 nm/1995, 250 nm/1998, 180 nm/2000 and 130 nm/2002. This new data indicates a two-year cycle timing, but delayed one year from the original 2001 ITRS timing. Data gathered on actual DRAM product ramped in the 2004 PIDS member surveys confirmed the two-year cycle step between 130 nm/2002 and 90 nm/2004. Although there was the possibility of a continuation of this new delayed two-year cycle trend, the 2004 DRAM product manufacturer consensus, confirmed by the PIDS 2004 survey update, continued to project a three-year timing cycle (0.71× reduction) for DRAM stagger-contacted M1 half-pitch throughout the 2007–2022 Roadmap period, as illustrated in Figure 7. As mentioned above, the most recent PIDS DRAM survey work has indicated that DRAM technology pace may be relaxed to be closer to the MPU M1 half-pitch 2.5-year cycle numbers. These survey recommendations will be continue to be evaluated for revision of the 2008 ITRS Update tables.

Also mentioned above, the DRAM interconnect half-pitch will no longer continue to be used as a representative feature of leading-edge semiconductor manufacturing technology for defining the achievement of a technology cycle (0.71× reduction of the feature size). In fact, the Flash uncontacted polysilicon half-pitch feature is now acknowledged as leading the DRAM M1 targets numerically by two years, and now is now the most leading driver of leading-edge technology manufacturing. Similarly, as mentioned, the lagging MPU and ASIC M1 stagger-contacted M1 interconnect half-pitches are running at a faster 2.5-year cycle pace and are presently expected to catch up and remain equal to the DRAM half-pitch in 2010/45 nm. With the new product-oriented focus since the 2005 ITRS, all product technology trends will be monitored, and any of the product trends may accelerate further and begin to drive the industry research and the equipment and materials supplier development at the leading edge. See Figure 7.

ROUNDED TREND NUMBERS

Using 180 nm DRAM product half pitch in the year 2000 as the calculation standard for trends, the 2007 ITRS now includes a correction of the past "rounding" convention for the technology cycle trend target. The actual calculated mathematical trend data (used for model calculations in the ORTC and TWG tables) reduces by 50% every other technology cycle, resulting in actual versus rounded number targets comparison below, starting from 350 nm in 1995, as follows in Table C.

Table C Rounded versus Actual Trend Numbers (DRAM Product Trend Example)

YEAR OF PRODUCTION	1995	1998	2000	2002	2003	2004	2006	2007	2009	2010	2012	2013	2015	2016	2018	2019	2022
Calculated Trend Numbers (nm)	**360**	**255**	**180**	**127.3**	**101**	**90**	**71.4**	**63.6**	**50.5**	**45**	**35.7**	**31.8**	**25.3**	**22.5**	**17.9**	**15.9**	**11.3**
ITRS Rounded Numbers (nm)	**350**	**250**	**180**	**130**	**100**	**90**	**70**	**65**	**50**	**45**	**36**	**32**	**25**	**22**	**18**	**16**	**11**

Note the new rounding corrections become more critical as the industry moves into the two-digit data cycles of the new nanotechnology (sub-100 nm) era. Please note also that some regions, for their own legacy publication consistency, will retain their right to continue to track the previous technology generations beginning with 100 nm/2003. Starting from 100 nm in 2003 will result in "milestones" that are targeted one year earlier than the present 2003 roadmap convention (example: 70 nm/2006; 50 nm/2009; 36 nm/2012; 25 nm/2015, etc.). By consensus of the IRC both number sets are available for long-term calculations, since the original 2001 ITRS long-term columns were retained (2010/45 nm; 2013/32 nm; 2016/22 nm), and new columns (2012/36 nm; 2015/25 nm; 2018/18 nm; 2021/13 nm) are now annualized and included as columns.

UPDATES TO THE ORTC

The MPU/ASIC M1 half-pitch continues to be defined as a stagger-contacted half-pitch the same as DRAM and both remain unchanged from the 2005 ITRS. , The Flash product half-pitch continues to be defined as an uncontacted

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polysilicon half-pitch, and has been revised from the 2005 ITRS by continuing the 2-year cycle trend through 2008/45 nm, then turning to a 3-year cycle through 2022..The *printed* MPU gate length received a major correction to more an aggressive starting point in the 2001 ITRS. In addition, a new *physical* gate length is being tracked that further reduces the bottom gate length dimension of a fully processed transistor. The physical gate length trends remain unchanged for the 2003 through the present 2007 ITRS, and are now forecast to continue scaling on a three-year cycle basis through the Roadmap horizon in 2022,. Refer to Figure 7.

The ORTC metrics are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to secure industry leadership. Thus, the highly competitive environment of the semiconductor industry quickly tends to make obsolete many portions of the ORTC metrics and, consequently, the Roadmap. Hopefully, the gathering and analysis of actual data, combined with the ITRS annual update process will provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the ITRS to the industry.

For example, the actual data and conference papers, along with company survey data and public announcements will be re-evaluated during the year 2008 ITRS Update process, and the possibility of a continued two-year node cycle in some of the individual product technology trends. As mentioned above, to reflect the variety of cycles and to allow for closer monitoring of future Roadmap trend shifts, it was agreed to continue the practice of publishing annual technology requirements from 2007 through 2015, called the "Near-term Years," and also annual requirements from 2015 through 2022, called the "Long-term years."

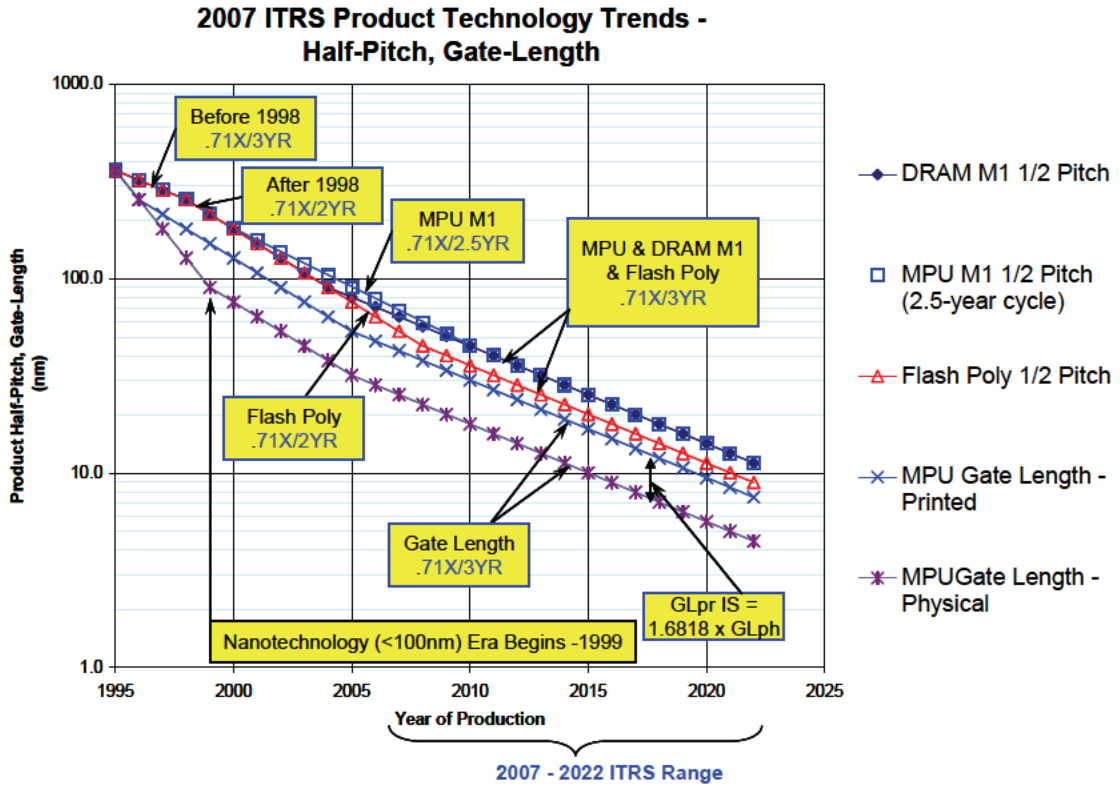


Figure 7 2007 ITRS—Half Pitch and Gate Length Trends

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PRODUCT GENERATIONS AND CHIP-SIZE MODEL

This section discusses "product generations" and their relationship to technology cycles, since, in the past, these terms have often been used interchangeably. However, the historically simple picture of a new DRAM product generation every three years (at 4× the previous density and based on an essentially new set of technology features) has become obsolete as a way to define technology cycle timing advancement. Continuing a practice that began with the 2005 ITRS, the 2007 ITRS edition bases the technology pace drivers on individual product technology trends. These product-based technology trends may move on different paces from one another, based upon market functionality and performance and affordability needs, as the leading-edge product evolution/shrink paths becomes more complex.

Historically, DRAM products have been recognized as the technology drivers for the entire semiconductor industry. Prior to the late-1990s, logic (as exemplified by MPU) technology moved at the same pace as DRAM technology, but after 2000/180 nm began moving at a slower 2.5-year technology cycle pace, while DRAM technology continued on the accelerated two-year pace. During the last few years, the development rate of new technologies used to manufacture microprocessors has continued on the 2.5-year pace, while DRAMs are now forecast to slow to a three-year cycle pace through the 2020 Roadmap horizon. By moving on the faster 2.5-year cycle pace, microprocessor products are closing the half-pitch technology gap with DRAM, and are now also driving the most leading-edge lithography tools and processes—especially for the capability to process the isolated-line feature of the printed and physical gate length. As noted above, the Flash technology, as defined by uncontacted polysilicon, has also accelerated to the point where it is now driving at the most leading edge.

However, several fundamental differences exist between the families of products. Due to strong commodity market economic pressure to reduce cost and increase fab output productivity, DRAM product emphasizes the minimization of the chip size. Therefore, development of DRAM technology focuses mainly on minimization of the area occupied by the memory cell. However, this pressure to minimize cell size is in conflict with the requirement to maximize the capacitance of the cell for charge storage performance, which puts pressure on memory cell designers to find creative ways through design and materials to meet minimum capacitance requirements while reducing cell size. In addition, to closely pack the highest number of DRAM cells in the smallest area requires minimization of cell pitch.

Microprocessors have also come under strong market pressure to reduce costs while maximizing performance. Performance is enabled primarily by the length of the transistor gate and by the number of interconnect layers. The 2007 ITRS teams have reached consensus on models for the required functionality, chip size, cell area, and density for the ORTC tables. The MPU product chip size tables continue to be similar to the DRAM model, with large introductory chip sizes that must shrink over time to achieve the affordable sizes. Additional line items communicate the model consensus, and the underlying model assumptions are included in the ORTC table notations.

Table 1a and 1b summarize the near and long-term technology trend metrics summarized above. For completeness, the ASIC/low power gate length trends are also included, and lag behind the leading-edge MPU in order to maximize standby and operating current drain. See the Glossary section for additional detail on the definition of the half-pitch and gate-length features. For each product generation, both the leading-edge ("at introduction") and the high-volume ("at production") DRAM products are included.

To summarize Figure 7, it should be noted that the long-term average annualized reduction rate of the DRAM contacted M1 half-pitch feature size is forecast to return to the three-year technology cycle pace after 2004/90 nm, which represents an approximately 11%/year (~30% reduction/three years). The previous (1998/250 nm–2004/90 nm) accelerated two-year cycle rate is approximately 16%/year reduction on an annual basis (~30% reduction/two years). As noted above the new Flash memory uncontacted polysilicon turns to the three-year pace in 2008 after crossing over the DRAM M1, and the MPU/ASIC M1 (generically referred to as MPU in graphs) catches up to DRAM M1 in 2010/45 nm, and returns to a three-year pace.

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Table 1a Product Generations and Chip Size Model Technology Trend Targets—Near-term Years

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
DRAM ½ Pitch (nm) (contacted)	65	57	50	45	40	36	32	28	25
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	68	59	52	45	40	36	32	28	25
MPU Printed Gate Length (nm) ††	42	38	34	30	27	24	21	19	17
MPU Physical Gate Length (nm)	25	23	20	18	16	14	13	11	10
ASIC/Low Operating Power Printed Gate Length (nm) ††	54	48	42	38	34	30	27	24	21
ASIC/Low Operating Power Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
Flash ½ Pitch (nm) (un-contacted Poly)(f)	54	45	40	36	32	28	25	22	20

Table 1b Product Generations and Chip Size Model Technology Trend Targets—Long-term Years

Year of Production	2016	2017	2018	2019	2020	2021	2022
DRAM ½ Pitch (nm) (contacted)	22	20	18	16	14	13	11
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	22	20	18	16	14	13	11
MPU Printed Gate Length (nm) ††	15	13	12	11	9	8.4	7.5
MPU Physical Gate Length (nm)	9	8	7	6.3	5.6	5.0	4.5
ASIC/Low Operating Power Printed Gate Length (nm) ††	19	17	15	13	12	11	9
ASIC/Low Operating Power Physical Gate Length (nm)	11	10	9	8	7	6.3	5.6
Flash ½ Pitch (nm) (un-contacted Poly)(f)	18	16	14	13	11	10	9

Notes for Tables 1a and 1b

†† MPU and ASIC gate-length (in resist) targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "physical" gate lengths may be reduced from the "as-printed" dimension. These physical gate-length targets are driven by the need for maximum speed performance in logic microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design chapter tables as needs that drive device design and process technology requirements.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

MPU Physical Gate Length targets are unchanged from the 2003 ITRS through the 2006 ITRS Update, but also included are the complete set of annualized Long-term targets through 2022. The printed gate length has been adjusted to reflect the agreement between the FEP and Lithography TWGs to use a standard factor, 1.6818, to model the relationship between the final physical gate length and the printed gate length, after additional processing is applied to that isolated feature.

MPU/ASIC M1 stagger-contact targets was accelerated to 90 nm in 2005 to reflect actual industry performance per the Interconnect ITWG recommendation, and a new consensus model technology cycle timing of 2.5 years (to 0.71× reduction) was applied through 2010, when the trend targets become equal to the DRAM stagger-contact M1 through 2022.

Numbers in the header are rounded from the actual trend numbers used for calculation of models in ITRS ORTC and ITWG tables (see discussion in the Executive Summary on rounding practices).

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Table 1c DRAM and Flash Production Product Generations and Chip Size Model—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
DRAM Product Table									
Cell area factor [a]	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af2] (um^2)	**0.024**	**0.019**	**0.015**	**0.012**	**0.0096**	**0.0077**	**0.0061**	**0.0048**	**0.0038**
Cell array area at production (% of chip size) §	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**
Generation at production §	**2G**	**2G**	**2G**	**4G**	**4G**	**4G**	**8G**	**8G**	**8G**
Functions per chip (Gbits)	**2.15**	**2.15**	**2.15**	**4.29**	**4.29**	**4.29**	**8.59**	**8.59**	**8.59**
Chip size at production (mm^2)§	**93**	**74**	**59**	**93**	**74**	**59**	**93**	**74**	**59**
Gbits/cm2 at production §	**2.31**	**2.91**	**3.66**	**4.62**	**5.82**	**7.33**	**9.23**	**11.63**	**14.65**
Flash Product Table									
Flash ½ Pitch (nm) (un-contacted Poly)(f)	**53.5**	**45.0**	**40.1**	**35.7**	**31.8**	**28.3**	**25.3**	**22.5**	**20.0**
Cell area factor [a]	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Cell area [Ca = af^2] (um^2)	**0.0115**	**0.0081**	**0.0064**	**0.0051**	**0.0041**	**0.0032**	**0.0026**	**0.0020**	**0.0016**
Cell array area at production (% of chip size) §	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**
Generation at production § SLC	**8G**	**8G**	**8G**	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**
Generation at production § MLC [2 bits/cell]	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**	**64G**	**64G**	**64G**
Generation at production § MLC [4 bits/cell]	**32G**	**32G**	**32G**	**64G**	**64G**	**64G**	**128G**	**128G**	**128G**
Functions per chip (Gbits) SLC	**8.59**	**8.59**	**8.59**	**17.18**	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**
Functions per chip (Gbits) MLC [2 bits/cell]	**17.18**	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**	**68.72**	**68.72**	**68.72**
Functions per chip (Gbits) MLC [4 bits/cell]	**34.36**	**34.36**	**34.36**	**68.72**	**68.72**	**68.72**	**137.44**	**137.44**	**137.44**
Chip size at production (mm^2)§ SLC	**143.96**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**
Chip size at production (mm2)§ MLC [2 bits/cell & 4 bits/cell]	**143.96**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**
***Bits**/cm^2 at production § SLC*	**5.97E+09**	**8.44E+09**	**1.06E+10**	**1.34E+10**	**1.69E+10**	**2.13E+10**	**2.68E+10**	**3.38E+10**	**4.25E+10**
Bits/cm2 at production § MLC [2 bits/cell]	**1.19E+10**	**1.69E+10**	**2.13E+10**	**2.68E+10**	**3.38E+10**	**4.25E+10**	**5.36E+10**	**6.75E+10**	**8.51E+10**
Functions per chip (Gbits) MLC [4 bits/cell]	**2.39E+10**	**3.38E+10**	**4.25E+10**	**5.36E+10**	**6.75E+10**	**8.51E+10**	**1.07E+11**	**1.35E+11**	**1.70E+11**

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Table 1d DRAM and Flash Production Product Generations and Chip Size Model—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
DRAM Product Table							
Cell area factor [a]	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af2] (um^2)	**0.0030**	**0.0024**	**0.0019**	**0.0015**	**0.0012**	**0.00096**	**0.00076**
Cell array area at production (% of chip size) §	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**	**56.08%**
Generation at production §	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**	**64G**
Functions per chip (Gbits)	**17.18**	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**	**68.72**
Chip size at production (mm^2)§	**93**	**74**	**59**	**93**	**74**	**59**	**93**
Gbits/cm2 at production §	**18.46**	**23.26**	**29.31**	**36.93**	**46.52**	**58.61**	**73.85**
Flash Product Table							
Flash ½ Pitch (nm) (un-contacted Poly)(f)	**17.9**	**15.9**	**14.2**	**12.6**	**11.3**	**10.0**	**8.9**
Cell area factor [a]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
Cell area [Ca = af^2] (um^2)	**0.0013**	**0.0010**	**0.00080**	**0.00064**	**0.00051**	**0.00040**	**0.00032**
Cell array area at production (% of chip size) §	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**	**68.35%**
Generation at production § SLC	**64G**	**64G**	**64G**	**128G**	**128G**	**128G**	**256G**
Generation at production § MLC [2 bits/cell]	**128G**	**128G**	**128G**	**256G**	**256G**	**256G**	**512G**
Generation at production § MLC [4 bits/cell]	**256G**	**256G**	**256G**	**512G**	**512G**	**512G**	**1024G**
Functions per chip (Gbits) SLC	**68.72**	**68.72**	**68.72**	**137.44**	**137.44**	**137.44**	**274.88**
Functions per chip (Gbits) MLC [2 bits/cell]	**137.44**	**137.44**	**137.44**	**274.88**	**274.88**	**274.88**	**549.76**
Functions per chip (Gbits) MLC [4 bits/cell]	**274.88**	**274.88**	**274.88**	**549.76**	**549.76**	**549.76**	**1099.51**
Chip size at production (mm^2)§ SLC	**128.26**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**	**128.26**
Chip size at production (mm2)§ MLC [2 bits/cell & 4 bits/cell]	**128.26**	**101.80**	**80.80**	**128.26**	**101.80**	**80.80**	**128.26**
***Bits**/cm^2 at production § SLC*	**5.36E+10**	**6.75E+10**	**8.51E+10**	**1.07E+11**	**1.35E+11**	**1.70E+11**	**2.14E+11**
Bits/cm2 at production § MLC [2 bits/cell]	**1.07E+11**	**1.35E+11**	**1.70E+11**	**2.14E+11**	**2.70E+11**	**3.40E+11**	**4.29E+11**
Functions per chip (Gbits) MLC [4 bits/cell]	**2.14E+11**	**2.70E+11**	**3.40E+11**	**4.29E+11**	**5.40E+11**	**6.80E+11**	**8.57E+11**

Notes for Tables 1c and 1d

§ DRAM Model—cell area factor (design/process improvement) targets are as follows

1999–2006/8× 2006-2022/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the last model 2005 ITRS timeframe refer to Figures 8 and 9 for bit size and bits/chip trends

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the latest DRAM consensus model changes for the 2007 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM product are delayed an additional year and now remains "flat" at less than 93 mm^2, about one third smaller than the MPU model. However, with the pull-in of the $6f^2$ "cell area factor" , the flat-chip-size model target still requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c, 1d).

In addition to the revisions noted above, the cell array efficiency (CAE – the Array % of total chip area) was change to 56.1% after 2006. Only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery, however, the CAE pull-in enables the production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

The Flash product model was also revised to extend the 2-year-cycle half-pitch to 2008, also targets an affordable (<145 mm^2) chip size and includes a doubling of functions (bits) per chip every technology cycle (three years after 2008) on an Inter-generation. Flash cells have reached a limit of the 4-design factor, so the reduction of the Flash single-level cell (SLC) size is paced by the uncontacted polysilicon (three-year cycle). However, the Flash technology has the ability to store and electrically access two bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half the size of an SLC product cell size; and the latest revision of the Flash model also includes the introduction of 4 bits/cell beginning 2010 (refer to Figures 8 and 9).

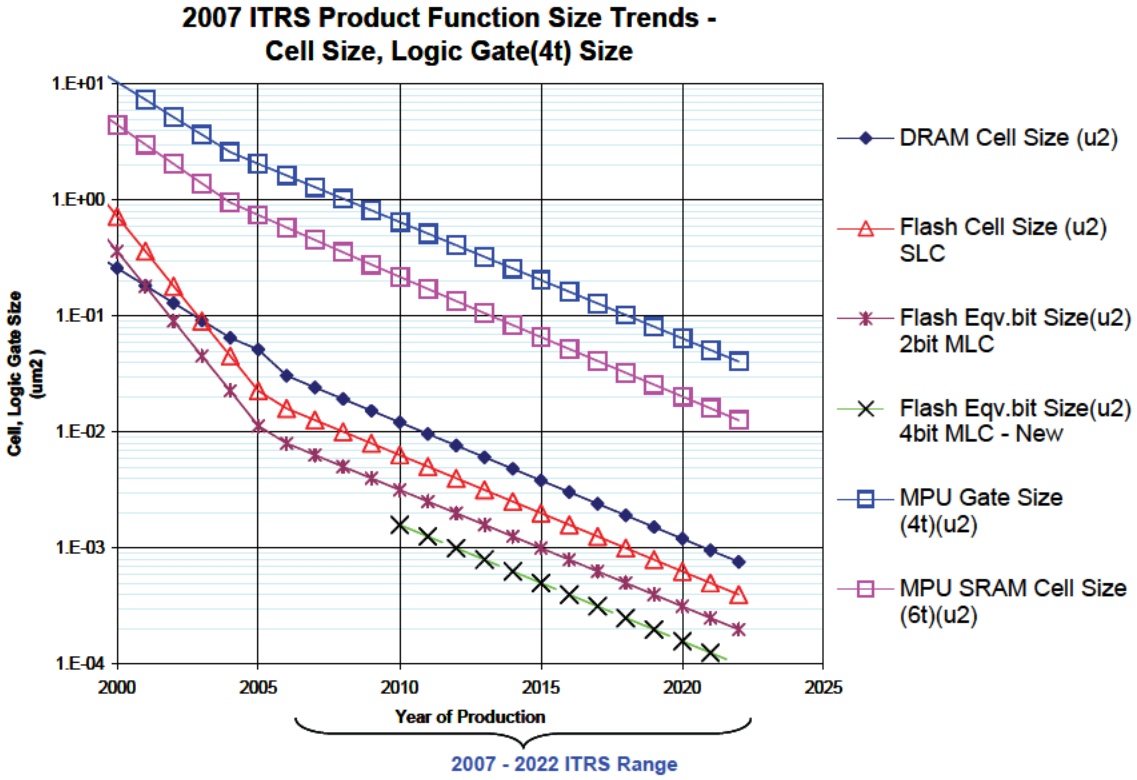


Figure 8 2007 ITRS Product Function Size Trends:
MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)]

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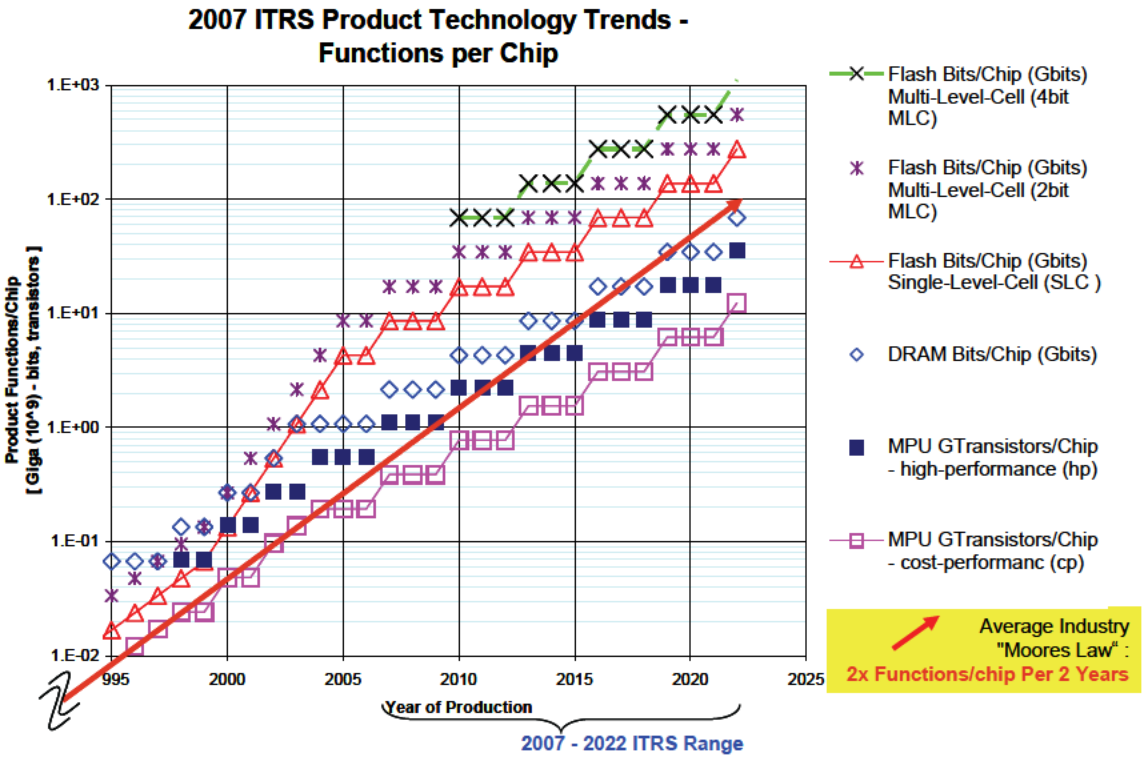


Figure 9 2007 ITRS Product Technology Trends:
Product Functions/Chip and Industry Average "Moore's Law" Trends

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Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Cell area factor [a]	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af^2] (um^2)	**0.024**	**0.019**	**0.015**	**0.012**	**0.0096**	**0.0077**	**0.0061**	**0.0048**	**0.0038**
Cell array area at introduction (% of chip size) §	**73.52%**	**73.76%**	**73.97%**	**74.16%**	**74.30%**	**74.47%**	**74.61%**	**74.70%**	**74.83%**
Generation at introduction §	**16G**	**16G**	**16G**	**32G**	**32G**	**32G**	**64G**	**64G**	**64G**
Functions per chip (Gbits)	**17.18**	**17.18**	**34.36**	**34.36**	**34.36**	**68.72**	**68.72**	**68.72**	**68.72**
Chip size at introduction (mm^2) §	**568**	**449**	**711**	**563**	**446**	**706**	**560**	**444**	**351**
Gbits/cm^2 at introduction §	**3.03**	**3.82**	**4.83**	**6.10**	**7.70**	**9.73**	**12.28**	**15.49**	**19.55**

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Cell area factor [a]	**6**	**6**	**6**	**6**	**6**	**6**	**6**
Cell area [Ca = af^2] (um^2)	**0.0030**	**0.0024**	**0.0019**	**0.0015**	**0.0012**	**0.00096**	**0.00076**
Cell array area at introduction (% of chip size) §	**74.93%**	**75.00%**	**75.09%**	**75.18%**	**75.27%**	**75.36%**	**75.45%**
Generation at introduction §	**128G**	**128G**	**128G**	**256G**	**256G**	**256G**	**512G**
Functions per chip (Gbits)	**137.44**	**137.44**	**137.44**	**274.88**	**274.88**	**274.88**	**549.76**
Chip size at introduction (mm^2) §	**557**	**442**	**350**	**555**	**440**	**349**	**553**
Gbits/cm^2 at introduction §	**24.67**	**31.11**	**39.24**	**49.50**	**62.44**	**78.77**	**99.36**

Notes for Tables 1e and 1f

§ DRAM Model—cell area factor (design/process improvement) targets are as follows

1999–2006/8× 2006-2022/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the last model 2005 ITRS timeframe refer to Figures 8 and 9 for bit size and bits/chip trends

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the latest DRAM consensus model changes for the 2007 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM product are delayed an additional year and now remains "flat" at less than 93 mm^2, about one third smaller than the MPU model. However, with the pull-in of the 6f^2 "cell area factor" , the flat-chip-size model target still requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c, 1d).

In addition to the revisions noted above, the cell array efficiency (CAE – the Array % of total chip area) was change to 56.1% after 2006. Only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery, however, the CAE pull-in enables the production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

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Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
SRAM Cell (6-transistor) Area factor ++	**97.5**	**100.7**	**104.1**	**107.8**	**106.7**	**105.7**	**104.8**	**104.1**	**103.4**
Logic Gate (4-transistor) Area factor ++	**279**	**292**	**306**	**320**	**320**	**320**	**320**	**320**	**320**
SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**
Logic Gate (4-transistor) Area efficiency ++	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
SRAM Cell (6-transistor) Area (um2)++	**0.45**	**0.35**	**0.28**	**0.22**	**0.17**	**0.13**	**0.11**	**0.084**	**0.066**
SRAM Cell (6-transistor) Area w/overhead (um2)++	**0.73**	**0.57**	**0.45**	**0.35**	**0.27**	**0.22**	**0.17**	**0.13**	**0.11**
Logic Gate (4-transistor) Area (um2) ++	**1.3**	**1.0**	**0.82**	**0.65**	**0.51**	**0.41**	**0.32**	**0.26**	**0.20**
Logic Gate (4-transistor) Area w/overhead (um2) ++	**2.6**	**2.1**	**1.6**	**1.3**	**1.0**	**0.82**	**0.65**	**0.51**	**0.41**
Transistor density SRAM (Mtransistors/cm^2)	**827**	**1,057**	**1,348**	**1,718**	**2,187**	**2,781**	**3,532**	**4,484**	**5,687**
Transistor density logic (Mtransistors/cm^2)	**154**	**194**	**245**	**309**	**389**	**490**	**617**	**778**	**980**
*Generation at introduction **	**p10c**	**p10c**	**p13c**	**p13c**	**p13c**	**p16c**	**p16c**	**p16c**	**p19c**
Functions per chip at introduction (million transistors [Mtransistors])	**773**	**773**	**1546**	**1546**	**1546**	**3092**	**3092**	**3092**	**6184**
Chip size at introduction (mm^2) ‡	**280**	**222**	**353**	**280**	**222**	**353**	**280**	**222**	**353**
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**276**	**348**	**438**	**552**	**696**	**876**	**1104**	**1391**	**1753**
*Generation at production **	**p07c**	**p07c**	**p07c**	**p10c**	**p10c**	**p10c**	**p13c**	**p13c**	**p13c**
Functions per chip at production (million transistors [Mtransistors])	**386**	**386**	**386**	**773**	**773**	**773**	**1546**	**1546**	**1546**
Chip size at production (mm^2) §§	**140**	**111**	**88**	**140**	**111**	**88**	**140**	**111**	**88**
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**276**	**348**	**438**	**552**	**696**	**876**	**1104**	**1391**	**1753**

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
SRAM Cell (6-transistor) Area factor ++	**102.8**	**102.2**	**101.7**	**101.3**	**100.9**	**100.5**	**100.1**
Logic Gate (4-transistor) Area factor ++	**320**	**320**	**320**	**320**	**320**	**320**	**320**
SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**
Logic Gate (4-transistor) Area efficiency ++	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
SRAM Cell (6-transistor) Area (um2)++	**0.052**	**0.041**	**0.032**	**0.026**	**0.020**	**0.016**	**0.01**
SRAM Cell (6-transistor) Area w/overhead (um2)++	**0.083**	**0.066**	**0.052**	**0.041**	**0.032**	**0.026**	**0.020**
Logic Gate (4-transistor) Area (um2) ++	**0.16**	**0.13**	**0.10**	**0.081**	**0.064**	**0.051**	**0.040**
Logic Gate (4-transistor) Area w/overhead (um2) ++	**0.32**	**0.26**	**0.20**	**0.16**	**0.13**	**0.10**	**0.08**
Transistor density SRAM (Mtransistors/cm^2)	**7,208**	**9,130**	**11,558**	**14,625**	**18,497**	**23,394**	**29,588**
Transistor density logic (Mtransistors/cm^2)	**1,235**	**1,555**	**1,960**	**2,469**	**3,111**	**3,920**	**4,938**
*Generation at introduction **	**p19c**	**p19c**	**p22c**	**p22c**	**p22c**	**p25c**	**p25c**
Functions per chip at introduction (million transistors [Mtransistors])	**6184**	**6184**	**12368**	**12368**	**12368**	**24736**	**24736**
Chip size at introduction (mm^2) ‡	**280**	**222**	**353**	**280**	**222**	**353**	**280**
Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**2209**	**2783**	**3506**	**4417**	**5565**	**7012**	**8834**
*Generation at production **	**p16c**	**p16c**	**p16c**	**p19c**	**p19c**	**p19c**	**p22c**
Functions per chip at production (million transistors [Mtransistors])	**3092**	**3092**	**3092**	**6184**	**6184**	**6184**	**12368**
Chip size at production (mm^2) §§	**140**	**111**	**88**	**140**	**111**	**88**	**140**
Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**2209**	**2783**	**3506**	**4417**	**5565**	**7012**	**8834**

Notes for Tables 1g and 1h

++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.

** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p04c, was introduced in 2002, but not ramped into volume production until 2004; similarly, the p07c, is introduced in 2004, but is targeted for volume production in 2007.*

‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/2000) plus Logic (20M transistors in 1 core in year 2000); and the combination of both SRAM and logic transistor functionality doubles every technology cycle. The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2022 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.

Refer to the Glossary for definitions.

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Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Logic (Low-volume Microprocessor) High-performance ‡									
Generation at Introduction	**p10h**	**p10h**	**p13h**	**p13h**	**p13h**	**p16h**	**p16h**	**p16h**	**p19h**
Functions per chip at introduction (million transistors)	**2212**	**2212**	**4424**	**4424**	**4424**	**8848**	**8848**	**8848**	**17696**
Chip size at introduction (mm^2)	**620**	**492**	**391**	**620**	**492**	**391**	**620**	**492**	**391**
Generation at production **	**p07h**	**p07h**	**p07h**	**p10h**	**p10h**	**p10h**	**p13h**	**p13h**	**p13h**
Functions per chip at production (million transistors)	**1106**	**1106**	**1106**	**2212**	**2212**	**2212**	**4424**	**4424**	**4424**
Chip size at production (mm^2) §§	**310**	**246**	**195**	**310**	**246**	**195**	**310**	**246**	**195**
High-performance MPU Mtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	**357**	**449**	**566**	**714**	**899**	**1133**	**1427**	**1798**	**2265**
ASIC									
ASIC usable Mtransistors/cm^2 (auto layout)	**357**	**449**	**566**	**714**	**899**	**1133**	**1427**	**1798**	**2265**
ASIC max chip size at production (mm^2) (maximum lithographic field size)	***858***	***858***	***858***	***858***	***858***	***858***	***858***	***858***	***858***
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**3,061**	**3,857**	**4,859**	**6,122**	**7,713**	**9,718**	**12,244**	**15,427**	**19,436**

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Logic (Low-volume Microprocessor) High-performance ‡							
Generation at Introduction	**p19h**	**p19h**	**p22h**	**p22h**	**p22h**	**p25h**	**p25h**
Functions per chip at introduction (million transistors)	**17696**	**17696**	**35391**	**35391**	**35391**	**70782**	**70782**
Chip size at introduction (mm^2)	**620**	**492**	**391**	**620**	**492**	**391**	**620**
Generation at production **	**p16h**	**p16h**	**p16h**	**p19h**	**p19h**	**p19h**	**p22h**
Functions per chip at production (million transistors)	**8848**	**8848**	**8848**	**17696**	**17696**	**17696**	**35391**
Chip size at production (mm^2) §§	**310**	**246**	**195**	**310**	**246**	**195**	**310**
High-performance MPU Mtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	**2854**	**3596**	**4531**	**5708**	**7192**	**9061**	**11416**
ASIC							
ASIC usable Mtransistors/cm^2 (auto layout)	**2854**	**3596**	**4531**	**5708**	**7192**	**9061**	**11416**
ASIC max chip size at production (mm^2) (maximum lithographic field size)	***858***	***858***	***858***	***858***	***858***	***858***	***1716***
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**24,488**	**30,853**	**38,873**	**48,977**	**61,707**	**77,746**	**195,906**

Notes for Tables 1i and 1j

** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p04c, was introduced in 2002, but not ramped into volume production until 2004; similarly, the p07c, is introduced in 2004, but is targeted for volume production in 2007.*

‡ MPU High-performance Model—High-performance MPU includes Level 2 (L2) on-chip SRAM (2048Kbyte in year 2000) plus Logic (25M transistors in 1 core in year 2000), and the combination of both SRAM and logic transistor functionality doubles every technology cycle. The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2022 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.

Refer to the Glossary for definitions.

CHIP-SIZE, LITHOGRAPHIC-FIELD, AND WAFER-SIZE TRENDS

Despite the continuous reduction in feature size of about 30% every two to three years, the chip size of first introductory-level leading-edge memory and logic product demonstrations in technical forums such as the IEEE International Solid State Circuits Conference (ISSCC) have continued to double every six years (an increase of about 12%/year). This increase in chip area has been necessary to accommodate 40%–60% more bits/capacitors/transistors per year in accordance with Moore's Law (historically doubling functions per chip every 1.5–2 years). However, to maintain the historical trend of reducing the leading-edge product cost/function by ~30%/year, it is necessary to continuously enhance equipment productivity, increase manufacturing yields, use the largest wafer size available, maintain or increase wafer and silicon area throughput, and, most of all, increase the number of functionality (transistors, bits, logic gates) and chips available on a wafer.

The increase in the gross number of functions and chips available on a wafer is primarily obtained by reducing the area of the functions and chips by means of a combination of smaller feature size (shrink/scaling) and product/process redesign (compaction). For instance, using the latest ITRS product chip size models, it is forecast that the introduction chip area of a cost-effective product generation [which doubles the inter-generation (generation-to-generation) functionality every two years] must remain as flat as possible. Furthermore, the area must be shrunk at an intra-generation (within a generation) annual reduction rate of 50% (the square of the .7× lithography reduction rate) during every technology cycle period, or faster when additional design-factor-related density improvement is available.

In order for affordable DRAM and Flash memory products to achieve virtually flat intra-generation chip-sizes, they must also maintain a cell area array efficiency ratio of 58–63% of total chip area. Historically, DRAM and Flash memory products have required reduction of cell area design factors (a) (cell area (Ca) in units of minimum-feature size (f) squared; $Ca = af^2$). The PIDS and FEP ITWGs have provided member survey data for the array efficiency targets, the cell area factors, and bits per chip. In addition, detailed challenges and needs for solutions to meet the aggressive cell area goals are documented in the Front End Processes chapter. Due to the importance of tracking/coordinating these new challenges, the DRAM and Flash memory cell area factors, the target cell sizes, and the cell array area percentage of total chip-size line items will continue to be tracked in ORTC Tables 1c, d, e, and f. (also refer to the Glossary for additional details).

Notably, the most recent survey data and publicly available announcements indicate that reduction rate of DRAM cell area factors for the 2007 ITRS models have accelerated, placing the 6 area factor in 2006 (versus 2008 in the 2005 ITRS). The area factor is still expected to remain flat at 6 through the 2020 ITRS horizon. In addition to the 6 factor pull-in, the survey pulled in the 56% array efficiency to begin in 2006. These gains in DRAM cell design efficiency and function density were traded off against a lower targeted production chip size starting point (100mm2 in 2007 versus 140mm2 in 2005) Therefore, the DRAM "Moore's Law" bits per chip targets have been delayed by 1 year, and continue to target 2× every three years in both the near term and long term. The 64 Gbit DRAM product now sits at the ITRS year 2022 horizon (refer to Function Size and Functions per Chip in Figures 8 and 9).

In the updated 2007 ORTC Flash product model, the function bit size is still calculated based upon it's the design factor and the also the critical feature scaling of the uncontacted polysilicon dense lines. The 2007 PIDS Flash survey indicated that the rapid 2-year scaling cycle will continue through 2008, however the single-level-cell physical design factor limit

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remains at 4. Therefore, the Flash model function (bit size) area reduction accelerated, and the Flash uncontacted polysilicon half-pitch now leads the DRAM stagger-contacted M1 half-pitch by two years. The Lithography TWG now believes that leading-edge Flash manufacturing technology is driving the most-leading-edge manufacturing, but is still using comparable processing equipment as leading-edge DRAM.

Flash single-level-cell (SLC) bit technology was thus able to drive quickly to a 76 nm uncontacted polysilicon half-pitch and a "4" design factor in 2005; and to continue the scaling reduction to 45nm in 2008, reducing SLC bit size to 0.008 um2, more than one-half the size of a DRAM cell that year (see Figure 8, 2005 ITRS Product Function Size Trends). This continued acceleration of Flash technology will enable the production of a 144 mm^2 8 Gbit SLC product in 2007, when DRAM product is still at 2 Gbit. Furthermore, Flash technology is able to create an electrical doubling of bits (multi-level-cell, or MLC) in the same area, resulting in a virtual doubling of bits per chip to 16 Gbits in the 140 mm^2 affordable first production chip size range. The PIDS Flash survey has also placed a quad-bit MLC beginning 2010 in production.

In the 2001 ITRS the Design ITWG improved the MPU chip size model to update with the latest transistor densities, large on-chip SRAM, and smaller target chip sizes. The Design ITWG added additional detail to the model, including transistor design improvement factors. The original Design ITWG model notes that design improvements occur at a slow rate in SRAM transistors and very little in logic gate transistors. Almost all the "shrink" and density improvement comes from lithography-enabled interconnect half-pitch scaling alone.

The present 2007 ITRS MPU model still "starts" in 2000/180 nm (versus original 1999/180 nm) chip size model is unchanged from the 2001 ITRS, and continues to reflect the additional competitive requirements for affordability and power management by targeting flat chip size trends for both high-performance MPUs (310 mm^2) and cost-performance MPUs (140 mm^2). Due to the MPU two-year-cycle half-pitch "catch-up phase" through the year 2004, the MPU products may be able to maintain flat chip sizes due to lithography improvements alone. However, after 2004, the inter-generation MPU chip size model, which is indexed to the ITRS technology cycles, can remain flat only by slowing the rate of on-chip transistors to double every technology generation. In a 2007 update, the MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends. Refer to Function Size and Functions per Chip in Figures 8 and 9.

Due to the forecasted return to a three-year technology cycle, the present MPU chip-size model slows the Moore's Law rate of on-chip transistors to 2× every three years. In order to maintain a flat chip size target and also return to the historical doubling every two years of on-chip functionality (transistors), MPU chip and process designers must add additional design/process improvements to the fundamental lithography-based scaling trends. The new target metrics of the MPU model are summarized in Tables 1g, h, i, and j.

To improve productivity, it is necessary to increase the output of good chips at each step in the fabrication process. The ability of printing multiple chips in a single exposure is a key productivity driver and is determined by the field size of the lithographic tool and the size and aspect ratio of the chips being printed on the wafer. In the past, lithography exposure field sizes doubled every other technology to meet the demand for increasing maximum introduction-level chip sizes. The result was the achievement of very large step-and-scan fields ($26 \times 33 = 858$ mm^2).

However, the Lithography ITWG indicates that maintaining the large field size under continued reduction of exposure features is increasing costs dramatically. Therefore, the Lithography ITWG is dependent upon the individual memory and logic product chip size models to drive the requirements for both the absolute maximum field size and also the more typical affordable field size ranges.

DRAM chip sizes have historically been the most appropriate driver of both the most difficult half-pitch exposures and also the affordable lithography field size range. In the 2007 ITRS chip-size model for DRAMs, the introduction-level chip size is targeted to be smaller than a 704 mm^2 lithography field size, fitting at least one introduction-level chip size within that field size. The latest 2007 ITRS production-level DRAM chip size model (less than 100 mm^2 flat target) fits five die within a 572 mm^2 field.

The combination of technology generation scaling and cell design improvements (A-factor reduction) accomplishes that goal, while also maintaining a goal of doubling on-chip bits every two years. However, as mentioned in the product chip size model discussions above, the slowing of DRAM design improvements, and the new 100mm2 affordable production chip size target, causes a requirement to add fewer on-chip bits to stay under the affordable chip size and lithography field size. This is accomplished in the present DRAM model by delaying the production bits/chip generations by 1 year, and slowing the Moore's Law bits/chip rate to 2×/ three years, as required. The data targets for the DRAM model are included

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in Tables 1c, d, e, and f. The new Flash production chip size model is also included in those tables, and still targets the Flash maximum affordable chip size at 140 mm^2.

The absolute maximum lithography field size is driven by the early introduction level chip sizes of high-performance MPUs and ASICs, which approach the maximum practical field size available from the Lithography TWG ($26 \times 33 = 858$ mm^2). It is anticipated that future mask magnification levels as high as 8× may reduce the maximum field size to one-fourth the present 858 $mm^{2,}$ reducing the maximum available area to less than 214 mm^2. The details surrounding the limitations of maximum field size and the mask magnification issue will be developed by the Lithography TWG in their chapter. The maximum Lithography field size is shown in Tables 2a and b.

The 2007 ITRS DRAM, MPU and Flash models depend upon achieving the aggressive DRAM, MPU, and Flash design and process improvement targets. If those targets slip, then pressure will increase to print chip sizes larger than the present roadmap, or further slow the rate of "Moore's-Law" on-chip functionality. Either of these consequences will result in a negative impact upon cost-per-function reduction rates—the classical measure of our industry's productivity-improvement and competitiveness.

With increasing cost-reduction pressures, the need for the 300 mm productivity boost will also increase in urgency, especially for leading-edge manufacturers, but the poor economy has created financial challenges and limited capital investment. The maximum substrate diameter in Tables 2a and b (and in additional detail in the FEP chapter) is consistent with the ramp of 300 mm capacity beginning 2001. Also, the first manufacturing capability for the next 1.5× wafer size conversion to 450 mm diameter is still not anticipated to be required until 2012 in the present Roadmap. However, should the other productivity-improvement drivers (lithography and design/process improvements) fail to stay on schedule, there would be a need to accelerate the use of increased wafer diameter, or an equivalent processing platform, as a productivity improvement.

The effects of future technology acceleration/deceleration and the timing of the next wafer generation conversion require the development and application of comprehensive long-range factory productivity and industry economic models. Such industry economic modeling (IEM) work is being sponsored and carried out jointly by Semiconductor Equipment and Materials International (SEMI) and SEMATECH. Most certainly, pre-competitive cooperation between the semiconductor supplier and manufacturer companies will be required to define the future technical and economic needs and to identify appropriate funding mechanisms for the required research and development.

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Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Lithography Field Size									
Maximum Lithography Field Size—area (mm^2)	**858**	**858**	**858**	**858**	**858**	**858**	**858**	**858**	**858**
Maximum Lithography Field Size—length (mm)	**33**	**33**	**33**	**33**	**33**	**33**	**33**	**33**	**33**
Maximum Lithography Field Size—width (mm)	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)									
Bulk or epitaxial or SOI wafer	**300**	**300**	**300**	**300**	**300**	**300 or 450**	**300 or 450**	**300 or 450**	**300 or 450**

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
Lithography Field Size							
Maximum Lithography Field Size—area (mm^2)	**858**	**858**	**858**	**858**	**858**	**858**	**858**
Maximum Lithography Field Size—length (mm)	**33**	**33**	**33**	**33**	**33**	**33**	**33**
Maximum Lithography Field Size—width (mm)	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	**450**	**450**	**450**	**450**	**450**	**450**	**450**

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PERFORMANCE OF PACKAGED CHIPS

NUMBER OF PADS AND PINS / PAD PITCH, COST PER PIN, FREQUENCY

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or bits (memory cells) for each product generation. Typically, the number of pads and pins necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases. (Refer to Tables 3a and b).

Additional power and ground connections to the chip are also necessary to optimize power management and to increase noise immunity. Based upon chip pad-count numbers supplied by the Test ITWG, logic products (MPUs and high-performance ASICs) both approach 4–6K pads over the ITRS period. The MPU products are forecast to increase the total number of pads through this period by nearly 50%, and the ASICs double the maximum number of pads per chip. The two product types also differ significantly in the ratio of power/ground pads. The MPU product pad counts typically have 1:3 signal I/O pads and 2:3 power and ground pads, or two power/ground pads for every signal I/O pad. Unlike MPUs, high-performance ASIC product pad counts typically include one power/ground pad for each signal I/O pad.

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Number of Chip I/Os (Number of Total Chip Pads)—Maximum									
Total pads—MPU unchanged	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**
Signal I/O—MPU (% of total pads)	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**
Power and ground pads—MPU (% of total pads)	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**
IS Total pads—ASIC High Performance unchanged	**4,400**	**4,400**	**4,600**	**4,800**	**4,800**	**5,000**	**5,400**	**5,400**	**5,600**
Signal I/O pads—ASIC high-performance (% of total pads)	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**
Power and ground pads—ASIC high-performance (% of total pads)	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**
Number of Total Package Pins—Maximum [1]									
Microprocessor/controller, cost-performance	**600–2140**	**600–2400**	**660–2801**	**660–2783**	**720-3061**	**720–3367**	**800–3704**	**800-4075**	**880–4482**
Microprocessor/controller, high-performance	**4000**	**4400**	**4620**	**4851**	**5094**	**5348**	**5616**	**5896**	**6191**
ASIC (high-performance)	**4000**	**4400**	**4620**	**4851**	**5094**	**5348**	**5616**	**5896**	**6191**

Notes for Tables 3a and 3b

[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by printed wiring board (PWB) technology and system cost. The highest pin count applications will as a result use larger pitches and larger package sizes. The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2 1 to 1 4.

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Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
Number of Chip I/Os (Number of Total Chip Pads)—Maximum							
Total pads—MPU unchanged	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**	**3,072**
Signal I/O—MPU (% of total pads)	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**	**33.3%**
Power and ground pads—MPU (% of total pads)	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**	**66.7%**
IS Total pads—ASIC High Performance unchanged	**6,000**	**6,000**	**6,200**	**6,200**	**6,200**	**6,840**	**6,840**
Signal I/O pads—ASIC high-performance (% of total pads)	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**
Power and ground pads—ASIC high-performance (% of total pads)	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**	**50.0%**
Number of Total Package Pins—Maximum [1]							
Microprocessor/controller, cost-performance	**880–4930**	**960-5423**	**960–5966**	**1050-6562**	**1050 - 7218**	**1155-7940**	**1155-8337**
Microprocessor/controller, high-performance	**6501**	**6826**	**7167**	**7525**	**7902**	**8297**	**8712**
ASIC (high-performance)	**6501**	**6826**	**7167**	**7525**	**7902**	**8297**	**8712**

Package pin count (Tables 3a and 3b) and cost-per-pin (Tables 4a and 4b), provided by the Assembly and Packaging ITWG, point out challenges to future manufacturing economics. Based upon the projected growth in the number of transistors/chip, it is forecast that the number of package pin/balls will continue to grow, while the cost/pin decreases. These trends make it more challenging for suppliers of packaging technologies to deliver cost-effective solutions, because the overall average cost of packaging will increase annually.

In the very competitive consumer electronics product environment (which is a focus end-product segment for characterizing Design and System-Driver Chapter Grand Challenges and Potential Solutions), prices for high-volume, high-tech products such as PCs and cell phones tend to remain flat or even decrease. These same high-tech products typically also deliver twice the performance every two years. This is the end-use market environment of the leading-edge semiconductor manufacturer, and it is the fundamental economic driver behind the ITRS economic requirement to reduce cost per function (bits, transistors) at an annual 30% or faster rate (2× functionality/chip at flat price every two years = 29%/year).

If future semiconductor component products must be targeted to maintain constant or decreasing prices and the average number of pins per unit increases while the average cost per pin decreases , then: the average packaging share of total product cost will continue to increase over the 15-year roadmap period; and

3. the ultimate result will be greatly reduced gross profit margins and limited ability to invest in R&D and factory capacity.

This conclusion is one of the drivers behind the industry trends to reduce the overall system pin requirements by combining functionality into systems-on-chip (SOC) and through the use of multi-chip modules (System-in-Package, i.e., SiP), bumped chip-on-board (COB), and other creative solutions.

In addition to the need to increase functionality while exponentially decreasing cost per function, there is also a market demand for higher-performance, cost-effective products. Just as Moore's Law predicts that functions-per-chip will double every 1.5–2 years to keep up with consumer demand, there is a corresponding demand for processing electrical signals at progressively higher rates. In the case of MPUs, processor instructions/second have also historically doubled every 1.5–2 years. However, in the latest 2007 ITRS, historical and forecast trends are suggesting a significant slowing in the rate of increase of on-chip frequency, to approximately only 8% growth per year or less. Performance increases accomplished historically by geometrical scaling (refer to Glossary) are now being provided through architecture and software improvements that enable the continued delivery of SOC, SIP, and system-level performance to customers while keeping power management under control.

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For MPU products, increased processing power, measured in millions of instructions per second (MIPs), is accomplished through a combination of "raw technology performance" (clock frequency) multiplied by "architectural performance" (instructions per clock cycle). The need for a progressively higher operational performance will continue to demand the development of novel process, design, and packaging techniques.

These considerations are reflected in Tables 4c and 4d, which include line items contributed by the Design TWG to forecast the maximum on- trends. The highest frequency obtainable in each product generation is directly related to the intrinsic transistor performance (on-chip, local clock). The difference between this "local" frequency and the frequency of signals traveling across the chip increases due to degradation of signal propagation delay caused by line-to-line and line-to-substrate capacitive coupling. Additional signal degradation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be the only viable way to eliminate any parasitic effect introduced by the package. To optimize signal and power distribution across the chip, it is expected that the number of layers of interconnect will continue to increase. As size downscaling of interconnect also continues, wider use of copper (low resistivity) and various inter-metal insulating materials of progressively lower dielectric constant (κ~2–3) will be adopted in the chip fabrication process. Multiplexing techniques will also be used to increase the chip-to-board operating frequency (off-chip).

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Chip Pad Pitch (micron)									
Pad pitch—ball bond [no update - deleted by A&P]	**30**	**30**	**25**	**25**	**25**	**20**	**20**	**20**	**20**
Pad pitch—wedge bond	**25**	**25**	**25**	**25**	**25**	**25**	**25**	**25**	**25**
Pad Pitch—area array flip-chip (cost-performance, high-performance)	**130**	**130**	**120**	**120**	**120**	**110**	**110**	**100**	**100**
Pad Pitch—2-row staggered-pitch (micron)	**45**	**45**	**40**	**40**	**35**	**35**	**35**	**35**	**35**
Pad Pitch—Three-tier-pitch pitch (micron)	**50**	**50**	**45**	**45**	**40**	**40**	**35**	**35**	**35**
Cost-Per-Pin									
Package cost (cents/pin) (Cost per Pin Minimum for Contract Assembly – Cost-performance) — minimum–maximum	**.69-1.19**	**.66-1.13**	**.63-1.70**	**.60-1.20**	**.57-.97**	**.54-.92**	**.51-.87**	**.48 -.83**	**.46 -.79**
Package cost (cents/pin) (Low-cost, hand-held and memory) — minimum–maximum	**.27-.50**	**.25-.48**	**.24-.46**	**.23-.44**	**.22-.42**	**.21-.40**	**.20-.38**	**.20-.36**	**.20 -.34**

Table 4b Performance and Package Chips: Pads, Cost—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Chip Pad Pitch (micron)							
Pad pitch—ball bond [no update - deleted by A&P]	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Pad pitch—wedge bond	**25**	**25**	**25**	**25**	**25**	**25**	**25**
Pad Pitch—area array flip-chip (cost-performance, high-performance)	**95**	**95**	**90**	**90**	**85**	**85**	**80**
Pad Pitch—2-row staggered-pitch (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Pad Pitch—Three-tier-pitch pitch (micron)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
Cost-Per-Pin							
Package cost (cents/pin) (Cost per Pin Minimum for Contract Assembly – Cost-performance) — minimum–maximum	**.44 -.75**	**.42 -.71**	**.39 -.68**	**.37 -.64**	**.35 -.61**	**.33-.58**	**0.32-0.55**

Package cost (cents/pin) (Low-cost, hand-held and memory) — minimum–maximum	**.20-.32**	**.20-.30**	**.20-.29**	**.20-.27**	**.20-.26**	**.19-.25**	**.19-.25**

Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Chip Frequency (MHz)									
On-chip local clock [1]	**4.700**	**5.063**	**5.454**	**5.875**	**6.329**	**6.817**	**7.344**	**7.911**	**8.522**
Maximum number wiring levels [3] ***[**]***	**11**	**12**	**12**	**12**	**12**	**12**	**13**	**13**	**13**

Table 4d Performance and Package Chips: Frequency On-chip Wiring Levels—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6*	*6*	*5*	*4*
Chip Frequency (MHz)							
On-chip local clock [1]	**9.180**	**9.889**	**10.652**	**11.475**	**12.361**	**13.315**	**14.343**
Maximum number wiring levels [3] ***[**]***	**13**	**14**	**14**	**14**	**14**	**15**	**15**

*[**] [Note ** The Interconnect TWG has deleted their "optional levels" from table 80a&b, therefore the ORTC "Maximum number wiring levels - maximum" line is deleted; also the "Maximum number wiring levels - minimum" is now just "Maximum number of wiring levels."*

Note for Tables 4c and 4d

[1] The on-chip frequency is based on the fundamental transistor delay (defined by the PIDS TWG), and an assumed maximum number of 12 inverter delays beginning 2007; after 2007, the PIDS model fundamental reduction rate of ~ -14.7% for the transistor delay results in an individual transistor frequency performance rate increase of ~17.2% per year growth. In the 2005 roadmap, the trend of the on-chip frequency was also increased at the same rate of the maximum transistor performance through 2022. Although the 17% transistor performance trend target is continued in the PIDS TWG outlook, the Design TWG has revised the long-range on-chip frequency trend to be only about 8% growth rate per year. This is to reflect recent on-chip frequency slowing trends and anticipated speed-power design tradeoffs to manage a maximum 200 watts/chip affordable power management tradeoff.

[2] The off-chip frequency, is defined by the Assembly and Packaging (A&P) model, and is available in the A&P chapter.

[3] The maximum number of interconnect wiring levels includes the optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

ELECTRICAL DEFECT DENSITY

The latest targets for electrical defect density of DRAM, MPU, and ASIC (necessary to achieve 83–89.5 % chip yield in the year of volume production) are shown in Tables 5a and b. The allowable number of defects is calculated by taking into account the different chip sizes based on the latest chip size model forecasts, as reported in Table 1 for DRAM and microprocessors. In addition, the data in the table are now reported only at the production-level of the product life-cycle. Other defect densities may be calculated at different chip sizes at the same technology by using the formula found in the Yield Enhancement chapter. The approximate number of masks for logic devices is included as an indicator of the ever-increasing process complexity.

Table 5a Electrical Defects—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
DRAM Overall Electrical D_0 (faults/m^2) at Critical Defect Size or Greater §	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**
MPU Overall Electrical D_0 (faults/m^2) at Critical Defect Size or Greater §§	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**
# Mask Levels—MPU	**33**	**35**	**35**	**35**	**35**	**35**	**37**	**37**	**37**
# Mask Levels—DRAM	**24**	**24**	**26**	**26**	**26**	**26**	**26**	**26**	**26**

Table 5b Electrical Defects—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
DRAM Overall Electrical D_0 (faults/m^2) at Critical Defect Size or Greater §	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**	**2437**
MPU Overall Electrical D_0 (faults/m^2) at Critical Defect Size or Greater §§	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**	**1395**
# Mask Levels—MPU	**37**	**39**	**39**	**39**	**39**	**39**	**39**
# Mask Levels—DRAM	**26**	**26**	**26**	**26**	**26**	**26**	**26**

Notes for Tables 5a and 5b

D_0 — defect density

§ DRAM Model—cell area factor (design/process improvement) targets are as follows

1999–2006/8× 2006-2022/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the last model 2005 ITRS timeframe refer to Figures 8 and 9 for bit size and bits/chip trends

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2022 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.

Refer to the Glossary for definitions.

POWER SUPPLY AND POWER DISSIPATION

The reduction of power supply voltage is driven by several factors—reduction of power dissipation, reduced transistor channel length, and reliability of gate dielectrics. As seen in Tables 6a and b, the value of the power supply voltage is now given as a range.

Selection of a specific V_{dd} value continues to be a part of the analysis undertaken to simultaneously optimize speed and power for an IC, leading to a range of usable power supply voltages in each product generation. Values of V_{dd} as low as 0.5 volts are not expected to be achieved by high-performance processors until beyond 2022. . The lowest V_{dd} target is still 0.5V in 2016 for the low operating power applications, but is targeted to drop to 0.45 volts in 2021.

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Maximum power trends (e.g., for MPUs) are presented in three categories—1) high-performance desktop applications, for which a heat sink on the package is permitted; 2) cost-performance, where economical power management solutions of the highest performance are most important; and 3) portable battery operations (now designated as the "Harsh" application category by the Assembly and Packaging TWG). In all cases, total power consumption continues to increase, despite the use of a lower supply voltage. The increased power consumption is driven by higher chip operating frequencies (significantly reduced in the 2007 roadmap from 17% CAGR to 8% CAGR), the higher interconnect overall capacitance and resistance, and the increasing gate leakage of exponentially growing and scaled on-chip transistors.

Table 6a Power Supply and Power Dissipation—Near-term Years

[1] Power will be limited more by system level cooling and test constraints than packaging

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Power Supply Voltage (V)									
Vdd (high-performance)	**1.1**	**1.0**	**1.0**	**1.0**	**0.95**	**0.90**	**0.90**	**0.90**	**0.80**
V_{dd} (Low Operating Power, high V_{dd} transistors)	**0.80**	**0.80**	**0.80**	**0.70**	**0.70**	**0.70**	**0.60**	**0.60**	**0.60**
Allowable Maximum Power [1]									
High-performance with heatsink (W)	**189**	**198**	**198**	**198**	**198**	**198**	**198**	**198**	**198**
Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation	**310**	**310**	**310**	**310**	**310**	**310**	**310**	**310**	**310**
Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation	**0.61**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**
Cost-performance (W)	**104**	**111**	**116**	**119**	**119**	**125**	**137**	**137**	**137**
Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation	**0.74**	**0.79**	**0.83**	**0.85**	**0.85**	**0.89**	**0.98**	**0.98**	**0.98**
Battery (W)—(low-cost/hand-held)	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**

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Table 6b Power Supply and Power Dissipation—Long-term Years

[1] Power will be limited more by system level cooling and test constraints than packaging

Year of Production	2016	2017	2018	2019	2020	2021	2022
DRAM ½ Pitch (nm) (contacted)	22	20	18	16	14	13	11
Flash ½ Pitch (nm) (un-contacted Poly)(f)	18	16	14	13	11	10	9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	22	20	18	16	14	13	11
MPU Physical Gate Length (nm)	9	8	7	6.3	5.6	5.0	4.5
Power Supply Voltage (V)							
Vdd (high-performance)	**0.80**	**0.70**	**0.70**	**0.70**	**0.65**	**0.65**	**0.65**
V_{dd} (Low Operating Power, high V_{dd} transistors)	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.45**	**0.45**
Allowable Maximum Power [1]							
High-performance with heatsink (W)	**198**	**198**	**198**	**198**	**198**	**198**	**198**
Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation	**310**	**310**	**310**	**310**	**310**	**310**	**310**
Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**
Cost-performance (W)	**151**	**151**	**151**	**151**	**151**	**151**	**151**
Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation	**1.08**	**1.08**	**1.08**	**1.08**	**1.08**	**1.08**	**1.08**
Battery (W)—(low-cost/hand-held)	**3**	**3**	**3**	**3**	**3**	**3**	**3**

COST

Tables 7a and 7b are dedicated to cost trends. The historical ability to reduce the leading-edge product manufacturing cost per function by an average 29% each year has represented one of the unique features of the semiconductor industry and is a direct consequence of the market pressure to continue to deliver twice the functionality on-chip every 1.5–2 years in an environment of constant or reducing prices. In support of this market cost reduction mandate, a continuously increasing amount of investment is needed for R&D and manufacturing capital. Even on a per-factory basis, the capital cost of manufacturing continues to escalate. Yet, the semiconductor industry has historically delivered two times as many functions per chip every 1.5–2 years with an approximately constant cost per cm2 of silicon. This technological and economic performance is the fundamental engine behind the growth of the semiconductor industry.

However, the customers in today's challenging economic and competitive market environment continue to resist even moderate increases in per unit cost, maintaining the pressure upon the semiconductor industry to slow the rate of doubling functions per chip (Moore's Law) in order to keep chip and unit costs under control. The semiconductor manufacturers had to seek a new model to deliver the same cost-per-function reduction requirements that have fueled industry growth. Consequently, the 1999 ITRS proposed a new model for achieving the required reduction: provide the customer twice the functionality every two years at constant cost targets. The 2001 and 2003, 2005, and now the 2007 ITRS models *all continue to use that model*, which results in 29% cost reduction of a function (bit, transistor, etc.). That rate of function cost reduction was achieved historically (prior to 1999) by delivering four times the functionality per chip every three years at 1.4× increase in cost per unit.

The 2007 ITRS DRAM and MPU cost models continue to use the need for that 29% cost-per-function productivity reduction rate as an economic driver of the industry. Therefore, that core cost-per-function trend has been used to set the INTRA-generation trends for the affordable cost/bit and cost/transistor for DRAM and microprocessors, respectively. Extrapolation of historical trends would indicate an "at introduction" affordable cost/bit of 5.3 microcents for 8 Gbit DRAMs in 2003. In addition, the historical trends indicate that, within a DRAM generation, a 45%/year reduction in cost/bit should be expected.[2] A corresponding analysis conducted from published data for microprocessors yields similar

[2] *McClean, William J., ed. Mid-Term 1994: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1994.*
McClean, William J., ed. Mid-Term 1995: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1995.

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results.[3] Therefore, the 29%/year target for reduction in affordable cost/transistor from generation to generation is also being used in the MPU model, along with the 45%/year reduction rate within the same generation.

The 2007 ITRS retains the original 2001 MPU chip size model. The Design ITWG updated the MPU model in the 2001 ITRS, based upon available data. At that time, the data indicated that logic transistor size is improving only at the rate of the lithography (0.7× linear, 0.5× area reduction every technology cycle). Therefore, in order to keep the MPU chip sizes flat, the number of transistors can be doubled only every technology cycle. The technology cycle rate is projected to be on a 2.5-year cycle from 180nm/2001 through 45nm/2010, and return to a three-year cycle after 2010. Therefore the transistors per MPU chip can double only every three years after 2004, unless increased chip size is allowed for specific applications which have markets that can afford the higher costs.

DRAM memory bit cell design improvements accelerated slightly, as reflected in the 2007 ITRS DRAM Chip Size Model targets. The "6" design factor, a 25% improvement over the "8" factor, was actually implemented in 2006, (versus 2008 in 2005 roadmap). However, the "5" design factor target, is still not anticipated, slowing the long-range cost-reduction productivity. However, the latest PIDS TWG survey of DRAM manufacturers has indicated that the target for the cell array efficiency percentage achieved 56% after 2006 (versus 2008 in 2005 roadmap). The combination of these recent model changes, along with the new goal of a more affordable starting production chip size (less than 100mm2 versus previous 140mm2) has delayed the bits/chip increase rate of DRAM by one year, and continued the rate of bits per chip at 2×/3 years. These DRAM model changes have pushed the 64 Gbit generation (introduction in 2013) to 2022 for production and moved the 128 Gbit DRAM (introduction 2016) beyond the present 2022 ITRS horizon. .

To compensate for slowing DRAM and MPU functions-per-chip, there will be increasing pressure to find alternative productivity enhancements from the "equivalent" productivity scaling benefits of chip, package, board, and system-level architecture and designs.

Even though the rate of increase of on-chip functionality could slow in the future, the amount of functions/chip is still growing exponentially, though at a slower rate. As the number of functions/chip continues to increase, it becomes increasingly difficult and, therefore, costly to test the final products. This issue is reflected in the escalating cost of testers. The number of tested pins (Tables 4a and 4b) is also increasing, which adds to the cost of the tester as well as the associated material and custom test fixtures that increase the total cost of ownership. Therefore, there will be an ongoing need for accelerated implementation of built-in-self-test and design-for-testability and design-for-manufacturability techniques within the time frame of the 2007 ITRS. Further discussion is detailed in the Test chapter.

Table 7a Cost—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*54*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Affordable Cost per Function ++									
DRAM cost/bit at (packaged microcents) at samples/introduction	**2.6**	**1.9**	**1.3**	**0.9**	**0.7**	**0.5**	**0.3**	**0.2**	**0.2**
DRAM cost/bit at (packaged microcents) at production §	**0.96**	**0.68**	**0.48**	**0.34**	**0.24**	**0.17**	**0.12**	**0.08**	**0.06**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**22.0**	**15.6**	**11.0**	**7.8**	**5.5**	**3.9**	**2.8**	**1.9**	**1.4**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**13.3**	**9.4**	**6.7**	**4.7**	**3.3**	**2.4**	**1.7**	**1.2**	**0.83**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**12.2**	**8.6**	**6.1**	**4.3**	**3.0**	**2.2**	**1.5**	**1.1**	**0.76**

[3] *a) Dataquest Incorporated. x86 Market: Detailed Forecast, Assumptions, and Trends. MCRO–WW–MT–9501. San Jose: Dataquest Incorporated, January 16, 1995.*
b) Port, Otis; Reinhardt, Andy; McWilliams, Gary; and Brull, Steven V. "The Silicon Age? It's Just Dawning," Table 1. Business Week, December 9, 1996, 148–152.

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Table 7b Cost—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
Flash ½ Pitch (nm) (un-contacted Poly)(f)	*18*	*16*	*14*	*13*	*11*	*10*	*9*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	**0.1**	**0.1**	**0.1**	**0.0**	**0.0**	**0.0**	**0.0**
DRAM cost/bit at (packaged microcents) at production §	**0.04**	**0.03**	**0.02**	**0.01**	**0.01**	**0.01**	**0.01**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**0.97**	**0.69**	**0.49**	**0.34**	**0.24**	**0.17**	**0.12**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**0.59**	**0.42**	**0.29**	**0.21**	**0.15**	**0.10**	**0.07**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**0.54**	**0.38**	**0.27**	**0.19**	**0.13**	**0.10**	**0.07**

Notes for Tables 7a and 7b

++ Affordable packaged unit cost per function based upon average selling prices (ASPs) available from various analyst reports less gross profit margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two to four years after introduction).

§ DRAM Model—cell area factor (design/process improvement) targets are as follows

1999–2006/8× 2006-2022/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the last model 2005 ITRS timeframe refer to Figures 8 and 9 for bit size and bits/chip trends

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the latest DRAM consensus model changes for the 2007 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM product are delayed an additional year and now remains "flat" at less than 93 mm^2, about one third smaller than the MPU model. However, with the pull-in of the 6f^2 "cell area factor" , the flat-chip-size model target still requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c, 1d).

In addition to the revisions noted above, the cell array efficiency (CAE – the Array % of total chip area) was change to 56.1% after 2006. Only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery, however, the CAE pull-in enables the production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2007 ITRS, the MPU model still includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target. . The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.

Refer to the Glossary for definitions.

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GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

2007 ITRS NEW DEFINITION ADDITION FOR "MORE MOORE" AND "MORE THAN MOORE" CONCEPTS

Moore's Law—An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

SCALING ("MORE MOORE")

a. *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.

b. *Equivalent Scaling* which occurs in conjunction with, and also enables, continued Geometrical Scaling, refers to 3-dimensional device structure ("Design Factor") Improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

FUNCTIONAL DIVERSIFICATION ("MORE THAN MOORE")

Functional Diversification refers to the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (*e.g.,* RF communication, power control, passive components, sensors, actuators) *to migrate from the system board-level* into a particular package-level (SiP) or chip-level (SoC) potential solution.

CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets. MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

Example: DRAM half pitches of 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, and 22 nm.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore's Law, there is a historically-based "corollary" to the "law," which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the

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cost-per-function reduction requirement. If functionality doubles only every three years, as suggested by consensus DRAM and MPU models of the 2005 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A Flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two bits of data in the same physical area.

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1 Mbytes/2001). Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71x/cycle period) generation.

High-performance MPU[4]—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example two cores at 25 Mt cores in 2002) with a large (example 4 Mbyte/2002) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip had increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is still required due to the new consensus 2007 ITRS forecast of cell-area-factor improvement to 6 by 2006, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the 2007 ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The 2003 ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology generation processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM

[4] *Note: The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.*

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products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology generation, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples.

Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, at least 10K/month) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 2 in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1 Gb/production, 4 G/introduction, plus 512 Mb/256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2003 ITRS, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 63% at the production level, and less than 50–55% for smaller previous generation shrunk die at the high-volume ramp level).

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DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E = 0.37\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.37e-6 mm^2/bit = 397 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half the size of an SLC product cell size and will also have a "virtual area factor" that is half of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

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Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology generation. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology generation. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology generation, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first production-qualified development manufacturing facilities.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

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FODLER 13

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2007 EDITION

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

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MASTAR Modeling Program Link

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PROCESS INTEGRATION, DEVICES, AND STRUCTURES

SCOPE

The *Process Integration, Devices, and Structures (PIDS)* chapter deals with overall IC process flow integration, with the main IC devices and structures, and with the reliability tradeoffs associated with new options. Physical and electrical requirements and characteristics are emphasized within PIDS, encompassing parameters such as physical dimensions, key device electrical parameters, including device electrical performance and leakage, and reliability criteria. The focus is on nominal targets, although statistical tolerances are discussed as well. Key technical challenges facing the industry in this area are addressed, and some of the best-known potential solutions to these challenges are discussed. The chapter is subdivided into the following major subsections: logic, memory (including both DRAM and non-volatile memory [NVM]), and reliability.

Main aims of the ITRS include identifying key technical requirements and challenges critical to sustaining the historical scaling of CMOS technology per Moore's Law and stimulating the needed research and development to meet the key challenges. The objective of listing and discussing potential solutions in this chapter is to provide the best current guidance about approaches that address the key technical challenges. However, the potential solutions list here is not comprehensive, nor are the solutions in the list necessarily the most optimal ones. Given these limitations, the potential solutions in the ITRS are meant to stimulate and not limit research exploring new and different approaches.

LOGIC

A major portion of semiconductor device production is devoted to digital logic. In this section, both high-performance and low-power logic (which is typically for mobile applications) are included, and detailed technology requirements and potential solutions are considered for both types. Key considerations are performance, power, and density requirements and goals. One key theme is continued scaling of the MOSFETs for leading-edge logic technology in order to maintain historical trends of improved device performance. This scaling is driving the industry toward a number of major technological innovations, including material and process changes such as high-κ gate dielectric, metal gate electrodes, etc., and in the long term, new structures such as ultra-thin body, multiple-gate MOSFETs (such as FinFETs). These innovations are expected to be introduced at a rapid pace, and hence understanding, modeling, and implementing them into manufacturing in a timely manner is expected to be a major issue for the industry

MEMORY

Logic and memory together form the predominant majority of semiconductor device production. The types of memory considered in this chapter are DRAM and non-volatile memory (NVM). The emphasis is on commodity, stand-alone chips, since those chips tend to drive the memory technology. However, embedded memory chips are expected to follow the same trends as the commodity memory chips, usually with some time lag. For both DRAM and NVM, detailed technology requirements and potential solutions are considered

The NVM discussion in this chapter is limited to devices that can be written and read many times; hence read-only memory (ROM) and one-time-programmable (OTP) memory are excluded. The current mainstream types of NVM currently is Flash, both NAND and NOR. There are serious issues with scaling that are dealt with at some length in the chapter. Other, non-charge-storage types of NVM are also considered, include ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase change RAM. For DRAM type memory, the key issue is dealing with increasing scaling difficulties, especially with ensuring very low levels of leakage.

RELIABILITY

Reliability is a critical aspect of process integration. Emerging technology generations require the introduction of new materials and processes at a rate that exceeds current capabilities for gathering information and generating the required database and models on new failure regimes and defects. Because process integration must then be performed without the benefit of extended learning, it will be difficult to maintain current reliability levels. Uncertainties in reliability can also lead to unnecessary performance, cost, and time-to-market penalties. These issues place difficult challenges on testing and wafer level reliability (WLR). Packaging interface reliability is particularly vulnerable to reliability problems because of new materials and processes, form factors, tighter lead and bond spacing, severe environments, adhesion, and customer manufacturing capability issues.

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DIFFICULT CHALLENGES

Table PIDS1a Process Integration Difficult Challenges—Near-term Years

Difficult Challenges ≥ 22 nm	*Summary of Issues*
1. Scaling of MOSFETs to the 22 nm technology generation	Scaling planar bulk CMOS will face significant challenges due to the high channel doping required, band-to-band tunneling across the junction and gate-induced drain leakage (GIDL), random doping variations, and difficulty in adequately controlling short channel effects. Also, keeping parasitics, such as series source/drain resistance with very shallow extensions and fringing capacitance, within tolerable limits will be significant issues. Implementation into manufacturing of new structures such as ultra-thin body fully depleted silicon-on-insulator (SOI) and multiple-gate (e.g., FinFET) MOSFETs is expected at some point. This implementation will be challenging, with numerous new and difficult issues. A particularly challenging issue is the control of the thickness and its variability for these ultra-thin MOSFETs, as well as control of parasitic series source/drain resistance for very thin regions.
2. With scaling, difficulties in inducing adequate strain for enhanced mobility.	With scaling, it is critically important to maintain (or even increase) the current significantly enhanced CMOS channel mobility attained by applying strain to the channel. However, the strain due to current process-induced strain techniques tends to decrease with scaling.
3. Timely assurance for the reliability of multiple and rapid material, process, and structural changes	Multiple major changes are projected over the next seven years, such as.: Material: high-κ gate dielectric, metal gate electrodes, lead-free solder Process: elevated S/D (selective epi) and advanced annealing and doping techniques Structure: ultra-thin body (UTB) fully depleted (FD) SOI, multiple-gate MOSFETs, multi-chip package modules It will be an important challenge to ensure the reliability of all these new materials, processes, and structures in a timely manner.
4. Scaling of DRAM and SRAM to the 22 nm technology generation	DRAM main issues with scaling—adequate storage capacitance for devices with reduced feature size, including difficulties in implementing high-κ storage dielectrics; access device design; holding the overall leakage to acceptably low levels; and deploying low sheet resistance materials for bit and word lines to ensure desired speed for scaled DRAMs. SRAM—Difficulties with maintaining adequate noise margin and controlling key instabilities and soft error rate with scaling. Also, difficult lithography and etch issues with scaling.
5. Scaling high-density non-volatile memory to the 22 nm technology generation	Flash—Non-scalability of tunnel dielectric and interpoly dielectric. Dielectric material properties and dimensional control are key issues. FeRAM—Continued scaling of stack capacitor is quite challenging. Eventually, continued scaling in 1T1C configuration. Sensitivity to IC processing temperatures and conditions. MRAM—Magnetic material properties and dimensional control. Sensitivity to IC processing temperatures and conditions

Table PIDS1b Process Integration Difficult Challenges—Long-term Years

Difficult Challenges<22 nm	*Summary of Issues*
6. Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs	Advanced non-classical CMOS (e.g., multiple-gate MOSFETs) with ultra-thin, lightly doped body will be needed to scale MOSFETs to 10 nm gate length and below effectively. Control of parasitic resistance and capacitance will be critical. To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, nanowires, carbon nanotubes, or other high transport channel materials (e.g., germanium or III-V thin channels on silicon) may be needed.
7. Dealing with fluctuations and statistical process variations in sub-11 nm gate length MOSFETs	Fundamental issues of statistical fluctuations for sub-10 nm gate length MOSFETs are not completely understood, including the impact of quantum effects, line edge roughness, and width variation.
8. Identifying, selecting, and implementing new memory structures	Dense, fast, low operating voltage non-volatile memory will become highly desirable Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness and attaining the very low leakage currents and power dissipation that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. See Emerging Research Devices section for more detail.
9. Identifying, selecting, and implementing novel interconnect schemes	Eventually, it is projected that the performance of copper/low-κ interconnect will become inadequate to meet the speed and power dissipation goals of highly scaled ICs. Solutions (optical, microwave/RF, etc.) are currently unclear. For detail, refer to ITRS Interconnect chapter.
10. Eventually, identification, selection, and implementation of advanced, non-CMOS devices and architectures for advanced information processing	Will drive major changes in process, materials, device physics, design, etc. Performance, power dissipation, etc., of non-CMOS devices need to extend well beyond CMOS limits. Non-CMOS devices need to integrate physically or functionally into a CMOS platform. Such integration may be difficult. See Emerging Research Devices sections for more discussion and detail.

DESCRIPTION OF PROCESS INTEGRATION, DEVICES, AND STRUCTURES DIFFICULT CHALLENGES

[1] Scaling of MOSFETs to the 22 nm technology generation—With scaling of planar bulk MOSFETs, the channel doping will need to be increased to undesirably high levels in order to gain adequate control of short-channel effects and to set the threshold voltage properly. As a result of the high channel doping, the mobility of holes and electrons will be reduced and the junction leakage due to band-to-band tunneling and gate-induced drain leakage will increase. Furthermore, due to the small total number of dopants in the channel of extremely small MOSFETs, the percent stochastic (random) variation in the number and location of the dopants will increase sharply, and this will sharply increase the statistical variability of the threshold voltage. Another challenge for highly scaled MOSFETs is reducing the parasitic series source/drain resistance (R_{sd}) to tolerable values with very shallow source and drain junction depth.

Due to the challenges with scaling planar bulk MOSFETs, advanced devices such as ultra-thin body fully depleted SOI MOSFETs and multiple-gate, particularly double-gate (DG) MOSFETs (e.g., FinFETs) are expected to be eventually implemented. Since such devices will typically have lightly doped channels and the threshold voltage will be controlled by the metal gate electrode's work function, the challenges associated with high channel doping and stochastic dopant variation in planar bulk MOSFETs will be avoided, but numerous new challenges are expected. Amongst the most critical of such challenges will be controlling the body thickness and its variability for these ultra-thin structures, and setting the metal gate electrode work function to its desired value. As with the planar bulk MOSFET, it will be highly challenging to reduce the parasitic series source/drain resistance (R_{sd}) to tolerable values, but here the ultra-thin body is an added difficulty.

With scaling, a common issue for both planar bulk and advanced MOSFETs is expected to be increased line edge roughness as a percentage of the gate length.

For high-performance logic, in the face of increased chip complexity and increasing transistor leakage current with scaling, chip static power dissipation is expected to become particularly difficult to control while at the same time meeting aggressive targets for performance scaling. Innovations in circuit design and architecture for performance management, as well as utilization of multiple transistors on chip, are needed to design chips with both the desired

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performance and power dissipation. The multiple transistors have different threshold voltages (V_t), with the low V_t, high leakage devices used mainly in the critical paths, and higher V_t, lower leakage devices used in the rest of the chip. For low-power logic, control of static power dissipation with scaling is the critical goal. To meet this goal, the transistor leakage current is projected to be much lower than for high-performance logic, and circuit and architectural innovations as well as multiple transistors on the chip will be needed, similarly to high-performance logic.

[2] With scaling, difficulties in inducing adequate strain for enhanced mobility— Currently, enhanced channel mobility due to applied strain to the channel is a major contributor to meeting the MOSFET performance requirements. With scaling, it is critically important to maintain (or even increase) the significantly enhanced CMOS channel mobility to continue to meet the performance requirements. However, the strain due to current process-induced strain techniques tends to decrease with scaling, and solutions to maintain the strain in scaled structures are needed. (For more detail, see Logic Potential Solutions section.)

[3] Timely assurance for the reliability of multiple and rapid material, process, and structural changes—In order to successfully scale ICs to meet performance, leakage current, and other requirements, it is expected that numerous major process and material innovations, such as high-κ gate dielectric, metal gate electrodes, elevated source/drain, advanced annealing and doping techniques, new low-κ materials, lead-free solders, multi-chip packages, etc., will need to be implemented in well under a decade. Also, it is projected that new MOSFET structures, starting with ultra-thin body SOI MOSFETs and moving on to ultra-thin body, multiple-gate MOSFETs, will need to be implemented. Understanding and modeling the reliability issues for all these innovations so that their reliability can be ensured in a timely manner is expected to be particularly difficult.

[4] Scaling of DRAM and SRAM to the 22 nm technology generation—For DRAM, a key issue is implementation of high-κ dielectric materials and eventually MIM structures in order to get adequate storage capacitance per cell even as the cell size is shrinking. Also important is controlling the total leakage current, including the dielectric leakage, the storage junction leakage, and the access transistor source/drain subthreshold leakage, in order to preserve adequate retention time. The requirement of low leakage currents causes problems in obtaining the desired access transistor performance. Finally, deploying of low sheet resistance materials for word and bit lines to ensure acceptable speed for scaled DRAMs is critically important.

For SRAM, difficulties with scaling are expected, particularly in maintaining both acceptable noise margins and controlling instability, especially hot electron instability and negative bias temperature instability (NBTI). Also, there are difficult lithography and etch issues with scaling, and difficult issues with keeping the leakage current within tolerable targets for highly scaled SRAMs. Solving these SRAM challenges is critical to system performance, since SRAM is typically used for fast, on-chip memory.

[5] Scaling high-density non-volatile memory (NVM) to the 22 nm technology generation—Inherent in the nature of available nonvolatile semiconductor memory are two challenges. The first is that the memory element structure for each NVM technology differs from the underlying CMOS technology in some way, and accommodating those differences while attempting to scale the memory cell poses some difficult issues. These issues vary depending on which NVM technology is being considered, and specific issues are listed for each NVM type in the table. The second challenge is that the normal operating process used to set and to reset the state of the memory cell generally stresses the materials, and degradation of cell characteristics can be expected. Degradation is usually associated with a defect related mechanism rather than with an intrinsic device characteristic. Endurance and retention requirements provide the user with guidance as to the probable capability of the device and define a "safe" range of use. For both parameters it is a continuous challenge to be able to realistically determine this long-term behavior. Failure causes are difficult to identify and real-time testing is not feasible.

[6] Implementation of advanced, non-classical CMOS with enhanced drive current and acceptable control of short channel effects for highly scaled MOSFETs—For the long-term years, when the transistor gate length is projected to become 10 nm and below, ultra-thin body, multiple-gate MOSFETs with lightly doped channels are expected to be utilized to effectively scale the device, and particularly, to control short-channel effects for such highly scaled devices. The other material and process solutions mentioned above, such as high-κ gate dielectric, metal gate electrodes, strained silicon channels, elevated source/drain, etc., are expected to be incorporated along with the non-classical CMOS structures. For 10 nm gate length and below, body thicknesses well below 10 nm are projected, and the impact of quantum and surface scattering effects on such thin devices are not well understood. Finally, for these advanced, highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal carrier velocity and injection at the source end appears to be necessary. Eventually, high transport channel materials, such as germanium or III-V channels on silicon, or carbon nanotubes or nanowires, may be utilized.

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[7] Dealing with fluctuations and statistical process variations in sub-11 nm gate length MOSFETs—For such devices, the impact of statistical variations is not well understood, including the impact of quantum effects, line edge roughness, and variation in the ultra-thin body width.

[8] Identifying, selecting, and implementing new memory structures—In the long term, increasing difficulty is expected in scaling both DRAMs and NVMs, as discussed for each of these memory types in the table. The need for high density, fast, and new non-volatile memory structures is expected to increase, particularly to reduce power dissipation. Implementing such advanced, non-volatile structures will be a major challenge.

[9] Identifying, selecting, and implementing novel interconnect schemes—The resistivity of copper increases somewhat with scaling for widths under ~100 nm, and at κ ~1–1.5, the limits of low-κ dielectric will be reached. At that point, further interconnect performance improvements will require novel architectural and/or materials solutions

[10] Eventually, identification, selection, and implementation of advanced, non-CMOS devices and architectures for advanced information processing—Eventually, toward the end of the Roadmap or beyond, scaling of MOSFETs is likely to become ineffective and/or very costly, and advanced non-CMOS solutions will need to be implemented to continue to improve performance, power, density, etc. It is expected that such solutions will be integrated either functionally or physically with a CMOS baseline technology that takes advantage of the high-performance, cost-effective, and very dense CMOS logic that will have been developed and implemented by then.

LOGIC TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

LOGIC TECHNOLOGY REQUIREMENTS

The technology requirements tables reflect the MOSFET transistor requirements of both high-performance and low-power digital ICs. High-performance logic refers to chips of high complexity, high performance, and high power dissipation, such as microprocessor unit (MPU) chips for desktop PCs, servers, etc. Low-power logic refers to chips for mobile systems, where the allowable power dissipation and hence the allowable leakage currents are limited by battery life. There are two major categories within low-power, low operating power (LOP) and low standby power (LSTP) logic. LOP chips are typically for relatively high-performance mobile applications, such as notebook computers, where the battery is likely to be high capacity and the focus is on reduced operating (i.e., dynamic) power dissipation. LSTP chips are typically for lower performance, lower cost consumer type applications, such as consumer cellular telephones, with lower battery capacity and an emphasis on the lowest possible static power dissipation, i.e., the lowest possible leakage current. The transistors for high-performance ICs have both the highest performance and the highest leakage current of all, and hence the physical gate length and all the other transistor dimensions are most rapidly scaled for high-performance logic. The transistors for LOP chips have somewhat lower performance and considerably lower leakage current, while the transistors for LSTP chips have both the lowest performance and the lowest leakage current of all. For LOP logic, the gate length lags behind the high-performance transistor gate length by two years, reflecting historical trends and the need for low leakage current in mobile applications. For LSTP logic, the gate length lags that of high-performance logic by four years, reflecting the ultra-low leakage current required.

For generating the entries in the logic technology requirements tables, the MASTAR MOSFET modeling software was used. T. Skotnicki, F. Boeuf and their collaborators developed MASTAR[1], [2], [3] and it contains detailed analytical MOSFET models that have been verified against literature data. It is well suited to efficiently analyzing technology tradeoffs for generating these tables. An important calculated output parameter is the intrinsic MOSFET delay, $\tau = CV/I$, where C is the total gate capacitance (including parasitic gate overlap and fringing capacitance) per micron transistor width, V is the power supply voltage (V_{dd}), and I is the saturation drive current per micron transistor width ($I_{d,sat}$). τ is a reasonable metric for the intrinsic MOSFET delay, and hence $1/\tau$, the transistor intrinsic switching frequency, is used as the key transistor performance metric. *(It should be noted that another transistor delay metric, CV/I_{eff}, where I_{eff} is a modified drain current derived from a linear superposition of currents,[4] has been developed recently and appears to be somewhat more accurate than the $CV/I_{d,sat}$ metric. We are continuing to use the latter metric because it is sufficiently accurate to follow the key scaling trends, and for consistency with previous Roadmaps.)*

To determine the projected parameter values in a table, a target is set for one of the key outputs, either leakage current (for low-power logic) or $1/\tau$ (for high-performance logic). Then the input parameters are tentatively chosen based on scaling rules, engineering judgment, and physical device principles. Using MASTAR, the input parameters are iteratively varied until the target is met, and the final set of values for the input parameters is entered into the table. The MASTAR program and the specific MASTAR process and roadmap files used to generate the tables are on the ITRS website at *http://www.itrs.net*.

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In each of these tables, multiple parallel paths are followed. Planar bulk CMOS is extended as long as possible, while advanced CMOS technologies, ultra-thin body fully depleted (UTB FD) silicon-on-insulator (SOI) MOSFETs and multiple-gate, particularly double-gate (DG) MOSFETs (such as FinFETs), are implemented in 2010 or later and run in parallel with the planar bulk CMOS (for details see the logic tables). With scaling, difficulties arise with planar bulk MOSFETs because of high channel doping, inability to adequately control short channel effects, and others (for more detail see Difficult Challenges section, Item 1). The advanced CMOS technologies can be scaled more effectively, and hence are utilized later in the Roadmap. In fact, multiple-gate MOSFET scaling is superior to UTB FD MOSFET scaling, and hence the ultimate MOSFET is projected to be the multiple-gate device. For the industry as a whole, multiple paths are likely, as different companies choose different timing in extending planar bulk and then switching to the advanced CMOS technologies, depending on their needs, plans, and technological strengths. The multiple parallel paths in this roadmap are meant to reflect this. The specific set of projected parameter values in each of the tables reflects a particular scaling scenario, in which the targeted values for the key output are achieved. However, since there are numerous input parameters that can be varied, and the output parameters are complicated functions of these numerous input parameters, other sets of projected parameter values (i.e., different scaling scenarios) can be found that achieve the targeted values for the key output. For example, if, in one scenario, the equivalent oxide thickness (EOT) were scaled rapidly so that gate leakage current scales upward rapidly, requiring early introduction of high-κ gate dielectric to reduce the gate leakage current to tolerable levels, an alternate scaling scenario would scale the EOT slower. As a result, the gate leakage current would scale upward more slowly, hence delaying the required introduction of high-κ gate dielectric. However, some of the other parameters, such as the gate length, the channel doping, and/or mobility enhancement, would have to be scaled differently to compensate for the slowed scaling of the EOT and to reach the same targeted output values. Hence, the scaling scenarios in these tables constitute a good guide for the industry, and are meant to be representative, but there will be considerable variance in the actual paths that the various companies will take.

For the high-performance logic tables (see Tables PIDS2a and b), the driver is the MOSFET intrinsic performance metric, $1/\tau$. Specifically, the target is an average 17% per year increase in $1/\tau$, which matches the historic rate of improvement in device performance. Meeting this target is an important enabler for the desired rate of improvement in the chip clock speed. All the other parameter values in the table are chosen iteratively to meet this target, as explained above. Several important consequences of meeting this target are clear from the tables. The NMOSFET saturation drive current, $I_{d,sat}$, pretty steadily increases over the course of the Roadmap in order to keep $1/\tau$ increasing at the desired 17% per year rate. The subthreshold source/drain leakage current, $I_{sd,leak}$, is relatively high, at 0.34 μA/μm in 2007, and it generally increases with succeeding years, which has important consequences for the chip power dissipation (to be discussed below). Figure PIDS1 shows the scaling of $1/\tau$ for high-performance logic. Overall, the 17%/year target is met, with several important exceptions. For planar bulk, for 2009 and beyond, the $1/\tau$ curve slopes increasingly down from the 17%/year curve, mainly because of the scaling difficulties discussed in the Difficult Challenges section, Item 1. (The scaling difficulties are also indicated in the MASTAR simulations, where the required channel doping increases sharply with year, to a very high value of ~8e18 cm^{-3} in 2012.) For UTB FD SOI, a similar decrease from the 17% curve happens after 2013, although to a lesser extent, and for DG devices, the curve slopes down from the 17%/year curve after 2019. In all these cases, difficulties with controlling short-channel effects with scaling results in a slowing in the transistor performance increase in order to keep the leakage current within tolerable limits. The LSTP and LOP curves for $1/\tau$ scaling show similar effects, although the overall performance increase is ~13-14%/year for these.

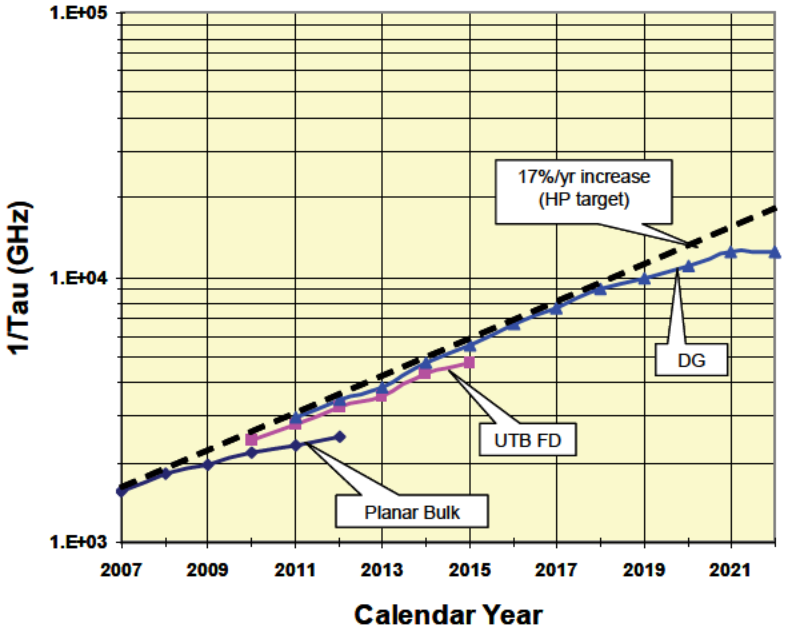


Figure PIDS1 High-Performance Logic: Scaling of Transistor Intrinsic Speed, 1/τ

The IC industry has begun to deploy architectural techniques such as multiple cores and multiple threads that exploit parallelism to improve the overall chip performance, enhance the chip functionality while maintaining chip power density and total chip power dissipation at a manageable level. With more than one central processing unit (CPU) core on chip, the cores can be clocked at a lower frequency while still getting better overall chip performance. Thus, there is a trend for system designers to emphasize integration level, which enables more cores to be put on a chip, instead of raw transistor speed in optimizing system-level performance. In addition, system designers are sweeping ever more cache memory onto the processor chip in order to minimize the system performance penalty associated with finite-cache effects. As DRAM cells are significantly smaller than SRAM cells, another high-performance system technology trend is to integrate DRAM cells onto a processor chip for use in higher-level cache memory. With scaling, it is expected that these techniques will be more and more heavily exploited. In subsequent editions of the Roadmap, the Design and PIDS Working Groups will consider the impact of these architectural techniques, and in particular whether improved architectural parallelism may allow a slackening in the 17%/year transistor performance scaling target.

For high-performance chips, the high subthreshold leakage current must be dealt with to keep chip static power dissipation within tolerable limits. One common approach is to fabricate more than one type of transistor on the chip, including the high-performance, low V_t device described above, as well as other MOSFET(s) with higher V_t and sometimes larger EOT to reduce the leakage current. These alternate, lower leakage devices will have lower saturation drive current and hence poorer device performance (i.e., lower MOSFET intrinsic switching frequency, 1/τ) than the high-performance devices. The high-performance device is used just in critical paths, and the low leakage devices are used everywhere else. Extensive use of the low leakage devices can significantly reduce the chip static power dissipation without seriously degrading chip performance. Current circuit/architectural techniques to curtail static power dissipation include pass gates to cut off access to power/ground rails or other techniques to power down circuit blocks. Other potential techniques include well biasing, or using electrically or dynamically adjustable V_t devices. Hence, a realistic picture of scaled high-performance ICs is that the static power dissipation is controlled by utilizing more than one type of transistor and by utilizing device/design/architectural techniques. In the technology requirements table, we have characterized only the high-performance transistor because this transistor is the technology driver.

For low-power chips, the targeted output parameter is the source/drain subthreshold leakage current, $I_{sd,leak}$, and the targets are relatively low, especially for LSTP logic, as discussed above. $I_{sd,leak}$ is 30 pA/μm and is held essentially constant for LSTP, while it is ~9 nA/μm for LOP in 2007, and it increases slowly with scaling. All the other parameter values in the tables are chosen iteratively to meet the $I_{sd,leak}$ targets, as explained above. Nevertheless, the resultant

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average improvement in the device performance metric, $1/\tau$, is about 13-14% per year for both LOP and LSTP. Note that, to meet the leakage current requirements, the gate length scaling of low-power logic lags behind that of high-performance logic (see the logic tables for details). One key issue for LSTP logic is the slow scaling of V_{dd}. Refer to Tables PIDS3a and b for LSTP data. This slow scaling is a result of the relatively slow scaling of the threshold voltage, V_t, required to meet the very low subthreshold leakage current targets. V_{dd} must follow V_t in scaling slowly because, to obtain reasonable device performance, the overdrive, $(V_{dd}-V_t)$, must remain relatively large. Since dynamic power dissipation is proportional to $(V_{dd})^2$, the dynamic power dissipation for the LSTP logic scales relatively slowly, but since the activity factor for this type of logic is expected to be relatively small, the lowered static power dissipation because of the very low leakage currents more than compensates. In contrast to LSTP logic, V_{dd} scales relatively quickly for LOP logic (see technology requirements tables for LOP, Tables PIDS3c and d), where, as mentioned above, the focus is on minimizing the operating power (i.e., the dynamic power dissipation, which is proportional to V_{dd}^2). However, since $I_{sd,leak}$ is larger than for LSTP logic, the saturation threshold voltage is low enough that the overdrive, $(V_{dd}-V_t)$, is reasonable.

For low-power chips, the key goal is low power dissipation in order to enhance battery life, with a tradeoff of low performance compared to high-performance chips. This overall goal is attained through the use of transistors with low $I_{sd,leak}$ as well as through the approaches utilized for high-performance logic: multiple transistors on chip and application of circuit and architectural techniques, including power management techniques to reduce chip leakage current in the standby mode. Eventually, effective dynamic threshold voltage adjust techniques may be feasible. The nominal targets for $I_{sd,leak}$ chosen in these LSTP logic tables are quite low, and reflect a transistor design emphasizing low leakage current in the active mode. In contrast, some companies will utilize transistors with significantly higher $I_{sd,leak}$ to get higher performance, and will thus rely more heavily on circuit and architectural techniques to lower overall chip power dissipation. Finally, for LOP logic, as discussed above, V_{dd} will be scaled relatively quickly to keep the dynamic power dissipation within tolerable limits.

A critical issue is the gate leakage current, and whether the current standard silicon oxy-nitride gate dielectric can meet the gate leakage current density limit as the oxy-nitride becomes increasingly thin with scaling (Refer to Tables PIDS2a and b, and PIDS3a through d and to table notes [2] and [5]). This is an important issue, since, in the EOT regime in the Roadmap, gate leakage current is due to direct tunneling and hence the gate leakage current increases approximately exponentially with decreasing EOT. The FEP TWG and North Carolina State University performed detailed simulations of direct tunneling leakage current density through oxides, and these simulations were used to calculate the expected value of the gate leakage current density due to tunneling through oxy-nitride, using as inputs the scaled V_{dd} and EOT per the technology requirements tables. For LSTP, LOP, and high-performance logic, these calculations of the expected gate leakage current density were compared to the gate leakage current density limit ($J_{g,limit}$) from the tables. The results are shown in Figures PIDS2 through PIDS4, where "simulated J_g" is the expected value of the gate leakage current density from the simulations. For the LSTP and high-performance logic transistors, the two Jg curves cross shortly before or at 2008, and hence, for 2008 and beyond, the leakage current limit cannot be met using silicon oxy-nitride because of direct tunneling. Furthermore, for both curves the $J_{g,simulated}$ curve separates rapidly from the $J_{g,limit}$ curve after 2008, indicating that gate leakage would rapidly become completely out of specification if oxy-nitride were to continue to be used for the gate dielectric after 2008. Hence, high-κ gate dielectric (which significantly reduces gate leakage current density for a given EOT) is clearly needed for LSTP and high-performance logic by 2008; this is the leading potential solution for high gate leakage. For LOP logic, the point where the leakage current limit cannot be met using oxy-nitride is in 2009, but high κ is assumed to be implemented for LOP in 2008 as well as for the others. Note that the J_g plots in all three figures are just for planar bulk MOSFETs; the plots for UTB FD and dual gate (DG) MOSFETs have not been included in order to avoid cluttering the figures and because the implications for when high-κ gate dielectrics are needed would be unchanged if those plots were included.

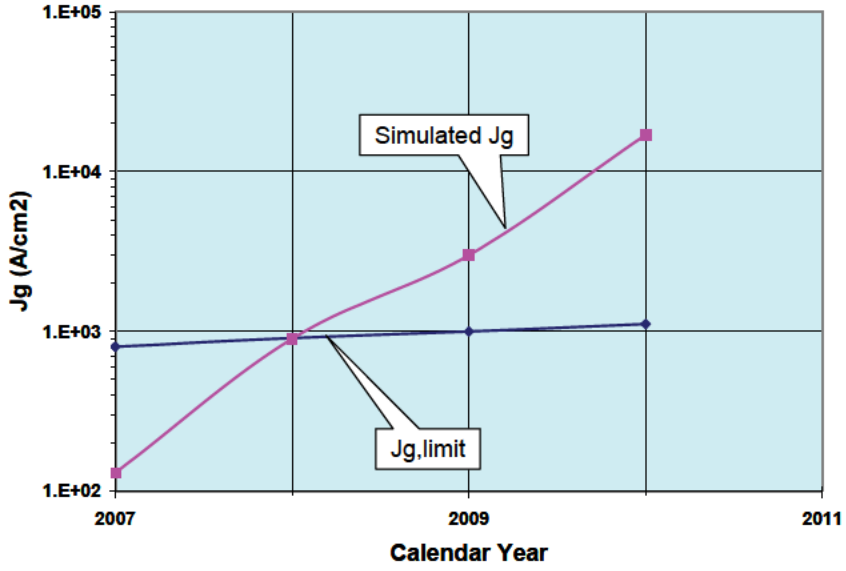


Figure PIDS2 High-Performance Logic: $J_{g,limit}$ versus Simulated Gate Leakage Current Density for SiON Gate Dielectric

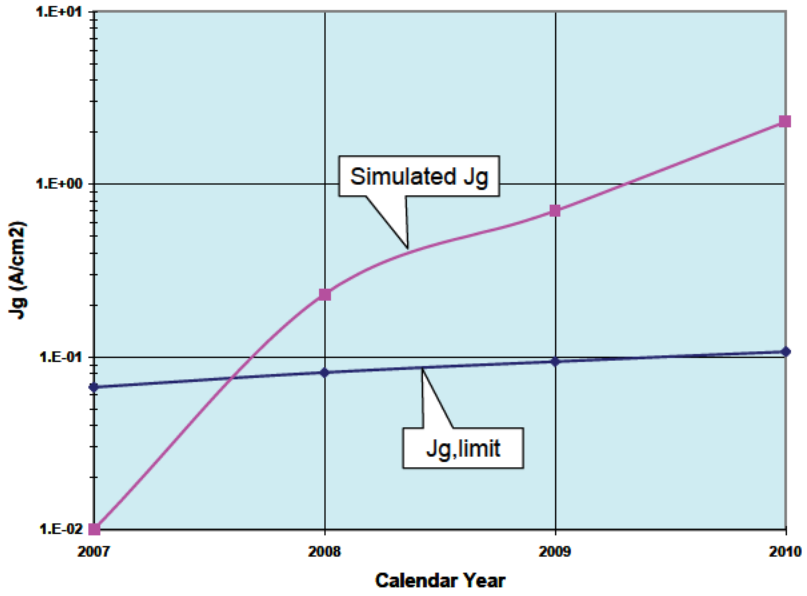


Figure PIDS3 LSTP: $J_{g,limit}$ versus Simulated Gate Leakage Current Density for SiON Gate Dielectric

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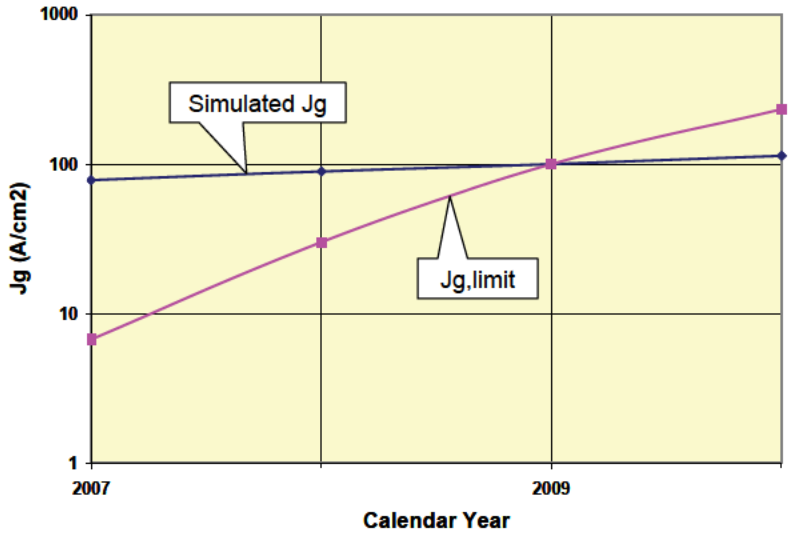


Figure PIDS4 LOP: $J_{g,limit}$ versus Simulated Gate Leakage Current Density for SiON Gate Dielectric

Table PIDS2a High-performance Logic Technology Requirements—Near-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	68	59	52	45	40	36	32	28	25
MPU Physical Gate Length (nm)	25	22	20	18	16	14	13	11	10
L_g Physical Lgate for High Performance logic (nm) [1]	25	22	20	18	16	14	13	11	10
EOT Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	11	9	7.5	6.5	5.5	5			
UTB FD (Å)				7	6	5.5	5	5	5
DG (Å)					8	7	6	6	6
Gate Poly Depletion and Inversion-Layer Equivalent Thickness [3]									
Extended Planar Bulk (Å)	7.4	3.1	2.9	2.8	2.7	2.6			
UTB FD (Å)				4	4	4	4	4	4
DG (Å)					4	4	4	4	4
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]									
Extended Planar Bulk (Å)	18.4	12.1	10.4	9.3	8.2	7.6			
UTB FD (Å)				11	10	9.5	9	9	9
DG (Å)					12	11	10	10	10
$J_{g,limit}$ Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm^2)	8.00E+02	9.09E+02	1.00E+03	1.11E+03	1.25E+03	1.43E+03			
UTB FD (A/cm^2)				1.11E+03	1.25E+03	1.43E+03	1.54E+03	1.82E+03	2.00E+03
DG (A/cm^2)					1.25E+03	1.43E+03	1.54E+03	1.82E+03	2.00E+03
V_{dd} Power Supply Voltage (V) [6]									
Extended Planar Bulk (V)	1.1	1	1	1	0.95	0.9			
UTB FD and DG (V)				1	1	0.9	0.9	0.9	0.8
$V_{t,sat}$ Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	134	94	94	103	101	112			
UTB FD (mV)				103	89	87	93	99	99
DG (mV)					115	105	103	108	111
$I_{sd,leak}$ Source/Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (µA/µm)	0.34	0.71	0.70	0.64	0.74	0.68			
UTB FD (µA/µm)				0.33	0.52	0.62	0.56	0.55	0.60
DG (µA/µm)					0.2	0.34	0.37	0.38	0.38
$I_{d,sat}$ NMOS Drive Current [9]									
Extended Planar Bulk (µA/µm)	1211	1513	1639	1807	1824	1762			
UTB FD (µA/µm)				1948	2000	1944	2109	2245	2030
DG (µA/µm)					1917	1943	2204	2365	2295
Mobility enhancement factor due to strain [10]	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
$I_{d,sat}$ enhancement factor due to strain [11]									
Extended Planar Bulk	1.09	1.08	1.08	1.08	1.09	1.08			
UTB FD				1.07	1.06	1.06	1.06	1.05	1.05
DG					1.04	1.04	1.04	1.03	1.03

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Table PIDS2a High-performance Logic Technology Requirements—Near-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Effective Ballistic Enhancement Factor , Kbal [12]									
Extended Planar Bulk	1	1	1	1	1	1			
UTB FD				1.05	1.1	1.16	1.2	1.24	1.28
DG					1.17	1.25	1.31	1.37	1.53
R_{sd} *Effective Parasitic series source/drain resistance [13]*									
Extended Planar Bulk (Ω-µm)	200	200	200	180	180	180			
UTB FD (Ω-µm)		-	-	180	180	180	170	160	160
DG (Ω-µm)					180	180	170	160	160
$C_{g,ideal}$ *Ideal NMOS Device Gate Capacitance [14]*									
Extended Planar Bulk (F/µm)	4. 70E-16	6.30E-16	6.63E-16	6.70E-16	6.71E-16	6.33E-16			
UTB FD (F/µm)				5.65E-16	5.52E-16	5.08E-16	4.98E-16	4.22E-16	3.83E-16
DG (F/µm)					4.60E-16	4.39E-16	4.48E-16	3.80E-16	3.45E-16
$C_{g,total}$ *Total gate capacitance for calculation of CV/I [15]*									
Extended Planar Bulk (F/µm)	7.10E-16	8.40E-16	8.43E-16	8.40E-16	8.35E-16	7.93E-16			
UTB FD (F/µm)				8.08E-16	7.22E-16	6.78E-16	6.58E-16	5.82E-16	5.43E-16
DG (F/µm)					6.50E-16	6.29E-16	6.28E-16	5.59E-16	5.25E-16
$\tau = CV/I$ *NMOSFET intrinsic delay (ps) [16]*									
Extended Planar Bulk (ps)	0.64	0.55	0.51	0.46	0.43	0.4			
UTB FD (ps)				0.41	0.36	0.31	0.28	0.23	0.21
DG (ps)					0.34	0.29	0.26	0.21	0.18
$1/\tau$ *NMOSFET intrinsic switching speed (GHz) [17]*									
Extended Planar Bulk (GHz)	1563	1818	1961	2174	2326	2500			
UTB FD (GHz)				2439	2778	3226	3571	4348	4762
DG (GHz)					2941	3448	3846	4762	5556

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Table PIDS2b High-performance Logic Technology Requirements—Long-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5.0*	*4.5*
L_g Physical Lgate for High Performance logic (nm) [1]	*9*	*8*	*7*	*6*	*5.5*	*5*	*4.5*
EOT Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)							
DG (Å)	5.5	5.5	5.5	5	5	5	5
Gate Poly Depletion and Inversion-Layer Equivalent Thickness [3]							
Extended Planar Bulk (Å)							
UTB FD (Å)							
DG (Å)	4	4	4	4	4	4	4
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]							
Extended Planar Bulk (Å)							
UTB FD (Å)							
DG (Å)	9.5	9.5	9.5	9	9	9	9
$J_{g,limit}$ Maximum gate leakage current density [5]							
Extended Planar Bulk (A/cm^2)							
UTB FD (A/cm^2)							
DG (A/cm^2)	2.22E+03	2.50E+03	2.86E+03	3.33E+03	3.64E+03	4.00E+03	4.44E+03
V_{dd} Power Supply Voltage (V) [6]							
Extended Planar Bulk (V)							
UTB FD and DG (V)	0.8	0.7	0.7	0.7	0.65	0.65	0.65
$V_{t,sat}$ Saturation Threshold Voltage [7]							
Extended Planar Bulk (mV)							
UTB FD (mV)							
DG (mV)	110	109	114	119	123	115	118
$I_{sd,leak}$ Source/Drain Subthreshold Off-State Leakage Current [8]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)							
DG (µA/µm)	0.44	0.48	0.45	0.47	0.43	0.62	0.60
$I_{d,sat}$ NMOS Drive Current [9]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)							
DG (µA/µm)	2627	2533	2804	2768	2677	2799	2786
Mobility enhancement factor due to strain [10]	1.8	1.8	1.8	1.8	1.8	1.8	1.8
$I_{d,sat}$ enhancement factor due to strain [11]							
Extended Planar Bulk							
UTB FD							
DG	1.03	1.03	1.02	1.02	1.02	1.02	1.02

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Table PIDS2b High-performance Logic Technology Requirements—Long-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year of Production	2016	2017	2018	2019	2020	2021	2022
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	22	20	18	16	14	13	11
MPU Physical Gate Length (nm)	9	8	7	6.3	5.6	5.0	4.5
Effective Ballistic Enhancement Factor , Kbal [12]							
Extended Planar Bulk							
UTB FD							
DG	1.67	1.87	1.99	1.97	2.11	2.11	2.11
R_{sd} Effective Parasitic series source/drain resistance [13]							
Extended Planar Bulk (Ω-μm)							
UTB FD (Ω-μm)							
DG (Ω-μm)	155	150	145	145	145	135	135
$C_{g,ideal}$ Ideal NMOS Device Gate Capacitance [14]							
Extended Planar Bulk (F/μm)							
UTB FD (F/μm)							
DG (F/μm)	3.27E-16	2.91E-16	2.68E-16	2.30E-16	2.11E-16	1.92E-16	1.72E-16
$C_{g,total}$ Total gate capacitance for calculation of CV/I [15]							
Extended Planar Bulk (F/μm)							
UTB FD (F/μm)							
DG (F/μm)	5.07E-16	4.81E-16	4.58E-16	4.10E-16	3.91E-16	3.62E-16	3.42E-16
τ=CV/I NMOSFET intrinsic delay (ps) [16]							
Extended Planar Bulk (ps)							
UTB FD (ps)							
DG (ps)	0.15	0.13	0.11	0.1	0.09	0.08	0.08
1/τ NMOSFET intrinsic switching speed (GHz) [17]							
Extended Planar Bulk (GHz)							
UTB FD (GHz)							
DG (GHz)	6667	7692	9091	1.00E+04	1.11E+04	1.25E+04	1.25E+04

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Notes for Tables PIDS2a and b

As described in the text, MASTAR[1 2 3], a detailed analytical MOSFET modeling software package, has been utilized to generate the parameter values in these tables. The MASTAR modeling package and user's manual are in the backup material on the ITRS website, as well as the detailed MASTAR simulations that underlay these tables. Also note that the parameters in this table are for an NMOSFET with nominal gate length at an operating temperature of 25°C. Furthermore, although there are multiple MOSFETs in a typical logic chip, with differing threshold voltages, I_{on}, I_{off}, and oxide thickness, the transistor specified here is the transistor with the lowest threshold voltage, highest I_{on} and highest I_{off}, lowest oxide thickness, and fastest intrinsic transistor switching speed. This transistor typically constitutes a small minority of the transistors on a chip; it is used mainly in critical paths, and most of the transistors on the chip have higher threshold voltage and lower leakage current. This high speed, high leakage transistor is specified in this table because it tends to drive the technology.

As explained in the text, multiple parallel options for the transistor type are included in the tables, including planar bulk CMOS extended to its practical scaling limits, ultra-thin body fully-depleted (UTB FD) SOI CMOS, also extended to its practical scaling limits, and double-gate (DG) CMOS (e.g., FinFETs). Note that the limit for planar bulk CMOS is through 2012, and for UTB FD it is through 2015, while DG continues through 2022. The challenges in scaling planar bulk are significant, resulting in an inability to attain the desired 17%/ year improvement in the transistor intrinsic switching speed beyond 2009 (see the text for further discussion). The scalability of UTB FD is superior to that of planar bulk. As a result, $I_{sd,leak}$ is higher for planar bulk than for UTB FD. Furthermore, EOT is scaled more rapidly from 2010 through 2012 for planar bulk than for UTB FD. Finally, from the MASTAR modeling results, the short channel effects such as drain induced barrier lowering (DIBL) are always larger for planar bulk than for UTB FD. In a similar vein, the scalability of DG is superior to that of UTB FD. Hence, $I_{sd,leak}$ is lower for DG than for UTB FD, while EOT is scaled more slowly for DG than for UTB FD. Furthermore, from the MASTAR modeling results, short channel effects are always lower for DG. Hence, DG is the ultimate MOSFET device, continuing through the end of the Roadmap in 2022.

For each transistor option, the scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goal for high-performance logic, 17% per year average improvement in the NMOS intrinsic switching speed, while keeping the leakage currents, the short channel effects, and other key characteristics under control. However, there are numerous parameters (such as EOT, V_{dd}, $I_{sd,leak}$, etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters. The scenarios in this table were selected to be as representative of the industry as possible. In particular, in this table, high-κ gate dielectric and metal gate electrode are assumed to be available in 2008. See the figures and discussion in the text for why high-κ gate dielectric is required in 2008. With the EOT=0.9 nm in 2008, metal gate electrode is needed to reduce the polysilicon depletion.

[1] L_g is the physical gate length the final, as-etched length of the bottom of the gate electrode. Values have been set by the ORTC. The gate dimensional control requirement is set by the Lithography and FEP Etch ITWGs, and is assumed to have a three-sigma value of ± 12% × L_g. It is expected that meeting this requirement will become increasingly difficult with scaling (refer to the Lithography chapter and the FEP chapter). Gate length variation is assumed to be a primary factor responsible for driving device parameter variation. Recent data indicate that the Lg scaling in the ITRS may be overly aggressive compared to the reality in the industry, and this will be re-examined in the 2008 ITRS.

[2] EOT For a gate dielectric of thickness T_d and relative dielectric constant κ, EOT is defined by EOT = T_d / (κ/3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide. For a MOSFET with the gate dielectric of thickness T_d, the ideal gate capacitance per unit area is the same as that of a similar MOSFET, but with a gate dielectric made up of thermal silicon dioxide with a thickness of EOT. It is projected that high-κ gate dielectric will be required by 2008 to control the gate leakage (see the text for further discussion on this point.) The rate of scaling of EOT has been slow from 2005 through 2007 to keep the gate leakage current within the specified limits while utilizing silicon oxy-nitride for the gate dielectric. However, there is a sharp EOT decrease in 2008, when we assume that high-κ gate dielectric will be implemented. The yellow coloring reflects the uncertainty in our high-κ solutions for EOT < 0.9nm, while the red coloring reflects the increased uncertainty of solutions for EOT < 0.7nm. Measurement of EOT is complicated, and is usually done via sophisticated MOS capacitor-voltage (CV) measurements on MOS capacitors or via optical measurements.

[3] Gate Poly Depletion and Inversion-Layer Equivalent Thickness accounts for gate electrode depletion and inversion-layer effects, including quantum effects, both of which are calculated by MASTAR. For polysilicon gate electrodes, the portion of the electrical thickness adjustment due to gate electrode depletion is dependent on the polysilicon doping. For 2008 and beyond, there is a projected inability to adequately dope polysilicon gate electrodes to meet the gate depletion thickness adjustment requirements, and hence it is assumed that metal-gate electrodes, which reduce the gate depletion effect to zero, will be introduced. The abrupt reduction in this parameter in 2008 reflects the zero depletion. For 2008 and beyond, the difference between the parameter value for planar bulk versus the 4 nm value for DG and UTB FD reflects the light channel doping in the latter types of MOSFET and the heavy channel doping in planar bulk. For planar bulk CMOS, the metal gate work function needs to be near the silicon conduction band edge for NMOS and near the silicon valence band edge for PMOS to properly set the MOSFET threshold voltage, as with polysilicon gates. For UTB FD and DG MOSFETs, the channel is very thin and lightly doped, and the work function of the metal gates needs to be within a few hundred millivolts of the silicon midgap (i.e., "near silicon midgap" work function) to properly set the MOSFET's threshold voltage. Multiple V_t's may be obtained by tuning the work function. The yellow and red colors generally follow that of EOT (see Note [2] above), reflecting the tight coupling between the metal gate electrode and the high-κ gate dielectric. For UTB FD and DG, the color is red, reflecting the uncertainties of setting and tuning the effective work function.

[4] EOT_{elec} is the sum of EOT and Gate Poly Depletion and Inversion-Layer Thickness (see Notes [2] and [3] above). For MOSFETs in inversion, ideal gate capacitance per unit area (see Note [14]) is εox / (EOT_{elec}), where εox is the dielectric constant of thermal silicon dioxide. The equivalent electrical oxide thickness in inversion is used in calculations of the transistor intrinsic delay, CV/I (see Note [16]). Red/yellow coloring follows that of EOT and Gate Poly Depletion and Inversion-Layer Thickness.

[5] $J_{g,limit}$ is the maximum allowed gate leakage current density at 25°C, and it is measured with the gate biased to V_{dd} and the source, drain, and substrate all tied to ground. $J_{g,limit}$ is related to $I_{sd,leak,TGT}$, the nominal subthreshold leakage current target at 25°C . $I_{sd,leak,TGT}$ is set to 0.2 μA/micron device width. Specifically, $J_{g,limit}$= [Initial Factor] x [$I_{sd,leak,TGT}$ / L_g] × [Hi T Factor] / [Circuit Factor]. Hi T Factor is set to 10, and it accounts for the high operating temperature (100°C) expected for high-performance logic, by adjusting for both the rapid increase in $I_{sd,leak}$ with temperature and the insensitivity of gate leakage current (since it is due to direct tunneling) to temperature. Circuit Factor is set to 1, and it accounts for the differences between the subthreshold leakage current and the gate leakage current in logic gates compared to single isolated transistors as specified by the $J_{g,limit}$ and $I_{sd,leak}$ parameters in this table. (The reason for these differences is the different bias conditions on the various transistors in logic gates compared to the bias conditions used to define $I_{sd,leak}$ (see Note [8]) and $J_{g,limit}$ for the NMOS transistor in this table). The Initial Factor is set to 0.1, and accounts for the fact that the transistor specified in this table is the low threshold voltage transistor with high subthreshold leakage, but that the predominant transistors in typical circuits have significantly lower subthreshold leakage current. The values of Hi T Factor, Circuit Factor, and Initial Factor used here are rough estimates. The yellow and red coloring follows that of EOT (see Note [2] above).

[6] V_{dd} is the nominal power supply voltage. It has been chosen to maintain sufficient voltage over-drive [V_{dd} – saturation threshold voltage (see Note 7)] in order to meet the required saturation current drive values while still maintaining reasonable vertical gate dielectric electric field strengths. Target power supply voltage values for actual ICs may vary ± 10% (or more) from the values in this table, depending on the particular circuit design application or technology optimization.

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[7] $V_{t,sat}$ is the saturation threshold voltage for a nominal gate length transistor with drain bias set equal to V_{dd}, as calculated by MASTAR. The threshold voltage values and the corresponding subthreshold leakage current values (see Note [8]) have been chosen to maintain sufficient voltage over-drive (V_{dd} – saturation threshold voltage) in order to meet the required saturation current drive values (see Note [9]). For planar bulk, the cross-hatched interim solution in 2007 indicates that because of the SiON gate dielectric, the EOT is large (1.1nm) and hence the short-channel effects are quite large (for example, DIBL is over 340 mV/V per MASTAR). The yellow color is associated with high substrate doping exceeding 4E18 cm^{-3} (from MASTAR), while the red color is associated with very high substrate doping exceeding 6E18 cm^{-3}. For UTB FD devices, the color is red in 2010 because of the challenges of controlling the very thin silicon body thickness (T_{si}) required to control $V_{t,sat}$ and short channel effects. For DG devices, the color is red right from the beginning because there are very many issues that are not understood now; in particular, defining and controlling the fin width, which is typically ~0.6 L_g, is a major challenge. The required silicon body thickness for UTB FD and the fin width for DG come from MASTAR.

[8] $I_{sd,leak}$ subthreshold leakage current is defined as the NMOSFET source current per micron of device width, at 25°C, with the drain bias set equal to V_{dd} and with the gate, source, and substrate biases set to zero volts. Total NMOS off-state leakage current (I_{off}) is the NMOSFET drain current per micron of device width at 25°C, and is the sum of the NMOS subthreshold, gate, and junction leakage currents (the latter includes band-to-band tunneling and gate induced drain leakage [GIDL] components). The subthreshold leakage current is assumed to be larger than the junction leakage current component at either 25°C or high-temperature conditions, but see Note [5] for the relation between Isd,leak and gate leakage current density. The yellow and red coloring follows that of $V_{t,sat}$ (see Note [7] above) because $V_{t,sat}$ is a critical determinant of $I_{sd,leak}$. The above subthreshold, gate, and junction leakage current scaling scenario also applies to PMOS devices.

[9] $I_{d,sat}$ saturation drive current is defined as the NMOSFET drain current per micron device width with the gate bias and the drain bias set equal to V_{dd} and the source and substrate biases set to zero. The saturation drive current values have been chosen to continue the historical 17% per year device performance scaling (see Note [16] below) as nearly as possible. PMOS saturation drive current value is assumed to be (40–50) % of the NMOS saturation drive current value. Yellow and red coloring follows that of four items the parasitic source/drain series resistance, R_{sd} (see Note [13] below), the equivalent electrical oxide thickness in inversion (see Note [4]), the required mobility enhancement factor (see Note [10]), and the ballistic enhancement factor (see Note [12]).

[10] Mobility Enhancement Factor due to Strain (μ_{ratio}). μ_{ratio} = [enhanced mobility]/[reference mobility], where [enhanced mobility] is the actual mobility including the enhancement due to strain, and [reference mobility] is the mobility in the absence of strain. Following the literature, the value of μ_{ratio} is limited to a maximum of 1.8[5]. Mobility enhancement was implemented in product in 2004[6] to meet the required saturation drive current, and hence the coloring for extended planar bulk is initially white. However, there are numerous approaches in the literature for mobility enhancement (including global strain using thin silicon epitaxial layers on SiGe epitaxial layers[7], different process induced strain approaches such as strained thin overlayers of SiN, selective epitaxial SiGe in the PMOS S/D and selective epitaxial Si C in the NMOS S/D, hybrid orientations, etc. [8 9]). As we continue to scale MOSFETs, it becomes more difficult to maintain the strain, and it is unclear what the optimal approach(es) will be and how to integrate them into the process flow. Consequently, the cells are colored yellow in 2009, when L_g=20 nm and the doping approaches 4.5E18 cm^{-3} according to the MASTAR modeling. For UTB FD and DG, the color is red because strain and enhanced mobility are less well understood in these structures.

[11] Mobility Enhancement Factor for $I_{d,sat}$ captures the improvement in the saturation drive current due to mobility enhancement. This factor is defined as [enhanced $I_{d,sat}$]/$I_{d,ref}$ = $I_{d,ratio}$, where [enhanced $I_{d,sat}$] is the actual saturation drive current including the impact of strain-enhanced mobility and $I_{d,ref}$ is the saturation drive current in the absence of mobility enhancement. MASTAR calculates $I_{d,ratio}$ as a function of the mobility enhancement factor, μ_{ratio} (see Note [10]). Generally, $I_{d,ratio}$ is significantly less than μ_{ratio} due to short channel effects and velocity saturation. The yellow or red coloring follows that for μ_{ratio} (Note [10]).

[12] Effective Ballistic Enhancement Factor is a multiplying factor for $I_{d,sat}$, reflecting quasi-ballistic enhanced transport (due largely to enhanced injection at the source) in highly scaled, ultra-thin body MOSFETs, both UTB FD SOI and DG MOSFETs. Planar bulk CMOS presumably does not have ballistic enhancement because of high doping in these devices. Values for this factor greater than 1 reflect quasi-ballistic enhancement. The value of this parameter is driven by the required saturation drive current to meet performance requirements. The red coloring reflects the lack of known enhanced quasi-ballistic transport solutions for transistors.

[13] R_{sd} is the maximum allowable parasitic series source plus drain resistance (i.e., total resistance for the two sides) per micron of MOSFET width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow and red coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling. The R_{sd} values have been increased from the 2005 ITRS, based on updated information.

[14] $C_{g,ideal}$ is the ideal gate capacitance per micron device width, in inversion. $C_{g,ideal}$ =[εox /(EOT_{elec})] × L_g, where εox is the dielectric constant of thermal silicon dioxide, EOT_{elec} is the equivalent electrical oxide thickness in inversion (see Note [4]), and L_g is the physical gate length (see Note [1]). The red and yellow coloring follows that of EOT_{elec} (see Note [4]).

[15] $C_{g,total}$ is the total gate capacitance per micron device width in inversion. This is the sum of $C_{g,ideal}$ and the parasitic gate overlap/fringing capacitance per micron device width [including the Miller effect]. Red and yellow color here follows that of $C_{g,ideal}$.

[16] τ is the intrinsic transistor delay for NMOS devices at 25°C. τ = ($C_{g,total}$ × V_{dd}) / $I_{d,sat}$. τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat}$ ~ (0.4–0.5) × (NMOS $I_{d,sat}$). τ is a reasonable metric for the intrinsic switching delay of the device, while 1/τ is a reasonable metric for the intrinsic switching speed of the device. Red and yellow coloring follows that of both saturation drive current (see Note [9]) and $C_{g,total}$ (see Note [15]).

[17] 1/τ is the NMOS intrinsic switching speed. Maintenance of the historical 17% per year improvement in this parameter is the key scaling goal for high-performance logic. Red and yellow coloring follows that of τ.

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Table PIDS3a Low Standby Power Technology Requirements—Near-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
L_g Physical gate length for LSTP [1]									
Extended Planar Bulk and DG (nm)	45	37	32	28	25	22	20	18	16
UTB FD (nm)						22	20	18	17
EOT Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	19	16	15	14	13	12	11		
UTB FD (Å)						13	12	11	10
DG (Å)						14	13	12	11
Gate Poly Depletion and Inversion-Layer Equivalent Thickness [3]									
Extended planar bulk (Å)	6.2	3.3	3.4	3.3	3.2	3.1	3.1		
UTB FD (Å)						4	4	4	4
DG (Å)						4	4	4	4
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]									
Extended planar bulk (Å)	25.2	19.3	18.4	17.3	16.2	15.1	14.1		
UTB FD (Å)						17	16	15	14
DG (Å)						18	17	16	15
$J_{g,limit}$ Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm^2)	6.67E-02	8.11E-02	9.38E-02	1.07E-01	1.20E-01	1.36E-01	1.50E-01		
UTB FD (A/cm^2)						1.36E-01	1.50E-01	1.67E-01	1.76E-01
DG (A/cm^2)						1.36E-01	1.50E-01	1.67E-01	1.88E-01
V_{dd} Power Supply Voltage (V) [6]									
Extended Planar Bulk (V)	1.1	1.1	1	1	1	1	0.95		
UTB FD (V)						0.9	0.9	0.9	0.85
DG (V)						0.85	0.85	0.85	0.8
$V_{t,sat}$ Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	534	567	535	535	544	552	547		
UTB FD (mV)						395	399	401	404
DG (mV)						380	362	361	366
$I_{sd,leak}$ Source/Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (µA/µm)	3.03E-05	3.03E-05	3.05E-05	3.07E-05	3.02E-05	3.02E-05	3.03E-05		
UTB FD (µA/µm)						3.14E-05	3.09E-05	3.17E-05	3.02E-05
DG (µA/µm)						1.15E-05	2.44E-05	2.82E-05	2.65E-05
$I_{d,sat}$ NMOS Drive Current [9]									
Extended Planar Bulk (µA/µm)	465	569	501	528	542	560	519		
UTB FD (µA/µm)						608	669	744	786
DG (µA/µm)						550	612	674	702
Mobility enhancement factor due to strain [10]									
Extended Planar Bulk	1.8	1.8	1.8	1.8	1.8	1.8	1.8		
UTB FD and DG						1.4	1.8	1.8	1.8

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Table PIDS3a Low Standby Power Technology Requirements—Near-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
$I_{d,sat}$ enhancement factor due to strain [11]									
Extended Planar Bulk	1.19	1.17	1.16	1.17	1.17	1.16	1.17		
UTB FD						1.04	1.07	1.07	1.07
DG						1.03	1.05	1.05	1.05
Effective Ballistic Enhancement Factor [12]									
Extended Planar Bulk	1	1	1	1	1	1	1		
UTB FD						1	1	1	1.1
DG						1	1	1	1.1
R_{sd} Effective Parasitic series source/drain resistance [13]									
Extended Planar Bulk (Ω-µm)	180	180	180	180	180	180	180		
UTB FD (Ω-µm)						200	200	180	160
DG (Ω-µm)						210	210	200	200
$C_{g,ideal}$ Ideal NMOS Device Gate Capacitance [14]									
Extended Planar Bulk (F/µm)	6.17E-16	6.62E-16	6.01E-16	5.58E-16	5.32E-16	5.02E-16	4.90E-16		
UTB FD (F/µm)						4.46E-16	4.31E-16	4.14E-16	4.19E-16
DG (F/µm)						4.22E-16	4.06E-16	3.88E-16	3.68E-16
$C_{g,total}$ Total gate capacitance for calculation of CV/I [15]									
Extended Planar Bulk (F/µm)	8.57E-16	9.02E-16	8.21E-16	7.68E-16	7.32E-16	6.92E-16	6.70E-16		
UTB FD (F/µm)						6.86E-16	6.71E-16	6.54E-16	6.39E-16
DG (F/µm)						6.62E-16	6.46E-16	6.28E-16	6.08E-16
$\tau = CV/I$ NMOSFET intrinsic delay (ps) [16]									
Extended Planar Bulk (ps)	2.03	1.74	1.64	1.46	1.35	1.24	1.23		
UTB FD (ps)						1.02	0.9	0.79	0.69
DG (ps)						1.02	0.9	0.79	0.69
$1/\tau$ NMOSFET intrinsic switching speed (GHz) [17]									
Extended Planar Bulk (GHz)	493	575	610	685	741	806	813		
UTB FD (GHz)						980	1111	1266	1449
DG (GHz)						980	1111	1266	1449

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



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Table PIDS3b Low Standby Power Technology Requirements—Long-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5*	*4.5*
L_g Physical gate length for LSTP [1]							
Extended Planar Bulk and DG (nm)	14	13	12	11	10	9	8
UTB FD (nm)	16	15					
EOT Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)	9	8					
DG (Å)	11	10	10	9	9	8	8
Gate Poly Depletion and Inversion-Layer Equivalent Thickness [3]							
Extended planar bulk (Å)							
UTB FD (Å)	4	4					
DG (Å)	4	4	4	4	4	4	4
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]							
Extended planar bulk (Å)							
UTB FD (Å)	13	12					
DG (Å)	15	14	14	13	13	12	12
$J_{g,limit}$ Maximum gate leakage current density [5]							
Extended Planar Bulk (A/cm^2)							
UTB FD (A/cm^2)	1.88E-01	2.00E-01					
DG (A/cm^2)	2.14E-01	2.31E-01	2.50E-01	2.73E-01	3.00E-01	3.33E-01	3.75E-01
V_{dd}: Power Supply Voltage (V) [6]							
Extended Planar Bulk (V)							
UTB FD (V)	0.8	0.8					
DG (V)	0.8	0.8	0.8	0.75	0.75	0.7	0.7
$V_{t,sat}$ Saturation Threshold Voltage [7]							
Extended Planar Bulk (mV)							
UTB FD (mV)	404	405					
DG (mV)	366	371	365	374	378	369	376
$I_{sd,leak}$ Source/Drain Subthreshold Off-State Leakage Current [8]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	3.10E-05	3.27E-05					
DG (µA/µm)	2.97E-05	2.55E-05	3.38E-05	2.62E-05	2.39E-05	3.38E-05	2.89E-05
$I_{d,sat}$ NMOS Drive Current [9]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	771	838					
DG (µA/µm)	738	839	889	895	935	934	946

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Table PIDS3b Low Standby Power Technology Requirements—Long-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5*	*4.5*
Mobility enhancement factor due to strain [10]							
Extended Planar Bulk							
UTB FD and DG	1.8	1.8	1.8	1.8	1.8	1.8	1.8
$I_{d,sat}$ *enhancement factor due to strain [11]*							
Extended Planar Bulk							
UTB FD	1.08	1.07					
DG	1.04	1.04	1.04	1.04	1.04	1.04	1.04
Effective Ballistic Enhancement Factor [12]							
Extended Planar Bulk							
UTB FD	1.15	1.18					
DG	1.15	1.22	1.27	1.4	1.45	1.5	1.55
R_{sd} *Effective Parasitic series source/drain resistance [13]*							
Extended Planar Bulk (Ω-µm)							
UTB FD (Ω-µm)	150	150					
DG (Ω-µm)	200	180	180	170	160	140	140
$C_{g,ideal}$ *Ideal NMOS Device Gate Capacitance [14]*							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	4.25E-16	4.31E-16					
DG (F/µm)	3.22E-16	3.20E-16	2.96E-16	2.92E-16	2.65E-16	2.59E-16	2.30E-16
$C_{g,total}$ *Total gate capacitance for calculation of CV/I [15]*							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	6.25E-16	6.31E-16					
DG (F/µm)	5.62E-16	5.60E-16	5.26E-16	5.02E-16	4.65E-16	4.49E-16	4.20E-16
$\tau = CV/I$ *NMOSFET intrinsic delay (ps) [16]*							
Extended Planar Bulk (ps)							
UTB FD (ps)	0.65	0.6					
DG (ps)	0.61	0.53	0.47	0.42	0.37	0.34	0.31
$1/\tau$ *NMOSFET intrinsic switching speed (GHz) [17]*							
Extended Planar Bulk (GHz)							
UTB FD (GHz)	1538	1667					
DG (GHz)	1639	1887	2128	2381	2703	2941	3226

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Table PIDS3c Low Operating Power Technology Requirements—Near-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
L_g Physical gate length for LOP (nm) [1]	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
EOT Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	12	11	10	9	8	8			
UTB FD (Å)					9	9	8	8	8
DG (Å)					9	9	9	8	8
Gate Poly Depletion and Inversion-Layer Equivalent Thickness [3]									
Extended planar bulk (Å)	6.4	3.4	3.3	3.4	3.3	3.2			
UTB FD (Å)					4	4	4	4	4
DG (Å)					4	4	4	4	4
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]									
Extended planar bulk (Å)	18.4	14.4	13.3	12.4	11.3	11.2			
UTB FD (Å)					13	13	12	12	12
DG (Å)					13	13	13	12	12
$J_{g,limit}$ Maximum gate leakage current density [5]									
Extended Planar Bulk (A/ cm^2)	78	89	100	114	125	139			
UTB FD (A/ cm^2)					125	139	156	179	192
DG (A/ cm^2)					125	139	156	179	192
V_{dd} Power Supply Voltage (V) [6]									
Extended Planar Bulk (V)	0.8	0.8	0.8	0.7	0.7	0.7			
UTB FD (V)					0.7	0.7	0.6	0.6	0.6
DG (V)					0.7	0.7	0.6	0.6	0.6
$V_{t,sat}$ Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	294	296	289	259	246	249			
UTB FD (mV)					218	209	195	202	202
DG (mV)					207	202	203	201	202
$I_{sd,leak}$ Source/Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (µA/µm)	9.08E-03	7.35E-03	8.96E-03	1.83E-02	2.55E-02	3.57E-02			
UTB FD (µA/µm)					8.32E-03	1.19E-02	2.02E-02	1.86E-02	1.98E-02
DG (µA/µm)					5.84E-03	7.73E-03	8.61E-03	1.07E-02	1.10E-02
$I_{d,sat}$ NMOS Drive Current [9]									
Extended Planar Bulk (µA/µm)	563	705	760	682	754	760			
UTB FD (µA/µm)					766	788	747	763	810
DG (µA/µm)					780	821	754	826	893
Mobility enhancement factor due to strain [10]	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
$I_{d,sat}$ enhancement factor due to strain [11]									
Extended Planar Bulk	1.15	1.11	1.11	1.11	1.1	1.09			
UTB FD					1.07	1.07	1.07	1.06	1.06
DG					1.05	1.05	1.05	1.05	1.04

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Table PIDS3c Low Operating Power Technology Requirements—Near-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Effective Ballistic Enhancement Factor [12]									
Extended Planar Bulk	1	1	1	1	1	1			
UTB FD					1	1	1.09	1.1	1.15
DG					1	1	1.15	1.18	1.25
R_{sd} *Effective Parasitic series source/drain resistance [13]*									
Extended Planar Bulk (Ω-μm)	190	190	190	190	190	190			
UTB FD (Ω-μm)					190	190	180	170	165
DG (Ω-μm)					190	180	180	180	170
$C_{g,ideal}$ *Ideal NMOS Device Gate Capacitance [14]*									
Extended Planar Bulk (F/μm)	6.01E-16	6.70E-16	6.48E-16	6.13E-16	6.12E-16	5.54E-16			
UTB FD (F/μm)					5.31E-16	4.78E-16	4.60E-16	4.02E-16	3.74E-16
DG (F/μm)					5.31E-16	4.78E-16	4.25E-16	4.02E-16	3.74E-16
$C_{g,total}$ *Total gate capacitance for calculation of CV/I [15]*									
Extended Planar Bulk (F/μm)	8.41E-16	9.10E-16	8.78E-16	8.13E-16	8.12E-16	7.54E-16			
UTB FD (F/μm)					7.51E-16	6.88E-16	6.60E-16	6.02E-16	5.54E-16
DG (F/μm)					7.71E-16	7.18E-16	6.65E-16	6.43E-16	6.14E-16
$\tau = CV/I$ *NMOSFET intrinsic delay (ps) [16]*									
Extended Planar Bulk (ps)	1.19	1.03	0.92	0.83	0.75	0.69			
UTB FD (ps)					0.69	0.61	0.53	0.47	0.41
DG (ps)					0.69	0.61	0.53	0.47	0.41
$1/\tau$ *NMOSFET intrinsic switching speed (GHz) [17]*									
Extended Planar Bulk (GHz)	840	971	1087	1205	1333	1449			
UTB FD (GHz)					1449	1639	1887	2128	2439
DG (GHz)					1449	1639	1887	2128	2439

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



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Table PIDS3d Low Operating Power Technology Requirements—Long-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5*	*4.5*
L_g Physical gate length for LOP (nm) [1]	***11***	***10***	***9***	***8***	*7*	***6.5***	***6***
EOT Equivalent Oxide Thickness [2]							
Extended planar bulk (Å)							
UTB FD (Å)	7						
DG (Å)	8	7	7	7	7	6	6
Gate Poly Depletion and Inversion-Layer Equivalent Thickness [3]							
Extended planar bulk (Å)							
UTB FD (Å)	4						
DG (Å)	4	4	4	4	4	4	4
EOT_{elec} Electrical Equivalent Oxide Thickness in inversion [4]							
Extended planar bulk (Å)							
UTB FD (Å)	11						
DG (Å)	12	11	11	11	11	10	10
$J_{g,limit}$ Maximum gate leakage current density [5]							
Extended Planar Bulk (A/ cm^2)							
UTB FD (A/ cm^2)	227						
DG (A/ cm^2)	227	250	278	313	357	385	417
V_{dd} Power Supply Voltage (V) [6]							
Extended Planar Bulk (V)							
UTB FD (V)	0.5						
DG (V)	0.6	0.5	0.5	0.5	0.5	0.45	0.45
$V_{t,sat}$ Saturation Threshold Voltage [7]							
Extended Planar Bulk (mV)							
UTB FD (mV)	187						
DG (mV)	202	188	194	190	195	190	201
$I_{sd,leak}$ Source/Drain Subthreshold Off-State Leakage Current [8]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	3.71E-02						
DG (µA/µm)	1.31E-02	2.23E-02	1.94E-02	2.55E-02	2.41E-02	3.26E-02	2.40E-02
$I_{d,sat}$ NMOS Drive Current [9]							
Extended Planar Bulk (µA/µm)							
UTB FD (µA/µm)	716						
DG (µA/µm)	916	808	850	900	919	874	876
Mobility enhancement factor due to strain [10]	1.8	1.8	1.8	1.8	1.8	1.8	1.8
$I_{d,sat}$ enhancement factor due to strain [11]							
Extended Planar Bulk							
UTB FD	1.06						
DG	1.04	1.04	1.04	1.04	1.03	1.03	1.03

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Table PIDS3d Low Operating Power Technology Requirements—Long-term Years

Grey cells delineate one of two time periods either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion).

Year in Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*22*	*20*	*18*	*16*	*14*	*13*	*11*
MPU Physical Gate Length (nm)	*9*	*8*	*7*	*6.3*	*5.6*	*5*	*4.5*
Effective Ballistic Enhancement Factor [12]							
Extended Planar Bulk							
UTB FD	1.24						
DG	1.27	1.35	1.43	1.45	1.5	1.6	1.68
R_{sd} *Effective Parasitic series source/drain resistance [13]*							
Extended Planar Bulk (Ω-µm)							
UTB FD (Ω-µm)	160						
DG (Ω-µm)	170	155	150	140	140	140	140
$C_{g,ideal}$ *Ideal NMOS Device Gate Capacitance [14]*							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	3.14E-16						
DG (F/µm)	3.16E-16	3.14E-16	2.82E-16	2.51E-16	2.20E-16	2.24E-16	2.07E-16
$C_{g,total}$ *Total gate capacitance for calculation of CV/I [15]*							
Extended Planar Bulk (F/µm)							
UTB FD (F/µm)	5.15E-16						
DG (F/µm)	5.56E-16	5.24E-16	4.82E-16	4.41E-16	4.10E-16	4.14E-16	3.97E-16
$\tau = CV/I$ *NMOSFET intrinsic delay (ps) [16]*							
Extended Planar Bulk (ps)							
UTB FD (ps)	0.36						
DG (ps)	0.36	0.32	0.28	0.24	0.22	0.21	0.2
$1/\tau$ *NMOSFET intrinsic switching speed (GHz) [17]*							
Extended Planar Bulk (GHz)							
UTB FD (GHz)	2778						
DG (GHz)	2778	3125	3571	4167	4545	4762	5000

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables PIDS3a through d

As described in the text, MASTAR[1,2,3], a detailed analytical MOSFET modeling software package, has been utilized to generate the parameter values in these tables. The MASTAR modeling package and user's manual are in the backup material on the ITRS website, as well as the detailed MASTAR simulations that underlay these tables. Also note that the parameters in this table are for an NMOSFET with nominal gate length at an operating temperature of 25°C. Furthermore, although there are multiple MOSFETs in a typical logic chip, with differing threshold voltages, Ion, Ioff, and oxide thickness, for LSTP logic the transistor specified in this table is the transistor with the highest threshold voltage, lowest Ion and Ioff, highest oxide thickness, and slowest intrinsic transistor speed. The majority of the transistors on the chip are of this type, in order to keep the leakage and static power dissipation within tolerable limits. This transistor is specified here because it drives the technology. In contrast, for LOP logic, the transistor specified in this table is the "standard" transistor, with intermediate threshold voltage, I_{on}, and I_{off}. The majority of the transistors on the chip are of this type, because the performance requirements are critical, and standby power dissipation is less critical than for LSTP. Dynamic power dissipation is critical here, and V_{dd} is rapidly scaled to keep this within tolerable limits. This transistor is specified here because it drives the technology.

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As explained in the text, multiple parallel options for the transistor type are included in the tables, including planar bulk CMOS extended to its practical scaling limits, ultra-thin body fully-depleted (UTB FD) SOI CMOS, also extended to its practical scaling limits, and double-gate (DG) CMOS (e.g., FinFETs). Note that, for LOP, the limit for planar bulk CMOS is through 2012, and for UTB FD is through 2016. UTB FD and DG start in 2011, with overlap of the three options from 2011 through 2012. In contrast, for LSTP, the limit for planar bulk CMOS is through 2013, and UTB FD continues through 2017. UTB FD and DG start in 2012, with overlap of the three options from 2012 through 2013.

For each transistor option, the scaling of the numbers in the tables reflects a particular scaling scenario in which we have attempted to optimally scale to meet the key goals while keeping the performance, short channel effects, and other key characteristics under control. For LSTP, the key goal is ultra-low leakage current, while for LOP the goal is relatively high speed and low dynamic power dissipation, along with low leakage current (but not as low as for LSTP). However, there are numerous parameters (such as EOT, V_{dd}, $I_{sd,leak}$, etc.) that can be varied, and different scaling scenarios are possible by making different choices on the scaling of these parameters. The scenarios in this table were selected to be as representative of the industry as possible. In particular, in these tables, high-κ gate dielectric and metal gate electrode are assumed to be available in 2008. See the figures and discussion in the text for why high-κ gate dielectric is required in 2008.

[1] L_g is the physical gate length the final, as-etched length of the bottom of the gate electrode. The values here lag behind the gate length values for high- performance logic by two years (LOP) or four years (LSTP) in order to meet the stringent leakage current requirements. For LSTP, for UTB FD devices, late in the ITRS L_g scaling lags slightly behind that for DG MOSFETs. This is because of the difficulty in scaling UTB FD MOSFETs and keeping the leakage current within tolerance for such short devices. The gate dimensional control requirement is set by the Lithography and FEP Etch ITWGs, and is assumed to have a three-sigma value of ± 12% × L_g. It is expected that meeting this requirement will become increasingly difficult with scaling (refer to the Lithography chapter and the FEP Chapter). Gate length variation is assumed to be a primary factor responsible for driving device parameter variation.

[2] EOT for a gate dielectric of thickness T_d and relative dielectric constant κ EOT is defined by EOT = T_d / (κ /3.9), where 3.9 is the relative dielectric constant of thermal silicon dioxide. For a MOSFET with the gate dielectric of thickness T_d, the ideal gate capacitance per unit area is the same as that of a similar MOSFET, but with a gate dielectric made up of thermal silicon dioxide with a thickness of EOT. It is projected that high-κ gate dielectric will be required by 2008 to control the gate leakage (see the text for further discussion on this point.) The yellow coloring reflects the uncertainty in our high-κ solutions for EOT < 0.9nm, while the red coloring reflects the increased uncertainty of solutions for EOT < 0.7nm. Measurement of EOT is complicated, and is usually done via sophisticated MOS capacitor-voltage (CV) measurements on MOS capacitors or via optical measurements.

[3] Gate Poly Depletion and Inversion-Layer Equivalent Thickness accounts for gate electrode depletion and inversion-layer effects, including quantum effects, both of which are calculated by MASTAR. For polysilicon gate electrodes, the portion of the electrical thickness adjustment due to gate electrode depletion is dependent on the polysilicon doping. For 2008 and beyond, it is assumed that metal-gate electrodes, which reduce the gate depletion effect to zero, will be introduced. The abrupt reduction in this parameter for 2008 reflects the zero depletion. For 2008 and beyond, the difference between the parameter value for planar bulk versus the 4 nm value for DG and UTB FD reflects the light channel doping in the latter types of MOSFET and the heavy channel doping in planar bulk. For planar bulk CMOS, the metal gate work function needs to be near the silicon conduction band edge for NMOS and near the silicon valence band edge for PMOS to properly set the MOSFET threshold voltage, as with polysilicon gates. For UTB FD and DG MOSFETs, the channel is very thin and lightly doped, and the work function of the metal gates needs to be within a few hundred millivolts of the silicon midgap (i.e., "near silicon midgap" work function) to properly set the MOSFET's threshold voltage. Multiple V_t's may be obtained by tuning the work function. The yellow and red colors generally follow that of EOT (see Note [2] above), reflecting the tight coupling between the metal gate electrode and the high-κ gate dielectric. For UTB FD and DG, the color is red, reflecting the uncertainties of setting and tuning the effective work function.

[4] EOT_{elec} is the sum of EOT and gate poly depletion and inversion-layer thickness (see Notes [2] and [3] above). For MOSFETs in inversion, ideal gate capacitance per unit area (see Note [14]) is $\varepsilon_{ox} / (EOT_{elec})$, where ε_{ox} is the dielectric constant of thermal silicon dioxide. The equivalent electrical oxide thickness in inversion is used in calculations of the transistor intrinsic delay, CV/I (see Note [16]). Red/yellow coloring follows that of EOT and gate poly depletion and inversion-layer thickness.

[5] $J_{g,limit}$ is the maximum allowed gate leakage current density at 25°C, and it is measured with the gate biased to V_{dd} and the source, drain, and substrate all set to ground. $J_{g,limit}$ is related to $I_{sd,leak,TGT}$, the nominal subthreshold leakage current target at 25°C . $I_{sd,leak,TGT}$ is set to 30 pA/micron device width for LSTP and to 5nA/micron device width for LOP. Specifically, $J_{g,limit} = [I_{sd,leak,TGT} / L_g] \times$ [Hi T Factor] / [Circuit Factor]. For LOP, Hi T Factor is set to 5, and it accounts for the high operating temperature (well over room temperature, but not as high as the 100°C for high-performance logic, where Hi T Factor = 10). Hi T Factor accounts for both the rapid increase in $I_{sd,leak}$ with temperature and the insensitivity of gate leakage current (since it is due to direct tunneling) to temperature. For LSTP, where the operating temperature is expected to be room temperature, Hi T Factor = 1. The Circuit Factor is set to 1, and it accounts for the differences between the subthreshold leakage current and the gate leakage current in logic gates compared to single isolated transistors as specified by the $J_{g,limit}$ and $I_{sd,leak}$ parameters in this table. (The reason for these differences is the different bias conditions on the various transistors in logic gates compared to the bias conditions used to define $I_{sd,leak}$ (see Note [8]) and $J_{g,limit}$ for the NMOS transistor in this table). The values of Hi T Factor and Circuit Factor used here are rough estimates. The yellow and red coloring follows that of EOT (see Note [2] above).

[6] V_{dd} is the nominal power supply voltage. It has been chosen to maintain sufficient voltage over-drive [V_{dd} – saturation threshold voltage (see Note [7]) in order to meet the required saturation current drive values while still maintaining reasonable vertical gate dielectric electric field strengths. Target power supply voltage values for actual ICs may vary ± 10% (or more) from the values in this table, depending on the particular circuit design application or technology optimization. Note that V_{dd} is relatively high and scales slowly for LSTP, because the saturation threshold voltage is high here to keep the subthreshold leakage current very low. On the other hand, for LOP V_{dd} scales down rapidly in order to keep the dynamic power dissipation low.

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[7] $V_{t,sat}$ is the saturation threshold voltage for a nominal gate length transistor with drain bias set equal to V_{dd}, as calculated by MASTAR. The threshold voltage values and the corresponding subthreshold leakage current values (see Note [8]) have been chosen to maintain sufficient voltage over-drive (V_{dd} – saturation threshold voltage) in order to meet the required saturation current drive values (see Note [9]). For planar bulk, the yellow color is associated with high substrate doping exceeding 4E18cm^{-3} (from MASTAR), while the red color is associated with very high substrate doping exceeding 6E18 cm^{-3}. These doping levels are required to set the threshold voltage to the desired level and to keep short channel effects under control. For UTB FD devices, the color is red from the beginning because of the challenges of controlling the very thin silicon body thickness (right from the beginning, ~7 nm for LOP and < 7 nm for LSTP) required to control $V_{t,sat}$ and short channel effects. For DG devices, the color is red right from the beginning because there are numerous issues that are not understood here; in particular, defining and controlling the fin width, which is typically ~0.6 L_g, is a major challenge. The required silicon body thickness for UTB FD and the fin width for DG come from MASTAR.

[8] $I_{sd,leak}$ subthreshold leakage current is defined as the NMOSFET source current per micron of device width, at 25°C, with the drain bias set equal to V_{dd} and with the gate, source, and substrate biases set to zero volts. Total NMOS off-state leakage current (I_{off}) is the NMOSFET drain current per micron of device width at 25°C, and is the sum of the NMOS subthreshold, gate, and junction leakage current (which includes band-to-band tunneling and gate induced drain leakage [GIDL]) components). The subthreshold leakage current is assumed to be larger than the junction leakage current component at either 25°C or high-temperature conditions, but see Note [5] for the relation between $I_{sd,leak}$ and gate leakage current density. The yellow and red coloring follows that of the $V_{t,sat}$ (see Note [7] above) because $V_{t,sat}$ is a critical determinant of $I_{sd,leak}$. The above subthreshold, gate, and junction leakage current scaling scenario also applies to PMOS devices. For LSTP, meeting the $I_{sd,leak}$ target of ~30pA/µm is the key scaling goal.

[9] $I_{d,sat}$ saturation drive current is defined as the NMOSFET drain current per micron device width with the gate bias and the drain bias set equal to V_{dd} and the source and substrate biases set to zero. PMOS saturation drive current value is assumed to be (40–50)% of the NMOS saturation drive current value. Yellow/red coloring follows that of four items the parasitic source/drain series resistance, R_{sd} (see Note [13] below), the equivalent electrical oxide thickness in inversion (see Note [4]), the mobility enhancement factor (see Note [10]), and the ballistic enhancement factor (see Note [12]).

[10] Mobility Enhancement Factor due to Strain (μ_{ratio}). μ_{ratio} = [enhanced mobility]/[reference mobility], where [enhanced mobility] is the actual mobility including the enhancement due to strain, and [reference mobility] is the mobility in the absence of enhancement. Following the literature, the value of μ_{ratio} is limited to a maximum of 1.8[10]. Mobility enhancement was implemented in product in 2004[11] to meet the required saturation drive current, and hence the coloring for extended planar bulk is initially white. However, there are numerous approaches in the literature for mobility enhancement (including global strain using thin silicon epitaxial layers on SiGe epitaxial layers[12], different process induced strain approaches such as strained thin overlayers of SiN, selective epitaxial SiGe in the PMOS S/D and selective epitaxial Si C in the NMOS S/D, hybrid orientations, etc.[13,14]). As we continue to scale MOSFETs, it becomes more difficult to maintain the strain, and it is unclear what the optimal approach(es) will be and how to integrate them into the process flow. The cells are colored yellow when L_g=20 nm. For UTB FD and DG, the color is red because strain and enhanced mobility are less well understood in these structures.

[11] Mobility Enhancement Factor for $I_{d,sat}$ captures the improvement in the saturation drive current due to mobility enhancement from strain. This factor is defined as [enhanced $I_{d,sat}$]/$I_{d,ref}$ = $I_{d,ratio}$, where [enhanced $I_{d,sat}$] is the actual saturation drive current including the impact of enhanced mobility and $I_{d,ref}$ is the saturation drive current in the absence of mobility enhancement. MASTAR calculates $I_{d,ratio}$ as a function of the mobility enhancement factor, μ_{ratio} (see Note [10]). Generally, $I_{d,ratio}$ is significantly less than μ_{ratio} due to short channel effects and velocity saturation. The yellow or red coloring follows that for μ_{ratio} (Note [10]).

[12] Effective Ballistic Enhancement Factor is a multiplying factor for $I_{d,sat}$, reflecting quasi-ballistic enhanced transport (due largely to enhanced injection at the source) in highly scaled, ultra-thin body MOSFETs, both UTB FD SOI and DG MOSFETs. Planar bulk CMOS presumably does not have ballistic enhancement because of high doping in these devices. Values for this factor greater than 1 reflect quasi-ballistic enhancement. The value of this parameter is driven by the required saturation drive current to meet performance requirements. The red coloring reflects the lack of known enhanced quasi-ballistic transport solutions for transistors.

[13] R_{sd} is the maximum allowable parasitic series source plus drain resistance (i.e., total resistance for the two sides) per micron of MOSFET width. The values are scaled to allow the required saturation current drive values (see Note [9]) to be met. Yellow/red coloring reflects FEP TWG projections on contact resistance, salicide sheet resistance, and drain extension scaling. The R_{sd} values have been increased from the 2005 ITRS, based on updated information.

[14] $C_{g,ideal}$ is the ideal gate capacitance per micron device width, in inversion. $C_{g,ideal}$ =[ε_{ox}/(EOT_{elec})] × L_g, where ε_{ox} is the dielectric constant of thermal silicon dioxide, EOT_{elec} is the equivalent electrical oxide thickness in inversion (see Note [4]), and L_g is the physical gate length (see Note [1]). The red/yellow coloring follows that of EOT_{elec} (see Note [4]).

[15] $C_{g,total}$ is the total gate capacitance per micron device width in inversion. This is the sum of $C_{g,ideal}$ and the parasitic gate overlap/fringing capacitance per micron device width [including the Miller effect]. Red/yellow color here follows that of $C_{g,ideal}$.

[16] τ is the intrinsic transistor delay for NMOS devices at 25°C. τ = ($C_{g,total}$ × V_{dd}) / $I_{d,sat}$. τ for PMOSFETs is assumed to scale similarly, but with PMOS $I_{d,sat}$ ~ (0.4–0.5) × (NMOS $I_{d,sat}$). τ is a reasonable metric for the intrinsic switching delay of the device, while 1/τ is a reasonable metric for the intrinsic switching speed of the device. Red/yellow coloring follows that of both saturation drive current (see Note [9]) and $C_{g,total}$ (see Note [15]).

[17] 1/τ is the NMOS intrinsic switching speed. Red/yellow coloring follows that of τ.

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LOGIC POTENTIAL SOLUTIONS

There is a strong correlation between the challenges indicated by the colors in the technology requirements tables and the potential solutions (see Figure PIDS5). In many cases, red coloring (manufacturable solutions are not known) in the technology requirements tables corresponds to the projected year of introduction for a potential solution to the challenge indicated by these colors. Another important general point is that each potential solution highlighted in the Potential Solutions figure involves significant technological innovation. The qualification/pre-production interval has been set to one and a half years in order to understand and deal with any new and different reliability, yield, and process integration issues associated with these innovative solutions. Most of the potential solutions, with the exception of high-κ gate dielectric and metal gate electrodes, are required first for high-performance logic. Finally, the industry faces a major overall challenge due to the sheer number of major technological innovations required over the next five years: enhanced mobility (already implemented but requiring continuous improvement with scaling), high-κ gate dielectric, metal gate electrodes, ultra-thin body, fully depleted SOI and multiple-gate MOSFETs with quasiballistic enhanced transport.

The first potential solution, enhanced mobility due to strain, is needed to enhance the saturation current drive to meet transistor performance targets. (Note that, in the Logic Technology Requirements tables, significantly enhanced mobility is assumed in the projections.) It was first implemented in 2004 for high-performance logic. There are numerous techniques to implement enhanced mobility, including via various types of process-induced local strain or by globally induced strain in a thin strained silicon layer, either on relaxed SiGe layers with controlled percentages of Ge or in SOI substrates. Other approaches include use of hybrid orientations (e.g., PMOSFET mobility is highest for the (110) substrate orientation) or use of strained SiGe or (eventually) strained Ge channels. The potential solutions figure indicates that continuous improvement will be needed here, to increase the mobility enhancement to the maximum extent possible for both NMOSFET and PMOSFET transistors, to integrate mobility enhancement optimally with the overall process flow, and eventually to utilize mobility enhancement for advanced MOSFETs such as UTB SOI and multiple-gate MOSFETs. In addition, continuous improvement will be needed to deal with the reduced effectiveness of process-induced strain techniques with scaling: as the spacing between transistors is reduced with scaling, techniques such as embedded SiGe or Si:C in the source/drain and the addition of stressed thin film silicon nitride liner layers over the top of the transistor tend to becomes less effective at inducing stress in the channel.

In order to scale the basic MOSFET structure significantly beyond 2007 (corresponding to physical gate length of 25 nm for high-performance logic), key technology issues involving the current standard device gate stack (silicon oxy-nitride gate dielectric and doped polysilicon gate electrode) need to be addressed. As the physical gate length is scaled, ideally the gate dielectric equivalent oxide thickness (EOT) is scaled correspondingly to control short-channel effects and to increase the saturation current drive. However, continued thinning of the silicon oxy-nitride results in a significant increase in gate leakage current due to an approximately exponential increase in the direct tunneling current(see Figures PIDS2-4). In addition, the effectiveness of continued EOT reduction becomes limited due to the non-scalability of gate electrode depletion and inversion layer effects, which both increase the equivalent electrical oxide thickness in inversion. High-κ gate dielectric material is a potential solution to solve the problem of high gate leakage current, since the gate leakage current density corresponding to a given EOT is much smaller for high-κ than for oxy-nitride gate dielectric. For all three logic types, it is projected that high-κ gate dielectric will be required by 2008 (see the discussion in the logic technology requirements section for more detail.) For all three logic types, metal gate electrodes are also projected for 2008, in order to effectively prevent gate electrode depletion and hence allow acceptable scaling of the equivalent electrical oxide thickness in inversion. To set the threshold voltage correctly for planar bulk CMOS, the gate electrode work function needs to be near the silicon valence band edge for PMOSFETs and near the silicon conduction band edge for NMOSFETs. Hence, different metals will probably be needed for the PMOSFET and NMOSFET.

As scaling proceeds, it will become increasingly difficult to effectively scale planar bulk CMOS devices. In particular, adequately controlling short channel effects is projected to become especially problematical for such short channel devices. Furthermore, the channel doping will need to be increased to exceedingly high values, which will tend to reduce the mobility and to cause high leakage current due to band-to-band tunneling between the drain and the body. Finally, the total number of dopants in the channel for such small MOSFETs becomes relatively small, which results in large random fluctuations in the dopant placement and number, and hence unacceptably large statistical variation of the threshold voltage. These difficulties become worse with further scaling. A potential solution is to utilize ultra-thin body, fully depleted (UTB FD) SOI MOSFETs. The channel doping is relatively light, and for such devices, the threshold voltage can be set by adjusting the work function of the gate electrode, rather than by doping the channel as in planar bulk MOSFETs. Metal gate electrodes with near-midgap work functions will be needed to set the threshold voltage to the desired values. Because of the different work functions in this case, the electrode material will presumably be different than those utilized for planar bulk MOSFETs. In fact, one electrode material with work function tunable within several hundred meV on either side of midgap may be possible. Due to the lightly doped and fully depleted channel, the threshold

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voltage control by the work function of the gate electrode, and the ultra-thin body, these SOI MOSFETs are considerably more scalable and develop more saturation drive current than comparable planar bulk MOSFETs. Single gate SOI MOSFETs are projected for 2010 for high-performance logic. Multiple-gate, ultra-thin body, fully depleted MOSFETs are both more complex and more scalable, and are projected to be implemented in 2011 for high-performance logic. As the gate length is scaled well below 20 nm, the fully depleted, lightly doped MOSFETs are likely to require enhanced quasi-ballistic transport to meet the performance requirements (see Row 12 of the Logic Technology Requirements tables for detailed numbers). These enhancements will be obtained through reduced scattering and particularly through improved injection at the source. Eventually, late in the Roadmap, more forward-looking solutions, such as utilization of high transport materials for the channel (e.g., Ge or III-V or silicon-based nanowire structures or carbon nanotubes) to further enhance the transport, may be adopted.

Finally, at the end of the Roadmap or beyond, MOSFET scaling will likely become ineffective and/or very costly, and novel, non-CMOS (emerging research) devices and/or circuits/architectures are a potential solution then (see Emerging Research Devices section for detailed discussion of these). Such solutions may be integrated, functionally or physically, with a CMOS baseline technology that takes advantage of the high-performance, cost-effective, and very dense CMOS logic that will have been developed and implemented by then.

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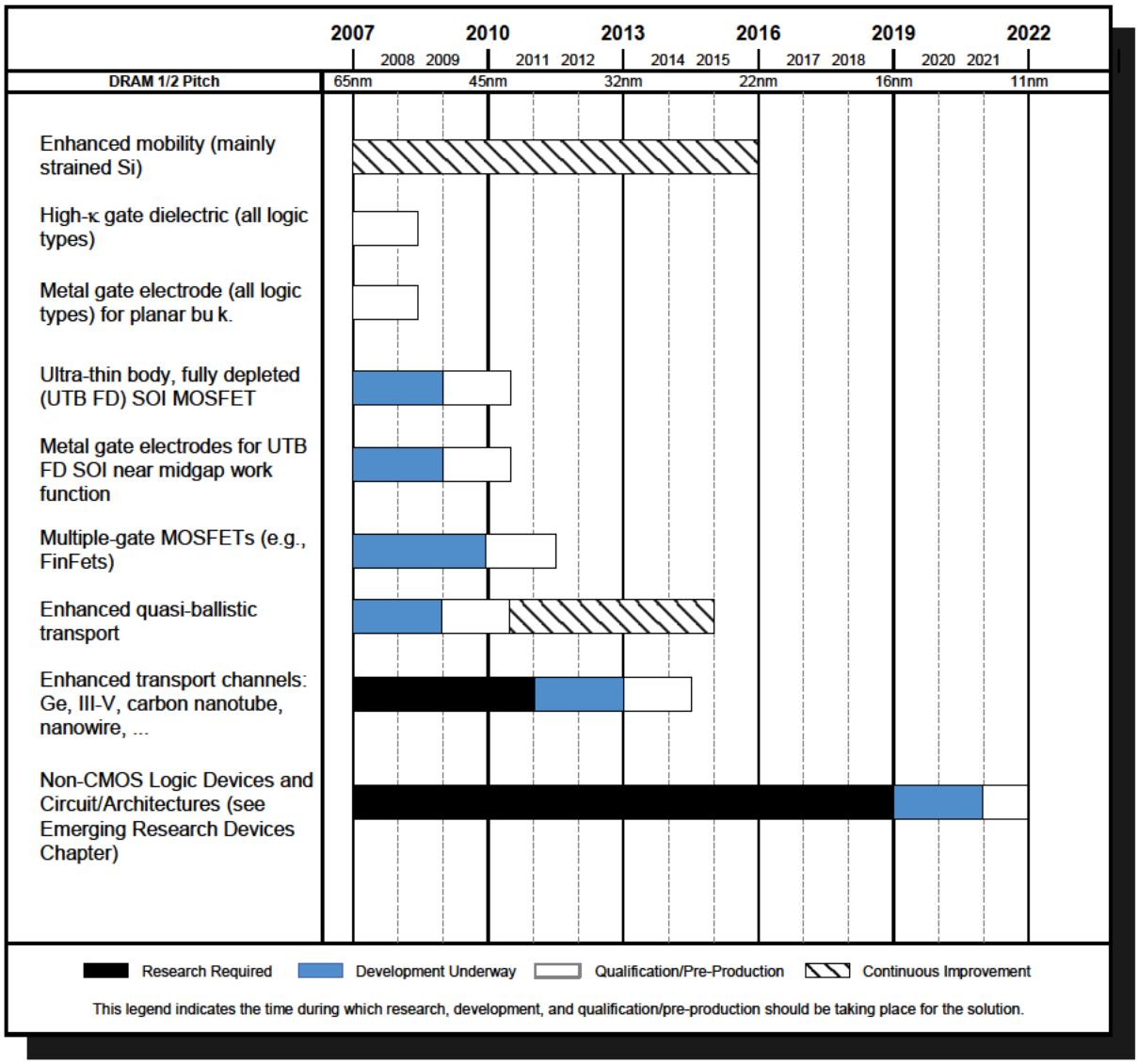


Figure PIDS5 Logic Potential Solutions

MEMORY TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

DRAM

Technical requirements for DRAMs become more difficult with scaling (see Table PIDS4a and b). The process associated with 193 nm argon fluoride (ArF) immersion lithography technology is the key for 60 nm or smaller half pitch DRAMs. However there exist several significant process flow issues for both trench and stack capacitor structures from a production standpoint. Process steps such as capacitor formation or high aspect ratio contact etches require photoresists that can stand up for a prolonged etch time. To overcome these challenges, the technology related to photoresists with a hard mask layer for pattern transfer is gaining in importance. Furthermore, continuous improvements in lithography and etch will be needed.

On the other hand, with the scaling of peripheral CMOS devices, a low temperature process flow is required for process steps after formation of these devices. This is a challenge for DRAM cells with stack capacitors, which are typically constructed after the CMOS devices are formed, and which will therefore be limited to low temperature processing. In addition, the planar access device (cell FET) for the one transistor-one capacitor (1T-1C) cell is getting difficult to design due to the need to maintain a low level of both subthreshold leakage and junction leakage current to meet the retention time requirements. Recessed channel cell FET is being adapted for 80 nm or smaller half pitch DRAMs. Furthermore,

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Fin-type cell FET is needed for the 50 nm half pitch and beyond to meet the high drive current requirement with low voltage operation. Another challenge is a highly reliable gate insulator. A highly boosted gate voltage is required to drive higher drain current with the relatively high threshold voltage adopted for the cell FET to suppress the subthreshold leakage current. The scaling of the DRAM cell FET dielectric, maximum word line (WL) level, and the electric field in the cell FET dielectric is plotted in Figure PIDS6. Because of the gate insulator reliability concerns, the EOT is relatively large, and the equivalent electric field in the dielectric is held approximately constant with scaling, as shown in the figure. Process requirements for DRAMs such as front end isolation, low resistance materials for the word lines, self-aligned and high aspect ratio etches, planarization, and Cu interconnection are all needed for future high density DRAMs.

Since the DRAM storage capacitor gets physically smaller with scaling, the EOT must scale down sharply to maintain adequate storage capacitance with scaling. To scale the EOT, dielectric materials having high relative dielectric constant (κ) will be needed. Several manufacturers have introduced MIM (Metal Insulator Metal) capacitors using HfSiO and Al_2O_3 (κ~ 10–25) for DRAMs with 70 nm ½ pitch in 2006. Eventually, in 2010, MIM structures and dielectric materials with even higher κ values such as ZrO_2 will be adopted.. Finally, it is expected that very high κ values of 50 and greater will be needed later in the Roadmap (See Figure PIDS8, DRAM Potential Solutions, for details). Also, the physical thickness of the high-κ insulator should be scaled down to fit the minimum feature size. All in all, maintaining sufficient storage capacitance will pose an increasingly difficult requirement for continued scaling of DRAM devices. The scaling of DRAM storage node cell dielectric, DRAM storage node capacitor voltage, and equivalent electric field of the storage capacitor dielectric is plotted in Figure PIDS7. As shown in the figure, the electric field in the capacitor dielectric is expected to increase sharply with scaling, due to aggressive scaling of EOT.

Keeping the chip size approximately constant as the DRAM capacity (number of bits per chip) is increased with scaling is very important from a chip cost point of view. In order to do so, the cell size factor (*a*) scaling (where a = [DRAM cell size]/[DRAM half pitch]) is critically important. Along with the overall technology scaling, some companies have started production of DRAMs with an *a* of 6 in 2006, but the other companies are staying with an *a* of 8 for now. It is expected that more companies will likely move to use an *a* of 6 to shrink chip size further. When *a* is decreased from 8 to 6, the array area efficiency (the ratio of cell storage array to total chip area) is decreased from 0.63 to 0.56 because the peripheral circuit area stays the same. Table PIDS4a and b does not include $a = 4$ because a $4F^2$ memory storage cell structure is not considered feasible yet, even though there are some research papers published.

Table PIDS4a DRAM Technology Requirements—Near-term Years

Year in Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
DRAM ½ Pitch (nm) [1]	68	58	50	45	40	36	32	30	25
DRAM cell size (μm^2) [2]	0.0277	0.0202	0.0150	0.0122	0.0096	0.0078	0.0061	0.0054	0.0038
DRAM storage node cell capacitor dielectric equivalent oxide thickness EOT (nm) [3]	1.2	0.90	0.80	0.60	0.50	0.40	0.30	0.30	0.30
DRAM storage node cell capacitor voltage (V) [4]	0.65	0.65	0.60	0.60	0.55	0.55	0.5	0.50	0.45
Equivalent Electric field of capacitor dielectric, (MV/cm) [5]	5.7	7.2	7.5	10.0	11.0	13.8	16.7	16.7	15.0
DRAM cell FET structure [6]	RCAT	RCAT	RCAT	FinFET	FinFET	FinFET	FinFET	FinFET	FinFET
DRAM cell FET dielectric equivalent oxide thickness, EOT (nm) [7]	5.0	5.0	4.5	4.0	4.0	4.0	4.0	4.0	4.0
Maximum Wordline (WL) level (V) [8]	3.0	2.8	2.7	2.7	2.7	2.7	2.6	2.6	2.4
Negative Wordline (WL) use [9]	yes	yes	yes	yes	yes	yes	yes	yes	yes
Equivalent Electric field of cell FET device dielectric (MV/cm) [10]	6.00	5.60	6.00	6.75	6.75	6.75	6.50	6.50	6.00
Cell Size Factor a [11]	6	6	6	6	6	6	6	6	6
Array Area Efficiency [12]	0.56	0.56	0.56	0.56	0.56	0.56	0.56	0.56	0.56
Minimum DRAM retention time (ms) [13]	64	64	64	64	64	64	64	64	64
DRAM soft error rate (fits) [14]	1000	1000	1000	1000	1000	1000	1000	1000	1000
V_{int} (support FET voltage) [V] [15]	1.3	1.2	1.1	1.1	1.1	1.1	1.1	1.0	0.9
Support nMOS EOT [nm] [16]	3.2	3	2.6	2.6	2.5	2.2	2	1.8	1.6
Support PMOS Gate Electrode [17]	P+Poly/W	P+Poly/W	P+Poly/W	P+Poly/W	P+Poly/W	P+Poly/W	P+Poly/W	TiN	TiN
Support Gate Oxide [18]	SiON	SiON	SiON	SiON	SiON	SiON	HfSiON	HfSiON	HfSiON
Support min. L_{gate} for NMOS FET, physical [nm] [19]	100	90	75	75	65	60	50	48	40
Support I_{sat-n} [$\mu A/\mu m$] (25C, $V_g=V_d=V_{int}$) [20]	500	465	470	450	410	430	450	445	440
Support min. V_{tn} (25C, $G_{m,max}$, V_d=55mV) [21]	0.40	0.40	0.38	0.37	0.37	0.33	0.33	0.31	0.31
Support I_{sat-p} [$\mu A/\mu m$] (25C, $Vg=V_d=-V_{int}$) [22]	220	210	220	210	165	170	175	170	190
Support min. V_{tp} (25C, $G_{m,max}$, V_d=55mV) [23]	-0.45	-0.40	-0.38	-0.38	-0.38	-0.34	-0.34	-0.32	-0.32

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



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Table PIDS4b DRAM Technology Requirements—Long-term Years

Year in Production	2016	2017	2018	2019	2020	2021	2022
DRAM ½ Pitch (nm) [1]	22	20	18	16	14	13	12
DRAM cell size (μm^2) [2]	0.0029	0.0024	0.0019	0.00154	0.00118	0.00101	0.00086
DRAM storage node cell capacitor dielectric equivalent oxide thickness EOT (nm) [3]	0.30	0.30	0.30	0.25	0.20	0.15	0.12
DRAM storage node cell capacitor voltage (V) [4]	0.45	0.4	0.4	0.35	0.35	0.35	0.35
Equivalent Electric field of capacitor dielectric, (MV/cm) [5]	15.0	13.3	13.3	14.0	17.5	23.3	29.2
DRAM cell FET structure [6]	FinFET	FinFET	FinFET	FinFET	FinFET	FinFET	FinFET
DRAM cell FET dielectric equivalent oxide thickness, EOT (nm) [7]	3.5	3.5	3.5	3.5	3.5	3.5	3.5
Maximum Wordline (WL) level (V) [8]	2.3	2.3	2.3	2.0	2.0	2.0	2.0
Negative Wordline (WL) use [9]	yes	yes	yes	yes	yes	yes	yes
Equivalent Electric field of cell FET device dielectric (MV/cm) [10]	6.57	6.57	6.57	5.71	5.71	5.71	5.71
Cell Size Factor a [11]	6	6	6	6	6	6	6
Array Area Efficiency [12]	0.56	0.56	0.56	0.56	0.56	0.56	0.56
Minimum DRAM retention time (ms) [13]	64	64	64	64	64	64	64
DRAM soft error rate (fits) [14]	1000	1000	1000	1000	1000	1000	1000
Vint (support FET voltage) [V] [15]	0.9	0.9	0.9	0.9	0.9	0.7	0.7
Support nMOS EOT [nm] [16]	1.5	1.4	1.4	1.3	1.3	1.3	1.2
Support PMOS Gate Electrode [17]	TiN	TiN	TiN	TiN	TiN	TiN	TiN
Support Gate Oxide [18]	HfSiON	HfSiON	HfSiON	HfSiON	HfSiON	HfSiON	HfSiON
Support min. L_{gate} for NMOS FET, physical [nm] [19]	35	31	28	25	23	21	19
Support $I_{sat\text{-}n}$ [μA/μm] (25C, V_g=V_d=V_{int}) [20]	480	550	550	550	550	550	550
Support min. V_{tn} (25C, $G_{m,max}$, V_d=55mV) [21]	0.31	0.31	0.31	0.31	0.31	0.31	0.31
Support $I_{sat\text{-}p}$ [μA/μm] (25C, V_g=V_d=-V_{int}) [22]	215.00	215.00	215.00	215.00	215.00	215.00	215.00
Support min. V_{tp} (25C, $G_{m,max}$, V_d=55mV) [23]	-0.32	-0.32	-0.32	-0.32	-0.32	-0.32	-0.32

Notes for Table PIDS4a and b

[1] From ORTC (Overall Roadmap Technology Characteristics) Table 1a and b. These DRAM half pitch numbers are the same as those in the 2006 ITRS due to no further speed up in the pace of DRAM half pitch scaling during 2006.

[2] The DRAM cell size is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and chip size numbers are based on the ORTC Tables 1a and 1b. Since the DRAM capacity and chip size numbers are quite aggressive, the cell size must also be scaled aggressively. The difficulty will lie in reducing the value of the cell size factor "a", where "a" equals (cell size /F^2) and F is the DRAM half pitch. The required values of "a" are 6 for 68 nm and beyond.

[3] Storage node cell dielectric EOT is defined as (dielectric physical thickness / [κ/3.9]), where κ is the relative dielectric constant of the storage node cell dielectric and 3.9 is the relative dielectric constant of thermal SiO_2. The value of EOT is driven by the values for DRAM capacity (bits per chip) and chip size, as discussed in more detail in the Front End Process chapter. The capacity and the chip size numbers used by FEP are from the ORTC Tables 1a and 1b. Since the values of DRAM capacity and chip size from FEP are quite aggressive, the EOT must also be scaled very aggressively. Up to 2009, the dielectric material is based on Al_2O_3 or HfO_2, and hence the color is white. Beyond 2009, breakthroughs such as MIM structure with higher κ insulator material of epsilon more than 40 and physical thickness of less than 9nm are needed, so the color is yellow. Finally, for 2012 and beyond, there are no known solutions with demonstrated credibility, and hence the color is red. The actual EOT required for each year also depends on other factors such as cell height and/or 3D structure, film leakage current and contact formation.

[4] The DRAM storage node capacitor voltage must be low enough that the resulting electric field in the dielectric (see Note [5]) is within acceptable limits.

[5] The equivalent electric field in the capacitor dielectric is (DRAM storage node capacitor voltage / DRAM storage node dielectric equivalent oxide thickness, EOT). The equivalent field is the electric field if the dielectric is silicon dioxide; if the dielectric is high-κ, the actual electric field is [equivalent field]/[κ/3.9]. Note the sharp increase in the equivalent field with scaling. The color turns yellow in 2009, when the field is 7.5 MV/cm, and red in 2012, when the field becomes 13.75 MV/cm..

[6] DRAM cell MOSFET structure migrates from RCAT (recessed channel array transistor) to FinFET. RCAT is a technology to improve retention time characteristics by introducing recessed channel structure. FinFET is used to increase the drive current in the limited cell FET area and also to improve retention time characteristics.

[7] DRAM cell FET dielectric EOT is defined as (dielectric physical thickness / [κ/3.9]), where κ is the relative dielectric constant of the DRAM cell FET dielectric and 3.9 is the relative dielectric constant of thermal SiO_2. The EOT values here are large, mainly because of the high word line voltage levels (see Note 8) and the need to keep the electric field in the dielectric within tolerable limits (see Note 9)

[8] Maximum word line level is the (highly boosted) gate voltage for cell FET devices. The high gate voltage is required to get enough device drive current with high threshold voltage due to back gate voltage at the operating condition.

[9] Negative word line is used to suppress sub-threshold leakage current of cell transistor even in the case of lower level of V_t value of cell FET. The low V_t is preferable to get higher drive current of cell FET.

[10] The equivalent electric field in the cell FET device dielectric is (maximum word line level / DRAM cell FET dielectric equivalent oxide thickness, EOT). The equivalent field is the electric field if the dielectric is silicon dioxide; if the dielectric is high-κ, the actual field is [equivalent field]/[κ/3.9].

[11] Cell size factor = a = (DRAM cell size/F^2), where F is the DRAM ½ pitch. The required values of a are 6 for 2007 and beyond. In contrast, the 2005 version of the DRAM table has a = 8 in 2005, 2006 and 2007.

[12] Array area efficiency is the ratio of cell array area to total chip area. Hence, array area efficiency = 1 / (1 + [peripheral circuit area]/NaF^2), where N is the DRAM capacity (number of bits per chip), F is the DRAM ½ pitch, and a is the cell size factor (see Note 9). For a = 8, array area efficiency is estimated to be 0.63, so when a is decreased to 6 from 2007, the array area efficiency of 0.56 is made in conjunction with a = 6, assuming the same relative peripheral circuit area.

[13] Retention time is defined at 85ºC, and is the minimum time during which the data from memory can still be sensed correctly without refreshing a row bit line. The 64 ms specified here is the value needed for PC applications. The retention time depends on the combined interaction of device leakage current, signal strength, and signal sensing circuit sensitivity, and also depends on operational frequency and temperature.

[14] This is a typical FIT rate and depends on cycle time and the quality of cell capacitor and sensing circuits.

[15] V_{int} is the nominal power supply voltage for DRAM support FET in peripheral circuit area. It has been chosen to maintain sufficient voltage over-drive in order to meet the required saturation current drive values while still maintaining reasonable vertical gate dielectric electric field strengths.

[16] DRAM support MOS FET dielectric EOT is defined as (dielectric physical thickness / [κ/3.9]), where κ is the relative dielectric constant of the DRAM cell FET dielectric and 3.9 is the relative dielectric constant of thermal SiO_2.

[17] Support PMOS FET Gate electrode material migrates from P+Poly/W to TiN.

[18] DRAM support MOS FET dielectric material migrates from SiON to HfSiON in order to leakage current to meet.

[19] Physical support min. L_{gate} for NMOS FET is the final, as-etched length of the bottom of the gate electrode.

[20] Support $I_{sat\text{-}n}$ (the saturation drive current for support NMOS FET) is defined as the NMOSFET drain current per micron device width with the gate bias and the drain bias set equal to V_{int} (see Note [15]) and the source and substrate biases set to zero at 25°C, namely $V_g=V_d=V_{int}$).

[21] Support min V_{tn} is the saturation threshold voltage measured at 25 ℃, $G_{m\ max}$,V_d=55mV.

[22] Support Isat-p (the saturation drive current for support PMOS FET) is defined as the PMOSFET drain current per micron device width with the gate bias and the drain bias set equal to -V_{int} (see Note [15]) and the source and substrate biases set to zero at 25°C ,namely, $V_g=V_d=-V_{int}$).

[23] Support min V_{tp} is the saturation threshold voltage measured at 25 ℃, $G_{m\ max}$,V_d=55mV.

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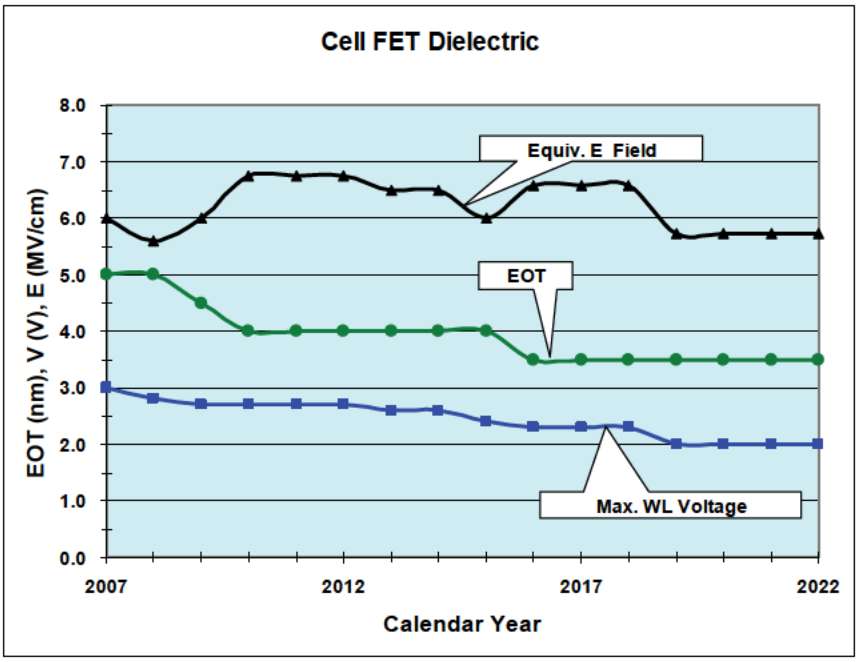


Figure PIDS6 Cell FET Devices

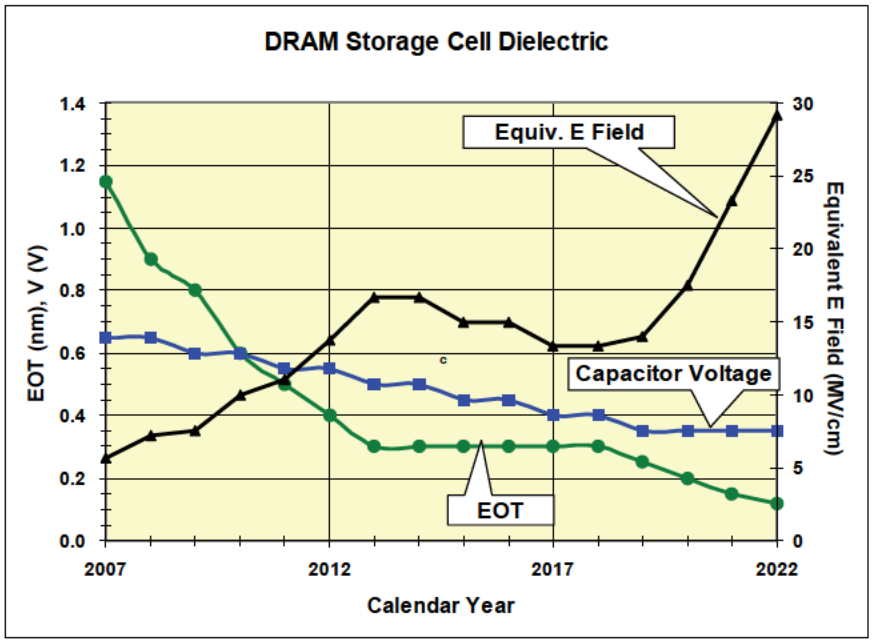


Figure PIDS7 Storage Node Capacitor

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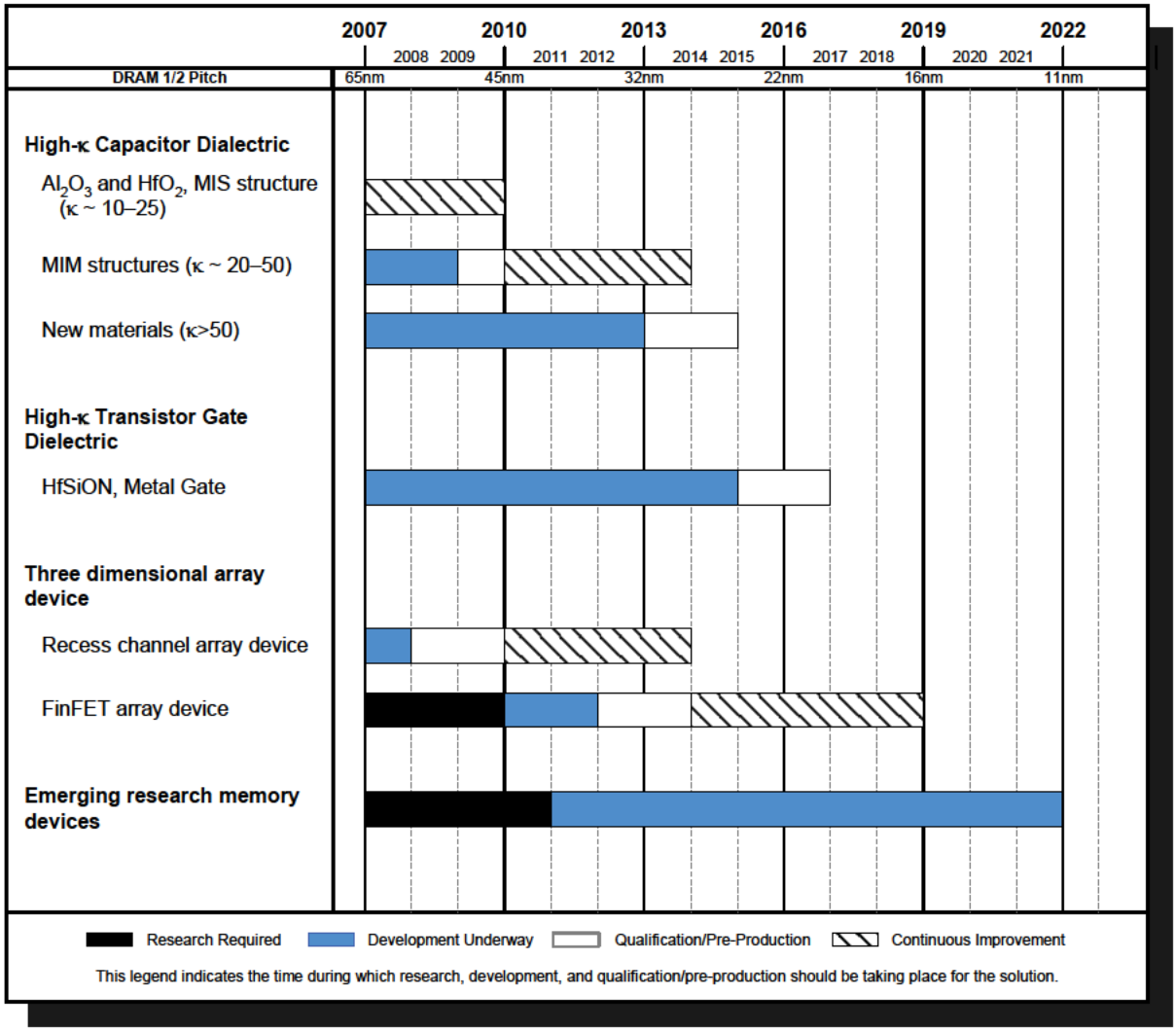


Figure PIDS8 DRAM Potential Solutions

NON-VOLATILE MEMORY

NON-VOLATILE MEMORY TECHNOLOGY REQUIREMENTS

Non-volatile memory consists of several intersecting technologies that share one common trait – non-volatility. The requirements and challenges differ according to the applications, ranging from RFIDs that only require KB of storage to high-density storage of tens of Gb in a chip. The requirements tables are divided into three categories—NAND Flash, NOR Flash, and non-charge-storage memories. Each category may contain more than one approach. For example, NOR Flash memories are fabricated using both floating gate device and nitride charge trapping device, each with their own design rules and scaling trend. Overlapping and/or succession of different technologies for the same application are indicated as appropriate, since as technology evolves best density and performance may be achieved through multiple paths.

Information on each technology is organized into three categories. The requirements tabulation for each technology first treats the issue of density. The applicable feature size "F" is identified and the expected area factor "a" is given (cell size in terms of the number of F^2 units required). Second, the tabulation presents a number of parameters important to each specific technology such as gate lengths, write-erase voltage maxima, key material parameters, etc. These parameters have significance because they are important to the scaling model and/or identify key challenge areas. Third, the endurance (erase-write cycle or read-write cycle) ratings and the retention ratings are presented. Endurance and retention

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are requirements unique to NVM technologies and determine whether the device has adequate utility to be of interest to an end customer.

Table PIDS5a and b show technology requirements for NAND Flash, NOR Flash and non-charge-storage memories for near term years and long term years, respectively. The tables identify both the current CMOS half-pitch and the feature size actually used to form the NVM cells (i.e., the NVM technology "F" in nanometers). Until recently NVM half-pitches have lagged those for DRAM or CMOS logic devices in the same year. Rapid progress in NAND technology has recently reversed this trend, and some design rules are now more aggressively driven by NAND than DRAM. This trend has not spread to other NVM applications yet, however.

Table PIDS5a Non-volatile Memory Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*68*	*58*	*50*	*45*	*40*	*36*	*32*	*30*	*25*
NAND Flash poly ½ Pitch (nm)	*51*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
NAND Flash									
NAND Flash technology – F (nm) [1]	51	45	40	36	32	28	25	22	20
Number of word lines in one NAND string [2]	32	32	64	64	64	64	64	64	64
Cell type (FG, CT, 3D, etc.) [3]	FG	FG	FG	FG/CT	CT	CT	CT-3D	CT-3D	CT-3D
3D NAND number of memory layers	1	1	1	1	1	1	2	2	2
A. Floating Gate NAND Flash									
Cell size – area factor a in multiples of F^2 SLC/MLC [4]	4.0/2.0	4.0/2.0	4.0/1.3	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Tunnel oxide thickness (nm) [5]	6-7	6-7	6-7	6-7	6-7	6-7	6-7	6-7	6-7
Interpoly dielectric material [6]	ONO	ONO	ONO	ONO	ONO	High-κ	High-κ	High-κ	High-κ
Interpoly dielectric thickness (nm)	10-13	10-13	10-13	10-13	10-13	9-10	9-10	9-10	9-10
Gate coupling ratio (GCR) [7]	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
Control gate material [8]	n-Poly	n-Poly	n-Poly	n-Poly	n-Poly	Poly/metal	Poly/metal	Poly/metal	Metal
Highest W/E voltage (V) [9]	17-19	17-19	15-17	15-17	15-17	15-17	15-17	15-17	15-17
Endurance (erase/write cycles) [10]	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05
Nonvolatile data retention (years) [11]	10-20	10-20	10-20	10-20	10-20	10-20	10-20	10-20	10-20
Maximum number of bits per cell (MLC) [12]	2	2	3	4	4	4	4	4	4
B. Charge trapping NAND Flash (MANOS or Barrier Engineering) [13]									
Cell size—area factor a in multiples of F^2 SLC/MLC				4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Tunnel dielectric material [14]				SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO
Tunnel dielectric thickness EOT (nm)				3-4	3-4	3-4	3-4	3-4	3-4
Blocking dielectric material [15]				SiO_2 or Al_2O_3	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3
Blocking dielectric thickness EOT (nm)				6–8	6–8	6–8	6–8	6–8	6–8
Charge trapping layer material [16]				SiN	SiN	SiN	SiN	SiN	SiN
Charge trapping layer thickness (nm) [17]				5–7	5–7	5–7	5–7	5–7	4–6
Gate material [18]				p-Poly/Metal	p-Poly/Metal	p-Poly/Metal	p-Poly/Metal	p-Poly/Metal	Metal
Highest W/E voltage (V)				15-17	15-17	15-17	15-17	15-17	15-17
Endurance (erase/write cycles) [19]				1.E+05	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05
Nonvolatile data retention (years) [20]				10-20	10-20	10-20	10-20	10-20	10-20
Maximum number of bits per cell (MLC)				4	4	4	4	4	4

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Table PIDS5a Non-volatile Memory Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*68*	*58*	*50*	*45*	*40*	*36*	*32*	*30*	*25*
NAND Flash poly ½ Pitch (nm)	*51*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
NOR Flash									
NOR Flash technology – F (nm) [21]	65	57	50	45	40	35	32	28	25
A. Floating gate NOR Flash									
Cell size—area factor a in multiples of F^2 [22], [23], [24], [25]	9-11	9-11	9-11	9-11	9-11	9-11	9-11	9-11	9-11
Gate length L_g, physical (nm) [26]	130	120	100	90	80	70	64	56	50
Tunnel oxide thickness (nm) [27]	8–9	8–9	8–9	8	8	8	8	7 - 8	7 - 8
Interpoly dielectric material [28]	ONO	ONO	ONO	ONO	ONO	ONO	High-κ	High-κ	High-κ
Interpoly dielectric thickness EOT (nm)	13-15	13-15	13-15	13-15	13-15	13-15	8-10	8-10	8-10
Gate coupling ratio [29]	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
Highest W/E voltage (V) [30]	7-9	7-9	7-9	7-9	7-9	7-9	6-8	6-8	6-8
I_{read} (μA) [31]	25-34	23-31	21-27	20-26	19-25	17-22	15-20	14-19	13-18
Endurance (erase/write cycles) [32]	1.00E+05	1.00E+05	1.00E+05	1.00E+06	1.00E+06	1.00E+06	1.00E+06	1.00E+06	1.00E+06
Nonvolatile data retention (years) [33]	10–20	10–20	10–20	10–20	10–20	10–20	20	20	20
Maximum number of bits per cell (MLC) [34]	2	2	2	2	2	2	2	2	2
Array architecture (with cell contact (CC) or virtual ground (VG))[35]	CC	CC	CC	CC	CC	CC	CC/VG	CC/VG	CC/VG
B. Charge trapping NOR Flash (SONOS/NROM) [36]									
SONOS/NROM technology, F (nm)	65	57	50	45	40	35	32	28	25
SONOS/NROM cell size - area factor a in multiples of F^2	6-7	6-7	6-7	6-7	7-8	7-8	7-8	7-8	8-9
Cell size (per bit) – area factor a in multiples of F^2 (SLC/MLC) [37]	3.3/1.6	3.3/1.6	3.3/1.6	3.3/1.6	3.7/1.9	3.7/1.9	3.7/1.9	3.7/1.9	4.3/2.2
Gate length L_g, physical (nm) [38]	140	130	120	110	110	100	100	90	90
Tunnel oxide thickness (nm) [39]	5	5	5	4.5	4.5	4.5	4	4	4
Charge trapping layer thickness (nm) [40]	5-7	5-7	5-7	4-6	4-6	4-6	4-6	4-6	4-5
Blocking (top) dielectric thickness EOT (nm) [41]	7–9	7–9	7–9	6–8	6–8	6–8	6–8	6–8	5–7
Highest W/E voltage (V)	7-9	7-9	7-9	6-8	6-8	6-8	6-8	5–7	5–7
I_{read} (μA) [31]	25-34	23-31	21-27	20-26	19-25	17-22	15-20	14-19	13-18
Endurance (erase/write cycles) [32]	1.00E+05	1.00E+05	1.00E+05	1.00E+06	1.00E+06	1.00E+06	1.00E+06	1.00E+06	1.00E+06
Nonvolatile data retention (years) [33]	10–20	10–20	10–20	10–20	10–20	10–20	10–20	10–20	10–20
Maximum number of bits per cell (physical 2-bit/cell + MLC) [37]	4	4	4	4	4	4	4	4	6
Non-charge-storage NVM									
A. FeRAM (Ferroelectric RAM)									
FeRAM technology – F (nm) [42]	180	180	180	130	130	130	90	90	90
FeRAM cell size – area factor a in multiples of F^2 [43]	22	22	22	20	20	20	16	16	16
FeRAM cell size (μm^2)	0.713	0.713	0.713	0.450	0.450	0.450	0.270	0.270	0.270
FeRAM cell structure [44]	2T2C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C

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Table PIDS5a Non-volatile Memory Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*68*	*58*	*50*	*45*	*40*	*36*	*32*	*30*	*25*
NAND Flash poly ½ Pitch (nm)	*51*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
FeRAM capacitor structure [45]	stack	stack	stack	stack	stack	stack	stack	stack	stack
FeRAM capacitor footprint (μm^2) [46]	0.330	0.330	0.330	0.200	0.200	0.200	0.106	0.106	0.106
FeRAM capacitor active area (μm^2) [47]	0.330	0.330	0.330	0.200	0.200	0.200	0.106	0.106	0.106
FeRAM cap active area/footprint ratio [48]	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Ferro capacitor voltage (V) [49]	1.50	1.50	1.50	1.20	1.20	1.20	1.20	1.20	1.20
FeRAM minimum switching charge density ($\mu C/cm^2$) [50]	13.5	13.5	13.5	20	20	20	34	34	34
FeRAM endurance (read/write cycles) [51]	1.0E+14	1E+14	1E+14	1E+14	1E+14	1E+14	1E+15	1E+15	1E+15
FeRAM nonvolatile data retention (years)	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years
B. MRAM (Magnetic RAM)									
MRAM technology F (nm) [52]	90	65	65	45	45	45	32	32	32
MRAM cell size area factor a in multiples of F^2	20	22	19	20	18	18	19	17	17
MRAM typical cell size (μm^2)	0.16	0.09	0.08	0.041	0.036	0.036	0.019	0.017	0.017
MRAM switching field (Oe) [53]	35	35	35	35	35	35	35	35	35
MRAM write energy (pJ/bit) [54]	70	35	35	25	25	25	20	20	20
MRAM active area per cell (μm^2) [55]	0.05	0.025	0.025	0.013	0.013	0.013	0.009	0.009	0.009
MRAM resistance-area product (KOhm-(μm^2) [56]	2	1.1	1	0.8	0.8	0.8	0.6	0.6	0.6
MRAM magnetoresistance ratio (%) [57]	70	70	70	70	70	70	70	70	70
MRAM nonvolatile data retention (years)	>10	>10	>10	>10	>10	>10	>10	>10	>10
MRAM write endurance (read/write cycles)	>3e16	>3e16	>3e16	>3e16	>3e16	>3e16	>3e16	>3e16	>3e16
MRAM endurance – tunnel junction reliability (years at bias) [58]	>10	>10	>10	>10	>10	>10	>10	>10	>10
C. PCRAM (Phase-Change RAM)									
PCRAM technology F (nm) [58]	72	58	46	40	35	32	28	25	22
PCRAM cell size area factor a in multiples of F^2 (BJT access device) [59]	4.8	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0
PCRAM cell size area factor a in multiples of F^2 (nMOSFET access device) [60]	15.0	14.0	12.0	11.0	10.0	8.9	8.8	8.4	7.4
PCRAM typical cell size (nm^2) (BJT access device) [61]	24883	13456	8464	6400	4900	4096	3136	2500	1936
PCRAM typical cell size (nm^2) (nMOSFET access device) [62]	77760	47096	25392	17600	12250	9114	6899	5250	3582
PCRAM number of bits per cell (MLC) [63]	1	1	2	2	2	4	4	4	4
PCRAM typical cell area per bit size (μm^2) (BJT access device) [64]	24883	13456	4232	3200	2450	1024	784	625	484
PCRAM typical cell area per bit size (μm^2) (nMOSFET access device) [65]	77760	47096	12696	8800	6125	2278	1725	1313	895
PCRAM storage element CD (nm) [66]	45	36	30	25	22	20	18	16	14
PCRAM phase change volume (nm^3) [67]	373,000	195,000	112,000	64,000	43,000	33,000	25,000	18,000	12,000

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Table PIDS5a Non-volatile Memory Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*68*	*58*	*50*	*45*	*40*	*36*	*32*	*30*	*25*
NAND Flash poly ½ Pitch (nm)	*51*	*45*	*40*	*36*	*32*	*28*	*25*	*22*	*20*
PCRAM reset current (μA) [68]	235	170	130	100	80	70	62	52	43
PCRAM set resistance (KOhm) [69]	3.54	4.57	5.68	7.08	8.29	9.21	10.20	11.66	13.56
PCRAM BJT current density (A/cm^2) [70]	1.50E+07	1.50E+07	1.50E+07	1.50E+07	1.50E+07	1.50E+07	1.50E+07	1.60E+07	1.70E+07
PCRAM BJT emitter area (nm^2) [71]	4072	2642	1662	1257	962	804	616	491	380
PCRAM nMOSFET apparent current density for reset (μA/nm) [72]	1.5	1.5	1.8	1.8	1.8	2.1	2.1	2.1	2.4
PCRAM nMOSFET apparent device width (nm) [73]	239	171	108	82	68	51	43	36	26
PCRAM nonvolatile data retention (years) [74]	>10	>10	>10	>10	>10	>10	>10	>10	>10
PCRAM write endurance (read/write cycles) [75]	1.0E+08	1.0E+08	1.0E+10	1.0E+10	1.0E+10	1.0E+12	1.0E+12	1.0E+12	1.0E+15

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



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Table PIDS5b Non-volatile Memory Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*					
NAND Flash poly ½ Pitch (nm)	*19*	*18*	*16*	*14*	*13*	*11*	*10*
NAND Flash							
NAND Flash technology – F (nm) [1]	19	18	16	14	13	11	10
Number of word lines in one NAND string [2]	64	64	64	64	64	64	64
Cell type (FG, CT, 3D, etc.) [3]	CT-3D	CT-3D	CT-3D	CT-3D	CT-3D	CT-3D	CT-3D
3D NAND number of memory layers	2	2	4	4	4	4	4
A. Floating Gate NAND Flash							
Cell size – area factor a in multiples of F^2 SLC/MLC [4]	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Tunnel oxide thickness (nm) [5]	4	4	4	4	4	4	4
Interpoly dielectric material [6]	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ
Interpoly dielectric thickness (nm)	9-10	9-10	9-10	9-10	9-10	9-10	9-10
Gate coupling ratio (GCR) [7]	0.6–0.7	0.6–0.7	0.6–0.7	0.6-0.7	0.6-0.7	0.6-0.7	0.6-0.7
Control gate material [8]	Metal	Metal	Metal	Metal	Metal	Metal	Metal
Highest W/E voltage (V) [9]	15-17	15-17	15-17	15-17	15-17	15-17	15-17
Endurance (erase/write cycles) [10]	1.E+04	1.E+04	1.E+04	1.E+04	1.E+04	1.E+04	1.E+04
Nonvolatile data retention (years) [11]	5-10	5-10	5-10	5-10	5-10	5-10	5-10
Maximum number of bits per cell (MLC) [12]	4	4	4	4	4	4	4
B. Charge trapping NAND Flash (MANOS or Barrier Engineering) [13]							
Cell size – area factor a in multiples of F^2 SLC/MLC	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Tunnel dielectric material [14]	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO	SiO_2 or ONO
Tunnel dielectric thickness EOT (nm)	3-4	3-4	3-4	3-4	3-4	3-4	3-4
Blocking dielectric material [15]	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3	SiO_2 or Al_2O_3
Blocking dielectric thickness EOT (nm)	6–8	6–8	6–8	6–8	6–8	6–8	6–8
Charge trapping layer material [16]	SiN / High-κ	SiN / High-κ	SiN / High-κ	SiN / High-κ	SiN / High-κ	SiN / High-κ	SiN / High-κ
Charge trapping layer thickness (nm) [17]	4–6	4–6	4–6	4–6	4–6	3-4	3-4
Gate material [18]	Metal	Metal	Metal	Metal	Metal	Metal	Metal
Highest W/E voltage (V)	15-17	15-17	15-17	15-17	15-17	15-17	15-17
Endurance (erase/write cycles) [19]	1.E+04	1.E+04	1.E+04	1.E+04	1.E+04	1.E+04	1.E+04
Nonvolatile data retention (years) [20]	5-10	5-10	5-10	5-10	5-10	5-10	5-10
Maximum number of bits per cell (MLC)	4	4	4	4	4	4	4

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Table PIDS5b Non-volatile Memory Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*					
NAND Flash poly ½ Pitch (nm)	*19*	*18*	*16*	*14*	*13*	*11*	*10*
NOR Flash							
NOR Flash technology – F (nm) [21]	22	20	18	16	14	12	10
A. Floating gate NOR Flash							
Cell size – area factor a in multiples of F^2 [22], [23], [24], [25]	10-13	10-13	10-13	10-13	10-13	10-13	10-13
Gate length L_g, physical (nm) [26]	44	40	36	32	28	24	20
Tunnel oxide thickness (nm) [27]	7 - 8	7 - 8	7 - 8	7 - 8	7 - 8	7 - 8	7 - 8
Interpoly dielectric material [28]	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ
Interpoly dielectric thickness EOT (nm)	8-10	8-10	7-9	6-8	6-8	6-8	6-8
Gate coupling ratio [29]	0.6–0.7	0.6–0.7	0.6–0.7	0.6-0.7	0.6-0.7	0.6-0.7	0.6-0.7
Highest W/E voltage (V) [30]	6-8	6-8	6-8	6-8	6-8	6-8	6-8
I_{read} (μA) [31]	12–17	11–16	10–15	9-14	8-13	7-12	6-10
Endurance (erase/write cycles) [32]	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07	1.00E+07
Nonvolatile data retention (years) [33]	20	20	20	20	20	20	20
Maximum number of bits per cell (MLC) [34]	2	2	2	2	2	2	2
Array architecture (with cell contact (CC) or virtual ground (VG))[35]	CC/VG	CC/VG	CC/VG	CC/VG	CC/VG	CC/VG	CC/VG
B. Charge trapping NOR Flash (SONOS/NROM) [36]							
SONOS/NROM technology, F (nm)	22	20	18	16	14	12	10
SONOS/NROM cell size - area factor a in multiples of F^2	8-9	8-9	8-9	9-10	9-10	9-10	9-10
Cell size (per bit) – area factor a in multiples of F^2 (SLC/MLC) [37]	4.3/2.2	4.3/2.2	4.3/2.2	4.8/2.4	4.8/2.4	4.8/2.4	4.8/2.4
Gate length L_g, physical (nm) [38]	80	80	70	70	70	60	60
Tunnel oxide thickness (nm) [39]	4	4	4	3.5	3.5	3.5	3.5
Charge trapping layer thickness (nm) [40]	4-5	4-5	4-5	4	4	4	4
Blocking (top) dielectric thickness EOT (nm) [41]	5–7	5–7	5–7	5–7	5–7	5–7	5–7
Highest W/E voltage (V)	5–7	5–7	5–7	5–7	5–7	4-6	4-6
I_{read} (μA) [31]	12–17	11–16	10–15	9-14	8-13	7-12	6-10
Endurance (erase/write cycles) [32]	1.00E+06	1.00E+06	1.00E+06	1.00E+06	1.00E+06	1.00E+06	1.00E+06
Nonvolatile data retention (years) [33]	10–20	10–20	10–20	10–20	10–20	10–20	10–20
Maximum number of bits per cell (physical 2-bit/cell + MLC) [37]	6	6	6	6	6	6	6

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Table PIDS5b Non-volatile Memory Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*					
NAND Flash poly ½ Pitch (nm)	*19*	*18*	*16*	*14*	*13*	*11*	*10*
Non-charge-storage NVM							
A. FeRAM (Ferroelectric RAM)							
FeRAM technology – F (nm) [42]	90	90	90	65	65	65	65
FeRAM cell size – area factor a in multiples of F^2 [43]	14	14	14	12	12	12	12
FeRAM cell size (μm^2)	0.113	0.113	0.113	0.051	0.051	0.051	0.051
FeRAM cell structure [44]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
FeRAM capacitor structure [45]	3D	3D	3D	3D	3D	3D	3D
FeRAM capacitor footprint (μm^2) [46]	0.041	0.041	0.041	0.016	0.016	0.016	0.016
FeRAM capacitor active area (μm^2) [47]	0.100	0.100	0.100	0.069	0.069	0.069	0.069
FeRAM cap active area/footprint ratio [48]	2.46	2.46	2.46	4.25	4.25	4.25	4.25
Ferro capacitor voltage (V) [49]	1.00	1.00	1.00	0.70	0.70	0.70	0.70
FeRAM minimum switching charge density ($\mu C/cm^2$) [50]	30	30	30	30	30	30	30
FeRAM endurance (read/write cycles) [51]	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16
FeRAM nonvolatile data retention (years)	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years	10 Years
B. MRAM (Magnetic RAM)							
MRAM technology F (nm) [52]	22	22	22	16	16	16	16
MRAM cell size area factor a in multiples of F^2	18	16	16	17	16	17	16
MRAM typical cell size (μm^2)	0.009	0.0077	0.0077	0.0044	0.0041	0.0044	0.0041
MRAM switching field (Oe) [53]	35	35	35	35	35	35	35
MRAM write energy (pJ/bit) [54]	20	20	20	20	20	20	20
MRAM active area per cell (μm^2) [55]	0.007	0.007	0.007	0.005	0.005	0.005	0.005
MRAM resistance-area product (KOhm-(μm^2) [56]	0.6	0.6	0.6	0.6	0.6	0.6	0.6
MRAM magnetoresistance ratio (%) [57]	70	70	70	70	70	70	70
MRAM nonvolatile data retention (years)	>10	>10	>10	>10	>10	>10	>10
MRAM write endurance (read/write cycles)	>3e16	>3e16	>3e16	>3e16	>3e16	>3e16	>3e16
MRAM endurance – tunnel junction reliability (years at bias) [58]	>10	>10	>10	>10	>10	>10	>10

Table PIDS5b Non-volatile Memory Technology Requirements—Long-term Years

Year of Production	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*
DRAM ½ Pitch (nm) (contacted)	*22*	*20*					
NAND Flash poly ½ Pitch (nm)	*19*	*18*	*16*	*14*	*13*	*11*	*10*
C. PCRAM (Phase-Change RAM)							
PCRAM technology F (nm) [58]	20	18	16	14	12	11	9
PCRAM cell size area factor a in multiples of F^2 (BJT access device) [59]	4.0	4.0	4.0	4.0	4.0	4.0	4.0
PCRAM cell size area factor a in multiples of F^2 (nMOSFET access device) [60]	7.3	7.3	6.0	6.0	6.0	5.5	5.5
PCRAM typical cell size (nm^2) (BJT access device) [61]	1600	1296	1024	784	576	480	340
PCRAM typical cell size (nm^2) (nMOSFET access device) [62]	2920	2365	1536	1176	864	650	450
PCRAM number of bits per cell (MLC) [63]	4	4	4	4	4	4	4
PCRAM typical cell area per bit size (μm^2) (BJT access device) [64]	400	324	256	196	144	120	85
PCRAM typical cell area per bit size (μm^2) (nMOSFET access device) [65]	730	591	384	294	216	162	112
PCRAM storage element CD (nm) [66]	13	12	10	9	8	8	7
PCRAM phase change volume (nm^3) [67]	9,000	6,700	4,700	3,200	2,000	1,300	900
PCRAM reset current (μA) [68]	37	32	27	22	18	15	13
PCRAM set resistance (KOhm) [69]	15.17	17.18	19.74	23.11	27.72	31.00	35.00
PCRAM BJT current density (A/cm^2) [70]	1.90E+07	2.00E+07	2.10E+07	2.20E+07	2.40E+07	2.50E+07	2.70E+07
PCRAM BJT emitter area (nm^2) [71]	314	254	201	154	113	91	73
PCRAM nMOSFET apparent current density for reset (μA/nm) [72]	2.4	2.4	2.88	2.88	2.88	2.88	2.88
PCRAM nMOSFET apparent device width (nm) [73]	23	21	16	14	12	10	9
PCRAM nonvolatile data retention (years) [74]	>10	>10	>10	>10	>10	>10	>10
PCRAM write endurance (read/write cycles) [75]	1.0E+15	1.0E+15	1.0E+15	1.0E+15	1.0E+15	1.0E+15	1.0E+15

Notes for Table PIDS5a and b

[1] NAND Flash has surpassed CMOS and DRAM technology since 2005. This entry provides the F value for designs in the indicated time period.

[2] NAND Flash architecture consists of bit line strings of a number of storage devices. Long bit line strings reduce the overhead for bit line transistors and increase the packing density, however, at the expense of higher overall resistance and consequently lower read current. The number of word lines in a bit line string has increased from 16 to 32 nm.

[3] Because of the difficulty in maintaining high gate coupling ratio and preventing cross talk between neighboring cells, NAND technology is forecasted to migrate gradually from floating gate devices (FG) to charge trapping devices (CT). (Ref K. Kim, "Technology for sub 50nm DRAM and NAND Flash manufacturing," in Tech. Digest International Electron Devices Meeting, pp. 539-543, 2005.) The statistical fluctuation limit of storing too few electrons imposes new challenges to data retention (Ref G. Molas, et al., "Impact of few electron phenomena on floating gate memory reliability," Tech. Digest 2004 International Electron Devices Meeting, pp. 877-880, 2004.) and 3D integration of multiple layers of devices may be required to continue the scaling. (Refs S.H. Lee et al., "Three dimensionally stacked NAND Flash memory technology using stacking single crystal Si layers on ILD and TANOS structure for beyond 30nm node," Tech. Digest 2006 International Electron Devices Meeting, pp. 37-40, 2006. E-K. Lai, et al., "A multi-layer stackable thin-film transistor (TFT) NAND-type Flash memory," Tech. Digest 2006 International Electron Devices Meeting, pp. 41-44, 2006.)

[4] The area factor "a" = cell area per bit/F^2, so this entry presents the expected range for Flash cell area in multiples of the implementation technology F^2. It is possible to store more than 1 bit of information in a Flash cell but increasing the logic levels from (1, 0) to (11, 10, 00, 01), etc. by using multi-level cell (MLC). Therefore, the area factor includes both single-level cell (SLC) and multi-level cell (MLC) devices.

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[5] The scaling of tunnel oxide for NAND Flash faces the same challenge as that for NOR Flash. However, the use of error code correction (ECC) in NAND tolerates tunnel oxide defects to a higher level than that for NOR, thus allowing tunnel oxide of 6–7 nm. Currently there are no known solutions to scale tunnel oxide significantly below 6 nm.

[6] ONO has been used as the interpoly dielectric (IPD) up to now and will continue in the near future. However, below 40 nm the spacing between floating gates becomes too narrow to fill effectively with ONO and word line polysilicon, and the loss of sidewall control gate to floating gate coupling will severely degrade the gate coupling ratio (GCR) and the device becomes inoperable. Since it is impossible to create additional space, higher dielectric constant IPD or charge trapping (CT) device must be used. Here the path of migrating to high-κ IPD is shown. It is shown in red color since engineering solutions have not been demonstrated yet.

[7] Gate coupling ratio (GCR) is defined as (control gate to floating gate capacitance)/(total floating gate capacitance). GCR represents the fraction of voltage drop across the tunnel oxide and must be higher than 0.6 for the device to function during write and erase operations. High GCR is normally achieved by wrapping the control gate around the sidewalls of the floating gate. This requires tall floating gate and the cross talk along the bit line direction with neighboring cells is a challenge for MLC operation. At below 40 nm , the spacing between floating gates may become too narrow for the IPD and control gate to wrap around and maintaining sufficiently high GCR is a difficult challenge. Planar device with high-K IPD is a potential solution.

[8] n-type polysilicon (and polycide) gate has been used for the control gate so far and will continue in the near future. The introduction of high-κ IPD, with a lower barrier height to Si, will cause severe gate injection during erase operation and high work function material such as p-type polysilicon or metal gate may have to be adopted.

[9] Low write and erase voltage is desirable but EOT for tunnel oxide and IPD must be decreased to allow lower W/E voltage without compromising W/E speed.

[10] Write and erase cycling endurance reflects the tunnel oxide damage caused by repeated passing of charges under high electric field. Scaling does not worsen the oxide damage, however, larger array strains the ECC capability and the tolerance for defects is thus reduced. High-κ IPD may also trap charge and cause degradation. Current projection is gradually reduced cycling endurance for future technology. Note that this is not suitable for certain applications, e.g., solid-state drive storage that requires high cycling endurance.

[11] Data retention is controlled by both tunnel oxide integrity and statistical distribution of the number of stored electrons. Both thinner tunnel oxide and fewer number of stored electrons in the long term contribute to the shorter retention forecast.

[12] Multi-level cell (MLC) with 4 logic levels (2-bit/cell) is commonly used for NAND Flash today and devices with 8 logic levels (3-bit/cell) and 16 logic levels (4-bit/cell) are being developed. 8-bit/cell MLC device requires 256 logic levels and so far seems beyond reach of current technology, thus no forecast is made for 8-bit/cell MLC even in the long-term years.

[13] MANOS (Metal-Al2O3-Nitride-Oxide-Si) devices use a relatively thin tunnel oxide, a SiN trapping layer for charge storage, Al_2O_3 to increase voltage drop across the tunnel oxide and high work function metal gate to stop gate injection. (Ref C.H. Lee, et al., "A novel SONOS structure of SiO_2/SiN/Al_2O_3 with TaN metal gate for multi-giga bit Flash memories," Tech. Digest 2003 International Electron Devices Meeting, pp. 613-616, 2003.) Barrier engineering uses composite tunneling barriers to allow easy erase operation by substrate hole tunneling, yet prevents low field hole direct tunneling during retention. (Ref H.T. Lue, et al., "BE-SONOS a bandgap engineered SONOS with excellent performance and reliability," Tech. Digest 2005 International Electron Devices Meeting, pp. 555-558, 2005.) Without floating gate GCR and cross talk issues, these two CT approaches promise to help NAND scaling below 30 nm.

[14] Tunnel dielectric for MANOS type device is a relatively thin silicon oxide (3-4nm). Tunnel dielectric for barrier engineered (BE) device may be a composite ONO (e.g., 2 nm/2 nm/2 nm) or other composites such as OAO.

[15] For MANOS device Al_2O_3 is the preferred blocking oxide since it has a high barrier height. Other composite blocking layers such as AN, ANO, or AHO are also potential candidates. For BE device the blocking oxide may be SiO_2, although Al_2O_3 and other composite layers may also be used.

[16] SiN is the most common and best known charge trapping layer with relatively deep electron traps that provide good data retention. Other exotic high-κ material with even deeper traps may be used in the long term years. (Ref A. Chin, et al., "Low voltage high speed SiO2/AlGaN/AlLaO3/TaN memory with good retention," Tech. Digest 2005 International Electron Devices Meeting, pp. 165-168, 2005.) Note that for CT device the charge loss mechanism may be mainly substrate hole tunneling in low field and thus deeper traps do not necessarily improve data retention except for high temperature applications.

[17] Trapping efficiency in SiN seems thickness dependent. (Ref H.T. Lue, et al., Proc. 2007 International Reliability Physics Symposium, 2007). Therefore, thinner SiN or other high-κ trapping layers forecasted for long-term years may suffer from reduced programming efficiency.

[18] High work function metal gate is the best to prevent gate injection. However, p-type polysilicon may become an interim solution because of its easy processing, low cost, and reasonably good performance.

[19] The mechanism for endurance degradation for CT devices is not well understood yet. Unlike floating gate device, CT devices are not sensitive to tunnel oxide damage since the charge is stored in discrete traps and one weak spot does not cause all stored charge to leak out as in floating gate devices. Published endurance data seem to indicate similar endurance as floating gate device.

[20] The mechanism for data retention loss for BE device seems understood. (Ref H.T. Lue, et al., "Reliability model of bandgap engineered SONOS (BE-SONOS)," Tech. Digest 2006 International Electron Devices Meeting, pp. 495-498, 2006.) Data retention mechanism for MANOS device is still not well understood. Published data suggest that data retention is comparable to floating gate devices under certain conditions.

[21] NOR Flash traditionally falls behind CMOS and DRAM but has caught up in recent years and is now on par with DRAM.

[22] High-κ interpoly dielectric is projected at 32 nm and beyond to achieve gate coupling ratio of >0.6 but this offers only limited help to the area factor. (Ref 2005 Symposium on VLSI Technology, 11B-3, E. S. Cho, et al.," Hf-silicate Inter-Poly Dielectric Technology for sub 70 nm Body Tied FinFET Flash Memory," pp. 208-209.)

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[23] Although virtual ground (VG) array may significantly decrease the cell size in the near term years (Ref 2005 Symposium on VLSI Technology, 11B-1, R. Koval, et al. "Flash ETOX Virtual Ground Architecture A Future Scaling Direction," pp. 204-205.), this effect has not been included in the current table because VG is radically different from the conventional array and large development effort is needed to implement it and so far there is no industrial consensus to take up this endeavor.

[24] Although non-planar devices (such as FinFET) are being developed for future Flash scaling, their impact has not been included in the current table. The dilemma of filling ONO and control and floating gates in the narrow gap between adjacent vertical devices has not been completely resolved yet.

[25] Both the cell size and the gate length for NOR Flash have been more aggressively scaled recently with an area factor of approximately 10F2. (Refs 2005 ISSCC, "A 90 nm 512Mb 166 MHz Multilevel Cell Flash Memory with 1.5MBytes/s Programming," pp. 54-55. 2003 Symposium on VLSI Technology, "Highly Manufacturable 90nm NOR Flash Technology with 0.081μm^2 Cell Size," pp. 91-92. 2004 Symposium on VLSI Technology, "A 70nm NOR Flash Technology with 0.049µm2 Cell Size," pp. 238-239.)

[26] NOR Flash uses channel hot electron programming which requires steep junction profile to generate, with the consequence of difficulties in controlling the short channel effect, but yet the NOR architecture is vulnerable to device leakage. Since the tunnel oxide thickness cannot be scaled, controlling the short channel effect imposes a very difficult challenge for scaling. The gate length generally is substantially larger than F in recent years. Despite this difficulty, the area factor has been maintained at 10F2 in recent years (see note 25).

[27] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This difficult trade-off problem hinders scaling. Tunnel oxides less than 7 nm pose fundamental problems for retention reliability.

[28] ONO has been used as the interpoly dielectric up to now and most likely in the near future. However, at 32 nm and beyond high-κ IPD may be necessary to maintain GCR at 0.6 or above. Currently, the GCR is achieved by wrapping the control gate over the sidewalls of the floating gate thus increasing the control gate to floating gate capacitor area. At 32 nm or below, the gap between adjacent gloating gates becomes too narrow for the ONO and control gate to fill in and this semi-vertical structure will cease to function.

[29] The gate coupling ratio (GCR) is the (control gate to floating gate capacitance)/(total floating gate capacitance). GCR must be greater than about 0.6 for proper device operation.

[30] This is the highest voltage relative to ground seen in the cell array, usually supplied by on-chip charge pumping circuits. Low voltage is desired to reduce the charge pumping circuit overhead and simplify processing. The introduction of high-κ IPD will help to reduce the erase voltage.

*[31] In principle the read current decreases with scaling at a rate W/(L*Cox) to prevent voltage overdrive (read disturb). Since access time depends critically on the read current and is an important performance parameter for NOR Flash the read current decreases slower than W/(L*Cox) to maintain performance. This may cause read disturb issues in long term years.*

[32] E/W endurance requirements vary with the specifics of an application, but 1E5 cycles have been accepted as the historical minimum acceptable level for a useful NOR product.

[33] Retention is a defect related parameter rather than an intrinsic device characteristic. Improvement in defect control and accumulation of device history is expected to eventually allow specification of 20 years retention. Also, it should become possible to accept a reduced retention specification as a tradeoff for increased E/W endurance.

[34] Cell read out distinguishes between four levels of charge storage to provide two storage bits (Multilevel cell MLC). Progression to 8 or 16 levels is potentially possible but maintaining reasonable V_t, read speed and array efficiency beyond 2-bit/cell are challenging. Unlike NAND Flash where density is a key competitive advantage, performance and reliability tend to hold higher importance than density for NOR Flash, thus the pressure to higher level MLC is not as strong as for NAND Flash.

[35] Virtual ground array uses junction isolation and buried diffusion for bit line, thus requires no STI isolation or bit line contact in the cell. In principle the area factor for VG array can be as small as $4F^2$, compared to ~ $10F^2$ for an array with cell STI isolation and contact. The scaling of buried diffusion is a difficult challenge and junction isolation produces more leakage paths and complicates the design. Large R&D effort is needed to implement VG array and overcome its shortcomings to take advantage of its smaller cell size.

[36] Charge trapping device for NOR application uses mainly a SONOS structure and thus often is confused with the conventional SONOS device. Conventional SONOS is more suitable for a NAND array. The device is programmed by Fowler-Nordheim tunneling of electrons from the substrate and the charge is stored in the SiN layer of SONOS. Since the electrons are stored in deep SiN traps it is difficult to de-trap by Fowler-Nordheim tunneling. Instead, a very thin (2–3 nm) tunnel oxide is used to allow substrate hole tunneling into the SiN to erase the device. However, such thin tunnel oxide also allows direct tunneling of holes from the substrate even under weak electric field produced by the stored electrons and good data retention is difficult to achieve. NROM is a device proposed to solve the SONOS problem in a NOR array[15]. Using channel hot electron to program the cell, electrons are stored in the SiN layer near the edge of S/D junctions. To erase, band-to-band tunneling generated hot holes are injected into the SiN. A relatively thick (4–5 nm) tunnel oxide is adopted and this solves the data retention issue. NROM also has the advantage of storing two bits of information in one device (source side and drain side) and it applies a reverse read method to distinguish the different states. NROM is built on a virtual ground array architecture and has a relatively small cell size. It is used not only for NOR Flash, but also for some data storage applications even though it is not a NAND structure.

[37] CT NOR SLC Flash stores one bit on the source side and one bit on the drain side, or 2-bit/cell. The MLC Flash stores 2 bits on the source side and two bits on the drain side, thus 4-bit/cell.

[38] Although physically storing two bits in the same device, the gate length scaling is not limited by left-right bit interference. The scaling is limited by the same factors for floating gate device - junction breakdown voltage and short channel effect. 4-bit/cell MLC device window, on the other hand, is affected by left-right bit interference and the L_g scaling for MLC may be more gradual than SLC.

[39] Because electrons are trapped in deep levels in SiN, the tunnel oxide can be scaled more aggressively than for floating gate device.

[40] Reducing the thickness of charge trapping SiN will reduce the EOT but will degrade trapping efficiency.

[41] Interpoly dielectric must be thick enough to assure retention.

[42] This entry is the critical dimension "F" within the FeRAM cell for stand-alone memory devices (not embedded devices).

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[43] This is the area factor "a" = cell size/F^2. FeRAM cell size is presented in terms of F^2 multiples of the FeRAM implementation technology.

[44] FeRAM cell structures have migrated to one transistor, one capacitor (1T1C) formats. (Refs. J.H. Park, et al., "Fully Logic Compatible (1.6V Vcc, 2 Additional FRAM Masks) Highly Reliable Sub 10F2 Embedded FRAM with Advanced Direct Via Technology and Robust 100 nm thick MOCVD PZT Technology", 2004 IEDM, 23.7.1, pp. 591-594. Y. M. Kang et al., "Sub-1.2V Operational, 0.15μm/12F^2 Cell FRAM Technologies for Next Generation SoC Applications", 2005 Symposium on VLSI Technology, 6B-4, pp. 102-103.) Other alternative configurations are under investigation such as Chain-FeRAM. (Refs. H. Kanaya et al., "A 0.602μm^2 Nestled Chain Cell Structure Formed by One Mask Etching Process for 64Mbit FeRAM," 2004 Symposium for VLSI Technology, pp. 150-151. N. Nagel et al., "New Highly Scalable 3 Dimensional Chain FeRAM Cell with Vertical Capacitor," 2004 Symposium on VLSI Technology, pp. 146-147.)

[45] The geometry of the capacitor is a key factor in determining cell size. Stacked planar films are expected to be replaced by more efficient 3D structures.

[46] This is the footprint of the capacitor in micrometers squared. It is this area that constitutes the capacitor area contribution to the cell size. For 2005–2006 ~19F^2, for 2007 - 2009 ~16F^2, and for 2010–2020 ~10F^2 (3D capacitor) are assumed.

[47] This is the actual effective area of the capacitor. It is larger than the footprint for 3D capacitor because of the utilization of area in the third dimension.

[48] This ratio of the effective area to the footprint gives a measure of the impact of utilization of the third dimension.

[49] This is the operating voltage (V_{op}) applied to the capacitor. Low voltage operation is a difficult key design issue. Generally the ferroelectric film thickness needs to be decreased in order to reduce the V_{op}, with great technological challenges. (Ref. D. C. Yoo et al., "Highly Reliable 50nm-thick PZT Capacitor and Low Voltage FRAM Device Using Ir/$SrRuO_3$/MOCVD PZT Capacitor Technology", 2005 Symposium on VLSI Technology, 6B-3, pp. 100-101.)

[50] The minimum switching charge density in $\mu C/cm^2$ is a useful design parameter. It is equal to the cell minimum switching charge divided by the capacitor actual effective area. The capacitor voltage is taken as V_{op}.

[51] FeRAM is a destructive read-out technology, so every read is accompanied by a write to restore the data. Endurance cycles are taken as the sum of all read and all write cycles. For FeRAM to compete with DRAM and SRAM the cycle endurance should be about 1E15. Testing time is a serious concern. Note that operation at 100 MHz for 3 years would accumulate 1E16 cycles.

[52] MRAM devices are expected to lag the CMOS current technology up until 45 nm half pitch in 2010. This entry provides the F value for designs in the indicated time period.

[53] The MRAM switching field is the magnetic intensity H required to change the direction of magnetization of the cell.

*[54] MRAM switching energy per bit is calculated as (write current * power supply voltage * write time). It is preferred to use the median value of switching energy measured on a multi-megabit array. A good estimate of power drain is (switching energy * number of writes per second).*

*[55] MRAM active bit area is the area of the magnetic material stack within the cell. It represents the "A" in the R*A product.*

*[56] MRAM resistance-area product (i.e., the R*A product) is an intrinsic property of the magnetic material stack that provides a convenient basis for comparing cells of different sizes. The R*A product can be computed by measuring the effective low state resistance (R_{low}) of the magnetic tunnel junction and multiply it by the active bit area of the magnetic stack.*

[57] MRAM magnetoresistive ratio is calculated as $100*(R_{high} - R_{low})/R_{low}$. This ratio summarizes the difference between a logic ONE and a logic ZERO, and as such it represents the intrinsic capability of the magnetic stack. The magnetic tunnel junction resistance values are to be measured at low currents.

[58]This is the critical dimension, F.

[59] The area factor "a" = cell area/F^2. This entry is the expected PCRAM cell area in multiples of the implementation technology F^2. PCRAM requires significant reset current to change the phase-change element from crystalline to amorphous. A BJT transistor is capable of providing more current per unit area compared to a MOSFET, thus helps to reduce the cell size. Both BJT and nMOSFET access device cells are represented in this table. PCRAM is capable of MLC multi-bit per cell. This area factor is per cell, not per bit.

[60] The area factor "a" = cell area/F^2. This entry is the expected PCRAM cell area in multiples of the implementation technology F^2. PCRAM requires significant reset current to change the phase-change element from crystalline to amorphous. A BJT transistor is capable of providing more current per unit area compared to a MOSFET, thus helps to reduce the cell size. An nMOSFET transistor has larger cell size in the near term years, but offers simple process and low voltage operation. Both BJT and nMOSFET access device cells are represented in this table. PCRAM is capable of MLC multi-bit per cell. This area factor is per cell, not per bit.

[61] The expected "typical" PCRAM cell size with BJT access device is presented in micrometers squared.

[62] The expected "typical" PCRAM cell size with nMOSFET access device is presented in micrometers squared.

[63] PCRAM is capable of MLC multi-bit/cell operation since the resistance ratio between amorphous and crystalline state is typically 100–1,000. This entry is the expected number of MLC bits per cell.

[64] The expected cell size per MLC bit for the PCRAM with BJT cell. It is the physical cell size divided by the number of MLC bits per cell.

[65] The expected cell size per MLC bit for the PCRAM with nMOSFET cell. It is the physical cell size divided by the number of MLC bits per cell.

[66] PCRAM phase change element must be substantially smaller than the technology F to have efficiency reset operation with reasonable current. This entry is the expected dimension for the phase change element in nanometers.

[67] PCRAM phase change volume is a key factor for device design and peak power requirement. This entry is the expected phase change volume in nanometer cubed.

[68] This entry is the expected reset current for PCRAM in microamperes.

[69] The set resistance is a key design factor for PCRAM read speed.

[70] This entry is the expected current density output from the BJT access device required to reset the PCRAM cell (from crystalline to amorphous state). It is a compromise between larger area BJT (which causes larger cell size) and higher output current (which requires higher operation voltage).

[71] This entry is the expected BJT emitter area that can provide the needed reset current, assuming the BJT current density is met.

[72] This entry is the expected current density output from the nMOSFET access device required to reset the PCRAM cell (from crystalline to amorphous state). It is a compromise between larger width nMOSFET (which causes larger cell size) and higher output current (which requires higher operation voltage or less reliable device).

[73] This entry is the expected nMOSFET gate width that can provide the needed reset current, assuming the MOSFET output current density is met.

[74] This entry is the expected PCRAM data retention that will allow it to be used as a nonvolatile memory. Data retention mechanism for PCRAM is not yet thoroughly studied. Recent published data indicate >10 years of retention at elevated temperatures. (Refs. S. J. Ahn et al., "Highly Manufacturable High Density Phase Change Memory of 64Mb and Beyond," 2004 IEDM, 37.2, pp. 907-910. A. L. Lacaita et al., "Electrothermal and Phase Change Dynamics in Chalcogenide-Based Materials," 2004 IEDM, 37.3, pp. 911-914.)

[75] This entry is the expected PCRAM W/E cycling endurance. Recent published data indicate cycling endurance from 1E+9 to 1E+13. (Refs. S.J. Ahn et al., "Highly Manufacturable High Density Phase Change Memory of 64Mb and Beyond," 2004 IEDM, 37.2, pp. 907-910. S. Lai et al., "Current Status of Phase Change Memory and Its Future," 2003 IEDM, pp. 255-258.)

NON-VOLATILE MEMORY POTENTIAL SOLUTIONS

Nonvolatile memory (NVM) technologies combine CMOS peripheral circuitry with a memory array. The memory array generally requires additional, but CMOS compatible, processes to implement the non-volatility. Non-volatile memories are used in a wide range of applications, some standalone and some embedded, with varying requirements that depend on the application. The memory array architecture and signal sensing method also differ for different applications. The technical challenges are difficult, and in some cases fundamental physics limitations may be reached before the end of the current roadmap. For charge storage devices, the number of electrons in the storage node, whether for single level logic cells (SLC) or multi-level logic cells (MLC), needs to be sufficiently high to maintain stable threshold voltage against statistical fluctuation, and cross talk between neighboring bits must be reduced while the spacing between neighbors decreases. Meanwhile, data retention and cycling endurance requirements must be maintained, and in some cases even increased for new applications. Non-charge-storage devices also may face fundamental limitations when the storage volume becomes small such that random thermal noise starts to interfere with signal.

FLOATING GATE FLASH DEVICES

Floating gate Flash devices achieve non-volatility by storing and sensing the charge on a floating gate. The conventional memory transistor vertical stack consists of a refractory polycide control gate, an interpoly dielectric (IPD) that usually consists of triple oxide-nitride-oxide (ONO) layers, a polysilicon floating gate, a tunnel dielectric, and the silicon substrate. The tunnel dielectric must be thin enough to allow charge transfer to the floating gate at reasonable voltage levels and thick enough to avoid charge loss when in read or off modes. The interpoly dielectric thickness must scale with the tunnel dielectric to maintain adequate coupling of applied erase or write pulses to the tunnel dielectric. The gate coupling ratio (GCR), defined as the capacitance ratio of the control gate to floating gate capacitor to the total floating gate capacitance (control gate to floating gate + floating gate to substrate), is a critical scaling parameter, and must be ≥ 0.6. In most structures, to achieve a GCR ≥ 0.6, the word line (control gate) wraps around the sidewall of the floating gate to provide extra capacitance. Since IPD (ONO) is ≥ 15 nm in thickness, it is difficult to achieve the wrap around structure when the bit line spacing becomes 30 nm or less. Therefore, maintaining the GCR is a major challenge for floating gate Flash device scaling.

The tunnel oxide thickness for the floating gate device poses a great scaling challenge, and there is no currently recognized solution. This inhibits the scaling of gate length for NOR Flash, since leakage from short channel effects introduces severe program disturb. The use of high-κ dielectric in the IPD dielectric (ONO) will be helpful to both reduce the total EOT while maintaining or even increasing the gate coupling ratio. However, planar devices must be used at half-pitch of 30nm or less, and the lost geometrical advantage (wrap around) must be compensated by the higher dielectric constant of high-κ. Therefore, the permittivity must be substantially higher (> 3×) than that of SiO_2.

NOR AND NAND FLOATING GATE FLASH

A NOR Flash cell consists of a single MOS transistor serving both as the cell isolation device and the storage node. The threshold voltage of the transistor is modulated by charges stored in the floating gate and is used as an indication of the storage status. The storage cell may store single level logic (SLC, actually means bi-level logic 1 and 0) or multiple logic levels (MLC, e.g., (11), (10), (00), and (01)). The memory array is an X-Y cross wire structure, thus allowing random access. Programming is by channel hot electron or other variations of hot electron generation, and erasing is by Fowler-Nordheim tunneling of electrons out of the floating gate. The generation of hot electrons requires high lateral electric field under the device and is provided by steep junction profiles. This in turn causes short channel effect and leakage current

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that produces program disturb. Halo implants are used to control device leakage, and this subsequently reduces the junction breakdown voltage and limits the scaling capability. If virtual ground array, which requires no bit line contact within the array, is successfully developed then the NOR Flash cell size can be drastically reduced in the near term years.

A NAND Flash cell also consists of a single MOS transistor, serving mainly as the storage device. The NAND array consists of bit line strings of 32 devices or more with a selection device at each end. This architecture requires no direct bit line contact to the cell, thus allows the smallest cell size. During programming or reading, the unselected cells in the selected bit line string must be turned on and serve as "pass" devices, thus the data stored in each device cannot be accessed randomly conveniently. Both programming and erasing are by Fowler-Nordheim tunneling of electrons into and out of the floating gate. The low Fowler-Nordheim tunneling current allows the simultaneous programming of many bits, thus gives high programming speed. Since devices in the same bit line string serve as pass transistors their leakage current does not affect programming or reading operation, and without the need for hot electrons junctions can be shallow. Thus even with the same tunnel oxide limitation NAND devices are easier to scale than NOR devices. Designed to provide storage and access to large quantities of data but not to instantly execute program codes, NAND Flash generally employs error correction code (ECC) algorithms, and is more fault tolerant than NOR Flash. How to maintain a GCR > 0.6 and to avoid floating gate to floating gate cross talk are two difficult challenges when scaling to 32 nm and below. The timely development of high-κ IPD in a planar device will be a key milestone for continued scaling. Eventually, the few-electron limitation will cause unacceptable retention time distribution, for which there is no currently recognized solution.

CHARGE TRAPPING (CT) DEVICES IN NOR ARCHITECTURE

The threshold voltage of a device may also be affected by charges stored in a charge trapping layer, such as SiN. Charge trapping devices using a SiN as the trapping layer are usually called SONOS, since the device has a SONOS stack—a Si (polycide) gate, a blocking oxide, a nitride storage layer, and a tunnel oxide. The prevailing SONOS device using a relatively thick tunnel oxide in a NOR architecture is commonly known as NROM.[15] NROM uses channel hot electron for programming, and band-to-band tunneling of hot hole for erasing. Since charges injected into the nitride storage layer are well localized near the junctions two bits of information can be stored, one on the source side and one on the drain side, in the same device. The threshold voltage of the device can be read out by shielding the drain side bit with a drain bias and "reverse read" the source side information.

NROM NOR array can be implemented in a virtual ground architecture for which buried diffusion serves as the bit line and the device channel lies along the word line (polycide) direction. This structure requires neither bit line contact nor STI in the cell, thus offering a substantially smaller cell than the conventional NOR array. The cross talk between the two storage nodes in the same device cannot be completely eliminated. This so-called "second bit effect" restricts the threshold voltage window each storage node can carry, and the implementation of MLC in NROM poses a higher level of challenge than for floating gate devices. However, NROM is intrinsically 2-bit/cell and a 4-level MLC implementation results in 4-bit/cell, compared to 16-level MLC required for floating gate device for the same density. The virtual ground array offers a factor of 1.5× to 2× density advantage over conventional NOR architecture using the same design rules, and the single poly process reduces the mask layers.

Charge trapping devices do not have the gate coupling ratio issue floating gate devices face; however, the scaling challenges are otherwise quite similar. The virtual ground array and 2-bit/cell operation are sensitive to device leakage and the use of hot carriers for programming and erasing increases the vulnerability to reliability failures. The scaling limitation is similar to floating gate NOR—leakage from short channel effect and junction breakdown.

CHARGE TRAPPING DEVICES IN NAND ARCHITECTURE

Currently most NAND products are fabricated with floating gate devices. The difficult challenges of maintaining or increasing the GCR and reducing the neighboring cell cross talk may be bypassed by using charge trapping devices. The single gate controls the MOS device channel directly and thus there is no GCR issue, and the cross talk between thin nitride storage layers is insignificant. Nitride trapping devices may be implemented in a number of variations of a basic SONOS type device. SONOS using a simple tunnel oxide, however, is not suitable for NAND application—once electrons are trapped in deep SiN trap levels they are difficult to detrap even under high electric field. In order to erase the device quickly holes in the substrate must be injected into the SiN to neutralize the electron charge. Since the hole barrier for SiO_2 is high (~4.1 eV), hole injection efficiency is poor and sufficient hole current is only achievable by using very thin tunnel oxide (~ 2 nm). Such thin tunnel oxide, however, results in poor data retention because direct hole tunneling from the substrate under the weak retention built-in field cannot be stopped.

Several variations of SONOS have been proposed recently. Tunnel dielectric engineering concepts are used to modify the tunneling barrier properties to create "variable thickness" tunnel dielectric. For example, triple ultra-thin (1–2 nm) layers

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of ONO are introduced to replace the single oxide (BE-SONOS).[16] Under high electric field, the upper two layers of oxide and nitride are offset above the Si valence band, and substrate holes readily tunnel through the bottom thin oxide and inject into the thick SiN trapping layer above. In data storage mode, the weak electric field does not offset the triple layer and both electrons in the SiN and holes in the substrate are blocked by the total thickness of the triple layer. In MANOS (metal-Al_2O_3-nitride-oxide-Si),[17] a high-κ blocking dielectric and metal gate are combined to both prevent gate injection during erase operation, and to boost the electric field at tunnel oxide. A thicker (3–4 nm) tunnel oxide may be used to prevent substrate hole direct tunneling during retention mode.

NON-PLANAR AND MULTI-GATE DEVICES

Non-planar and multi-gate devices such as FinFET and surround-gate devices provide better channel control and allow further scaling of both floating gate and nitride trapping devices. However, the vertical structure also presents new challenges. For example, the space between fins must be sufficiently wide to allow room for tunnel oxide, floating gate and IPD (for floating gate device) and may forbid scaling beyond 30 nm if innovative solutions are not found.

3D STACKING OF MEMORY ARRAYS

When the number of stored electrons reaches statistical limits, even if devices can be further scaled and smaller cells achieved, the threshold voltage distribution of all devices in the memory array will become uncontrollable and logic states unpredictable. The memory density cannot be increased by continued scaling, but may be increased by stacking memory layers vertically. Successful stacking of memory arrays vertically has been demonstrated recently. One approach uses single crystal Si by lateral epitaxial growth.[18] Another uses polycrystalline Si thin-film transistor (TFT) device.[19] The processing temperature and thermal budget must be such that the layers fabricated earlier are not degraded by the additional thermal processes. This imposes a significant challenge to either achieve identical devices in different layers that experience different thermal processes, or design circuits that can handle devices that are slightly different in each layer. Although 3D stacking can help increase the memory density beyond conventional scaling, its effectiveness diminishes after several layers are stacked. The complexity in interconnects increases and the array efficiency decreases with the number of layers. In addition, the complex processing and the large number of masks cumulatively affect the yield. Recently, a "punch and plug" approach is proposed to fabricate the bit line string vertically to simplify the processing steps.[20]

NON-CHARGE-STORAGE NON-VOLATILE MEMORIES

Since the ultimate scaling limitation for charge storage devices is too few electrons, devices that provide memory states without electric charges are promising to scale further. Several non-charge-storage memories have been extensively studied and some commercialized, and each has its own merits and unique challenges. Some of these are uniquely suited for special applications and may follow a scaling path independent of NOR and NAND Flash. Some may eventually replace NOR or NAND in the longer term. Logic states that do not depend on charge storage eventually also run into fundamental physics limits. For example, small storage volume may be vulnerable to random thermal noise, such as the case of superparamagnetism limitation for MRAM.

FeRAM devices achieve non-volatility by switching and sensing the polarization state of a ferroelectric capacitor. To read the memory state the hysteresis loop of the ferroelectric capacitor must be traced and the data must be written back after reading. Because of this "destructive read," it is a challenge to find ferroelectric and electrode materials that provide both adequate change in polarization and the necessary stability over extended operating cycles. The ferroelectric materials are foreign to the normal complement of CMOS fabrication materials, and can be degraded by conventional CMOS processing conditions. Thus the ferroelectric materials, buffer materials, and process conditions are still being refined. So far the most advanced FeRAM[21] is less dense than NOR and NAND Flash using the same design rules, fabricated at least one technology generation behind NOR and NAND Flash, and not capable of MLC. Thus the hope for near term replacement of NOR or NAND Flash has faded. However, FeRAM is fast, low power, and low voltage and thus is suitable for RFID, smart card, ID card, and other embedded applications. In order to achieve density goals with further scaling, the basic geometry of the cell must be modified while maintaining the desired isolation. Recent progress in electrode materials shows promise to thin down the ferroelectric capacitor and extends the viability of 2D stacked capacitor through most of the near term years. Beyond this the need for 3D capacitor still poses steep challenges.

MRAM devices employ a magnetic tunnel junction (MTJ) as the memory element. An MTJ cell consists of two ferromagnetic materials separated by a thin insulating layer that acts as a tunnel barrier. When the magnetic moment of one layer is switched to align with the other layer (or to oppose the direction of the other layer) the effective resistance to current flow through the MTJ changes. The magnitude of the tunneling current can be read to indicate whether a ONE or a ZERO is stored. MRAM probably is the closest to an ideal "universal memory" since it is non-volatile and fast and can be cycled indefinitely, thus may be used as NVM as well as SRAM and DRAM. Control and development of the MTJ

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dimensions and material properties is the major challenge. Also, the tunnel Al_2O_3 layer must endure current stressing at each read/write operation. Management of the material sensitivities to IC processing temperatures and conditions is also an issue. In the long term, the challenge will be the achievement of adequate magnetic intensity H fields to accomplish switching in scaled cells, where electromigration limits the current density that can be used. Recent advances in "spin transfer torque" approach where the spin polarity is transferred from one material directly to another through a "spin current" without resorting to an external magnetic field offer a new potential solution.[22]

PCRAM devices use the resistivity difference between the amorphous and the crystalline states of chalcogenide glass (the most commonly used compound is $Ge_2Sb_2Te_5$, or GST) to store the logic ONE and logic ZERO levels. The device consists of a top electrode, the chalcogenide phase change layer, and a bottom electrode. The leakage path is cut off by an access transistor in series with the phase change element. The phase change write/erase consist of two operations: (1) RESET, for which the chalcogenide glass is momentarily melted by a short electric pulse and then quickly quenched into amorphous solid with high resistivity, and (2) SET, for which a lower amplitude but longer pulse (10ns–100ns) anneals the amorphous phase into low resistance crystalline state. The 1T1R cell is comparable in size to NOR Flash, but the device may be programmed to any final state without erasing the previous state, thus provides substantially faster programming speed. The simple resistor structure and the low voltage operation also make PCRAM attractive for embedded NVM applications. The major challenges for PCRAM are the high current (fraction of mA) required to reset the phase change element, and the relatively long set time. Since the volume of phase change material decreases rapidly with each technology generation, both above issues become easier with scaling. Interaction of phase change material with electrodes may pose long-term reliability issues and limit the cycling endurance and is a major challenge for the maturity of PCRAM.

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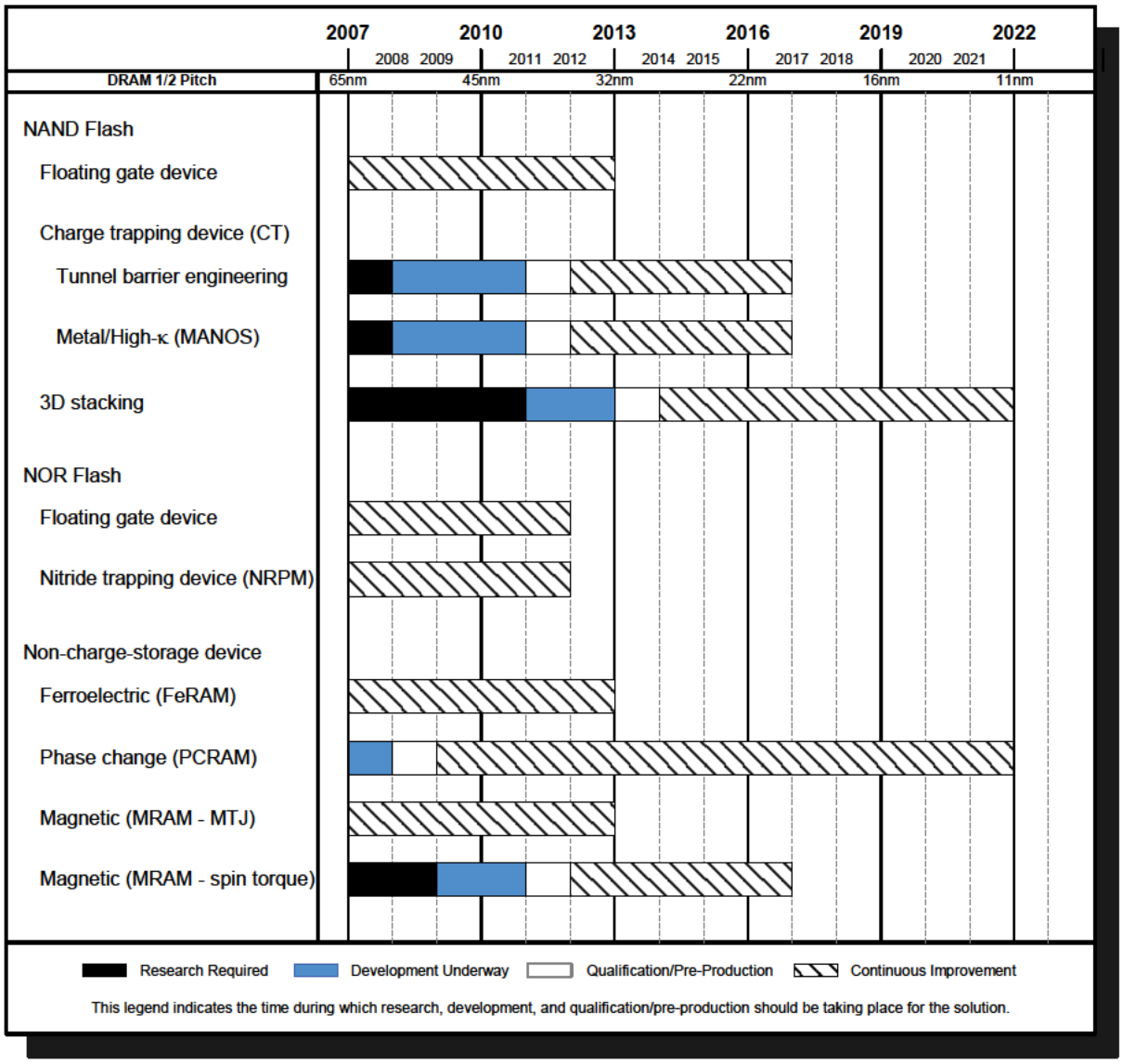


Figure PIDS9 Non-volatile Memory Potential Solutions

RELIABILITY TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

INTRODUCTION

Reliability is an important requirement for almost all users of integrated circuits. The challenge of realizing the required levels of reliability is increasing due to scaling, the introduction of new materials and devices, increasing stresses (fields, current densities, temperatures), and increasing constraints of time and money. Scaling produces ICs with more transistors and more interconnections, both on-chip and in the package. This leads to an increasing number of potential failure sites. Failure mechanisms are impacted by scaling. For example, the time dependent dielectric breakdown (TDDB) of silicon oxy-nitride gate insulators has changed from electric-field-driven to voltage-driven as the insulator thickness has been scaled below 5 nm. In addition, negative bias temperature instability (NBTI) in p-channel devices, which used to be a minor effect when threshold voltages were larger, is now a great concern at the smaller threshold voltages of state-of-the-art devices.

Scaling also leads to increases in the stresses that cause failures. First, the current density is increasing and this increase impacts interconnect reliability. Second, voltages are often scaled down more slowly than dimensions, leading to increased electric fields that impact insulator reliability. Third, scaling has led to increasing power dissipation that results

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in higher temperatures, larger temperature cycles, and increased thermal gradients, all of which impact multiple failure mechanisms. The temperature effects are further aggravated by the reduced thermal conductivity that accompanies the reduction in the dielectric constant of the dielectrics between metal lines.

There are even more profound reliability challenges associated with revolutionary changes associated with new materials and new devices. Recognized failure mechanisms can change. For example, aluminum is stable after being deposited and the preferred path for electromigration is along grain boundaries. In contrast, there is grain boundary growth in copper after electroplating that can lead to stress voiding failures when a single via is connected to a wide metal line. In addition, in copper the preferred electromigration path is along the surface, making copper electromigration and stress voiding much more sensitive to the properties of the intermetal dielectric. This makes the reliability of copper lines much more sensitive to interfaces compared to aluminum. The electromigration in copper will also become worse as the cross section of the copper lines is reduced with scaling. New materials and devices can introduce new failure mechanisms. For example, the poor mechanical and thermal properties of low-κ intermetal dielectrics can lead to mechanical failure mechanisms not seen in silicon dioxide intermetal dielectrics. The impact of an unrecognized failure mechanism that made it into end products would be significant.

These reliability challenges will be exacerbated by the need to introduce multiple major technology changes in a brief period of time. Interactions between changes can increase the difficulty of understanding and controlling failure modes. Furthermore, having to deal simultaneously with several major issues will tax limited reliability resources.

TOP RELIABILITY CHALLENGES

Table PIDS6 indicates the SEMATECH Reliability Council's consensus view of the top five near-term difficult reliability challenges. It expands on the PIDS overall Difficult Challenge 3, "Timely assurance for the reliability of multiple and rapid material, process, and structural changes," described at the beginning of this chapter.

The first near-term reliability challenge concerns failure mechanism associated with the MOS transistor. The time to a first breakdown event is decreasing with scaling. This first event is often a "soft" breakdown. However, depending on the circuit it may take more than one soft breakdown to produce an IC failure. Negative bias temperature instability is a gradual degradation in the properties of p channel transistors. It has grown in importance as threshold voltages have been scaled down and as silicon oxy-nitride has replaced silicon dioxide as the gate insulator. Burn-in may be impacted, as it may accelerate NBTI shifts. High κ will impact insulator failure modes (e.g., breakdown and stability) as well as transistor failure modes such as hot carrier effects and negative bias temperature instability. To put this change into perspective, even after decades of study, there are still issues with silicon dioxide reliability that need to be resolved. The replacement of polysilicon with metal gates also impacts insulator reliability and raises new thermo-mechanical issues. The simultaneous introduction of high κ and metal will make it more difficult to determine reliability than if high κ were first introduced with poly gates.

As mentioned above, the move to copper and low κ has raised issues with electromigration, stress voiding, the poorer mechanical, interface adhesion and thermal conductivity of low-κ dielectrics and the porosity of low-κ dielectrics. The change from Al to Cu has changed electromigration (from grain boundary to surface diffusion) and stress voiding (from thin lines to vias over wide lines). Reliability in the Cu/low-κ system is very sensitive to interface issues. The poorer mechanical properties of low κ also impact wafer probing and packaging. The poorer thermal conductivity of low-κ dielectrics leads to higher on-chip temperatures and higher localized thermal gradients, which impact reliability. The porosity of low-κ dielectrics can trap and transport process chemicals and moisture leading to corrosion and other failure mechanisms

There are additional reliability challenges associated with advanced packaging for higher performance, higher power integrated circuits. Increasing power, increasing pin count, and increasing environmental regulations (e.g., lead-free) all impact package reliability. The interaction between the package and die will increase, especially with the introduction of low-κ intermetal dielectrics. The move to multi-chip packaging and/or heterogeneous integration makes reliability even more challenging. As currents increase and the size of balls/bumps decreases, there is an increased risk of failures due to electromigration.

ICs are used in a variety of different applications. There are some special applications for which reliability is especially challenging. First, there are the applications in which the environment subjects the ICs to stresses much greater than found in typical consumer or office applications. For example, automotive, military, and aerospace applications subject ICs to extremes in temperature and shock. In addition, aviation and space-based applications also have a more severe radiation environment. Second, there are important applications (e.g., implantable electronics, safety systems) for which the consequences of an IC failure are much greater than in mainstream IC applications. In general scaled-down ICs are less "robust" and this makes it harder to meet the reliability requirements of these special applications.

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At the heart of reliability engineering is the fact that there is a distribution of lifetimes for each failure mechanism. With low failure rate requirements we are interested in the early-time edge of the failure time distributions. There has been an increase in process variability with scaling (e.g., distribution of dopant atoms, CMP variations, line-edge roughness). At the same time the size of a critical defect decreases with scaling. These trends will translate into an increasing spread in the time to failure distributions and, thus, a decreasing time to first failure. We need to develop reliability engineering tools (e.g., screens, qualification, Design for Reliability) software that can handle this increase in variability.

The single long-term Reliability Difficult Challenge concerns novel, disruptive changes in devices, structures, materials, and applications. For example, at some point there will be a need to implement non-Copper interconnect (e.g., optical interconnect). For the selected non-Copper solution it is likely that there will be little, if any, reliability knowledge (as least as far as use in ICs is concerned). This will involve a significant effort to discover, model (both a statistical model of lifetime distributions and a physical model of how lifetime depends on stress, geometries, and materials), and apply (new building-in reliability, designing-in reliability, screens, and tests). It also seems likely that there will be less-than-historic amounts of time and money to develop these new reliability capabilities. Disruptive material or devices lead to disruption in reliability capabilities and it will take considerable resources to develop those capabilities.

Table PIDS6 Reliability Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Transistor Reliability	Time dependent dielectric breakdown Negative bias temperature instability Threshold voltage shifts due to traps, carrier injection, program or erase Mobility degradation due to mechanical stress relaxation or interface state density change New or changed failure mechanisms (TDDB, PBTI, NBTI< moisture absorption, etc.) resulting from high κ/metal gate
Interconnect Reliability	Copper electromigration and stress voiding in scaled interconnects (lines and vias) Electrical breakdown of interconnect dielectrics, especially low κ and ultra low κ Moisture absorption/transport due to voids in porous low κ dielectrics Cu (ionic) migration through cracked or thin barrier metals
Packaging Reliability	New failure mechanisms associated with Pb-free solders and new mold compounds Electromigration in package traces, vias, and bumps Impact of multichip modules and stacked dies on failure rate Solder ball electromigration, for example in CSP and flip chip Radioactive contaminants in packaging materials
Reliability in Extreme and/or Critical Applications	Automotive (define mission profile for HOT underhood versus passenger and substantial cycling) Military (rugged versus shock and dust, highly diverse environmental requirements) Space, i.e., radiation hard Aeronautical (singe event effects tolerant and large, fast temperature swings) Medical (corrosive, hermeticity, and safety)
Impact of Variability on Reliability	Statistic variation growing larger and defect size is comparable to feature size: Distribution of dopant atoms; subtle ultra-thin gate oxide defects; line edge roughness and other litho "fidelity" issues; surface scattering How to cope with cost-effective screens and qualifications that capture some "good" units Design for Reliability in face of large percentage process variability How to use yield to drive reliability
Difficult Challenges< 22 nm	*Summary of Issues*
Reliability of novel devices, structures, materials and applications	ITRS proposes many new materials and structures, yet currently very little known about failure mechanisms Need to have reliability characterization in place well in advance of application to develop appropriate reliability requirements and qualification procedures Design for Reliability tools

RELIABILITY REQUIREMENTS

Reliability requirements are highly application dependent. For most customers, current overall chip reliability levels (including packaging reliability) need to be maintained over the next fifteen years in spite of the reliability risk inherent in massive technology changes. However, there are also niche markets that require reliability levels to improve. Applications that require higher reliability levels, harsher environments, and/or longer lifetimes are more difficult than the

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mainstream office and mobile applications. Note that even with constant overall chip reliability levels, there must be continuous improvement in the reliability per transistor and the reliability per meter of interconnect because of scaling. Meeting reliability specifications is a critical customer requirement and failure to meet reliability requirements can be catastrophic.

These customer requirements flow down into requirements for manufacturers that include an in-depth knowledge of the physics of all relevant failure modes and the existence of powerful reliability engineering capabilities for design-for-reliability, building-in-reliability, reliability qualification, and defect screening. There are some significant gaps in these capabilities today. Furthermore, these gaps will become even larger with the introduction of new materials and new device structures. Inadequate reliability tools lead to unnecessary performance penalties and/or unnecessary risks. Finally, as trade-offs between reliability and performance become more difficult, excess reliability margins need to be eliminated.

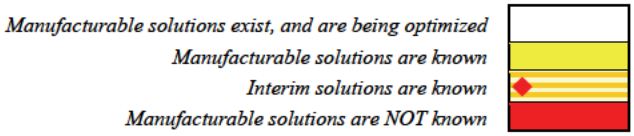
Reliability qualification always involves some risk. There is a risk of qualifying a technology that does not, in fact, meet reliability requirements or a risk of rejecting a technology that does, in fact, meet requirements. At any point in time a qualification can be attempted on a new technology. However, the risk associated with that qualification can be large. The level of risk is directly related to the quality of the reliability physics and reliability engineering knowledge base and capabilities.

The color-coding of the Reliability technology requirements is meant to represent the reliability risk associated with incomplete knowledge and tools for new materials and devices. The progression from white to yellow to striped indicates a growing reliability risk. The requirements first turn to yellow (Manufacturing Solutions are Known) in 2008 indicating a relative smaller risk associated with scaling, increased power. The "wild card" in 2008 will be if manufacturers introduce low κ/metal gate transistor stacks, which will present a considerable reliability risk.

The requirements then turn to striped (Interim Solutions Known) in 2013. This date is approximate. It is meant to represent the point in time where novel devices or materials are introduced (e.g., optical interconnect or a non-CMOS transistor or memory). As mentioned above these changes present a considerable reliability risk and require a considerable lead time to develop the needed capabilities in reliability physics and reliability engineering. Since we do not know exactly what these disruptive technologies will be we have no way, in advance of knowing the reliability risk. When we know the exact technologies proposed we can provide a better assessment of the reliability risk. We choose to use striped as opposed to solid red to reflect that reliability qualification can always be attempted. However, the poorer the quality of our reliability knowledge, the greater the reliability risk.

Table PIDS7a Reliability Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
Early failures (ppm) (First 4000 operating hours) [1]	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
Long term reliability (FITS = failures in 1E9 hours) [2]	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
SRAM Soft error rate (FITs/MBit)	1000-2000	1000-2000	1000-2000	1000-2000	1000-2000	1000-2000	1000-2000	1000-2000	1000-2000
Relative failure rate per transistor (normalized to 2007 value) [3]	1.00	0.83	0.71	0.66	0.57	0.51	0.46	0.40	0.37
Relative failure rate per m of interconnect (normalized to 2007 value) [4]	1.00	0.50	0.50	0.50	0.25	0.25	0.25	0.12	0.12



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Table PIDS7b Reliability Technology Requirements—Long-term Years

Year of Production	2016	2017	2018	2019	2020	2021	2022
DRAM ½ Pitch (nm) (contacted)	22	20	18	16	14	13	11
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	22	20	18	16	14	13	11
MPU Physical Gate Length (nm)	9	8	7	6.3	5.6	5.0	4.5
Early failures (ppm) (First 4000 operating hours) [1]	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
Long term reliability (FITS = failures in 1E9 hours) [2]	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000	50–2000
SRAM Soft error rate (FITs/MBit)	1000-2000	1000-2000	1000-2000	1000-2000	1000-2000	1000-2000	1000-2000
Relative failure rate per transistor (normalized to 2007 value) [3]	0.31	0.29	0.26	0.23	0.20	0.18	0.16
Relative failure rate per m of interconnect (normalized to 2007 value) [4]	0.12	0.06	0.06	0.06	0.03	0.03	0.03

Notes for Table PIDS7a and b

Reliability requirements vary with different applications. For many mainstream customers it will be sufficient to hold current reliability levels steady during this period of rapid technological change. However, other customers would like reliability levels to be improved. Degradation of current reliability levels is not acceptable. Reliability requirements are for the packaged device and include both chip and package related failure modes.

A reliability qualification can always be attempted with available knowledge. The better the knowledge the less risk in the qualification and vice versa. Yellow coloring indicates some risk. Striped indicates a greater risk (due to changed and possible new failure modes). Finally, red indicates an unspecified solution (e.g., what technology will be used for post-Cu) for which the reliability risk cannot be assessed until details about the solution are provided.

[1] Failures during the first 4000 hours of operation (~1 year's use at 50% duty cycle). Early failures are associated with defects.

[2] Long term reliability rate applies for the specified lifetime of the IC.

[3] While the overall IC failure rate does not change with time, as the number of transistors per chip increases [from ORTC], the relative failure rate per transistor must decrease

[4] As the length of interconnect per chip increases [from Interconnect Technology Requirements tables], the failure rate per m of interconnect must decrease. Even more important for reliability is the increase in the number of vias.

RELIABILITY POTENTIAL SOLUTIONS

The most effective way to meet requirements is to have complete built-in-reliability and design-for-reliability solutions available at the start of the development of each new technology generation. This would enable finding the optimum reliability/performance/power choice and would enable designing a manufacturing process that can consistently have high reliability yields. Unfortunately, there are serious gaps in these capabilities today and these gaps are likely to grow even larger in the future. The penalty will be an increasing risk of reliability problems and a reduced ability to push performance, cost and time-to-market.

Meeting requirements requires an in-depth understanding of the physics of each failure mechanism and the development of powerful and practical reliability engineering tools. Historically, it has taken many years (typically a decade) before the start of production for a new technology generation to develop these capabilities (R&D is conducted on characterizing failure modes, deriving validated, predictive models and developing design for reliability and reliability TCAD tools.) The ability to qualify technologies has improved, but there still are significant gaps.

However, there is a limit to how fast reliability capabilities can be developed, especially for major technology discontinuities such as alternate gate insulators or non-traditional devices. An eleventh-hour "sprint" to try and qualify major technology shifts will be highly problematical without an existing and adequate reliability knowledge base.

The Reliability Potential Solutions shown in Figure PIDS10 cover the major technical discontinuities over the lifetime of the Roadmap. (There is a wide variety of changes not listed in this figure that also could impact reliability.) Because these are major discontinuities with serious reliability issues it takes several years to conduct the R&D to identify and model the failure modes (black bars), turn these results into practical reliability engineering capabilities (blue bars), and, finally to perform the qualification of a new technology (white bars). Even when new materials or devices enter production, there still is a need to improve the reliability models and the reliability engineering capabilities continually. Of course, less profound changes can be characterized in much less time. At present, the actual development of these potential solutions lags behind the needed milestones shown in Figure PIDS10.

For reliability capabilities to catch up requires a substantial increase in reliability research-development-application and cleverness in acquiring the needed capabilities in much less than the historic time scales. Work is needed on rapid characterization techniques, validated models, and design tools for each failure mechanism. The impact of new materials

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like Cu, low κ and alternate gate dielectrics needs particular attention. Breakthroughs may be needed to develop design for reliability tools that can provide a high fidelity simulation of a large fraction of an IC in a reasonable time. As mentioned above, increased reliability resources also will be needed to handle the introduction of a large number of major technology changes in a brief period of time.

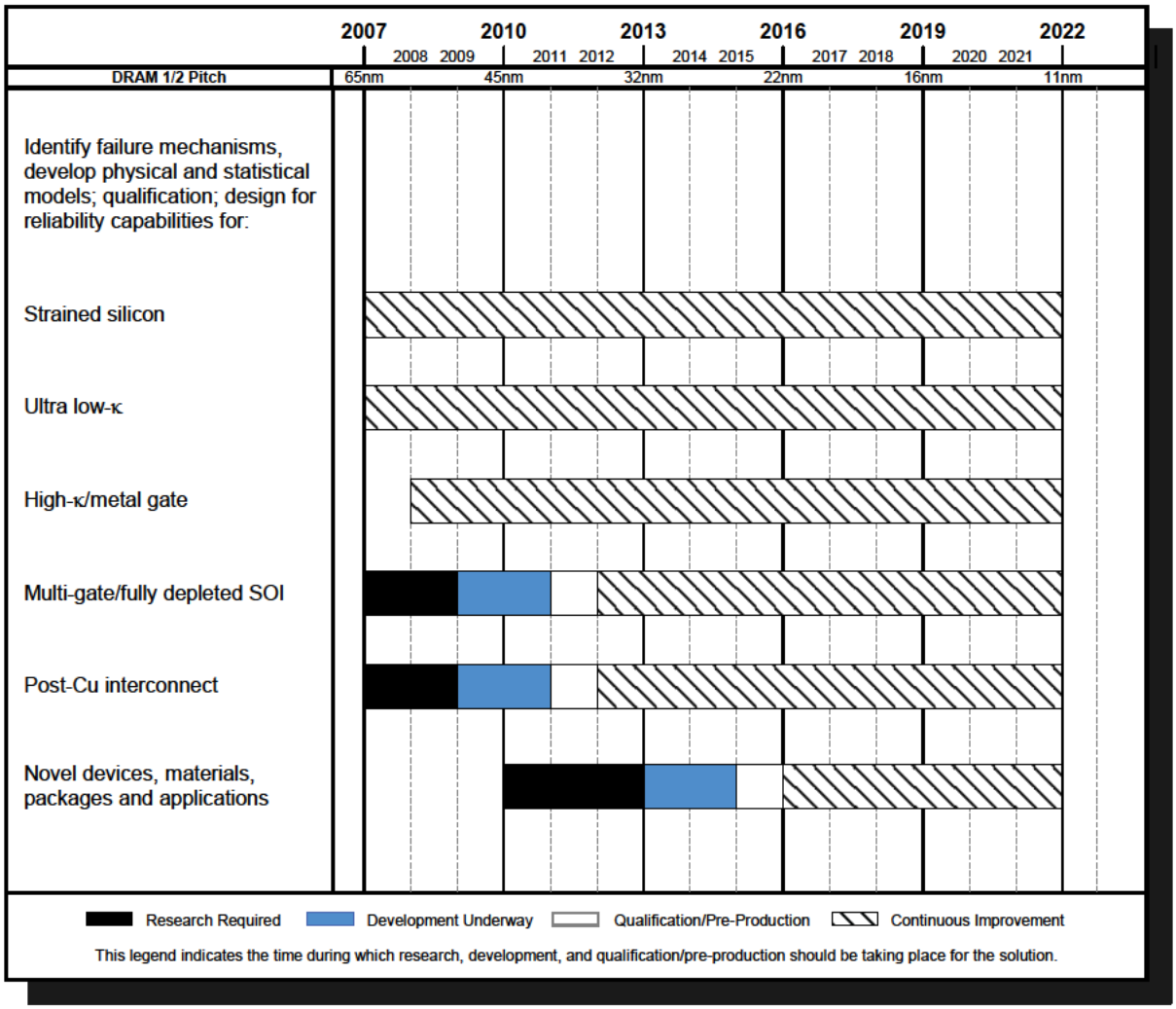


Figure PIDS10 Reliability Potential Solutions

Notes for Figure PIDS10
[1] Strained Silicon has entered volume production. More aggressive use of strained silicon is expected in future technologies. Need to assess its impact on transistor failure mechanisms (e.g., hot carrier and NBTI) continually.
[2] Low-κ interlevel dielectrics have entered production. Successive technology generations will introduce lower and lower κ materials that may modify existing failure mechanisms and could introduce new failure mechanisms.
[3] Driven by PIDS Logic requirement to introduced high-κ gate insulator in 2008.
[4] Driven by PIDS Logic requirement to introduced metal gate(s) in 2008
[5] Driven by PIDS Logic requirement to introduce fully depleted SOI in 2008
[6] Driven by PIDS Logic requirement to introduce double (or triple) gate transistors in 2011.
[7] The timing of the need for a Post-Cu interconnect solution is not clear. We have assumed in this table that it will be introduced in 2013. If it is earlier or later than these boxes will need to be correspondingly shifted. The key message is that we need approximately a 6-year lead time for reliability.
[8] The timing of the need novel, non-CMOS devices is not clear. We have assumed in this table that it will be introduced in 2016. If it is earlier or later, then these boxes will need to be correspondingly shifted. The key message is that we need approximately a 6 year lead time for reliability.

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CROSS TWG ISSUES

MODELING AND SIMULATION

Modeling and simulation needs to be enhanced to deal with the key innovations requested by the *PIDS* section, including enhanced mobility, high-κ gate dielectrics, metal gate electrodes, non-classical CMOS (ultra-thin body fully depleted SOI and multiple-gate MOSFETs), and quasi-ballistic transport leading to enhanced saturation current. These innovations will collectively drive major changes in process, materials, physics, design, etc. Other long-term issues requiring enhanced modeling and simulation include atomic-level fluctuations, statistical process variations, new interconnect schemes, and mixed-signal device technology. With the shrinking of feature sizes, new process steps, architectures and materials reliability issues at the device, interconnect and circuit level will become even more important and will need support from modeling and simulation to achieve the development speed required. Especially for devices that use SOI material, existing models (e.g., for dopant diffusion and activation, carrier transport or for stress) must be extended to cope with interface effects, which become increasingly important compared with bulk properties. These issues are in the *Modeling and Simulation* chapter of this ITRS, especially included in the subchapters on "Front-End Process Modeling," "Device Modeling" and "Interconnects and Integrated Passives Modeling." Finally, non-classical CMOS devices require the development of appropriate compact models to support their introduction.

INTER-FOCUS ITWG DISCUSSION

EMERGING RESEARCH DEVICES

The Emerging Research Devices (ERD) chapter describes and evaluates potential technology, including devices, architectures, and materials, beyond the current standard silicon CMOS technology. As such, it is concerned with the potential successor(s) to the CMOS described in the PIDS chapter. Toward or beyond the end of this Roadmap, when CMOS scaling will likely become ineffective and/or prohibitively costly, some version(s) of ERD technology will presumably be needed if the industry is to continue to enjoy rapid improvements in performance, lower power dissipation and cost per function, and higher functional density. Hence, the PIDS potential solutions tables include ERD solutions late in the Roadmap time period, and refer to the ERD chapter for detail about them.

FRONT END PROCESSES

There is strong linkage between the Front End Processes (FEP) and the PIDS chapters. Key areas of joint concern regarding planar bulk MOSFETs include the replacement of silicon oxy-nitride gate dielectric and polysilicon gate electrodes with high-κ dielectric and metal gate electrodes. Also, the challenge of keeping the parasitic series source/drain resistance within tolerable limits with scaling, and the difficult tradeoffs, including very high channel doping, required to set the threshold voltage and to control short-channel effects (SCEs) as scaling proceeds beyond about 2008. For ultra-thin body fully depleted SOI and multiple-gate MOSFETs, which are expected to be introduced beginning in 2008, some key issues are similar to those for planar bulk, such as high-κ gate dielectric and metal gate electrode and keeping the parasitic resistance within tolerable limits, but channel doping is not an issue, since these devices are essentially undoped. However, there are new issues, such as control of the very thin silicon body required for these devices, and designing and fabricating these devices for optimal operation. For DRAMs, key areas of joint concern include implementation of Metal Insulator Metal (MIM) storage capacitors with high-κ dielectric to scale the equivalent oxide thickness aggressively, as well as keeping the leakage of the access transistor ultra-low as the DRAM is scaled. For non-volatile memory, a key issue of joint concern involves the difficult tradeoffs in scaling the interpoly and the tunneling dielectrics in Flash memory.

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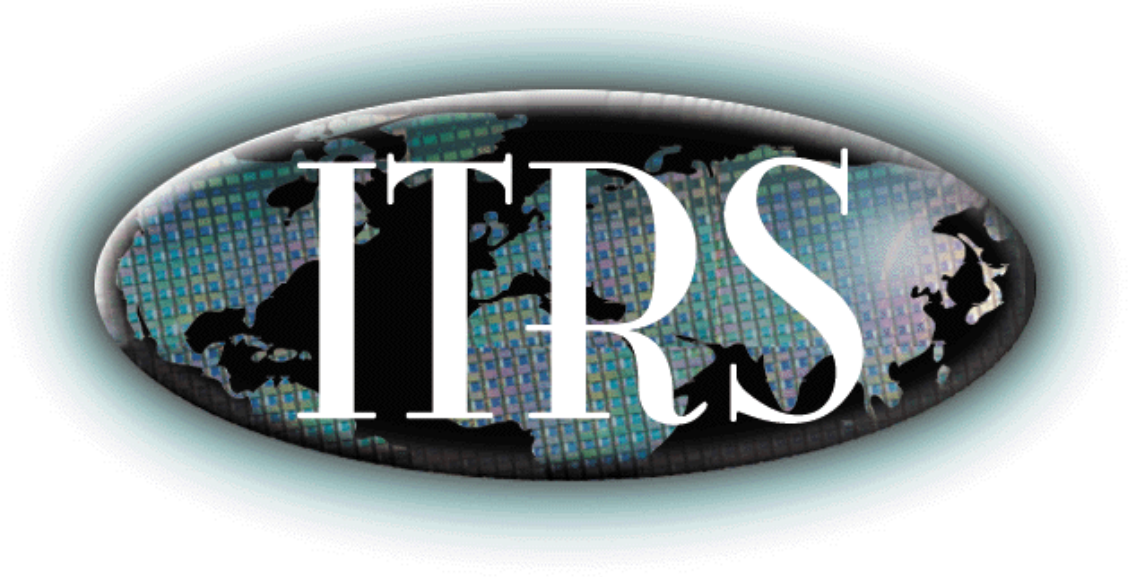
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FOLDER 14



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2009 Friends of the Roadmap















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INTRODUCTION

OVERVIEW

For more than four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles roughly every 24 months). The most significant trend is the decreasing cost-per-function, which has led to significant improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor throughput**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last three and a half decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for Semiconductors (NTRS), which had 1992, 1994, and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of the Roadmap and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999. Since then, the ITRS has been updated in even-numbered years and fully revised in odd-numbered years. The overall objective of the ITRS is to present industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, universities, governments, and other research providers or funders. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that most need research breakthroughs.

The ITRS is a dynamic process, evident by the evolution of the ITRS documents. The ITRS reflects the semiconductor industry migration from geometrical scaling to equivalent scaling. Geometrical scaling [such as Moore's Law] has guided targets for the previous 35 years, and will continue in many aspects of chip manufacture. Equivalent scaling targets, such as improving performance through innovative design, software solutions, and innovative processing, will increasingly guide the semiconductor industry in this and the subsequent decade. Since 2001 the ITRS has responded by introducing new chapters on System Drivers (2001), Emerging Research Devices and Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (2005), and most recently in 2007, Emerging Research Materials, to better reflect this evolution of the semiconductor industry.

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of electronics would further reduce the cost per function (historically, ~25–29%% per year) and promote market growth for integrated circuits (historically averaging ~17% per year, but maturing to slower growth in more recent history). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?"

It is forecasted that by the end of the next decade it will be necessary to augment the capabilities of the CMOS process by introducing multiple new devices that will hopefully realize some properties beyond the ones of CMOS devices. However, it is believed that most likely these new devices will not have all the properties of CMOS devices and therefore

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it is anticipated that heterogeneous integration either at the chip level or at the package level will integrate these new capabilities around a CMOS core.

The participation and continued consensus of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. ensures that the 2009 ITRS remains the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The complete 2009 ITRS and past editions of the ITRS are available for viewing and printing as electronic documents at the Internet web site *http://www.itrs.net*.

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

Overall coordination of the ITRS process is the responsibility of the International Roadmap Committee (IRC), which has two-to-four members from each sponsoring region (Europe, Japan, Korea, Taiwan, and the U.S.A.). The principal IRC functions include the following:

- Providing guidance/coordination for the International Technology Working Groups (ITWGs)
- Hosting the ITRS Workshops
- Editing the ITRS

The International Technology Working Groups write the corresponding technology-area chapters of the ITRS. The ITWGs are of two types: *Focus* ITWGs and *Crosscut* ITWGs. The Focus ITWGs correspond to typical sub-activities that sequentially span the Design/Process/Test/Package product flow for integrated circuits. The Crosscut ITWGs represent important supporting activities that tend to individually overlap with the "product flow" at multiple critical points.

For the 2009 ITRS, the Focus ITWGs are the following:

- System Drivers
- Design
- Test and Test Equipment
- Process Integration, Devices, and Structures
- RF and Analog / Mixed-signal Technologies for Wireless Communications
- Emerging Research Devices
- Front End Processes
- Lithography
- Interconnect
- Factory Integration
- Assembly and Packaging

Crosscut ITWGs are the following:

- Emerging Research Materials
- Environment, Safety, and Health
- Yield Enhancement
- Metrology
- Modeling and Simulation

The ITWGs are composed of experts from industry (chip-makers as well as their equipment and materials suppliers), government research organizations, and universities. The demographics per ITWG reflect the affiliations that populate the technology domains. For example, with a longer-term focus area such as Emerging Research Devices, the percentage of research participants is higher than suppliers. In the process technologies of Front End Processes, Lithography, and Interconnect, the percentages of suppliers reflect the equipment/materials suppliers' participation as much higher due to the near-term requirements that must be addressed.

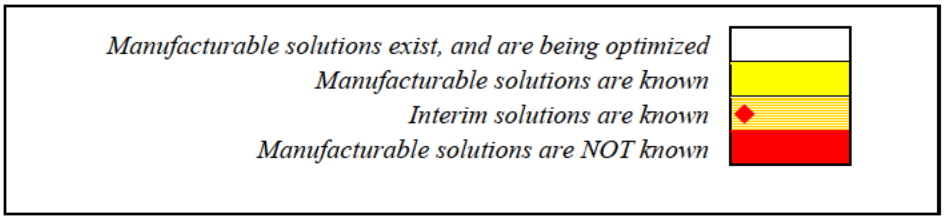
For the 2009 edition, three ITRS meetings were held worldwide as follows: Brussels, Belgium (sponsored by the ESIA and hosted by NXP Semiconductors); San Francisco, U.S.A., sponsored by the SIA, organized by SEMATECH and co-hosted with SEMI/North America; and Hsinchu, Taiwan (sponsored and co-hosted by TSIA and TSMC). These meetings provided the main forums for face-to-face discussions among the members of each ITWG and coordination among the different ITWGs. In addition, the ITRS teams hold public ITRS conferences bi-annually to present the latest Roadmap information and to solicit feedback from the semiconductor industry at-large.

The ITRS is released annually, with updates and corrections to data tables each even-numbered year (such as 2000, 2002, 2004, 2006, 2008) while complete editions are released each odd-numbered year (2001, 2003, 2005, 2007, 2009). This ITRS process thus ensures continual assessment of the semiconductor industry's near and long-term needs. It also allows the teams to correlate in a timely fashion the ITRS projections to most recent research and development breakthroughs that may provide solutions to those needs.

ROADMAP CONTENT

The ITRS assesses the principal technology needs to guide the shared research, showing the "targets" that need to be met. These targets are as much as possible quantified and expressed in tables, showing the evolution of key parameters over time. Accompanying text explains and clarifies the numbers contained in the tables where appropriate.

The ITRS further distinguishes between different maturity and confidence levels, represented by colors in the tables, for these targets:



The first situation, "Manufacturable solutions exist, and are being optimized," indicates that the target is achievable with the currently available technology and tools, at production-worthy cost and performance. The yellow color is used when additional development is needed to achieve that target. However, the solution is already identified and experts are confident that it will demonstrate the required capabilities in time for production start. The situation "Interim Solutions are Known" means that limitations of available solutions will not delay the start of production, but work-arounds will be initially employed in these cases. Subsequent improvement is expected to close any gaps for production performance in areas such as process control, yield, and productivity. The fourth and last situation is highlighted as "red" on the Roadmap technology requirements tables and has been referred to as the "Red Brick Wall" since the beginning of ITRS. (The "red" is officially on the Roadmap to clearly warn where progress might end if tangible breakthroughs are not achieved in the future.) Numbers in the red regime, therefore, are only meant as warnings and should not be interpreted as "targets" on the Roadmap. For some Roadmap readers, the "red" designation may not have adequately served its *sole* purpose of highlighting significant and exciting challenges. There can be a tendency to view *any* number in the Roadmap as "on the road to sure implementation" regardless of its color. To do so would be a serious mistake.

"Red" indicates where there are no "known manufacturable solutions" (of reasonable confidence) to continued scaling in some aspect of the semiconductor technology. An analysis of "red" usage might classify the "red" parameters into two categories:

1. where the consensus is that the particular value will ultimately be achieved (perhaps late), but for which the industry doesn't have much confidence in any currently proposed solution(s), or
2. where the consensus is that the value will never be achieved (for example, some "work-around" will render it irrelevant or progress will indeed end)

To achieve the red parameters of the first category, breakthroughs in research are needed. It is hoped that such breakthroughs would result in the "red" turning to "yellow" (manufacturable solutions are known) and, ultimately "white" (manufacturable solutions are known and are being optimized) in future editions of ITRS.

As indicated in the overview, the Roadmap has been put together in the spirit of defining what technical capabilities the industry needs to develop in order to stay on Moore's Law and the other trends, and when. So the ITRS is not so much a forecasting exercise as a way to indicate where research should focus to continue Moore's law. In that initial "challenge"

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spirit, the Overall Roadmap Technology Characteristics (ORTC) team updates key high-level technology needs, which establish some common reference points to maintain consistency among the chapters. The high-level targets expressed in the ORTC tables are based in part on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies.

Over the years, however, the Roadmap has sometimes been seen as a self-fulfilling prophecy. To a certain extent this is also a valid view, as companies have benchmarked each other against the Roadmap, and it proved very effective in providing thrust for research. So it is not unreasonable to use the Roadmap targets, when manufacturing solutions or acceptable workarounds are known, as guidelines to forecasting exercises.

What these targets should never be used for, however, is as basis for legal claims in commercial disputes or other circumstances. In particular, the participation in the ITRS road-mapping process does not imply in any way a commitment by any of the participating companies to comply with the Roadmap targets. We recall that the ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual product or equipment.

TECHNOLOGY CHARACTERISTICS

As mentioned above, a central part of the IRC guidance and coordination is provided through the initial creation (as well as continued updating) of a set of Overall Roadmap Technology Characteristics tables. Each ITWG chapter contains several principal tables. They are individual ITWGs' technology requirements tables patterned after the ORTC tables. For the 2007 ITRS, the ORTC and technology requirements tables are fully annualized and in both the "Near-term Years" (2009, 2010… through 2016) and "Long-term Years" (2017, 2018 … through 2024) This format is illustrated in Table B, which contains a few key rows from lithography-related Table ORTC1, including the Flash product uncontacted polysilicon half-pitch technology trend line item as the most aggressive technology target. In the previous 2005 Roadmap editions, the DRAM stagger-contacted M1 half pitch line item was used as a standard header for all the ITRS ITWG tables; however, beginning with the 2007 edition, the IRC has requested that only the year of first production be required as a standard header. At the discretion of the ITWGs, other product technology trend driver line items may be selected from Table ORTC1 for use in their ITWG tables as overall headers indicating key drivers for their tables.

Table B ITRS Table Structure—Key Lithography-related Characteristics by Product

Near-term Years

YEAR OF PRODUCTION	2009	2010	2011	2012	2013	2014	2015	2016
Flash Uncontacted Poly Si ½ Pitch (nm)	38	32	28	25	23	20	18	15.9
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	52	45	40	36	32	28	25	22.5
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	54	45	38	32	27	24	21	18.9
MPU Printed Gate Length (nm)	47	41	35	31	28	25	22	19.8
MPU Physical Gate Length (nm)	29	27	24	22	20	18	17	15.3

Long-term Years

YEAR OF PRODUCTION	2017	2018	2019	2020	2021	2022	2023	2024
Flash Uncontacted Poly Si ½ Pitch (nm)	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
DRAM stagger-contacted Metal 1 (M1) ½ Pitch (nm)	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
MPU/ASIC stagger-contacted Metal 1 (M1) ½ Pitch (nm)	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5
MPU Printed Gate Length (nm)	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9
MPU Physical Gate Length (nm)	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4

The ORTC and technology requirements tables are intended to indicate current best estimates of introduction timing for specific technology requirements. Please refer to the Glossary for detailed definitions for Year of Introduction and Year of Production.

TECHNOLOGY PACING

In previous editions of the ITRS, the term "technology node" (or "hpXX node") was used in an attempt to provide a single, simple indicator of overall industry progress in integrated circuit (IC) feature scaling. It was specifically defined as the smallest half-pitch of contacted metal lines on any product. Historically, DRAM has been the product which, at a given time, exhibited the tightest contacted metal pitch and, thus, it "set the pace" for the ITRS technology nodes.

However, we are now in an era in which there are multiple significant drivers of scaling and believe that it would be misleading to continue with a single highlighted driver, including DRAM

For example, along with half-pitch advancements, design factors have also rapidly advanced in Flash memory cell design, enabling additional acceleration of functional density. Flash technology has also advanced the application of electrical doubling of density of bits, enabling increased functional density independent of lithography half-pitch drivers. A second example is given by the MPU/ASIC products, for which the speed performance driver continues to be the gate-length isolated feature size, which requires the use of leading-edge lithography and also additional etch technology to create the final physical dimension.

Significant confusion relative to the historical ITRS node definition continues to be an issue in many press releases and other documents that have referred to "node acceleration" based on other, frequently undefined, criteria. Of course, we now expect different IC parameters to scale at different rates, and it is certainly legitimate to recognize that many of these have product-specific implications. In the 2009 ITRS, we will continue the practice of eliminating references to the term "technology node." As mentioned above, the IRC has recommended that the only standard header will be year of first production, and DRAM M1 half-pitch is just one among several historical indicators of IC scaling. With this latest change to standard ITRS table format policy, it is hoped that the ITRS will not contribute to industry confusion related to the concept of "technology node." Of course, "node" terminology will continue to be used by others. Hopefully, they will define their usage within the context of the application to the technology of a specific product.

For reference on the 2005 ITRS common definition of M1 half-pitch for all products, as well as the definition of polysilicon half-pitch for FLASH memory, see Figure 1.

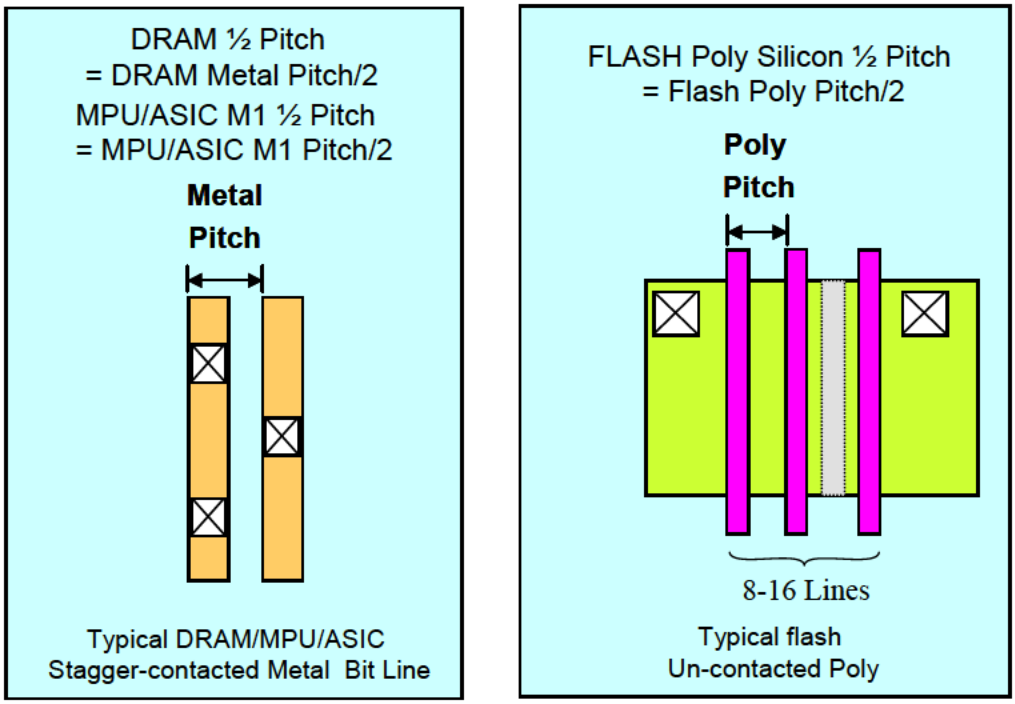


Figure 1 2009 Definition of Pitches

MEANING OF ITRS TIME OF INTRODUCTION

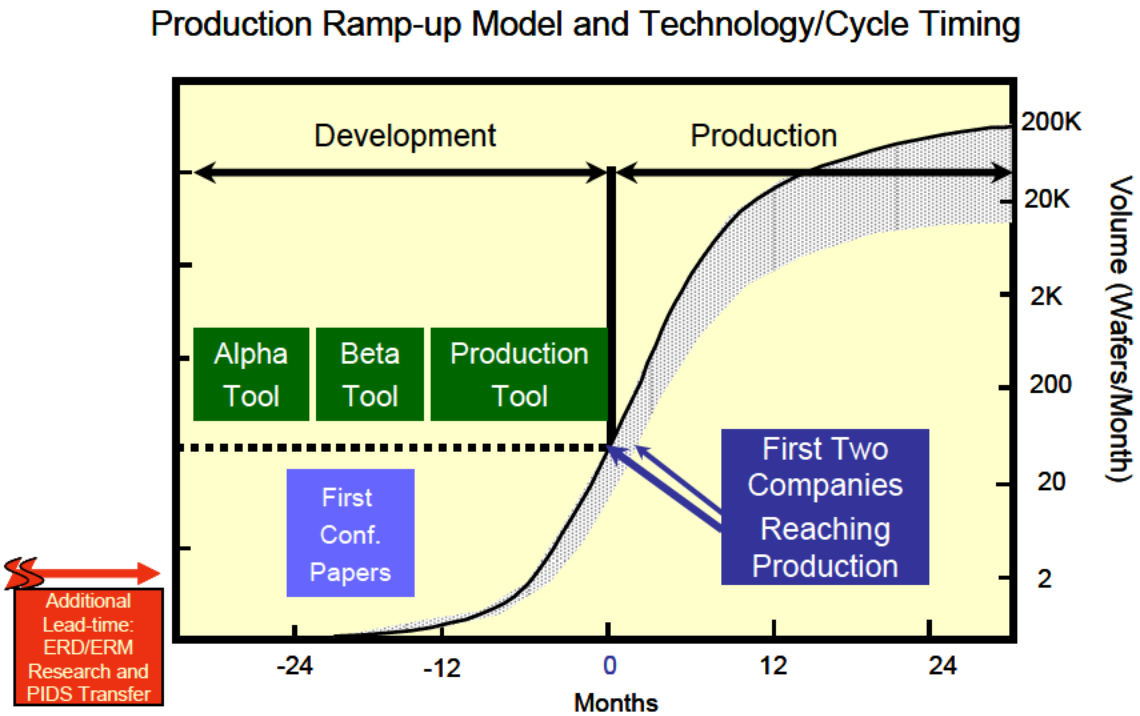
The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "Time of Introduction" in the ITRS is the "Year of Production," which is defined in Figure 2a.

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Figure 2a has been revised from previous roadmaps and no longer includes reference to volume parts per month, due to the variability of different product die sizes for first production targets. Therefore, only the typical industry high volume ramp scale is retained in the 2009 roadmap.

In addition, a graphical note was added at the request of the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) TWGs to highlight that it is necessary to consider the very-wide-time-range required to capture early research activities that may result in Potential Solutions items for the ITWG Grand Challenges. It has become increasingly important to communicate a broad horizon encompassing both the period preceding the first manufacturing alpha tools and materials and also the period that extends to the classic ITRS 15-year horizon and even beyond. The preceding horizon is required to capture the period of the very first technical conference paper proposals until the start of development activities; at which point typically a transfer from ERD/ERM to PIDS/FEP ITWGs occurs.

For more explicit clarification, see Figure 2b, in which an example is shown for a new gate structure potential solution targeted for 2019 production. In this example, the first research papers appear in 2007, and the Potential Solution technology would be planned for transfer to PIDS during the 2011 ITRS roadmap work, when more detailed line item characteristics would be defined.



(also see Figure 2b below for ERD/ERM Research and PIDS Transfer timing; and also Figure 2c for Typical Wafer Generation Pilot and Production "Ramp Curves"

Figure 2a A Typical Technology Production "Ramp" Curve (within an established wafer generation)

The "Production" time in the ITRS refers to the time when the first company brings a technology to production and a second company follows, typically within three months; however sometimes there is a longer time for the second company to get into production. Production means the completion of both process and product qualification. The product qualification means the approval by customers to ship products, which may take one to twelve months to complete after product qualification samples are received by the customer. Preceding the production, process qualifications and tool development need to be completed. Production tools are developed typically 12 to 24 months prior to production. This means that alpha and succeeding beta tools are developed preceding the production tool.

Also note that the Production "time zero (0)" in Figures 2a and 2b can be viewed as the time of the beginning of the ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (WSPM) capacity or more, the time to ramp from 20 WSPM to full capacity can take nine to twelve months. As an example, this time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month [for the example of a chip size

at 140 mm^2 (430 gross die per 300 mm wafer × 20K WSPM × 70% total yield from wafer starts to finished product = 6M units/month)].

In addition, note that the ITRS ramp timing in this example is in reference to the ramp of a technology cycle within a given wafer generation. Now that the industry is approaching the time for a new 450 mm wafer generation transition, additional scrutiny has been given to the historical ramp rate for a technology cycle that has been ramped in two wafer generations of the first leading companies at the same time (see the discussion and the new 2009 ITRS Figure 5 in the 450 mm section). It is during that transition of a technology cycle coexisting within two wafer generations that the economic productivity gain modeling is also examined.

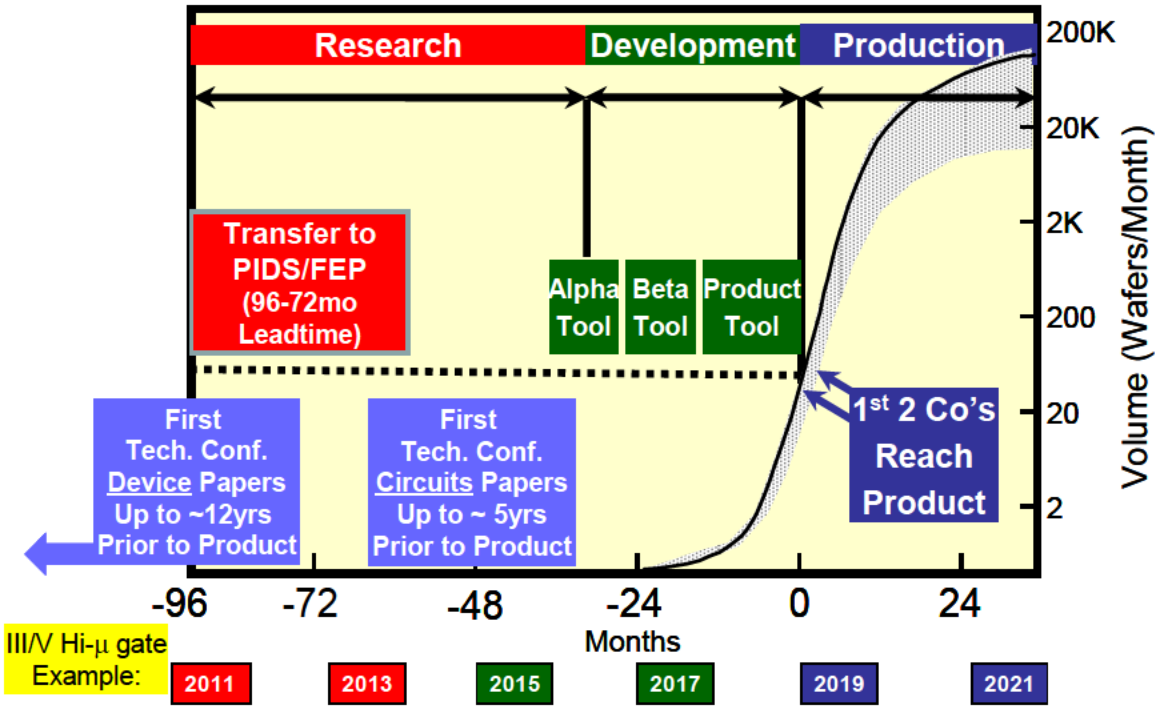


Figure 2b A Typical Technology Production "Ramp" Curve for ERD/ERM Research and PIDS Transfer timing (including an example for III/V Hi-Mobility Gate Technology Timing Scenario)

2009 SICAS Industry Manufacturing Technology Capacity Update

It is noted that the ITRS, by its definition, focuses on forecasting the earliest introduction of the leading-edge semiconductor manufacturing technologies, which support the production of selective leading-edge driver product markets, such as DRAM, Flash, MPU, and high-performance ASICs. It is, however, true that many companies, for a variety of reasons, may choose to introduce a leading-edge technology later than the earliest introduction of the leading-edge technology; hence, there is a wide variation of the technologies in actual production status from leading edge to trailing edge.

Furthermore, it has been observed that some companies consciously choose to utilize aggressively leading-edge technologies only for a subset of their product portfolio; because it is not economically attractive to do so for all products. Individual Companies decide to go slower or even stick to trailing technologies with specific products because further shrinking might not even make sense anymore. Therefore there appears to be a broader split of technologies in use which is becoming even broader.

Figure 3 [updated with 2Q09 SICAS data] shows, in horizontal bar graph format (each bar width is proportional to silicon processing capacity), the actual, annual worldwide wafer production technology capacity distributions over different process feature sizes. The distributions of the overall industry technology capacity segments are tracked by feature-size splits, which are quite widespread.

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The ITRS technology cycle, as measured by DRAM metal 1 (M1) half-pitch, is shown as yellow marks (for the historical actual timing), as reported by the industry surveys conducted by ITRS TWGs. The surveys conducted in 2003, 2005, and 2007 have indicated that first production of the leading-edge DRAM M1 half-pitch has been on a two-year cycle (for 0.71× reduction per technology cycle), from 250 nm in 1998 through 90 nm in 2004. However, the most recent survey update is indicating that the DRAM historical trend is tracking closer to the ITRS MPU trend. This was investigated further in 2007 and 2008, and reported in the 2008 Update.

The Table ORTC1 was revised in the 2008 Update so that the DRAM M1 contacted half-pitch was on the same 2.5-year cycle as the MPU M1 contacted half pitch targets. The DRAM M1 contacted half-pitch targets for the 2009 ITRS Table ORTC1 remains unchanged on a 2.5-year technology cycle through 2010/45 nm. From 2010 through the 2024 timeframe, the DRAM M1 targets retain the 3-year technology cycle. The Flash Memory uncontacted poly half-pitch targets for the 2009 ITRS Table ORTC1 was extended on a two-year pace through 2010/32 nm, at which point it turns to a three-year technology cycle pace. The MPU M1 contacted half-pitch targets for the 2009 ITRS Table ORTC1 were revised to a trailing two-year cycle pace that crosses the DRAM M1 in 2010/45 nm. The two-year pace continues through 2013 and then turns parallel to the DRAM and Flash three-year technology cycle pace.

The blue mark on the Figure 3 graph indicates the timing for the next 2009 ITRS target for the DRAM 2010/45 nm and then continuing on the three-year cycle to 2013. Also included in the updated Figure 3 graphics are the data points for the new two-year cycle MPU trend (blue circle) and the Flash (violet rectangle) trends

Note that the first production of the leading-edge feature size has historically ramped into a 20–30% industry capacity share within one year, and the timing of that 20–30% capacity share has been on the same cycle as the same historical two-year-pace timing for first production. However, the latest SIA WSTS statistics for the "<0.08μm" technology demand split [added to the worldwide semiconductor trade statistics (WSTS) survey in 2008] indicate that the pace for that most-leading-edge capacity has actually accelerated faster than the two-year demand pace

Furthermore, the relative percentage of the most leading-edge technology capacity has been rapidly growing. The combined capacity of the most recent two technology generations has typically grown to nearly half the capacity of the industry within two to three years after their introduction. The 2009 ITRS has updated the Flash technology trend to continue on a two-year cycle until 2010, which should add even more capacity at the most leading edge.

It can be observed in Figure 3 that the capacity for the most leading edge technology (45 nm) is presently only available within the SICAS "<0.08μm" capacity split. The availability of the "<0.06 μm" split survey data, which would include the rapidly ramping 45 nm Flash and MPU/ASIC technology cycle capacity, has been delayed from SICAS until 2010. Therefore, the actual analysis of the 1.5-year to three-year technology demand cycles (to the 20–30% of total MOS capacity ramp point) will not be available until possibly the 2010 Update of the ITRS.

It is notable that relative share of trailing edge capacity does not decline as rapidly as might be expected (migrate upward to leading-edge); and the leading-edge capacity split shares should be expected to continue to "crowd" as products migrate to the most leading-edge capacity ("<0.08 μm" capacity data). This phenomenon continues to hold significant implication for the markets and business models of the materials and equipment suppliers that ultimately develop and deliver the required solutions to the ITRS technology Grand Challenges.

Suppliers must provide support for not only the longer-lasting trailing edge factories, but also the many diverse product and technology factories at the leading edge. In addition, suppliers must deliver alpha and beta tools and materials two to three years ahead of the first production requirement, and then they must be prepared to ramp into production with overlapping technology demand capacities. These scenarios present both a market opportunity and also an R&D and support resource challenge to both suppliers and manufacturers, especially with the preparation for 450 mm wafer generation investments.

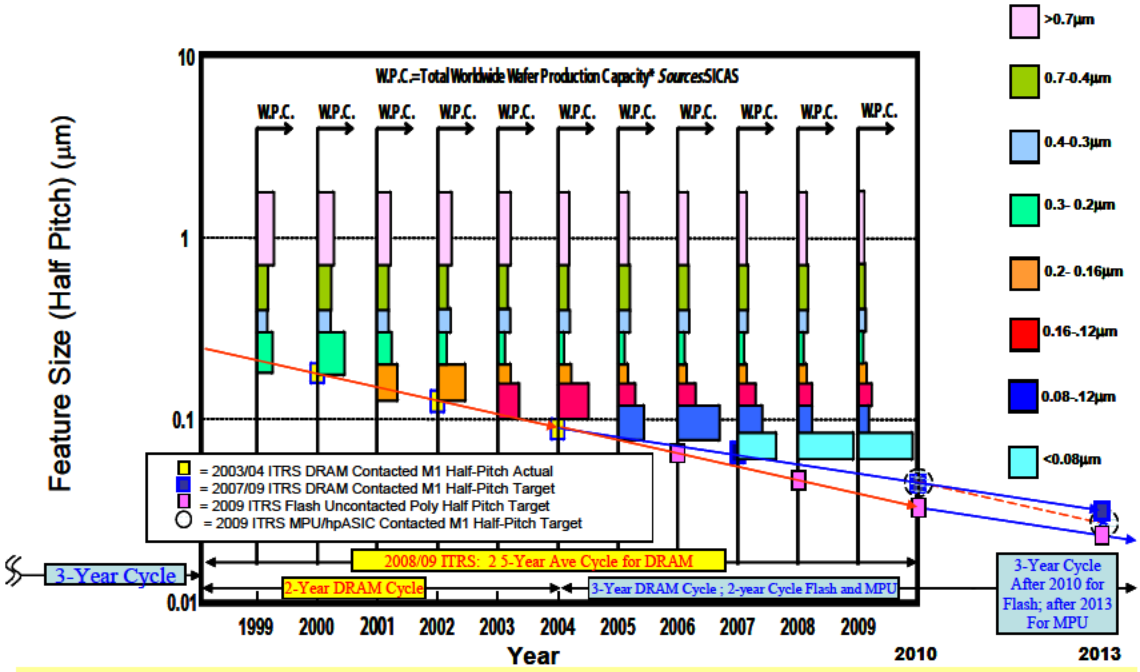


Figure 3 Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution[1]

ROADMAP SCOPE

Traditionally, the ITRS has focused on the continued scaling of CMOS (Complementary Metal-Oxide-Silicon) technology. However, since 2001, we have reached the point where the horizon of the Roadmap challenges the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths below 9 nm). It is also difficult for most people in the semiconductor industry to imagine how we could continue to afford the historic trends of increase in process equipment and factory costs for another 15 years! Thus, the ITRS must address post-CMOS devices. The Roadmap is necessarily more diverse for these devices, ranging from more familiar non-planar CMOS devices to exotic new devices such as spintronics. Whether extensions of CMOS or radical new approaches, post-CMOS technologies must further reduce the cost-per-function and increase the performance of integrated circuits. In addition, product performance increasingly does not scale only with the number of devices, but also with a complex set of parameters given by design choices and technology. Thus new technologies may involve not only new devices, but also new manufacturing and design paradigms.

Microprocessors, memories, and logic devices require silicon-based CMOS technologies. The downscaling of minimum dimensions enables the integration of an increasing number of transistors on a single chip, as described by Moore's Law. The essential functions on such a system-on-chip (SoC) are data storage and digital signal processing. However, many quantitative requirements, such as power consumption and communications bandwidth (e.g., RF), and many functional requirements, such as the functions performed by passive component, sensors and actuators, biological functions, and even embedded software functions, do not scale with Moore's Law. In many of these cases, non-CMOS solutions are employed. In the future, the integration of CMOS- and non-CMOS based technologies within a single package (or system-in-package, (SiP)) will become increasingly important. In terms of functionality, SoC and SiP can be complementary, and hence are not necessarily competing with each other. Functions initially fulfilled by non-CMOS

[1] *The data for the graphical analysis were supplied by the Semiconductor Industry Association (SIA) from their Semiconductor Industry Capacity Statistics (SICAS). The SICAS data is collected from worldwide semiconductor manufacturers (estimated >90% of Total MOS Capacity) and published by the Semiconductor Industry Association (SIA), as of August, 2009. The detailed data are available to the public online at the SIA website, www.sia-online.org.*

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dedicated technologies may eventually be integrated onto a CMOS SoC, using mixed technologies derived from core CMOS. Consequently, the partitioning of system-level functions between *and within* SoC and SiP is likely to be dynamic over time. This will require innovations in cross-disciplinary fields, such as nano-electronics, nano-thermomechanics, nano-biology, extremely parallel software, etc. For SiP applications, packaging will be a functional element and a key differentiator. This trend is represented graphically in the 2009 ITRS Figure 4.

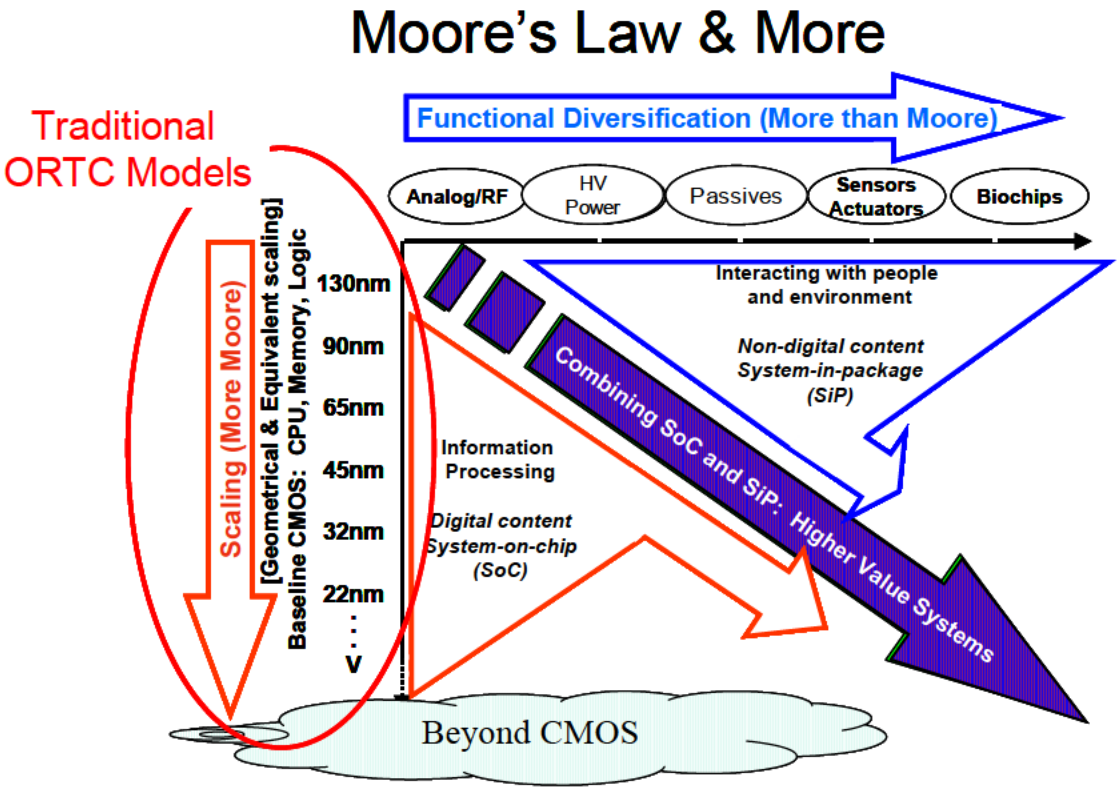


Figure 4 Moore's Law and More

MORE THAN MOORE

This concept of "More than Moore," introduced in the 2005 roadmap, has been further discussed and refined since. For example the "Beyond CMOS" concept has been given more discussion and detail in the ERD and ERM chapters, and white papers have been placed on the public website to provide more details on the "More Than Moore" and system-on-chip (SOC) and system in package (SIP) concepts. In addition consensus was reached on the following definitions, which were added and updated in the 2009 ITRS. (Refer to Figure 4 and the Glossary):

Scaling ("More Moore")—

- *Geometrical (constant field) Scaling*—refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)*—refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)*—refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
    - "Examples (not exhaustive) are: design-for-variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multi-core SOC architectures."

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- Addresses the need for quantifiable, specific design technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs; and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

- Design technologies enable new functionality that takes advantage of More than Moore technologies.
- "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology."
- Addresses the need for design technologies which enable functional diversification

Beyond CMOS—emerging research devices (ERD) and Materials (ERM), focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switches, and nano-electro-mechanical-system (NEMS) switches.

It is expected that the relative weight of the "More than Moore" component of the industry evolution will increase over time. This increase leads to a growing diversity of the scientific fields that the research must cover in order to sustain the pace of innovation, while the financial constraints are becoming tighter. The question of the guidance of the research efforts, in which the ITRS is playing a pivotal role, is therefore crucial. Taking this into consideration, various working groups of the ITRS have been investigating the consequences of the "More than Moore" trend in their field of expertise. The results of that work, which will further gain momentum in the coming years, can be found in their respective chapters.

The scope of the 2009 ITRS specifically includes detailed technology requirements for all CMOS integrated circuits, including wireless communication and computing products. This group constitutes over 75% of the world's semiconductor consumption. Of course, many of the same technologies used to design and manufacture CMOS ICs are also used for other products such as compound semiconductor, discrete, optical, and micro-electromechanical systems (MEMS) devices. Thus, to a large extent, the Roadmap covers many common technology requirements for most IC-technology-based micro/nanotechnologies, even though that is not the explicit purpose of the Roadmap.

2009 ITRS SPECIAL TOPICS

ENERGY

Energy consumption has become an increasingly important topic of public discussion in recent years because of global CO_2 emission. Since semiconductor electronics are broadly applicable to energy collection, conversion, storage, transmission, and consumption/usage, it is not surprising that the ITRS addresses many factors of significance to energy issues. In general, the ITRS documents the impressive trends and, more importantly, sets aggressive targets for future electronics energy efficiency, for example, computational energy/operation (per logic and per memory-bit state changes). The most detailed targets relate directly to semiconductor materials, process, and device technologies, which form the bases of integrated-circuit manufacturing and components, respectively.

At the next level, the ITRS addresses integrated circuit design and its system-level drivers. In both the ITRS Design and the ITRS System Driver chapters, there is increasingly direct influence of energy factors on design technologies, which started a number of years ago. Power consumption is now one of the major constraints in chip design, and the ITRS has identified it as one of the top three overall challenges for the last 5 years. Leakage power consumption, including its variability, has been identified as a clear long term threat and a focus topic for design technology in the next 15 years. The connection with the energy challenge is based on the increasing worldwide usage of information technology devices.

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In addition to improved efficiency of the basic components (i.e., switches, wires, and memory bits) and of the circuits they compose, the major favorable impact on energy usage of advancing semiconductor technology is in the applications of the circuits themselves, which are often designed specifically to improve the energy efficiency of end-equipment systems which they control. For example, microcontrollers, signal processors, and power/battery management circuits are key to the efficiency of communications systems, household appliances, transportation (e.g., cars), industrial machines, etc.

The ITRS also addresses the minimization of energy usage in semiconductor manufacturing. In particular, the Factory Integration and the Environmental, Safety, and Health chapters present goals for further reducing the amount of energy and other resources required to produce integrated circuits and to generally increase the environmental friendliness of IC fabrication. For 2008, the Factory Integration Technology Working Group agreed to use Wait Time Waste and Equipment Output Waste as the first two high level metrics for which to define a roadmap for waste reduction.

Their next goal is to incorporate waste reduction roadmaps for these two metrics in the 2009 ITRS update. They report "Systematic waste visualization is expected to identify waste in both material and energy use. A strategy will be defined for how to determine the starting point/baseline value and the feedback mechanism for each high level metric."

Similarly, the 2008 Front-End Processing (FEP) Technology Working Group reports that with respect to the current global energy and environmental situation, technology development in FEP is now driven not only by a desire to improve circuit density and speed, but also by a desire to reduce power consumption and manufacturing waste. The implementation of high-k/metal gate technology for logic transistors provides faster transistors while simultaneously reducing leakage and power consumption. Both power consumption and performance will eventually drive the transitions to Fully Depleted Silicon-On-Insulator (FDSOI) and MG transistor structures. As has already been noted at various points in the 2007 ITRS publication, efforts continue to reduce chemical and material usage and waste. For instance, more dilute solutions continue to be implemented for cleaning steps. In addition, FEP continues to work closely with the Factory Integration technology working group to identify process equipment that could be put into a reduced power consumption 'sleep mode' condition while not being used to process wafers. Of course, the concept of "sleep" and other energy-saving modes originated in circuit design. The Glossary of the 2008 ITRS documents these techniques as part of Design Equivalent Scaling. See the previous section "More than Moore."

Finally, near its 15-year horizon, the ITRS anticipates beyond-CMOS devices that may greatly extend the energy efficiency of information technologies. As part of its work in this area, the Emerging Research Devices Technology Working Group summarized the output of the 2008 Virtual Immersion Architecture (VIA) Forum: "An area of concern is that the growing popularity of VIA applications is driving a substantial increase in global energy consumption. This emphasis on more computational throughput per unit of energy holds not only for desk-top machines but also for handheld devices. In hand-held applications very little energy is available for information processing, and much higher performance per joule of expended energy is required if the extended range of applications is to be realized. Both of these trends imply that computation performance, in some suitable metric, must be increased by one-to-two orders of magnitude by 2020. This raises the question of the maximum attainable performance per joule and suggests a rapprochement between information theory and thermodynamics. An approximate, first principles analysis of a four-instruction, single-bit processors indicates that operating efficiencies of less than thirty percent are being realized by CMOS technologies and classical computing architectures. Perhaps architectures that can adapt themselves to their workloads to achieve energy-efficient operation would offer an alternative approach with higher performance per joule of energy expended."

ITRS will continue to focus diligently on energy-related issues along the directions outlined above, and to make important contributions to the energy challenges facing the world.

EMERGING RESEARCH MATERIALS

Many of the new device and memory concepts that are being discussed in the ERD chapter will employ new materials, for example, for the device itself as well as for interconnect and passivation. The requirements for these new materials are critically dependant on the properties and specifications of the new devices and memories. This led in 2005 to the creation, within the ERD chapter, of a sub-group for Emerging Research Materials (ERM). In the 2007 edition of the roadmap, this subgroup had become a full-fledged working group, and the results of this work are further expanded and enhanced in 2009 and published in the dedicated Emerging Research Materials (ERM) chapter.

TRANSITION TO 450 MM

The rationale for a transition to 450 mm diameter wafer is productivity, one of the enablers of Moore's law. This is the ability—everything else staying the same—to decrease the manufacturing cost of each mm² of IC by the use of larger

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diameter wafers. Based on economic considerations, during the 2007 ITRS roadmap development, the International SEMATECH Manufacturing Initiative (ISMI) had determined that to stay on this productivity curve, the industry needed to achieve 30% cost reduction and 50% cycle time improvement in manufacturing by 2012, which in their opinion would be achievable only via a transition to 450 mm (while the cost reduction goal has been achieved through previous wafer generation changes, the cycle time goal is new). This was reinforced in 2007 by the conclusions of an analysis of potential 300 mm improvements, which showed that the so-called "300 mm Prime" program had cycle time opportunity but fell short of the traditional cost reduction required to stay on Moore's Law. This realization prompted ISMI to kick-off the 450 mm initiative in July 2007.

More recently, Intel, Samsung, and TSMC (IST) announced in May 2008 that they will work together with suppliers, other semiconductor players, and ISMI to develop 450 mm with a goal of a pilot line in 2012. Full production may be two to three years after that.[2]. This Public announcement and assessment may be subject to revision based on future statements; but it is the statement of record by these three companies and ISMI, as of the date of writing of the ITRS 2009 edition

The timing of the production ramp of 450 mm facilities (versus early pilot line capability) depends not only on the mastering of all technical issues, associated with this transition to a new diameter, but also on the preparedness of the industry. To assess the likelihood of that timing, the whole value chain must therefore be examined:

- On the equipment suppliers' side, the ITRS is lacking visibility on the plans of key suppliers for prototype tools.
- On the manufacturers' side, an important question is related to the initial investment "step function": the promises for productivity gains in 300 mm fabs have proved to become true for very large investments, in the range of $4B or beyond. One might expect that the minimal economical size of a 450 mm fab will be even larger, putting it beyond the reach of many companies. Furthermore, while an economic model which takes into consideration the industry as a whole may conclude that 2012 is the right time for transition to 450 mm (as concluded by the ISMI in 2007), decisions of individual companies may differ. So both the initial rate of growth of the 450 mm equipment market and its size at maturity can be questioned, which could lead equipment suppliers to delay their investment in the development of this new generation.

Taking lessons from the past, it can be observed that each wafer size transition has been different from any of the previous ones. The conversion to 300 mm wafer can be characterized by fact that for the first time the consortia (I300I and Selete) led the whole industry effort. The well-tested consortium effort is also the chosen approach for the 450 mm wafer size conversion. SEMI participation was also essential in the 300 mm wafer size conversion since for the first time "provisional standards" were agreed upon by the whole industry before the final manufacturing equipment was fully developed. In particular, the industry solved a fundamental problem by agreeing on adopting full wafer transport automation. All the suppliers abandoned their proprietary solutions to wafer transport, port design, and load size in favor of the agreed FOUP/ overhead solution. This effort took many years of discussion before the final solution was finally agreed by all parties. In this respect, the 450 mm wafer size transition is taking fully advantage of the work previously done to standardize the 300 mm wafer transport by having already adopted the same whole automation scheme with only minor upgrades thus placing the 450 mm automation schedule ahead of the corresponding 300 mm wafer size conversion schedule with respect to automation.

On the other hand, the Front-End Processes working group has advised the IRC that, although significant progress has been made and reported by SEMATECH/ISMI, specific development-level targets for epi and flatness have not yet been met, and is now estimating that wafer suppliers will move the work on 450 mm wafers from research to development by 2011. For 300 mm, this transition occurred approximately seven years before 300 mm was used by IC manufacturers in production, which would put 450 mm production timing by 2018 if development will continue at the same rate as before. Accelerated development on this item (which may be underway in the work at SEMATECH/ISMI with suppliers), will be required to achieve a transition date for IC manufacturers to start moving to 450 mm in the 2014–2016 timeframe. For that reason, the FEP starting materials metrics table (Table FEP10) colored 450 mm "yellow" for 2014, showing a possible timing disconnect with the IST/ISMI 2014 production date, while not excluding it, and the need for deliberate wafer supplier industry effort to be in line with the planning announced by ISMI and the three IST companies. Progress will continue to be monitored during the work and conferences of the ITRS 2010 Update work.

Given all of the above, and with advancements on the work of Next Generation Factory (NGF) programs at SEMATECH/ISMI that may create opportunities for improvement of 300 mm equipment which might eventually also be

[2] *Source: "May 2008"/ "Oct 2008 ISMI symposium"/Dec'08 ISMI 450 mm Transition Program Status Update for ITRS IRC,Seoul,Korea*

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applicable to 450 mm processing, the ITRS IRC expects manufacturing tools to be available between 2012 to 2014 for pilot lines; with possible production manufacturing ramp from 2014–2016 and beyond, subject to 450 mm wafer high volume availability at that date. The ITRS/IRC further estimates that wafer diameter should not be tied to technology generations—leading edge technologies will for a limited period be running both in 300 and 450 mm technologies, as happened with the 300 mm wafer generation ramp on two succeeding technology cycles in the 2001–2003 (180 nm-130 nm M1) timeframe.

Furthermore, and new in the 2009 ITRS, a 450 mm Production Ramp-up Model Graphic has been provided (Figure 5) to clarify the special dual "S-curve" timing required when a new wafer generation is being introduced (modeled after the experience with the 300 mm wafer generation ramp on two succeeding technology cycles in the 2001–2003 (180 nm-130 nm M1) timeframe.

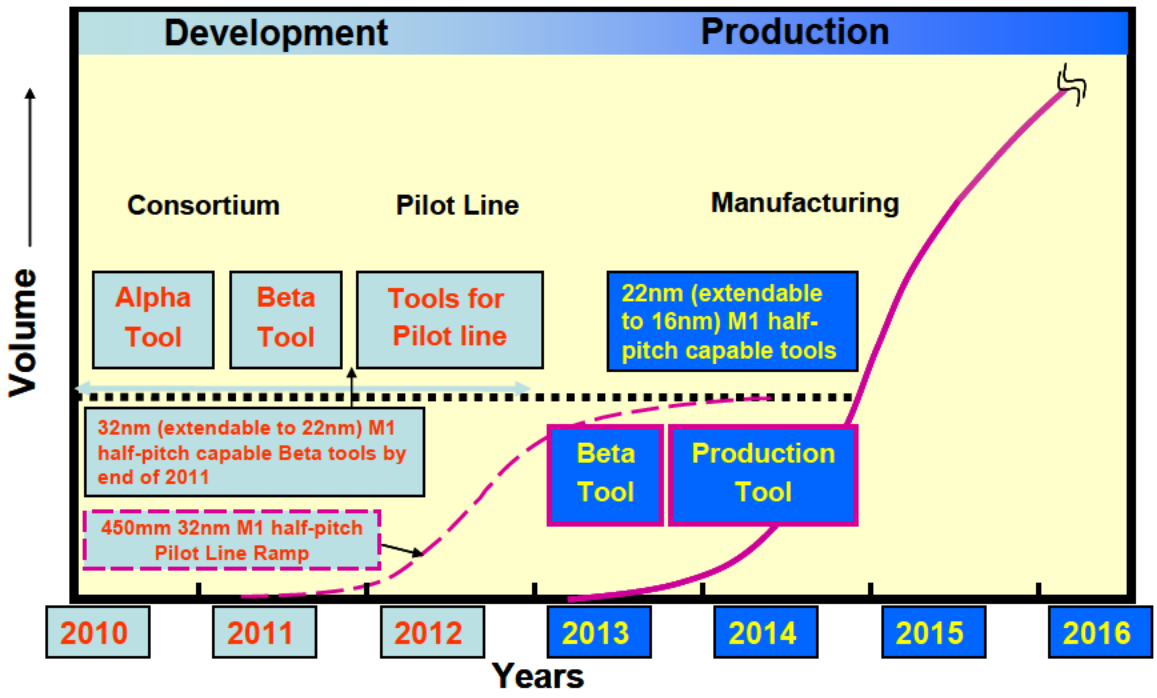


Figure 5 A Typical Wafer Generation Pilot Line and Production "Ramp" Curve applied to Forecast Timing Targets of the 450 mm Wafer Generation

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GRAND CHALLENGES

IN THE NEAR-TERM (THROUGH 2016) AND LONG-TERM (2017 AND BEYOND)

OVERVIEW

The continued research and development efforts in our industry have brought about reacceleration and diversification of scaling. Flash device's scaling continues a two-year cycle until 2010, MPU is also on a two-year cycle until 2013, and DRAM is a three-year cycle. The word "node" cannot define technology trend clearly anymore. In the chapter on PIDS, it is observed that there are many choices to improve MOSFET performance, which we call "Parallel Paths" of planar bulk metal-oxide semiconductor field effect transistor (MOSFET), multiple gate field effect transistors (e.g., FinFET), and silicon-on-insulator MOSFET.

The ITRS is entering a new era as the industry begins to address the theoretical limits of CMOS scaling. There remain many technological challenges in patterning, advanced materials, strain engineering particularly in non-planar device structures, junction leakage, process control, and manufacturability. Challenges also span SoC and SiP integration of CMOS with new types of memory devices. All these will be essential elements for the continuous growth of the semiconductor industry.

Each ITWG identified and listed "Difficult Challenges," which are included in this Executive Summary. In this section of "Grand Challenges," major "Difficult Challenges" are selected and described. This section is intended to help readers grasp an overall picture concerning major technological issues.

These "Grand Challenges" are classified into two categories: "Enhancing Performance" and "Cost-effective Manufacturing." They are also described according to the "near term" (2009 through 2016) and the "long term" (2017 through 2024) timeframes of the Roadmap.

IN THE NEAR TERM (THROUGH ~ 2017)

ENHANCING PERFORMANCE

LOGIC DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, FRONT END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

Scaling planar CMOS will face significant challenges. The conventional path of scaling, which was accomplished by reducing the gate dielectric thickness, reducing the gate length, and increasing the channel doping, might no longer meet the application requirements set by performance and power consumption. Introduction of new material systems as well as new device architecture, in addition to continuous process control improvement are needed to break the scaling barriers.

Reduction of the equivalent gate oxide thickness (EOT) will continue to be a difficult challenge particularly for the HP and LOP segments in the near term despite the inception of high-κ metal gate (HKMG). Interfacial layer scaling and/or silicon-high-κ interface quality are critical to the EOT scaling for the 22 nm node and beyond. Integration of higher-κ materials while limiting the fundamental increase in gate tunneling currents due to band-gap narrowing are also challenges need to be faced in the near term. The complete gate stack material systems need to be optimized together for best device characteristics (power and performance) and cost. These material changes pose a great challenge in MOSFET technology, where silicon dioxide/poly Si has long played a central role as the most reliable gate stack system.

Planar MOSFET requires high-channel doping to control short-channel effects, the trade-offs are mobility degradation and increased leakage power consumption. Using doping to control threshold voltage in scaled device also causes increasing variation of the threshold voltage, posing difficulty in circuit design while scaling the supply voltage. New device architecture such as multiple-gate MOSFETs (e.g., finFETs) and ultra-thin body FD-SOI are expected. A particularly challenging issue is the control of the thickness, including its variability, of these ultra-thin MOSFETs. The solutions for these issues should be pursued concurrently with circuit design and system architecture improvements.

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MEMORY DEVICE SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES, EMERGING RESEARCH DEVICES, FRONT-END PROCESSES, MODELING AND SIMULATION, AND METROLOGY]

The continued research and development efforts in the industry have brought about reacceleration and diversification of scaling. The baseline memories now includes both stand-alone and embedded DRAM and SRAM, and both NAND and NOR Flash. The new prototype memories table includes silicon/oxide/nitride/oxide/silicon (SONOS), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase-change memory (PCM).

The challenges for DRAM devices are adequate storage capacitance with reduced feature size, high-κ dielectrics implementation, low leakage access device design, and low sheet resistance materials for bit and word lines. For stand-alone DRAM, high-κ materials are currently being used in an SIS structure for trench capacitors. Metal top electrode will be needed by 2007 and a full MIM structure with high-κ dielectric may be needed by 2009, when a dielectric constant greater than 60 is required for beyond 50 nm. Embedded DRAM in SOC applications will drive additional integration challenges. One such key challenge is the matching between the ground rules required for the deep contacts around the stacked capacitor with the contact ground rules for the logic devices.

The need for advanced capacitor materials in trench DRAM are postponed relatively to the stacked capacitor by a few years; however the cell size factor for stack capacitor DRAM is 6, while that for the trench DRAM remains at 8. Novel cell concepts for the trench capacitor, depending upon the replacement of the conventional planar transfer device by 3D array transistor structures, are envisaged for 65 nm in order to alleviate device scaling issues.

The rapid expansion of the market for Flash memories brings more focus on the material and process challenges for these devices. With this acceleration, Flash memory is becoming a new technology driver for both critical dimension scaling and material technology. The effective dimension, F, of Flash NAND device now appears to lead the DRAM half pitch.

The key challenges in Flash memory device are non-scalability of tunnel dielectrics, non-scalability of interpoly dielectrics, dielectric material properties, and dimensional control. In Flash memory devices, continuous scaling and the reduction in write voltage requires the use of a thinner inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. It is no longer feasible for the control gate poly Si to overlap the sides of the floating gate as the space between adjacent poly Si gates shrink. Thus high-κ interlayer dielectrics will be required to maintain an acceptable coupling ratio. Flash memory challenges also include the inception into mainstream manufacturing and the scaling of new memory types and storage concepts such as MRAM, phase-change memory, and FeRAM, for example. MRAM scalability of cell-size and write-power reduction still needs further breakthroughs. FeRAM critical issues relate to cell endurance, scalability of power supply and cell-size. Another challenge for MRAM and FeRAM going forward is their cost effective integration with logic technologies, FeRAM being particularly more challenging while MRAM seems more suitable for integration in the backend of the flow. Complex/transitional metal oxides resistive cells could have the potential for high density apps, if cross-point diode and 3D integration are successful.

HIGH-PERFORMANCE, LOW-COST RF AND ANALOG/MIXED-SIGNAL SOLUTIONS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS]

Cost, power consumption and performance of wireless transceiver ICs in the <10GHz and the mm-wave applications continue to be the main technology drivers. The <10GHz application space, serviced by deep sub-micron CMOS technologies with emerging high κ dielectrics and channel strain engineering may require techniques to keep the device mismatch and the 1/f noise within acceptable levels. Applications that use HBT devices will benefit from a more aggressive vertical scaling. Less expensive integrated passive components with higher Q factors and higher densities for the MIM capacitor may require integration of new materials. MEMS development, MEMS integration with active Si and off-chip passive network processes are expected to significantly contribute to the overall system performance. Mm-wave applications will benefit from development of non-Si (GaN) based devices.

Signal isolation between the digital and the analog regions of the chip is becoming more critical as the chip complexity and operating frequencies increase while the power supply voltage decreases. While noise coupling through the power supply and the ground line can be addressed by design techniques, substrate noise coupling reduction may require significant amount of innovation.

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NEW GATE STACK PROCESSES AND MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND FRONT END PROCESSES]

Major breakthrough in the gate stack of silicon-based field effect transistors in advanced microprocessors with nitrided SiO_2 gate dielectric replaced by a hafnium-based dielectric with a dielectric constant (κ) approximately 20 took place in 2008. The n- and p-doped polysilicon gate electrodes also got replaced by dual work function metal gates that eliminated poly depletion effects. Still, reduction of the equivalent gate oxide thickness (EOT) below 0.8 nm for 16 nm node and below 0.6 nm beyond 16 nm node with appropriate metal gates remains as the most difficult challenge associated with the future device scaling. Higher dielectric constant dielectrics with adequate conduction and valence band offsets with silicon and thinner interfacial silicon dioxide layer are required. Reduction of interface states for gate stack on multi-gate devices is one of key challenges for 16 nm node and beyond. Another critical challenge is scaling the interfacial layer between the high-κ dielectric and the silicon without channel mobility degradation from increased Coulomb and remote phonon scattering. Higher mobility materials such as Ge, SiGe, and III-V compound semiconductors will be needed for channel transport enhancement which will introduce additional challenges for future high-κ dielectric stacks due to the complex nature of their surfaces and lack of a high quality native interfacial oxide. Furthermore, reliability requirements for newer high-κ oxides, including dielectric breakdown characteristics (hard and soft breakdown), transistor instability (charge trapping, work function stability) must be resolved.

Continued DRAM scaling requires construction of memory capacitors in ever-smaller cell area, while maintaining the memory capacitance of 25–35 fF to ensure reliability of stored data. This will result in the introduction of dielectric materials with a higher dielectric constant (higher-κ), such as tetragonal zirconium oxide, tantalum oxide, Ba/Ti doped high-κ dielectrics or a combination of them in a multi component stack, along with a 3D memory structure. Going down to sub 3Å equivalent oxide thickness beyond the sub-45 nm node while maintaining very low leakage current (femto ampere per cell) is one of the major challenges the DRAM industry is facing.

In Flash memory devices, on the other hand, continuous scaling and the reduction in write voltage requires the use of a thinner inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of erase/write. Inter-poly dielectric must be thick enough to assure retention but thin enough to keep an almost constant coupling ratio. This difficult trade-off problem hinders scaling, suggesting the need to introduce high-κ material and 3D structure devices into Flash memory processing. While replacing the floating gate by either charge trapping layers or embedded nanocrystals will facilitate scaling, the grand challenge is to maintain adequate electron storage during cycling within the trapping layers in scaled device footprints to ensure sufficient read margins. This will be more challenging in multi level cells (MLC) where less than 10 electrons will separate the storage bits.

32 AND 22 NM HALF PITCH [LITHOGRAPHY]

32 nm half pitch remains a crucial turning point for lithography imaging scheme. The 193 nm water immersion process is limited with NA to resolve this pitch, unless tight pitches are split into larger ones by double patterning or exposure; however the lithography cost will almost double. Extreme-UV lithography (EUVL) with wavelength reduced to 13.5 nm, an order of magnitude smaller than that of the water-immersion wavelength of ArF excimer lasers, is the official hope of the industry to advance Moore's law. It does not need double exposure until approaching the 11 nm half pitch. As a result there is less restriction in design rules. However, EUVL is still awaiting high-power and high-efficiency sources, fast resists, defect-free and high-flatness masks, as well as related infrastructures. Development efforts in these areas are heavy. Multiple-e-beam maskless lithography, which has the potential to bypass mask difficulties, remove restricted design rules, and provide manufacturing flexibility, is in an early-stage of development. Two pre-alpha tools are in the field. Progress has been made in demonstrating high-resolution imaging and CD control. Timing of manufacturing tools, costs, defects, overlay accuracy, and resists are other areas to further develop.

For 22-nm half-pitch lithography, water-immersion 193 nm scanners and double patterning will be severely stretched with extremely large mask error enhancement factor (MEEF), wafer line edge roughness (LER), and design rule restrictions. Resorting to more than two passes through the patterning tools can alleviate some of the above problems at the expense of higher costs. The numerical aperture of EUV systems will have to be raised to more than 0.36 to have the k_1 factor comparable to NA 0.25 for 32 nm half pitch. There is a likelihood of increasing the number of mirrors in the imaging lens, thus leading to requirement of even higher power source while limiting throughput loss, thus less favorable economy. Multiple-e-beam maskless lithography will be better developed by that time but it has to support a high writing rate per beam or more parallelism to maintain the increased pixel count within the same-size field. If the potential is realized to keep the per-pass exposure and processing cost as well as the footprint similar to that of mask-based exposure tools, then it will be the most economical and sought-after solution for logic and memory applications.

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MASKS [LITHOGRAPHY]

The mask technology is becoming very expensive and challenging. Mask cost has escalated each generation. Increased resolution plus larger MEEF, due to higher levels of resolution enhancement technique (RET), make the mask CDU difficult to meet. Double and multiple patterning impose stringent requirement of mask pattern placement accuracy. Mask feature sizes becoming sub-resolution coupled with finite absorber thickness and polarized illumination worsen the problem. EUV masks have further stringent requirements of defect-free ultra-flat substrate and exposure without a pellicle. Inspecting advanced masks is expensive and time consuming. The inspection resolution is reaching limits with practical inspection wavelengths. Actinic mask inspection and verification are eventually inevitable for EUVL. It further adds to the cost and complexity of the EUV mask infrastructure.

RESISTS [LITHOGRAPHY]

LER of photoresist has substantially sustained the same absolute value and therefore has attained an even larger percentage of CD. As pattern geometry shrinks, shot noise starts to become an issue. Resist collapse after development limits its height-to-width aspect ratio to between 2.5 and 3, thus reducing the absolute resist thickness at each technology-generation advancement. With immersion lithography, resist material development has to ensure low resist-induced defectivity, further restricting material choices. For EUVL, resist outgassing can contaminate the delicate reflecting optical surfaces. The tradeoffs between high resist sensitivity for throughput, low resist sensitivity for shot noise, and low LER, impose more problems than just resist collapse. E-beam resists also have to trade off for sensitivity and shot noise as well as LER. The sensitivity requirement is not as severe as that of EUVL.

CD AND L_{EFF} CONTROL [FRONT END PROCESSES, LITHOGRAPHY AND PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

With the aggressive scaling of gate length, control of CD has been one of the most difficult issues in lithography and etching. In particular, resist slimming and profile-control of the sidewall, which are commonly utilized to minimize the dimension of effective gate length (L_{eff}), have made CD control far more difficult. Although the acceptable 3-sigma variation of the gate length is shared by lithography and etching at an optimum ratio, the tolerances in both technologies are approaching their limits. The inception of increasingly restrictive design rules aimed to promote design regularity have become mainstream as key enablers for near term scalable CD control. Line-edge-roughness (LER) has become also a critical element of device variability. Suppression of LER will continue to pose significant challenges to patterning processes (etch and lithography) as well to metrology in terms of accuracy and throughput. Moreover, the introduction of new gate materials and non-planar transistor structure requires many more challenges in selective etch processes, and improved anisotropy with the controlled sidewall features.

INTRODUCTION OF NEW MATERIALS TO MEET HIGH CONDUCTIVITY AND LOW DIELECTRIC PERMITTIVITY REQUIREMENTS [INTERCONNECT]

To minimize signal propagation delay and power consumption, the industry introduced high-conductivity metal and low-permittivity dielectric through damascene processes at 130 nm. Even lower permittivity dielectric has been introduced at 45 nm. The continued scaled-down interconnect poses increasing challenges to technology development and manufacturing. The fast introduction of new metal/dielectric systems becomes critical. For low-κ dielectrics, the conventional approach is the introduction of homogeneous porous low-κ material. Reduction of κ damage due to Etch and CMP processes becomes more important with more porous materials. Another approach is air gap. It attracted attention because it keeps same low-κ materials with more volume of air gaps that gives lower effective κ. Among various techniques to incorporate air gaps, thermal or UV degradable sacrificial layer method is one of the low-cost approaches. Furthermore, low-κ material must have sufficient mechanical strength to survive dicing, packaging, and assembling. For the metal, fast rising resistivity of narrow Cu wires due to electron scattering at the Cu/barrier metal or dielectric interfaces and the grain boundary has become a key challenge. A very thin and conformal low-resistivity barrier metal is required to integrate with Cu to achieve low resistivity and good reliability.

ENGINEERING MANUFACTURABLE INTERCONNECT [INTERCONNECT]

The integration of conductive and low-κ material must meet material, geometrical, planarity, and electrical requirements. The low-κ material with good mechanical, chemical, thermal, and physical properties are needed for manufacturable integration with other processes that may induce damage, in particular dry and wet etching, ashing, sputtering, and polishing. Defect, variability, and cost must be engineered to ensure a manufacturable process. The advancement of interconnect should address performance, power, and reliability issues for traditional scaling or equivalent scaling with functional diversity. Since material solutions with traditional scaling cannot deliver performance, new technology has been proposed in recent years including 3D (including tight pitch through silicon vias (TSV)) or air gap structures,

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different signaling methods, novel design and package options, emerging interconnect using different physics and radical solutions, etc. The realization of these innovative technologies challenges new material systems, process integration, CMOS compatibility, metrology, predictive modeling, and optimization tools for interconnect/packaging architecture design.

POWER MANAGEMENT [DESIGN]

Cost-effective heat removal from packaged chips remains almost flat in the foreseeable future. Driven by the 2× increase in transistor count per generation, power management is now the primary issue across most application segments. Power management challenges need to be addressed across multiple levels, especially system, design, and process technology. Circuit techniques to contain system active and leakage power include multiple V_{dd} domains, clock distribution optimization, frequency stepping, interconnect architectures, multiple V_t devices, well biasing, block shutdowns among others. The implementation challenges of these approaches expand upwards into system design requirements, the continuous improvements in CAD design tools for power optimization (including design robustness against process variability), and downwards into leakage and performance requirements of new device architectures.

CIRCUIT ELEMENT AND SYSTEM MODELING FOR HIGH FREQUENCY (UP TO 160 GHZ) APPLICATIONS

Accurate and efficient compact modeling of non-quasi-static effects, substrate noise, high-frequency and 1/f noise, temperature and stress layout dependence and parasitic coupling will be of prime importance. Computer-efficient inclusion of statistics (including correlations) before process freeze into circuit modeling is necessary, treating local and global variations consistently. To support concurrent optimization of devices and circuits, efficient building block/circuit-level assessment using process/device/circuit simulation must be supported. Compact models are needed for III-V-, CMOS-, and HV- devices. Compact scalable models for passive devices are needed for varactors, inductors, high-density capacitors, transformers, and transmission lines. The parameter extraction for RF compact models preferably tries to minimize RF measurements. Parameters should be extracted from standard I-V and C-V measurements with supporting simulations, if needed. Extreme RF applications like 77 GHz car radar approach the 100 GHz range. Third harmonic distortion for 40 GHz applications implies modeling of harmonics up to 120 GHz. Modeling of effects that have a more global influence gains in importance. Examples are cross talk, substrate return path, substrate coupling, EM radiation, and heating. CAD-tools must be further enhanced to support heterogeneous integration (SoC+SiP) by simulating mutual interactions of building blocks, interconnect, dies and package dealing with possibly different technologies while covering and combining different modeling and simulation levels as well as different simulation domains.

FRONT-END PROCESS MODELING FOR NANOMETER STRUCTURES [MODELING AND SIMULATION]

Advanced USJ formation is critical to support continued scaling of device features. Millisecond anneal and SPER are expected to be widely used to reduce diffusion and enhance activation. Modeling capability and accurate calibration of the model parameters for dopant diffusion/activation and damage evolution during millisecond anneal and SPER will be critical. Since various channel materials will be required to further enhance mobility, such modeling will need to be done for various Si-based substrate including Si, SiGe:C, Ge, SOI, epilayers, and ultra-thin body devices. Such modeling will also need to account for additional factors, including, possible anisotropy in thin layers, co-implants and stress dependence, over layer influence including interface effects and the layer formation thermal process. Modeling of advanced implant technology such as use of molecular species for reducing damage will be needed. Epitaxial processes such as SiGe:C will be expanded to multi-channel devices with complex geometries, therefore, modeling of epitaxially grown layers including the shape, morphology will be useful to optimize such epitaxial processes. Extensive use of stress to enhance device mobility will continue. More accurate modeling of stress including material properties evolution during process such as plastic deformation during anneal, and stress relaxation due to defect generation will be needed. There will be continued needs for refining metrology / reverse modeling of USJ - 2D/3D doping/stress profiling to sufficient resolution to help calibration of simulation models and parameters. Devices are expected to largely deviate from quansi-2D and become 3D in nature, therefore more advanced 3D meshing to improve 3D computational efficiency and accuracy, especially for moving boundaries will be needed. Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces will be helpful in understanding nano-scale feature related effects. High-κ/metal gate is expected to be the basic building block, therefore modeling of High-κ/metal gate work function per charge and their reliability implications will be necessary.

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COST-EFFECTIVE MANUFACTURING

DESIGN PRODUCTIVITY AND DESIGN FOR MANUFACTURING [DESIGN]

The number of available transistors double every technology cycle, increasing design complexity as well. In order to maintain design quality even after process technologies advance, design implementation productivity must be improved to the same degree as design complexity is scaled. Improving design productivity and IP reuse are key considerations for this issue. Challenges at high-level abstraction, platform-based design, multiprocessor programmability, design verification, analog and mixed-signal circuit synthesis are critical to secure design productivity scaling at a pace consistent with process technology cycles. Cost-effective product manufacturing also requires continuous improvements in the area of design for manufacturability, specifically areas such as design to minimize performance/power variability, lithography-friendly designs (regular layout styles consistent with increasingly more restrictive design rules), and design for testability and reliability.

TEST COMPLEXITY [TEST AND TEST EQUIPMENT]

The complexity of next generation technologies is further convoluted by design and process interaction, which imposed challenges in yield learning for production ramp. Actual device characteristics on silicon could be dependent on layout environment and difficult, if not impossible, to be fully captured by model. As a consequence, the occurrence of abnormal product behavior either hard defect or parametric shift related is expected to worsen. The effectiveness and efficiency of test and analysis of product failure becomes the gating factor for yield ramp. Although the field of semiconductor failure analysis moves along with technology advancement, more effort is required to shortening the cycle time from product failure to root-cause fix by process or design. The areas for further improvement includes new equipment, methodology and software for (1) effective localization by DFT scan diagnostics and BIST, (2) physical failure analysis techniques, and (3) efficient implementation of refined DFM solution.

CONTINUED ECONOMIC SCALING OF TEST [TEST AND TEST EQUIPMENT]

The ever-improving economies of scale predicted by Moore's Law may not translate to test naturally. Design for test innovations, widespread use of structural test techniques such as scan testing, and the enabling of higher levels of test parallelism have been very successful in keeping test costs in check to date. However, new test requirements for increasingly complex devices, testing for yield learning, increasing quality requirements, and practical limits on parallel testing continue to present great challenges to test cost. In particular, test tooling cost including probe cards are not scaling and threaten to dominate the total test cost if present trends continue. Accelerating the test learning curve for new device architectures or integration schemes is critical to maintain test cost scaling curve in sync with overall technology cost-scaling goals. Product cost optimization should strike a balance between design, manufacturing, yield learning, and test while securing overall quality of shipped products. Automation of generation entire test programs for automatic test equipment (ATE), convergence of test and system reliability solutions, integration of simulation and modeling of test interfaces hardware and instrumentation into the device design process are challenging opportunities for test cost scaling reduction.

RESPONDING TO RAPIDLY CHANGING COMPLEX BUSINESS REQUIREMENTS [FACTORY INTEGRATION]

Wide ranging business models beyond the integrated device manufacturer (IDM) such as the fabless and foundry model, joint venture, and the variety of task sharing and out-sourcing scenarios have become pervasive in response to customers' rapidly changing complex business requirements. Furthermore, diversified customers' requirement on SoC devices have placed strong demand on manufacturing environments to rapidly and efficiently adapt to high-mix and low-volume product runs. These requirements continue to pose critical near-term challenges in several areas such as integration of larger numbers and different types of equipment, software applications, and fully featured software systems to manage the factory complexity while enabling decreasing time to ramp high volume production.

Development of information exchange/control platform covering all the relevant operation fields, extending from design, mask, front-end-of-line (FEOL), and back-end-of-line (BEOL) to testing, packaging, etc., is also a crucial challenge. Continuous improvements to model factory capacity and performance to optimize output, improve cycle time, and reduce cost are key to successful high-mix factory operations.

IMPROVEMENT IN TRADE-OFF BETWEEN MANUFACTURING COST AND CYCLE TIME [FACTORY INTEGRATION]

Enhanced tool availability, improvements in material handling automation and systems for operational flexibility and control; single-wafer manufacturing; and the reduction/elimination of non product wafers (NPW); are representative areas for continuous improvement in 300 mm lines to meet the challenges of cycle time and cost reduction. The transition from

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300 mm to the next wafer size (i.e., 450 mm) is another critical challenge for the semiconductor industry in the 2014–2016 time frame. This transition is considered critical to simultaneously meet the 30% cost/die reduction and a 50% improvement in cycle time.

MEET THE CHANGING COST AND PERFORMANCE REQUIREMENT OF THE MARKET [ASSEMBLY AND PACKAGING]

"More than Moore" is driving rapid change in packaging technology. Everything is changing: architectures, materials, processes, and equipment. Many new materials have been introduced in IC packages and more new materials will be continuingly introduced in the next few years in order to meet requirements of environmental regulations; to improve package performance; and to be compatible with low-k dielectrics used in Cu interconnects with 45 nm half pitch and beyond. Nano-materials present significant opportunities for the packaging community. 3D/SiP packaging requirements are stimulating new technologies: stacked die, wafer level packaging, through silicon vias, passive network interposers, embedded components, wafer thinning, wafer-to-wafer bonding, die-to-wafer bonding, and new materials. For automotive packaging, the rapid growth in hybrid and electric vehicles brings an additional class of electronics and a new subset of environmental conditions.

SOLUTIONS FOR INTEGRATION OF OFF-CHIP COMPONENTS [RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS, ASSEMBLY AND PACKAGING]

System-in-package solutions have been developed to meet different applications and system requirements especially in the rapidly changing and increasing market of portable wireless communication devices. The integration of these SiP solutions to construct a universal design platform is increasingly important. High Q RF devices by MEMS or other processes are usually off-chip and need to be made as integrated passive devices (IPD). Three-dimensional stacking and embedded components are two major methodologies to address off-chip components. Forming passive component (as opposed to inserting discrete components) into substrates often involves additional materials such as high-κ dielectric for capacitors, resistive films or paste for resistors, and high permeability (μ) material for inductors. Devising process simplification for this variety of embedded passives is a key challenge to enable a cost-effective alternative. Testing and tuning also pose significant challenges, especially after packaging or assembly processes. Accurate models that include process tolerances as well as circuit and tester parasitic elements are needed for designers to simulate circuit performance with embedded passives before the manufacturing process. Lack of CAD tools for embedded passives also needs to be resolved.

CHEMICAL AND MATERIAL ASSESSMENTS [ESH]

The rapid introduction of new chemicals, materials, and processes requires new rapid assessment methodologies to ensure that new chemicals and materials can be utilized in manufacturing without inducing new hazardous impacts on human health, safety, and the environment. Although methodologies are needed to meet the evaluation and quantification demands for ESH impacts, the focus is currently on expediting process implementation. As such, near-term challenges - include emissions reduction from processes using chemicals classified as having significant global warming potential (GWP), the complete transition to lead-free packaging, and the need for a robust and rapid assessment of new materials/chemicals critical to surmount technology roadblocks while complying with ESH requirements

RESOURCE CONSERVATION [ESH]

As the industry grows and its technology advances toward finer patterning and larger wafer sizes, the natural tendency is toward increased use of water, energy, chemicals, and materials. Resource conservation is becoming a major concern with respect to availability, cost reduction, manufacturing location, sustainability, and waste disposal. Thus, it is necessary to develop diverse process equipment capable of utilizing resources efficiently. Continuous improvement is needed in chemicals and materials utilization and energy consumption reduction in facilities and processing equipment, as well as in efficient thermal management of clean rooms.

DETECTION OF MULTIPLE KILLER DEFECTS AND SIGNAL-TO-NOISE RATIO [YIELD ENHANCEMENT]

Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes required by technology cycles. Inspection sensitivity can be increased to address defect size trends; however challenges arise in terms of efficiently and cost-effectively differentiating defects of interest (DOI) from a vast amount of nuisance and false defects. Reduction of background noise from detection units and samples are key challenges to enhance signal to noise ratio for defect delineation. Increasing aspect ratios and interconnect complexity will continue to pose increasingly difficult challenges and also opportunities to inspection tools development.

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LAYOUT STYLE AND SYSTEMATIC YIELD LOSS: HIGH THROUGHPUT LOGIC DIAGNOSIS CAPABILITY [YIELD ENHANCEMENT]

Random logic areas are very sensitive to systematic yield loss mechanisms such as patterning marginalities across the lithographic process window. Solutions exist but need continuous improvements. Before reaching random-defect limited yields, the systematic yield loss mechanisms should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. Potential issues can arise due to different automatic test pattern generation (ATPG) flows accommodation; ATE architecture that lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge, and logic diagnosis run time per die.

WAFER EDGE AND BEVEL CONTROL AND INSPECTION [YIELD ENHANCEMENT]

Defects and process problems around wafer edge and wafer bevel are known to cause yield problems. Development and continuous improvement in terms of defect detection, throughput, and cost of ownership (CoO) of wafer edge and bevel defect inspection tools are increasingly critical to yield enhancement in advance device technologies.

FACTORY-LEVEL AND COMPANY-WIDE METROLOGY INTEGRATION [METROLOGY]

Metrology areas should be carefully chosen and sampling must be statistically optimized for process control based on cost of ownership (CoO). *In situ* and inline metrology has become requisite for both tight process control and throughput. Information from all metrology (i.e., online and offline), associated with advanced process control (APC), fault detection and classification (FDC), and other systems should be integrated into an efficient database for determining process control parameters and key correlations to drive yield enhancement. Such efficient and seamless integration requires that standards for process controllers and interfaces, data management and the database structure be established. Continuous improvement of sensors, including calibration, sensing method, and data processing is clearly expected. Development of new sensors must also be concurrently done with the development of advanced process modules and ever increasing aspect-ratio levels

MEASUREMENT OF COMPLEX MATERIAL STACKS, INTERFACIAL PROPERTIES, AND STRUCTURES [METROLOGY]

Metal-gate high-κ gate stacks, advanced strain and mobility enhancement techniques, as well as advanced interconnect and low-κ dielectric structures require novel or continuous improvement of measurement methodologies and standards in terms of critical dimensions (film thickness, feature sizes, LER, etc.), materials' physical properties (e.g., strain), and electrical properties including interface characteristics (e.g., workfunction, interface states, etc.). Metrology of film stacks for both front-end and back-end generally provide average physical or electrical property behavior from large area test structures. Therefore, new metrology techniques capable of characterizing stack structures at near nominal dimensions are also needed in the near term.

CRITICAL METROLOGY CONSIDERATION—PRECISION AND UNCERTAINTY [METROLOGY]

When comparing measurements with numbers in the roadmap, there are several important considerations. The validity of the comparison is strongly dependent upon how well those comparisons are made. The conventional interpretation of the ITRS precision has been in terms of the single tool reproducibility. The term "precision" is best understood in broader terms as *uncertainty*. Measurement error is a complex function of time (reproducibility), tool (tool-to-tool matching) and sample (sample-to-sample bias variation). The measurement uncertainty is thus defined by the total bias variation with measurement-to-measurement, tool-to-tool, and sample-to-sample components. These components may be of varying importance depending on the instrument and the application.

LITHOGRAPHY METROLOGY [METROLOGY]

Lithography metrology continues to be challenged by rapid advancement of patterning technology. A proper control of the variation in transistor gate length starts with mask metrology. Indeed, larger values for mask error factor (MEF) might require a tighter process control at mask level, too; hence, a more accurate and precise metrology has to be developed. Mask metrology includes measurements that determine that the phase of the light correctly prints. Both on-wafer measurement of critical dimension and overlay are also becoming more challenging. The metrology needs for process control and product disposition continue to drive improvements in precision, relative accuracy, and matching. Acceleration of research and development activities for CD and overlay are essential if to provide viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability which is another important metrology challenge.

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IN THE LONG TERM (~2017 THROUGH 2024)

ENHANCING PERFORMANCE

MANAGEMENT OF LEAKAGE POWER CONSUMPTION [DESIGN]

While power consumption is an urgent challenge, its leakage or static component will become a major industry crisis in the long term, threatening the survival of CMOS technology itself, just as bipolar technology was threatened and eventually disposed of decades ago. Leakage power varies exponentially with key process parameters such as gate length, oxide thickness, and threshold voltage. This presents severe challenges in light of both technology scaling and variability. Off-currents in low-power devices increase by a factor of 10 per generation, and will emphasize a combination of drain and gate leakage components. Therefore design technology must be the key contributor to maintain constant or at least manageable static power.

IMPLEMENTATION OF NON-CLASSICAL CMOS CHANNEL MATERIALS [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND EMERGING RESEARCH DEVICES]

To attain adequate drive current for the highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal velocity and injection at the source end appears to be needed. Eventually, high transport channel materials such as III-V or germanium thin channels on silicon, or even semiconductor nanowires, carbon nanotubes, graphene or others may be needed. Non-classical CMOS devices need to integrate physically or functionally onto a CMOS platform. Such integration requires epitaxial growth of foreign semiconductor on Si substrate which is challenging. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified and addressed early in the technology development

IDENTIFICATION, SELECTION, AND IMPLEMENTATION OF NEW MEMORY STRUCTURES [PROCESS INTEGRATION, DEVICES, AND STRUCTURES AND EMERGING RESEARCH DEVICES]

Line-dense, fast, and low-operating-voltage non-volatile memory will become highly desirable, and ultimate density scaling may require three-dimensional architecture, such as vertically stackable cell arrays in monolithic integration, with acceptable yield and performance. Increasing difficulty is expected in scaling DRAMs, especially scaling down the dielectric equivalent oxide thickness (EOT) and attaining the very low leakage currents and power dissipation that will be required. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies.

SHIFTING FROM TRADITIONAL SCALING TOWARD EQUIVALENT SCALING AND FUNCTIONAL DIVERSITY THROUGH UNCONVENTIONAL APPROACHES [INTERCONNECT]

Line edge roughness, trench depth and profile, via sidewall roughness, etch bias, thinning due to cleaning, CMP effects, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge. Etching, cleaning, and filling high aspect ratio structures, especially low-κ dual damascene metal structures and DRAM at nano-dimensions are also big challenges. Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbates thermo-mechanical effects. Novel/active devices may be incorporated into the interconnect lines. Three-dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets is a key challenge.

RESIST MATERIALS [LITHOGRAPHY]

Limits of chemically amplified resist sensitivity come after 22 nm half pitch due to acid diffusion length. With aggressive scaling of devices, the required gate CD control comes down to 1.5 nm in 3σ with a line width reduction (LWR) of less than 1.4 nm in 3σ in 2016 for every lithography potential solution. (Please note that Si-Si lattice distance is 0.235 nm.) New resist materials with improved dimensional, LWR control and low defect density in less than 10 nm size are necessary. Resist and antireflection coating materials composed of alternatives to PFAS compounds are expected for future ESH concern.

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TRANSITION TO NOVEL STRUCTURES FOR BOTH CMOS AND MEMORY DEVICES [FRONT END PROCESSES]

Several scenarios coexist for keeping continued scaling of CMOS and memory devices. It is anticipated to proceed with scaling (equivalent scaling), by introducing new materials, new structures, and/or 3D integration. Among all, the selection of a fundamental structure for CMOS is very challenging, for example, a channel material and a multi-gate structure will require new process technologies to be concurrently developed. These technologies include starting materials, surface preparation, lithography, pattern etching, and gate stack with booster technique, doping, metrology, process uniformity, and reliability. Once selected, there is no going back. Coordination and discussion are needed in all aspects among ITWGs viewed from process integration and manufacturing. In the memory area, charge-based devices are facing physical limits such as variability and cross-talk. In order to maintain scaling trends in both cost and functionality, innovative technologies will be needed by realizing new data-storage mechanisms or cost-effective 3D integration.

NON-DESTRUCTIVE, PRODUCTION WORTHY WAFER AND MASK-LEVEL MICROSCOPY [METROLOGY]

Non-destructive (without charging or contaminating the surface) and high-resolution wafer/mask level microscopy for measuring the critical dimensions of 3D structures is required. The relationship between the physical object and the waveform analyzed by the instrument should be understood to improve CD measurement including physical feature measurement. Surface charging and contamination need to be improved as well as sensor and sensing method. New design of optics with aberration correction is required for high resolution and better throughput. The combination of high-resolution optics, waveform analysis, and non-charging technique enables precise grasp of 3D structures for CD measurement including sidewall shape and trench structures of damascene process. At the same time, CD metrology tool must be calibrated by using standard reference material or structure for reliable and stable measurement.

SYSTEM-LEVEL DESIGN CAPABILITY TO INTEGRATED CHIPS, PASSIVES, AND SUBSTRATES [ASSEMBLY AND PACKAGING]

Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. Complex standards for information types and management of information quality along with a structure for moving this information will be required. Embedded passives may be integrated into the “bumps” as well as the substrates.

MATERIALS TECHNOLOGIES [EMERGING RESEARCH MATERIALS]

There are many challenges to define, prioritize, and reach consensus to recommend potential solutions that will deliver materials with controlled properties. Furthermore these properties must be defined in sufficient detail to enable ultimately to transfer to the Process and Integrated Device Structures (PIDS) teams in a timely fashion for further pragmatic research and development. These properties must be able to describe the operation of emerging research devices in high density at the necessary nanometer scale of the long-range roadmap timing horizon and beyond. In order to improve control of material properties for high density devices, research on materials synthesis must be coordinated and integrated in parallel with work on new and improved metrology and modeling.

POST-CONVENTIONAL CMOS MANUFACTURING UNCERTAINTY TECHNOLOGIES [FACTORY INTEGRATION]

Uncertainty of novel device types replacing conventional CMOS, and the impact of their manufacturing requirements, will have a big influence on a factory design. Due to the timing uncertainty of the industry to identify and develop new devices, and to create new evolutionary and disruptive process technologies, there is a need to model and design next-generation factories for a wide spectrum of flexibility. Such future factories must have the ability and flexibility to be implemented through early development phases and into production just in time for low risk industry transitions; and also taking into account the potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and with cost efficiency. These are huge industry challenges to simply imagine and define and also for the Factory Integration resources to implement.

COST-EFFECTIVE MANUFACTURING

MODELING OF CHEMICAL, THERMOMECHANICAL, AND ELECTRICAL PROPERTIES OF NEW MATERIALS [MODELING AND SIMULATION]

Computational material science tools need to predict materials synthesis, structure, properties, process options, and operation behavior for new materials applied in devices and interconnects. Especially needed are modeling of: gate stacks; predictive modeling of dielectric constant; bulk polarization charge; surface states; phase change; thermo-

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mechanical (including stress effects on mobility); optical properties; reliability; breakdown; leakage currents (including band structure); and tunneling from process/materials and structure conditions. Novel integration in 3D interconnects needs modeling of airgaps; and data is also needed to model ultrathin material properties, and new ultra-low-κ (ULK) materials (whose models must also able to predict process impact on their inherent properties). Modeling-assisted metrology needs to link between: first principle computation; reduced models (classical MD or thermodynamic computation); and metrology (including ERD and ERM applications). Accumulation of databases for semi-empirical computation is becoming increasingly important.

IN-LINE DEFECT CHARACTERIZATION AND ANALYSIS [YIELD ENHANCEMENT]

Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.

COST CONTROL AND RETURN ON INVESTMENT [LITHOGRAPHY]

Extending lithography to beyond 22 nm half pitch requires the introduction of new lithography technologies such as Extended-Ultraviolet Lithography (EUVL) or new techniques such as multiple patterning. All of these techniques introduce large changes into the single exposure immersion lithography process, targeted presently for the 32 nm Flash Poly uncontacted half-pitch and the 45 nm DRAM contacted M1 half pitch technology cycle. Therefore, achieving constant/improved ratio of exposure-related tool cost to throughput might be an insoluble dilemma. Mask costs are a significant component of lithography costs even up to high mask usage, so development of cost-effective post-optical masks is necessary. Also cost effective lithography systems are expected for the upcoming 450 mm wafer generation manufacturing.

TEST FOR YIELD LEARNING [TEST AND TEST EQUIPMENT]

Test's peripheral role as a feedback loop for understanding underlying defect mechanisms, process marginalities, and as an enabler for rapid fabrication process yield learning and improvement has traditionally been considered a secondary role to screening hard defects. With the increasing reduction in feature (and defect) sizes well below optical wavelengths, rapidly increasing failure analysis throughput times, reduction in failure analysis efficacy, and approaching practical physical limits to other physical techniques (pica, laser probes), the industry is reaching a strategic inflection point for the semiconductor business where the criticality of Design-for-Test (DFT) and test-enabled diagnostics and yield learning becomes paramount. In other words, the yield learning rates of the past process generations are not sustainable by historical fault isolation and failure analysis methods per se. Rather, they need to be augmented by more universal deployment of enabling on-die circuitry (DFT, etc.) across and throughout products, as well as improvements in the on-die instrumentation and diagnostic software tools with respect to fault isolation specificity. Where it may have been sufficient to isolate to failing bit in an array or failing gate in logic in the past, there is a real business need to be able to isolate electrically to at least the failing transistor or interconnect in the future, or suffer the economic consequences of reduced yield improvement learning rates on new process technologies, perhaps even to the point of lowering the asymptotic maximum achievable yields per die size on future processes.

SUSTAINABILITY AND PRODUCT STEWARDSHIP [ESH]

Business considerations and also sustainability metrics (in a cost-effective and timely way) are required for product stewardship. In addition, Design for Environment, Safety, and Health (DFESH) should become an integral part of the facility, equipment, and product design as well as management's decision-making. Environmentally friendly end-of-life reuse/recycle/reclaim of facilities, manufacturing equipment, and industry products are increasingly important to serve both business and ESH needs.

AC POWER SCALING [PROCESS INTEGRATION, DEVICES, AND STRUCTURES]

While the DC power is controlled by I_{off}, off current, the AC power is largely dependent on Vdd, supply voltage. Due to the fact that Vdd cannot be scaled effectively in order to attend adequate drive current for the requirement of speed, the power density and total power continue to climb. Alternate channel materials are required to provide potential solutions.

MEETING THE FLEXIBILITY, EXTENDIBILITY, AND SCALABILITY NEEDS OF A COST-EFFECTIVE, LEADING-EDGE FACTORY [FACTORY INTEGRATION]

Ability to load the fab within manageable range under changeable market demand and to utilize task sharing opportunities such as manufacturing outsourcing is required to keep the manufacturing profitable. Enhanced customer

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visibility for quality assurance of high reliability products including manufacturing outsourcing continues to challenge. Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] promotes reuse of building, production and support equipment, and factory information and control systems across multiple technology generations. Cost and task sharing scheme is highly expected on industry standardization activity for industry infrastructure development such as data standardization and visualization methodology.

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WHAT IS NEW FOR 2009— THE WORKING GROUP SUMMARIES

SYSTEM DRIVERS

In 2009 the System Drivers teams made the following updates to the System Drivers chapter:

- Updated in detail the SoC Consumer drivers to indicate the reasoning and detail of the updates in the section itself, relevant to key parameters such as power consumption.
- Other updates have been also included as necessary maintenance and evolution.

Table ITWG1 Major Product Market Segments and Impact on System Drivers

Market Drivers	*SOC*	*Analog/MS*	*MPU*
I. Portable/consumer			
1. Size/weight ratio: peak in 2004 2. Battery life: peak in 2004 3. Function: 2×/2 years 4. Time-to-market: ASAP	Low power paramount Need SOC integration (DSP, MPU, I/O cores, etc.)	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
II. Medical			
1. Cost: slight downward pressure (~1/2 every 5 years) 2. Time-to-market: >12 months 3. Function: new on-chip functions 4. Form factor often not important 5. Durability/safety 6. Conservation/ ecology	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SOC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
III. Networking and communications			
1. Bandwidth: 4×/3–4 years 2. Reliability 3. Time-to-market: ASAP 4. Power: W/m^3 of system	Large gate counts High reliability More reprogrammability to accommodate custom functions	Migrating on-chip for MUX/DEMUX circuitry MEMS for optical switching.	MPU cores, FPGA cores and some specialized functions

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Table ITWG1 Major Product Market Segments and Impact on System Drivers (continued)

IV. Defense			
1. Cost: not prime concern 2. Time-to-market: >12 months 3. Function: mostly on SW to ride technology curve 4. Form factor may be important 5. High durability/safety	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
V. Office			
1. Speed: 2×/2 years 2. Memory density: 2×/2 years 3. Power: flat to decreasing, driven by cost and W/m^3 4. Form factor: shrinking size 5. Reliability	Large gate counts; high speed Drives demand for digital functionality Primarily SOC integration of custom off-the-shelf MPU and I/O cores	Minimal on-chip analog; simple A/D and D/A Video i/f for automated camera monitoring, video conferencing Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-position resolution	MPU cores and some specialized functions Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
VI. Automotive			
1. Functionality 2. Ruggedness (external environment, noise) 3. Reliability and safety 4. Cost	Mainly entertainment systems Mainly ASSP, but increasing SOC for high end using standard HW platforms with RTOS kernel, embedded software	Cost-driven on-chip A/D and D/A for sensor and actuators Signal processing shifting to DSP for voice, visual Physical measurement ("communicating sensors" for proximity, motion, positioning); MEMS for sensors	

A/D—analog to digital ASSP—application-specific standard product D/A—digital to analog DEMUX—demultiplexer DSP—digital signal processing FPGA—field programmable gate array i/f—interface I/O—input/output HW—hardware MEMS—microelectromechanical systems MUX—multiplexer RTOS—real-time operating system

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DESIGN

In 2009 the Design teams made the following updates to the Design TWG chapter:

- Started a resilience / reliability roadmap. We have consequently added text to (a) crosscutting challenges (b) DFM section (c) other scattered spots elsewhere in the Design Chapter – for this new topic, attached to reliability.
- Updated crosscut text from Modeling and Simulation
- Overhauled the DFT section, thanks to a collaboration from our colleagues in the Test chapter. There is a new DFT challenges table (see spreadsheets). We have deleted DFT solutions table. There is new DFT section text.
- Updated the ORTC power consumption challenge.
- Extended all key tables and figures until the 2024 year, consistent with the rest of the 2009 roadmap.
- Added requirements (rows) in the system level section tables to indicate the impact of system level design versus lower level design, on power reduction.

Table ITWG2 Overall Design Technology Challenges

Challenges ≥ 32 nm	*Summary of Issues*
Design productivity	System level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation Verification: executable specification, ESL formal verification, intelligent test bench, coverage-based verification Logic/circuit/layout: analog circuit synthesis, multi-objective optimization
Power consumption	Logic/circuit/layout: dynamic and static (leakage), system and circuit, power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Reliability	Logic/circuit/layout: MTTF-aware design, BISR, soft-error correction
Interference	Logic/circuit/layout: signal integrity analysis, EMI analysis, thermal analysis
Challenges <32 nm	*Summary of Issues*
Design productivity	Complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage Tools specific for SOI and non-static logic, and emerging devices Cost-driven design flow Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	SOI power management
Manufacturability	Uncontrollable threshold voltage variability Advanced analog/mixed signal DFT (digital, structural, radio), "statistical" and yield-improvement DFT Thermal BIST, system-level BIST
Reliability	Autonomic computing, robust design, SW reliability
Interference	Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.)

ATE—automatic test equipment BISR—built-in self repair BIST—built-in self test DFT—design for test
EMI—electromagnetic interference ESL—Electronic System-level Design HW/SW—hardware/software
MTTF—mean time to failure SOI—silicon on insulator

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TEST AND TEST EQUIPMENT

The 2009 edition of the Test Roadmap contains some significant changes to many of the tables; includes a new section on Adaptive Test; includes some discussion of 3D silicon devices; and added accelerometers to the Specialty Devices section. A survey on Cost of Test was completed in 2009 and the results are included in the Cost of Test Focus topic section. The high speed interfaces section was heavily updated. Other sections of the chapter contain only minor revisions.

Adaptive test has been being adopted as a method to reduce overall product test cost and improve product yields. The Test chapter now devotes an entire section to adaptive test concepts, challenges, impact to engineering and factory methodology, IT infrastructure requirements; and some implementation examples.

3D (Three Dimensional) silicon devices have been added to the key drivers for 2009. The concept of 3D devices is that a single design is implemented across multiple die connected by TSVs (Thru Silicon Vias) in order to optimize the cost and performance of devices. The SoC methodology of integrating a very complex system on a single chip can require many mask layers to be added to a technology to accommodate the requirements of the SoC. The 3D concept allows each die domain to be process optimized (i.e. Logic, DRAM, NVM, Analog), but introduces design and test complexities.

The test parallelism table has remained controversial even though new device categories have been added since 2005, so typical functional pin count assumptions have been added as notes. However, as many devices are being tested at wafer probe using reduce pin interfaces; all possible parallelisms cannot be included in the table.

The SoC table has been revised to reflect the latest trends and the chapter section has been appropriately changed. Formulas based changes in the Logic Table reflect the impact of the 2009 MPU and Consumer transistor count changes in the ORTC tables. Memory changes were also driven by the 2009 ORTC density roadmap.

Carrier frequency range in the RF table has been broken into general and special radio categories and the rapid increase in modulation bandwidth required for technologies such as UWB has moved out in time. The remainder of the table reflects small changes in numeric values and some cell color changes.

Prober, probecard, Handlers and test socket tables have had significant changes. The prober table has had a near complete rewrite, so changes are not easily summarized. Probecards now reflect a special LCD display driver probe requirements section to specify the unique challenges of testing these devices. Handlers broke the high power (>10W) device requirements into a med-hi (10-50W) range and a high range (>50W). Test sockets now covers blade rubber contacts and also included a table showing socket self-inductance must be reduced below 0.3nH to properly support 6GHz; and below 0.1nH for support of 20GHz signals.

There were either no changes, or only cell color changes or small numerical changes to the Vector multiplier, Mixed Signal, Burn-in and Probing difficult challenges tables.

2010 DIRECTIONS

Only tables will be updated for the 2010 roadmap, but the team will be preparing for the 2011 update which will include high speed test challenges, DFT enhancements and an update to the SoC and 3D device sections.

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KEY TEST DRIVERS, DIFFICULT CHALLENGES, AND OPPORTUNITIES

Table ITWG3 Summary of Key Test Drivers, Challenges, and Opportunities

Key Drivers (not in any particular order)	
Device trends	Increasing device interface bandwidth (# of signals and data rates) Increasing device integration (SoC, SiP, MCP, 3D packaging) Integration of emerging and non-digital CMOS technologies Complex package electrical and mechanical characteristics Device characteristics beyond one sided stimulus/response model 3 Dimensional silicon - multi-die and Multi-layer Multiple I/O types and power supplies on same device
Increasing test process complexity	Device customization during the test process "Distributed test" to maintain cost scaling Feedback data for tuning manufacturing Dynamic test flows via "Adaptive Test" Higher order dimensionality of test conditions
Continued economic scaling of test	Physical limits of test parallelism Managing (logic) test data and feedback data volume Defining an effective limit for performance difference for HVM ATE versus DUT Managing interface hardware and (test) socket costs Trade-off between the cost of test and the cost of quality Multiple insertions due to system test and BIST
Difficult Challenges (in order of priority)	
Test for yield learning	Critically essential for fab process and device learning below optical device dimensions
Detecting Systemic Defects	Testing for local non-uniformities, not just hard defects Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects
Screening for reliability	Implementation challenges and efficacies of burn-in, IDDQ, and Vstress Erratic, non deterministic, and intermittent device behavior
Potential yield losses	Tester inaccuracies (timing, voltage, current, temperature control, etc) Over testing (e.g., delay faults on non-functional paths) Mechanical damage during the testing process Defects in test-only circuitry or spec failures in a test mode e.g., BIST, power, noise Some IDDQ-only failures Faulty repairs of normally repairable circuits Decisions made on overly aggressive statistical post-processing
Future Opportunities (not in any order)	
Test program automation (not ATPG)	Automation of generation of entire test programs for ATE
Simulation and modeling	Seamless Integration of simulation and modeling of test interface hardware and instrumentation into the device design process
Convergence of test and system reliability solutions	Re-use and fungibility of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMs—micro-electromechanical systems

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PROCESS INTEGRATION, DEVICES, AND STRUCTURES

PIDS has three main sections: Logic, Memory (DRAM and Non-Volatile Memory), and Reliability. Major changes are listed under each section heading below.

LOGIC

- Recent surveys and literature indicate that the gate-length scaling has been/will be less aggressive than the past roadmap predictions. Realignment for this effect was the major change in the ITRS 2008 Edition. Reiterating that change in 2008 in comparison to that in 2007, the physical gate length L_g scaling for HP logic is slowed down by three to five years, with a change of slope. It is also observed that with the new L_g scaling model, the *CV/I* speed metric has a slope of ~13% increase per year instead of 17%. Similar changes were made to LOP technology whose physical gate length had a slow-down of one to three years, also with a change of slope. In this 2009 Edition, a minor adjustment of one-year slow-down is made compared to the 2008 Edition for most logic devices.
- Ring oscillator delay is added besides *CV/I* as a more realistic speed metric. Both fan-out of 1 and fan-out of 4 are included.
- In order to simulate a CMOS inverter in a ring oscillator, the saturation current of *p*-channel MOSFET is added. All other parameters are assumed symmetric to those of *n*-channel MOSFET.
- The subthreshold source-drain leakage currents are held constant independent of years. The values used for HP, LOP, and LSTP are 100 nA/μm, 5 nA/μm, and 50 pA/μm respectively.
- The criterion for source/drain parasitic resistance is set for degradation of 33% (1/3) of saturation current compared to an idealized case without any series resistance.

MEMORY: DRAM

- Smaller cell size of $4F^2$ is introduced, starting in 2011.
- Total bit size per chip is shifted later by 1 year.

MEMORY: NON-VOLATILE MEMORY (NVM)

- Transition from floating-gate type to charge-trapping type is delayed by 2 years, to 2012.
- 3-D charge-trapping flash is delayed by 1 year to 2014.
- Transition from 3-bit/cell to 4-bit/cell is delayed by 2 years, to 2012.
- NAND flash half-pitch is pulled-in by 1 year.
- Spin-torque-transfer MRAM table is added.

RELIABILITY

- Major correction in the reliability requirement specifications.
- Increase emphasis on circuit impact of device reliability issues. Bring up the need for paradigm change and the challenges involved.

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DIFFICULT CHALLENGES

Table ITWG3 Process Integration Difficult Challenges.

Difficult Challenges for $L_g \geq 16$ nm	*Summary of Issues*
1. Scaling of logic MOSFETs	Scaling planar bulk CMOS Implementation of fully depleted SOI and multi-gate (MG) structures Controlling source/drain series resistance within tolerable limits Further scaling of EOT with higher κ materials (κ > 30) Threshold voltage tuning and control with metal gate and high-κ stack Inducing adequate strain
2. Scaling of DRAM and SRAM	DRAM— Adequate storage capacitance with reduced feature size; implementing high-κ dielectric Low leakage in access transistor and storage capacitor Low resistance for bit and word lines to ensure desired speed Improve bit density and to lower production cost in driving toward $4F^2$ cell size SRAM— Maintain adequate noise margin and control key instabilities and soft-error rate Difficult lithography and etch issues
3. Scaling high-density non-volatile memory	Endurance, noise margin, and reliability requirements Non-scalability of tunnel dielectric and interpoly dielectric in flash Difficult lithography and etch issues with pitch scaling Maintain high gate coupling ratio in floating-gate flash
4. Reliability due to material, process, and structural changes	Threshold voltage shifts due to traps, carrier injection, and program/erase cycling in memory cells Mobility degradation due to mechanical stress relaxation or interface states New or changed failure mechanisms resulting from high-κ/metal gate and new doping/activation processes New failure mechanism resulting from fundamental length scales or new device structures Process variability
Difficult Challenges for $L_g < 16$ nm	*Summary of Issues*
1. Implementation of advanced non-classical CMOS structures	Advanced non-planar multi-gate MOSFETs below 10 nm gate length Control of short-channel effects Drain engineering to control parasitic resistance Strain enhanced thermal velocity and quasi-ballistic transport
2. Implementation of non-classical CMOS channel materials	Identification and demonstration of alternate channel materials New issues from materials, devices, and processing Integration of alternate channel materials on Si platform
3. Identification and implementation of new memory structures	Density and voltage scaling of NVM 3-D integration of NVM Implementing non-charge-storage type of NVM Scaling storage capacitor for DRAM DRAM and SRAM replacement solutions
4. Reliability of novel devices, structures, materials, and applications	Reliability characterization of new devices Dealing with fluctuations and statistical process variations Impact of microscopic physical effects Need for Design for Reliability tools
5. Power scaling	V_{dd} scaling Controlling subthreshold current
6. Beyond CMOS	Identification and implementation of non-CMOS devices and architectures Integration onto Si-CMOS platform See ERD and ERM chapters for more discussions and details

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RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

OVERVIEW

- Micro-electro-mechanical systems (MEMS) now are treated in a separate technology section of the RF and AMS roadmap. In 2007, they were part of the More-than-Moore Section
- 3-D integration trends are affecting many RF and AMS technologies.

RF AND AMS CMOS

- Many product families skip nodes entirely when migrating to new application versions.
- Power-management and analog are being supported by optional devices since perhaps the 90 nm node.
- Millimeter-wave CMOS technologies are now discussed in the mm-wave section

RF AND AMS BIPOLAR DEVICES

- High-speed (HS) HBTs underwent a major update for the 2009 RFAMS roadmap to reflect higher f_{MAX} / f_T ratios.
- High-voltage (HV) HBTs were removed from the table for this section
- High-speed (HS) PNP transistors are now included in this section.
- Power-amplifier (PA) HBTs were update to anticipate changes in battery-voltages.

ON-CHIP AND OFF-CHIP PASSIVES FOR RF AND AMS

- On-chip: 3D integrated circuits enable improved performance of passive devices.
- Off-chip: The section now includes inorganic substrate roadmaps to reflect 3D integration and passives-only integration.

POWER AMPLIFIERS (0.4 GHZ–10 GHZ)

- This section addresses four major trends in handsets - 1) Drive to lower end-of-life battery voltage, 2) More complex biasing schemes, 3) Low-cost markets driving CMOS Pas, and 4) Growing number of modes supported by PA modules.
- It also addresses two major trends in basestations – 1) Due to the increasing use of GaN, discussions on GaAs were removed from the section and 2) The use of very-efficient architectures is increasing.

MILLIMETER WAVE (10 GHZ–100 GHZ)

- The parameter for maximum current (Imax) was removed as a technical requirement in the tables for low noise devices.
- Maximum available gain] (MAG) predictions at 60 and 94 GHz were added to the SiGe HBT and CMOS tables.
- The prediction for the production of mm-wave GaN power HMETs was delayed to 2010.

MEMS

- The roadmap for 2009 now includes bulk acoustic wave (BAW) devices, resonators, and both metal-contact and capacitive-contact switches.
- The roadmap acknowledges other emerging MEMS devices such as gyroscopes, accelerometers, microphones, and displays and growing interests in sub-THz applications.
- There remain needs to develop appropriate quantitative metrics in tables such as insertion loss and tuning ratio for capacitive-contact switches and other key metrics per device or area.

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DIFFICULT CHALLENGES

Table ITWG4 RF and Analog Mixed-Signal (RF and AMS) Technologies for Wireless Communications Difficult Challenges

Difficult Challenges	*Summary of Issues*
CMOS	New materials (e.g., high-permittivity gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes) make predicting trends uncertain for transistor mismatch and for 1/f noise.
Bipolar HS-NPNs and HS-PNPs transisters	Increasing f_T by more aggressive vertical profiles and still maintaining acceptable figures of merit, manufacturing control, and punch-through margins
Bipolar Power Amplifiers	Improving the trade-off between f_T/f_{MAX} and breakdown voltages to provide acceptable voltage handling and power densities at performance levels that can effectively complete with alternative technologies.
On-Chip Passive Devices	Integrating new materials in a cost-effective manner to realize compact and high quality factor (Q) inductors and high-density metal-insulator-metal (MIM) capacitors demanded by the roadmap for increased RF performance.
Off-Chip Passive Devices	The large number of options for embedded passives increases complexity and cost. And accurate models for process tolerance and parasitic effects and computer assisted design (CAD) tools.
Handset Power Amplifiers	Increasing functionality in terms of operating frequency and modulation schemes and simultaneously meeting increasingly stringent linearity requirements at the same or lower cost.
Base-station Power Amplifiers	Enhancing performance with continual product-price pressure. And Improving amplifier efficiency.
mm-Wave Devices	Thermal management for high power density circuits, multi-level integration and E/D mode transistors. And reduction of leakage current and understanding of failure mechanisms, particularly for GaN materials which are piezoelectric in nature.
MEMS	Incorporating the great process diversity of MEMS into specific ITRS processes. And developing design tools, packaging, performance drivers, and cost drivers for each MEMS device type.

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EMERGING RESEARCH DEVICES

The 2009 edition of the Emerging Research Devices chapter evaluates emerging research logic and memory devices, proposed for two different scenarios, complemented by a re-directed section discussing architectural opportunities. One scenario addresses charge-based devices and technologies for extending CMOS scaling to the end of the Roadmap. The other explores "Beyond CMOS" devices for complementing and enhancing CMOS by, for example, performing synergistic accelerator functions in the nearer term, and, eventually, for supplementing CMOS in a new information processing paradigm. For example, research on MOSFETs employing an alternate channel material (Ge or III-V Compound Semiconductor) has made substantial progress in the past two years and is beginning to show significant potential for sustaining performance scaling of CMOS to the end of the Roadmap. Similarly, a "Beyond CMOS" device could potentially use particle spin to perform non-volatile memory and logic functions on a CMOS chip, or could perform an information processing function utilizing spin waves.

Connecting these two scenarios, the 2009 ERD chapter features a particular emerging research information processing technology, carbon-based nanoelectronics, which exhibits high potential and is maturing rapidly. Carbon-based nanoelectronics, including carbon nanotubes, graphene, and graphene nanoribbons, was chosen because of its potential performance advantages when applied to MOSFETs and the rich physics it enables for realizing a new information processing device.

Several new research technologies are emerging for non-volatile random access memories offering potential for dense, high speed and lower power memory devices. Operation of most of these technologies is based on employing a resistive element for storing binary data. Leading candidates include the Spin Transfer Torque RAM, the Nanothermal RAM (i.e., PCM and Fuse/Antifuse), and the Nanoionic RAM (i.e., Atomic Switch and Memristor). Of particular interest are those technologies capable of being scaled to and beyond the 16 nm generation. Two other memory technologies, Nanocrystal Memory and Engineered Tunnel Barrier Memory, tracked and evaluated by ERD through several previous editions, have reached sufficient potential and maturity to be transferred to PIDS and FEP for their treatment in 2009.

The Architecture section has been re-directed and expanded to include new activities for benchmarking emerging research logic and information processing devices, a new memory architecture section, a new example of processing using a Bayesian inference network, and a new analysis of limits. These are summarized below:

1. Benchmarking— The Nanoelectronics Research Initiative (NRI) has begun developing a new methodology for benchmarking the performance of nineteen alternative information processing devices on both Boolean and special purpose logic operations. The Boolean logic operations are parameterized in terms of energy and delay for three selected logic gates. These methods are currently being further developed and applied to compare disparate device technologies. Results of this benchmarking analysis are planned for publication when available, tentatively next year.
2. Memory Architecture is discussed in the context of using new memory technologies to reduce the substantial energy dissipation inherent in current memory technologies
3. An example of a Bayesian inference network is discussed to illustrate the potential of merging one or more Beyond CMOS devices with a completely new architecture to extend information processing into scaling, power, and performance domains beyond that attainable by ultimately scaled, end-of-the-roadmap CMOS.
4. A new thermodynamic analysis of limits is outlined in which the physics of an emerging research device in the Boltzmann-Heisenberg limit is connected to the parameters of digital circuits implemented using these devices. The proposed methodology should be extensible to estimate the optimal achievable performance for information processors implemented in that technology.

DIFFICULT CHALLENGES

Difficult challenges related to emerging research devices, as shown in the table below, are divided into those related to memory technologies and those related to information processing or logic devices. One challenge is the need of a new memory technology that combines the best features of current memories in a fabrication technology compatible with CMOS process flow scaled to and beyond the present limits of SRAM and FLASH, 22–16 nm. A related challenge is to sustain scaling of CMOS logic technology beyond 16 nm.

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Table ITWG5 Emerging Research Devices Difficult Challenges

Difficult Challenges ≥ 16 nm and < 16 nm	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile and non-volatile memory technologies to and beyond the 16 nm technology generation.	SRAM and FLASH scaling will reach definite limits within the next several years (see PIDS Difficult Challenges). These are driving the need for new memory technologies to replace SRAM and FLASH memories. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in the technology development
Scale CMOS to and beyond the 16 nm technology generation.	Develop new materials to replace silicon as an alternate channel and source/drain to increase the saturation velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation for technology scaled to 16 nm and beyond. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in t
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and a primitive-level architecture to provide special purpose optimized functional cores heterogeneously integrable with silicon CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and develop a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. Bridge a knowledge gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in the technology development

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EMERGING RESEARCH MATERIALS

The 2009 Emerging Research Materials (ERM) chapter is an updated version of the 2007 ITRS ERM. The 2009 ERM Chapter has been reorganized to review material for specific applications, while the 2007 ERM reviewed materials and discussed their potential applications to future roadmap needs. The 2009 ERM reviews materials for ERD Logic and Memory applications, lithography including novel resist, front end process and process integration and devices applications, interconnects, and assembly and package applications. The ERM chapter also identifies metrology, modeling, and environmental safety and health research needed to support these materials for their potential applications. While these ERMs have properties that make them attractive as potential solutions to future technology needs, significant progress is required for them to be adopted in future technologies.

In addition to restructuring the ERM to focus on applications, several new applications and materials are included. Materials for Emerging Research Devices includes materials for Logic including "Alternate Channel Materials (that includes a critical assessment of Ge, III-V, graphene, carbon nanotubes, and nanowires), "Materials for Charge Based Beyond CMOS Devices," and "Materials for Noncharge based Beyond CMOS," and a new section on Materials for Memory. Lithography Materials has been expanded beyond Materials for Directed Self Assembly" to also include a materials for non-evolutionary 193 nm and EUV resist materials including non chemically amplified resist (Non-CAR), negative tone resist, materials for pitch division, novel EUV approaches including negative tone cationic, negative tone Non-CAR, inorganic-organic hybrids, and other Non CAR materials. Materials and Processes for Front End Processes reviews a number of technologies for deterministic dopant placement and directed self assembly materials for selective etch, clean and deposition processes. Interconnect materials now includes a review of potential ultrathin Cu barrier layers and low κ ILD materials to extend Cu interconnects, as well as single wall and Multiwalled carbon nanotubes and single crystal nanowires for via and interconnect replacements. Assembly and Package Materials reviews nanometals for low temperature solders and anisotropically conducting interconnect materials, carbon nanotubes for high current chip to package interconnects, and the use of nanoparticles and macromolecules to deliver package polymers to meet the multiple conflicting properties required for application to underfill, mold compound, and multiple adhesive applications.

The ERM and ERD chapters also highlight the need for an increased focus on carbon based (i.e. carbon nanotubes and graphene) electronics for potential application as alternate channel materials and for potential application to Beyond CMOS applications, based on an assessment of Beyond CMOS technologies.

DIFFICULT CHALLENGES

The current set of sub-16 nm ERM Difficult Research Challenges is summarized in Table ITWG6. Perhaps ERM's most difficult challenge continues to be delivering material options, with controlled and desired properties, in time to impact insertion decisions. These material options must exhibit the potential to enable high density emerging research devices, lithographic technologies, and interconnect fabrication and operation at the sub 20 nanometer scale and be extensible to nanometer scale. This challenge, to improve the control of material properties for nanometer (nm) scale applications, requires collaboration and coordination within the research community. Accelerated synthesis, metrology, and modeling initiatives are needed to enhance targeted material-by-design capabilities and enable viable emerging material technologies. Improved metrology and modeling tools also are needed to guide the evolution of robust synthetic methods for these emerging nanomaterials. The success of many ERMs depend on robust synthetic methods that yield useful nanostructures, with the required control of composition, morphology, an integrated set of application specific properties, and compatibility with manufacturable technologies.

To achieve high density devices and interconnects, ERMs must assemble in precise locations, with controlled orientations. Another critical ERM factor for improving emerging device, interconnect, and package technologies is the ability to characterize and control embedded interface properties. As features approach the nanometer scale, fundamental thermodynamic stability considerations and fluctuations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties.

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Table ITWG6 Emerging Research Material Technologies Difficult Challenges

Difficult Challenges ≤16 nm	*Summary of Issues*
Integration of alternate channel materials with high performance	III-V has high electron mobility, but low hole mobility
	Germanium has high hole mobility, but electron mobility is not as high as III-V materials
	Demonstration of high mobility n and p channel alternate channel materials co-integrated with high κ dielectric
	Demonstration of high mobility n and p channel carbon (graphene or carbon nanotubes) FETs with high on-off ratio co-integrated with high κ dielectric and low resistance contacts
	Selective growth of alternate channel materials in desired locations with controlled properties and directions on silicon wafers (III-V, Graphene, Carbon nanotubes and semiconductor nanowires)
	Achieving low contact resistance to sub 16 nm scale structures (graphene and carbon nanotubes)
	Ge dopant thermal activation is much higher than III-V process temperatures
	Growth of high κ dielectrics with unpinned Fermi Level in the alternate channel material
Control of nanostructures and properties	Ability to pattern sub 16 nm structures in resist or other manufacturing related patterning materials (resist, imprint, self assembled materials, etc.)
	Control of CNT properties, bandgap distribution and metallic fraction
	Control of stoichiometry, disorder and vacancy composition in complex metal oxides
	Control and identification of nanoscale phase segregation in spin materials
	Control of surfaces and interfaces
	Control of growth and heterointerface strain
	Control of interface properties (e.g., electromigration)
	Ability to predict nanocomposite properties based on a "rule of mixtures"
	Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability
Controlled assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components
	Control of line width of self-assembled patterning materials
	Control of registration and defects in self-assembled materials
Characterization of nanostructure-property correlations	Correlation of the interface structure, electronic and spin properties at interfaces with low-dimensional materials
	Characterization of low atomic weight structures and defects (e.g., carbon nanotubes, graphitic structures, etc.)
	Characterization of spin concentration in materials
	Characterization of vacancy concentration and its effect on the properties of complex oxides
	3D molecular and nanomaterial structure property correlation
Characterization of properties of embedded interfaces and matrices	Characterization of the roles of vacancies and hydrogen at the interface of complex oxides and the relation to properties
	Characterization of transport of spin polarized electrons across interfaces
	Characterization of the structure and electrical interface states in complex oxides
	Characterization of the electrical contacts of embedded molecule(s)
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures
	Device structure-related properties, such as ferromagnetic spin and defects
	Dopant location and device variability

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FRONT END PROCESSES

In 2009, the FEP chapter has been restructured. The 2009 FEP chapter now starts with device-related Technology Requirements (logic devices, including high performance, low operating power, and low stand-by power; memory devices, including DRAM, flash, phase-change, and FeRAM) followed by the material and process Technology Requirements (starting materials; surface preparation; thermal/thin films/doping; plasma etch; and CMP). After studying current industry practice, and in consultation with ORTC, PIDS, Design, and other Technology Working Groups, the scaling rate of the logic physical gate length was further delayed by one-year, compared to the 2008 update.

Material-limited device scaling has placed new demands on virtually every front end material and unit process, starting with the silicon wafer substrate and encompassing the fundamental planar CMOS building blocks and memory storage structures. Continued scaling of planar bulk CMOS is becoming more and more difficult. As a consequence we must be prepared for the emergence of CMOS technology that uses non-conventional MOSFETs or alternatives such as planar FDSOI devices and dual- or multi-gate devices either in a planar of vertical geometry. An overview of the device alternatives is presented in the *Emerging Research Devices chapter*. Projections for the manufacturing introduction of non-conventional MOSFET devices are 2013–2015 for FDSOI and/or multi-gate. The challenges associated with integration of these diverse new materials and structures are the central theme of the FEP difficult challenges.

High-κ gate dielectric with metal gate electrode is in production. Continued scaling of equivalent oxide thickness (EOT) below 0.8 nm while preserving electrical performance and reliability, will be a challenge. Continued improvement in strain engineering and application to new device structures is identified as an FEP difficult challenge. The introduction of new materials is also expected to impose added challenges to the methods used to dope and activate silicon. Series resistance is critical in the near term and needs to be addressed to achieve the goals through 2015.

In the memory area, stand-alone DRAM device manufacturing has narrowed to the stacked capacitor approach. Therefore, the Technology Requirements table and text for DRAM trench capacitor has been removed. A new requirements table has been added to address charge-trapping Flash technology scaling. FeRAM will make a significant commercial appearance where ferroelectric and ferromagnetic storage materials would be used. In addition, phase-change memory (PCM) devices are expected to make a commercial appearance by 2010.

In starting materials, it is expected that alternatives to bulk silicon such as silicon-on-insulator substrates will proliferate. An important difficult challenge expected to emerge within this 2009 Roadmap horizon is the need for the next generation 450 mm silicon substrate. Based upon historical diameter change cycles, the industry is already several years behind the pace necessary to allow the next generation 450 mm silicon substrate to be ready for device manufacture in the year 2014.

Front end cleaning processes will continue to be impacted by the introduction of new front end materials such as high-κ dielectrics, metal gate electrodes, and mobility-enhanced channel materials. Scaled devices are expected to become increasingly shallow, requiring that cleaning processes become completely benign in terms of substrate material removal and surface roughening. Scaled and new device structures will also become increasingly fragile, limiting the physical aggressiveness of the cleaning processes that may be employed.

The persistent challenge in scaling device sizes is the control of gate length critical dimensions (CD). As gate CD shrinks, the presence of line width roughness (LWR) is becoming the biggest portion of CD variation at 28 nm technology node and beyond. The LWR is at best staying constant as the line width shrinks, which makes it a major scaling concern. Current methods of quantification need to be standardized to allow the industry to address the problem. As non-planar transistors become necessary, etch becomes much more challenging. FinFET configurations bring new constraints to selectivity, anisotropy, and damage control.

Chemical-Mechanical Planarization (CMP) is becoming more important for Front End Processing and is being given specific consideration in the 2009 FEP Chapter for the first time. Uniformity, selectivity, and pattern density dependency continue to be challenges for CMP processes.

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DIFFICULT CHALLENGES

Table ITWG7 Front End Processes Difficult Challenges

Difficult Challenges ≥ 16 nm (Metal 1 1/2-pitch)	*Summary of Issues*
	Strain Engineering - continued improvement for increasing device performance - application to FDSOI and Multi-gate technologies
	Achieving DRAM cell capacitance with dimensional scaling - finding robust dielectric with dielectric constant of ~60 - finding electrode material with high work function
	Achieving clean surfaces free of killer defects - with no pattern damage - with low material loss (<0.2 A)
	High-k/Metal Gate - introduction to full scale manufacturing for HP, LOP, and LSTP - scaling equivalent oxide thickness (EOT) below 0.8 nm
	450 mm wafers - meeting production level quality and quantity
Difficult Challenges < 16 nm (Metal 1 1/2-pitch)	*Summary of Issues*
	Continued scaling of HP multigate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation.
	Lowering required DRAM capacitance by 4F2 cell scheme or like, while continuing to address materials challenges
	Continued achievement of clean surfaces while eliminating material loss and surface damage and sub-critical dimension particle defects
	Continued EOT scaling below 0.7 nm with appropriate metal gates
	Continued charge retention with dimensional scaling and introduction of new non-charged based NVM technologies

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LITHOGRAPHY

It is becoming increasingly more difficult to extend optical lithography as we know it today. In 2010, flash devices will be manufactured using 32 nm half-pitch (hp) double patterning (DP) as a way of extending the half-pitch while keeping the NA and wavelength constant. This approach will be pushed harder as DRAM and MPU drive down to the 32 nm hp and flash starts to test the limits of optical solutions at the 22 nm half-pitch node in 2013. But it is at this point that an alternative next generation lithography (NGL) must be introduced into manufacturing to ensure a smooth transition into the lithography approaches beyond 22 nm.

At the 22 nm node, the international community that contributes to the ITRS saw four possible technologies that could be used and that could extend the roadmap out to 11 nm half-pitch. These were all ranked at each year for their desirability and feasibility as solutions. EUV lithography is the lead candidate because of its lower cost of ownership (COO). Second is extending 193 immersion double patterning down to a k1 of 0.15 for the 22 nm half-pitch node, followed by maskless lithography (ML2) and imprint lithography. Alpha and soon beta tools are being delivered to the semiconductor industry for evaluation and further development using all of these approaches. In many cases, the technology is not limited by the lithography tool, but rather by the supporting technologies.

DIFFICULT CHALLENGES < 22 NM VERSUS TECHNOLOGY

The difficult challenges moving into the NGL regime are many and are not just incremental improvements in the technologies that we know and understand. The technology options are still vast, and in many cases the technology and the supporting infrastructure technologies need significant inventions to approach the manufacturing stage. The Difficult challenges table for ≤22 nm shows the major challenges that must be solved to bring NGL technologies to the manufacturing stage. These challenges are listed in the order of perceived difficulty. For EUV lithography, three major components have long been flagged as needing substantial improvements. First is EUV source brightness/reliability. The leading contender for a bright EUV source has changed from discharge produced plasma (DPP) to laser produced plasma (LPP) in recent years, but the sustained proven power levels are still about 4 to 6× less than the power that is needed for manufacturing. The second is the EUVL resist system since specifications for resolution, linewidth roughness (LWR), and sensitivity must be achieved simultaneously at a low exposure dose. Additionally, each photon of EUV radiation has 15× more energy than a 193 photon. Thus the dose for exposure is achieved by 15× fewer photons, putting the image closer to the quantum noise limits. The third issue involves the EUV mask and the infrastructure that is needed to support it. A printing defect on this mask can derive not only from the traditional opaque defect in the patterning layer but also from small phase defects on the EUV substrate or a phase defect generated in the multilayer of the reflective blank. These phase defects are at the limits of today's metrologies and as such are very difficult to observe and improve upon. Currently, the infrastructure inspection equipment (substrate, blank, patterned mask, AIMs) needed for EUV mask manufacturing at the 22 nm node does not exist.

Maskless lithography is another NGL technology that must overcome major challenges before being considered a manufacturing technology. Foremost is the system throughput combined with the resist sensitivity that will also provide adequate LWR and resolution. This is both a system issue with respect to the e-beam flux and a resist material issue. The second most pressing concern is the inability to inspect wafer images at the same capability that we now have for 4× mask patterns. Inspection involves two issues: the resolution of the wafer inspection (at sufficient speed) and die-to-database inspection to ensure no systematic recurring defects are present.

Imprint lithography has three major needs: 1× masks, imprint materials, and imprint systems. The 1× mask has many areas contributing to difficult obstacles. First is mask inspection. The mask must be inspected to find defects in the 1× pattern that are just 10% of the width of the feature. An e-beam system might be able to do this but not at the speeds needed for manufacturing. Second is the write time to expose the slower speed e-beam resists to meet the LWR and CD specifications for 1× patterning. Third, 1× defect sizes are 4× smaller than what current 4× optical mask processes require; therefore, imprint template and e-beam resist patterning processes need to be developed to match these specifications. Another challenge is that the imprint materials must be of sufficiently low viscosity to be applied quickly for sufficient throughput. The last major challenge is with the imprint system. The lithography community believes that throughput, defect levels, and overlay all need a significant overhaul for the technology to be accepted in manufacturing.

Although there are many near-term challenges, the industry is addressing them. Lithographic systems are being made to run at throughputs that are about 2× the throughput of older steppers, thus addressing some of the COO issues associated with double patterning. Registration and overlay issues with lithographic mask patterning systems are also being

addressed to move double patterning into manufacturing. The industry is likewise addressing the fundamental challenges associated with the NGL technologies, in particular the EUV lithography and the mask infrastructure that is needed. With these gains, the lithography industry will be back on course for improving ROI into the future.

Table ITWG8A Lithography Difficult Challenges >22 nm

Difficult Challenges > 22 nm	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features
	Registration, CD, and defect control for masks
	Eliminating formation of progressive defects and haze during exposure
	Understanding and achieving the specific signature and specifications for a Double Patterned mask
	Establishing a stable process so that signatures can be corrected.
Double patterning	Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures
	Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs
	Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
	Photoresists with independent exposure of multiple passes
	Fab logistics and process control to enable low cycle time impact that efficient scheduling of multiple exposure passes.
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time
	ROI for small volume products
	Resources for developing multiple technologies at the same time
	Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume
	450 mm diameter wafer infrastructure
Process control	New and improved alignment and overlay control methods independent of technology option to <5.7 nm 3σ overlay error
	Controlling LER, CD changes induced by metrology, and defects < 10 nm in size
	Greater accuracy of resist simulation models
	Accuracy of OPC and OPC verification, especially in presence of polarization effects
	Lithography friendly design and design for manufacturing (DFM)

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Table ITWG8B Lithography Difficult Challenges ≤22 nm

Difficult Challenges ≤22 nm	*Summary of Issues*
EUV lithography	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components Cost control and return on investment Resist with < 1.5 nm 3s LWR, < 10 mJ/cm^2 sensitivity and < 20 nm ½ pitch resolution Fabrication of Zero Printing Defect Mask Blanks Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection) Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs) Controlling optics contamination to achieve > five-year lifetime Protection of EUV masks from defects without pellicles Fabrication of optics with < 0.10 nm RMS figure error and < 7% intrinsic flare
Resist materials	Limits of chemically amplified resist sensitivity for < 22 nm half pitch due to acid diffusion length Materials with improved dimensional and LWR control add (limits) Resist and antireflection coating materials composed of alternatives to PFAS compounds Low defects in resist materials (size < 10 nm) Line width roughness < 1.4 nm 3 sigma
Mask fabrication	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair) Mask process control methods and yield enhancement Cost control and return on investment
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput Development of cost-effective post-optical masks Cost effective 450 mm lithography systems Achieving ROI for small volume products
193 nm Immersion Multiple Patterning	Cost control and return on investment Wafer processing to tighter overlay and CD controls Mask fabrication to tighter specifications
Metrology and defect inspection	Defect inspection on patterned wafers for defects < 20 nm Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3s Metrology for achieving < 2.8 nm 3s wafer overlay error Template inspection for 1× Imprint Patterned Masks Phase shifting masks for EUV
Gate CD control improvements and process control	Development of processes to control gate CD < 1.5 nm 3s with < 1.4 nm 3s line width roughness Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3s overlay error, especially for imprint lithography
Maskless Lithography	Wafer throughput Cost control and return on investment Die-to-database inspection of wafer patterns written with maskless lithography Pattern placement - including stitching Controlling variability between beams in multibeam systems
Imprint Lithography	Defect-free imprint templates at 1× dimensions Infrastructure for 1× technology templates (key here is inspection!) Template fabrication to tighter specifications Protection of imprint templates from defects without pellicles Mask life time Throughput Cost control and return on investment Overlay Process control methods to compensate for systematic CD and overlay errors

INTERCONNECT

The Interconnect chapter of the ITRS addresses the wiring system that distributes clock and other signals to the various functional blocks of the integrated circuit, along with providing necessary power and ground connections. For 2008, the scope has been expanded to include the contact level and continues up through the device from metal 1 through to the global wiring levels. Traditionally, global wiring delay has been the "Grand Challenge" and tackling delay generally, is still a primary focus.

The current approach of the 2008 Interconnect Technical Working Group (TWG) for addressing delay is to enable high-bandwidth low-power signaling solutions and a new table, INTC6 High Density Through Silicon Via Specification has been added. The group continues to project the use of copper as the primary conductor in a dual-damascene architecture; however, much of the work in progress focuses on the latest challenges and trends related to 3D integration and emerging technology.

- The Technology Requirements Table (INTC2) has been substantially revised and reorganized and divided into
  - general requirements – e.g., bulk resistivity and dielectric constant
  - level specific requirements determined by the nature of the wire or via geometry – e.g., barrier thickness or effective resistivity
- Low-k roadmap – small slowdown
  - New range for bulk κ
  - Air gaps moved out of emerging sections – considered mainstream
  - Air gaps expected to be the solution for $\kappa_{bulk} < 2.0$
- Atomic layer deposition (ALD) barrier processes and metal capping layers for Cu are lagging in introduction – needed to meet sub 1 nm specifications
  - Hybrid barriers containing ruthenium are proliferating
- J_{max} current limit model show a width dependence – a new reliability concern
- Technology drivers expanded to support both traditional geometric scaling and equivalent scaling
  - Requirements for CMOS-compatible equivalent scaling are highlighted in an expanded *Emerging Interconnect Properties* section along with a new first principle consideration of interconnect properties for new (non-FET) switches
- Design and processing of three-dimensional chip stacking through the use of high-density through silicon vias (TSVs) is a key focus area to address delay and power concerns and a new TSV table has been introduced

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DIFFICULT CHALLENGES

Table ITWG9 Interconnect Difficult Challenges

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures, processes and new materials*	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Three-dimensional control of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Difficult Challenges < 22 nm	*Summary of Issues*
Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Identify solutions which address 3D structures and other packaging issues*	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

** Top three challenges*

CMP—chemical mechanical planarization DRAM—dynamic random access memory

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FACTORY INTEGRATION

The Factory Integration ITWG identifies needed operational factory services and relevant technologies, and it updates the near term and longer term technology requirements and potential solutions to meet these requirements. FI ITWG has five thrust teams and their technology focuses are shown in the following table.

Functional Area	*Key technology focuses and issues*
Factory Operations (FO)	1) Systematic productivity improvement methodology prior to 450 mm insertion 2) Systematic factory waste visualization of cycle times and factory output losses
Production Equipment (PE)	1) 450 mm production tool development 2) Reliable and predictable equipment availability improvement
Material Handling Systems (MHS)	1) Reduction in average material delivery times 2) More interactive control with FICS and PE for accurate scheduled delivery
Factory Information and Control Systems (FICS)	1) Increased FICS reliability performance for more complex factory control 2) Enhanced system extendibility
Facilities	1) Enhanced extendibility for 450 mm and facility cost reduction 2) AMC management, electric static control on masks, wafers, and facility surfaces

2009 HIGHLIGHTS

The Factory Operations technology requirements table was updated so to accommodate *Next Generation Factory* (NGF) and *Waste Reduction Management* requirements with the new metrics introduction. The other FI thrusts' technology requirements tables were revised in accordance with the Factory Operations technology requirements table and their specific technology updates.

NGF TECHNOLOGY REQUIREMENTS INCLUSION

The FI focus areas activity concluded that a significant productivity improvement as NGF is to be promoted before 450 mm introduction. NGF is best described as systematic waste reduction approach that should facilitate comprehensive productivity improvement with the aid of proactive service visibility. NGF can be loaded with so-called 300 mm Prime mission as well. The industry can focus on common technology development for the current wafer diameters and 450 mm.

WASTE REDUCTION MANAGEMENT

Waste Reduction approach has been identified as the effective NGF driver. The ultimate goal for waste reduction is that all the technology requirements tables in the ITRS roadmap adopt waste reduction scheme, i.e., as a new driving axis in addition to the historic Si scaling cost reduction. Two high-level waste metrics have been introduced to promote this approach into Factory Operation technology requirements table. They are Factory WTW (Wait Time Waste) defined as a total sum of wait time for a wafer to go through all the process and Factory EOW (Equipment Output Waste) defined as opportunity loss of production calculated as normalized difference between instantaneous throughput and averaged throughput.

CROSS CUT ISSUES

Green Fab Initiative, Advanced Process Control, fab temperature and humidity control, single wafer versus batch processing for thermal processes and 450 mm cross-cut issues are reflected to the requirements and solutions tables.

FUTURE TREND AND FI ACTIVITIES

Systematic factory services requirements specific to 450 mm manufacturing should be captured as they become available. Onset of single wafer manufacturing is located for 2019 as an ultimate implementation of waste reduction. More understanding is needed for this manufacturing method. Waste Reduction Management needs to be comprehended extensively by ITRS and the industry. It is also required for the industry members to comprehend their own factory-level waste reduction requirements and come up with their own waste reduction roadmap. Green Fab Initiative should be understood from factory services so to have comprehensive set of FI requirements.

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DIFFICULT CHALLENGES

Table ITWG10 Factory Integration Difficult Challenges

Difficult Challenges through 2017	*Summary Of Issues*
1. Responding to rapidly changing, complex business requirements	Increased expectations by customers for faster delivery of new and volume products (design → prototype and pilot → volume production) Rapid and frequent factory plan changes driven by changing business needs Ability to load the fab within manageable range under changeable market demand Enhancement in customer visibility for quality assurance of high reliability products
2. Managing ever increasing factory complexity	Quickly and effectively integrating rapid changes in process technologies Increased requirements for high mix factories. Examples are (1) significantly short life cycle time of products that calls frequent product changes, (2) the complex process control as frequent recipe creations and changes for process tools and frequent quality control criteria due to small lot sizes Manufacturing knowledge and control information need to be shared as required among factory operation steps and disparate factories Need to concurrently manage new and legacy FICS software and systems with increasingly high interdependencies Ability to model factory performance to optimize output and improve cycle time for high mix factories Need to manage clean room environment for more environment susceptible processes, materials, and, process and metrology tools Comprehending increased purity requirements for process and materials
3. Achieving growth targets while margins are declining	Ability to visualize cost and cycle time for systematic waste reduction from all aspects. Reducing complexity and waste across the supply chain Minimize the cost of new product ramp up against the high cost of mask sets and product piloting
4. Meeting factory and equipment reliability, capability and productivity requirements per the Roadmap	Increased impacts that single points of failure have on a highly integrated and complex factory More equipment reliability, capability and productivity visualization that can be used bidirectionally between equipment suppliers and users for more efficient task sharing Design-in of equipment capability visualization in production equipment Equipment supplier roadmap for equipment quality visualization and improvement, and, reduction of Equipment Output Waste. Reduction of equipment driven NPW (non-product wafers) operations that compete for resources with production wafers and Dandori operations[1]
5. Emerging factory paradigm and next wafer size change	Uncertainty about 450 mm conversion timing and ability of 300 mm wafer factories to meet historic 30% cost effectiveness. Uncertainty concerning how to reuse buildings, equipment, and systems to enable 450 mm wafer size conversion at an affordable cost
Difficult Challenges Beyond 2017	*Summary of Issues*
1. Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	Ability to utilize task sharing opportunities to keep the manufacturing profitable such as manufacturing outsourcing Enhanced customer visibility for quality assurance of high reliability products including manufacturing outsourcing business models Scalability implications to meet large 300 mm factory needs [40K–50K WSPM] Cost and task sharing scheme on industry standardization activity for industry infrastructure development
2. Managing ever increasing factory complexity	Higher resolution and more complications in process control due to smaller process windows and tighter process targets in many modules Complexity of integrating next generation lithography equipment into the factory More comprehensive traceability of individual wafers to identify problems to specific process areas Comprehensive management that allows sharing and re-usages of complex engineering knowledge and contents such as process recipes, APC algorithms, FD and C criteria, equipment engineering best known methods
3. Increasing global restrictions on environmental issues	Need to meet regulations in different geographical areas Need to meet technology restrictions in some countries while still meeting business needs Comprehending tighter ESH/Code requirements Lead free and other chemical and materials restrictions New material introduction
4. Post-conventional CMOS manufacturing uncertainty	Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements on factory design Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency

[1] Dandori operations Peripheral equipment related operations that are in parallel or in-line and prior to or following to the main thread PE operations. So-called in-situ chamber cleaning is another good example than NPW operations.

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ASSEMBLY AND PACKAGING

The rapid growth in three dimensional electronics, System in Package (SiP) and other new technologies that enable "More than Moore" has resulted in an accelerated pace of change in the Roadmap for Assembly and Packaging. There will be several sections added or expanded in the 2009 ITRS to address these emerging technologies. Several of these areas are initially addressed in the table changes for 2008.

The major changes include:

- Optical interconnect on chip and chip to chip within a SiP has been added as a volume technology in 2011.
- Modifications were made to Tables AP3 and AP4 to reflect changes in bonding pitch for specific technologies. In some cases driven by changes in demand rather than capability.
- A new table, AP4b was added to address the increasingly serious issues associated with warpage and its impact on assembly.
- Tables AP5a, AP5b and AP5c were altered to provide greater clarity for differences between the Roadmap for polymer package substrates and the glass-ceramic substrate used for certain high temperature device types.
- Table AP9 was restructured to provide quantitative projections to replace the qualitative information in the 2007 version of the table.
- Table AP10 has been modified to provide greater detail and has been segmented into the major process types.
- Table AP11 has been modified to incorporate changes in component sizes, reflow temperatures and other parameters that are changing to meet the requirements of SiP.
- Table AP15 has added Active Optical cables. This table and the associated text will see major revisions in 2009 reflecting the incorporation of optical interconnect in SiP and system interconnect.
- Table AP16 has been segmented by application in recognition of the different packaging challenges for different optoelectronic applications.
- Table AP19 is in the process of a major revision that will be incorporated into the 2009 ITRS.
- Table AP21: Automotive Operating Environment Specifications has been added. This material was treated in the text for 2007 but with the increase in electronic content including components for electric and hybrid cars it needs to be a numbered table. This topic will be substantially expanded in the text of the 2009 ITRS.

There are a number of other minor changes incorporated in the AP tables for 2008. The most important issues identified in this update are related to major changes already underway for the rewrite in 2009. They will incorporate a more detailed treatment of the materials, processes and design changes required to address the challenges of 3D electronics and the functional diversification of the "More than Moore" era.

DIFFICULT CHALLENGES

Innovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices. Near term difficult challenges exist in all phases of the assembly and packaging process from design through manufacturing, test, and reliability.

Many critical technology requirements are yet to be met and they are listed in Table ITWG11 below. Meeting these requirements will demand significant investment in research and development.

Table ITWG11 Assembly and Packaging Difficult Challenges

Difficult Challenges ≥22 nm	*Summary of Issues*
Impact of BEOL including Cu/low κ on packaging	-Direct wire bond and bump to Cu or improved barrier systems bondable pads - Dicing for ultra low k dielectric -Bump and underfill technology to assure low-κ dielectric integrity including lead free solder bump system -Improved fracture toughness of dielectrics -Interfacial adhesion -Reliability of first level interconnect with low κ -Mechanisms to measure the critical properties need to be developed. -Probing over copper/low κ
Wafer level CSP	-I/O pitch for small die with high pin count -Solder joint reliability and cleaning processes for low stand-off -Wafer thinning and handling technologies -Compact ESD structures -TCE mismatch compensation for large die
Coordinated design tools and simulators to address chip, package, and substrate co-design	-Mix signal co-design and simulation environment -Rapid turn around modeling and simulation -Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis -Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) -System level co-design is needed now. -EDA for "native" area array is required to meet the Roadmap projections. -Models for reliability prediction
Embedded components	-Low cost embedded passives: R, L, C -Embedded active devices -Quality levels required not attainable on chip -Wafer level embedded components
Thinned die packaging	- Wafer/die handling for thin die - Different carrier materials (organics, silicon, ceramics, glass, laminate core) impact -Establish infrastructure for new value chain -Establish new process flows -Reliability -Testability -Different active devices -Electrical and optical interface integration

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Table ITWG11 Assembly and Packaging Difficult Challenges (continued)

Difficult Challenges ≥ 22 nm	*Summary of Issues*
Close gap between chip and substrate Improved organic substrates	-Increased wireability at low cost -Improved impedance control and lower dielectric loss to support higher frequency applications -Improved planarity and low warpage at higher process temperatures -Low-moisture absorption -Increased via density in substrate core -Alternative plating finish to improve reliability -Solutions for operation temp up to C5-interconnect density scaled to silicon (silicon I/O density increasing faster than the package substrate technology -Production techniques will require silicon-like production and process technologies after 2005 -Tg compatible with Pb free solder processing (including rework at260 C)
High current density packages	-Electromigration will become a more limiting factor. It must be addressed through materials changes together with thermal/mechanical reliability modeling. -Whisker growth -Thermal dissipation
Flexible system packaging	-Conformal low cost organic substrates -Small and thin die assembly -Handling in low cost operation
3D packaging	-Thermal management -Design and simulation tools -Wafer to wafer bonding -Through wafer via structure and via fill process -Singulation of TSV wafers/die - Test access for individual wafer/die -Bumpless interconnect architecture
Difficult Challenges <22 nm	*Summary of Issues*
Package cost does not follow the die cost reduction curve	-Margin in packaging is inadequate to support investment required to reduce cost -Increased device complexity requires higher cost packaging solutions
Small die with high pad count and/or high power density	These devices may exceed the capabilities of current assembly and packaging technology requiring new solder/UBM with: -Improved current density capabilities -Higher operating temperature
High frequency die	-Substrate wiring density to support >20 lines/mm -Lower loss dielectrics—skin effect above 10 GHz -“Hot spot” thermal management There is currently a “brick wall” at five-micron lines and spaces.
System-level design capability to integrated chips, passives, and substrates	-Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult. -Complex standards for information types and management of information quality along with a structure for moving this information will be required. -Embedded passives may be integrated into the “bumps” as well as the substrates.
Emerging device types (organic, nanostructures, biological) that require new packaging technologies	-Organic device packaging requirements not yet defined (will chips grow their own packages) -Biological interfaces will require new interface types

TSV—through silicon via

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ENVIRONMENT, SAFETY, AND HEALTH

The four basic ITRS ESH Chapter strategies in 2009 remain as they were in the previous edition; namely: 1) Understand (characterize) processes and materials during the development phase; 2) Use materials that are less hazardous or whose by-products are less hazardous; 3) Design products and systems (equipment and facilities) that consume less raw material and resources and, 4) Make the factory safe for employees.

There is one additionally significant new element in 2009, which is the addition of ESH Categories. Previous ESH chapter tables presented a requirements set that related ESH concerns to the technical thrusts (e.g., Interconnect, Front End Processes, etc.). They also identified ESH concerns that are broader and more general than those pertaining to a single technology thrust (referred to as Intrinsic).

To focus available resources toward those areas of greatest added benefit, in addition to the ESH improvements gained, all ESH requirements have now been placed in one of three Categories:

1. *Critical*—Any requirement in this category is an essential item for technology success/implementation as well as ESH benefits. If not addressed, it could compromise the ability to insert the technology into manufacturing.
2. *Important*—Any requirement in this category is a key item for process success as well as ESH benefits. If not addressed, it could compromise the cost of ownership (CoO) of the technology in manufacturing, based on factors such as throughput, yield, and chemical/material and/or tool costs.
3. *Useful*—Any requirement in this category is a key item for ESH benefits ("best practices"), but without any clear additional factors that would place it in either of the above two categories. If not addressed, it could compromise the ability to achieve the lowest ESH impact for the technology when inserted into manufacturing.

Also new for 2009 is a table of all ESH requirements considered for the 2009 Roadmap sorted according to the following ESH domains for easy reference. These are *Restricted Chemicals, New Chemicals, Nanotechnology (*former subset of New Chemicals*), Utilization/Waste Reduction, Energy,* and *Green Fab.*

For 2010 one critical area for the ESH chapter will be to further refine needs in technical terms to efficiently incorporate impacts from ESH policy (government and public) on materials. This will be done by continued harmonizing of the ESH Categorization with technology requirements.

Other areas for 2010 emphasis will be Energy and Carbon Footprint (improving perspective for new technology role in energy conservation), improvements needed for the timely availability of Chemical Assessment Data and Methodologies, more in depth evaluation of potential 450 mm impacts and evaluation of how ESH requirements may differ between memory and logic roadmaps.

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DIFFICULT CHALLENGES

Table ITWG12A Environment, Safety, and Health Difficult Challenges—Near-term

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials can be utilized (without delay) in manufacturing, while protecting human health, safety, and the environment. Given the global movement possible for R&D, pre-manufacturing, and full commercialization, these methodologies must recognize regional regulatory/policy differences, and the overall trends towards lower exposure limits and increased monitoring. • *Chemical Data Availability*: There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use In addition, methods for anticipating and forecasting such future requirements are not well developed.. • *Chemical Exposure Management*: There is incomplete information on how chemicals/materials are used and the process by-products formed. Also, while methods used to obtain such information are becoming more standardized, their availability varies depending on the specific issue being addressed, and can use improvement.
Process and equipment management	• *Process Chemical Optimization* There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). • *Environment Management* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations (including the capability for component isolation in waste streams) for such hazardous and non-hazardous emissions and by-products can be addressed. • *Global Warming Emissions Reduction*: There is a need to reduce emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Water and Energy Conservation* There is a need for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization* There is a need for more efficient chemical/material utilization, with improved reuse/recycling/reclaiming of them and their process emissions and byproducts. • *Byproducts Management*: There is a need for improved metrology for byproduct speciation. • *Chemical Exposure Management* There is a need to design-out chemical exposure potentials and the requirements for personal protective equipment (PPE) • *Design for Maintenance* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities use, and for more efficient cleanrooms' and facilities systems' thermal management. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics* There is a need for methodologies to define and measure a technology generation's sustainability. • *Design for ESH* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes, and products. • *End-of-Life Reuse/Recycle/Reclaim* There is a need to design facilities, equipment and products to facilitate these end-of-life issues

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Table ITWG12B Environment, Safety, and Health Difficult Challenges—Long-term

Difficult Challenges < 16 nm	*Summary of Issues*
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials can be utilized (without delay) in manufacturing, while protecting human health, safety, and the environment. • *Chemical Data Availability*: There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use • *Chemical Exposure Management*: There is incomplete information on how chemicals/materials are used and the process by-products formed.
Process and equipment management	• *Chemical Reduction*: There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). There is a need to reduce emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Environment Management* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations for such hazardous and non-hazardous emissions and by-products can be addressed. • *Water and Energy Conservation* There is a need to reduce water and energy consumption, and for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization* There is a need for more efficient chemical/material utilization, with their increased reuse/recycle/reclaim (and of their process emissions and byproducts). • *Chemical Exposure Management* There is a need to design-out chemical exposure potentials and personal protective equipment (PPE) requirements. • *Design for Maintenance* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities use, and for more efficient cleanrooms' and facilities systems' thermal management. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics* There is a need for methodologies to define and measure a technology generation's sustainability, and also sustainability at a factory infrastructure level. • *Design for ESH* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes, and products, with methodologies to holistically evaluate and quantify the ESH impacts of facilities operations, processes, chemicals/materials, consumables, and process equipment for the total manufacturing flow. • *End-of-Life Reuse/Recycle/Reclaim*: There is a need to design facilities, equipment and products to facilitate these end-of-life issues

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YIELD ENHANCEMENT

DIFFICULT CHALLENGES

The key challenges were adapted to latest developments and challenges recognized by the 2009 International Technical Working Group Yield Enhancement. In 2009 a new long term key challenge was identified. This is the introduction of 450 mm wafers which is expected to impact the defect detection and characterization but as well defect budgets and yield models due to the large surface of the substrate. The introduction of 450 mm wafers requires a new generation of inspection tools. The cost of ownership is impacted by throughput and tool cost. It will be difficult to maintain the throughput of inspection tools at the 45 mm wafer size. Therefore, the tool costs are crucial. 450 mm handling for inspection has the risk of large substrate flexibility but also coordinate accuracy required for defect review. Due the large surface a huge amount of inspection data will be obtained. Improvement of data quality and reduction of the amount of data will be important. Defect budgets and yield models are impacted by the unknown defect densities on the large substrates.

The order and type of near term key challenges was not changed in 2009. Currently, the most important key challenge will be the detection of multiple killer defects and the signal-to-noise ratio. It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership and high through put. Furthermore, it is a dare to identify but yield relevant defects under a vast amount of nuisance and false defects. As a challenge with second priority the requirement for 3D inspection was identified. This necessitates for inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The demand for high-speed and cost-effective inspection tools remains. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases. E-beam inspection seems not to be the solution for all those tasks any more.

Other topics challenging the Yield Enhancement community are prioritized as follows in the near term:

- Process Stability vs. Absolute Contamination Level Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.
- Wafer Edge and Bevel Monitoring and Contamination Control – Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems. Currently, the monitoring and contamination control methods require intensive development.

In the long term the following key challenges are currently identified:

- Non-Visual Defects and Process Variations: Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.
- In - line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.
- Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.
- Introduction of 450 mm substrates (see above)

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The Yield Enhancement chapter consists of three subchapters as Defect Budget and Yield Model, Defect Detection and Characterization, and Wafer Environment and Contamination Control. The major work during 2009 was the control and update of the tables. The changes summarizes as follows:

Defect Budget and Yield Model

- The tables for Defect budgets were not updated. The ITWG requires a solution to access updated particle per wafer pass data or particle control limits to supply defects and tolerable particle per wafer pass data to equipment suppliers and integrated device manufacturers in the future.

Defect Detection and Characterization

- The tables YE 6, 7 and 8 were checked carefully against latest developments for defect inspection and detection.

Table ITWG13 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Detection of Multiple Killer Defects / Signal to Noise Ratio - Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.	Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. Reduction of inspection costs and increase of throughput is crucial in view of CoO. Detection of line edge roughness due to process variation. Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. Reduction of background noise from detection units and samples to improve the sensitivity of systems. Improvement of signal to noise ratio to delineate defect from process variation. Where does process variation stop and defect start?
3D Inspection – For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases.	Detection of non visible defects e.g. voids, embedded defects, and sub surface defects in the structures. The demand for high-speed and cost-effective inspection is crucial. Large number of contacts and vias per wafer E-beam inspection seems not to be the solution for all those tasks any more. Sensitivity of the inspection tool to process variation and definition of maximum process variation (control limits).
Process Stability vs. Absolute Contamination Level – Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect.
Wafer Edge and Bevel Monitoring and Contamination Control – Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems.	Currently, the monitoring and contamination control methods require intensive development.

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Table ITWG13 Yield Enhancement Difficult Challenges

Difficult Challenges < 16 nm	*Summary of Issues*
Non-Visual Defects and Process Variations – Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.	SMLY, resulting from unrecognized models hidden in the chip, should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. It is required to manage the above models at both the design and manufacturing stage. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis runs time per die. d) Statistical methodology to analyze results of logic diagnosis for denoising influence of random defects and building a layout-dependent systematic yield model. Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic yield loss, and has to improve their coverage.
In - line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality. [1]	Data volume + quality: strong increase of data volume due to miniaturization The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. It will be recommended to supply information on chemical state and bonding especially of organics. Small volume technique adapted to the scales of technology generations. Capability to distinguish between the particle and the substrate signal.
Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	A lot of models should be operated at the design stage. For example, Optical Proximity Correction, Well Proximity, Stress Proximity, CMP and so on The Amount of models seems to be rapidly increasing. Not only accuracy of models, but also optimization of trade-off between models might be requested. Development of test structures for new technology generations
The introduction of 450 mm wafers is expected to impact the defect detection and characterization but as well defect budgets and yield models due to the large surface of the subtrate. The introduction of 450 mm wafers requires a new generation of inspection tools.	The cost of ownership is impacted by throughput and tool cost. It will be difficult to maintain the throughput of inspection tools at the 45 mm wafer size. Therefore, the tool costs are crucial. 450 mm handling for inspection has the risk of large substrate flexibility but also coordinate accuracy required for defect review. Due the large surface a huge amount of inspection data will be obtained. Improvement of data quality and reduction of the amount of data will be important. Defect budgets and yield models are impacted by the unknown defect densities on the large substrates.

[1] Cross-link to Metrology chapter

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METROLOGY

Metrology requirements continue to be driven by advanced lithography processes, new materials, and Beyond CMOS materials, structures, and devices. The introduction of dual patterning and double exposure lithography add the complexity of measuring two distributions of linewidth, sidewall angle, and line width roughness inside the same measurement area. Another key challenge to critical dimension metrology is tool matching. Precision requirements for the next several years can be met using single tools. There are many gaps in metrology for EUV lithography especially for mask metrology. The entire mask fabrication process needs advances in capability especially for actinic patterned mask inspection and aerial imaging. Overlay metrology capability lags behind the need for improved overlay control. Front end processes continues to drive metrology to provide measurements for new higher dielectric constant materials, dual work function metal gates, and new ultra shallow junction doping processes. The sub 1 nm EOT gate stacks require greatly improved film thickness and composition control during manufacturing. Interconnect structures continue the cycle of new materials. The need for porosity control for low k materials has driven a renewed interest in porosity measurements. 3D interconnect metrology requirements are largely driven by the activity in through silicon vias (TSV) R&D. Bonded wafer overlay control for next generation TSV now has potential solutions that are under investigation. In the area of metrology for Beyond CMOS R&D, graphene measurements have advanced in the areas of microscopy and electrical characterization. In addition, there are now several means of determining the number of graphene layers in a sample. The need for understanding large area graphene uniformity is driving both physical and electrical metrology. In addition, metrology R&D is working with other Beyond CMOS materials.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 22 nm technology generation. Metrology needs after 2015 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table ITWG14 presents the ten major challenges for metrology.

Table ITWG14 Metrology Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of new process technology such as Dual Patterning Lithography, complicated 3D structures such as capacitors and contacts for memory, and 3D Interconnect are not ready for their rapid introduction.	Overlay measurements for Dual Patterning have tighter control requirements. Overlay defines CD. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures including capacitors, devices, and contacts.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 16 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks. Sampling plan optimization is key to solve these issues.
Statistical limits of sub-32 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for ***beyond CMOS.***	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

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MODELING AND SIMULATION

Modeling and Simulation is the virtual counterpart of semiconductor device and chip fabrication and characterization: Computer programs are used to predict the geometries, strain and chemical composition (dopants, SiGe, etc.) of devices, their electrical performance and reliability, and finally the behavior of circuits and systems. The overall aim of Modeling and Simulation is to support the development of real-world technologies, devices, circuit and systems by providing information which is more difficult, more costly, less efficient or too time-consuming to obtain from experiments, and in this way to reduce development times and costs. To enable this, Modeling and Simulation tools must contain appropriate physical models including appropriate parameter settings, and also meet various requirements in terms of generality of application, speed of simulation, complexity of the applications which can be addressed, and, last but not least, user interfaces and interactions. In turn, dedicated research and development activities on Modeling and Simulation capabilities are needed.

In order to best meet the needs of the users of simulation tools in industry and research, the Modeling and Simulation group in the ITRS has also in 2009 based its work strongly on the industrial requirements, both from own assessments and from the results of the other groups in the ITRS, which deal with the various areas of process technology, integration, and fabrications issues. Starting from thorough review of all their texts and presentations and detailed discussions with these groups, also for the 2009 ITRS so-called crosscut sections have been prepared for the 2009 Modeling and Simulation chapter, and been used for the 2009 work.

The main part of the Modeling and Simulation chapter was prepared based on these crosscuts and an overall assessment of the state-of-the-art. In the following, the main elements of the chapter are summarized especially in view of the changes made compared with the 2007/2008 ITRS.

Similar to earlier years, the Modeling and Simulation Difficult Challenges are emphasized in the beginning of the chapter. The six short-term challenges refer in 2009 to nodes until 16 nm including. Among these, two challenges have been renamed to *Nanoscale device simulation capability: Methods, models and algorithms that contribute to prediction of CMOS limits* and *Electrical-thermal-mechanical modeling for interconnect and packaging*. Because of the developments of the industrial needs and the state-of-the-art, the detailed contents of all of these challenges were significantly changed, as displayed in Table ITWG15 below and Table MS-1 of the 2009 Modeling and Simulation Chapter. The long-term challenges now refer to nodes smaller than 16 nm. Here, only the contents of the first two of them were slightly modified.

Similar to these crosscuts with the other groups of the ITRS, there are also strong links between the areas covered by the Modeling and Simulation chapter, ranging from the area of equipment simulation through processes, devices, interconnects and circuits up to packages. Also in 2009 Modeling and Simulation chapter contains seven subchapters which deal with the various levels of modeling: *Equipment / Feature Scale modeling*, *Lithography Modeling*, *Front-end Process Modeling*, *Device Modeling*, *Interconnects and Integrated Passives Modeling*, *Circuit Modeling*, and *Package Simulation*. Whereas the scope of these subchapters has not changed compared to 2007, the requirements described therein have considerably evolved based on the development of the industry and the state-of-the-art in modeling and simulation.

In the 2007 ITRS, there were three topics which crosscut these seven areas, namely *Materials Modeling*, *TCAD for Design, Manufacturing and Yield*, and *Numerical Methods*. For the 2009 ITRS, the latter subchapter was extended to also include the *Interoperability of Tools*, which is an important requirement for the efficient use of simulation in industry and research. The second of these crosscutting subchapters has evolved in scope to a subchapter on *Modeling for Design Robustness, Manufacturing, and Yield*. Furthermore, because reliability issues get more important at all levels of simulation and, moreover, reliability problems at device, circuit, or package level are partly based on details of fabrication processes and their variations, a new separate crosscutting subchapter on *Reliability Modeling* has been added in the 2009 Modeling and Simulation chapter.

The development of new modeling capability generally requires long-term research, and increasingly interdisciplinary activities, which can be carried out best in an academic or a laboratory setting. For this reason, a vigorous research effort at universities and independent research institutes is a prerequisite for success in the modeling area, together with a close cooperation with industry, along the simulation food chain mentioned above.

Because the necessary basic work generally needs significant development time, it is vital that adequate research funds will be made available in a timely manner in order to address the industry's future critical needs. Currently, the shortage of such research funds is even more severe than the technical difficult challenges summarized above. For example, several Modeling and Simulation requirements listed in the 2005 and 2007 ITRS had in this 2009 issue to be pushed out and delayed in time because sufficient R&D could not be done due to insufficient research funding.

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DIFFICULT CHALLENGES

Table ITWG15 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Lithography simulation including EUV	Models and experimental verification of optical and non-optical immersion lithography effects (e.g., topography and change of refractive index distribution)
	Simulation of multiple exposure/patterning including database splitting
	Multi-generation lithography system models
	Simulation of defect influences/defect printing in EUV. Mask optimization including defect compensation
	Optical simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including extensions for inverse lithography
	Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects
	Predictive resist models (e.g., mesoscale models) including line-edge roughness, etch resistance, adhesion, mechanical stability, leaching, and time-dependent effects in single and multiple exposure; resist processing techniques special for double patterning
	Resist model parameter calibration methodology (including kinetic and transport parameters)
	Simulation of ebeam mask making (single-beam and multibeam)
	Simulation of directed self-assembly of sublitho patterns
	Modeling lifetime effects of equipment and masks
	Predictive coupled deposition-lithography-etch simulation (incl. double patterning, self-aligned patterning)
	Modeling metrology equipment for enhancing its accuracy
Front-end process modeling for nanometer structures	Coupled diffusion/activation/damage/stress models and parameters including SPER and millisecond processes in Si-based substrate, that is, Si, SiGe, SiGe:C, Ge-on-Si, III/V-on-Si, SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers
	Modeling of interface and dopant passivation by hydrogen or halogens
	Modeling of cluster or cocktail implants
	Modeling of plasma doping, e.g. for FinFETs
	Modeling of epitaxially grown layers: Shape, morphology, stress, defects, doping
	Modeling of stress memorization (SMT) during process sequences
	Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
	Efficient and robust 3D meshing for moving boundaries
	Front-end processing impact on device leakage (e.g. residual defects) and reliability
Integrated modeling of equipment, materials, feature scale processes and influences on devices, including variability	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-)products, rates ...) , and simplified but physical models for complex chemistry and plasma reaction
	Linked equipment/feature scale models (including high-κ metal gate integration, damage prediction)
	Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
	Spin-on-dielectrics (stress, poriosity, dishing, viscosity, …) for high aspect ratio fills
	Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
	Simulation of polishing, grinding and wafer thinning in backend processing

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Table ITWG15 Modeling and Simulation Difficult Challenges

	Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulation
Nanoscale device simulation capability: Methods, models and algorithms that contribute to prediction of CMOS limits	General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra
	Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
	Models (incl. material models) to investigate new memory devices like MRAM, PCM/PRAM, etc
	Gate stack models for ultra-thin dielectrics with respect to. electrical permittivity, built-in charges, influence on workfunction by interface interaction with metals, reliability, tunneling currents and carrier transport
	Modeling of salicide/silicon contact resistance and engineering (e.g. Fermi-level depinning to reduce Schottky barrier height)
	Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure and dopant variations in order to assess the impact of variations on statistics of device performance
	Physical models for novel materials, e.g., high-κ stacks, Ge and compound III/V channels, etc.: Morphology, band structure, defects/traps, etc.
	Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation
	Reliability modeling for ultimate CMOS
	Physical models for stress induced device performance
Electrical-thermal-mechanical-modeling for interconnect and packaging	Model thermal-mechanical, thermodynamic and electrical properties of low κ, high κ, and conductors for efficient on-chip and off-chip incl. SIP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension
	Thermal modeling for 3D ICs and assessment of modeling tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keepout regions, etc.). Size effects (microstructure, surfaces, etc.) and variability of thinned wafers.
	Signal integrity modeling for stacked die
	Model effects which influence reliability of interconnects/packages incl. 3D integration (e.g., stress voiding, electromigration, fracture, dielectric breakdown, piezoelectric effects)
	Physical models to predict adhesion on interconnect-relevant interfaces (homogeneous and heterogeneous)
	Simulation tools for adhesion and fracture toughness characteristics for packaging and die interfaces
	Dynamic simulation of mechanical problems of flexible substrates and packages
	Models for electron transport in ultra fine patterned interconnects
Circuit element and system modeling for high frequency (up to 160 GHz) applications	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package: - possibly consisting of different technologies, - covering and combining different modelling and simulation levels as well as different simulation domains
	Scalable active component circuit models [1] including non-quasi-static effects, substrate noise and coupling,, high-frequency RT and 1/f noise, temperature and stress layout dependence and parasitic coupling
	Scalable passive component models [1] for compact circuit simulation, including interconnect, transmission lines, …
	Scalable circuit models [1] for More-than-Moore devices including switches, filters, accelerometers, …
	Physical circuit element models for new memory devices, such as PCM, and standardization of models for III/V devices

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Table ITWG15 Modeling and Simulation Difficult Challenges

	Computer-efficient inclusion of aging, reliability and variability including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently
	Efficient building block/circuit-level assessment using process/device/circuit simulation, including process variations
Difficult Challenges < 16 nm	*Summary of Issues*
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: 1) Gate stacks: Predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. 2) Models for novel integrations in 3D interconnects including airgaps and data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties 3) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. 4) Accumulation of databases for semi-empirical computation.
Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials	*Ab-initio* modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping, quantum dots, atomic electronics, multiferroic materials and structures, strongly correlated electron materials)
	Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …). Modeling impact of geometry, interfaces and bias on transport for carbon-based nanoelectronics
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling
	Physical design tools for integrated electrical/optical systems
NGL simulation	Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects & impact on LER); heating and charging effects), including impact on device characteristics (e.g. due to local crystal damage by electron scattering or charging effects)
	Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

[1] In More than Moore, scalability refers to the ability to model litho-defined device variations

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OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

BACKGROUND

The Overall Roadmap Technology Characteristics (ORTC) tables are created early in the Roadmap process and are used as the basis for initiating the activities of the International Technology Working Groups in producing their detailed chapters. These tables are also used throughout the renewal effort of the Roadmap as a means of providing synchronization among the TWGs by highlighting inconsistencies between the specific tables. The process to revise the tables includes increasing levels of cross-TWG and international coordination and consensus building to develop underlying models of trends and to reach agreement on target metrics. As a result, the ORTC tables undergo several iterations and reviews.

The metric values of the ORTC tables can be found throughout the Roadmap in greater detail in each Technology Working Group chapter. The information in this section is intended to highlight the current rapid pace of advancement in semiconductor technology. It represents a completion of the revision update and renewal work that began in 2008. Additionally, the ORTC Glossary has been updated in 2009.

OVERVIEW OF 2009 REVISIONS

DEFINITIONS

As noted above, the Overall Roadmap Technology Characteristics tables provide a consolidated summary of the key technology metrics. Please note that, unless otherwise specified for a particular line item, the default year header still refers (as in previous Roadmaps) to the year when product shipment first exceeds thousands of units per month of ICs from a manufacturing site using "production tooling." Furthermore, a second company must begin production within three months (see Figure 2a). To satisfy this timing definition, ASIC production may represent the cumulative volume of many individual product line items processed through the facility.

It was mentioned in the Introduction section of the ITRS Executive Summary, but it is worth repeating, that there continues to be confusion in the industry regarding individual company public press announcements of their "node" progress and timing, which may or may not align with the ITRS definitions and specific targets.

During the 2003 ITRS development, an attempt was made to reconcile the many published press releases by Logic manufacturers referencing "90 nm" technology "node" manufacturing in 2003. Since the contacted metal 1 (M1) half-pitch of actual devices was cited at 110–120 nm, confusion arose regarding the relationship to the ITRS DRAM stagger-contacted M1 half-pitch-based header targets. After conversation with leading-edge manufacturers, it was determined that some of the public citations were in reference to an "indexed" technology node roadmap that represented the average of the half-pitch (for density) and the printed gate length (for speed performance). Some companies also referenced the timing for doubling of functionality on a given product (for example the doubling of logic gates or memory bits) as a measure of "node" advancement. This approach of measuring technology progress complicates the "node" relationship, because density improvements can be accomplished by design improvements added along with linear lithographic feature size reduction.

Additional confusion has developed due to the technology "node" references in Flash memory product announcements, and Flash technology received increased emphasis in both the 2005 and 2007 ITRS. For example, Flash product cell density is defined by the un-contacted poly-silicon (poly) interconnect half-pitch, rather than a metal 1 (M1) half-pitch (the key feature which drives density in DRAM and MPU and ASIC products). Also, very aggressive Flash memory Cell Area Factor (see Glossary) improvements have been added by Flash cell designers in order to aggressively reduce costs and meet the rapidly ramping demand for non-volatile memory (NVM) storage.

The International Roadmap Committee (IRC) decided in the 2007 ITRS roadmap that the best way to minimize confusion between the ITRS and individual company public announcements was to continue the separate tracking of the various technology trend drivers by product—DRAM, MPU/ASIC, and Flash. As mentioned earlier, the MPU/ASIC and DRAM product half-pitches are now both defined by a common reference to the M1 stagger-contact, while the Flash NVM

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product is referenced to un-contacted poly dense parallel lines (refer to Figure 1). Individual TWG tables will utilize the product table header line items that are most representative of the technology trend drivers for each table.

Due to the emphasis on separate product trend tracking, no common product technology header is required. Only the year of production of the referenced technology line item is required as the minimum ITWG table header. In each of the roadmaps since the 2007 ITRS, the technology trends and the functional (transistors, bits, logic gates) or characteristic (speed, power) performance associated with the individual product groups (DRAM, Flash, MPU, ASIC) are emphasized. Individual company references that wish to compare to the ITRS must now reference the specific product technology trend line item, as further defined by the ITRS Executive Summary and Glossary.

Individual product technology trends continue to be monitored, and the most recent TWG survey update is indicating that the DRAM historical trend continues to track close to the average 2.5-year cycle (*cycle = one-half reduction per two cycle periods) trend, and the 2009 DRAM M1 half-pitch targets are therefore unchanged from the 2008 ITRS Update ORTC Tables. The modeled and calculated projection trends may produce slight differences from the actual survey results, however the timing which influences the Grand Challenges and Potential Research and Development solutions are consistent with the average trends of latest survey results.

In the most recent Flash technology survey, the overall lithography resolution continues to be driven at the most leading edge by the feature size trend from Flash product. For example, as is described in additional detail below, the uncontacted polysilicon half-pitch of FLASH memories is now projected to be even further ahead of DRAM stagger-contacted M1 half-pitch (by three years by 2010). A two-year lead by the Flash uncontacted polysilicon half-pitch is considered equivalent (in lithographic processing difficulty) to a one-year lead of the DRAM stagger-contacted M1 half-pitch, and this additional timing lead increase is therefore causing Flash memory technology to continue to drive leading-edge lithography. Please see the Glossary section for additional detail on the "Year of Production" timing definition.

The 2009 ITRS table technology trend targets continue as annualized targets from 2009 through the 15-year Roadmap horizon in 2024. However, per previously established IRC guidelines, the 2009 ITRS retains the *definition of a technology trend cycle time as the period of time to achieve a significant advancement in the process technology. To be explicit, a technology trend cycle time advancement continues to be defined as the period of time to achieve an approximate 0.71× reduction per cycle (precisely 0.50× per two cycles). Refer to Figures 6 and 7.

Please note from the 2009 ITRS Table ORTC-1 that the timing of a technology cycle remains different for a particular product. For example, the DRAM stagger-contact half-pitch M1 in the 2009 ITRS is still forecast to be on an average 0.71× reduction every two and one-half years (0.50×/5-years) timing cycle until 2010/45 nm). After 2010, the DRAM M1 trend is forecast to be on a three-year cycle through the 2024/~9 nm target. The annual multiplier for the three-year cycle timing is 0.8909× reduction per year, which is used to calculate the interim annual trend targets (examples: 2011/40 nm, 2020/14 nm).

After taking into account the available industry PIDS survey data and other ITWG and IRC inputs, consensus was reached on a new Flash product technology timing model (based on the uncontacted polysilicon half-pitch definition). The Flash uncontacted polysilicon half-pitch is now set on a two-year cycle timing pace from 2000/180 nm, but extended through 2010/32 nm. The Lithography ITWG also continues to use the Flash uncontacted polysilicon half-pitch (now projected to be numerically three years "ahead" of the DRAM stagger-contacted M1 half-pitch in 2010) to drive the technology process equipment being used to achieve that target. After 2010/45 nm, the Flash uncontacted polysilicon half-pitch is expected to turn to a three-year timing cycle, parallel, but three years ahead of the DRAM trend, and would extend to 2024/6 nm on an annual basis.

In response to new Design TWG data and model updates for the 2009 ITRS, the MPU (and high-performance ASIC) (MPU/hpASIC) Product Trend cycle timing (based on the same stagger-contact M1 half-pitch definition as DRAM) has been updated. After analysis of historical data and consensus agreement by the ITWGs and IRC, the MPU M1 half-pitch is now delayed behind the DRAM trend; however the MPU/hpASIC is set on a two-year (reducing in half every 4-years) cycle timing pace through 2013/27 nm. At the 2010/45 nm point, it was decided that the MPU/hpASIC M1 targets would cross over the DRAM M1 cycle timing target and at the 2013/27 nm point will turn to a three-year timing cycle through the end of the roadmap in 2024.

The MPU/hpASIC final physical gate-length (phGL) was significantly revised in the 2008 Update, and then again during the 2009 ITRS work. The targets for a portion of the historical trend remain unchanged from the 2003 ITRS, in which the timing was set at a two-year cycle (0.5×/4-years; 0.8409×/year) from 1999 through the 2003/45 nm point. From that point through the new 2009/29 nm target, the trend was adapted to track actual data points provided by the FEP and PIDS ITWGs. From the 2009/29 nm point the model tracks the PIDS survey data, and utilizes trend targets calculated by using

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a 3.8-year timing (reducing in half every 7.6 years; or 0.9128 reduction per year) cycle through the end of the Roadmap to 2024/7.4 nm. The Lithography and FEP ITWGs revised their agreement on a new consensus variable ratio between the printed gate length targets and the final physical gate length, which includes etch.

The low-operating-power ASIC gate length targets are likewise adapted to the new PIDS survey data (by shifting their introduction timing relative to the MPU printed and physical gate lengths); and a new standby-power physical gate length line item was added in the 2008 Update and is updated in the 2009 ORTC tables.

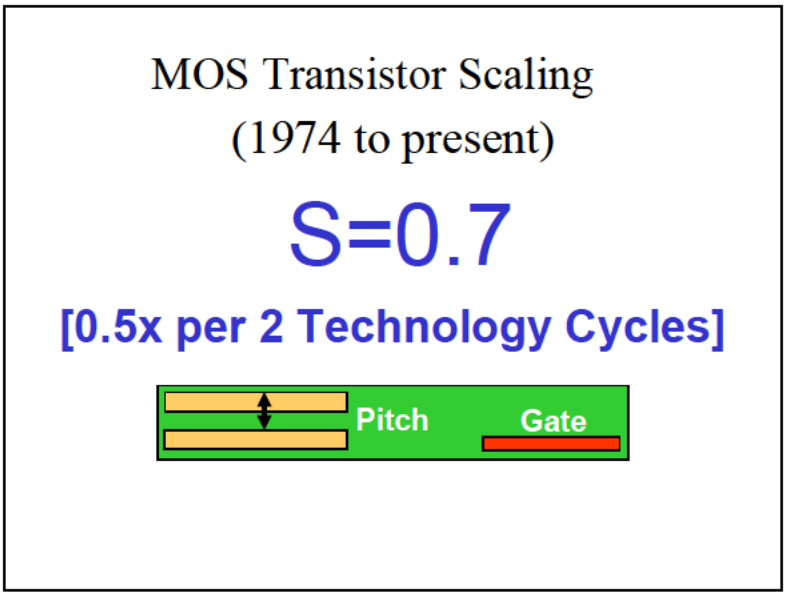


Figure 6 MOS Transistor Scaling—1974 to present

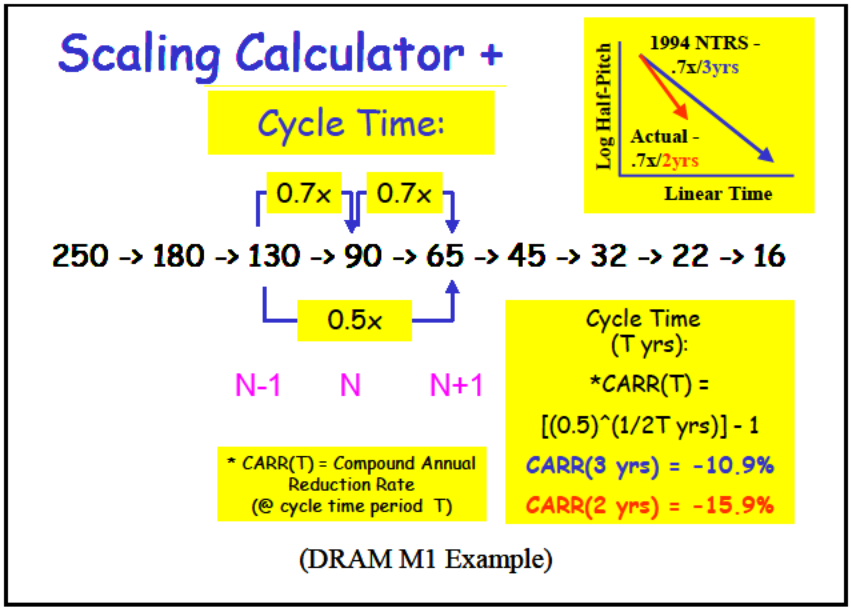


Figure 7 Scaling Calculator

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ROADMAP TIMELINE

The 2009 edition of the Roadmap maintains a 15-year projection, from 2009 as a reference year and through 2024. The timing trends of the future technology pace of the DRAM product, in past roadmaps, has represented the leading edge for stagger-contacted M1 half-pitch, and is forecast to return to the three-year cycle (three years between 0.71× reduction of the feature size) after 45 nm/2010, unchanged from the 2008 edition. In the 2008 Update, from surveys updates by the PIDS TWG, the 90 nm DRAM half-pitch began production ramp in 2005, on the completion of customer product qualification, which was made an explicit requirement of the "Production" definition for DRAM product for the 2003 ITRS.

Also based on the PIDS TWG surveys, the 2008 ITRS Table ORTC-1 DRAM product M1 half-pitch trend targets were calculated to align with an observed industry historical 2.5-year technology cycle (calculated from 180 nm/2000, 90 nm in 2005, and forecast to be 45 nm in 2010). Data provided by DRAM manufacturers suggests a three-year timing cycle (0.71× reduction) for DRAM stagger-contacted M1 half-pitch from the 2007/45 nm–2024/9 nm Roadmap period, as illustrated in Figure 8a.

Also mentioned above, the DRAM interconnect half-pitch will no longer continue to be used as a representative feature of leading-edge semiconductor manufacturing technology for defining the achievement of a technology cycle (0.71× reduction of the feature size). In fact, the Flash uncontacted polysilicon half-pitch feature is expected to continue on its 2-year cycle pace through 2010/32 nm, when it will be leading the DRAM M1 targets numerically by three years, and now is acknowledged by the Lithography ITWG to be the most leading driver of leading-edge technology manufacturing. Similarly, as mentioned, the lagging MPU and ASIC M1 stagger-contacted M1 interconnect half-pitches are running at a faster 2-year cycle pace and are presently expected to cross over the DRAM half-pitch in 2010/45 nm, and continue the 2-year pace through 2013/27 nm With the new product-oriented focus since the 2005 ITRS, all product technology trends will be monitored, and any of the product trends may accelerate further and begin to drive the industry research and the equipment and materials supplier development at the leading edge. See Figures 8a and 8b.

ROUNDED TREND NUMBERS

Using 180 nm DRAM product half pitch in the year 2000 as the calculation standard for trends, the 2009 ITRS now includes an update of the past "rounding" convention for the technology cycle trend target. The actual calculated mathematical trend data (used for model calculations in the ORTC and TWG tables) reduces by 50% every other technology cycle, resulting in actual versus rounded number targets comparison below, starting from 350 nm in 1995, as follows in Table C.

Table C Rounded versus Actual Trend Numbers (DRAM Product Trend Example)

YEAR OF PRODUCTION	1995	1998	2000	2002.5	2004	2005	2006	2007.5
Calculated Trend Numbers (nm)	**360**	**255**	**180**	**127.3**	**103.4**	**90**	**68.2**	**63.6**
ITRS Rounded Numbers (nm)	**350**	**250**	**180**	**130**	**100**	**90**	**70**	**65**

YEAR OF PRODUCTION	2009	2010	2012	2013	2015	2016	2018	2019	2022	2023	2024
Calculated Trend Numbers (nm)	**51.7**	**45**	**35.7**	**31.8**	**25.3**	**22.5**	**17.9**	**15.9**	**11.3**	**10.0**	**8.9**
ITRS Rounded Numbers (nm)	**52**	**45**	**36**	**32**	**25**	**22.5**	**17.9**	**15.9**	**11.3**	**10.0**	**8.9**

Note that the rounding corrections have become more critical as the industry moved into the two-digit data cycles of the nanotechnology (sub-100 nm) era. Please note also that some regions, for their own legacy publication consistency, will retain their right to continue to track the previous technology generations beginning with "100 nm"/2004. Starting from "100 nm" in 2004 will result in "milestones" that are targeted one year earlier than the present 2009 roadmap convention (example: 70 nm/2006; 50 nm/2009; 36 nm/2012; 25 nm/2015, etc.). By consensus of the IRC both number sets are available for long-term calculations, since the original 2001 ITRS long-term columns were retained (2010/45 nm; 2013/32 nm; 2016/22 nm), and interim columns (2012/36 nm; 2015/25 nm; 2018/18 nm; 2021/13 nm) are now annualized and included as columns. It was decided for the 2008 ITRS ORTC Update to include one decimal place of rounding accuracy after 2016 for the Table ORTC-1 header technology trend line items. The 2009 ORTC tables are now available in excel table files at www.itrs net; and even more decimal places of accuracy calculated by the models are available for the use of readers in those excel tables.

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UPDATES TO THE ORTC

The MPU/hpASIC M1 half-pitch continues to be defined as a stagger-contacted half-pitch the same as DRAM. The DRAM trend is unchanged from 2008, however the MPU/hpASIC M1 half-pitch has been revised to a lagging two-year cycle trend that crosses DRAM in 2010/45 nm, and then continues to 2013/27 nm before it turns to a three-year cycle for the balance of the roadmap period. The Flash product half-pitch continues to be defined as an uncontacted polysilicon half-pitch, and has also been revised from the 2008 ITRS by continuing the two-year cycle trend through 2010/32 nm, then turning to a three-year cycle through 2024. Refer to Figures 8a and 8b.

Due to trade-offs with "equivalent-scaling" process enhancements (copper and low-κ interconnect, strained silicon, high-K/Metal Gate, etc.), as performance and power management alternatives (see Figure 8c), the *printed* MPU and *physical* gate length trends received major corrections in the 2008 and 2009 ITRS ORTC. As described above, the physical gate length trend has been aligned with historical and survey data and is on a slower 3.8-year cycle trend beginning 2009/32 nm through 2024/7.5 nm. The printed gate length begins a delayed three-year cycle trend in 2011, and continues through 2024 on a "shrinking" ratio relationship to the physical gate length out to 2024/7.9 nm, just slightly larger than the expected final physical gate length at that time. Refer to Figure 8b.

The ORTC metrics are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to secure industry leadership. Thus, the highly competitive environment of the semiconductor industry quickly tends to make obsolete many portions of the ORTC metrics and, consequently, the Roadmap. Hopefully, the gathering and analysis of actual data, combined with the ITRS annual update process will continue to provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the ITRS to the industry.

For example, the actual data and conference papers, along with company survey data and public announcements will be re-evaluated during the year 2010 ITRS Update process, and the possibility of additional adjustments to the technology cycle in some of the individual product technology trends. As mentioned above, to reflect the variety of cycles and to allow for closer monitoring of future Roadmap trend shifts, it was agreed to continue the practice of publishing annual technology requirements from 2009 through 2016, called the "Near-term Years," and also annual requirements from 2017 through 2024, called the "Long-term years." As can be noted in Figures 8a and 8b, the Long-term years of the 2009 ITRS are somewhat aligned with the timing of the especially-challenging sub-16 nm technology era.

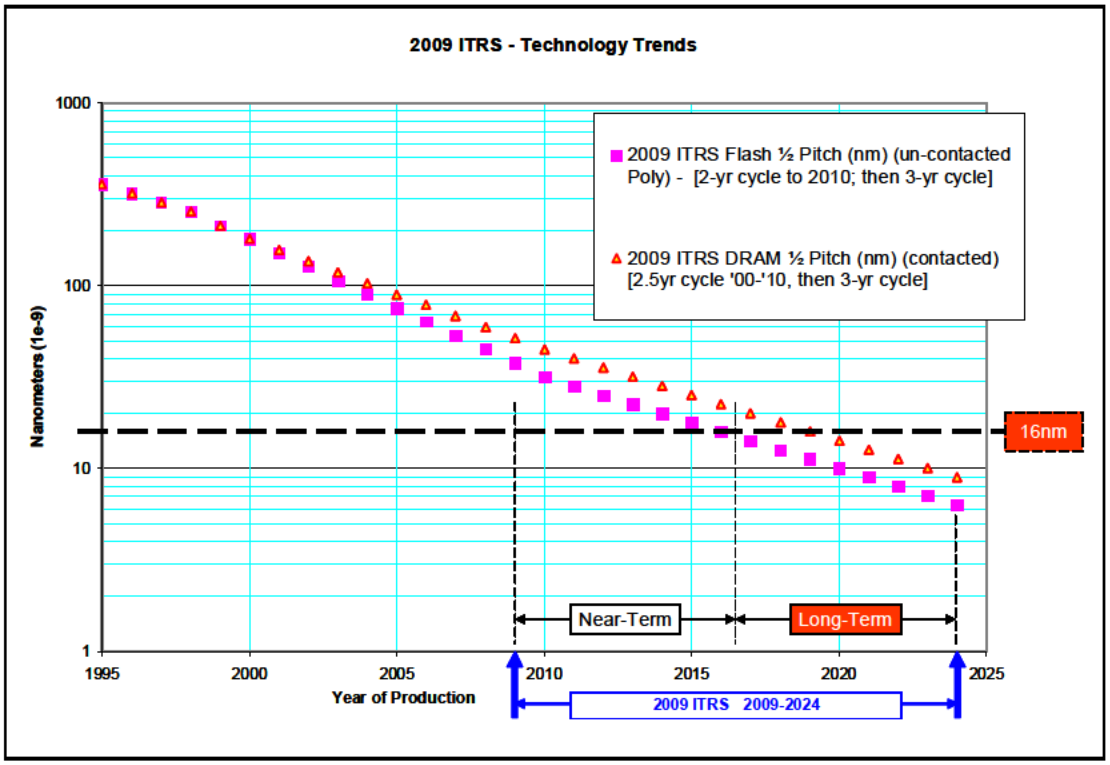


Figure 8a 2009 ITRS—DRAM and Flash Memory Half Pitch Trends

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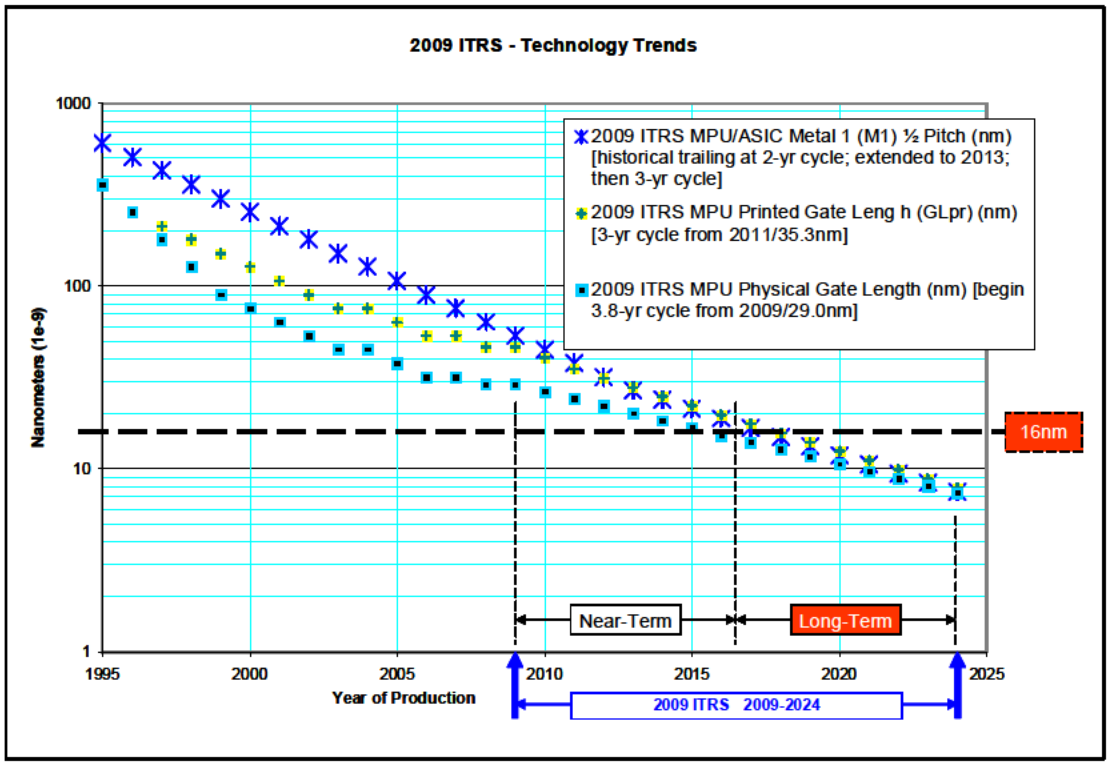
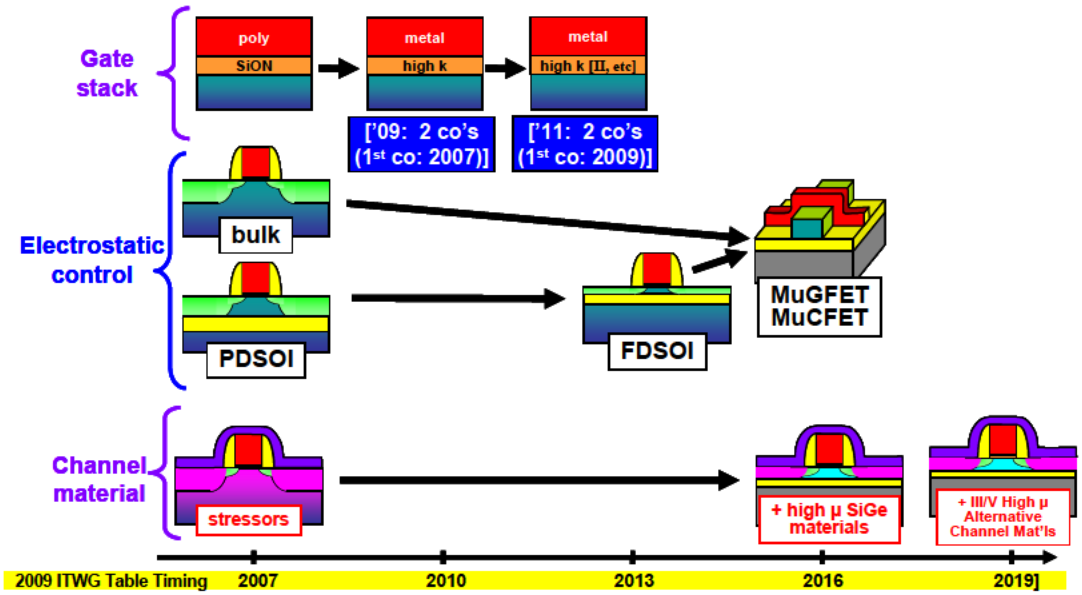


Figure 8b 2009 ITRS—MPU/high-performance ASIC Half Pitch and Gate Length Trends



(See also PIDS, FEP, ERD, and ERM chapters' text and tables for additional detail)

Figure 8c 2009 ITRS "Equivalent Scaling" Process Technologies Timing compared to ORTC MPU/high-performance ASIC Half Pitch and Gate Length Trends and Timing

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PRODUCT GENERATIONS AND CHIP-SIZE MODEL

This section discusses "product generations" and their relationship to technology cycles, since, in the past, these terms have often been used interchangeably. However, the historically simple picture of a new DRAM product generation every three years (at 4× the previous density and based on an essentially new set of technology features) has become obsolete as a way to define technology cycle timing advancement. Continuing a practice that began with the 2005 ITRS, the 2009 ITRS edition bases the technology pace drivers on individual product technology trends. These product-based technology trends may move on different paces from one another, based upon market functionality and performance and affordability needs, as the leading-edge product evolutions/shrink paths become more complex.

Historically, DRAM products have been recognized as the technology drivers for the entire semiconductor industry. Prior to the late-1990s, logic [as exemplified by MPU/high-performance ASIC (MPU/hpASIC)] technology moved at the same pace as DRAM technology, but lagged behind. The 2007 PIDS surveys of DRAM manufacturers concluded that after 2000/180 nm DRAM technology advancement was moving at an average 2.5-year. During the last few years, the development rate of new technologies used to manufacture MPU/hpASIC has continued on the 2-year pace, and is expected to continue on the 2-year pace through 2013/27 nm, while DRAM technology is presently forecast to slow to a three-year cycle pace beginning 2010/45 nm through the 2024 Roadmap horizon. By moving on the faster 2-year cycle pace, MPU/hpASIC products are closing the half-pitch technology gap with DRAM, and are expected, along with Flash technology needs, to drive the most leading-edge lithography tools and "equivalent-scaling" processes—especially for the capability to process and add power-management and performance enhancement characteristics to the isolated-line feature of the printed and physical gate length (such as etch-shaping, strained silicon, high-K/Metal Gate, etc.). As noted above, the Flash technology, as defined by uncontacted polysilicon, and has also accelerated to the point where it is now driving at the most leading edge. As mentioned, the latest Flash technology also drives the most leading lithography and the PIDS surveys forecast the Flash 2-year un-contacted poly half-pitch technology cycle pace to continue to 2010/32 nm before turning to a 3-year cycle pace through 2024.

However, several fundamental differences exist between the families of products. Due to strong commodity market economic pressure to reduce cost and increase fab output productivity, DRAM product emphasizes the minimization of the chip size. Therefore, development of DRAM technology focuses mainly on minimization of the area occupied by the memory cell. However, this pressure to minimize cell size is in conflict with the requirement to maximize the capacitance of the cell for charge storage performance, which puts pressure on memory cell designers to find creative ways through design and materials to meet minimum capacitance requirements while reducing cell size. In addition, to closely pack the highest number of DRAM cells in the smallest area requires minimization of cell pitch. The 2009 ITRS is now forecasting the insertion of new buried word and bit line cell technology, which will enable the $4f^2$ cell size beginning 2011 (4=design factor and f=half-pitch in microns).

Microprocessors have also come under strong market pressure to reduce costs while maximizing performance. Performance is enabled primarily by the length of the transistor gate and by the number of interconnect layers. The 2009 ITRS teams have reached consensus on models for the required functionality, chip size, cell area, and density for the updated ORTC tables. The MPU product chip size tables continue to be similar to the DRAM model, with large introductory chip sizes that must shrink over time to achieve the affordable sizes. Additional line items communicate the model consensus, and the underlying model assumptions are included in the ORTC table notations.

Table ORTC-1 summarizes the technology trend metrics summarized above. For completeness, the ASIC/low power gate length trends are also included, and lag behind the leading-edge MPU in order to maximize standby and operating current drain. See the Glossary section for additional detail on the definition of "equivalent-scaling," design factor, half-pitch, and gate-length features. For each product generation, both the leading-edge ("at introduction") and the high-volume ("at production") DRAM products are included.

To summarize Figures 8a and 8b, it should be noted that the long-term average annualized reduction rate of the DRAM contacted M1 half-pitch feature size is forecast to return to the three-year technology cycle pace after 2010/45 nm, which represents an approximately 11%/year (~30% reduction/three years). The previous (2000/180 nm–2010/45 nm) average 2.5year cycle rate is approximately 13%/year reduction on an annual basis (~24% reduction/two years). As noted above, the Flash memory uncontacted polysilicon is now expected to change to the three-year pace in 2010 and leads both the DRAM M1. The MPU/hpASIC M1 (generically referred to as MPU/ASIC in graphs) crosses over the DRAM M1 in 2010/45 nm, and is forecast to continue on the two-year pace through 2013/27 nm before changing to a three-year pace.

Table ORTC-1 ITRS Technology Trend Targets

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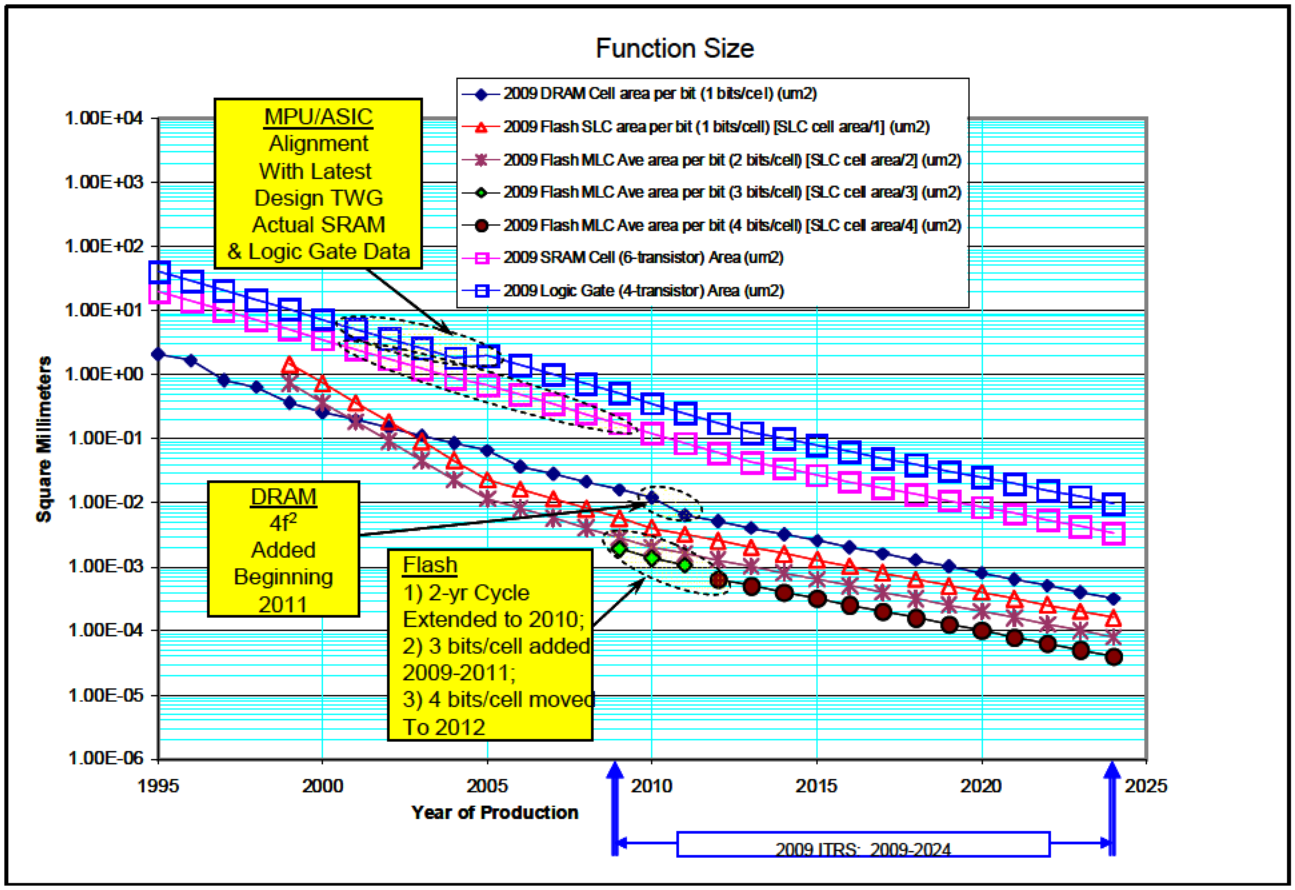


Figure 9 2009 ITRS Product Function Size Trends: MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)]

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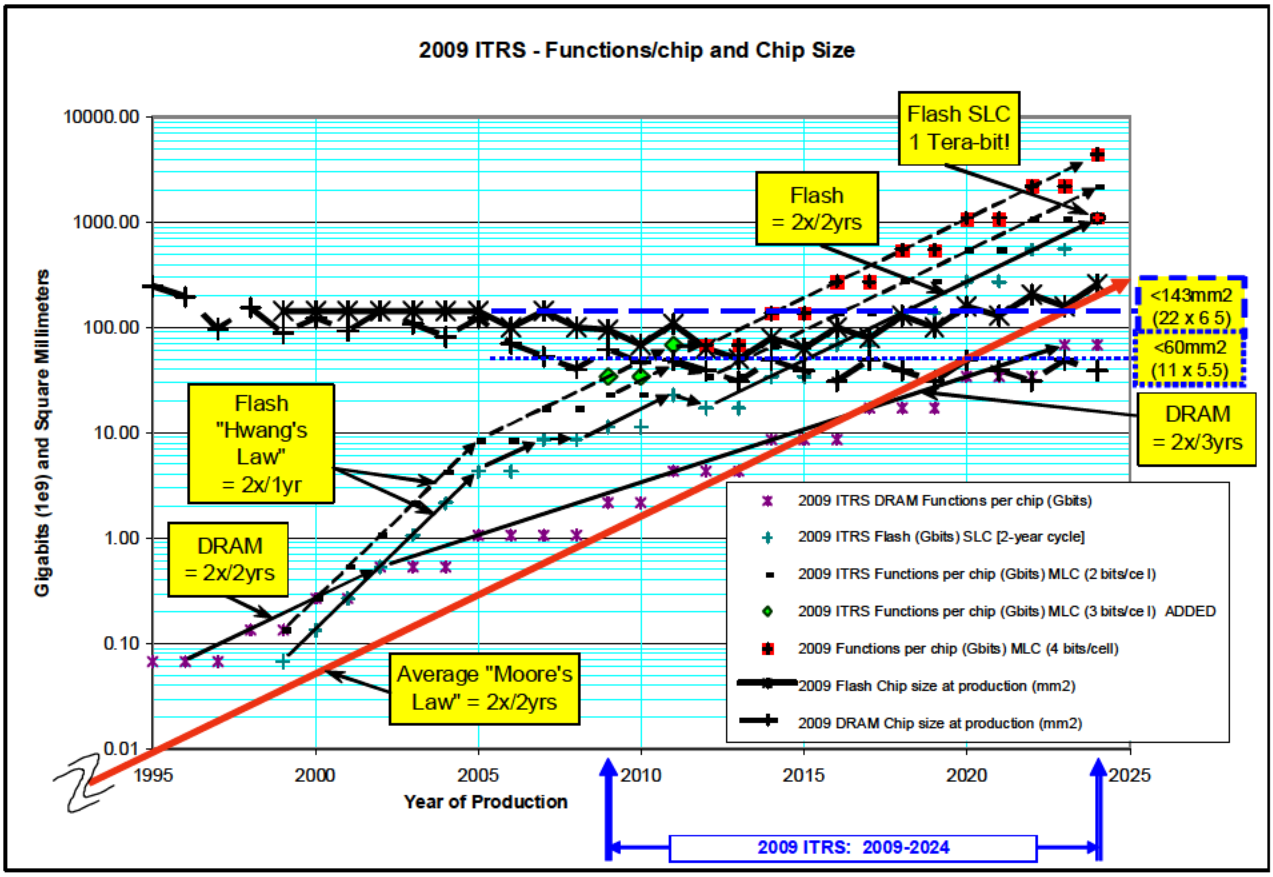


Figure 10a 2009 ITRS Product Technology Trends:
Memory Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

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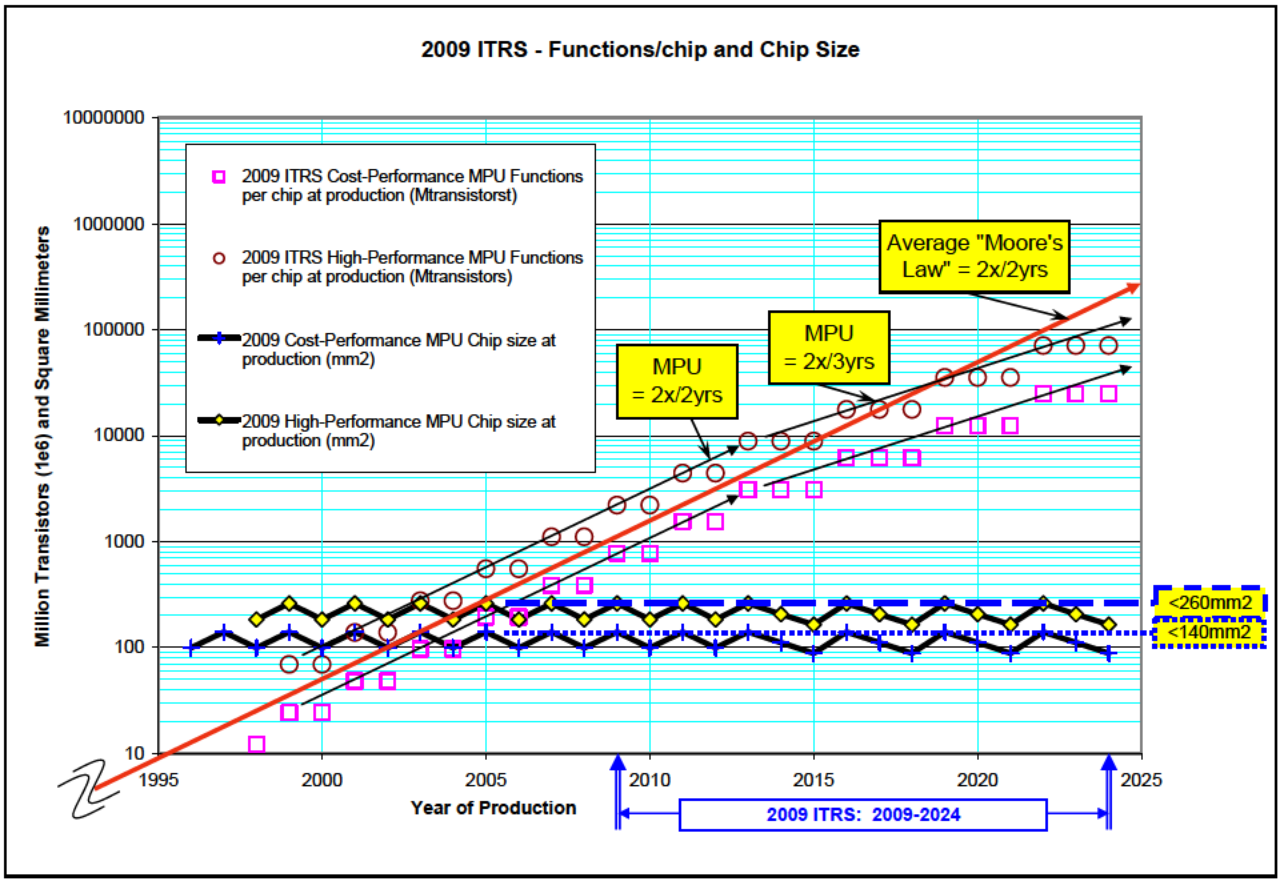


Figure 10b 2009 ITRS Product Technology Trends:
MPU Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

CHIP-SIZE, LITHOGRAPHIC-FIELD, AND WAFER-SIZE TRENDS

Despite the continuous reduction in feature size of about 30% every two to three years, the chip size of first introductory-level leading-edge memory and logic product demonstrations in technical forums such as the IEEE International Solid State Circuits Conference (ISSCC) have continued to double every six years (an increase of about 12%/year). This increase in chip area has been necessary to accommodate 40%–60% more bits/capacitors/transistors per year in accordance with Moore's Law (historically doubling functions per chip every 1.5–2 years). However, to maintain the historical trend of reducing the leading-edge product cost/function by ~30%/year, it is necessary to continuously enhance equipment productivity, increase manufacturing yields, use the largest wafer size available, maintain or increase wafer and silicon area throughput, and, most of all, increase the number of functionality (transistors, bits, logic gates) and chips available on a wafer.

The increase in the gross number of functions and chips available on a wafer is primarily obtained by reducing the area of the functions and chips by means of a combination of smaller feature size (shrink/scaling) and product/process redesign (compaction). For instance, using the latest ITRS product chip size models, it is forecast that the introduction chip area of a cost-effective product generation [which doubles the inter-generation (generation-to-generation) functionality every two years] must remain as flat as possible. Furthermore, the area must be shrunk at an intra-generation (within a generation) annual reduction rate of 50% (the square of the .7× lithography reduction rate) during every technology cycle period, or faster when additional design-factor-related density improvement is available.

In order for affordable DRAM and Flash memory products to achieve virtually flat intra-generation chip-sizes, they must also maintain a cell area array efficiency ratio of 58–63% of total chip area. Historically, DRAM and Flash memory products have required reduction of cell area design factors (a) (cell area (Ca) in units of minimum-feature size (f) squared; $Ca = af^2$). The PIDS and FEP ITWGs have provided member survey data for the array efficiency targets, the cell area factors, and bits per chip. In addition, detailed challenges and needs for solutions to meet the aggressive cell area

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goals are documented in the Front End Processes chapter. Due to the importance of tracking/coordinating these new challenges, the DRAM and Flash memory cell area factors, the target cell sizes, and the cell array area percentage of total chip-size line items will continue to be tracked in Tables ORTC-2A and 2B. (Also refer to the Glossary for additional details).

Table ORTC-2A DRAM and Flash Production Product Generations and Chip Size Model

Table ORTC-2B DRAM Introduction Product Generations and Chip Size Model

Notably, the most recent survey data and publicly available announcements indicate that reduction rate of DRAM cell area factors for the 2009 ITRS models will accelerate, placing the $4f^2$ area factor in 2011 (versus the flat $6f^2$ area factor in the 2005 ITRS). Beginning 2011 the area factor is expected to remain flat at $4f^2$ through the 2024 ITRS horizon. In addition to the $4f^2$ factor insertion, the survey extends the 56% array efficiency from 2006 to the roadmap horizon in 2024. These gains in DRAM cell design efficiency and function density were traded off against a lower targeted production chip sizes, which are now targeted for production sizes to be below $60mm^2$. Therefore, the DRAM "Moore's Law" bits per chip targets have been delayed by one year, and continue to target 2× every three years in both the near term and long term. The 64 Gbit DRAM product now sits at the ITRS year 2023 horizon (refer to Function Size and Functions per Chip in Figures 9, 10a and 10b).

In the updated 2009 ORTC Flash product model, the function bit size is still calculated based upon the single-level cell (SLC) design factor and the also the critical feature scaling of the uncontacted polysilicon dense lines. The 2009 PIDS Flash survey indicated that the rapid 2-year scaling cycle now is expected to continue through 2010; however, the single-level-cell physical design factor limit remains at 4. Therefore, the Flash model function (bit size) area reduction has accelerated, and the Flash uncontacted polysilicon half-pitch will numerically lead the DRAM stagger-contacted M1 half-pitch by three years. The Lithography TWG now believes that leading-edge Flash manufacturing technology is clearly driving the most-leading-edge manufacturing, which also uses comparable processing equipment to manufacture leading-edge DRAM products.

Flash SLC bit technology was thus able to drive quickly to a 76 nm uncontacted polysilicon half-pitch and a "4" design factor in 2005; and is expected to continue the scaling reduction to 32 nm in 2010, reducing SLC bit size to 0.004 um^2, one third the size of a DRAM cell that year (see Figure 9, 2005 ITRS Product Function Size Trends). This continued acceleration of Flash technology will enable the production of a 96 mm^2 11 Gbit SLC product in 2009, when DRAM product is still at 2 Gbit (however, is only $61mm^2$ to meet demanding market affordability and productivity requirements). Furthermore, Flash technology is able to create an electrical doubling of bits (multi-level-cell, or MLC) in the same area, resulting in a virtual doubling of bits per chip to 22 Gbits in the $96mm^2$ affordable first production chip size range. The PIDS Flash survey has also added a three-bits-per-chip MLC product beginning 2009, enabling the more difficult quad-bit MLC to shift to 2012 production.

By recommending the most dramatic changes since the 2001 ITRS, the Design ITWG has improved the MPU chip size model to update with the latest transistor densities, large on-chip SRAM, and smaller target chip sizes. The Design ITWG added additional detail to the model, including new transistor design improvement factors. The new Design ITWG model utilizes a 60 design factor (significantly down from over 100 in previous roadmaps), in SRAM transistors, and is no longer expected to slowly improve over time. The logic gate transistor design factor was also dramatically reduced from over 300 to 175, and is also expected to remain flat throughout the roadmap period. Barring any significant changes in array efficiencies (the only other variable affecting the chip size models), the "shrink" and density improvements will continue to come from lithography-enabled interconnect half-pitch scaling.

The present 2009 ITRS MPU model ties to historical data by lagging an M1 half-pitch data trend on a two-year cycle trend, which crosses over the DRAM M1 half-pitch in 2010/45 nm, and then continues on the two-year cycle to 2013/27 nm before turning to a three-year cycle parallel to both DRAM M1 and Flash Poly half-pitch trends. The technology dimension and design factor model is significantly revised from past ITRS roadmaps, but still continues to reflect the competitive requirements for affordability by targeting flat chip size trends for both high-performance MPUs (now lowered to $260mm^2$) and cost-performance MPUs (still 140 mm^2).

Due to the MPU two-year-cycle half-pitch "catch-up-and cross-over phase" through the year 2013, the MPU products are targeted to maintain flat chip sizes due to lithography improvements alone. However, after 2013, the inter-generation

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MPU chip size model can remain flat only by slowing the rate of on-chip transistors to double every technology generation (3-year cycle after 2013).

In the 2009 ITRS, the MPU model continues to use the approach of doubling the logic cores only every other technology cycle. However, function size and density of the core was kept unchanged by doubling the transistors per core targets. The Design ITWG consensus opinion is that this approach to the MPU Model is more representative of current design trends. Refer to Function Size and Functions per Chip in Figures 9, 10a and 10b.

Due to the latest forecast extension of the MPU M1 half-pitch two-year technology cycle, the present MPU chip-size model can continue the historical Moore's Law doubling of on-chip functionality (transistors) until the 2013/27 nm point. After 2013, the Moore's Law rate of on-chip transistors slows to 2× every three years, to match the slower 3-year technology cycle (in order to maintain flat chip size targets). To keep the effective historical functional productivity on track after the 2013 point, MPU chip and process designers must add even more "equivalent scaling " design/process improvements to the designs to enhance the improvements provided by the fundamental lithography-based scaling trends. The new target metrics of the MPU model are summarized in Tables ORTC-2C and 2D.

Table ORTC-2C MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model

Table ORTC-2D High-Performance MPU and ASIC Product Generations and Chip Size Model

To improve productivity, it is necessary to increase the output of good chips at each step in the fabrication process. The ability of printing multiple chips in a single exposure is a key productivity driver and is determined by the field size of the lithographic tool and the size and aspect ratio of the chips being printed on the wafer. In the past, lithography exposure field sizes doubled every other technology to meet the demand for increasing maximum introduction-level chip sizes. The result was the achievement of very large step-and-scan fields (26×33 = 858 mm^2).

However, the Lithography ITWG indicates that maintaining the large field size under continued reduction of exposure features is increasing costs dramatically. Therefore, the Lithography ITWG limits the absolute maximum field size at 858 mm^2 and allows the individual memory and logic product chip size surveys and models to drive the requirements up to the absolute maximum field size and also the more typical affordable field size ranges.

DRAM chip sizes have historically been the driver of both the most difficult half-pitch exposures and also the affordable lithography field size range. In the 2009 ITRS chip-size model for DRAMs, the introduction-level chip size is targeted to be smaller than a 750 mm^2 lithography field size well under the 858mm^2 maximum, and fitting at least one introduction-level chip size within that field size. The latest 2009 ITRS production-level DRAM chip size model (less than 60 mm^2 flat target) fits nine die within a 572 mm^2 field.

The combination of technology generation scaling and cell design improvements (including the new $4f^2$ A-factor reduction from $6f^2$ in the 2007 ITRS) accomplishes that goal, while also allowing a goal of doubling on-chip bits to a slower 3-year cycle. As mentioned in the product chip size model discussions above, the 2011 accelerated DRAM design improvement to 4, and the new 60mm2 affordable production chip size target, caused a requirement to add fewer on-chip bits to stay under the affordable chip size and lithography field size. This was accomplished in the present DRAM model by delaying the production bits/chip generations by 1 year, and continuing the slower Moore's Law bits/chip rate at 2×/ three years to the end of the roadmap period. The data targets for the DRAM model are included in Tables ORTC-2A and 2B.

The Flash production chip size model is also included in those tables, and still targets the Flash maximum affordable chip size at 143 mm^2, while continuing to target the doubling of Flash bits per chip every two years. Due to the extension of 2-year technology cycles to 2010/32 nm poly half pitch processing, plus the addition of 3bits/chip and 4bits/chip multi-level cell (MLC) devices, the Flash product chip sizes remain below 143mm^2 through 2021. In 2022, the chip size hits the industry maximum affordable 200mm^2 limit, and may require adjustment of the Flash bits per chip model in future ITRS work.

The absolute maximum lithography field size is driven by the early introduction level chip sizes of high-performance MPUs and ASICs, which approach the maximum practical field size available from the Lithography TWG (26 × 33 =

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858 mm^2). It is anticipated that future mask magnification levels as high as 8× may reduce the maximum field size to one-fourth the present 858 $mm^{2,}$ reducing the maximum available area to less than 214 mm^2. The details surrounding the limitations of maximum field size and the mask magnification issue are provided by the Lithography TWG in their chapter. The maximum Lithography field size targets are shown in Table ORTC-3, and are unchanged from the 2007 ITRS targets.

Table ORTC-3 Lithographic-Field and Wafer Size Trends

The 2009 ITRS DRAM, MPU and Flash models depend upon achieving the aggressive DRAM, MPU, and Flash design and process improvement targets. If those targets slip, then pressure will increase to print chip sizes larger than the present roadmap, or further slow the rate of "Moore's-Law" on-chip functionality. Either of these consequences will result in a negative impact upon cost-per-function reduction rates—the classical measure of our industry's productivity-improvement and competitiveness.

With increasing cost-reduction pressures, the need for upgrading 200mm manufacturing to 300 mm productivity boost (and also continuous improvement of the productivity of fabs) has increased in urgency more than ever, especially for leading-edge independent and foundry manufacturers. However, the poor economy, especially the most recent global recession, has created financial challenges and limited capital investment. The maximum substrate diameter in Table ORTC-3 (and in additional detail in the FEP chapter) is consistent with the ramp of 300 mm capacity, which began in 2001, and has now achieved 50 per cent of the industry silicon area capacity.

The challenging economy has also affected the investment into, and the timing of, the incremental productivity boost expected from the first manufacturing capability for the next 1.5× wafer size conversion to 450 mm diameter (as described in the 450 mm section of the Executive Summary above). Therefore the availability of the 450 mm productivity boost has been re-targeted by the ITRS executive steering committee (IRC) for 32 nm (M1 half-pitch processing measured) pilot-line capability in 2012, with 22 nm production ramps anticipated by leading microprocessor, memory, and foundry companies to be required 2014-2016.

However, should the other productivity-improvement drivers (lithography and design/process improvements) fail to stay on schedule, there would be a need to accelerate the use of increased wafer diameter, or other equivalent processing solutions, to drive productivity improvement.

The effects of future technology acceleration/deceleration and the timing of the next wafer generation conversion require the development and application of comprehensive long-range factory productivity and industry economic models. Such industry economic modeling (IEM) work continues to be sponsored and carried out jointly by Semiconductor Equipment and Materials International (SEMI) and SEMATECH. Most certainly, pre-competitive cooperation between the semiconductor supplier and manufacturer companies will be required to define the future technical and economic needs and to identify appropriate funding mechanisms for the required research and development.

PERFORMANCE OF PACKAGED CHIPS

NUMBER OF PADS AND PINS / PAD PITCH, COST PER PIN, FREQUENCY

The demand for a higher number of functions on a single chip requires the integration of an increased number of transistors or bits (memory cells) for each product generation. Typically, the number of pads and pins necessary to allow Input/Output (I/O) signals to flow to and from an integrated circuit increases as the number of transistors on a chip increases. (Refer to Table ORTC-4).

Additional power and ground connections to the chip are also necessary to optimize power management and to increase noise immunity. MPU and high-performance ASIC products approach 3–7K pads over the ITRS period. The MPU products are forecast to increase the total number of pads through this period by nearly 50%, and the ASICs double the maximum number of pads per chip. The two product types also differ significantly in the ratio of power/ground pads. The MPU product pad counts typically have 1:3 signal I/O pads and 2:3 power and ground pads, or two power/ground pads for every signal I/O pad. Unlike MPUs, high-performance ASIC product pad counts typically include one power/ground pad for each signal I/O pad.

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Table ORTC-4 Performance and Packaged Chips Trends

Package pin count and cost-per-pin (Table ORTC-4), provided by the Assembly and Packaging ITWG, point out challenges to future manufacturing economics. Based upon the projected growth in the number of transistors/chip, it is forecast that the number of package pin/balls will continue to grow, while the cost/pin decreases. These trends make it more challenging for suppliers of packaging technologies to deliver cost-effective solutions, because the overall average cost of packaging will increase annually.

In the very competitive consumer electronics product environment (which is a focus end-product segment for characterizing Design and System-Driver Chapter Grand Challenges and Potential Solutions), prices for high-volume, high-tech products such as PCs and cell phones tend to remain flat or even decrease. These same high-tech products typically also deliver twice the performance every two years. This is the end-use market environment of the leading-edge semiconductor manufacturer, and it is the fundamental economic driver behind the ITRS economic requirement to reduce cost per function (bits, transistors) at an annual 30% or faster rate (2× functionality/chip at flat price every two years = 29%/year).

If future semiconductor component products must be targeted to maintain constant or decreasing prices and the average number of pins per unit increases while the average cost per pin decreases, then: the average packaging share of total product cost will continue to increase over the 15-year roadmap period; and the ultimate result will be greatly reduced gross profit margins and limited ability to invest in R&D and factory capacity.

This conclusion is one of the drivers behind the industry trends to reduce the overall system pin requirements by combining functionality into systems-on-chip (SOC) and through the use of multi-chip modules (System-in-Package, i.e., SiP), bumped chip-on-board (COB), and other creative solutions.

In addition to the need to increase functionality while exponentially decreasing cost per function, there is also a market demand for higher-performance, cost-effective products. Just as Moore's Law predicts that functions-per-chip will double every 1.5–2 years to keep up with consumer demand, there is a corresponding demand for processing electrical signals at progressively higher rates. In the case of MPUs, processor instructions/second have also historically doubled every 1.5–2 years. However, beginning in earlier roadmaps and continued in the latest 2009 ITRS, historical and forecast trends are suggesting a significant slowing in the rate of increase of on-chip frequency, to approximately only 8% growth per year or less. Performance increases accomplished historically by geometrical scaling (refer to Glossary) are now being provided through process "equivalent scaling" and also design-related "equivalent scaling" (see new definition updates in the Glossary) architecture and software improvements that enable the continued delivery of SOC, SIP, and system-level performance to customers while keeping power management under control.

For MPU products, increased processing power, measured in millions of instructions per second (MIPs), is accomplished through a combination of "raw technology performance" (clock frequency) multiplied by "architectural performance" (instructions per clock cycle). The need for a progressively higher operational performance will continue to demand the development of novel process, design, and packaging techniques.

These considerations are reflected in Table ORTC-4, which include line items contributed by the Design TWG to forecast the maximum on-chip trends. The highest frequency obtainable in each product generation is directly related to the intrinsic transistor performance (on-chip, local clock). The difference between this "local" frequency and the frequency of signals traveling across the chip increases due to degradation of signal propagation delay caused by line-to-line and line-to-substrate capacitive coupling. Additional signal degradation is associated with the inductance of wire bonds and package leads. Direct chip attachment may eventually be the only viable way to eliminate any parasitic effect introduced by the package. To optimize signal and power distribution across the chip, it is expected that the number of layers of interconnect will continue to increase. As size downscaling of interconnect also continues, wider use of copper (low resistivity) and various inter-metal insulating materials of progressively lower dielectric constant will be adopted in the chip fabrication process. Multiplexing techniques will also be used to increase the chip-to-board operating frequency (off-chip – see the A&P chapter for details).

ELECTRICAL DEFECT DENSITY

The latest targets for electrical defect density of DRAM, MPU, and ASIC (necessary to achieve 83–89.5 % chip yield in the year of volume production) are shown in Table ORTC-5. The allowable number of defects is calculated by taking into account the different chip sizes based on the latest chip size model forecasts, as reported in Table 2 for DRAM and microprocessors. In addition, the data in the table are reported only at the production-level of the product life-cycle. Other defect densities may be calculated at different chip sizes at the same technology by using the formula found in the Yield

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Enhancement chapter. The approximate number of masks for logic devices is included as an indicator of the ever-increasing process complexity, and work in underway in 2009 by the Lithography TWG to survey companies and revise the targets for the 2010 update.

Table ORTC-5 Electrical Defects

POWER SUPPLY AND POWER DISSIPATION

The reduction of power supply voltage is driven by several factors—reduction of power dissipation, reduced transistor channel length, and reliability of gate dielectrics. As seen in Table 6, the value of the power supply voltage is now given as specific target, rather than a range.

Selection of a specific V_{dd} value continues to be a part of the analysis undertaken to simultaneously optimize speed and power for an IC, leading to a range of usable power supply voltages in each product generation. Values of V_{dd} as low as 0.6 volts are not expected to be achieved by high-performance processors until 2024. . The lowest V_{dd} target is still 0.6V in 2021 for the low operating power applications, and is not expected to drop below that level out to 2024.

Maximum power trends (e.g., for MPUs) are presented in three categories—1) high-performance desktop applications, for which a heat sink on the package is permitted; 2) cost-performance, where economical power management solutions of the highest performance are most important; and 3) portable (low-cost, hand-held) battery operations. In all cases, total power consumption targets are relatively flat in the 2009 Table ORTC-6, despite the use of a lower supply voltage. The power consumption is driven by higher chip operating frequencies, the higher interconnect overall capacitance and resistance, and the increasing gate leakage of exponentially growing and scaled on-chip transistors.

The approach for calculating maximum power targets is being re-evaluated in 2009, and the 2010 roadmap update calculation models from the Design and Assembly and Packaging (A&P) ITWGs are expected to take into account specific "hot-spot" area calculations rather than the overall chip area.

Table ORTC-6 Power Supply and Power Dissipation

COST

Table ORTC-7 is dedicated to cost trends. The historical ability to reduce the leading-edge product manufacturing cost per function by an average 29% each year (0.5× per 2 years) has represented one of the unique features of the semiconductor industry and is a direct consequence of the market pressure to continue to deliver twice the functionality on-chip every 1.5–2 years in an environment of constant or reducing prices. In support of this market cost reduction mandate, a continuously increasing amount of investment is needed for R&D and manufacturing capital. Even on a per-factory basis, the capital cost of manufacturing continues to escalate. Yet, the semiconductor industry has historically delivered two times as many functions per chip every 1.5–2 years with an approximately constant cost per cm2 of silicon. This technological and economic performance is the fundamental engine behind the growth of the semiconductor industry.

However, the customers in today's challenging economic and competitive market environment continue to resist even moderate increases in per unit cost, maintaining the pressure upon the semiconductor industry to slow the rate of doubling functions per chip (Moore's Law) in order to keep chip and unit costs under control. The semiconductor manufacturers had to seek a new model to deliver the same cost-per-function reduction requirements that have fueled industry growth. Consequently, the 1999 ITRS proposed a new model for achieving the required reduction: provide the customer twice the functionality every two years at constant cost targets. The 2001 and 2003, 2005, 2007 and now the 2009 ITRS models *all continue to use that idealized and simplistic model*, which results in 29% cost reduction of a function (bit, transistor, etc.). Note that the 29% average rate of function cost reduction was achieved historically (prior to 1999) by delivering four times the functionality per chip every three years at 1.4× increase in cost per unit.

The 2009 ITRS DRAM and MPU cost models continue to use the need for that average 29% cost-per-function productivity reduction rate as an economic driver of the industry. Therefore, that cost-per-function trend has been used to set the INTRA-generation trends for the affordable cost/bit and cost/transistor for DRAM and microprocessors, respectively. Extrapolation of historical trends would indicate an "at introduction" affordable cost/bit of 1.3 microcents for DRAMs in 2009. In addition, the historical trends indicate that, within a DRAM generation, a 45%/year reduction in

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cost/bit should be expected.[3] A corresponding analysis conducted from published data for microprocessors provides similar results.[4] Therefore, the 29%/year target for reduction in affordable cost/transistor from generation to generation is also being used in the MPU model, along with the 45%/year reduction rate within the same generation.

The 2009 ITRS has significantly revised the MPU chip size model. The Design ITWG has updated the MPU model in the 2009 ITRS, based upon their most recent available data and models. The new data and model indicate that logic transistor size is improving at the rate of the lithography (0.7× linear, 0.5× area reduction every technology cycle). Therefore, in order to keep the MPU chip sizes flat to the 140mm2 target, the number of transistors can be doubled only every technology cycle. The technology cycle rate is projected to be on a 2-year cycle through 45 nm/2010, and turn to a three-year cycle after 2010. Therefore the transistors per MPU chip can double only every three years after 2013, unless increased chip size is allowed for specific applications which have markets that can afford the higher costs.

DRAM memory bit cell design improvements is expected to accelerate, as reflected in the 2009 ITRS DRAM Chip Size Model targets (see Table ORTC-2). The "4" design factor, a 33% improvement over the "6" factor, is now expected to be implemented in 2011, accelerating incrementally the long-range cost-reduction productivity. Furthermore, the latest PIDS TWG survey of DRAM manufacturers has indicated that the target for the cell array efficiency percentage achieved 56% after 2006 is expected to continue through the roadmap horizon, 2024. The recent model changes, along with the new goal of a more affordable starting production chip size (less than 60mm2 versus previous 100mm2) has delayed the bits/chip increase rate of DRAM by one year, while continuing the increase rate of bits per chip at 2×/3 years. These DRAM model changes have pushed the 64 Gbit generation (introduction in 2013) to 2023 for production and moved the 128 Gbit DRAM (introduction 2016) beyond even the present 2024 ITRS horizon. .

To compensate for slowing DRAM and MPU (after 2013) functions-per-chip, there will be increasing pressure to find alternative productivity enhancements from the "equivalent" productivity scaling benefits of chip, package, board, and system-level architecture and designs.

Even though the rate of increase of on-chip functionality could slow in the future, the amount of functions/chip is still growing exponentially. As the number of functions/chip continues to increase, it becomes increasingly difficult and, therefore, costly to test the final products. This issue is reflected in the escalating cost of testers. The number of tested pins (see Table ORTC4) is also increasing, which adds to the cost of the tester as well as the associated material and custom test fixtures that increase the total cost of ownership. Therefore, there will be an ongoing need for accelerated implementation of built-in-self-test and design-for-testability and design-for-manufacturability techniques within the time frame of the 2009 ITRS. Further discussion is detailed in the Test and Test Equipment chapter.

Table ORTC-7 Cost

[3] *McClean, William J., ed. Mid-Term 1994: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1994.*
McClean, William J., ed. Mid-Term 1995: Status and Forecast of the IC Industry. Scottsdale: Integrated Circuit Engineering Corporation, 1995.

[4] *a) Dataquest Incorporated. x86 Market: Detailed Forecast, Assumptions, and Trends. MCRO–WW–MT–9501. San Jose: Dataquest Incorporated, January 16, 1995.*
b) Port, Otis; Reinhardt, Andy; McWilliams, Gary; and Brull, Steven V. "The Silicon Age? It's Just Dawning," Table 1. Business Week, December 9, 1996, 148–152.

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GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (ALSO WITH OBSERVATIONS AND ANALYSIS)

PLEASE NOTE THAT THE 2009 ITRS GLOSSARY INCLUDES NEW DEFINITION ADDITIONS AND UPDATES.

Moore's Law—An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that device affordability must be taken into account and also performance. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been recently acknowledged and celebrated as a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 40 years.

Scaling ("More Moore")—

- *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)* refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)* refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
    - "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures."
    - Addresses the need for quantifiable, specific Design Technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs, and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—The incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

- Design technologies enable new functionality that takes advantage of More than Moore technologies.
- "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology."
- Addresses the need for design technologies which enable functional diversification

Beyond CMOS—emerging research devices, focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switch, NEMS switches, etc.

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CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets.

MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

As defined above, additional "Equivalent Scaling" process technologies can be combined with transistor gate dimensional scaling technology advancement to further advance the performance and power-management characteristics of a device. The "Equivalent Scaling" technologies can also be "mix-and-matched" by companies within their specific product fabs. In some cases the most recent ITRS TWG surveys have indicated that dimensional scaling (both gate length and gate material thickness) reduction can be slowed and still meet power management and performance requirements, when traded off with "equivalent scaling" process insertion.

Some (not comprehensive or complete) examples of "equivalent scaling" process and transistor design technology are: copper interconnect; low-K interconnect materials; strained silicon; high-K/metal gate; fully depleted silicon-on-insulator (FDSOI); multiple-gate 3-D transistors, III-V gate material; etc.

It should be noted that the timing of availability and implementation of "equivalent scaling" process insertion may not be as regular as dimensional cycles. See the Interconnect and process integration and device structures (PIDS) chapters for additional technology description and timing details.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to the "Moore's Law" driver of functions/chip doubling every two years , there has been a historically-based "corollary" to the "law," which suggests that, to be affordable and competitive, manufacturing productivity improvements must also enable the cost-per-function (micro-cents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 2 years, cost per function must also reduce by half every 2 years (-29%/year average). On average then cost-per-chip (packaged unit) , for affordability, could remain approximately constant (requires both flat chip cost targets and flat back-end packaging targets to remain constant), If functionality doubles only every three years, then the manufacturing cost per chip (packaged unit) can remain flat if the cost per function reduction rate slows to one-half every 3 years.(-21%/year average). It should be noted that this simplistic manufacturing cost affordability model, used as a first-order driver for the ITRS, does not take into account the economic supply and demand market complexity of actual external market environments.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

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DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A Flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two to four bits of data in the same physical area.

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two and level-three (L2 and L3) cache. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation.

High-performance MPU[5]—MPU product optimized for maximum system performance by combining a single or multiple CPU cores with large level-two and level-3 (L2 and L3) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory. Recently the typical pattern among MPU products is to keep the number of cores constant within a generation and double the number of transistors within each core, and the latest ITRS ORTC modeling reflects this trend in the table targets.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip had increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is still maintained, although the latest consensus ITRS forecast of cell-area-factor improvement to 4 by 2011, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate. Therefore, the latest ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The latest ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology generation processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology generation, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples.

Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2005 Production-level targets.

[5] *Note: The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.*

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Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (typically <1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, 10K/month or higher, depending upon die size and wafer generation size) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 2a in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: .5 Gb/production, 4 G/introduction, plus 256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2009 ITRS, the typical high-performance ASIC (hpASIC) design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 74% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 56% at the production level, and also for shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

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Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=74% of total chip area, the $C_{AVE} = C/E = 0.35\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.35e-6 mm^2/bit = 376 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two to four bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half to one-fourth the size of an SLC product cell size and will also have a "virtual area factor" that is half to one-fourth of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 10–15 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2–3 times greater than an SRAM 6t cell area factor, and 30–40 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology generation. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology generation. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

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Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology generation, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first production-qualified development manufacturing facilities. Additional clarification was added by the IRC in 2009 to differentiate the new 450 mm wafer generation early consortia pilot line equipment readiness from the timing of anticipated production readiness and ramp.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

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FOLDER 15

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2009 EDITION

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

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PROCESS INTEGRATION, DEVICES, AND STRUCTURES

SCOPE

The *Process Integration, Devices, and Structures (PIDS)* chapter deals with the main IC devices and structures, with overall IC process-flow integration, and with the reliability tradeoffs associated with new options. Physical and electrical requirements and characteristics are emphasized within PIDS, encompassing parameters such as physical dimensions, key device electrical parameters, including device electrical performance and leakage, and reliability criteria. The focus is on nominal targets, although statistical tolerances are discussed as well. Key technical challenges facing the industry in this area are addressed, and some of the best-known potential solutions to these challenges are discussed. The chapter is subdivided into the following major subsections: logic, memory (including both DRAM and non-volatile memory [NVM]), and reliability.

The main aims of the ITRS include identifying key technical requirements and challenges critical to sustaining the historical scaling of CMOS technology per Moore's Law and stimulating the needed research and development to meet the key challenges. The objective of listing and discussing potential solutions in this chapter is to provide the best current guidance about approaches that address the key technical challenges. However, the potential-solution list here is not comprehensive, nor are the solutions in the list necessarily the most optimal ones. Given these limitations, the potential solutions in the ITRS are meant to stimulate but not limit research exploring new and different approaches.

LOGIC

A major portion of semiconductor device production is devoted to digital logic. In this section, both high-performance logic and low-power logic, which is typically for mobile applications, are included and detailed technology requirements and potential solutions are considered for both types separately. Key considerations are performance, power, and density requirements and goals. One key theme is continued scaling of the MOSFETs for leading-edge logic technology in order to maintain historical trends of improved device performance. This scaling is driving the industry toward a number of major technological innovations, including material and process changes such as high-κ gate dielectric, metal gate electrodes, strain enhancement, etc., and in the long term, new structures such as ultra-thin body and multi-gate (MG) MOSFETs (such as FinFETs). These innovations are expected to be introduced at a rapid pace, and hence understanding, modeling, and implementing them into manufacturing in a timely manner is expected to be a major issue for the industry.

MEMORY

Logic and memory together form the predominant majority of semiconductor device production. The types of memory considered in this chapter are DRAM and non-volatile memory (NVM). The emphasis is on commodity, stand-alone chips, since those chips tend to drive the memory technology. However, embedded memory chips are expected to follow the same trends as the commodity memory chips, usually with some time lag. For both DRAM and NVM, detailed technology requirements and potential solutions are considered

The NVM discussion in this chapter is limited to devices that can be written and read many times; hence read-only memory (ROM) and one-time-programmable (OTP) memory are excluded. The current mainstream of NVM is Flash, for both NAND and NOR architectures. There are serious issues with scaling that are dealt with at some length in the chapter. Other non-charge-storage types of NVM are also considered, including ferroelectric RAM (FeRAM), magnetic RAM (MRAM), and phase-change RAM. For DRAM, the key issue is dealing with increasing scaling difficulties, especially with ensuring very low levels of leakage.

RELIABILITY

Reliability is a critical aspect of process integration. Emerging technology generations require the introduction of new materials and processes at a rate that exceeds current capabilities for gathering and generating the required database to ensure product reliability. Consequently, process integration is often performed without the benefit of extended learning, which will make it difficult to maintain current reliability levels. Uncertainties in reliability can lead to performance, cost, and time-to-market penalties. Insufficient reliability margin can lead to field failures that are costly to fix and damaging to reputation. These issues place difficult challenges on testing and reliability modeling. This chapter emphasizes mostly front-end (transistor) reliability issues. The goal is to identify the challenges that are in need of significant research and development.

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DIFFICULT CHALLENGES

Table PIDS1 Process Integration Difficult Challenges

Difficult Challenges for $L_g \geq 16$ nm	*Summary of Issues*
1. Scaling of logic MOSFETs	Scaling planar bulk CMOS Implementation of fully depleted SOI and multi-gate (MG) structures Controlling source/drain series resistance within tolerable limits Further scaling of EOT with higher κ materials (κ > 30) Threshold voltage tuning and control with metal gate and high-κ stack Inducing adequate strain
2. Scaling of DRAM and SRAM	DRAM— Adequate storage capacitance with reduced feature size; implementing high-κ dielectric Low leakage in access transistor and storage capacitor Low resistance for bit and word lines to ensure desired speed Improve bit density and to lower production cost in driving toward $4F^2$ cell size SRAM— Maintain adequate noise margin and control key instabilities and soft-error rate Difficult lithography and etch issues
3. Scaling high-density non-volatile memory	Endurance, noise margin, and reliability requirements Non-scalability of tunnel dielectric and interpoly dielectric in flash Difficult lithography and etch issues with pitch scaling Maintain high gate coupling ratio in floating-gate flash
4. Reliability due to material, process, and structural changes	Threshold voltage shifts due to traps, carrier injection, and program/erase cycling in memory cells Mobility degradation due to mechanical stress relaxation or interface states New or changed failure mechanisms resulting from high-κ/metal gate and new doping/activation processes New failure mechanism resulting from fundamental length scales or new device structures Process variability
Difficult Challenges for $L_g < 16$ nm	*Summary of Issues*
1. Implementation of advanced non-classical CMOS structures	Advanced non-planar multi-gate MOSFETs below 10 nm gate length Control of short-channel effects Drain engineering to control parasitic resistance Strain enhanced thermal velocity and quasi-ballistic transport
2. Implementation of non-classical CMOS channel materials	Identification and demonstration of alternate channel materials New issues from materials, devices, and processing Integration of alternate channel materials on Si platform
3. Identification and implementation of new memory structures	Density and voltage scaling of NVM 3-D integration of NVM Implementing non-charge-storage type of NVM Scaling storage capacitor for DRAM DRAM and SRAM replacement solutions
4. Reliability of novel devices, structures, materials, and applications	Reliability characterization of new devices Dealing with fluctuations and statistical process variations Impact of microscopic physical effects Need for Design for Reliability tools
5. Power scaling	V_{dd} scaling Controlling subthreshold current
6. Beyond CMOS	Identification and implementation of non-CMOS devices and architectures Integration onto Si-CMOS platform See *ERD* and *ERM chapters* for more discussions and details

DESCRIPTION OF PROCESS INTEGRATION, DEVICES, AND STRUCTURES DIFFICULT CHALLENGES

NEAR-TERM ($L_G \geq 16$ NM):

[1] Scaling of logic MOSFETs—

Planar bulk CMOS devices compared to SOI and multi-gate structures have more difficulty in adequately controlling short-channel effects. Continued scaling will face significant challenges due to the high channel doping required to control short-channel effects and to set the threshold voltage properly, resulting in band-to-band tunneling across the junction, gate-induced drain leakage (GIDL), and degradation of carrier mobility. Furthermore, threshold voltage variation due to random (stochastic) dopant variation is projected to become more and more severe with scaling.

Implementation of fully depleted SOI and multi-gate will be challenging. Since such devices will typically have lightly doped channels, the threshold voltage will not be controlled by the channel doping. The challenges associated with high

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channel doping and stochastic dopant variation in planar bulk MOSFETs will be avoided, but numerous new challenges are expected. Amongst the most critical will be controlling the thickness and its variability for these ultra-thin bodies, and establishing a cost-effective method for reliably setting the threshold voltage.

Controlling source/drain series resistance within tolerable limits will be significant issues. Due to the increase of current density, the demand for lower resistance with smaller dimensions at the same time poses a great challenge. This problem becomes even more severe with thin bodies in SOI and multi-gate structures.

Metal gate/high-κ gate stacks have been implemented in the recent technology generation in order to allow scaling of the EOT, consistent with the overall transistor scaling while keeping gate leakage currents within tolerable limits. Further scaling of EOT with higher κ materials (κ > 30) becomes increasing difficult and has diminishing returns. The reduction or elimination of the SiO_2 interfacial layer has been shown to cause interface states and degradation of mobility and reliability. Another challenge is growing gate dielectrics on vertical surfaces in multi-gate structures.

Threshold-voltage tuning and control with metal gate/high-κ gate stacks has proven to be challenging, especially for low-threshold-voltage devices. For planar bulk devices, this is mainly because of difficulties in cost-effectively and reliably setting the gate stack's effective work-function at or near the conduction band edge for *n*-MOSFETs and at or near the valence band edge for *p*-MOSFETs. This issue will be even more critical in fully depleted channels such as multi-gate and FD SOI, where the effective work-function needs to be in the bandgap (although at different values for *p*-MOSFETs and *n*-MOSFETs), and where the work-function is especially critical in setting the threshold voltage because of the lack of channel doping. Furthermore, since multiple threshold voltages are required, an ability to cost-effectively tune the work-function over the bandgap would be very useful.

Enhanced channel-carrier mobility and high-field velocity due to applied strain is a major contributor to meeting the MOSFET performance requirements. In inducing adequate strain some current process techniques tend to be less effective with scaling. Also, to apply known techniques derived from planar structure to non-planar structures will be facing additional difficulty and complexity. Moreover, transport enhancement is projected to saturate with stain at some point. (For more detail, see Logic Potential Solutions section.)

[2] Scaling of DRAM and SRAM—

For DRAM, a key issue is implementation of high-κ dielectric materials in order to get adequate storage capacitance per cell even as the cell size is shrinking. Also important is controlling the total leakage current, including the dielectric leakage, the storage junction leakage, and the access transistor source/drain subthreshold leakage, in order to preserve adequate retention time. The requirement of low leakage currents causes problems in obtaining the desired access transistor performance. Deploying low sheet resistance materials for word and bit lines to ensure acceptable speed for scaled DRAMs and to ensure adequate voltage swing on word line to maintain margin is critically important**.** The need to increase bit density and to lower production cost is driving toward $4F^2$ cell size, which will require high aspect ratio and non-planar structures. Novel solution to have a capacitor-less cell would be highly beneficial.

For SRAM scaling, difficulties include maintaining both acceptable noise margins in the presence of increasing random V_T fluctuations and random telegraph noise, and controlling instability, especially hot-electron instability and negative bias temperature instability (NBTI). There are difficult issues with keeping the leakage current within tolerable targets, as well as difficult lithography and etch process issues with scaling. Solving these SRAM challenges is critical to system performance, since SRAM is typically used for fast, on-chip memory.

[3] Scaling high-density non-volatile memory (NVM)—

For floating-gate devices there is a fundamental issue of non-scalability of tunnel oxide and interpoly dielectric (IPD), and high (> 0.6) gate coupling ratio (GCR) must be maintained to control the channel and prevent gate electron injection during erasing. For NAND flash, these requirements can be slightly relaxed because of page operation and error code correction (ECC), but IPD < 10 nm seems unachievable. This geometric limitation will severely challenge scaling below 20 nm half-pitch. In addition, fringing field effect and floating-gate interference, noise margin, and few-electron statistical fluctuation for V_t all impose steep challenges. Since NAND half-pitch has pulled ahead of DRAM and logic, lithography and etching and other processing advances are also first tested by NAND technology.

Charge-trapping devices help alleviate the floating-gate interference and GCR issues, and the planar structure relieves lithography and etching challenges slightly. Scaling below 20 nm is still a difficult challenge, however, because fringing-field effects and few-electron V_t noise margin are still not proven.

Endurance reliability and write speed for both devices are still difficult challenges for MLC (multi-level cell) high-density applications.

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[4] Reliability due to material, process, and structural changes—

In order to successfully scale ICs to meet performance, leakage current, and other requirements, it is expected that numerous major process and material innovations, such as high-κ gate dielectric, metal gate electrodes, elevated source/drain, advanced annealing and doping techniques, new low-κ materials, etc., are needed. Also, it is projected that new MOSFET structures, starting with ultra-thin body SOI MOSFETs and moving on to ultra-thin body, multi-gate MOSFETs, will need to be implemented. Understanding and modeling the reliability issues for all these innovations so that their reliability can be ensured in a timely manner is expected to be particularly difficult.

The first near-term reliability challenge concerns failure mechanisms associated with the MOS transistor. The failure could be caused by either breakdown of the gate dielectric or threshold voltage change beyond the acceptable limits. The time to a first breakdown event is decreasing with scaling. The most severe threshold voltage related failure is associated with the negative bias temperature instability (NBTI) observed in *p*-channel transistors in the inversion state. Burn-in may be impacted, as it may accelerate NBTI shifts. Introduction of high-κ gate dielectric may impact both the insulator failure modes (e.g., breakdown and instability) as well as the transistor failure modes such as hot-carrier effects, positive and negative bias temperature instability. The replacement of polysilicon with metal gates also impacts insulator reliability and raises new thermo-mechanical issues. The simultaneous introduction of high-κ and metal gate makes it even more difficult to determine reliability mechanisms.

At the heart of reliability engineering is the fact that there is a distribution of lifetimes for each failure mechanism. With low failure rate requirements we are interested in the early-time range of the failure time distributions. There has been an increase in process variability with scaling (e.g., distribution of dopant atoms, CMP variations, line-edge roughness). At the same time the size of a critical defect decreases with scaling. These trends will translate into an increased time spread of the failure distributions and, thus, a decreasing time to first failure. It also translates into a need to increase the number of devices tested for reliability projection. We need to develop reliability testing tool to handle the vastly increased sample size (long-term reliability and large sample size are difficult combination), and the engineering software tools (e.g., screens, qualification, reliability-aware design) that can handle the increase in variability of the device physical properties.

LONG-TERM (L_G < 16 NM):

[1] Implementation of advanced non-classical CMOS structures—

For the long-term years, when the transistor gate length is projected to become 10 nm and below, ultra-thin body multi-gate MOSFETs with lightly doped channels are expected to be utilized to effectively scale the device and control short-channel effects. The other material and process solutions mentioned above, such as high-κ gate dielectric, metal gate electrodes, strained silicon channels, elevated source/drain, etc., are expected to be incorporated along with the non-classical CMOS structures. Body thicknesses well below 10 nm are projected, and the impact of quantum confinement and surface scattering effects on such thin devices are not well understood. The ultra-thin body also adds additional constraint on meeting the source/drain parasitic resistance requirements. Finally, for these advanced, highly scaled MOSFETs, quasi-ballistic operation with enhanced thermal carrier velocity and injection at the source end appears to be necessary for high current drive.

[2] Implementation of non-classical CMOS channel materials —

Eventually, toward the end of the Roadmap or beyond, scaling of MOSFETs is likely to require alternate channel materials in order to continue to improve performance, power, density, etc. To attain adequate drive current for the highly scaled MOSFETs, materials with light effective masses are greatly beneficial in quasi-ballistic operation with enhanced thermal velocity and injection at the source end. The next materials of choice seems to be III-V materials or/and germanium (or SiGe). Eventually, other candidates such as semiconductor nanowires, carbon nanotubes, or graphene nanoribbons may be utilized.

Difficult challenges include developing a new knowledge base concerning new material and device properties, as well as processing issues, such as interface passivation to provide a low-defect interface between channel and gate dielectric. These could be quite different from the long-accumulated knowledge base on Si. Also, it is expected that such solutions will be integrated either functionally or physically with the high-performance, cost-effective, and very dense CMOS logic platform. Such integration requires epitaxial growth of foreign semiconductor on Si substrate which has shown to be challenging.

See Emerging Research Devices and Emerging Research Materials chapters for more discussions and details.

[3] Identification and implementation of new memory structures—

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Dense, fast, and low-voltage non-volatile memory will become highly desirable. Ultimate density scaling may require 3-D architecture, such as vertically stackable cell arrays in monolithic integration, with acceptable yield and performance. All of the existing forms of nonvolatile memory face limitations based on material properties. Success will hinge on finding and developing alternative materials and/or development of alternative emerging technologies. For example, the conflicting requirements of low-voltage operation and retention time make the tunnel-oxide scaling difficult, if not impossible. This fact makes the non-charge type of NVM, such as phase-change memory, attractive, but their ultimate scalability is also unproven. Ultimate density scaling may require 3-D architecture, such as vertically stackable cell arrays in monolithic integration, with acceptable yield and performance.

Increasing difficulty is expected in scaling DRAMs, especially in continued demand of scaling down the foot-print of the storage capacitor. Thinner dielectric EOT utilizing ultra-high-κ materials and attaining the very low leakage currents and power dissipation will be required. A DRAM replacement solution getting rid of the capacitor all together would be a great benefit. The current 6-transistor SRAM structure is area-consuming, and a challenge is to seek a replacement solution which would be highly rewarding. See Emerging Research Devices chapter for more detail.

[4] Reliability of novel devices, structures, materials, and applications—

Many new materials and structures have been proposed, yet currently very little is known about the corresponding failure mechanisms. There is a need to have reliability characterization in place well in advance of application in order to develop appropriate reliability requirements and qualification procedures. For disruptive solutions it is likely that there will be little, if any, reliability knowledge (as least as far as their application in ICs is concerned). This will require significant efforts to investigate, model (both a statistical model of lifetime distributions and a physical model of how lifetime depends on stress, geometries, and materials), and apply the acquired knowledge in design, screens, and tests. It also seems likely that there will be less-than-historic amounts of time and money to develop these new reliability capabilities. Disruptive material or devices lead to disruption in reliability capabilities and it will take considerable resources to develop those capabilities.

For such devices, the impact of statistical variations is not well understood. Compounding the issue is the ability to control the critical dimensions of the device is diminishing. Percent variation in gate length and width is increasing with each generation of technology.

Difficult challenge is also to deal with the impact of microscopic dimensions that may result in quantum effects, including line-edge roughness, ultra-thin body thickness and narrow width.

The fraction of electronic products that demand much higher level of reliability than is generally acceptable is rising. "Life at stake" applications are increasing (e.g., biotechnology products that are implanted into people's bodies). The rise of these applications and the increasingly difficult challenge of assuring reliability are on a collision course. There is need for "Design for reliability" circuit tools such as "Reliability-aware design" and "Fault-tolerant design." At some point, a paradigm change from ensuring all devices meeting specifications to accepting a certain probability of failure at the device level may become necessary.

[5] Power Scaling—

It is well known that V_{dd} is more difficult to scale than other parameters, mainly because of the fundamental limit of the subthreshold slope of ~60 mV/decade. This trend will continue and become more severe when it approaches the regime of 0.6 V. This fact along with the continuing increase of current density causes the active power density ($\sim V_{dd}^2$) to climb with scaling, soon to an unacceptable level. Alternate channel materials and/or devices such as tunnel field-effect transistor can provide some relief in this area by potentially allowing more aggressive V_{dd} scaling or/and steeper subthreshold slope.

For high-performance logic, in the face of increasing chip complexity and increasing transistor leakage current with scaling, chip static power dissipation is expected to become particularly difficult to control while at the same time meeting aggressive targets for performance scaling. Innovations in circuit design and architecture for performance and power management (e.g., utilization of parallelism as an approach to improve circuit/system performance, aggressive use of power down of inactive transistors, etc.), as well as utilization of multiple transistors (high performance with high leakage and low performance with low leakage) on chip, are needed to design chips with both the desired performance and power dissipation.

[6] Beyond CMOS—

Eventually, toward the end of the Roadmap or beyond, scaling of MOSFETs is likely to become ineffective and/or very costly, and advanced non-CMOS solutions will need to be implemented to continue to improve performance, power, density, etc. It is expected that such solutions will be integrated with a CMOS baseline technology.

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LOGIC TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

LOGIC TECHNOLOGY REQUIREMENTS

The technology requirements reflect the MOSFET requirements of both high-performance (HP) and low-power digital ICs. High-performance logic refers to chips of high complexity, high performance, and high power dissipation, such as microprocessor unit (MPU) chips for desktop PCs, servers, etc. Low-power logic refers to chips for mobile systems, where the allowable power dissipation and hence the allowable leakage currents are limited by battery life. There are two major categories within low-power; low operating power (LOP) and low standby power (LSTP) logics. LOP chips are typically for relatively high-performance mobile applications, such as notebook computers, where the battery is likely to be high capacity and the focus is on reduced operating (i.e., dynamic) power dissipation. LSTP chips are typically for lower-performance, lower-cost consumer type applications, such as consumer cellular telephones, with lower battery capacity and an emphasis on the lowest possible static power dissipation, i.e., the lowest possible leakage current. The transistors for high-performance ICs have both the highest performance and the highest leakage current of the three, and hence the physical gate length and all the other transistor dimensions are most rapidly scaled for high-performance logic. The transistors for LOP chips have somewhat lower performance and considerably lower leakage current, while the transistors for LSTP chips have both the lowest performance and the lowest leakage current of the three. For LOP logic, the gate length lags behind the high-performance transistor gate length by ~1 year in near-term years, reflecting historical trends and the need for low leakage current in mobile applications. For LSTP logic, the gate length lags that of high-performance logic by ~2 years in near-term years, reflecting the ultra-low leakage current required. However, both kinds of low-power transistors merge with the high-performance logic in gate length around year 2014 (*See the 2009 Executive Summary).*

It should be mentioned here that recent surveys and literature indicate that the gate-length scaling has been less aggressive than the past roadmap predictions. Realignment for this effect was the major change in the ITRS 2008 edition. Reiterating that change in 2008 in comparison to that in 2007, the physical gate length L_g scaling for HP logic is slowed down by 3-5 years, with a change of slope. It is also observed that with the new L_g scaling model, the *CV/I* speed metric has a slope of ~13% increase per year instead of 17%. Similar changes were made to LOP technology whose physical gate length had a slow-down of 1-3 years, also with a change of slope. In this year's edition, a minor adjustment of 1-year slow-down is made compared to the 2008 edition for most logic devices.

For generating the entries in the logic technology requirements tables, the *MASTAR* MOSFET modeling software was used.[1,2,3] The software contains detailed analytical MOSFET models that have been verified against literature data. It is well suited to efficiently analyzing technology tradeoffs for generating these tables, and has been used for the PIDS calculations for many years. An important calculated output parameter is the intrinsic MOSFET delay, $\tau = CV/I$, where C is the total gate capacitance (including parasitic gate overlap and fringing capacitance) per micron transistor width, V is the power supply voltage (V_{dd}), and I is the saturation drive current per micron transistor width ($I_{d,sat}$). τ is a reasonable metric for the intrinsic MOSFET delay, and hence $1/\tau$, the transistor intrinsic switching frequency, is used as a key transistor performance metric. (It should be noted that another transistor delay metric, CV/I_{eff}, where I_{eff} is a modified drain current derived from a linear superposition of currents,[4] has been developed and appears to be somewhat more accurate than the $CV/I_{d,sat}$ metric. We are continuing to use the original metric because it is sufficiently accurate to follow the key scaling trends, and for consistency with previous Roadmaps.)

To reflect more accurately the transistor speed metric, added in this year is the ring-oscillator speed, in delay per stage, for fan-outs of one and four. Ring-oscillator speed is slower than the intrinsic transistor speed, but is considered the fastest circuit speed that can be realized, and is a measured parameter, so we feel it is a more suitable parameter to monitor the real speed performance of a CMOS technology. For a CMOS inverter, the *p*-channel performance is also important but not captured in the past. In order to avoid having to double the table size from adding the *p*-channel MOSFET, only one parameter is entered—the ratio of $I_{d,sat}$ between the two types of channels. This is a reasonable compromise by assuming the capacitances associated with *p*-channel are similar, along with all other parameters such as threshold voltage and off-current. The inverter chain or ring-oscillator simulation is also conveniently performed by *MASTAR*. The *CV/I* metric is also kept for continuity and comparison.

To determine the projected parameter values in a table, the main target is $1/\tau$ vs. years, for a given fixed off-current. Then the input parameters are tentatively chosen based on scaling rules, engineering judgment, and physical device principles. Using MASTAR, the input parameters are iteratively varied until the target is met, and the final set of values for the input parameters is entered into the table. *The MASTAR program and the specific MASTAR process and roadmap files used to generate the tables are on the ITRS website.*

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The specific set of projected parameter values in each of the tables reflects a particular scaling scenario in which the targeted values for the key outputs are achieved. However, since there are numerous input parameters that can be varied, and the output parameters are complicated functions of these input parameters, other sets of projected parameter values (i.e., different scaling scenarios) may be found that achieve the same target. For example, one technology would scale the EOT more aggressively by introducing high-κ dielectric, while another would achieve equivalent results by optimizing doping or/and strain enhancement. Hence, the scaling scenarios in these tables constitute a good guide for the industry, and are not meant to be unique solutions, but there will be considerable variance in the actual paths that the various companies will take.

In each of these logic devices, multiple parallel paths in structures are followed. Planar bulk CMOS is extended as long as possible, while advanced CMOS technologies—ultra-thin body fully depleted (UTB FD) silicon-on-insulator (SOI) MOSFETs and multi-gate (MG) MOSFETs (such as FinFETs), are implemented in 2013 or later, and run in parallel with the planar bulk CMOS for some period (for details see the logic tables). There is always a question that for the multi-gate structures, whether they will be on bulk wafers or SOI wafers. It is understood that their DC and AC performances are equivalent in these two difference substrates, so they do not affect the outcome of the performance prediction.[5] The issues there have to do with trade-offs in cost, process complexity, variability, and design layout complexity. Hopefully that choice will become clear in the near future. With scaling, difficulties arise with planar bulk MOSFETs because of high channel doping, inability to adequately control short-channel effects, and other issues (for more detail see Difficult Challenges section, Item 1). The advanced CMOS structures can be scaled more effectively, and hence are utilized later in the Roadmap. In fact, multi-gate MOSFET scaling is superior to UTB FD MOSFET scaling, and hence the ultimate MOSFET is projected to be the multi-gate device. For the industry as a whole, multiple paths are likely, as different companies choose different timing in extending planar bulk and then switching to the advanced CMOS technologies, depending on their needs, plans, and technological strengths. The multiple parallel paths in this roadmap are meant to reflect this.

For the high-performance logic tables (see Table PIDS2), the driver is the MOSFET intrinsic performance metric, $1/\tau$, although there is plan to switch to ring-oscillator speed eventually. Specifically, the target is an average 13% per year increase in $1/\tau$, which matches the historic rate of improvement in device performance in recent years, and has been slowed down from the previous 17% per year. Meeting this target is an important enabler for the desired rate of improvement in the chip clock speed. All the other parameter values in the table are chosen iteratively to meet this target, as explained above. Several important consequences of meeting this target are clear from the tables. The NMOSFET saturation drive current, $I_{d,sat}$, pretty steadily increases over the course of the Roadmap in order to keep $1/\tau$ increasing at the desired 13% per year rate. The subthreshold source/drain leakage current, $I_{sd,leak}$, is fixed at a value of 100 nA/μm for all years, which has important consequences for the chip power dissipation (to be discussed below). Figure PIDS1 shows the scaling of $1/\tau$ for high-performance logic. Overall, the 13%/year target is met, with some precaution. For planar bulk, for 2009 and beyond, the $1/\tau$ curve slopes increasingly downward from the 13%/year curve, mainly because of the scaling difficulties discussed in the Difficult Challenges section, Item 1. (The scaling difficulties are also indicated in the MASTAR simulations, where the required channel doping increases sharply with year, to a very high value of 7.5×10^{18} cm^{-3} in 2015.) For UTB FD SOI, even though the pace is kept up with the 13% slope, the thin-body thickness requirement becomes extremely demanding, in the range of 4 nm in year 2019. This thin-body requirement is relaxed with the MG structure and scaling could continue until the end of this range 2024.

Table PIDS2 High-performance Logic Technology Requirements

Figure PIDS1 also includes ring-oscillator speed which is defined as the reciprocal of the delay per stage, for both cases of fan-out of 1 and fan-out of 4. It is shown here that these frequencies are somewhat slower than the transistor intrinsic frequency, as expected. For fan-out of one, the frequency ratio is about 5, where as for fan-out of 4, the ratio is about 10. The slopes for both cases are slightly less than that of *CV/I*, around 11%.

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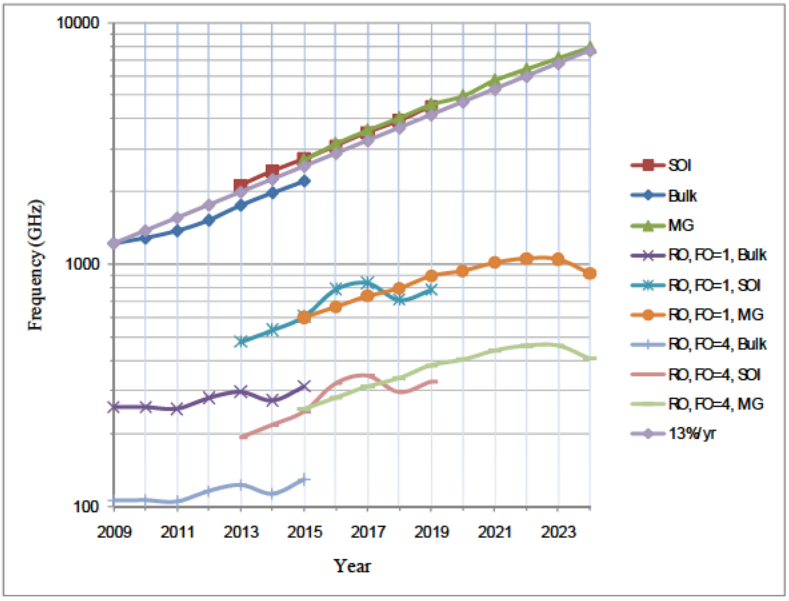


Figure PIDS1 Scaling of Transistor Intrinsic Speed of High-Performance Logic

In the legend section, the first set of 3 symbols represent the inverse of CV/I ($1/\tau$). The second set represent inverse of the ring-oscillator delay per stage, for fan-out of 1. The third set represents the same but with fan-out of 4. The last curve is the reference of 13% increase per year.

The IC industry has begun to deploy architectural techniques such as multiple cores and multiple threads that exploit parallelism to improve the overall chip performance, and to enhance the chip functionality while maintaining chip power density and total chip power dissipation at a manageable level. With more than one central processing unit (CPU) core on chip, the cores can be clocked at a lower frequency while still getting better overall chip performance. Thus, there is a trend for system designers to emphasize integration level, which enables more cores (multi-core) to be put on a chip, instead of raw transistor speed in optimizing system-level performance. In addition, system designers are sweeping ever more cache memory onto the processor chip in order to minimize the system performance penalty associated with finite-cache effects. As DRAM cells are significantly smaller than SRAM cells, another high-performance system technology trend is to integrate DRAM cells onto a processor chip for use in higher-level cache memory. With scaling, it is expected that these techniques will be more and more heavily exploited. In subsequent editions of the Roadmap, the Design and PIDS Working Groups will consider the impact of these architectural techniques, and in particular whether improved architectural parallelism may allow a slackening in the 13%/year transistor performance scaling target.

For high-performance chips, the high subthreshold leakage current must be dealt with to keep chip static power dissipation within tolerable limits. One common approach is to fabricate more than one type of transistor on the chip, including the high-performance, low-V_t device described above, as well as other MOSFET(s) with higher-V_t and sometimes larger EOT to reduce the leakage current. These alternate, lower leakage devices will have lower saturation drive current and hence poorer device performance (i.e., lower MOSFET intrinsic switching frequency, $1/\tau$) than the high-performance devices. The high-performance device is used just in critical paths, and the low leakage devices are used everywhere else. Extensive use of the low leakage devices can significantly reduce the chip static power dissipation without seriously degrading chip performance. Current circuit/architectural techniques to curtail static power dissipation include pass gates to cut off access to power/ground rails or other techniques to power down circuit blocks. Other potential techniques include well biasing, or using electrically or dynamically adjustable-V_t devices. Hence, a realistic picture of scaled high-performance ICs is that the static power dissipation is controlled by utilizing more than one type of transistor and by utilizing device/design/architectural techniques. In the technology requirements table, we have characterized only the high-performance transistor because this transistor is the technology driver.

For low-power chips, the important boundary is the source/drain subthreshold leakage current, $I_{sd,leak}$. For LSTP logic, $I_{sd,leak}$ is set at 50 pA/μm, while it is 5 nA/μm for LOP devices. All the other parameter values in the tables are chosen

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iteratively to meet the $I_{sd,leak}$ targets, while optimizing $1/\tau$. Nevertheless, the resultant speed improvement in the device performance metric, $1/\tau$, is also around 13% improvement per year for both LOP and LSTP, the same as that of HP devices. Note that, to meet the leakage current requirements, the gate length scaling of low-power logic lags behind that of high-performance logic (see the logic tables for details). One key issue for LSTP logic is the slower scaling of V_{dd}. Refer to Table PIDS3a for LSTP data. This slow scaling is a result of the relatively slow scaling of the threshold voltage, V_t, required to meet the very low subthreshold leakage current targets. V_{dd} must follow V_t in scaling slowly because, to obtain reasonable device performance, the overdrive, $(V_{dd} - V_t)$, must remain relatively large. Since dynamic power dissipation is proportional to V_{dd}^2, the dynamic power dissipation for the LSTP logic scales relatively slowly. But since the activity factor for this type of logic is expected to be relatively small, the lowered static power dissipation because of the very low leakage currents more than compensates for the dynamic power. In contrast to LSTP logic, V_{dd} scales relatively quickly for LOP logic (see technology requirements tables for LOP, Table PIDS3b), where, as mentioned above, the focus is on minimizing the operating power (i.e., the dynamic power dissipation, which is proportional to V_{dd}^2). However, since $I_{sd,leak}$ is larger than for LSTP logic, the saturation threshold voltage is low enough that the overdrive, $(V_{dd} - V_t)$, is reasonable.

For low-power chips, the key goal is low power dissipation in order to enhance battery life, with a trade-off of low performance compared to high-performance chips. This overall goal is attained through the use of transistors with low $I_{sd,leak}$ as well as through the approaches utilized for high-performance logic: multiple transistors on chip and application of circuit and architectural techniques, including power management techniques to reduce chip leakage current in the standby mode. Eventually, effective dynamic threshold voltage adjust techniques may be feasible. The nominal targets for $I_{sd,leak}$ chosen in these LSTP logic tables are quite low, and reflect a transistor design emphasizing low leakage current in the active mode. In contrast, some companies will utilize transistors with significantly higher $I_{sd,leak}$ to get higher performance, and will thus rely more heavily on circuit and architectural techniques to lower overall chip power dissipation. Finally, for LOP logic, as discussed above, V_{dd} will be scaled relatively quickly to keep the dynamic power dissipation within tolerable limits.

Table PIDS3A Low Standby Power Technology Requirements

Table PIDS3B Low Operating Power Technology Requirements

LOGIC POTENTIAL SOLUTIONS

There is a strong correlation between the challenges indicated by the colors in the technology requirements tables and the potential solutions (see Figure PIDS2). In many cases, red coloring (manufacturable solutions are not known) in the technology requirements tables corresponds to the projected year of introduction for a potential solution to the challenge indicated by these colors. Another important general point is that each potential solution highlighted in the Potential Solutions figure involves significant technological innovation. The qualification/pre-production interval has been set to around two years in order to understand and deal with any new and different reliability, yield, and process integration issues associated with these innovative solutions. Many of the potential solutions may be required first for high-performance logic. Finally, the industry faces a major overall challenge due to the sheer number of major technological innovations required over the next five years: enhanced mobility[6] and high-field transport, high-κ/metal gate stack (which are already implemented but requiring continuous improvement with scaling), ultra-thin body fully depleted SOI, and multi-gate MOSFETs, with quasi-ballistic transport.

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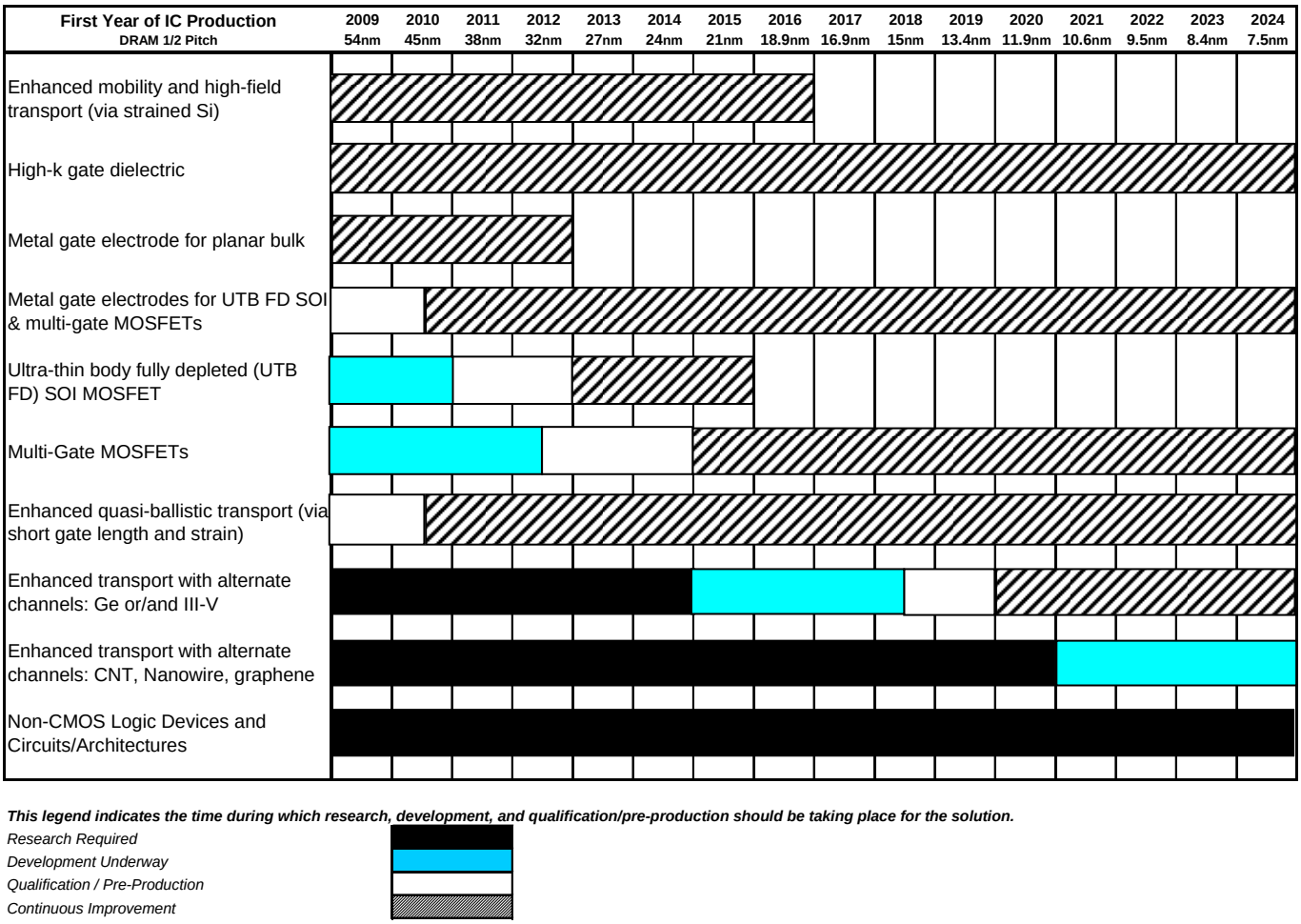


Figure PIDS2 Logic Potential Solutions

The first potential solution, enhanced mobility and high-field transport due to strain, is needed to enhance the saturation current drive to meet transistor performance targets. (Note that, in the Logic Technology Requirements tables, significantly enhanced mobility is assumed in the projections.) It was first implemented in 2004 for high-performance logic. There are numerous techniques to implement enhanced mobility, including various types of process-induced local strain (such as heterojunction source/drain and strained liner layer) or by globally induced strain in a thin strained silicon layer, either on relaxed SiGe layers with controlled percentages of Ge or in SOI substrates. Other approaches include use of hybrid orientations (e.g., PMOSFET mobility is highest for the (110) substrate orientation) or use of strained SiGe or (eventually) strained Ge channels. The potential solutions figure indicates that continuous improvement will be needed here, to increase the mobility enhancement to the maximum extent possible for both NMOSFET and PMOSFET, to integrate mobility enhancement optimally with the overall process flow, and eventually to utilize mobility enhancement for advanced MOSFETs such as UTB SOI and multi-gate MOSFETs. In addition, continuous improvement will be needed to deal with the reduced effectiveness of process-induced strain techniques with scaling: as the spacing between transistors is reduced with scaling, techniques such as embedded SiGe or Si:C in the source/drain and the addition of stressed thin film silicon nitride liner layers over the top of the transistor tend to becomes less effective at inducing stress in the channel. Overall, continue to increase the strain is getting more difficult, and the improvement of mobility and high-field transport saturates at some high strain level.

In order to scale the basic MOSFET structure significantly beyond 2009 (corresponding to physical gate length of 29 nm for high-performance logic), key technology issues include the device gate stack which consists of the gate dielectric and the gate electrode. As the physical gate length is scaled, ideally the gate dielectric equivalent oxide thickness (EOT) is scaled correspondingly to control short-channel effects and to increase the inversion charge and saturation current drive.

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But the effectiveness of continued EOT reduction becomes limited due to the non-scalability of poly-gate electrode depletion and inversion layer effects, which both increase the equivalent electrical oxide thickness in inversion. High-κ gate dielectric material is a solution to solve the problem of high gate leakage current, since the gate leakage current density corresponding to a given EOT is much smaller for high-κ than for oxy-nitride gate dielectric. Use of metal gate to replace poly-Si gate is effective in eliminating the poly-depletion phenomenon. For HP logic, high-κ gate dielectric and metal gate electrode have been introduced in 2009 in order to effectively prevent gate electrode depletion and hence allow acceptable scaling of the equivalent electrical oxide thickness in inversion. Low-power devices will follow in about 2 years. To set the threshold voltage correctly for planar bulk CMOS, the gate electrode work-function needs to be near the silicon valence band edge for PMOSFETs and near the silicon conduction band edge for NMOSFETs. Hence, different metals will probably be needed for the PMOSFET and NMOSFET.

As scaling proceeds, it will become increasingly difficult to effectively scale planar bulk CMOS devices. In particular, adequately controlling short-channel effects is projected to become especially problematical for such short-channel devices. Furthermore, the channel doping will need to be increased to exceedingly high values, which will tend to reduce the mobility and to cause high leakage current due to band-to-band tunneling between the drain and the body. Finally, the total number of dopants in the channel for such small MOSFETs becomes relatively small, which results in large random fluctuations in the dopant placement and number, and hence unacceptably large statistical variation of the threshold voltage. These difficulties become worse with further scaling. A potential solution is to utilize ultra-thin body, fully depleted (UTB FD) SOI MOSFETs. The channel doping is relatively light, and for such devices, the threshold voltage can be set by adjusting the work-function of the gate electrode, rather than by doping the channel as in planar bulk MOSFETs. Metal gate electrodes with near-midgap work-functions will be needed to set the threshold voltage to the desired values. Because of the different work-functions in this case, the electrode material will presumably be different than those utilized for planar bulk MOSFETs. In fact, one electrode material with work-function tunable within several hundred meV on either side of midgap may be possible. Due to the lightly doped and fully depleted channel, the threshold voltage control by the work-function of the gate electrode, and the ultra-thin body, these SOI MOSFETs are considerably more scalable and can deliver higher saturation drive current than comparable planar bulk MOSFETs. Single gate SOI MOSFETs are projected for 2013 for high-performance logic. Multi-gate, ultra-thin body, fully depleted MOSFETs are both more complex and even more scalable, and are projected to be implemented in 2015 for high-performance logic.

As the gate length is scaled well below 20 nm, the fully depleted, lightly doped MOSFETs are likely to require enhanced quasi-ballistic transport to meet the performance requirements (see Ballistic Enhancement Factor in the Logic Technology Requirements tables for detailed numbers). These enhancements will be obtained through reduced scattering in short channel length, through improved injection at the source, and through reduction of effective mass by strain.

Eventually, late in the Roadmap, more forward-looking solutions in utilization of alternate channel materials to further enhance the transport may be adopted. It is anticipated the first solutions would be III-V or/and Ge (or SiGe) channel materials, still based on MOSFET operation. Other possibilities beyond these are semiconductor nanowire, carbon nanotube, and graphene nanoribbon.

Finally, at the end of the Roadmap or beyond, MOSFET scaling will likely become ineffective and/or very costly. Completely new, non-CMOS type of logic devices and maybe even new circuits/architectures are a potential solution (see Emerging Research Devices section for detailed discussions). Such solutions may be integrated onto Si-based platform.

MEMORY TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

DRAM

Technical requirements for DRAMs become more difficult with scaling (see Table PIDS4). The process associated with 193 nm argon fluoride (ArF) immersion high-NA lithography and double patterning technology are keys for 40 nm or smaller half-pitch DRAMs.

In recent years, DRAM cell structure was migrating to stack capacitor cell. Trench DRAM cell could not survive future scaling due to its difficulties of getting the adequate process and performance of memory cell. But, even in the stack capacitor cell, it also has many technology challenges for 40 nm or smaller size DRAM.

Table PIDS4 DRAM Technology Requirements

However, there exist several significant process flow issues from a production standpoint, such as process steps of capacitor formation or high aspect ratio contact etches requiring photoresists that can stand up for a prolonged etch time. To overcome these challenges, the technology related to photoresists with a hard mask layer for pattern transfer is gaining importance. Furthermore, continuous improvements in lithography and etch will be needed.

On the other hand, with the scaling of peripheral CMOS devices, a low-temperature process flow is required for process steps after formation of these devices. This is a challenge for DRAM cell processes which are typically constructed after the CMOS devices are formed, and therefore are limited to low-temperature processing. In addition, the planar access device (cell FET) for the one transistor-one capacitor (1T-1C) cell is getting difficult to design due to the need to maintain a low level of both subthreshold leakage and junction leakage current to meet the retention time requirements. To compromise that, recessed channel cell FET is being adapted and optimization work have been done under half-pitch scaling. But below the 40's nm half-pitch, FinFET or 3-D type FET will be required to get the high drive current and low-voltage operation. Another challenge is a highly reliable gate insulator. A highly boosted gate voltage is required to drive higher drain current with the relatively high threshold voltage adopted for the cell FET to suppress the subthreshold leakage current.

The scaling of the DRAM cell FET dielectric, maximum word-line (WL) level, and the electric field in the cell FET dielectric are critical points for gate insulator reliability concern. To keep the electric field in the dielectric with scaling, process requirements for DRAMs such as front-end isolation, low-resistance materials for the word lines, self-aligned and high aspect ratio etches, planarization, and Cu interconnection are all needed for future high-density DRAMs.

Since the DRAM storage capacitor gets physically smaller with scaling, the EOT must scale down sharply to maintain adequate storage capacitance. To scale the EOT, dielectric materials having high relative dielectric constant (κ) will be needed. Therefore MIM (Metal Insulator Metal) capacitors have been adopted and using high k ($HfSiO/Al_2O_3$, κ~10-25) as the capacitor of 70's nm half-pitch DRAM, ZrO/HfO as the capacitor of 50's nm half-pitch DRAM. And this material evolution will be continued and eventually ultra high-κ (perovskite $\kappa > 50$) material will be released in 2011. (See Figure PIDS4, DRAM Potential Solutions, for details.) Also, the physical thickness of the high-κ insulator should be scaled down to fit the minimum feature size. Due to that, capacitor 3-D structure will be changed from cylinder to pedestal shape.

All in all, maintaining sufficient storage capacitance will pose an increasingly difficult requirement for continued scaling of DRAM devices. In Figure PIDS4, the potential solutions are listed, but many future technologies will be necessary for 30 nm half-pitch or less. And these future technologies are still unknown.

Keeping the chip size approximately constant as the DRAM capacity (number of bits per chip) is increased with scaling is very important from a chip cost point of view. In order to do so, the cell size factor (a) scaling (where a = [DRAM cell size]/[DRAM half pitch]^2) is critically important. Companies have started production of DRAMs with an a of 6 in 2006. And in order to accelerate the cost efficiency, $4F^2$ (a = 4) cell will be introduced in 2011. Migration of $4F^2$ cell required many technology challenges such as 3-D type cell FET, etc. [7]

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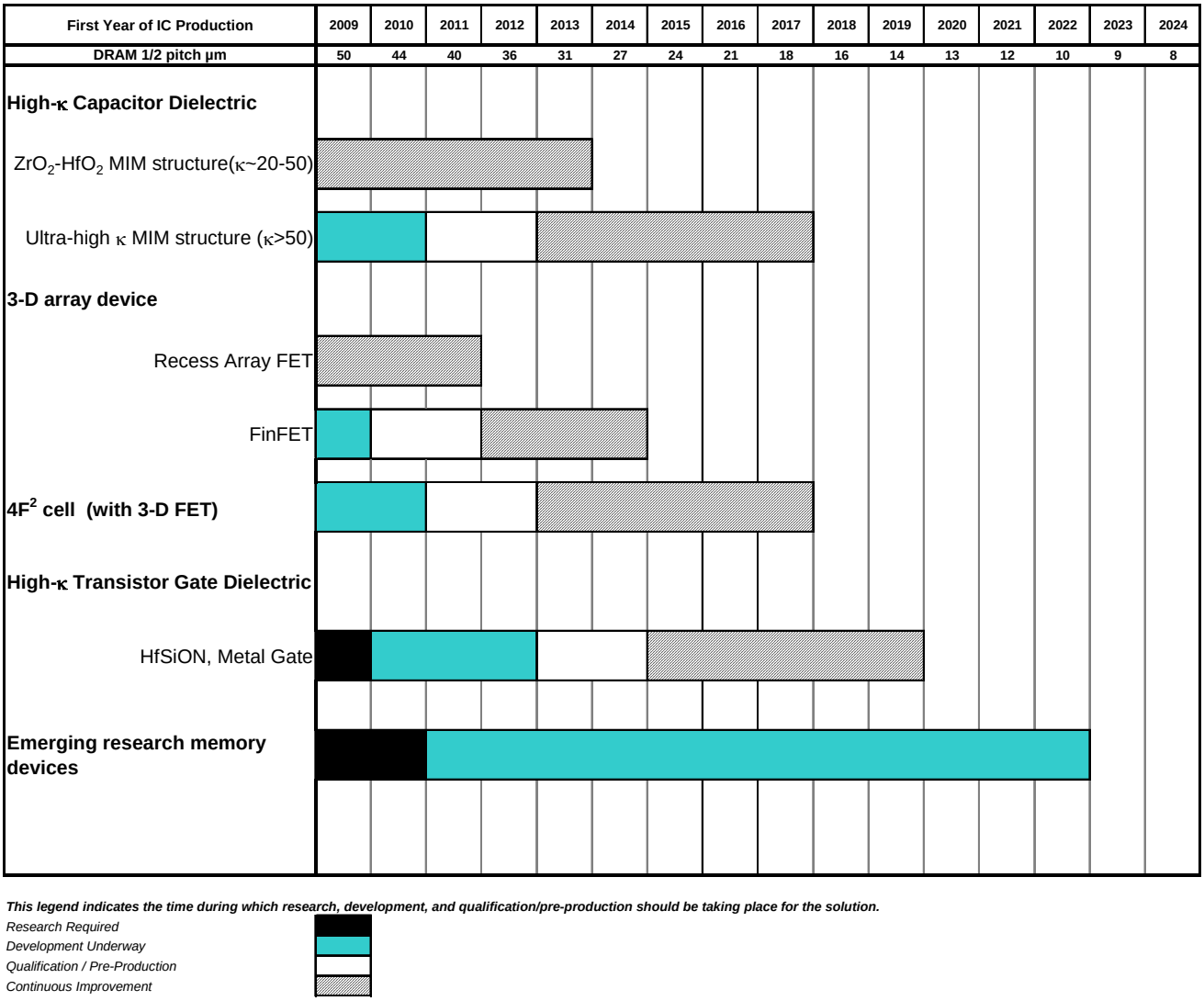


Figure PIDS3 DRAM Potential Solutions

NON-VOLATILE MEMORY

NON-VOLATILE MEMORY TECHNOLOGY REQUIREMENTS

Non-volatile memory consists of several intersecting technologies that share one common trait–non-volatility. The requirements and challenges differ according to their applications, ranging from RFIDs that only require KByte of storage to high-density storage of tens of Gbit in a chip. The requirements tables are divided into three categories—NAND Flash, NOR Flash, and non-charge-storage memories. Each category may contain more than one approach. For example, NOR Flash memories are fabricated using both floating-gate device and nitride charge-trapping device, each with their own design rules and scaling trend. Overlapping and/or succession of different technologies for the same application are indicated as appropriate, since as technology evolves best density and performance may be achieved through multiple paths.

Information on each technology is organized into three categories. The requirements tabulation for each technology first treats the issue of density. The applicable feature size "F" is identified and the expected area factor "*a*" is given (cell size in terms of the number of F^2 units required). Second, the tabulation presents a number of parameters important to each specific technology such as gate lengths, write-erase voltage maxima, key material parameters, etc. These parameters have significance because they are important to the scaling model and/or identify key challenge areas. Third, the

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endurance (erase-write cycle or read-write cycle) ratings and the retention ratings are presented. Endurance and retention are requirements unique to NVM technologies and they determine whether the device has adequate utility to be of interest to an end customer.

Table PIDS5 shows technology requirements for NAND Flash, NOR Flash and non-charge-storage memories for 2009 through 2024. The tables identify both the current CMOS half-pitch and the feature size actually used to form the NVM cells (i.e., the NVM technology "F" in nanometers). Until recently NVM half-pitches have lagged those for DRAM or CMOS logic devices in the same year. Rapid progress in NAND technology has not only reversed this trend but also has surpassed the half-pitches of DRAM and CMOS logic devices. This trend has not spread to other NVM applications yet, however.

Table PIDS5 Non-Volatile Memory Technology Requirements

NON-VOLATILE MEMORY POTENTIAL SOLUTIONS

Nonvolatile memory (NVM) technologies combine CMOS peripheral circuitry with a memory array. The memory array generally requires additional, but CMOS compatible, processes to implement the non-volatility. Non-volatile memories are used in a wide range of applications, some stand-alone and some embedded, with varying requirements that depend on the application. The memory array architecture and signal sensing method also differ for different applications. The technical challenges are difficult, and in some cases fundamental physics limitations may be reached before the end of the current roadmap. For charge-storage devices, the number of electrons in the storage node, whether for single level logic cells (SLC) or multi-level logic cells (MLC), needs to be sufficiently high to maintain stable threshold voltage against statistical fluctuation, and cross talk between neighboring bits must be reduced while the spacing between neighbors decreases. Meanwhile, data retention and cycling endurance requirements must be maintained, and in some cases even increased for new applications. Non-charge-storage devices also may face fundamental limitations when the storage volume becomes small such that random thermal noise starts to interfere with signal. (Figure PIDS4)

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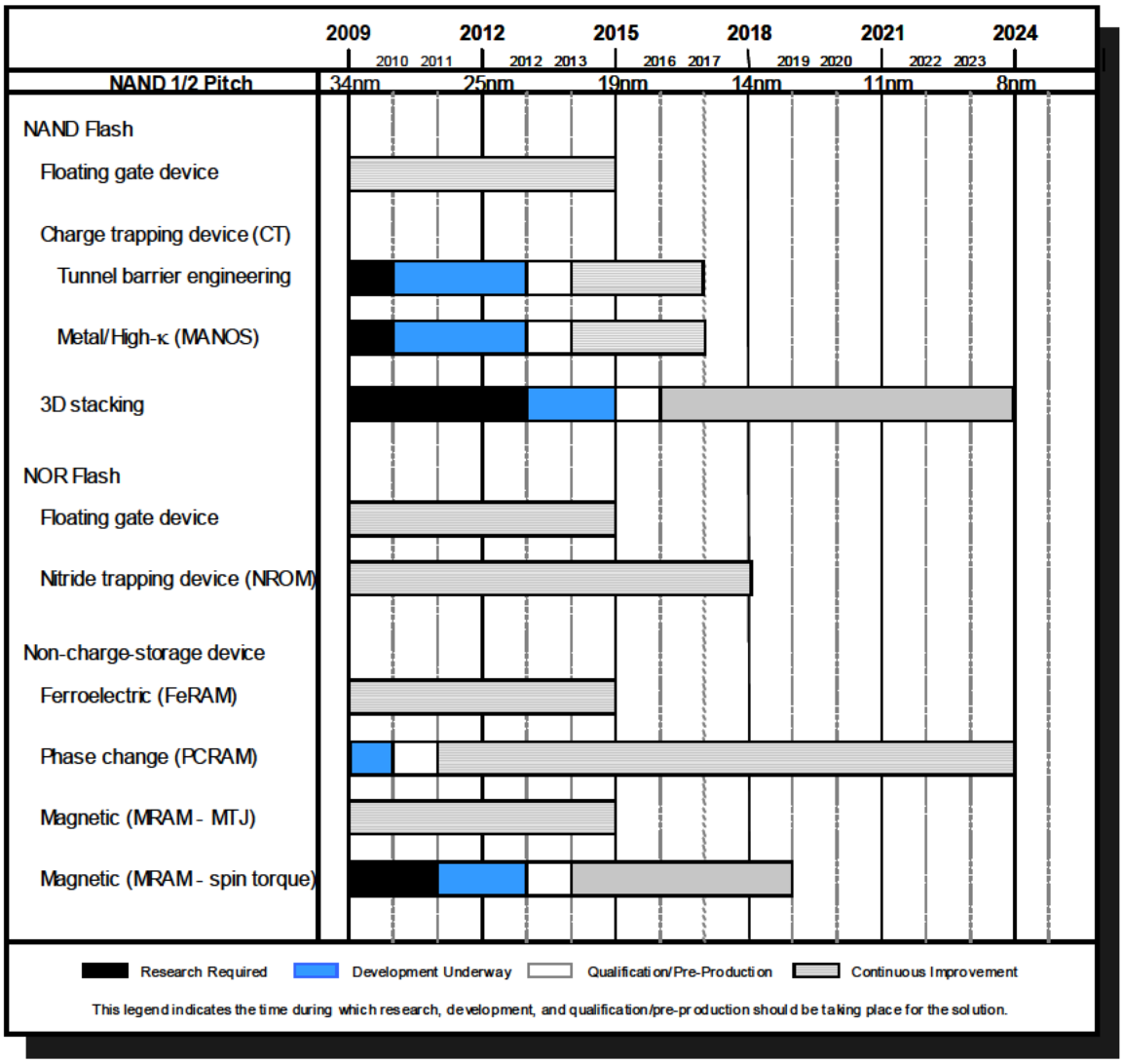


Figure PIDS4 Non-Volatile Memory Potential Solutions

FLOATING-GATE NAND FLASH

Floating-gate Flash devices achieve non-volatility by storing and sensing the charge on a floating gate. The conventional memory transistor vertical stack consists of a refractory polycide control gate, an interpoly dielectric (IPD) that usually consists of triple oxide-nitride-oxide (ONO) layers, a polysilicon floating gate, a tunnel dielectric, and the silicon substrate. The tunnel dielectric must be thin enough to allow charge transfer to the floating gate at reasonable voltage levels and thick enough to avoid charge loss when in read or off modes. The gate coupling ratio (GCR), defined as the capacitance ratio of the control gate to floating-gate capacitor to the total floating-gate capacitance (control gate to floating gate + floating gate to substrate), is a critical scaling parameter, and must be ≥ 0.6. In most structures, to achieve a GCR ≥ 0.6, the word line (control gate) wraps around the sidewall of the floating gate to provide extra capacitance.

The interpoly dielectric thickness must scale with the tunnel dielectric to maintain adequate coupling of applied erase or write pulses to the tunnel dielectric. Because of data retention requirement, both tunnel dielectric and IPD scale slowly. In 2009, the most advanced NAND technology (34 nm half-pitch) uses an IPD around 12 nm. It is difficult to achieve the wrap-around structure when the bit-line spacing becomes 20 nm or less. Therefore, maintaining the GCR is a major challenge for floating-gate Flash device scaling.

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A NAND Flash cell consists of a single MOS transistor, serving mainly as the storage device. The NAND array consists of bit-line strings of 32 devices or more with a selection device at each end. This architecture requires no direct bit-line contact to the cell, thus allows the smallest cell size. During programming or reading, the unselected cells in the selected bit-line string must be turned on and serve as "pass" devices, thus the data stored in each device cannot be accessed randomly. Both programming and erasing are through Fowler-Nordheim tunneling of electrons into and out of the floating gate. The low Fowler-Nordheim tunneling current allows the simultaneous programming of many bits, thus gives high programming speed. Since devices in the same bit-line string serve as pass transistors their leakage current does not affect programming or reading operation, and without the need for hot electrons junctions can be shallow. Designed to provide storage and access to large quantities of data but not to instantly execute program codes, NAND Flash generally employs error correction code (ECC) algorithms, and is thus more fault tolerant than NOR Flash. Because of fault tolerance NAND has weaker tunnel oxide limitation than NOR flash and is easier to scale.

How to maintain a GCR > 0.6 and to avoid floating gate to floating gate cross talk are two difficult challenges when scaling to 22 nm and below. Eventually, the few-electron limitation will cause unacceptable retention time distribution, for which there is currently no recognized solution.

CHARGE-TRAPPING NAND FLASH

Currently all NAND products are fabricated with floating-gate devices. The difficult challenges of maintaining or increasing the GCR and reducing the neighboring cell cross talk may be bypassed by using charge-trapping devices. The single gate controls the MOS device channel directly and thus there is no GCR issue, and the cross talk between thin nitride storage layers is insignificant. Nitride trapping devices may be implemented in a number of variations of a basic SONOS type device. SONOS using a simple tunnel oxide, however, is not suitable for NAND application—once electrons are trapped in deep SiN trap levels they are difficult to detrap even under high electric field. In order to erase the device quickly holes in the substrate must be injected into the SiN to neutralize the electron charge. Since the hole barrier for SiO_2 is high (~4.1 eV), hole injection efficiency is poor and sufficient hole current is only achievable by using very thin tunnel oxide (~ 2 nm). Such thin tunnel oxide, however, results in poor data retention because direct hole tunneling from the substrate under the weak retention built-in field cannot be stopped.

Several variations of SONOS have been proposed recently. Tunnel dielectric engineering concepts are used to modify the tunneling barrier properties to create "variable thickness" tunnel dielectric. For example, triple ultra-thin (1–2 nm) layers of ONO are introduced to replace the single oxide (BE-SONOS).[8] Under high electric field, the upper two layers of oxide and nitride are offset above the Si valence band, and substrate holes readily tunnel through the bottom thin oxide and inject into the thick SiN trapping layer above. In data storage mode, the weak electric field does not offset the triple layer and both electrons in the SiN and holes in the substrate are blocked by the total thickness of the triple layer. In MANOS (metal-Al_2O_3-nitride-oxide-Si),[9] a high-κ blocking dielectric and metal gate are combined to both prevent gate injection during erase operation, and to boost the electric field at tunnel oxide. A thicker (3-4 nm) tunnel oxide may be used to prevent substrate hole direct tunneling during retention mode.

NON-PLANAR AND MULTI-GATE DEVICES FOR NAND

Non-planar and multi-gate devices such as FinFET and devices provide better channel control and allow further scaling of both floating-gate and nitride-trapping devices. However, the vertical structure also presents new challenges. For example, the space between fins must be sufficiently wide to allow room for tunnel oxide, floating gate and IPD (for floating-gate device) and may forbid scaling beyond 30 nm if innovative solutions are not found.

3-D NAND ARRAYS

When the number of stored electrons reaches statistical limits, even if devices can be further scaled and smaller cells achieved, the threshold voltage distribution of all devices in the memory array will become uncontrollable and logic states unpredictable. The memory density cannot be increased by continued scaling, but may be increased by stacking memory layers vertically. Successful stacking of memory arrays vertically has been demonstrated in recent years. One approach uses single-crystal Si by lateral epitaxial growth.[10] Another uses polycrystalline Si thin-film transistor (TFT) device.[11] The processing temperature and thermal budget must be such that the layers fabricated earlier are not degraded by the additional thermal processes. This imposes a significant challenge to either achieve identical devices in different layers that experience different thermal processes, or to design circuits that can handle devices that are slightly different in each layer. Although 3-D stacking can help increase the memory density beyond conventional scaling, its effectiveness diminishes after several layers are stacked. The complexity in interconnection increases and the array efficiency decreases

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with the number of layers. In addition, the complex processing and the large number of masks cumulatively affect the yield, and the cost per bit benefit is only moderate.

Recently, a "punch and plug" approach is proposed to fabricate the bit-line string vertically to simplify the processing steps.[12, 13] This approach and other 3-D stacking that make devices in a few steps and not through repetitive processing,[14, 15, 16] hopefully, can provide a new low-cost scaling path to NAND flash. Note that in all 3-D approaches, the lateral (planar) half-pitch stops scaling and the density is increased by increasing the number of layers. In the requirement table, the half-pitch for 3-D NAND flash should be read as the equivalent density, no longer the lithographic half pitch. It should also be noted that charge-trapping devices are used for almost all 3-D stacking approaches, because (1) leakage of floating-gate tunnel oxide not made on Si substrate is intolerable, and (2) it is very hard, probably not possible, to build complicated floating-gate 3-D structures that can give high enough gate coupling ratio (GCR). Therefore, in the requirement table, only charge-trapping devices are considered with 3-D structures.

FLOATING-GATE NOR FLASH

A NOR Flash cell consists of a single MOS transistor serving both as the cell isolation device and the storage node. The threshold voltage of the transistor is modulated by charge stored in the floating gate and is used as an indication of the storage status. The storage cell may store single-level logic (SLC, actually means bi-level logic 1 and 0) or multiple logic levels (MLC, e.g., (11), (10), (00), and (01)). The memory array is an X-Y cross-wire structure, thus allowing random access of data. Programming is by channel hot electron or other variations of hot-electron generation, and erasing is by Fowler-Nordheim tunneling of electrons out of the floating gate. The generation of hot electrons requires high lateral electric field under the device and is provided by a steep junction profile. This in turn causes short-channel effect and leakage current that produces program disturb. Halo implants are used to control device leakage, and this subsequently reduces the junction breakdown voltage and limits the scaling capability.

The tunnel oxide thickness for the floating-gate device poses a great scaling challenge because leakage through oxide thinner than about 8 nm destroys retention, and there is no currently recognized solution. The short-channel effect caused by thick tunnel oxide and the conflict between hot-carrier generation and junction breakdown severely limit the outlook of NOR flash scaling below 32 nm half-pitch.

High-density applications for NOR flash, especially in the 3G and beyond cell phone market, have also been steadily eroded by increasing popularity of other solutions such as DRAM/NAND SiP, that provide better performance. The weaker market driving force in turn diminishes resources put on meeting technology challenges. In the requirement table, question marks are used in half-pitches < 32 nm to reflect the uncertainties of continued scaling below 32 nm.

CHARGE-TRAPPING (CT) NOR FLASH

The threshold voltage of a device may also be affected by charges stored in a charge-trapping layer, such as SiN. Charge-trapping devices using a SiN as the trapping layer are usually called SONOS, since the device has a SONOS stack—a Si (polycide) gate, a blocking oxide, a nitride storage layer, and a tunnel oxide. The prevailing SONOS device using a relatively thick tunnel oxide in a NOR architecture is commonly known as NROM.[17] NROM uses channel hot electron for programming, and band-to-band tunneling of hot hole for erasing. Since charges injected into the nitride storage layer are well localized near the junctions two bits of information can be stored, one on the source side and one on the drain side, in the same device. The threshold voltage of the device can be read out by shielding the drain side bit with a drain bias and "reverse read" the source side information.

NROM NOR array can be implemented in a virtual ground architecture for which buried diffusion serves as the bit line and the device channel lies along the word-line (polycide) direction. This structure requires neither bit-line contact nor STI in the cell, thus offering a substantially smaller cell than the conventional NOR array. The cross talk between the two storage nodes in the same device cannot be completely eliminated. This so-called "second bit effect" restricts the threshold voltage window each storage node can carry, and the implementation of MLC in NROM poses a higher level of challenge than for floating-gate devices. However, NROM is intrinsically 2-bit/cell and a 4-level MLC implementation results in 4-bit/cell, compared to 16-level MLC required for floating-gate device for the same density. The virtual-ground array offers a factor of 1.5× to 2× density advantage over conventional NOR architecture using the same design rules, and the single poly process reduces the mask layers.

Charge-trapping devices do not have the gate coupling ratio issue floating-gate devices face; however, the scaling challenges are otherwise quite similar. The virtual-ground array and 2-bit/cell operation are sensitive to device leakage and the use of hot carriers for programming and erasing increases the vulnerability to reliability failures. The scaling

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limitation is similar to floating-gate NOR–leakage from short-channel effect and junction breakdown, but without the severe limitation of tunnel oxide scaling the outlook may be somewhat better.

NON-CHARGE-BASED NON-VOLATILE MEMORIES

Since the ultimate scaling limitation for charge-storage devices is too few electrons, devices that provide memory states without electric charges are promising to scale further. Several non-charge-storage memories have been extensively studied and some commercialized, and each has its own merits and unique challenges. Some of these are uniquely suited for special applications and may follow a scaling path independent of NOR and NAND Flash. Some may eventually replace NOR or NAND flash. Logic states that do not depend on charge storage eventually also run into fundamental physics limits. For example, small storage volume may be vulnerable to random thermal noise, such as the case of superparamagnetism limitation for MRAM.

FeRAM devices achieve non-volatility by switching and sensing the polarization state of a ferroelectric capacitor. To read the memory state the hysteresis loop of the ferroelectric capacitor must be traced and the data must be written back after reading. Because of this "destructive read," it is a challenge to find ferroelectric and electrode materials that provide both adequate change in polarization and the necessary stability over extended operating cycles. The ferroelectric materials are foreign to the normal complement of CMOS fabrication materials, and can be degraded by conventional CMOS processing conditions. Thus the ferroelectric materials, buffer materials, and process conditions are still being refined. So far the most advanced FeRAM[18] is substantially less dense than NOR and NAND Flash, fabricated at least one technology generation behind NOR and NAND Flash, and not capable of MLC. Thus the hope for near-term replacement of NOR or NAND Flash has faded. However, FeRAM is fast, low power, and low voltage and thus is suitable for RFID, smart card, ID card, and other embedded applications. In order to achieve density goals with further scaling, the basic geometry of the cell must be modified while maintaining the desired isolation. Recent progress in electrode materials shows promise to thin down the ferroelectric capacitor and extends the viability of 2-D stacked capacitor through most of the near-term years. Beyond this the need for 3-D capacitor still poses steep challenges.

MRAM devices employ a magnetic tunnel junction (MTJ) as the memory element. An MTJ cell consists of two ferromagnetic materials separated by a thin insulating layer that acts as a tunnel barrier. When the magnetic moment of one layer is switched to align with the other layer (or to oppose the direction of the other layer) the effective resistance to current flow through the MTJ changes. The magnitude of the tunneling current can be read to indicate whether a ONE or a ZERO is stored. Field switching MRAM probably is the closest to an ideal "universal memory" since it is non-volatile and fast and can be cycled indefinitely, thus may be used as NVM as well as SRAM and DRAM. However, producing magnetic field in an IC circuit is both difficult and inefficient. Nevertheless, field switching MTJ MRAM has successfully been made into products. In the near term, the challenge will be the achievement of adequate magnetic intensity H fields to accomplish switching in scaled cells, where electromigration limits the current density that can be used. Therefore, it is expected that field switch MTJ MRAM is unlikely to scale beyond 65 nm node, and this is reflected in the requirement table (*Table PIDS5A*). Recent advances in "spin-torque transfer (STT)" approach where a spin-polarized current transfers its angular momentum to the free magnetic layer and thus reverses its polarity without resorting to an external magnetic field offer a new potential solution.[19] For details of STT MRAM please see the *ERD* and *ERM* chapters. Although STT MRAM is still under development and both device and materials study continues, but because of the closeness of product introduction, a special requirement Table PIDS5A is compiled this year, including a comparison with field switching MRAM. During the spin-transfer process, substantial current passes through the MTJ tunnel layer and this stress may reduce the writing endurance.

Table PIDS5A Requirements for Spin-Torque Transfer (STT) MRAM

(Field switching MRAM is shown for reference and is also included in the main NVM table PIDS5.)

PCRAM devices use the resistivity difference between the amorphous and the crystalline states of chalcogenide glass (the most commonly used compound is $Ge_2Sb_2Te_5$, or GST) to store the logic ONE and logic ZERO levels. The device consists of a top electrode, the chalcogenide phase-change layer, and a bottom electrode. The leakage path is cut off by an access transistor (or diode) in series with the phase-change element. The phase-change write operation consists of: (1) RESET, for which the chalcogenide glass is momentarily melted by a short electric pulse and then quickly quenched into amorphous solid with high resistivity, and (2) SET, for which a lower amplitude but longer pulse (> 100 ns) anneals the amorphous phase into low resistance crystalline state. The 1T1R (or 1D1R) cell is larger or smaller than NOR Flash,

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depending on whether MOSFET or BJT (or diode) is used, and the device may be programmed to any final state without erasing the previous state, thus provides substantially faster programming speed. The simple resistor structure and the low-voltage operation also make PCRAM attractive for embedded NVM applications. The major challenges for PCRAM are the high current (fraction of mA) required to reset the phase-change element, and the relatively long set time. Since the volume of phase-change material decreases rapidly with each technology generation, there is hope both the above issues become easier with scaling. Interaction of phase-change material with electrodes may pose long-term reliability issues and limit the cycling endurance and is a major challenge for the maturity of PCRAM. Because PCRAM does not need to operate in page mode (no need to erase) it is a true random access, bit alterable memory like DRAM. This property may help it secure a unique space in application.

RELIABILITY TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

INTRODUCTION

Reliability is an important requirement for almost all users of integrated circuits. The challenge of realizing the required levels of reliability is increasing due to scaling, the introduction of new materials and devices, increasing stresses (fields, current densities, temperatures), and increasing constraints of time and money. Scaling produces ICs with more transistors and more interconnections, both on-chip and in the package. This leads to an increasing number of potential failure sites. Failure mechanisms are also impacted by scaling. For example, the time dependent dielectric breakdown (TDDB) of silicon oxy-nitride gate insulators has changed from electric-field-driven to voltage-driven as the insulator thickness has been scaled below 5 nm. In addition, negative bias temperature instability (NBTI) in *p*-channel devices, which used to be a minor effect when threshold voltages were larger, is now a great concern at the smaller threshold voltages of state-of-the-art devices. When the size of the transistor becomes comparable to or smaller than the values of the fundamental parameters such as mean-free-path of phonons and electrons, and de Broglie wavelength, familiar degradation mechanism may change and new ones may appear. For example, simulation suggests, a hot spot much smaller than the phonon mean-free-path exist around the drain junction. The temperature of such a hot spot may be hundreds of degree higher than predicted by heat diffusion, and can significantly affect the transistor reliability.

Increase in variability is expected as a result of scaling. Reliability mechanisms that are sensitive to device parameters will couple with the variability and be magnified, making reliability projection with limited number of measurements extremely difficult.

Scaling may also leads to an effective increase of the stress factors. First, the current density is increasing and this increase impacts interconnect reliability. Second, voltages are often scaled down more slowly than dimensions, leading to increased electric fields that impact insulator reliability. Third, scaling has led to increasing power dissipation that result in higher chip temperatures, larger temperature cycles, and increased thermal gradients, all of which impact multiple failure mechanisms. The temperature effects are further aggravated by the reduced thermal conductivity that accompanies the reduction in the dielectric constant of the dielectrics between metal lines.

There are even more profound reliability challenges associated with revolutionary changes associated with new materials and new devices. Recognized failure mechanisms can change. New materials, such as high-κ and low-κ dielectrics or metal gates, and new device architectures, such as multi-gate or FinFETs, can introduce new failure mechanisms or change the behavior of well-known failure mechanisms such as TDDB or BTI. For example, with the transition from oxynitride/poly-Si gates to high-κ/metal gates, a new failure mechanism, positive bias temperature instability (PBTI) in *n*-channel devices, has appeared. In addition, the nature of TDDB changes from progressive or multiple breakdowns, observed in poly-Si gate MOSFETs, to a more abrupt breakdown. The poor mechanical and thermal properties of low-κ intermetal dielectrics can lead to mechanical failure mechanisms not seen in silicon dioxide intermetal dielectrics.

Moreover the speed of introduction of these new materials and devices is exceeding our capability to build up learning on new failure mechanisms and physics, whereas the failure rate requirement are become more and more demanding. The impact of an unrecognized failure mechanism that made it into end products would be significant.

These reliability challenges will be exacerbated by the need to introduce multiple major technology changes in a brief period of time. Interactions between changes can increase the difficulty of understanding and controlling failure modes. Furthermore, having to deal simultaneously with several major issues will tax limited reliability resources.

There is consensus that one of the route to continue to the increase functionality of an IC is to integrate sensors and actuators on top of the CMOS platform. Such kind of “More than Moore” approach will greatly increase the complexity of reliability assurance. It is highly likely that such technology will come on line before the end of the road map and we

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must prepare for it. The likelihood that each sensor/actuator brings along a unique set of reliability problem is high and will present a whole new challenge to the reliability effort.

RELIABILITY REQUIREMENTS

Reliability requirements are highly application dependent. For most customers, current overall chip reliability levels (including packaging reliability) need to be maintained over the next fifteen years in spite of the reliability risk inherent in massive technology changes. However, there are also niche markets that require reliability levels to improve. Applications that require higher reliability levels, harsher environments, and/or longer lifetimes are more difficult than the mainstream office and mobile applications. Note that even with constant overall chip reliability levels, there must be continuous improvement in the reliability per transistor and the reliability per meter of interconnect because of scaling. Meeting reliability specifications is a critical customer requirement and failure to meet reliability requirements can be catastrophic.

These customer requirements flow down into requirements for manufacturers that rely on an in-depth knowledge of the physics of all the relevant failure modes and a powerful reliability engineering capability in design-for-reliability, building-in-reliability, reliability qualification, and defect screening to meet them. There are some significant gaps in these capabilities today. Furthermore, these gaps will become even larger with the introduction of new materials and new device structures. Inadequate reliability tools lead to unnecessary performance penalties and/or unnecessary risks.

Reliability qualification always involves some risk. There is a risk of qualifying a technology that does not, in fact, meet reliability requirements or a risk of rejecting a technology that does, in fact, meet requirements. At any point in time a qualification can be attempted on a new technology. However, the risk associated with that qualification can be large. The level of risk is directly related to the quality of the reliability physics and reliability engineering knowledge base and capabilities.

The color-coding of the Reliability technology requirements is meant to represent the reliability risk associated with incomplete knowledge and tools for new materials and devices. The progression from white to yellow to striped indicates a growing reliability risk. The requirements first turn to yellow (Manufacturing Solutions are Known) in 2009 indicating a relative smaller risk associated with scaling, increased power. It is expected more manufacturers will introduce high-κ/metal-gate transistor stacks during the time frame of now to 2012, which will present a considerable reliability risk. The risk assessment is, naturally, not very reliable for there are a number of known reliability issues that are still poorly understood. A case in point is the strong acceleration of NBTI in the presence of a drain bias, particularly for highly scaled devices. The assessment of moderate risk is a reflection of the awareness level of the problems. Solving these problems requires considerable effort and resources.

The requirements then turn to striped (Interim Solutions Known) in 2013. This date is approximate. It is meant to represent the point in time where novel devices or materials are introduced (e.g., optical interconnect or a non-CMOS transistor or memory). As mentioned above these changes present a considerable reliability risk and require a considerable lead time to develop the needed capabilities in reliability physics and reliability engineering. Since we do not know exactly what these disruptive technologies will be and when they will be introduced, we have no way of knowing in advance the reliability risk. Solid red reflects the combination of increase variability, unknown reliability behavior from new materials and new structures, and the interaction between them. It signifies the greatly increased unknown rather than known issues that do not have known solution. The poorer the quality of our reliability knowledge is, the greater the reliability risks.

Table PIDS6 Reliability Technology Requirements

RELIABILITY POTENTIAL SOLUTIONS

The most effective way to meet requirements is to have complete built-in-reliability and design-for-reliability solutions available at the start of the development of each new technology generation. This would enable finding the optimum reliability/performance/power choice and would enable designing a manufacturing process that can consistently have high reliability yields. Unfortunately, there are serious gaps in these capabilities today and these gaps are likely to grow even larger in the future. The penalty will be an increasing risk of reliability problems and a reduced ability to push performance, cost and time-to-market.

It is commonly thought that the ultimate nanoscale device will have high degree of variation and high percentage of non-functional devices right from the start. This is viewed as an intrinsic nature of devices at the molecular scale. As a result it

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will not be possible any longer for designer to take into account a 'worst case' design window, because this would jeopardize the performance of the circuits too much. To deal with it, a complete paradigm change in circuit and system design will therefore be needed. While we are not there yet, the increase in variability is clearly already a reliability problem that is taxing the ability of most manufacturers. This is because variability degrades the accuracy of lifetime projection, forcing a dramatic increase in the number of devices tested. The coupling between variability and reliability is squeezing out the benefit of scaling. At some point, perhaps before the end of the roadmap, the cost of ensuring each and every one of the transistors in a large integrated circuit to function within specification may become too high to be practical. As a result, the fundamental philosophy of how to achieve product reliability may need to be changed. One potential solution would be to integrate so-called knobs and monitors in the circuits that are sensing circuit parts that are running out of performance and then during runtime can change the biasing of the circuits. Such solutions needs to be further explored and developed. Ultimately, circuits that can dynamically reconfigure itself to avoid failing and failed devices (or to change/improve functionality) will be needed.

Some small changes may already be underway quietly. A first step may be simply to fine-tune the reliability requirements to trim out the excess margin. Perhaps even have product specific reliability specifications. More sophisticated approaches involve fault-tolerant design, fault-tolerant architecture, and fault-tolerant systems. Research in this direction has increased substantially. However, the gap between device reliability and system reliability is very large. There is a strong need for device reliability investigation to address the impact on circuits. Recent increase in using circuits such as SRAM and ring oscillator to look at many of the known device reliability issue is a good sign. More device reliability research is needed to address the circuit and perhaps system aspects. For example, most of the device reliability studies are based on quasi-DC measurements. There is no substantial research on the impact of degradation on devices at circuit operation speed. This gap in measurement speed make modeling the impact of device degradation on circuit performance difficult and risky.

In the mean time, we must meet the conventional reliability requirements. That means an in-depth understanding of the physics of each failure mechanism and the development of powerful and practical reliability engineering tools. Historically, it has taken many years (typically a decade) before the start of production for a new technology generation to develop the needed capabilities (R&D is conducted on characterizing failure modes, deriving validated, predictive models and developing design for reliability and reliability TCAD tools.) The ability to qualify technologies has improved, but there still are significant gaps.

There is a limit to how fast reliability capabilities can be developed, especially for major technology discontinuities such as alternate gate insulators or non-traditional devices. An eleventh-hour "sprint" to try and qualify major technology shifts will be highly problematical without the pre-existing and adequate reliability knowledge base.

For the reliability capabilities to catch up requires a substantial increase in reliability research-development-application and cleverness in acquiring the needed capabilities in much less than the historic time scales. Work is needed on rapid characterization techniques, validated models, and design tools for each failure mechanism. The impact of new materials like Cu, low-κ dielectric and alternate gate dielectrics needs particular attention. Breakthroughs may be needed to develop design for reliability tools that can provide a high fidelity simulation of a large fraction of an IC in a reasonable time. As mentioned above, increased reliability resources also will be needed to handle the introduction of a large number of major technology changes in a brief period of time.

The needs are clearly many, but a specific one is the optimal reliability evaluation methodology, which would deliver relevant long-term degradation assessment while preventing excessive accelerated testing which may produce misleading results. This need is driven by the decreasing process margin and increasing variability, which greatly degrades the accuracy of lifetime projection from a standard sample size. The ability to stress a large number of devices simultaneously is highly desirable, particularly for long term reliability characterization. Doing it at manageable cost is a challenge that is very difficult to meet and becoming more so as we migrate to more advanced technology nodes. A breakthrough in testing technology is badly needed to address this problem.

CROSS TWG ISSUES

MODELING AND SIMULATION

Currently, PIDS uses physical process parameters mostly provided by the Front End Processes group, and uses *MASTAR* to calculate the device *I-V* characteristics. Since MASTAR is based on analytical equations, even though it had been calibrated with real device data, prediction into the far future has some uncertainty. There might be advantages in the future to consider a full-blown physics-based TCAD device simulator to carry on such device simulations. Ideally, TCAD process simulation tool is also used to provide proper doping levels and geometries. But in order to do these, these

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simulation tools need to be enhanced to deal with the key innovations requested by the *PIDS* section, including enhanced mobility, high-κ gate dielectrics, metal-gate electrodes, non-classical CMOS structures (ultra-thin body fully depleted SOI and multi-gate MOSFETs), and quasi-ballistic transport leading to enhanced saturation current, etc. These innovations will collectively drive major changes in process, materials, physics, design, etc. Similar features on III-V and Ge materials are also needed to justify as alternate channel materials. Other long-term issues requiring enhanced modeling and simulation include atomic-level fluctuations, statistical process variations, new interconnect schemes, and mixed-signal device technology. With the shrinking of feature sizes, new process steps, architectures and materials reliability issues at the device, interconnect, and circuit levels will become even more important and will need support from modeling and simulation to achieve the development speed required. Especially for devices that use SOI material, existing models (e.g., for dopant diffusion and activation, carrier transport or for stress) must be extended to cope with interface effects, which become increasingly important compared with bulk properties. Finally, non-classical CMOS devices require the development of appropriate compact models to support their introduction.

INTER-FOCUS ITWG DISCUSSION

FRONT END PROCESSES

There is strong linkage between the *Front End Processes (FEP)* and the PIDS chapters. Key areas of joint concern include predicting introduction years of SOI and multi-gate structures. For bulk devices, we face the difficult trade-offs of very high channel doping required to control short-channel effects. For ultra-thin body fully depleted SOI and multi-gate MOSFETs, the key issue is controlling the required ultra-thin silicon body. All devices face the stringent requirement of source/drain series resistance, especially challenging with ultra-thin bodies. Another concern is V_{dd} scaling which affects almost all parameters, especially current drive, speed, EOT, and power density. Both groups feel that a device power metric needs to be added. For DRAMs, key areas of joint concern include implementation of Metal-Insulator-Metal (MIM) storage capacitors with high-κ dielectric to scale the equivalent oxide thickness aggressively, as well as keeping the leakage of the access transistor ultra-low as the DRAM is scaled. For non-volatile memory, a key issue of joint concern involves the difficult trade-offs in scaling the interpoly and the tunneling dielectrics in flash memories.

IMPACT OF FUTURE EMERGING RESEARCH DEVICES

EMERGING RESEARCH DEVICES

The *Emerging Research Devices (ERD) chapter* describes and evaluates potential technologies, including devices and architectures, beyond the current standard silicon CMOS technology. As such, it is concerned with the potential successor(s) to the CMOS described in the PIDS chapter. Toward or beyond the end of this Roadmap, when CMOS scaling will likely become ineffective and/or prohibitively costly, some version(s) of ERD technology will presumably be needed if the industry is to continue to enjoy rapid improvements in performance, lower power dissipation, and cost per function, and higher functional density. Hence, the PIDS potential solutions tables include ERD solutions late in the Roadmap time period, and refer to the ERD chapter for details. Similarly, material-related topics come from the *Emerging Research Materials (ERM) chapter*. One issue to be addressed is to start a mechanism for PIDS to receive potential devices and materials that have been transited out of the ERD and ERM tables.

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FOLDER 16



INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2010 UPDATE

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Update to Design Chapter	2009 Design
2010 Test and Test Equipment Tables Update file	2009 Test and Test Equipment
2010 Process Integration, Devices, and Structures (PIDS)Tables Update file	2009 Process Integration, Devices, and Structures (PIDS)
2010 Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (RF A/MS) Tables Update file	2009 Radio Frequency and Analog/Mixed-Signal Technologies for Wireless Communication
Emerging Research Devices (ERD) and Emerging Research Materials (ERM) 2010 Memory Assessment Workshop Summary	2009 Emerging Research Devices
	2009 Emerging Research Materials
2010 Front End Processes (FEP) Tables Update file	2009 Front End Processes
2010 Lithography Tables Update file	2009 Lithography
2010 Interconnect Tables Update file	2009 Interconnect
2010 Factory Integration Tables Update file	2009 Factory Integration
2010 Assembly and Packaging Tables Update file	2009 Assembly and Packaging
2010 Environment, Safety, and Health (ESH) Tables Update file	2009 Environment, Safety, and Health
2010 Yield Enhancement Tables Update file	2009 Yield Enhancement
2010 Metrology Tables Update file	2009 Metrology
2010 Modeling and Simulation Tables Update file	2009 Modeling and Simulation

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OVERVIEW

For more than four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table A with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles roughly every 24 months). The most significant trend is the decreasing cost-per-function, which has led to significant improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics.

Table A Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor throughput**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last three decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for Semiconductors (NTRS), which had 1992, 1994, and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of the Roadmap and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999. Since then, the ITRS has been updated in even-numbered years and fully revised in odd-numbered years. The overall objective of the ITRS is to present industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, universities, governments, and other research providers or funders. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that most need research breakthroughs.

The ITRS is a dynamic process, evident by the evolution of the ITRS documents. The ITRS reflects the semiconductor industry migration from geometrical scaling to equivalent scaling. Geometrical scaling [such as Moore's Law] has guided targets for the previous 30 years, and will continue in many aspects of chip manufacture. Equivalent scaling targets, such as improving performance through innovative design, software solutions, and innovative processing, will increasingly guide the semiconductor industry in this and the subsequent decade. Since 2001 the ITRS has responded by introducing new chapters on System Drivers (2001), Emerging Research Devices and Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (2005), and, in 2007, Emerging Research Materials, to better reflect this evolution of the semiconductor industry. The ITRS 2010 Update will also begin to address the subject of Energy.

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of electronics would further reduce the cost per function (historically, ~25–29% per year) and promote market growth for integrated circuits (historically averaging ~17% per year, but maturing to slower growth in more recent history). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?"

In order to properly represent the continuously evolving facets of the semiconductor industry as it morphs into new and more functional devices in response to the broadening requirements of new customers, the 2010 ITRS has addressed the concept of Functional Diversification ("More than Moore"). This new definition (MtM) addresses and emerging category of devices that incorporate functionalities that does not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution and ultimately into Stacked Chip SoC (SCS).

It is forecasted that by the end of the next decade it will be necessary to augment the capabilities of the CMOS process by introducing multiple new devices that will hopefully realize some properties beyond the ones of CMOS devices. However, it is believed that most likely these new devices will not have all the properties of CMOS devices and therefore it is anticipated that heterogeneous integration either at the chip level or at the package level will integrate these new capabilities around a CMOS core.

The participation and continued consensus of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. ensure that the 2010 ITRS remains the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The complete ITRS 2010 Update and past editions of the ITRS are available for viewing and printing as electronic documents at the Internet web site ***http://www.itrs.net***.

Link to 2009 Executive Summary.

SPECIAL TOPICS

ENERGY

Energy consumption has become an increasingly important topic of public discussion in recent years due, in part, to concerns regarding global CO_2 emission. Since semiconductor electronics are broadly applicable to energy collection, conversion, storage, transmission, and consumption/usage, it is not surprising that the ITRS addresses many factors of significance to energy issues. In general, the ITRS documents the impressive trends and, more importantly, sets aggressive targets for future electronics energy efficiency, for example, computational energy/operation (per logic and per memory-bit state changes). The most detailed targets relate directly to semiconductor materials, process, and device technologies, which form the bases of integrated-circuit manufacturing and components, respectively.

At the next level, the ITRS addresses integrated circuit design and its system-level drivers. In both the ITRS Design and the ITRS System Driver chapters, there is increasingly direct influence of energy factors on design technologies, which started a number of years ago. Power consumption is now one of the major constraints in chip design, and the ITRS has identified it as one of the top three overall challenges for the last seven years. Leakage power consumption, including its variability, has been identified as a clear long-term threat and a focus topic for design technology in the next 15 years. The connection with the energy challenge is based on the increasing worldwide usage of information technology devices.

In addition to improved efficiency of the basic components (i.e., switches, wires, and memory bits) and of the circuits they compose, the major favorable impact on energy usage of advancing semiconductor technology is in the applications of the circuits themselves, which are often designed specifically to improve the energy efficiency of end-equipment systems which they control. For example, microcontrollers, signal processors, and power/battery management circuits are key to the efficiency of communications systems, household appliances, transportation (e.g., cars), industrial machines, etc.

The ITRS also addresses the minimization of energy usage in semiconductor manufacturing. In particular, the Factory Integration and the Environmental, Safety, and Health (ESH) chapters present goals for further reducing the amount of energy and other resources required to produce integrated circuits and to generally increase the environmental friendliness of IC fabrication.

The ITRS will continue to focus diligently on energy-related issues along the directions outlined above, and to make important contributions to the energy challenges facing the world. In particular, near its 15-year horizon, the ITRS Emerging Research Devices (ERD) and Emerging Research Materials (ERM) chapters are tracking developments for potential beyond-CMOS devices that may greatly extend the energy efficiency of information technologies.

TECHNOLOGY PACING

The ORTC Technology Pacing Trends drivers for the 2010 Update are unchanged from the published 2009 ITRS tables, except for some corrections on Tables ORTC-2C and 2D. The corrections to ORTC -2C, and 2D do not affect the ITWG table update drivers for the ITRS 2010 Update (See additional detail in the *2010 ITRS ORTC section* below.)

However, the ITRS International Roadmap Committee (IRC) and the PIDS ITWG Team felt it was important for the 2010 Update readers to also be aware of recent 2011 technology pacing update proposals, which are based on real-time changes in the manufacturing technology environment, and to know that the ITRS is responding to the industry pacing with a preview of several key changes, with more details provided in the next ITRS 2011 edition..

The PIDS survey team has made proposals to change the memory technology pacing drivers, which will affect the overall effort of ITWG work in the 2011 ITRS edition. , The preparation for the 2011 edition work began with a "Kick-off" workshop meeting on December 1–2, 2010 ITRS meetings in Tsukuba, Japan.

The PIDS projections for the 2011 proposed technology trend changes are identified below; and are also summarized as data in ORTC table form, Figure 1 and portrayed in graphical and overlay form, Figure 2. The projections are also included in the ***2010 ITRS PIDS update tables***. The remaining ITRS ITWGs will review and respond to these proposals in their tables and text during the 2011 ITRS edition effort. The following is a brief summary of the PIDS ITWG proposals:

PIDS DRAM Metal 1 (M1) Contacted Half-Pitch Proposal:

1. ~1-year pull-in to 2010/42 nm
2. Then 3-year technology cycle (.5× per 2 cycles) out to 2024
3. Design Factor $4f^2$ delayed until 2013

PIDS Flash Poly Un-contacted Half-Pitch Proposal:

1. ~2-year pull-in to 2010/26 nm
2. Then ~4-year cycle to 2017/14 nm
3. Then back on 2009 Trend at 3-year cycle to 2022/8 nm
4. Then flat through end of roadmap at 8 nm due to physics limits of voltage and electron storage
5. The multi-level-cell (MLC) 4 bits/cell is delayed to 2019

The 2010 ORTC Update MPU M1 half-pitch and gate length trends remain unchanged from the 2009 ITRS; however, new surveys are underway and new proposals will be considered for possible changes during the 2011 ITRS work, including:

1. Evaluation of the "Two-company" ITRS rule for the M1 contacted half-pitch and other key trends;
2. Evaluation of the alignment of industry published "nodes" trends and the relationship between "Moore's Law" high-density and high-performance drivers with low-power needs in both high-performance and mobile applications
    a. Consideration will also be given in the 2011 ORTC and ITWG tables to possible technology pacing driver segment convergence—MPU high performance, MPU/ASIC low operating power (LOP), and MPU/ASIC low standby power (LSTP) into two segments.
3. Alignment and trade-off with the "equivalent scaling" technology roadmap trends (see also the "Equivalent Scaling" special topic below)

	Table ORTC-1 ITRS Technology Trend Targets [including PIDS 2011 Roadmap Flash and DRAM Trend Driver Proposals]								
	Year of Production	2009	2010	2011	2012	2013	2014	2015	2016
2010 ORTC	Flash ½ Pitch (nm) (un-contacted Poly)(f) [A]	38	32	28	25	23	20	18	15.9
2010 PIDS Projection based on survey data	Flash ½ Pitch (nm) (un-contacted Poly)(f) [B]	N/A	26	24	22	20	19	18	16
2010 WAS	DRAM ½ Pitch (nm) (contacted) [C]	52	45	40	36	32	28	25	22.5
2010 PIDS Projection based on survey data	DRAM ½ Pitch (nm) (contacted) [D]	N/A	42	36	31	28	25	24.0	21.0
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) [1, 2]	54	45	38	32	27	24	21	18.9
	MPU Printed Gate Length (GLpr) (nm) ††[1]	47	41	35	31	28	25	22	19.8
	MPU Physical Gate Length (GLph) (nm) [1]	29	27	24	22	20	18	17	15.3
	ASIC/Low Operating Power Printed Gate Length (nm) ††[1]	54	47	41	35	31	25	22	19.8
	ASIC/Low Operating Power Physical Gate Length (nm) [1]	32	29	27	24	22	18	17	15.3
	ASIC/Low Standby Power Physical Gate Length (nm) [1]	38	32	29	27	22	18	17	15.3
	MPU Etch Ratio GLpr/GLph (nm) [1]	1.6039	1.5296	1.4588	1.4237	1.3895	1.3561	1.3235	1.2917

2017	2018	2019	2020	2021	2022	2023	2024	2025
14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3	N/A
14	13	12	11	9	8	8	8	N/A
20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	N/A
18.0	16.0	14.0	13.0	12.0	10.0	9.0	8.0	N/A
16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5	N/A
17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9	N/A
14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	N/A
17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9	N/A
14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	N/A
14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4	N/A
1.2607	1.2304	1.2008	1.1720	1.1438	1.1163	1.0895	1.0633	N/A

Figure 1 ORTC Table 1 with PIDS update proposals for 2011 ITRS effort)

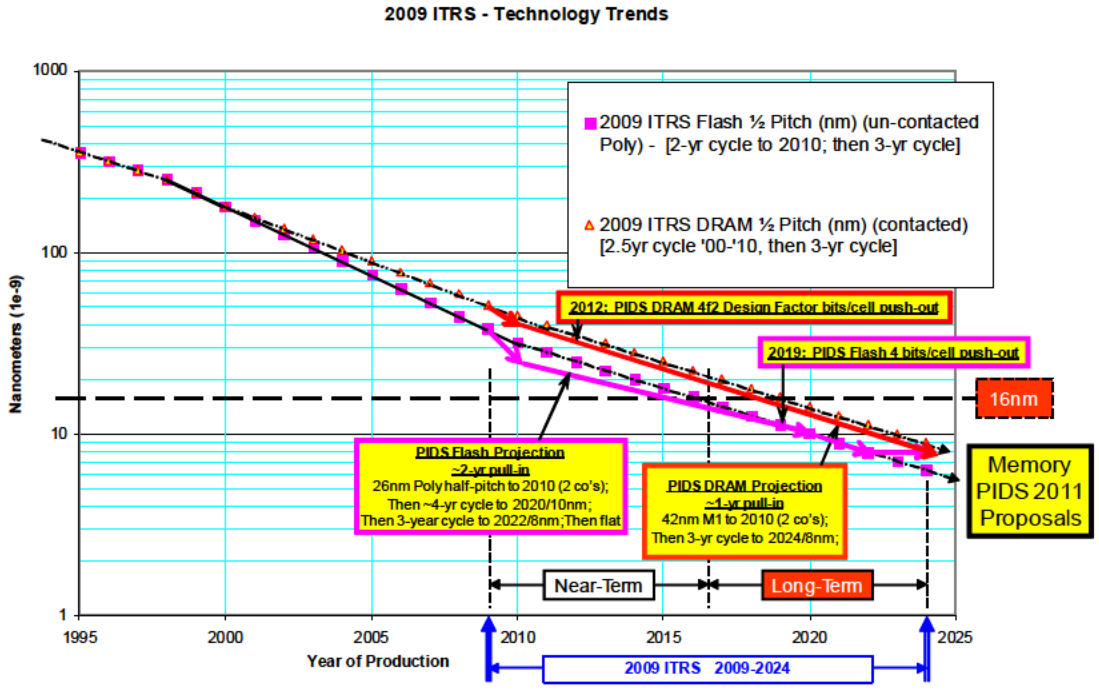


Figure 2 ORTC Table 1 Graphical Trends (including overlay of PIDS update proposals for 2011 ITRS effort)

Link to Overall Roadmap Technology Characteristics section

EQUIVALENT SCALING

The ORTC Technology Pacing Trends drivers for the 2010 ITRS Roadmap Update also include "equivalent scaling" technology introductions, along with the classical "Moore's Law" dimensional trends (***Refer to the Glossary for additional definition detail).*** Also see examples of "equivalent scaling" technology included in Figure 3.

Individual companies are on different technology implementation timing paces for differing reasons, based on their product market needs, competitive position, and their company technology roadmap differences. During the 2010 ITRS update work, the ITRS IRC determined that clarification and flexibility were needed to properly communicate the ITRS vision for various equivalent scaling pathways. These "Equivalent Scaling Roadmap" pathways were first shown in the Figure 8c of the 2009 Executive summary and needed to be updated to current industry status.

In particular, the pathways for bulk CMOS and SOI needed to be separated, and the grouping of associated technologies aided the simplification of the graphic. This clarification and simplification was in preparation for the ITRS 2011 edition work, which would do the following:

1. Reposition the technology insertion timing for the possible relationship with "mix and match" trade-offs between "equivalent scaling" technology and dimensional technology progressions (for "Moore's Law" density requirements versus power and performance management trade-offs). This is especially true when taking into account the impact of recent memory technology pacing proposals and anticipated proposals on logic technology pacing
2. Prepare the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) ITWGS for their cross-TWG negotiations with the Process and Integrated Devices (PIDS) and Front-End Processes (FEP) ITWGs to transfer responsibility for new high-mobility gate channel materials (i.e., Germanium channel and III/V materials) and new logic switch and memory storage candidates from the "Beyond CMOS" region.

The work of clarification and simplification of the "Equivalent Scaling Technology Roadmap" resulted in a preliminary consensus represented in Figure 3. That figure will receive additional consensus-building during the 2011 ITRS work, including the development of agreement on additional timing shifting of the 3-dimensional multi-gate transistor technology insertion. See Figure 3.

The dimensional industry "node" and ITRS technology pacing targets are also shown in Figure 3, not necessarily to suggest an absolute relationship/linkage between the equivalent scaling and dimensional scaling timing. Rather it is shown for convenience of the reader to view what is in fact the present timing of the latest dimensional and technology pathways to date. Please note that the dimensional pacing is based on the 2009 ITRS and does not yet include the proposals for the memory DRAM and Flash proposals under consideration for the 2011 ITRS edition work.

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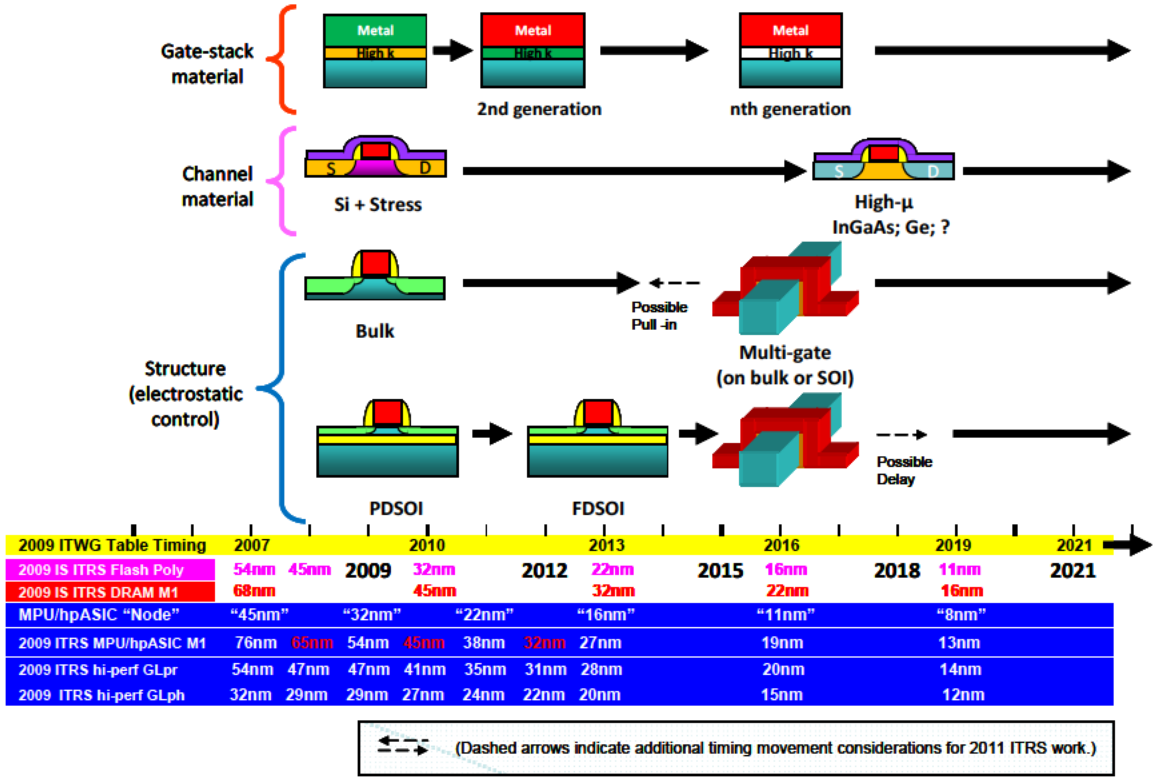


Figure 3 *ORTC Table 1 Graphical Trends (including overlay of 2009 industry logic "nodes" and ITRS trends for comparison)*

Please see the PIDS, FEP, ERD, and ERM chapters' text and tables for additional details.

MORE THAN MOORE

Link to More than Moore white paper

During the year 2010, the ITRS community has been continuing its active engagement in the investigation of the "More than Moore" (MtM) concept, which was first introduced in the 2005 ITRS.

Given the benefits that roadmapping has brought to the semiconductor industry so far, the International Roadmap Committee clearly wants to include more significant parts of the "More-than-Moore" domain in the work of the ITRS community. In particular, it has tackled the difficult question of how to build a roadmap (or several roadmaps) for the various "More than Moore" technologies. Indeed, in the absence of a single law of expected progress such as Moore's law for the many devices and technologies that enable the "More than Moore" trends, a different methodology is needed to identify and guide roadmap efforts in the MtM domain.

The ITRS has therefore elaborated *a white paper, available at this link on the ITRS website,* to propose a methodology that helps the ITRS community to identify those MtM technologies for which a roadmapping effort is feasible and desirable. It departs from the traditional "technology push" approach that the ITRS has followed for roadmapping the continuation of Moore's law (i.e., linear scaling), and requires to collect both technical and market data, thus implying the involvement of many actors beyond the ITRS historical membership, and representing the application domains. In particular, the ITRS has been actively engaging with other entities involved in roadmapping, such as *the International Electronics Manufacturing Initiative (iNEMI).*

It should be stressed here that the white paper is not intended to be the "final words" on MtM roadmapping methodology, but rather a way to collect more inputs and advices on what promises to be a very challenging task.

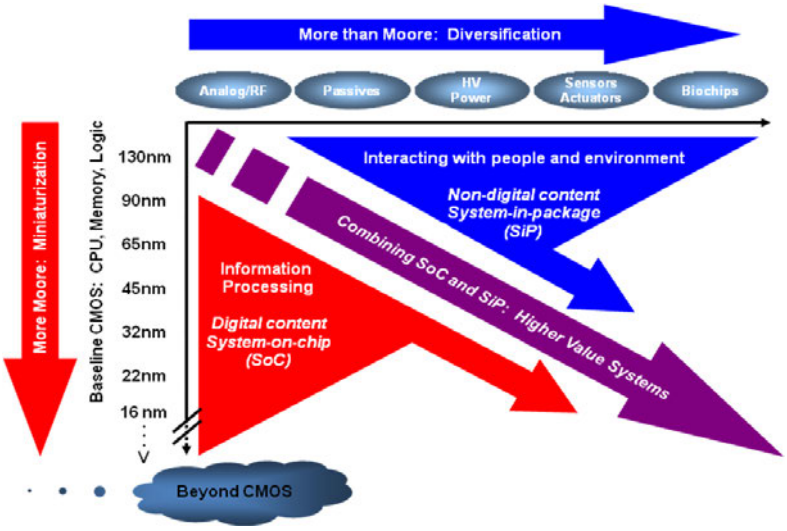


Figure 4 The Concept of Moore's Law and More

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS —2010 UPDATE

SUMMARY

The ITRS Overall Roadmap Technology Characteristics (ORTC) section provides both originating guidance from ORTC Product Models and also consolidates items from other ITRS International Technology Working Group (ITWG) tables.

The metric values of the ORTC tables can be found throughout the 2010 Update Roadmap in greater detail in each technology working group update section. The information in this section is intended to highlight the current rapid pace of advancement in semiconductor technology. It represents a completion of the revision update work that began in 2010, and summarizes the major changes to the ORTC Tables. This 2010 Update version of the ORTC summary is abbreviated from the 2009 ITRS edition Executive Summary, which can be viewed online at ***www.itrs.net***. Additionally, the ORTC Glossary has been included in this 2010 Overview from 2009 ITRS Executive Summary.

There continues to be confusion in the industry regarding individual company public press announcements of their "node" progress and timing, which may or may not align with the ITRS definitions and specific targets. Industry technology progress alignment and communication continues to be a challenge for the ITRS and is further complicated by the recent trends to trade off historical dimensional scaling with technology solutions known as "equivalent scaling" (examples: copper interconnect, strained silicon, metal gate, high-κ gate dielectric, fully-depleted SOI; multi-gate transistors; etc.).

There will also be added complication to the technology progression tracking issue as the market and company public and media relations attempt to describe and connect "design equivalent scaling" and the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) "Beyond CMOS "potential solutions to their chapters and their cross-ITWG modeling with Process Integration, Devices, and Structures (PIDS) and Front End Processes (FEP). New "design equivalent scaling" definitions had been added to the ITRS definitions for "More Moore Geometrical and Equivalent Scaling;" and "More than Moore Functional Diversification" to the Glossary in the ITRS 2009 edition to continue to address the subtleties and for needed clarification of the definitions of the new "More Moore" and "More than Moore" solutions.

2010 UPDATE NOTES

The following notes highlight the key updates for each table set. ***To download or review the 2010 Update ORTC tables , select this link.***

TABLE 1—"PRODUCT GENERATIONS AND CHIP SIZE MODEL TECHNOLOGY TREND TARGETS"

For the 2010 Update version, the ORTC 2009 tables remain unchanged in guiding the 2010 TWG table update work. Flash Un-contacted Poly Half Pitch is unchanged from the 2009 ITRS, and after accelerating in the 2009 version one year to 2010/32 nm, the Flash technology pacing trend goes forward from 2010 at a 3-year cycle pace. The DRAM M1 Contacted half-pitch also remains unchanged for the 2010 update, and based on the 2007 PIDS TWG survey recommendations, is on a 2.5-year cycle through 2010/45 nm, then returns (unchanged) to a 3-year cycle. (See Figures 5a and 5b.)

However, it must be noted that the PIDS ITWG has updated their survey in 2010 and have included their proposals for revision of the 2011 tables in their 2010 Update tables (see the Technology Pacing in the Special Topics section above). This is atypical of ITRS Update work (due to the potential for confusion), but was done in order to make the ITRS 2010 Update readers aware of the dramatic changes that have occurred this year. This will also allow the other TWGs dependent on these changes to prepare for the 2011 ITRS Full Renewal work that will kick off in December in Tokyo.

A preview of these proposed-for 2011-work PIDS changes is noted above in Figures 1 and 2, which include preliminary 2011 ORTC Table 1 line items, and also proposal trend graphics overlaid on the 2009 and 2010 unchanged trends.

The MPU Contacted M1 Half Pitch is also unchanged from the 2009 ITRS, and continues on a 2-year cycle until 2013/29 nm, when the trend shifts to a 3-year cycle through the remainder of the ITRS timeframe (2024);

The most significant impact to the 2008 and 2009 ITRS editions was due to revisions of the ORTC Table 1 physical and printed gate length trends. Data from surveys in 2008 and 2009 by the PIDS and FEP and Design TWGs indicated that

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the final physical gate length reduction had slowed dramatically from past anticipated trends, resulting in revisions that affected many of the 2009 ITRS Update tables, and are used as drivers again for the 2010 ITWG Update tables:

- MPU Physical Gate Length (GLph) is now calculated based on a 3.8-year cycle after 2007 to align on a best-fit with the PIDS survey data;
- MPU Printed (Lithography) Gate Length (GLpr) is based on the Lithography TWG Proposal, and is unchanged in the 2009 and 2010 editions. It should be noted as an important reminder to the reader that the gate length trends are no longer based on a parallel relationship to the MPU/DRAM Half Pitch; therefore, the 1.6818 GLpr/GLph past constant ratio is a variable shrinking ratio throughout the roadmap period*.
- ASIC Low Operating Power Printed Gate Length is unchanged and was adjusted in the 2009 version for consistency with the 3.8-year-cycle MPU High Performance Printed Gate Length and also with the new Litho TWG variable GLpr/GLph etch ratio*;
- ASIC Low Standby Power Physical Gate Length was added in the 2009 edition as a new ORTC Line Item and also remains unchanged in 2010;
- *The MPU High Performance variable GLpr/GLph etch ratio (versus fixed ratio) continues as a new ORTC Line Item in the 2009 and 2010 version;
- The impact of the physical and printed gate length changes are included with additional table detail and notes in the PIDS and FEP and Lithography section tables and notes.
    - Included in the 2009 ITRS edition and continued unchanged in the 2010 Update edition is a more robust FEP, PIDS, and Design model impact update; including the relationship with "equivalent scaling" (next generation metal gate and gate high-κ dielectrics, FDSOI, multi-gate transistors, etc.) trade-offs and the timing placement for future "equivalent scaling" technologies as potential solutions for performance and power management.

Please read the Equivalent Scaling special topic above and make note of 2010 revision proposals of the Equivalent Scaling Technology Roadmap graphic, Figure 3.

TABLES 2A THROUGH 2D—"PRODUCT GENERATIONS (DRAM, FLASH, MPU/ASIC) AND CHIP SIZE MODEL TECHNOLOGY TRENDS"

In 2010, there were no changes to the 2009 ORTC DRAM and Flash technology trend and product models. As a result, the memory product tables, ORTC -2A and 2B, which are sourced from those models, remain unchanged. (See Figures 6 and 7a.)

However, in the 2011 ITRS work, begun in December 2010, these ORTC product models will be updated to reflect the impact of the new PIDS memory DRAM and Flash projection proposals noted in the Technology Pacing special topic above.

The MPU product models in Tables ORTC-2C and 2D underwent some corrections which affected the introduction-level trends, but did not impact the work of the 2010 Update of the ITWG Tables, since the ITWG tables are driven by the ORTC production-level model trends. The production-level trends remained unchanged from the 2009 ITRS. See Figures 7a and 7b. (The previous ITRS graphics of combined memory and logic half-pitch and gate-length trends were replaced in the 2009 ITRS edition by separate Figures 5a and 5b and, similarly, the previously combined memory and logic functions per chip and chip sizes trends graphics were updated in the 2009 ITRS edition, too, as shown in Figures 7a and 7b.)

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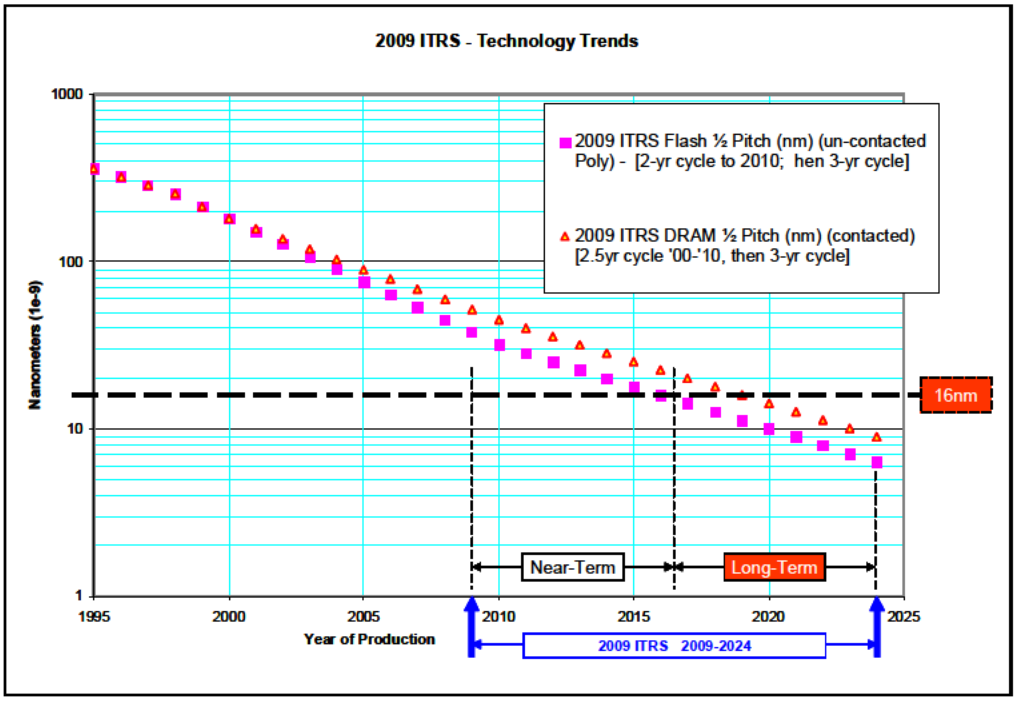


Figure 5a DRAM and Flash Memory Half Pitch Trends

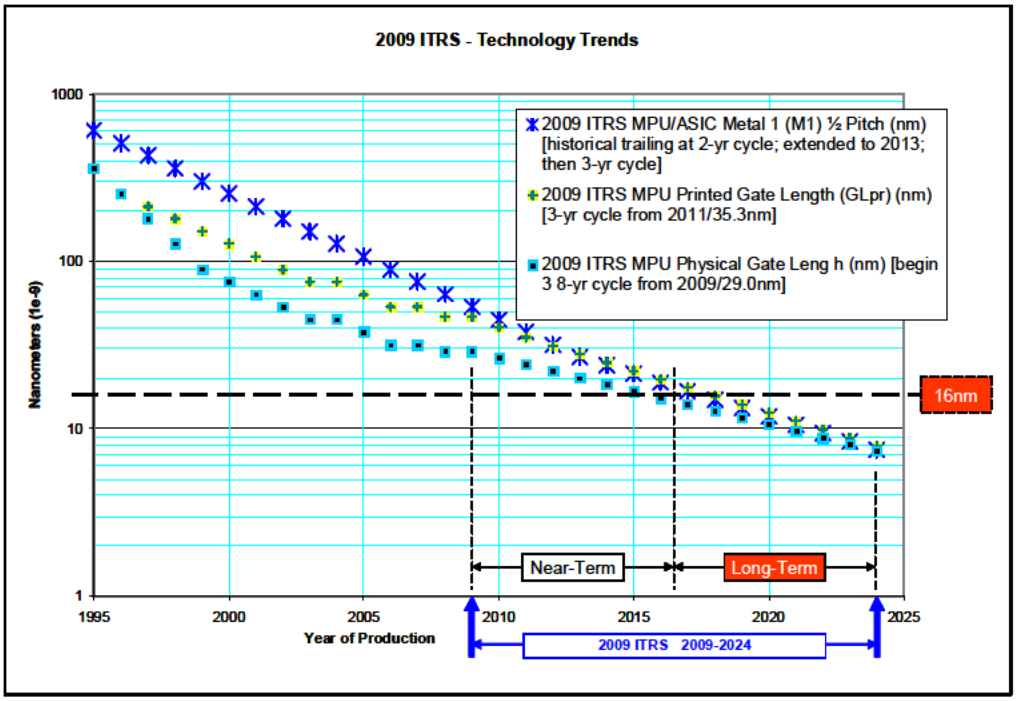


Figure 5b MPU/high-performance ASIC Half Pitch and Gate Length Trends

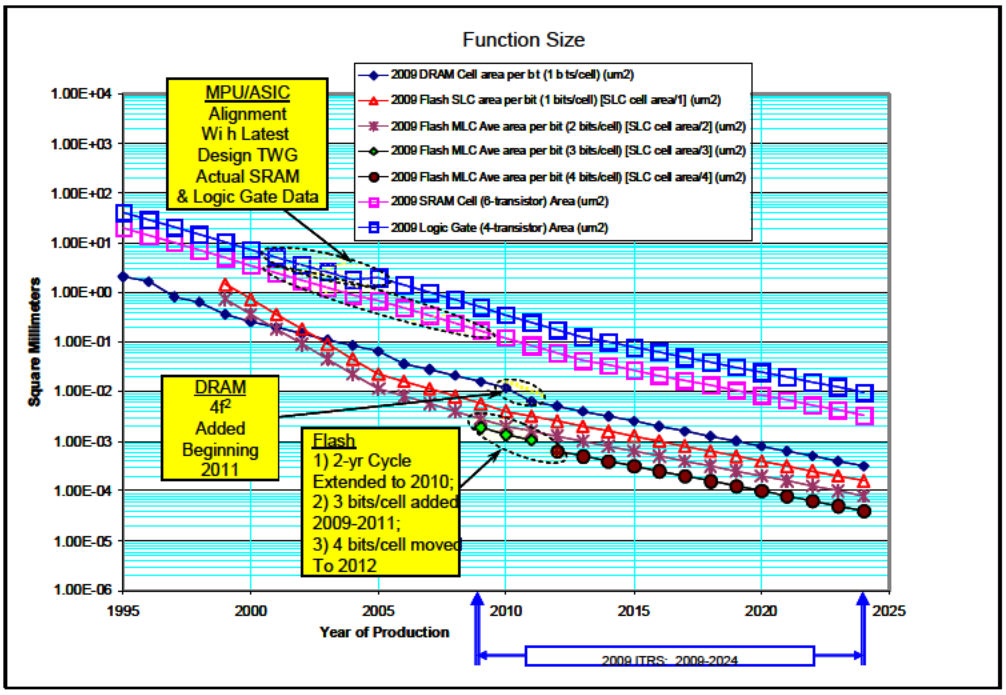


Figure 6 2009 ITRS Product Function Size Trends:
MPU Logic Gate Size (4-transistor); Memory Cell Size [SRAM (6-transistor); Flash (SLC and MLC), and DRAM (transistor + capacitor)]

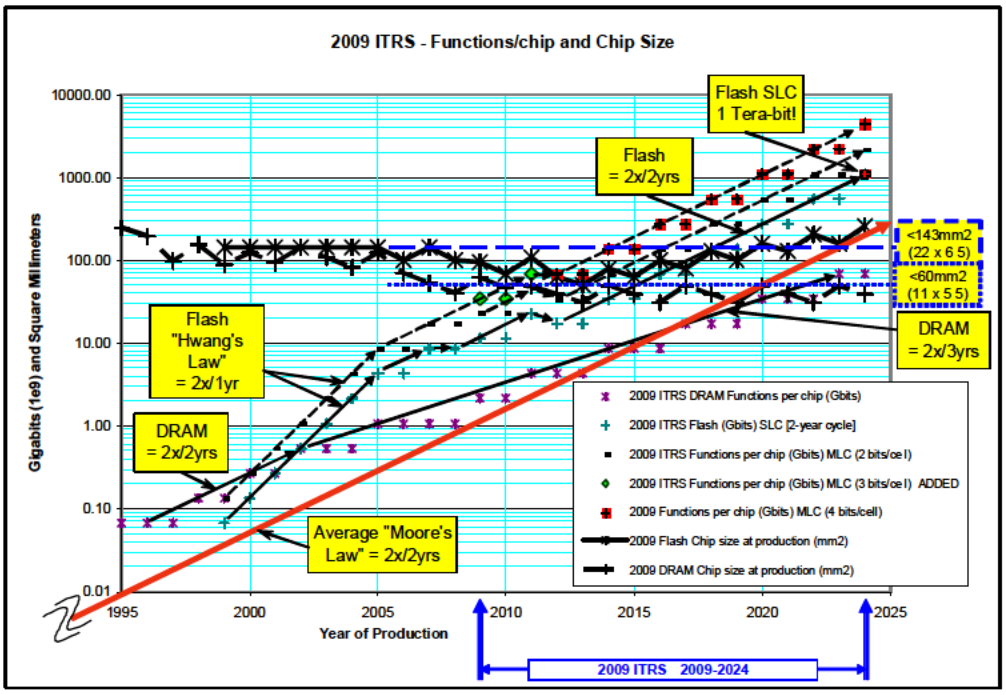


Figure 7a 2009 ITRS Product Technology Trends:
Memory Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

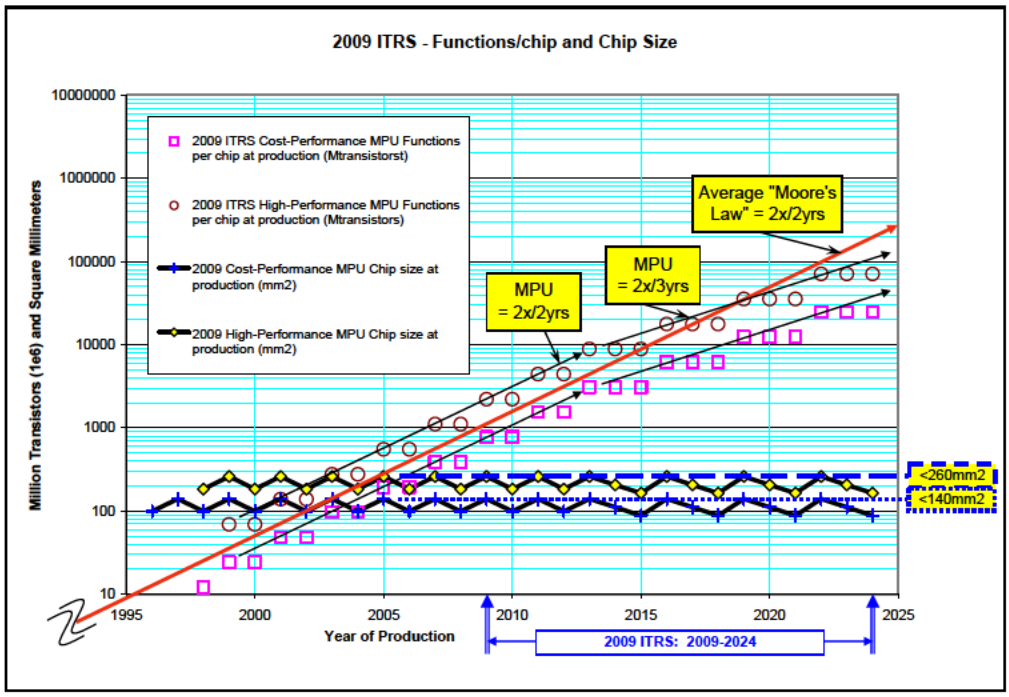


Figure 7b 2009 ITRS Product Technology Trends:
MPU Product Functions/Chip and Industry Average "Moore's Law" and Chip Size Trends

The remaining changes to Tables ORTC-3 through ORTC-7 for the 2010 Update are derived from corresponding changes to ITWG tables, which are used as the various source line items for consolidation in the ORTC. A review of these ITWG-related ORTC tables is included below.

TABLE 3—"LITHOGRAPHIC-FIELD AND WAFER-SIZE TRENDS"

Lithography field size trends are unchanged from the 2009 ITRS document. The 2010 update wafer generation timing targets for the 450 mm generation also remain unchanged from the 2009 ITRS. The 450 mm targets were revised in the 2009 ITRS to begin production in the 2014–2016 timeframe on a delayed 12–14-year cycle).The International Roadmap Committee (IRC) had originally commented in 2008 that the 450 mm volume production ramp by product group "could range at different rates from 2012–2016," but that range was narrowed to 2014–16 in the 2009 and 2010 editions, and will undergo re-evaluation for possible updating during the 2011 ITRS work.

Significant progress by consortia is ongoing, as is dialogue between semiconductor manufacturers and suppliers to assess standards and productivity improvement options on 300mm and 450 mm generations. Economic analysis of option scenarios also continues to examine the required R&D cost, benefits, return-on-investment, along with funding mechanism analysis and proposals from companies, and different regional consortia and governments. See Figure 8 for the timing targets for 450 mm, which were added to the 2009 ITRS Executive Summary, and continue unchanged in the 2010 edition.

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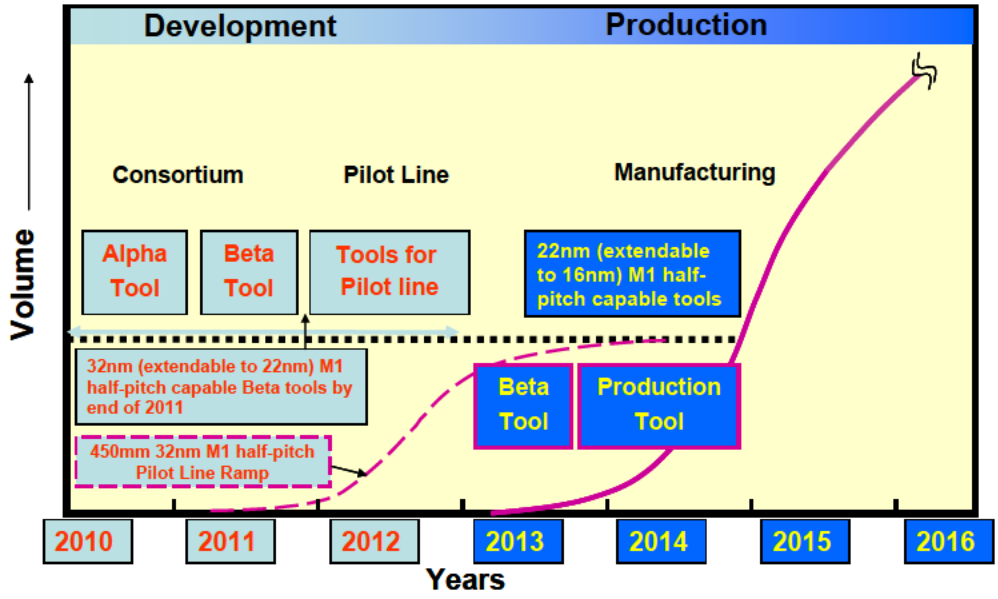


Figure 8 *A Typical Wafer Generation Pilot Line and Production "Ramp" Curve applied to Forecast Timing Targets of the 450 mm Wafer Generation*

TABLE 4—"PERFORMANCE AND PACKAGE CHIPS TRENDS":

The 2010 update for internal chip pad counts for both I/O and power and ground remain unchanged (2:1 ratio I/O-to-power/ground for high-performance MPU; 1:1 ratio for high-performance ASIC). And numerical targets and trends for the maximum pin counts and packaging costs also remain unchanged from the 2009 ITRS,

The Assembly and Packaging ITWG has made adjustments to their targets for pad pitch. Cost-per-pin targets are unchanged by Assembly and Packaging (A&P) and reflect that ITWG's estimates and response to cost challenges.

In the 2007 ITRS edition, the chip-to-board (off-chip) frequency was removed from the ORTC to avoid confusion with the Design/Process Integration (PIDS) targets for on-chip frequency (see the A&P ITWG tables for off-chip frequency). The Design and PIDS ITWG recommended targets for maximum on-chip frequency remain unchanged from the 2009 ITRS target of 8% average annual growth trend. The 8% growth trend forecast, was derived from the 2007 Design ITWG surveys and Product Performance Models. The PIDS ITWG has maintained a 13% intrinsic transistor speed growth target, which provides significant designer "headroom" compared to the 8% Design ITWG chip frequency trend drivers.

The maximum chip frequency in actual product is running lower than the ITRS targets, and it is likely that the models from both PIDS and Design will be revised during the 2011 ITRS work. The Interconnect ITWG has left the number of on-chip wiring levels unchanged, as reflected in the 2009 and 2010 ORTC line item tracking that trend.

TABLE 5—"ELECTRICAL DEFECTS"

Due to the unchanged product models, the ORTC defect density targets remain unchanged from the 2009 ITRS edition. The number of mask levels, provided by the Lithography ITWG, also remains unchanged, but is under evaluation by the Lithography ITWG to determine the impact of recent trends of increasing mask levels; especially due to the growth trend of double-masking to extend optical lithography until the anticipated arrival of EUV solutions.

TABLE 6—"POWER SUPPLY AND POWER DISSIPATION"

The targets for V_{dd} for both high performance and low operating power voltage remain unchanged from the 2009 Roadmap. However, the A&P ITWG is re-evaluating the approach for modeling maximum power, which is based on per square centimeter targets alone. The A&P ITWG approach takes into account "hot spots" on the chip and the need for cross-TWG potential solutions from both the Interconnect ITWG and the packaging roadmap which would mitigate those power dissipation challenges. In the meantime the ORTC maximum Watts targets in the 2010 tables continue to be calculated for specific product maximum production start chip sizes, which are unchanged from the targets in the 2009 ORTC chip size models (See Tables ORTC-2A through 2D and Figures 7a and 7b).

TABLE 7—"COST"

The "tops-down" semiconductor market driver models for cost-per-function remain unchanged from the 2009 ITRS. The cost table targets for both memory and logic represent the need to preserve the historical economic semiconductor device productivity trend for continuous reduction of the cost-per-function by -29% compound annual reduction rate (CARR) throughout the roadmap timeframe.

Preserving this cost-per-function productivity trend in view of increasing packaging costs, plus the slowing of product function densities due to slower technology cycles (three-year versus two-year) and design factor improvements, represent the over-arching economic grand challenge for the industry; and the major driver of the Factory Integration ITWG productivity improvement grand challenges and potential solutions

Link to 2009 Executive Summary

Link to 2010 Update ORTC tables' file

2010 UPDATE: WORKING GROUP SUMMARIES

SYSTEM DRIVERS AND DESIGN

Link to the 2010 Update file for System Drivers.

Link to the 2010 Update file for Design.

Link to the 2009 System Drivers Chapter.

Link to 2009 Design chapter.

In the 2010 Update of the ITRS Design and System Drivers chapters, focus is on a few selected key messages and updates described below.

Key messages continue to be delivered by these chapters. First, design productivity continues to be center focus of our design technology roadmap, as scaling depends fundamentally on time to market for electronic products. Accurate design productivity and cost models are crucial. Second, power consumption has become the key technical parameter that controls feasible semiconductor scaling. As a result, the device roadmap has become power-driven, and frequency is being pushed to a flat trend. Third, More than Moore has become a necessary component of semiconductor product scaling. Mixed SiP-SoC analog-digital drivers also need to be roadmapped.

Although this year's design technology roadmap does not feature any major changes, the following workflows are worth mentioning. First, the Design chapter's productivity and cost models are being improved. Second, a "Power Chart" that mimics our well-known productivity chart is being developed, given the critical importance of power to design. Third, 3D/TSV content continues to be made consistent with other chapters, even if there is not a separate section for it within the Design and System Drivers ITWG chapters, due to the breadth of impact of these technologies. Finally, several sections continue to be improved, including the Design for Manufacturing (DFM)—e.g., adding quantifiable Design for Reliability (DFR) requirements)—, Verification, and Logic-Circuit-Physical sections. Finally, for 2010, a refresh of the well-known design cost figure has been provided, with the recognition that the beyond-CMOS part of the curve will require more work as device structures and their design impact are all but unknown in the most distant years.

For the System Drivers chapter, the MPU frequency roadmap is being updated to reflect a flatter trend that has been confirming itself over the last few years—a change whose impact will be reflected beyond these two chapters. Other drivers are being improved not dissimilarly from prior years, including the SoC-CP and SoC-CS models, the RF and Analog/Mixed-signal fabric drivers (in coordination with the Wireless chapter), and an extended/new More-Than-Moore RF andAnalog/Mixed-signal SoC (based on the SoC-Portable driver). All of them will be more accurate integration realities as the roadmap moves to its next 15 years. In the very short term, for 2010, it has been ensured that minimal consistency exists with other chapters such as PIDS by flowing known changes through the key consumer system driver models. This is reflected in Figures DESN5-7 and DESN9-11.

Cooperation with other groups is also being reflected in these two chapters. Additionally, input from the 2nd ITRS-driven EDA Roadmap Workshop at the IEEE/ACM DAC Conference is being incorporated.

Table ITWG1 Major Product Market Segments and Impact on System Drivers

Market Drivers	*SOC*	*Analog/MS*	*MPU*
I. Portable/consumer			
1. Size/weight ratio: peak in 2004 2. Battery life 3. Function: 2×/2 years 4. Time-to-market: ASAP	Low power paramount Need SOC integration (DSP, MPU, I/O cores, etc.)	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
II. Medical			
1. Cost: slight downward pressure (~1/2 every 5 years) 2. Time-to-market: >12 months 3. Function: new on-chip functions 4. Form factor often not important 5. Durability/safety 6. Conservation/ ecology	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SOC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
III. Networking and communications			
1. Bandwidth: 4×/3–4 years 2. Reliability 3. Time-to-market: ASAP 4. Power: W/m^3 of system	Large gate counts High reliability More reprogrammability to accommodate custom functions	Migrating on-chip for MUX/DEMUX circuitry MEMS for optical switching.	MPU cores, FPGA cores and some specialized functions
IV. Defense			
1. Cost: not prime concern 2. Time-to-market: >12 months 3. Function: mostly on SW to ride technology curve 4. Form factor may be important 5. High durability/safety	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important Recent advances in multicore processors have made programmability and real-time performance possible
V. Office			
1. Speed: 2×/2 years 2. Memory density: 2×/2 years 3. Power: flat to decreasing, driven by cost and W/m^3 4. Form factor: shrinking size 5. Reliability	Large gate counts; high speed Drives demand for digital functionality Primarily SOC integration of custom off-the-shelf MPU and I/O cores	Minimal on-chip analog; simple A/D and D/A Video i/f for automated camera monitoring, video conferencing Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-position resolution	MPU cores and some specialized functions Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
VI. Automotive			
1. Functionality 2. Ruggedness (external environment, noise) 3. Reliability and safety 4. Cost	Mainly entertainment systems Mainly ASSP, but increasing SOC for high end using standard HW platforms with RTOS kernel, embedded software	Cost-driven on-chip A/D and D/A for sensor and actuators Signal processing shifting to DSP for voice, visual Physical measurement ("communicating sensors" for proximity, motion, positioning); MEMS for sensors	

A/D—analog to digital ASSP—application-specific standard product D/A—digital to analog DEMUX—demultiplexer DSP—digital signal processing FPGA—field programmable gate array i/f—interface I/O—input/output HW—hardware MEMS—microelectromechanical systems MUX—multiplexer RTOS—real-time operating system

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Table ITWG2 Overall Design Technology Challenges

Challenges ≥ 22nm	*Summary of Issues*
Design productivity	System-level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation Verification: executable specification, ESL formal verification, intelligent test bench, coverage-based verification Logic/circuit/physical: analog circuit synthesis, multi-objective optimization Logic/circuit/physical: SiP and 3D (TSV-based) planning and implementation flows Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	Logic/circuit/physical: dynamic and static, system- and circuit-level power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Reliability	Logic/circuit/physical: MTTF-aware design, BISR, soft-error correction
Interference	Logic/circuit/physical: signal integrity analysis, EMI analysis, thermal analysis
Challenges <22nm	*Summary of Issues*
Design productivity	Verification: complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage Tools specific for SOI and non-static logic, and emerging devices Cost-driven design flow
Power consumption	Logic/circuit/physical: SOI power management Logic/circuit/physical : Reliability- and temperature-constrained 3D physical implementation flows
Manufacturability	Uncontrollable threshold voltage variability Advanced analog/mixed signal DFT (digital, structural, radio), "statistical" and yield-improvement DFT Thermal BIST, system-level BIST
Reliability	Autonomic computing, robust design, SW reliability
Interference	Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.)

ATE—automatic test equipment BISR—built-in self repair BIST—built-in self test DFT—design for test EMI—electromagnetic interference ESL—Electronic System-Level HW/SW—hardware/software MTTF—mean time to failure SOI—silicon on insulator

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TEST AND TEST EQUIPMENT

Link to the 2010 Test and Test Equipment update file.

Link to 2009 Test and Test Equipment chapter.

The 2010 test and test equipment roadmap contains minor updates to table trends, but contains some significant changes to the overall test drivers that reflect the implications of More than Moore trends and the proliferation of multi-core and fault tolerant devices. CPU clock rates have not significantly changed in the last few years and are forecasted to be on a much slower growth curve than forecasted five years ago, but communication and other devices in the >20 Gigahertz range are on the fast change track to higher frequencies and present challenges to traditional test methods.

TEST DRIVERS

The trend toward system in a package solutions to obtain higher performance, lower cost, and reduced power consumption remains, but is being enhanced with a focus on the test challenges for 3D multi-die and multi-layer implementations which either use multiple die connected with TSVs or a single base silicon where a second, third or N layers are added to the previously completed circuit layer by forming a new silicon (or other material) base layer and forming new circuits in the added layer. The use of TSV (through silicon via) or TLV (through layer via) solutions will add complexities to the test and design for test processes to ensure the overall quality and reliability of the connections, while at the same time not increasing the test cost by a non-similar scaling factor over the cost of testing individual pieces of silicon. Cost containment will require concurrent or phase shift concurrent testing of similar logical block or cores.

Circuits are becoming more fault tolerant through the use of error detection, which then reacts to the error by disabling and replacing the faulty block, correcting the information, or throttling the system in some manner to achieve reliable and continuing operation. These non-deterministic but algorithmic methods to keep functionality further add to the complexity of determining whether a device is shippable. Improving yield and reducing cost via adaptive test adds the requirement of reliable unit and die-level tracking to take full advantage of the benefits of intelligent test.

High gigahertz frequency radio devices will require innovative solutions that do not depend on the traditional insertion of a device into a socket. These may bring wireless testing of units into mainstream high-volume product along with the added complexity of signal and interference management.

LOOKING TO 2011

The next year will examine the impacts of the key drivers changes made in this 2010 revision. Memory testing has become more type specific and this will be reflected in future tables by replacing the combined memory trends with specific sections for DRAM and NAND. Further focus will be on DFT and testing of 3D structures. Greater than 100GHz testing, concurrent testing, test data volume reduction, and test cost control will also be included in development of the 2011 roadmap.

Table ITWG3 Summary of Key Test Drivers, Challenges, and Opportunities—Updated

Key Drivers (not in any particular order)	
Device trends	Increasing device interface bandwidth and data rates Increasing device integration (SoC, SiP, MCP, 3D packaging) Integration of emerging and non-digital CMOS technologies Device characteristics beyond the deterministic stimulus/response model Fault Tolerant architectures and protocols 3 Dimensional silicon - multi-die and Multi-layer Multiple Power modes and Multiple time domains
Test process complexity	Adaptive test and Feedback data Concurrent test within a DUT Maintaining unit level test traceability Device customization / configuration during the test process
Economic scaling of test	Physical limits of packaged test parallelism Test data volume Managing interface hardware and (test) socket costs Multiple Insertions and System test
Difficult Challenges (in order of priority)	
Test for yield learning	Critically essential for fab process and device learning below optical device dimensions
Detecting Systemic Defects	Testing for local non-uniformities, not just hard defects Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects
Screening for reliability	Effectiveness and Implementation of burn-in, IDDQ, and Vstress testing Detection of erratic, non deterministic, and intermittent device behavior
Future Opportunities (not in any order)	
Test program automation (not ATPG)	Automation of generation of entire test programs for ATE
Majority of effort on mixed-signal and RF tests	Digital tests are just "data" Mixed signal and RF tests tend to be hand coded.
Simulation and modeling	Seamless Integration of simulation and modeling of test interface hardware and instrumentation into the device design process
Convergence of test and system reliability solutions	Re-use and fungibility of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMs—micro-electromechanical systems

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PROCESS INTEGRATION, DEVICES, AND STRUCTURES

Link to the 2010 Process Integration, Devices, and Structures update file.

Link to 2009 PIDS chapter.

SUMMARY

The changes made in this update fall into two categories: reduction of power supply voltages V_{dd} for low-power logic technologies, both LSTP and LOP, and incorporation of the latest observations and projections on the fast-moving memory technologies, both DRAM and NVM.

For low-power technologies, the supply voltages are lowered to reduce the dynamic power component. The trade-off is lower speed (I/CV) which is sufficient to meet their performance requirements. The specific changes for each low-power device type are detailed below:

Table PIDS3A: Low Standby Power Technology Requirements

- Off-current I_{off} is reduced from 50 pA/μm to 10 pA/μm to decrease the static power.
- Power supply voltages V_{dd} are lowered to similar values as those of high performance technology to reduce the dynamic power.
- From these changes, the speed I/CV values are reduced by the amounts ranging 20–57% from those of 2009. These speeds are considered to be adequate for their functions.

Table PIDS3B: Low Operating Power Technology Requirements

- Power supply voltages V_{dd} are lowered to reduce the dynamic power.
- From this change, the speed I/CV values are reduced by amounts ranging 14–34% from those of 2009. These speeds are considered adequate.

For memories, the Japan PIDS sub-group had recently finished another survey on future scaling. Together with the latest public product announcements, PIDS has decided to incorporate the latest projections in this update. However, time does not allow the ITRS ORTC tables to propagate such changes across the board to all working groups' tables during the 2010 Update. It has been agreed that PIDS should still go ahead with the latest projections in this 2010 update, and the new projections will be adopted, to be adjusted if necessary per later information, by the rest of ITRS in the 2011 ITRS technology pacing work. Specific changes for each memory device type in the 2010 PIDS tables are listed below:

Table PIDS4: DRAM Technology Requirements

- Half-pitch scaling is accelerated by one year for the next five years.
- Structure transition from RCAT to FinFET is delayed by two years to 2012.
- Vertical channel transistor (VCT) will be launched in 2013 and continue till end of roadmap.
- Cell size factor of $4F^2$ will be delayed by two years.
- Support PMOS gate electrode transition to TiN metal gate is delayed by two years.

Table PIDS5: Non-Volatile Memory Technology Requirements

- Half-pitch scaling is accelerated by one year.
- Product total bit size (in Gb) is accelerated by one year.
- Introduction of 3-D stacking is delayed by one year to 2015.
- 4 bit/cell is delayed by seven years to 2019.

All other tables remain unchanged from the 2009 ITRS chapter:

Table PIDS1: Process Integration Difficult Challenges.
Table PIDS2: High-performance Logic Technology Requirements.
Table PIDS5A: Requirements for Spin-Torque Transfer (STT) MRAM.
Table PIDS6 Reliability Technology Requirements.

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Table ITWG4 Process Integration Difficult Challenges

Difficult Challenges for $L_g \geq 16$ nm	*Summary of Issues*
1. Scaling of logic MOSFETs	Scaling planar bulk CMOS Implementation of fully depleted SOI and multi-gate (MG) structures Controlling source/drain series resistance within tolerable limits Further scaling of EOT with higher κ materials (κ > 30) Threshold voltage tuning and control with metal gate and high-κ stack Inducing adequate strain
2. Scaling of DRAM and SRAM	DRAM— Adequate storage capacitance with reduced feature size; implementing high-κ dielectric Low leakage in access transistor and storage capacitor Low resistance for bit and word lines to ensure desired speed Improve bit density and to lower production cost in driving toward $4F^2$ cell size SRAM— Maintain adequate noise margin and control key instabilities and soft-error rate Difficult lithography and etch issues
3. Scaling high-density non-volatile memory	Endurance, noise margin, and reliability requirements Non-scalability of tunnel dielectric and interpoly dielectric in flash Difficult lithography and etch issues with pitch scaling Maintain high gate coupling ratio in floating-gate flash
4. Reliability due to material, process, and structural changes	Threshold voltage shifts due to traps, carrier injection, and program/erase cycling in memory cells Mobility degradation due to mechanical stress relaxation or interface states New or changed failure mechanisms resulting from high-κ/metal gate and new doping/activation processes New failure mechanism resulting from fundamental length scales or new device structures Process variability
Difficult Challenges for $L_g < 16$ nm	*Summary of Issues*
1. Implementation of advanced non-classical CMOS structures	Advanced non-planar multi-gate MOSFETs below 10 nm gate length Control of short-channel effects Drain engineering to control parasitic resistance Strain enhanced thermal velocity and quasi-ballistic transport
2. Implementation of non-classical CMOS channel materials	Identification and demonstration of alternate channel materials New issues from materials, devices, and processing Integration of alternate channel materials on Si platform
3. Identification and implementation of new memory structures	Density and voltage scaling of NVM 3-D integration of NVM Implementing non-charge-storage type of NVM Scaling storage capacitor for DRAM DRAM and SRAM replacement solutions
4. Reliability of novel devices, structures, materials, and applications	Reliability characterization of new devices Dealing with fluctuations and statistical process variations Impact of microscopic physical effects Need for Design for Reliability tools
5. Power scaling	V_{dd} scaling Controlling subthreshold current
6. Beyond CMOS	Identification and implementation of non-CMOS devices and architectures Integration onto Si-CMOS platform See ***ERD*** and ***ERM chapters*** for more discussions and details

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RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

Link to the 2010 Wireless update file.

Link to 2009 Wireless chapter.

Radio frequency (RF) and analog/mixed-signal (A/MS) technologies serve the rapidly growing wireless communications market and represent essential and critical technologies for the success of many semiconductor manufacturers. Communications products are becoming key drivers of volume manufacturing. Consumer products now account for over half of the demand for semiconductors.[1] For example, third generation (3G) cellular phones now have a much higher semiconductor content and now are 50 % of the cellular phone market compared to only 5 % of the market a few years ago. The consumer portions of wireless communications markets are very sensitive to cost. With different technologies capable of meeting technical requirements, time to market and overall system cost will govern technology selection.

The scope of the RF and A/MS ITWG remains the same as in the 2009 ITRS. The requirements for wireless transceiver ICs are technology drivers that contribute substantially to the recent ITRS-defined More than Moore thrust. This 2010 ITRS RF and A/MS chapter update is divided into applications for less than 10 GHz and mm-wave applications. The RF and A/MS ITWG has five technology subgroups. Four of the subgroups cover applications below 10 GHz: CMOS, bipolar, passives, power amplifiers (PAs) and MEMS. The fifth subgroup on mm-wave applications focuses on power and low-noise requirements of both III-V compound semiconductor and silicon-based devices used in transceiver ICs.

Some portions of the RF and A/MS technology roadmap pertain more to prototype capabilities rather than usual CMOS volume production of most of the other ITRS chapters. Production implies applications and markets. But emerging mm-wave connectivity and imaging applications that are part of the RF and A/MS ITWG currently lag technology capabilities. Also, collaborations with the International Electronics Manufacturing Initiative (iNEMI) are ongoing to generate a matrix of applications versus technologies that cover emerging applications such as ultra low-power, medical, security, and the like.

For CMOS, the 2010 technology requirements tables continue the link of Performance-RF to low standby power (LSTP) CMOS with a one-year lag and mm-wave CMOS to high performance (HP) CMOS with a two-year lag as reflected in the 2009 table. Three adjustments were made for 2010; matching is dramatically lowered to reflect published data for high-κ/metal-gate technologies; f_{MAX} was lowered to better reflect recent publications, and the fact the analog-friendly FETs are now commonly available is reflected in the Precision Analog table.

For bipolar, only the figures of the HS PNP transistor, newly introduced in 2009, have been updated. BV_{CEO} reduction is delayed at the expense of a slower increase in f_T over time in order to better fit to the key applications that are more BV_{CEO} driven than f_T driven today. f_T and f_{MAX} colors have been updated for the HS PNP and PA NPN bipolar transistors in agreement with published data. The key driving forces for the bipolar roadmap continue to include speed, power consumption, noise, and breakdown voltages.

For passive devices, the density and leakage for the on-chip MOS capacitor lag one year behind those for CMOS active devices as shown in the 2010 tables. Inductors with Q factor values of 35 are expected to be manufactured at high volumes in 2012 according to a 2010 publication. However, the technology of 3D IC interposer is expected to enable, higher Q factors in the near future. RF capacitors with densities near 1.5 $fF/\mu m^2$ are now available from some vendors of III-V compound semiconductor PAs. In the table on off-chip inorganic substrate capacitors, the leakage current density tends to be in the range of nA which is reflected in the reliability data of some publications. In the table on potential solutions for 0.4 GHz to 10GHz applications, materials for thinner layers with higher dielectric constants used in decoupling capacitors would require one more year of R&D activities. And, the high-μ materials that are needed in inductors with greater Q factors for use in analog or power devices and circuits would require two more years of R&D activities.

For power amplifiers, Handset Devices—The battery requirements are expected to remain at current levels for at least few more years. The MEMS adoption seems to be happening more slowly than expected, but remains an active area of development. It is also likely to be going directly toward an integrated solution. Base-Station Devices—The tables show that 48V LDMOS is likely to be introduced into the cellular infrastructure market in 2011. This introduction is primarily due to increased demand for higher power parts for Doherty PAs, and, due to the possibility that for the longer term, it

[1] *P. H. Singer, "Dramatic Gains in Performance on the Horizon," editorial in* Semiconductor International*, Vol. 29, No. 8, 29, July 2006, page 15.*

may serve as an envelope tracking or drain modulation solution to achieve higher efficiencies than can be achieved with Doherty PAs alone. In addition, the increased focus on efficiency is reflected in both the P1dB drain efficiency and peak drain efficiency. The goals for high efficiency architecture and drain efficiency have increased for both LDMOS and GaN.

For MEMS, we have no changes to the 2009 ITRS tables. Because MEMs is a very broad and diverse area, we are having ongoing discussions with other ITRS working groups and with iNEMI working group about the optimum way in which to do technology roadmaps for MEMs.

For millimeter wave applications, we have assumed "production" implies that at least one company offers products with "data sheets" or that the technology is available for custom designs from one or more companies as a foundry service. The main changes in the technology requirements table from 2009 are manifested as a delay in the trend to smaller critical dimensions in HBT and HEMT technologies. Because InP HBTs are not moving as fast as predicted to smaller dimensions, increases in f_t and f_{MAX} are slowing-down. For GaN HEMTs, technology challenges of maintaining breakdown voltage are delaying shrinking gate lengths. Nevertheless, we still predict that GaAs and InP will begin to be replaced by GaN as early as 2012 and 2014, respectively, for new applications. Power MHEMT is also likely to eventually be replaced by GaN HEMTs. As predicted in 2009, LN MHEMT at 70 nm is now available. However, continued progress in shrinking dimensions and higher frequency performance will be driven by market applications. Volume markets will be very cost sensitive, and SiGe and RF CMOS will be utilized in applications where their performance is adequate, resulting in possible further delay in transitioning III-V R&D advances into production.

DIFFICULT CHALLENGES

Table ITWG5 RF and Analog Mixed-Signal (RF and AMS) Technologies for Wireless Communications Difficult Challenges

Difficult Challenges	*Summary of Issues*
CMOS	New materials (e.g., high-permittivity gate dielectrics, embedded structures to induce channel strain, and metal-gate electrodes) make predicting trends uncertain for transistor mismatch and for 1/f noise.
Bipolar HS-NPNs and HS-PNPs transistors	Increasing f_T by more aggressive vertical profiles and still maintaining acceptable figures of merit, manufacturing control, and punch-through margins
Bipolar Power Amplifiers	Improving the trade-off between f_T/f_{MAX} and breakdown voltages to provide acceptable voltage handling and power densities at performance levels that can effectively complete with alternative technologies.
On-Chip Passive Devices	Integrating new materials in a cost-effective manner to realize compact and high quality factor (Q) inductors and high-density metal-insulator-metal (MIM) capacitors demanded by the roadmap for increased RF performance.
Off-Chip Passive Devices	The large number of options for embedded passives increases complexity and cost. And accurate models for process tolerance and parasitic effects and computer assisted design (CAD) tools.
Handset Power Amplifiers	Increasing functionality in terms of operating frequency and modulation schemes and simultaneously meeting increasingly stringent linearity requirements at the same or lower cost.
Base-station Power Amplifiers	Enhancing performance with continual product-price pressure. And Improving amplifier efficiency.
mm-Wave Devices	Thermal management for high power density circuits, multi-level integration and E/D mode transistors. And reduction of leakage current and understanding of failure mechanisms, particularly for GaN materials which are piezoelectric in nature.
MEMS	Incorporating the great process diversity of MEMS into specific ITRS processes. And developing design tools, packaging, performance drivers, and cost drivers for each MEMS device type.

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EMERGING RESEARCH DEVICES

Link to the 2010 ERD and ERM Memory Workshop file.

Link to 2009 ERD chapter.

The ITRS Emerging Research Devices (ERD) International Technical Working Group (ITWG), in collaboration with the Emerging Research Materials (ERM) ITWG and co-sponsored by the National Science Foundation, evaluated and updated their information on several new technologies proposed for beyond CMOS information processing, memory, and storage technologies. In particular, the ERD and ERM ITWGs thoroughly assessed eight of the most promising emerging memory technologies to determine whether one or more has high potential and is sufficiently mature to justify its accelerated research and technology development toward commercialization. To be considered, a memory technology was required to have demonstrated good performance with at least a partially understood storage mechanism and be scalable multiple generations beyond the 16 nm technology generation. Further, it should be ready for manufacturing within the next five to ten years.

This study was initiated for two reasons. First, current memory technologies, such as DRAM, SRAM, and NAND Flash, are approaching very difficult issues related their continued scaling to and beyond the 16 nm generation. Second, research over the past ten to fifteen years has led to discovery of several promising new non-volatile memory technologies, many in the category of resistive RAMs. These emerging research memory technologies include the ferroelectric-gate FET, nanoelectromechanical RAM, spin transfer torque (STT) MRAM, nanoionic or redox memory (including the fuse/antifuse memory and related electrochemical metallization, programmable metal cell and the atomic switch), nanowire phase change memory, electronic effects memory (i.e., charge trapping, mott transition, ferroelectric barrier effects), macromolecular memory, and molecular memory. Research has provided some clarification and insight to the physical storage mechanisms and the limits of several of these approaches; this information was used to establish a basis for judging their long-term potential, The ERD and ERM ITWGs reviewed white papers and listened to arguments presented by advocates and challenged by "friendly critics" for each of the eight technologies. Following considerable discussion, these work groups recommended to the IRC that STT-MRAM and redox RAM receive additional attention in research and development to accelerate progress toward commercialization of one or both of these technologies. The IRC approved communication of these recommendations to the research community and to funding agencies**.** A subsequent workshop will be held to identify specific materials and process research needed to enable critical progress on these technologies.

An ERD Logic Device workshop, also co-sponsored by the National Science Foundation, was conducted in 2010 to evaluate progress and potential of emerging research spin-based and graphene-based logic devices. This workshop followed up an intensive evaluation of several candidate beyond CMOS logic technologies, in July 2008, which resulted in "carbon-based nanoelectronics" being identified as promising candidate information processing by the ERD and ERM ITWGs. Another objective of this workshop was to gather material on selected research areas in order to have current information the 2011 ERD chapter rewrite.

Table ITWG6 Emerging Research Devices Difficult Challenges

Difficult Challenges ≥ 16 nm and < 16 nm	*Summary of Issues and opportunities*
Scale high-speed, dense, embeddable, volatile and non-volatile memory technologies to and beyond the 16 nm technology generation.	SRAM and FLASH scaling will reach definite limits within the next several years (see PIDS Difficult Challenges). These are driving the need for new memory technologies to replace SRAM and FLASH memories. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile RAM The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in the technology development
Scale CMOS to and beyond the 16 nm technology generation.	Develop new materials to replace silicon as an alternate channel and source/drain to increase the saturation velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation for technology scaled to 16 nm and beyond. Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in t
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Discover and reduce to practice new device technologies and a primitive-level architecture to provide special purpose optimized functional cores heterogeneously integrable with silicon CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and develop a new information processing technology eventually to replace CMOS Ensure that a new information processing technology is compatible with the new memory technology discussed above; i.e., the logic technology must also provide the access function in a new memory technology. Bridge a knowledge gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing Reliability issues should be identified & addressed early in the technology development

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EMERGING RESEARCH MATERIALS

Link to the 2010 ERD and ERM Memory Workshop file.

Link to 2009 ERM chapter.

The 2010 Emerging Research Materials (ERM) chapter is unchanged from the 2009 chapter. In 2010, the ERM Technology Working Group held meetings and workshops to prepare for the rewrite of the ERM chapter in 2011 and worked with other ITWGs to define materials that should be added to the ERM chapter or transitioned to other ITWGs. Workshops and e-workshops were held for the topics of nanowires for devices, carbon nanotube device materials, memory materials, directed self assembly (DSA) for lithography, deterministic doping, "native" interconnects, and ultrathin barrier layers for extending copper interconnects. Meetings were also planned for early 2011 to review progress on carbon nanotubes and graphene for interconnects; directed self assembly for lithography extension, and assembly and package materials. The ERM also participated with ERD, PIDS, and FEP in development of a critical assessment of the maturity of III-V and Ge as alternate channel materials for their potential transition to FEP and PIDS in 2011. The ERM also participated in several meetings with the Assembly and Package and Interconnect ITWGs to identify potential ERM needed to support future 3D interconnect technologies.

The workshops and planning in 2010 were focused on determining the scope of the 2011 ERM chapter and identifying progress and research needed on promising materials. The nanowire workshop reviewed performance of silicon and III-V nanowires and assessed whether the performance of grown nanowires was better than patterned and etched structures. The carbon nanotube (CNT) workshop reviewed progress on the ability to grow CNTs in desired locations with controlled directions and bandgaps. The memory material workshop focused on materials and interfaces to reduce write energy in spin transfer torque (STT) devices and also materials physical mechanisms that enable operation of the Redox RAM. A workshop, organized by SEMATECH, at Kobe, Japan reviewed progress in DSA to determine whether there were any intermediate applications that could be used in integrated circuit manufacturing. The "native" interconnect review assessed the speed of signal propagation and power dissipation of several alternate state variables (i.e., spin, plasmons, etc.) to determine whether signals in beyond CMOS devices can be transmitted between devices without converting to electrical signals. The ultrathin barrier layer workshop reviewed progress of ruthenium based alloys and self assembled layers of organic molecules being scaled to sub 5 nm thicknesses to preventing diffusion of copper. For 3D interconnect technologies, it was determined that ERM should focus on materials to enable a thermal hierarchy for chip attach, stress management polymers that also spread heat and have required mechanical, electrical properties, and moisture resistance properties.

Additional workshops have been planned for early 2011 to get updates on ERM for devices, lithography, interconnects, and assembly and package. An update on graphene is being planned for alternate channel applications and this will be completed prior to the Alternate Channel Material Critical Assessment. A second workshop on DSA will be held on March 4, 2011 at the SPIE conference to assess the state of defect control and identify the potential for defects being reduced to levels compatible with integrated circuit processing. An e-workshop is being planned for February 2011 to review progress of carbon nanotubes and graphene for interconnect and via applications. Multiple e-workshops will be held to review progress in Assembly and Packaging materials including low-temperature chip-to-package or chip-to-chip interconnect materials, polymers to manage stress, thermal, and moisture, and high performance thermal interface materials.

The ERM is also working with other ITWGs to potentially transition more mature materials to their ITWGs. In 2010, the ERM, ERD, PIDS, and FEP held workshops and conducted a critical assessment survey to determine whether Ge and III-V materials were mature enough to transition into the PIDS and FEP roadmaps. ERM is working with the Lithography ITWG to potentially transition evolutionary resist materials into the Lithography roadmap. ERM is also working with the Interconnect ITWG to potentially transition evolutionary copper barrier layers into their chapter in 2011.

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Table ITWG7 Emerging Research Material Technologies Difficult Challenges

Difficult Challenges ≤16 nm	*Summary of Issues*
Integration of alternate channel materials with high performance	III-V has high electron mobility, but low hole mobility Germanium has high hole mobility, but electron mobility is not as high as III-V materials Demonstration of high mobility n and p channel alternate channel materials co-integrated with high κ dielectric Demonstration of high mobility n and p channel carbon (graphene or carbon nanotubes) FETs with high on-off ratio co-integrated with high κ dielectric and low resistance contacts Selective growth of alternate channel materials in desired locations with controlled properties and directions on silicon wafers (III-V, Graphene, Carbon nanotubes and semiconductor nanowires) Achieving low contact resistance to sub 16 nm scale structures (graphene and carbon nanotubes) Ge dopant thermal activation is much higher than III-V process temperatures Growth of high κ dielectrics with unpinned Fermi Level in the alternate channel material
Control of nanostructures and properties	Ability to pattern sub 16 nm structures in resist or other manufacturing related patterning materials (resist, imprint, self assembled materials, etc.) Control of CNT properties, bandgap distribution and metallic fraction Control of stoichiometry, disorder and vacancy composition in complex metal oxides Control and identification of nanoscale phase segregation in spin materials Control of surfaces and interfaces Control of growth and heterointerface strain Control of interface properties (e.g., electromigration) Ability to predict nanocomposite properties based on a "rule of mixtures" Data and models that enable quantitative structure-property correlations and a robust nanomaterials-by-design capability
Controlled assembly of nanostructures	Placement of nanostructures, such as CNTs, nanowires, or quantum dots, in precise locations for devices, interconnects, and other electronically useful components Control of line width of self-assembled patterning materials Control of registration and defects in self-assembled materials
Characterization of nanostructure-property correlations	Correlation of the interface structure, electronic and spin properties at interfaces with low-dimensional materials Characterization of low atomic weight structures and defects (e.g., carbon nanotubes, graphitic structures, etc.) Characterization of spin concentration in materials Characterization of vacancy concentration and its effect on the properties of complex oxides 3D molecular and nanomaterial structure property correlation
Characterization of properties of embedded interfaces and matrices	Characterization of the roles of vacancies and hydrogen at the interface of complex oxides and the relation to properties Characterization of transport of spin polarized electrons across interfaces Characterization of the structure and electrical interface states in complex oxides Characterization of the electrical contacts of embedded molecule(s)
Fundamental thermodynamic stability and fluctuations of materials and structures	Geometry, conformation, and interface roughness in molecular and self-assembled structures Device structure-related properties, such as ferromagnetic spin and defects Dopant location and device variability

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FRONT END PROCESSES

Link to the 2010 Front End Processes update file.

Link to 2009 FEP chapter.

SUMMARY

The 2010 FEP updates are minimal. Changes to the FEP tables in an update year are typically minor changes or a result of adjustments in the ORTC scaling numbers that impact the models that feed into the FEP tables. In 2010, one parameter so modified is the physical gate length—which impacts scaling for high performance (HP), low operating power (LOP), and low standby power (LSTP) logic devices, and DRAM ½-pitch scaling—these changes further impact defect and yield numbers in starting materials and surface preparation. This year the ORTC elected not to make any changes to the tables so the FEP tables were not significantly modified. The 2010 update changes focused on Table FEP13 for etch and Figure FEP16 for surface preparation.

The most significant updates for FEP occur in Table FEP13, "Etching Process Technology Requirements." The changes in FEP13 are driven by the many new etch challenges with advanced CMOS technologies. Through-pitch gate CD variations (gate linewidth roughness, across chip variation, and across wafer variation), are changing for gate CD targeting because of the critical effect of etch micro-loading. Micro-loading among various patterns, such as single gate transistor, multiple-finger transistor, array transistor, minimum-pitch transistor, and isolated transistor, becomes more critical as gate CD shrinks. OPC model optimization is critical to minimize gate CD variation among various patterns. Etch-induced loading effect should be included into the OPC model to further improve OPC model accuracy. Similarly, dense versus isolated pattern etch micro-loading effect is critical for SiGe recess etch because the SiGe to gate distance which is critical for transistor performance is strongly dependent on the SiGe etch micro-loading effect. Transistor gate CD control for 3D interconnect technology will also be challenging. Through silicon via (TSV), a key component for the TSV technology may have a transistor exclusion zone due to the high stress of TSV. CD control adjacent to the TSV excluded zone will be challenging due to the low local gate density. The line width roughness (LWR) budget remains constant at 2.28 nm between 2010 and 2011 because recent advanced lithography tools greatly improve across chip line width variation. However, LWR now becomes the largest portion of gate CD variation and resist improvement is urgently needed to further reduce this value. Further reductions in lot-to-lot and wafer-to-wafer gate CD variation will require the development of in-situ CD metrology in the etch tools, possibly with dynamic feed forward correction.

Updates were made to the Surface Preparation Potential Solutions table. As the industry moves toward materials requiring low temperature processing, controlling the interface prior to film deposition will become more critical. Controlled environments (FOUPS, clustered cleans) aqueous and subcritical solvent cleans, and advanced passivants and formulations are all potential method for accomplishing interface control. New materials and technologies will require new photoresist techniques and challenges for photoresist and residue removal. These include multilevel resists, fluorocarbon based residues, and, accomplished with low material loss, no structural damage, no impact to V_t, or work function while being potentially metal gate/high-κ compatible.

An issue of concern to the FEP working group has been the status of high-κ gate dielectric as a volume manufacturing solution. By the spirit of the ITRS guidelines of achieving sufficient volume to be considered in high volume manufacturing, it has done so. In 2011 we will change the coloration of this part of the Technology Requirement tables and of the Potential Solutions tables to indicate this. At the same time, we acknowledge that this solution has not achieved the expected number of implementations at time of writing this to fully fit the high volume definition, although a second manufacturer has just announced high volume implementation of high-κ metal gates for 32 nm technology.

In 2010 FEP worked closely with the Design and PIDS ITWGs to converge on a V_{cc} scaling roadmap for HP, LP, and LSTP. Along with V_{cc} scaling, FEP/PIDS/Design will work together in 2011 towards device metrics including I_{on}, I_{off}, CV/I, which will then guide the roadmap for module metrics (Gate stack, junctions, contacts, etc). The associated Thermal and Thin Films tables will be updated accordingly, with NMOS and CMOS requirements listed separately.

Looking toward 2011, FEP will work with other sub-groups to refine the timelines (and tables) associated with ERM and ERD ITWGs. The timing of MUGFET (ERD) and III-V /heterogeneous (ERM) integration will move two to three years ahead to address industry needs for advanced logic—necessitating changes to the tables to account for the corresponding infrastructure and FEOL module needs. The FEP high-mobility III-V (InGaAs and Ge) substrates identified for ERM will have a wide range of issues. Some of those identified include high throughput CVD epi processes, damage-free doping strategies, resist removal without III-V damage, low D_{it} high-κ dielectrics, defect and surface passivation, barriers and contact metal technologies.

Table ITWG8 Front End Processes Difficult Challenges

Difficult Challenges ≥ 16 nm (Metal 1 1/2-pitch)	*Summary of Issues*
	Strain Engineering - continued improvement for increasing device performance - application to FDSOI and Multi-gate technologies
	Achieving DRAM cell capacitance with dimensional scaling - finding robust dielectric with dielectric constant of ~60 - finding electrode material with high work function
	Achieving clean surfaces free of killer defects - with no pattern damage - with low material loss (<0.2 A)
	High-k/Metal Gate - introduction to full scale manufacturing for HP, LOP, and LSTP - scaling equivalent oxide thickness (EOT) below 0.8 nm
	450 mm wafers - meeting production level quality and quantity
Difficult Challenges < 16 nm (Metal 1 1/2-pitch)	*Summary of Issues*
	Continued scaling of HP multigate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, contact silicidation.
	Lowering required DRAM capacitance by 4F2 cell scheme or like, while continuing to address materials challenges
	Continued achievement of clean surfaces while eliminating material loss and surface damage and sub-critical dimension particle defects
	Continued EOT scaling below 0.7 nm with appropriate metal gates
	Continued charge retention with dimensional scaling and introduction of new non-charged based NVM technologies

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LITHOGRAPHY

Link to the 2010 Lithography update file.

Link to 2009 Lithography chapter.

It is becoming increasingly more difficult to extend optical lithography as we know it today. In 2010, Flash devices are being manufactured using 32 nm half-pitch double patterning (DP) as a way of extending the half-pitch while keeping the NA and wavelength constant. This approach will be pushed harder as DRAM and MPU drive down to the 32 nm half pitch and Flash starts to test the limits of optical solutions at the 22 nm half-pitch node in 2013. But it is at this point that an alternative next generation lithography (NGL) must be introduced into manufacturing to ensure a smooth transition into the lithography approaches beyond 22 nm.

At 22 nm, the international community that contributes to the ITRS saw possible divergence between Flash and DRAM/MPU products. Flash will continue using 193 nm immersion as the lithography technology of choice due to the high volume requirement in manufacturing. DRAM and MPU have four possible technologies that could be used and that could extend the roadmap out to 11 nm half-pitch. These were all ranked at each year for their desirability and feasibility as solutions. EUV lithography is the lead candidate because of its lower cost of ownership (COO). Second is extending 193 immersion double patterning down to a k1 of 0.15 for 22 nm half-pitch, followed by maskless lithography (ML2) and imprint lithography. Alpha and soon beta tools are being delivered to the semiconductor industry for evaluation and further development using all of these approaches. In many cases, the technology is not limited by the lithography tool, but rather by the supporting technologies.

DIFFICULT CHALLENGES < 16 NM VERSUS TECHNOLOGY

The difficult challenges moving into the NGL regime are many and are not just incremental improvements in the technologies that we know and understand. The technology options are still vast, and in many cases the technology and the supporting infrastructure technologies need significant inventions to approach the manufacturing stage. The Difficult Challenges table for ≤16 nm shows the major challenges that must be solved to bring NGL technologies to the manufacturing stage. These challenges are listed in the order of perceived difficulty. For EUV lithography at 16 nm, defect free masks, sources brightness, and optimal resist system are key components needing substantial improvements. All three components will be further challenged as requirements for <16 nm will be tightened. In addition, the NA for the exposure system will be required to be increased which will bring a different set of challenges. The incidence angles may be required to be increased which will require thinner absorber thicknesses and flare mitigation. It is not clear how much the increase in the source power may cause additional challenges to the substrate in term of thermal management. Any other lithography enhancement techniques such as double pattern may be considered for deep sub 16 nm nodes.

EUV printing defect can derive not only from the traditional opaque defect in the patterning layer but also from small phase defects on the EUV substrate or a phase defect generated in the multilayer of the reflective blank. These phase defects are beyond the limits of today's metrologies and as such are very difficult to observe and improve upon. Currently, the infrastructure inspection equipment (substrate, blank, patterned mask, AIMs) needed for EUV mask manufacturing at the 16 nm node does not exist.

Maskless lithography is another NGL technology that must overcome major challenges before being considered a manufacturing technology. Foremost is the system throughput combined with the resist sensitivity that will also provide adequate LWR and resolution. This is both a system issue with respect to the e-beam flux and a resist material issue. ML2 is listed as possible lithography option for <16 nm DRAM/MPU and Flash. There is significantly higher throughput to price challenge for Flash than logic due to its high volume requirement in manufacturing. The second most pressing concern for ML2 is the inability to inspect wafer images at the same capability that we now have for 4× mask patterns. Inspection involves two issues: the resolution of the wafer inspection (at sufficient speed) and die-to-database inspection to ensure no systematic recurring defects are present.

Imprint lithography has three major needs: 1× masks, imprint materials, and imprint systems. The 1× mask has many areas contributing to difficult obstacles. First is mask inspection. The mask must be inspected to find defects in the 1× pattern that are just 10% of the width of the feature. An e-beam system might be able to do this but not at the speeds needed for manufacturing. Second is the write time to expose the slower speed e-beam resists to meet the LWR and CD specifications for 1× patterning. Third, 1× defect sizes are 4× smaller than what current 4× optical mask processes require; therefore, imprint template and e-beam resist patterning processes need to be developed to match these specifications. Another challenge is that the imprint materials must be of sufficiently low viscosity to be applied quickly for sufficient throughput. The last major challenge is with the imprint system. The lithography community believes that

throughput; defect levels, and overlay all need a significant improvement for the technology to be accepted in manufacturing.

Although there are many near-term challenges, the industry is addressing them. Lithographic systems are being made to run at throughputs that are about 2× the throughput of older steppers, thus addressing some of the COO issues associated with double patterning. Registration and overlay issues with lithographic mask patterning systems are also being addressed to move double patterning into manufacturing. The industry is likewise addressing the fundamental challenges associated with the NGL technologies, in particular the EUV lithography and the mask infrastructure that is needed. With these gains, the lithography industry will be back on course for improving ROI into the future.

Table ITWG9A Lithography Difficult Challenges ≥ 16 nm—Updated

Difficult Challenges > 16 nm	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features Registration, CD, and defect control for masks Eliminating formation of progressive defects and haze during exposure Understanding and achieving the specific signature and specifications for a Double Patterned mask Establishing a stable process so that signatures can be corrected.
Double and multiple patterning	Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs Availability of high productivity scanner, track, and process to maintain low cost-of-ownership Photoresists with independent exposure of multiple passes Fab logistics and process control to enable low cycle time impact that efficient scheduling of multiple exposure passes.
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time ROI for small volume products Resources for developing multiple technologies at the same time Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume 450 mm diameter wafer infrastructure if at 16 nm
Process control	New and improved alignment and overlay control methods independent of technology option to <5.7 nm 3σ overlay error Controlling LER, CD changes induced by metrology, and defects < 10 nm in size Greater accuracy of resist simulation models Accuracy of OPC and OPC verification, especially in presence of polarization effects Lithography friendly design and design for manufacturing (DFM)
EUV lithography	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components Cost control and return on investment Resist with < 1.5 nm 3s LWR, < 10 mJ/cm2 sensitivity and < 20 nm ½ pitch resolution Fabrication of Zero Printing Defect Mask Blanks Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection) Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs) Controlling optics contamination to achieve > five-year lifetime Protection of EUV masks from defects without pellicles Fabrication of optics with < 0.10 nm RMS figure error and < 7% intrinsic flare

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Table ITWG9B Lithography Difficult Challenges <16 nm—Updated

Difficult Challenges <16 nm	*Summary of Issues*
EUV lithography—extendibility	Increased in NA
	Higher source power is needed to meet the throughput requirement
	Possible double patterning needed.
	Possibly new resist needed.
	Change of incident angle
	Different LTEM and absorber material to deal with high source power and heating
	Flare
Resist materials	Limits of chemically amplified resist sensitivity for <16 nm half pitch due to acid diffusion length
	Materials with improved dimensional and LWR control add (limits)
	Resist and antireflection coating materials composed of alternatives to PFAS compounds
	Low defects in resist materials (size <10 nm)
	Line width roughness <1.4 nm 3 sigma
Mask fabrication	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair)
	Increasingly long mask write and cycle time
	Mask process control methods and yield enhancement
	Cost control and return on investment
	Required degree of complexity with computational Lithography
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
	Development of cost-effective post-optical masks
	Cost effective 450 mm lithography systems
	Achieving ROI for small volume products
193 nm immersion multilple patterning	Cost control and return on investment
	Wafer processing to tighter overlay and CD controls
	Mask fabrication to tighter specifications
	Required degree of complexity with computational Lithography
	Increasing numbers of masks required.
Metrology and defect inspection	Defect inspection on patterned wafers for defects <20 nm
	Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3s
	Metrology for achieving <2.8 nm 3s wafer overlay error
	Template inspection for 1× Imprint Patterned Masks
	Phase shifting masks for EUV
CD control improvements and process control	Development of litho and post litho processes to control gate CD <1.5 nm 3s with <1.4 nm 3s line width roughness. Printed, post print process reduction, and final roughness
	Development of new and improved alignment and overlay control methods independent of technology option to achieve total <2.8 nm 3s overlay error on products.
Maskless lithography	Wafer throughput
	Cost control and return on investment
	Die-to-database inspection of wafer patterns written with maskless lithography
	Pattern placement—ncluding stiching
	Controlling variability between beams in multibeam systems
Imprint lithography	Defect-free Imprint templates at 1× dimensions
	Infrastructure for 1× technology templates (write, inspection, and repair)
	Template fabrication to tighter specifications
	Protection of imprint templates from defects without pellicles
	Throughput
	Cost control and return on investment
	Overlay
	Process control methods to compensate for systematic CD and overlay errors

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INTERCONNECT

Link to the 2010 Interconnect update file.

Link to 2009 Interconnect chapter.

The Interconnect chapter of the ITRS addresses the wiring system that distributes clock and other signals to the various functional blocks of the integrated circuit, along with providing necessary power and ground connections. For 2008, the scope has been expanded to include the contact level and continues up through the device from metal 1 through to the global wiring levels. Traditionally, global wiring delay has been the "Grand Challenge" and tackling delay generally, is still a primary focus.

The current approach of the 2010 Interconnect TWG for addressing delay is to enable high-bandwidth low-power signaling solutions and a new table, INTC6 "High Density Through Silicon Via Specification" has been added. The group continues to project the use of copper as the primary conductor in a dual-damascene architecture; however, much of the work in progress focuses on the latest challenges and trends related to 3D integration and emerging technology.

- The Technology Requirements Table (INTC2) has been substantially revised and reorganized and divided into
  - general requirements – e.g., bulk resistivity and dielectric constant
  - level specific requirements determined by the nature of the wire or via geometry – e.g., barrier thickness or effective resistivity
- Low-k roadmap – small slowdown
  - New range for bulk κ
  - Air gaps moved out of emerging sections – considered mainstream
  - Air gaps expected to be the solution for κ_{bulk} <2.0
- Atomic layer deposition (ALD) barrier processes and metal capping layers for Cu are lagging in introduction – needed to meet sub 1 nm specifications
  - Hybrid barriers containing ruthenium are proliferating
- J_{max} current limit model show a width dependence – a new reliability concern
- Technology drivers expanded to support both traditional geometric scaling and equivalent scaling
  - Requirements for CMOS-compatible equivalent scaling are highlighted in an expanded *Emerging Interconnect Properties* section along with a new first principle consideration of interconnect properties for new (non-FET) switches
- Design and processing of three-dimensional chip stacking through the use of high-density through silicon vias (TSVs) is a key focus area to address delay and power concerns and a new TSV table has been introduced

DIFFICULT CHALLENGES

Table ITWG10 Interconnect Difficult Challenges--Updated

Five Most Critical Challenges ≥ 16 nm	*Summary of Issues*
Material Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Manufacturable Integration Engineering manufacturable interconnect structures, processes and new materials	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool
Reliability Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Metrology Three-dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Cost & Yield for Manufacturability Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.
Five Most Critical Challenges < 16 nm	*Summary of Issues*
Material Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Metrology Three-dimensional control of interconnect features (with it's associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Process Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.
Complexity in Integration Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
Practical Approach for 3D Identify solutions which address 3D structures and other packaging issues	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

CMP—chemical mechanical planarization DRAM—dynamic random access memory

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FACTORY INTEGRATION

Link to 2010 Factory Integration update file.

Link to 2009 Factory Integration chapter.

The Factory Integration (FI) ITWG identifies needed operational factory services and relevant technologies, and it updates the near term and longer term technology requirements and potential solutions to meet these requirements. The Factory Integration ITWG has five thrust teams and their technology focuses are shown in the following table.

Functional Area	*Key technology focuses and issues*
Factory Operations (FO)	1) Systematic productivity improvement methodology prior to 450 mm insertion 2) Systematic factory waste visualization of cycle times and factory output losses
Production Equipment (PE)	1) 450 mm production tool development 2) Reliable and predictable equipment availability improvement 3) Energy conservation/management in process tools
Material Handling Systems (MHS)	1) Reduction in average material delivery times 2) More interactive control with FICS and PE for accurate scheduled delivery
Factory Information and Control Systems (FICS)	1) Increased FICS reliability performance for more complex factory control 2) Enhanced system extendibility
Facilities	1) Enhanced extendibility for 450 mm and facility cost reduction 2) AMC management, electric static control on masks, wafers, and facility surfaces

NGF TECHNOLOGY REQUIREMENTS INCLUSION

The FI focus areas activity concluded that a significant productivity improvement as NGF is to be promoted before 450 mm introduction. NGF is best described as systematic waste reduction approach that should facilitate comprehensive productivity improvement with the aid of proactive service visibility. NGF can be loaded with the so-called 300 mm Prime mission as well. The industry can focus on common technology development for the current wafer diameters and 450 mm.

WASTE REDUCTION MANAGEMENT

Waste reduction approach has been identified as the effective NGF driver. The ultimate goal for waste reduction is that all the technology requirements tables in the ITRS roadmap adopt waste reduction scheme, i.e., as a new driving axis in addition to the historic Si scaling cost reduction. Two high-level waste metrics have been introduced to promote this approach into Factory Operation technology requirements table. They are factory wait time waste (WTW) defined as a total sum of wait time for a wafer to go through all the process and factory equipment output waste (EOW) defined as opportunity loss of production calculated as normalized difference between instantaneous throughput and averaged throughput.

CROSS CUT ISSUES

Green fab initiatives, advanced process control (APC), fab temperature and humidity control, single wafer versus batch processing for thermal processes and 450 mm cross-cut issues are reflected to the requirements and solutions tables.

2010 HIGHLIGHTS

The FI team continues to focus on factory issues that are driven by cost, quality, productivity, and speed. Good progress has been made in developing the metrics and identifying potential solutions for these key drivers.

A major initiative in 2010 for the FI team was a focused effort on energy conservation and management. Energy consumption has become an increasingly important topic of public discussion in recent years because of global CO_2 emission and to reduce cost. An energy workshop was held in July 2010 to map and study the energy-related issues. The output of this workshop was a better understanding the challenges and an initial definition of the scope of work for the FI team in 2010/11. Working with other ITWGs, FI will start defining the metrics, challenges, key focus areas, and potential solutions, including more efficient process flows, reducing waste and improving energy use at the equipment level.

A logical progression might be: (i) baseline existing fab energy consumption at whatever level of granularity seems reasonable; (ii) identify challenges, potential solutions, and key focus areas and hence potential scope for energy reduction, and (iii) map this into technology tables for future years. The team also decided to start development of baseline process for generating metrics. Specifically, this will be used for the following:

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- Define a generic process flow
- Benchmarking/data quality
- Development of 300 mm/450 mm fab model for energy and related modeling/simulation

Table ITWG10 Factory Integration Difficult Challenges—Updated

Difficult Challenges through 2017	*Summary Of Issues*
1. Responding to rapidly changing, complex business requirements	• Increased expectations by customers for faster delivery of new and volume products (design → prototype and pilot → volume production)
	• Rapid and frequent factory plan changes driven by changing business needs
	• Ability to load the fab within manageable range under changeable market demand
	• Enhancement in customer visibility for quality assurance of high reliability products
2. Managing ever increasing factory complexity	• Quickly and effectively integrating rapid changes in process technologies
	• Increased requirements for high mix factories. Examples are (1) significantly short life cycle time of products that calls frequent product changes, (2) the complex process control as frequent recipe creations and changes for process tools and frequent quality control criteria due to small lot sizes
	• Manufacturing knowledge and control information need to be shared as required among factory operation steps and disparate factories
	• Need to concurrently manage new and legacy FICS software and systems with increasingly high interdependencies
	• Ability to model factory performance to optimize output and improve cycle time for high mix factories
	• Need to manage clean room environment for more environment susceptible processes, materials, and, process and metrology tools
	• Comprehending increased purity requirements for process and materials
3. Achieving growth targets while margins are declining	• Ability to visualize cost and cycle time for systematic waste reduction from all aspects.
	• Reducing complexity and waste across the supply chain; reducing white space in cycle times
	• Minimize the cost of new product ramp up against the high cost of mask sets and product piloting
4. Meeting factory and equipment reliability, capability and productivity requirements per the Roadmap	• Increased impacts that single points of failure have on a highly integrated and complex factory
	• More equipment reliability, capability and productivity visualization that can be used bidirectionally between equipment suppliers and users for more efficient task sharing
	• Design-in of equipment capability visualization in production equipment; design-in of APC to meet quality requirements
	• Equipment supplier roadmap for equipment quality visualization and improvement, and, reduction of Equipment Output Waste.
	Reduction of equipment driven NPW (non-product wafers) operations that compete for resources with production wafers and Dandori operations[1]
	• Moving from reactive to predictive paradigm for scheduling, maintenance and yield management
5. Emerging factory paradigm and next wafer size change	• Uncertainty about 450 mm conversion timing and ability of 300 mm wafer factories to meet historic 30% cost effectiveness.
	• Uncertainty concerning how to reuse buildings, equipment, and systems to enable 450 mm wafer size conversion at an affordable cost

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Table ITWG10 Factory Integration Difficult Challenges (continued)—Updated

Difficult Challenges Beyond 2017	*Summary of Issues*
1. Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	• Ability to utilize task sharing opportunities to keep the manufacturing profitable such as manufacturing outsourcing
	• Enhanced customer visibility for quality assurance of high reliability products including manufacturing outsourcing business models
	• Scalability implications to meet large 300 mm factory needs [40K–50K WSPM]
	• Cost and task sharing scheme on industry standardization activity for industry infrastructure development
2. Managing ever increasing factory complexity	• Higher resolution and more complications in process control due to smaller process windows and tighter process targets in many modules
	• Complexity of integrating next generation lithography equipment into the factory
	• More comprehensive traceability of individual wafers to identify problems to specific process areas
	• Comprehensive management that allows for automated sharing and re-usages of complex engineering knowledge and contents such as process recipes, APC algorithms, FD and C criteria, equipment engineering best known methods
	• Linking yield and throughput prediction into factory operation optimization
	• Real-time simulation in lock-step with production for operations prediction
3. Increasing global restrictions on environmental issues	• Need to meet regulations in different geographical areas
	• Need to meet technology restrictions in some countries while still meeting business needs
	• Comprehending tighter ESH/Code requirements
	• Lead free and other chemical and materials restrictions
	• New material introduction
4. Post-conventional CMOS manufacturing uncertainty	• Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements on factory design
	• Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition
	• Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency

Notes for Table ITWG10
[1] Dandori operations Peripheral equipment related operations that are in parallel or in-line and prior to or following to the main thread PE operations. So-called in-situ chamber cleaning is another good example than NPW operations.

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ASSEMBLY AND PACKAGING

Link to the 2010 Assembly and Packaging update file.

Link to 2009 Assembly and Packaging chapter.

The 2010 update of the Assembly and Packaging Chapter incorporates into our tables the major addition to the contained in the 2009 Edition. Many changes in the text and tables were driven by the rapid changes in three dimensional electronics and System in Package (SiP) architecture. The work for 2010 was focused on preparation for major changes to be incorporated in the 2011 edition, which will include expanded coverage of automotive electronics, optical component packaging including optical fiber data paths, LED packaging, and photovoltaic packaging requirements.

The materials used in packaging have had a major change in this decade with 100% of the packaging materials undergoing significant change. This will be followed in the next decade with half of the materials changing again as we adopt new nano-materials, new molecules, and complex composite materials. The section on materials will provide expanded coverage to address these new materials.

The expansion of 3D architectures for packaging poses unique challenges that are not encountered in conventional 2D packaging. These include:

- Thinning wafers and die, and the handling of these thinned wafer and die
- Thermal management when several layers of semiconductor devices are stacked
- Power delivery and the maintenance of power integrity as the operating voltages are dropped to near the threshold voltage
- Testing for 3D structures when test access is a challenge

These and other challenges are reflected in our Difficult Challenges table. There were no major changes in other tables for 2010. Minor changes to existing tables will be included in our 2011 edition. The Assembly and Packaging is also in the process of updating our System in Package paper which should be complete in early 2011. This update will reflect the significant changes made in SiP technology since the original publication of the paper. The growth of SiP and 3D integration results in a greater dependence on the cross-TWG interactions. This will be reflected in the major rewrite for 2011 which will include:

- Joint efforts with the Design ITWG to address the needs for design and simulation tools to address needs of 3D and deep sub-micron package requirements. The goal will be to perform the development cycles in the computer and avoid the cost and time required for multiple physical prototypes of each new product.
- Joint efforts with the Emerging Research Materials and Emerging Research Devices ITWGs to meet the materials properties required for new packaging and accommodate the packaging requirements for new device types as replacements for conventional CMOS are introduced.
- Joint efforts with the Test ITWG to define package architectures and test solutions that will satisfy the requirements to ensure quality and reliability for these new packages types particularly in 3D and for very high frequencies.
- Joint efforts with the Interconnect ITWG to ensure that we coordinate the interface between the global interconnect architecture and package interconnect architecture and identify a consistent set of challenges and potential solutions in the overlap areas.

DIFFICULT CHALLENGES

Innovation in assembly and packaging is accelerating in response to the realization that packaging is now the limiting factor in cost and performance for many types of devices. Near-term difficult challenges exist in all phases of the assembly and packaging process from design through manufacturing, test, and reliability.

Many critical technology requirements are yet to be met and they are listed in Table ITWG11 below. Meeting these requirements will demand significant investment in research and development.

Table ITWG11 Assembly and Packaging Difficult Challenges ≥16 nm—Updated

Difficult Challenges ≥16 nm	*Summary of Issues*
Impact of BEOL including Cu/low κ on packaging	-Direct wire bond and bump to Cu or improved barrier systems bondable pads - Dicing for ultra low k dielectric -Bump and underfill technology to assure ultra low-κ/ air gap dielectric integrity -Improved fracture toughness of dielectrics -Interfacial adhesion -Reliability of first level interconnect (increasing with decreasing contact pitch) -Mechanisms to measure the critical properties (particularly for thin layers and interfaces)
Wafer level Packaging	-Redistribution processing for pad pitch below 50 μm -Thermal management (for high power devices used in automotive and other areas) -Wafer thinning and handling technologies -TCE mismatch compensation for large die
Coordinated design tools and simulators to address chip, package, and substrate co-design	-Models for Reliability prediction -Rapid turn around modeling and simulation -Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis -Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching) -System level co-design(cm to nm) is needed now (including mixed signal and simulation). -EDA for "native" area array is required to meet the Roadmap projections.
Embedded components	-Low cost embedded passives: R, L, C -Embedded active devices -Quality levels required not attainable on chip -Die size for high C, low L integrated circuit matching die size -Wafer level embedded components
Thinned die packaging	-Wafer/die handling for thin die (must address die warpage) -Reliability -stress impact on device performance and assembly yield -Interconnect thickness and bonding for die stacking -Testability (ohmic contacts without damage)

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The Difficult Challenges for <16nm reflect the fundamental changes associated with continued scaling. The list is relatively short but the challenges are complex and will require substantial innovation.

Table ITWG11 Assembly and Packaging Difficult Challenges<16nm—Updated

Difficult Challenges < 16 nm	*Summary of Issues*
Close gap between chip and substrate	-Increased wireability at low cost -Improved impedance control and lower dielectric loss to support higher frequency applications -Improved planarity and low warpage at high process temperatures -Low-moisture absorption -Increased via density in substrate core -Production techniques will require silicon-like production and process technologies
High current density packages	-Electromigration will become a more limiting factor. -Thermal dissipation
Post CMOS switch devices	-The structures and materials employed will present serious challenges for packaging that will need to be addressed during this Roadmap period. The specifics of the requirements and challenges are not known at this time.

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ENVIRONMENT, SAFETY, AND HEALTH

Link to the 2010 Environment, Safety, and Health update file.

Link to 2009 ESH chapter.

The four basic ITRS ESH chapter strategies in 2010 remain as they were in the previous edition; namely:

1) Understand (characterize) processes and materials during the development phase;

2) Use materials that are less hazardous or whose by-products are less hazardous;

3) Design products and systems (equipment and facilities) that consume less raw material and resources and,

4) Make the factory safe for employees.

The significant new element added in 2009 was retained in 2010 for further validation, which is the addition of ESH Categories. Previous ESH chapter tables presented a requirements set that related ESH concerns to the technical thrusts (e.g., Interconnect, Front End Processes, etc.). They also identified ESH concerns that are broader and more general than those pertaining to a single technology thrust (referred to as "intrinsic").

To focus available resources toward those areas of greatest added benefit, in addition to the ESH improvements gained, all ESH requirements have now been placed in one of three Categories:

1. *Critical*—Any requirement in this category is an essential item for technology success/implementation as well as ESH benefits. If not addressed, it could compromise the ability to insert the technology into manufacturing.
2. *Important*—Any requirement in this category is a key item for process success as well as ESH benefits. If not addressed, it could compromise the cost of ownership (CoO) of the technology in manufacturing, based on factors such as throughput, yield, and chemical/material and/or tool costs.
3. *Useful*—Any requirement in this category is a key item for ESH benefits ("best practices"), but without any clear additional factors that would place it in either of the above two categories. If not addressed, it could compromise the ability to achieve the lowest ESH impact for the technology when inserted into manufacturing.

Some minor corrections to the tables were made in the 2010 revision, which include some simple word changes to add clarity to the intent of ESH technical requirements and correction of errors found in metric definitions so they match the associated values in technology requirements.

For 2011 two critical areas, both focused on materials, will be where efforts are concentrated. The first is defining research needs that decrease polarization of public/government policy expectations versus future technology needs, where critical materials are needed or new materials required to assure future technology. The second area is determining how to specify technology requirements in non-quantifiable or non-data supported terms where data do not exist, are not representative, or do not have granularity for defining a technical objective—while the objective remains important for ESH.

Table ITWG12 ESH Difficult Challenges ≥16 nm—Updated

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials can be utilized (without delay) in manufacturing, while protecting human health, safety, and the environment. Given the global movement possible for R&D, pre-manufacturing, and full commercialization, these methodologies must recognize regional regulatory /policy differences and the overall trends towards lower exposure limits and increased monitoring. • *Chemical Data Availability*: There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use In addition, methods for anticipating and forecasting such future requirements are not well developed.. • *Chemical Exposure Management*: There is incomplete information on how chemicals/materials are used and the process by-products formed. Also, while methods used to obtain such information are becoming more standardized, their availability varies depending on the specific issue being addressed, and can use improvement.
Process and equipment management	• *Process Chemical Optimization* There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). • *Environment Management* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations (including the capability for component isolation in waste streams) for such hazardous and non-hazardous emissions and by-products can be addressed. Global Warming Emissions Reduction: There is a need to limit emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Water and Energy Conservation* There is a need for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization* There is a need for more efficient chemical/material utilization, with improved reuse/recycling/reclaiming of them and their process emissions and byproducts. • *Byproducts Management*: There is a need for improved metrology for byproduct speciation. • *Chemical Exposure Management* There is a need to design-out chemical exposure potentials and the requirements for personal protective equipment (PPE) • *Design for Maintenance* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities use, and for more efficient cleanrooms' and facilities systems' thermal management. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics* There is a need for methodologies to define and measure a technology generation's sustainability. • *Design for ESH* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes and products. • *End-of-Life Reuse/Recycle/Reclaim* There is a need to design facilities, equipment and products to facilitate these end-of-life issues

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Table ITWG12 ESH Difficult Challenges <16 nm—Updated

Difficult Challenges < 16 nm	*Summary of Issues*
Chemicals and materials management	• *Chemical Assessment*: There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials can be utilized (without delay) in manufacturing, while protecting human health, safety, and the environment. • *Chemical Data Availability*: There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use • *Chemical Exposure Management*: There is incomplete information on how chemicals/materials are used and the process by-products formed.
Process and equipment management	· Chemical Reduction: There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). There is a need to limit emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Environment Management* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations for such hazardous and non-hazardous emissions and by-products can be addressed. • *Water and Energy Conservation* There is a need to reduce water and energy consumption, and for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization* There is a need for more efficient chemical/material utilization, with their increased reuse/recycle/reclaim (and of their process emissions and byproducts). • *Chemical Exposure Management* There is a need to design-out chemical exposure potentials and personal protective equipment (PPE) requirements. • *Design for Maintenance* There is a need to design equipment so that commonly serviced components and consumable items are easily and safely accessed, with such maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation*: There is a need to reduce energy, water and other utilities use, and for more efficient cleanrooms' and facilities systems' thermal management. • *Global Warming Emissions Reduction*: There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics* There is a need for methodologies to define and measure a technology generation's sustainability, and also sustainability at a factory infrastructure level. • *Design for ESH* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes and products, with methodologies to holistically evaluate and quantify the ESH impacts of facilities operations, processes, chemicals/materials, consumables, and process equipment for the total manufacturing flow. • *End-of-Life Reuse/Recycle/Reclaim*: There is a need to design facilities, equipment and products to facilitate these end-of-life issues

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YIELD ENHANCEMENT

Link to 2010 Yield Enhancement update file.

Link to 2009 Yield Enhancement chapter.

The key challenges were adapted to latest developments and challenges recognized by the 2010 Yield Enhancement ITWG. Currently, the most important key challenge will be "detection and identification of small yield limiting defects from nuisance." It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership, and high throughput. Furthermore, it is a challenge to identify yield-relevant defects under a vast amount of nuisance and false defects. In the long term the requirements for next generation inspection were identified.

Other topics challenging the yield enhancement community are prioritized as follows in the near term:

- *Detection and identification of small yield limiting defects from nuisance*—Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.
- *Non-visual defects and process variations*–Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.
- *3D inspection*—For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases.
- *Process stability versus absolute contamination level including the correlation to yield test structures*—Methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water, and substrate surface cleanliness.

In the long term the following key challenges are currently identified:

- *Next generation inspection*—As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm. Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy; near-field scanning optical microscopy; interferometry; scanning capacitance microscopy, and e-beam. This path finding exercise needs to assess each technique's ultimate resolution, throughput, and potential interactions with samples (contamination or degree of mechanical damage) as key success criteria.
- *In-line defect characterization and analysis*—Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and energy dispersive x-ray spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.
- *Development of model-based design-manufacturing interface*—Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.

The Yield Enhancement chapter consists of two active subchapters—"Defect Detection and Characterization," and "Wafer Environment and Contamination Control (WECC)." Two subchapters are currently not active for "Defect Budget" and "Yield Model and Yield Learning." The major work during 2010 was the control and update of the tables. The changes summarizes as follows.

- Defect Budget and Yield Model
  - In 2010 a new initiative collecting data from a defect budget survey of manufacturing sites in Japan, United States, and Europe was started. The aim of the survey is to supply defect density data for processes and equipment.
- Defect Detection and Characterization
  - The tables YE 4, YE5 and YE6 were checked carefully against latest developments for defect inspection and detection.
- Wafer Environment and Contamination Control
  - The table YE 7 was extended and checked carefully.

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Table ITWG14 Yield Enhancement Difficult Challenges ≥ 16 nm—Updated

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Detection and identification of Small Yield Limiting Defects from Nuisance - Detection of multiple killer defects and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.	Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. Reduction of inspection costs and increase of throughput is crucial in view of CoO. Detection of line edge roughness due to process variation. Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. Reduction of background noise from detection units and samples to improve the sensitivity of systems. Improvement of signal to noise ratio to delineate defect from process variation. Where does process variation stop and defect start?
Non-Visual Defects and Process Variations – Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.	Systematic Mechanisms Limited Yield (SMLY), resulting from unrecognized models hidden in the chip, should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. It is required to manage the above models at both the design and manufacturing stage. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the number of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis runs time per die. d) Statistical methodology to analyze results of logic diagnosis for denoising influence of random defects and building a layout-dependent systematic yield model. Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic yield loss, and has to improve their coverage.
3D Inspection – For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases.	Detection of non visible defects e.g. voids, embedded defects, and sub surface defects in the structures. The demand for high-speed and cost-effective inspection is crucial. Large number of contacts and vias per wafer E-beam inspection seems not to be the solution for all those tasks any more. Sensitivity of the inspection tool to process variation and definition of maximum process variation (control limits).
Process Stability vs. Absolute Contamination Level – Including the Correlation to Yield Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.	Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product Relative importance of different contaminants to wafer yield. Define a standard test for yield/parametric effect.
Wafer Edge and Bevel Monitoring and Contamination Control – Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems.	Currently, the monitoring and contamination control methods require intensive development.

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Table ITWG14 Yield Enhancement Difficult Challenges <16 nm—Updated

Difficult Challenges < 16 nm	*Summary of Issues*
Next Generation Inspection - As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm node.	Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This path finding exercise needs to assess each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.
In - line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality. [1]	Data volume + quality: strong increase of data volume due to miniaturization The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. It will be recommended to supply information on chemical state and bonding especially of organics. Small volume technique adapted to the scales of technology generations. Capability to distinguish between the particle and the substrate signal.
Development of model-based design-manufacturing interface — Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.	A lot of models should be operated at the design stage. For example, Optical Proximity Correction, Well Proximity, Stress Proximity, CMP and so on The Amount of models seems to be rapidly increasing. Not only accuracy of models, but also optimization of trade-off between models might be requested. Development of test structures for new technology generations

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METROLOGY

Link to 2010 Metrology update file.

Link to 2009 Metrology chapter.

2009 SUMMARY

Metrology requirements continue to be driven by advanced lithography processes, new materials, and Beyond CMOS materials, structures, and devices. The introduction of dual patterning and double exposure lithography add the complexity of measuring two distributions of linewidth, sidewall angle, and line width roughness inside the same measurement area. Another key challenge to critical dimension metrology is tool matching. Precision requirements for the next several years can be met using single tools. There are many gaps in metrology for EUV lithography especially for mask metrology. The entire mask fabrication process needs advances in capability especially for actinic patterned mask inspection and aerial imaging. Overlay metrology capability lags behind the need for improved overlay control. Front end processes continue to drive metrology to provide measurements for new higher dielectric constant materials, dual work function metal gates, and new ultra shallow junction doping processes. The sub 1 nm EOT gate stacks require greatly improved film thickness and composition control during manufacturing. Interconnect structures continue the cycle of new materials. The need for porosity control for low k materials has driven a renewed interest in porosity measurements. 3D interconnect metrology requirements are largely driven by the activity in through silicon vias (TSV) R&D. Bonded wafer overlay control for next generation TSV now has potential solutions that are under investigation. In the area of metrology for Beyond CMOS R&D, graphene measurements have advanced in the areas of microscopy and electrical characterization. In addition, there are now several means of determining the number of graphene layers in a sample. The need for understanding large area graphene uniformity is driving both physical and electrical metrology. In addition, metrology R&D is working with other Beyond CMOS materials.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 22 nm technology generation. Metrology needs after 2015 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table ITWG15 presents the ten major challenges for metrology.

Table ITWG15 Metrology Difficult Challenges

Difficult Challenges ≥16 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of new process technology such as Dual Patterning Lithography, complicated 3D structures such as capacitors and contacts for memory, and 3D Interconnect are not ready for their rapid introduction.	Overlay measurements for Dual Patterning have tighter control requirements. Overlay defines CD. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures including capacitors, devices, and contacts.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges <16 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks. Sampling plan optimization is key to solve these issues.
Statistical limits of sub-32 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for *beyond CMOS.*	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

MODELING AND SIMULATION

Link to 2010 Modeling and Simulation update file.

Link to 2009 Modeling and Simulation chapter.

SUMMARY

Modeling and Simulation software tools span the entire semiconductor world. These tools are being used daily with increasing efficiency. The Modeling and Simulation (M&S) chapter of the ITRS presents specific needs to increase this effectiveness and to provide impact on the semiconductor industry in the future. Similar to the other chapters of the ITRS, in the Modeling and Simulation chapter only the tables have been revised in the 2010 Update. Besides this, the preparations for the next full version of the ITRS, the 2011 edition, have been started. Again in 2010, much effort has been spent on the analysis of the requirements of the other chapters towards the Modeling and Simulation chapter, based on face-to-face meetings with other ITWGs in the ITRS and the extraction of relevant material from their documents This analysis has on one hand been used as background and input for the discussions on the 2010 update of the Modeling and Simulation tables, and on the other hand will be further updated throughout 2010 and until the edit deadline of the 2011 ITRS, to serve as a key input to the 2011 Modeling and Simulation chapter.

Concerning the *Modeling and Simulation Difficult Challenges*, mainly the scope of the challenge on integrated modeling from equipment through devices was extended. It now reads "Integrated modeling of equipment, materials, feature scale processes and influences on device and circuit performance and reliability, including random and systematic variability". Especially, it now additionally includes "Pattern/microloading effects in radiative annealing or plasma processing" and "Propagation of process variations into circuit block simulation". Besides this, several details were updated in the other challenges, among others due to the selection of favourable options for beyond CMOS devices by the ERD ITWG.

The table *"Modeling and Simulation Technology Requirements: Capabilities—Near-term Years"* again summarizes the needs in the areas of process, device, circuit and package simulation, and includes premier general requirements on tools. The most important changes are as follows: Concerning *lithography simulation*, "Innovative 193 nm immersion multiple patterning" was included, due to the prioritization of technological options by the Lithography ITWG. In the requirements *for numerical device modeling*, the simulation of random device variability was added as a new requirement for device modeling in 2010, especially concerning the efficient inclusion in commercial simulation tools. Several items have been delayed by one year due to the state-of-the-art not yet meeting the needs.

Compared to this the M&S table on "*Modeling and Simulation Technology Requirements: Capabilities—Long-term Years*" is far less detailed, because long-tem technology options are so far only partly defined or prioritized in the other parts of the ITRS. Generally, this long-term requirements table contains a majority of "*red" items* for which so far no solutions are known. Partly this is due to the fact that the technological options are not yet known or prioritized, and in turn also simulation approaches can not yet be developed or selected. Another problem is the inherent difficulty to develop models and tools to meet the ambitious requirements—in turn, the success of the development work required from M&S cannot be predicted ten or more years in advance.

The table on *"Modeling and Simulation Technology Requirements: Accuracy—Near-term Years"* is quite similar to the other requirement tables grouped into lithography modeling, front end process modeling, topography modeling, numerical device modeling, circuit element modeling/ECAD, and package modeling. Here, the estimate of about one third, given for the cost and time reduction from use of TCAD in best practice cases reported by industry, is based on an industrial survey already discussed in the 2008 ITRS. In this table, accuracy refers to models and tools calibrated to a certain technology (at a company), not to a certain experiment. Most accuracy specifications are given as percent of the respective nominal value or of some top-level parameter of the respective technology node, e.g., the physical gate length. A key issue in the preparation of this table has been how to define the accuracy of simulation when comparing with experiment which themselves have a significant inaccuracy or uncertainty. Detailed definitions made are listed in the footnotes of the table, e.g., "compared with median value of statistically meaningful samples". Furthermore, the table does not only specify the required accuracy in the simulation of nominal values like a junction depth, but also the accuracy of the sensitivity of such values with respect to changes in process conditions. This is important for tracing the impact of process variations through a simulation sequence, as requested in M&S subchapter on "Modeling for Design Robustness, Manufacturing and Yield" of the 2009 ITRS. In the 2010 Update, some details were changed in the definition of the items specified, compared with the 2009 ITRS. Furthermore, the specification for *gate 2D/3D topography accuracy* has been identified as somewhat duplicating the other topography specifications, and has therefore been skipped. For the error of the output characteristics of devices, in the 2010 Update no more difference is made between the saturation and the linear region. Some changes compared to the 2009 ITRS in the absolute accuracies specified are due to slight modifications of top-level ITRS specifications, like printed gate length, late in the 2009 process.

Table ITWG16 Modeling and Simulation Difficult Challenges—Updated

Difficult Challenges ≥ 16 nm	*Summary of Issues*
Lithography simulation including EUV	Models and experimental verification of optical and non-optical immersion lithography effects (e.g., topography and change of refractive index distribution)
	Simulation of multiple exposure/patterning including database splitting
	Multi-generation lithography system models
	Simulation of defect influences/defect printing in EUV. Mask optimization including defect compensation
	Optical simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including extensions for inverse lithography
	Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects
	Predictive and separable resist models (e.g., mesoscale models) including line-edge roughness, accurate profiles, topcoat interactions, etch resistance, adhesion, mechanical stability, leaching, and time-dependent effects in in single and multiple exposure
	Resist model parameter calibration methodology (including kinetic and transport parameters)
	Fast, predictive simulation of ebeam mask making (single-beam and multibeam)
	Simulation of directed self-assembly of sublithography patterns
	Modeling lifetime effects of equipment and masks, including lens and mirror heating effects
	Predictive coupled deposition-lithography-etch simulation (incl. double patterning, self-aligned patterning)
	Modeling metrology equipment for enhancing its accuracy
Front-end process modeling for nanometer structures	Coupled diffusion/activation/damage/stress models and parameters including SPER and millisecond processes in Si-based substrate, that is, Si, SiGe, SiGe:C, Ge-on-Si, III/V-on-Si, SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers
	Diffusion in advanced gate stacks
	Predictive segregation and dose loss models
	Modeling of interface and dopant passivation by hydrogen or halogens
	Modeling of cluster or cocktail implants
	Modeling of plasma doping, e.g. for FinFETs. Predictive modeling of de-activation of dopants.
	Modeling of epitaxially grown layers: Shape, morphology, stress, defects, doping, diffusion, activation
	Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
	Efficient and robust 3D meshing for moving boundaries
	Modeling the impact of front-end processing-induced damage to devices on their leakage, noise and reliability bahavior during operation
Integrated modeling of equipment, materials, feature scale processes and influences on device and circuit performance and reliability, including random and systematic variability	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-) products, rates ...) , and simplified but physical models for complex chemistry and plasma reaction.
	Linked equipment/feature scale models (including high-κ metal gate integration, damage prediction)
	Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
	Spin-on-dielectrics (stress, poriosity, dishing, viscosity, …) for high aspect ratio fills
	Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
	Pattern/microloading effects in radiative annealing or plasma processing
	Propagation of process variations into circuit block simulation
	Simulation of polishing, grinding and wafer thinning in backend processes
	Efficient extraction of impact of equipment - and/or process induced variations on devices and circuits, using simulations
Nanoscale device simulation capability: Methods, models and algorithms	General, accurate, computationally efficient and robust quantum based simulators incl. fundamental parameters linked to electronic band structure and phonon spectra
	Efficient models and tools for-analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
	Models (incl. material models) to investigate new memory devices like STT-MRAM, nanoionic memories, PCM/PRAM, etc
	Gate stack models for ultra-thin/high-k dielectrics with respect to electrical permittivity, built-in charges, influence on workfunction by interface interaction with metals, reliability, tunneling currents and carrier transport

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Difficult Challenges ≥ 16 nm	*Summary of Issues*
	Modeling of salicide/silicon contact resistance and engineering (e.g. Fermi-level depinning to reduce Schottky barrier height)
	Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure and dopant variations in order to assess the impact of variations on statistics of device performance
	Physical models for novel channel materials, e.g., Ge and compound III/V channels …: Band structure, defects/traps, ...
	Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation
	Reliability modeling for ultimate CMOS
	Device simulators (software) for STT and nanoionic memories
	Physical models for stress induced device performance
Electrical-thermal-mechanical-modeling for interconnect and packaging	Model thermal-mechanical, thermodynamic and electrical properties of low κ, high κ, and conductors for efficient on-chip and off-chip incl. SIP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension
	Thermal modeling for 3D ICs and assessment of modeling and CAD tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keepout regions, …). Size effects (microstructure, surfaces, ...) and variability of thinned wafers.
	Signal integrity modeling for stacked die
	Identify effects and apply/extend models which influence reliability of interconnects/packages incl. 3D integration (e.g., stress voiding, electromigration, fracture initiation, dielectric breakdown, piezoelectric effects)
	Physical models and simulation tools to predict adhesion and fracture toughness on interconnect-relevant interfaces (homogeneous and heterogeneous), packages and die interfaces
	Dynamic simulation of mechanical problems of flexible substrates and packages
	Models for electron transport in ultra fine patterned interconnects
Circuit element and system modeling for high frequency (up to 300 GHz) applications	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package: - possibly consisting of different technologies, - covering and combining different modelling and simulation levels as well as different simulation domains
	Scalable active component circuit models [1] including non-quasi-static effects, substrate noise and coupling, high-frequency RT and 1/f noise, temperature and stress layout dependence and parasitic coupling
	Scalable passive component models [1] for compact circuit simulation, including interconnect, transmission lines, …
	Scalable circuit models [1] for More-than-Moore devices including switches, filters, accelerometers, …
	Physical circuit element models for new memory devices, such as PCM, and standardization of models for III/V devices
	Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently
	Computer-efficient assessment of building block/circuit-level using process/device/circuit simulation, including process variations

Notes for Table ITWG16
[1] In More than Moore, scalability refers to the ability to model litho-defined device variations.

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Table ITWG16 Modeling and Simulation Difficult Challenges <16nm—Updated

Difficult Challenges < 16 nm	*Summary of Issues*
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: 1) Layer stacks for gates, junctions and channels: Predictive modeling of dielectric constant, bulk polarization charge, ferroelectric/-magnetic properties, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. 2) Models for novel integrations in 3D interconnects including data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties 3) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications. 4) Accumulation of databases for semi-empirical computation.
Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials	Ab-initio modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping, quantum dots, atomic electronics, multiferroic materials and structures, strongly correlated electron materials)
	Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport, …). Modeling impact of geometry, interfaces and bias on transport for carbon-based nanoelectronics
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, fast and efficient optical interconnect models of larger domains, semiconductor laser modeling
	Physical design tools for integrated electrical/optical systems
	Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects & impact on LER); heating and charging effects), including impact on device characteristics (e.g. due to local crystal damage by electron scattering or charging effects)
NGL simulation	Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

Notes for Table ITWG16
[1] In More than Moore, scalability refers to the ability to model litho-defined device variations.

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GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (ALSO WITH OBSERVATIONS AND ANALYSIS)

Moore's Law—An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that device affordability must be taken into account and also performance. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been recently acknowledged and celebrated as a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 40 years.

Scaling ("More Moore")—

- *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)* refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)* refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
    - "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures."
    - Addresses the need for quantifiable, specific Design Technologies that address the power and performance trade-offs associated with meeting "More Moore" functionality needs, and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—The incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

- Design technologies enable new functionality that takes advantage of More than Moore technologies.
- "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology."
- Addresses the need for design technologies which enable functional diversification

Beyond CMOS—emerging research devices, focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switch, NEMS switches, etc.

CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle

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timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets.

MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

As defined above, additional "Equivalent Scaling" process technologies can be combined with transistor gate dimensional scaling technology advancement to further advance the performance and power-management characteristics of a device. The "Equivalent Scaling" technologies can also be "mix-and-matched" by companies within their specific product fabs. In some cases the most recent ITRS ITWG surveys have indicated that dimensional scaling (both gate length and gate material thickness) reduction can be slowed and still meet power management and performance requirements, when traded off with "equivalent scaling" process insertion.

Some (not comprehensive or complete) examples of "equivalent scaling" process and transistor design technology are: copper interconnect; low-K interconnect materials; strained silicon; high-K/metal gate; fully depleted silicon-on-insulator (FDSOI); multiple-gate 3-D transistors, III-V gate material; etc.

It should be noted that the timing of availability and implementation of "equivalent scaling" process insertion may not be as regular as dimensional cycles. See the Interconnect and process integration and device structures (PIDS) chapters for additional technology description and timing details.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to the "Moore's Law" driver of functions/chip doubling every two years , there has been a historically-based "corollary" to the "law," which suggests that, to be affordable and competitive, manufacturing productivity improvements must also enable the cost-per-function (micro-cents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 2 years, cost per function must also reduce by half every 2 years (-29%/year average). On average then cost-per-chip (packaged unit) , for affordability, could remain approximately constant (requires both flat chip cost targets and flat back-end packaging targets to remain constant), If functionality doubles only every three years, then the manufacturing cost per chip (packaged unit) can remain flat if the cost per function reduction rate slows to one-half every 3 years.(-21%/year average). It should be noted that this simplistic manufacturing cost affordability model, used as a first-order driver for the ITRS, does not take into account the economic supply and demand market complexity of actual external market environments.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A Flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two to four bits of data in the same physical area.

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MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two and level-three (L2 and L3) cache. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation.

High-performance MPU[2]—MPU product optimized for maximum system performance by combining a single or multiple CPU cores with large level-two and level-3 (L2 and L3) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory. Recently the typical pattern among MPU products is to keep the number of cores constant within a generation and double the number of transistors within each core, and the latest ITRS ORTC modeling reflects this trend in the table targets.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip had increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is still maintained, although the latest consensus ITRS forecast of cell-area-factor improvement to 4 by 2011, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate. Therefore, the latest ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The latest ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology generation processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology generation, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples.

Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2005 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (typically <1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

[2] *Note: The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.*

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, 10K/month or higher, depending upon die size and wafer generation size) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 2a in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: .5 Gb/production, 4 G/introduction, plus 256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2009 ITRS, the typical high-performance ASIC (hpASIC) design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 74% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 56% at the production level, and also for shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C = Af^2 = 0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=74% of total chip area, the $C_{AVE} = C/E = 0.35\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.35e-6 mm^2/bit = 376 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two to four bits in the same cell area, creating a multi-level-cell (MLC)

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"virtual" per-bit size that is one-half to one-fourth the size of an SLC product cell size and will also have a "virtual area factor" that is half to one-fourth of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 10–15 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2–3 times greater than an SRAM 6t cell area factor, and 30–40 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology generation. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology generation. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology generation, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

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MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first production-qualified development manufacturing facilities. Additional clarification was added by the IRC in 2009 to differentiate the new 450 mm wafer generation early consortia pilot line equipment readiness from the timing of anticipated production readiness and ramp.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

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APPENDIX—ITRS TABLES LISTING

Link to the 2010 Update webpage.

SYSTEM DRIVERS

	Table SYSD1	Major Product Market Segments and Impact on System Drivers
	Table SYSD2	SOC Consumer Driver Design Productivity Trends
	Table SYSD3	Projected Mixed-Signal Figures of Merit for Four Circuit Types
	Table SYSD4	Embedded Memory Requirements
	The System Drivers chapter did not have table updates. The following figures were updated for 2010:	
Updated	Figure SYSD5	SOC Consumer Portable Design Complexity Trends
Updated	Figure SYSD6	SOC Consumer Portable Power Consumption Trends
Updated	Figure SYSD7	SOC Consumer Portable Processing Performance Trends
Updated	Figure SYSD9	SOC Consumer Stationary Design Complexity Trends
Updated	Figure SYSD10	SOC Consumer Stationary Performance Trends
Updated	Figure SYSD11	SOC Consumer Stationary Power Consumption Trends

DESIGN		
	Design Chapter section update	Analog, Mixed-Signal and RF Specific DT Trends and Challenges
	Table DESN1	Overall Design Technology Challenges
	Table DESN2	System-Level Design Requirements
	Table DESN3	Correspondence Between System-Level Design Requirements and Solutions
	Table DESN4	Logical/Circuit/Physical Design Technology Requirements
	Table DESN5	Correspondence Between Logical/Circuit/Physical Requirements and Solutions
	Table DESN6	Design Verification Requirements
	Table DESN7	Correspondence Between Design Verification Requirements and Solutions
	Table DESN8	Design for Test Technology Requirements
	Table DESN9	Design for Manufacturability Technology Requirements
	Table DESN10	Correspondence Between Design for Manufacturability Requirements and Solutions
	Table DESN11	Design Technology Improvements and Impact on Designer Productivity
	The Design chapter did not have table updates. The following figure was updated for 2010:	
Updated	Figure DESN1	Impact of Design Technology on SoC SOC Consumer Portable Implementation Cost

TEST AND TEST EQUIPMENT		
Updated	Table TST1	Summary of Key Test Drivers, Challenges, and Opportunities
Updated	Table TST2	Multi-site Test for Product Segments
	Table TST3	"Stages" of Adaptive Test
	Table TST4	Implications of Adaptive Test

TEST AND TEST EQUIPMENT		
Updated	Table TST5	System on Chip Test Requirements
Updated	Table TST6	Logic Test Requirements
	Table TST7	Vector Multipliers
Updated	Table TST8	Memory Test Requirements
	Table TST9	Mixed-signal Test Requirements
Updated	Table TST10	RF Test Requirements
	Table TST11	Burn-in Requirements
	Table TST12	Test Handler and Prober Difficult Challenges
	Table TST13	Prober Requirements
	Table TST14	Handler Requirements
Updated	Table TST15	Probing Difficult Challenges
Updated	Table TST16	Wafer Probe Technology Requirements
	Table TST17	Test Socket Technology Requirements

RF AND AMS FOR WIRELESS		
Updated	Table RFAMS1	RF and Analog Mixed-Signal CMOS Technology Requirements
Updated	Table RFAMS2	RF and Analog Mixed-Signal Bipolar Technology Requirements
	Table RFAMS3	On-Chip Passives Technology Requirements
	Table RFAMS4	Off-Chip Passives Technology Requirements
Updated	Table RFAMS5	Power Amplifier Technology Requirements
Updated	Table RFAMS6	Base Station Devices Technology Requirements
Updated	Table RFAMS7	Millimeter Wave 10 GHz–100 GHz Technology Requirements
	Table RFAMS8	RF and Analog Mixed-Signal RFMEMS
Updated	Figure RFAMS2	0.4 GHz–10 GHz Potential Solutions
Updated	Figure RFAMS3	10 GHz–100 GHz Potential Solutions

PROCESS INTEGRATION, DEVICES, AND STRUCTURES (PIDS)		
	Table PIDS1	Process Integration, Devices, and Structures Difficult Challenges
	Table PIDS2	High-performance Logic Technology Requirements
Updated	Table PIDS3A	Low Standby Power Technology Requirements
Updated	Table PIDS3B	Low Operating Power Technology Requirements
Updated	Table PIDS4	DRAM Technology Requirements
Updated	Table PIDS5	NAND Flash Technology Requirements
	Table PIDS5A	Requirements for Spin-Torque Transfer (STT) MRAM
	Table PIDS6	Reliability Technology Requirements

EMERGING RESEARCH DEVICES	
	Please refer to the ERD summary in the 2010 Update Overview with respect to the Future Memory Devices Workshop

EMERGING RESEARCH MATERIALS		
	Please refer to the ERM summary in the 2010 Update Overview with respect to the Future Memory Devices Workshop	

FRONT END PROCESSES		
	Table FEP1	Front End Processes Difficult Challenges
	Table FEP2	High Performance Device Technical Requirements
	Table FEP3	Low Operating Power Device Technical Requirements
	Table FEP4	Low Standby Power Devices Techical Requirements
	Table FEP5	DRAM Stacked Capacitor Technology Requirements
	Table FEP6	Floating Gate FLASH Non-volatile Memory Technology Requirements
	Table FEP7	Charge Trapping FLASH Non-volatile Memory Technology Requirements
	Table FEP8	Phase Change Memory (PCM) Technology Requirements
	Table FEP9	FeRAM Technology Requirements
	Table FEP10	Starting Materials Technology Requirements
	Table FEP11	Front End Surface Preparation Technology Requirements
	Table FEP12	Thermal, Thin Film, Doping Process Technology Requirements
Updated	Table FEP13	Etching Process Technology Requirements
	Table FEP14	Shallow Trench Isolation CMP Process Technology Requirements
Updated	Figure FEP16	Surface Preparation Potential Solutions

LITHOGRAPHY		
	Table LITH1	Various Techniques for Achieving Desired CD Control and Overlay with Optical Projection Lithography for MPU and DRAM
Updated	Table LITH2A	Lithography Difficult Challenges >16nm
Updated	Table LITH2B	Lithography Difficult Challenges ≤16nm
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	Table LITH4B	Resist Sensitivities
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Updated	Table LITH5B	Double Patterning / Spacer Requirements
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	Table LITH6	Maskless Lithography Technology Requirements
Updated	Figure LITH3	DRAM and MPU Potential Solutions—Updated
NEW	Figure LITH4	Flash Potential Solutions—New for 2010

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	Table INTC1	3D Interconnect Technologies Based on the Interconnect Hierarchy
	Table INTC2	3D-WLP Via Pitch Requirements Based on Table ORTC-4 Chip Pad Pitch Trend (μm)
Updated	Table INTC3	Global interconnect level 3D-SIC/3D-SOC roadmap
Updated	Table INTC4	Intermediate interconnect level 3D-SIC roadmap

INTERCONNECT		
Updated	Table INTC5	2009 Interconnect Difficult Challenges
Updated	Table INTC6	MPU Interconnect Technology Requirements
	Table INTC7	DRAM Interconnect Technology Requirements
	Table INTC8	Interconnect Surface Preparation Technology Requirements
	Table INTC9	Advantages and Concerns for Cu Extensions, Replacements and Native Device Interconnects.
	Table INTC10	Minimum Density of Metallic SWCNTs Needed to Exceed Minimum Cu Wire Conductivity
Updated	Figure INTC15	Planarization Applications and Equipment Potential Solutions
Updated	Figure INTC16	Planarization Consumables Potential Solutions

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Updated	Table FAC2	Key Focus Areas and Issues for FI Functional Areas Beyond 2009
Updated	Table FAC3	Factory Operations Technology Requirements
Updated	Table FAC4	Context Data Importance for Good Equipment Visibility
Updated	Table FAC5	Production Equipment Technology Requirements
Updated	Table FAC6	Material Handling Systems Technology Requirements
Updated	Table FAC7	Factory Information and Control Systems Technology Requirements
Updated	Table FAC8	Facilities Technology Requirements
Updated	Table FAC9	Crosscut Issues Relating to Factory Integration

ASSEMBLY AND PACKAGING		
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	Table AP2	Single-chip Packages Technology Requirements
	Table AP3	Chip-to-package Substrate Technology Requirements
	Table AP4	Package Failure Modes
	Table AP5	Substrate to Board Pitch
	Table AP6	Package Warpage at Peak Processing Temperature
	Table AP7	Package Substrates: Low Cost (PBGAs
	Table AP8	Package Substrates: Hand-held (FBGA)
	Table AP9	Package Substrates: Mobile Products (SiP, PoP)
	Table AP10	Package Substrates: Cost performance (CPU, GPU,Game Processor)
	Table AP11	Package Substrates: High Performance (High End)
	Table AP12	Package Substrates: High Performance (LTCC)
	Table AP13	Wafer Level Packaging
	Table AP14	Key Technical Parameters for Stacked Architectures Using TSV
	Table AP15	System in Package Requirements
	Table AP16	Difficult Challenges for SiP
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	Table AP20	Telecommunications: Long Haul (100's of Km) to Metro (>1Km)
	Table AP21	Datacom Receivers: Short range LAN, FTTX, Active Optical Cable (AOC), Backplane, On-circuit Board and On-to and Off-of chip Data Transfer Applications
	Table AP22	Difficult Challenges for Optical Packaging
	Table AP23	Technology Requirements for Optical Packaging
	Table AP24	Potential Solutions for Optical Packaging
	Table AP25	Cross TWG Issues for Optoelectronics
	Table AP26	High Brightness LEDs
	Table AP27	MEMS Packaging Methods
	Table AP28	MEMS Packaging Examples
	Table AP29	Automotive Operating Environment Specifications
	Table AP30	Multiple-Sun Photovoltaic Cell Packaging Issues
	Table AP31	Thinned Silicon Wafer Thickness 200 mm/300 mm
	Table AP32	Challenges and Potential Solutions in Thinning Si Wafers
	Table AP33	Materials Challenges
	Table AP34	Packaging/Gaps/Technology Needs Summary
	Table AP35	Consortia and Research Institutes in Packaging Technology

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Updated	Table ESH1a	ESH Difficult Challenges—Near- and Long-term Years
	Table ESH2	ESH Requirements by Domain and Category
Updated	Table ESH3a	ESH Intrinsic Requirements—Near-term Years
Updated	Table ESH3b	ESH Intrinsic Requirements—Long-term Years
	Table ESH4a	Chemicals and Materials Management Technology Requirements—Near-term Years
	Table ESH4b	Chemicals and Materials Management Technology Requirements—Long-term Years
	Table ESH5a	Process and Equipment Management Technology Requirements—Near-term Years
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YIELD ENHANCEMENT		
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Updated	Table YE2	Yield Enhancement Difficult Challenges
	Table YE3	Defect Budget Technology Requirement Assumptions
Updated	Table YE4	Defect Inspection on Pattern Wafer Technology Requirements
Updated	Table YE5	Defect Inspection on Unpatterned Wafers: Macro, and Bevel Inspection Technology Requirements
Updated	Table YE6	Defect Review and Automated Defect Classification Technology Requirements
Updated	Table YE7	Technology Requirements for Wafer Environmental Contamination Control

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*METROLOGY**		
**ONLY A FEW COLOR CHANGES WERE MADE TO A FEW TABLES FOR 2009; AS SUCH THESE TABLES ARE NOT INDICATED AS UPDATED. (SOME 2010 CELLS WERE CHANGED FROM YELLOW TO WHITE.)		
	Table MET1	Metrology Difficult Challenges
	Table MET2	Metrology Technology Requirements
	Table MET3	Lithography Metrology (Wafer) Technology Requirements
	Table MET4a	Lithography Metrology (Mask) Technology Requirements: Optical
	Table MET4b	Lithography Metrology (Mask) Technology Requirements: EUV
	Table MET5	Front End Processes Metrology Technology Requirements
	Table MET6	Interconnect Metrology Technology Requirements

MODELING AND SIMULATION		
Updated	Table MS1	Modeling and Simulation Difficult Challenges
Updated	Table MS2A	Modeling and Simulation Technology Requirements: Capabilities—Near-term Years
Updated	Table MS2B	Modeling and Simulation Technology Requirements: Capabilities—Long-term Years
Updated	Table MS3	Modeling and Simulation Technology Requirements: Accuracy [1] —Near-term Years

Link to the 2010 Update webpage.