

ClearSpeed kicks it up a notch

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At almost exactly this time last year, a company called ClearSpeed Technologies [made waves](#) on the hardware scene with some pretty incredible claims about the performance of their first product: an add-in daughtercard for the PC that featured a processor, the CS301, with 64 floating-point "processing elements" that could allegedly do 25.6 Gflops.

In a lengthy [news post](#) that was actually more of a mini-article, I took a look at the CS301 and compared it to the PS2's Emotion Engine. In brief, the original card featured an array of 64 PE's, each of which consisted of two floating-point execution units, a register file, a 4K data cache, and an interface unit. The 200MHz, 40 million-transistor, 0.13-micron processor was remarkable in that it [consumed only 2 Watts](#) of power; so that's quite a bit of Gflop power per Watt.

The successor to the CS301, [codenamed Avebury](#), features 96 cores per chip and runs at 250MHz, with an integrated DDR2 interface. Regarding the latter feature, in my original post, I suggested that RAMBUS would be preferable because its combination of high bandwidth, high granularity, and low pin count made it a great fit for a daughtercard. But RAMBUS has since disappeared off the consumer radar, so oh well. At any rate, there's more per-chip horsepower on Avebury than on the CS301.

Avebury's individual processing elements have also been beefed up, and each PE now has an integer MAC, in addition to the dual-pipeline FPU (FMAC + ALU). Furthermore cache size of each PE has been increased to 6K. The addition of integer hardware will increase the flexibility of the design and broaden its appeal. As for the increased d-cache size, it should probably be seen in light of the increased number of PE's per chip. Pretty much any application that you use a chip like this for will be cache-polluting, so the real performance issue will be the amount of bandwidth in the fabric connecting the PEs. But having more cache on each individual PE has got to help with moving all that data around a network of that size.

All of Avebury's new hardware comes at a price, though. The new chip consists of 96 million transistors on a .13u copper process, and its power consumption is over twice that of the CS301. Still, 5 Watts for what ClearSpeed claims is a 50Gflop chip ain't too shabby. Finally, the pipes that connect Avebury to the rest of the daughterboard have been increased.

One of the take-home points from my original ClearSpeedpost was that there wasn't enough bandwidth on the PC to really feed this thing. But the bandwidth situation has now been improved with the introduction of PCIe hardware, and it's only going to get better. Avebury is made to go in a PCI-X slot, but ClearSpeed claims that PCIe support will be forthcoming.

I think it's worth keeping an eye on this chip--on how it performs in the real world, and on how well software writers are able to take advantage of it. The type of overall approach embodied by this chip is pretty close to what IBM is working on for the PS3, which brings me to the final thing that I want to note about ClearSpeed. The PE's on their chips are described as "VLIW cores," and that makes a lot of sense. There's not (yet) enough room in a stripped-down mini-core like this to put out-of-order execution logic, so you want to move as much instruction scheduling work as you can to the compiler. For this reason, I think it's likely that the PS3 will also be VLIW, like the vector units in the PS2.

Finally, when you combine VLIW with support for multithreading in the way that ClearSpeed has done, and in the way that the PS3 is likely to do, you wind up with a situation where compilers and software writers have a lot of responsibility for performance. That situation should be familiar to the brave souls who coded the first games for the PS2.

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