

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Milton Clair Webb, et al.
U.S. Patent No.: 9,831,306 Attorney Docket No.: 39843-0151IP1
Issue Date: November 28, 2017
Appl. Serial No.: 15/024,750
Filing Date: December 19, 2013
Title: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT
AND METHOD TO FABRICATE SAME

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 9,831,306 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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EXHIBITS

SAMSUNG-1001	U.S. Patent No. 9,831,306 to Webb, et al. (“the ’306 Patent”)
SAMSUNG-1002	Excerpts from the Prosecution History of the ’306 Patent (“the Prosecution History”)
SAMSUNG-1003	Declaration of David Kuan-Yu Liu
SAMSUNG-1004	U.S. Patent Pub. No. 2015/0054078 to Xie (“Xie”)
SAMSUNG-1005	U.S. Patent No. 9,397,217 to Tseng (“Tseng”)
SAMSUNG-1006	U.S. Patent Pub. No. 2012/0086055 to Anderson (“Anderson”)
SAMSUNG-1007	U.S. Patent No. 9,041,125 to Lin (“Lin”)
SAMSUNG-1008	U.S. Patent Pub. No. 2013/0026572 to Kawa (“Kawa”)
SAMSUNG-1009	U.S. Patent Pub. No. 2007/0080380 to Chang (“Chang”)
SAMSUNG-1010	U.S. Patent No. 9,324,790 to Akarvardar (“Akarvardar”)
SAMSUNG-1011	U.S. Patent No. 8,994,116 to Gan (“Gan”)
SAMSUNG-1012	U.S. Patent No. 11,037,923 to Bohr (“Bohr”)
SAMSUNG-1013	U.S. Patent No. 7,898,037 to Chuang (“Chuang”)
SAMSUNG-1014	U.S. Patent No. 9,166,053 to Kuo (“Kuo”)
SAMSUNG-1015	U.S. Patent Pub. No. 2013/0164924 to Shieh (“Shieh”)
SAMSUNG-1016	U.S. Patent No. 8,895,381 to Cheng (“Cheng”)
SAMSUNG-1017	U.S. Patent No. 9,196,613 to Basker (“Basker”)
SAMSUNG-1018	Robert H. Havemann and James A. Hutchby, “High-Performance Interconnects: An Integration Overview,”

Proceedings of the IEEE, vol. 89, no. 5, pp. 586-601, May 2001

SAMSUNG-1019	Dick James, “Intel Ivy Bridge Unveiled – The First Commercial Tri-Gate, High-k, Metal-Gate CPU,” Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, September 2012
SAMSUNG-1020	U.S. Patent No. 8,492,841 to Anderson (“Anderson-841”)
SAMSUNG-1021	U.S. Patent Pub. No. 2012/0037996 to Schultz (“Schultz”)
SAMSUNG-1022	U.S. Patent No. 8,952,424 to Herberholtz (“Herberholtz”)
SAMSUNG-1023	U.S. Patent Pub. No. 2017/0186882 to Koldiaev (“Koldiaev”)
SAMSUNG-1024	Reserved
SAMSUNG-1025	U.S. Patent No. 9,281,378 to Ching (“Ching”)
SAMSUNG-1026	U.S. Patent No. 6,894,357 to Guo (“Guo”)
SAMSUNG-1027	U.S. Patent No. 7,586,159 to Lee (“Lee”)
SAMSUNG-1028	U.S. Patent Pub. No. 2006/0220090 to Metz (“Metz”)
SAMSUNG-1029	U.S. Patent Pub. No. 2015/0200275 to Zhu (“Zhu”)
SAMSUNG-1030	U.S. Patent No. 8,637,931 to Basker (“Basker-931”)
SAMSUNG-1031	U.S. Patent No. 8,697,515 to Yin (“Yin”)
SAMSUNG-1032-1033	Reserved
SAMSUNG-1034	U.S. Patent No. 7,632,745 to Chen (“Chen-745”)
SAMSUNG-1035	U.S. Patent No. 9,246,003 to Cheng (“Cheng”)
SAMSUNG-1036	U.S. Patent No. 7,592,675 to Liaw (“Liaw”)
SAMSUNG-1037	U.S. Patent No. 9,214,529 to Chang (“Chang-529”)
SAMSUNG-1038	U.S. Patent Pub. No. 2011/0031552 to Iwamatsu

(“Iwamatsu”)

SAMSUNG-1039 U.S. Patent No. 9,461,143 to Pethe (“Pethe”)

SAMSUNG-1040 U.S. Patent No. 8,901,665 to Kelly (“Kelly”)

SAMSUNG-1041 U.S. Patent No. 6,720,619 to Chen (“Chen-619”)

SAMSUNG-1042-1049 Reserved

SAMSUNG-1050 *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. and Taiwan Semiconductor Manufacturing Company Limited and TSMC North America*, Complaint, ITC Inv. No. 337-TA-1336 (ITC) (“ITC Complaint”)

SAMSUNG-1051 ITC Complaint: Public Exhibit 12

SAMSUNG-1052 ITC Complaint: Public Exhibit 39

SAMSUNG-1053 ITC Complaint: Public Exhibit 45

SAMSUNG-1054 *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00352, E.D. Tex.

CLAIM LISTING

Limitation	Claim Language
[26pre]	An integrated circuit structure, comprising:
[26a]	a first fin comprising silicon, the first fin having a longest dimension along a first direction;
[26b]	a second fin comprising silicon, the second fin having a longest dimension along the first direction;
[26c]	an isolation material between the first fin and the second fin;
[26d]	a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;
[26e]	a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;
[26f]	a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and
[26g]	a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.
[27]	The integrated circuit structure of claim 26, wherein the gate edge isolation structure comprises silicon and nitrogen.
[28]	The integrated circuit structure of claim 26, wherein the dielectric material is in contact with the gate edge isolation structure.

Limitation	Claim Language
[29]	The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.
[30]	The integrated circuit structure of claim 29, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.
[31]	The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.
[32]	The integrated circuit structure of claim 26, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.
[33]	The integrated circuit structure of claim 32, further comprising: a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.
[34]	The integrated circuit structure of claim 33, wherein the local interconnect electrically couples the first gate structure to the second gate structure.
[35]	The integrated circuit structure of claim 33, further comprising: a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) petitions for IPR of claims 26-35 (“Challenged Claims”) of U.S. Patent No. 9,831,306 (“the ’306 Patent”).

II. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’306 Patent is available for IPR. Petitioner is not barred or estopped from requesting this review.

B. Challenge and Relief Requested

Petitioner requests IPR of the Challenged Claims on the below grounds.
SAMSUNG-1003, ¶¶1-197.

Ground	Claims	Basis
1	26-31	§103: Xie
2	26-31	§103: Xie and Tseng
3A	26-29, 31-32	§103: Anderson and Lin
3B	33-35	§103: Anderson, Lin, and Kawa

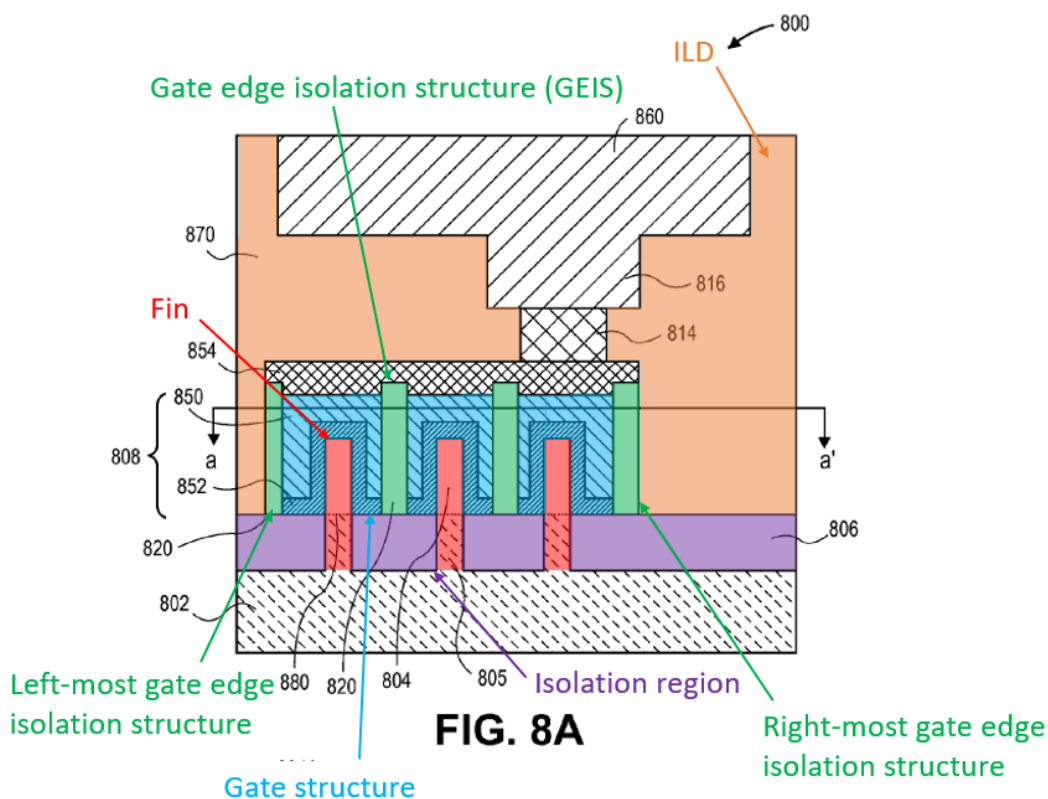
Each reference pre-dates December 19, 2013 (“Critical Date”), which is the earliest filed application from which the ’306 Patent claims priority. Petitioner does not take a position as to whether the ’306 Patent is entitled to the claimed priority date, but has applied references that pre-date the Critical Date and qualify as prior art, as shown below.

Reference	Date	Section
Xie	08/21/2013 (filed)	§102(a)(2)
Tseng	12/28/2012 (filed)	§102(a)(2)
Anderson	10/12/2010 (filed); 04/12/2012 (published)	§§102(a)(1), 102(a)(2)
Lin	04/19/2013 (filed)	§102(a)(2)
Kawa	07/29/2011 (filed) 01/31/2013 (published)	§§102(a)(1), 102(a)(2)

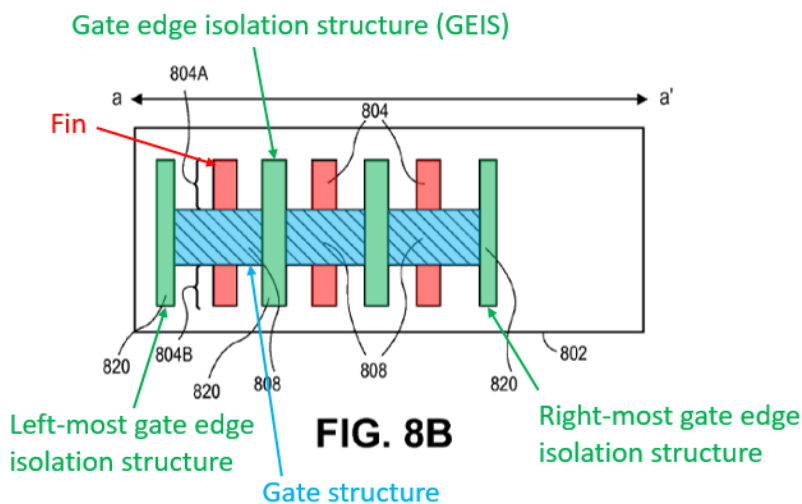
III. SUMMARY OF THE '306 PATENT

A. Brief Description

The '306 Patent describes “[s]elf-aligned gate edge and local interconnect structures.” SAMSUNG-1001, Abstract. An example of such a structure—a “non-planar semiconductor device having self-aligned gate isolation”—is shown in cross-section and plan view in FIGS. 8A-8B, *infra. Id.*, 9:27-30; SAMSUNG-1003, ¶21.



Excerpt from '306 Patent, FIG. 8A (annotated)



Excerpt from '306 Patent, FIG. 8B (annotated)

This semiconductor device includes “non-planar active regions (e.g., a fin structure[] including protruding fin portion 804 and sub-fin region 805) formed from substrate 802, and within isolation region 806.” SAMSUNG-1001, 9:34-37; *see* claim 26. The **fin structures** are highlighted in red and the **isolation region** in purple. “**Gate structures** 808,” blue, are “disposed over the **protruding portions** 804 of the non-planar active regions as well as over a portion of the **isolation region** 806.” SAMSUNG-1001, 9:37-39; *see* claim 26. “Gate structures 808 are separated by self-aligned **gate edge isolation structures** 820,” green. *Id.*, 9:43-44; *see* claim 26. SAMSUNG-1003, ¶22.

Interconnects and contacts are “disposed in **inter-layer dielectric stacks or layers** 870,” orange. SAMSUNG-1001, 9:45-49. As shown in FIG. 8A, the **inter-layer dielectric (ILD)** covers the **gate structures** and **gate edge isolation structures**, filling the space next to the exposed sidewalls of the right-most and left-most **gate edge isolation structures**.¹ SAMSUNG-1003, ¶23.

¹ FIG. 8B does not label the ILD. However, since FIG. 8B illustrates a top view through the a-a' cut in FIG. 8A, a POSITA would have understood that the ILD is present at least next to the left-most and right-most gate edge isolation structures of FIG. 8B. SAMSUNG-1003, ¶23.

B. Spatial Relationships of Elements of the Challenged Claims²

The Challenged Claims recite spatial relationships between features of an integrated circuit structure. The following paragraphs provide an overview of some of these features, with reference to FIGS. 8A and 8B, excerpted *infra*.

SAMSUNG-1003, ¶¶24-30.

The Challenged Claims recite that the fins (red) have “a longest dimension *along a first direction*,” illustrated *infra*. SAMSUNG-1001, claim 26. In doing so, the claims indicate the orientation of the fins, thus defining an orientation along the first direction. Based on the figures and read in light of the specification, a POSITA would have understood that the longest dimension of the fins extends from top to bottom in the top view (FIG. 8B), and correspondingly into the page in the cross-sectional view (FIG. 8A): this direction is the first direction. *See id.*, Abstract, 13:47-49, 14:4-8; SAMSUNG-1003, ¶25.

² This discussion is incorporated by reference into any portion of Grounds 1-3 where these terms are referenced.

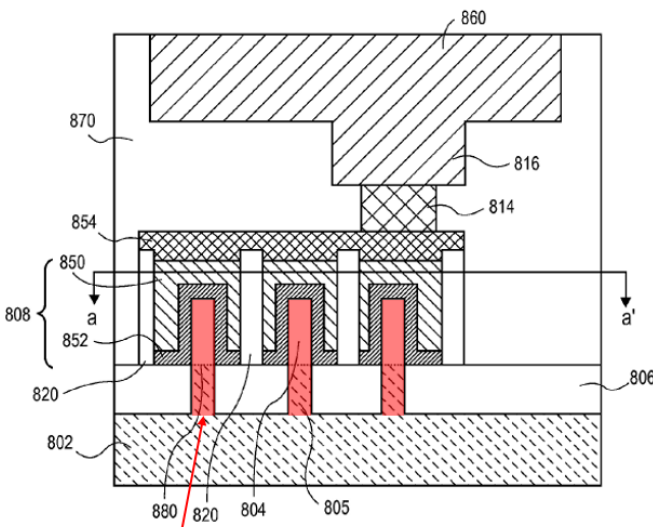


FIG. 8A

Fin
First Direction
Longest dimension of fins (into the page)

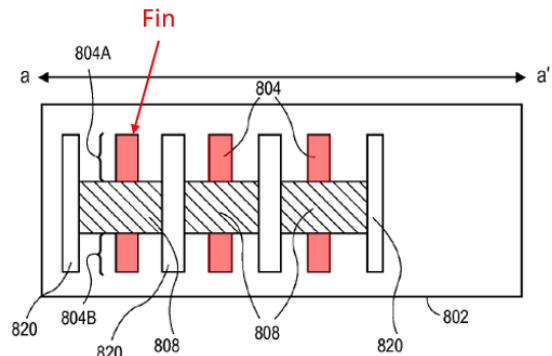
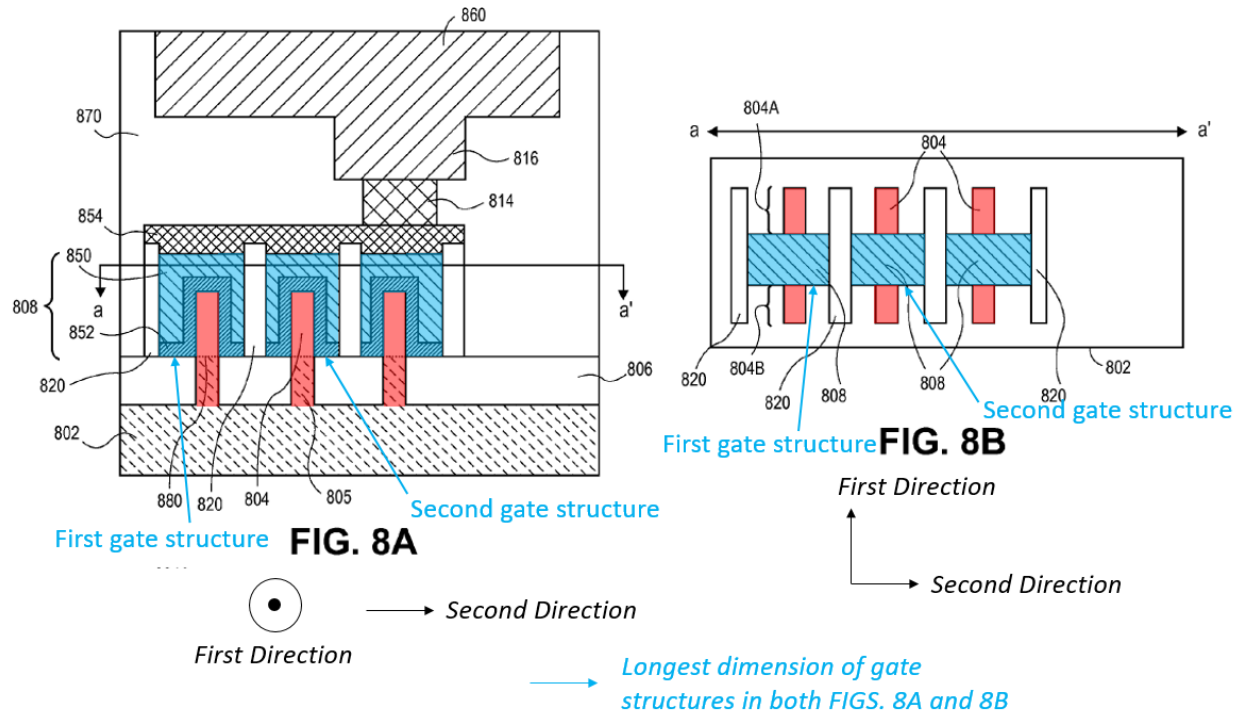


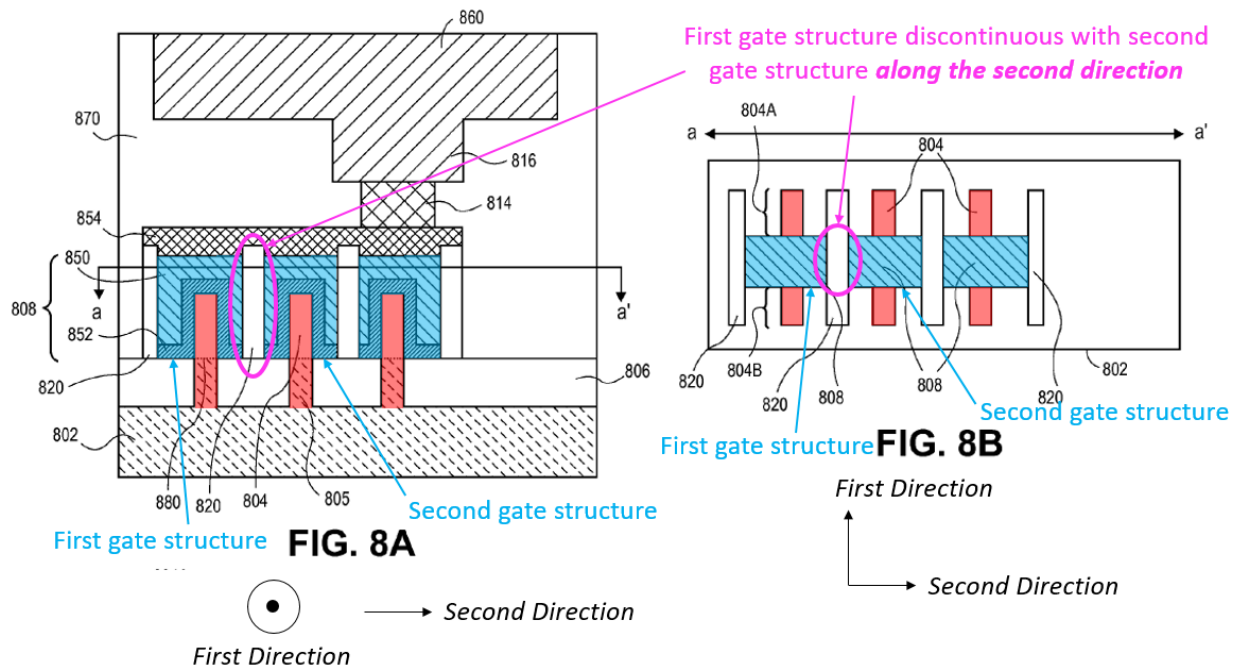
FIG. 8B

First Direction
Longest dimension of fins

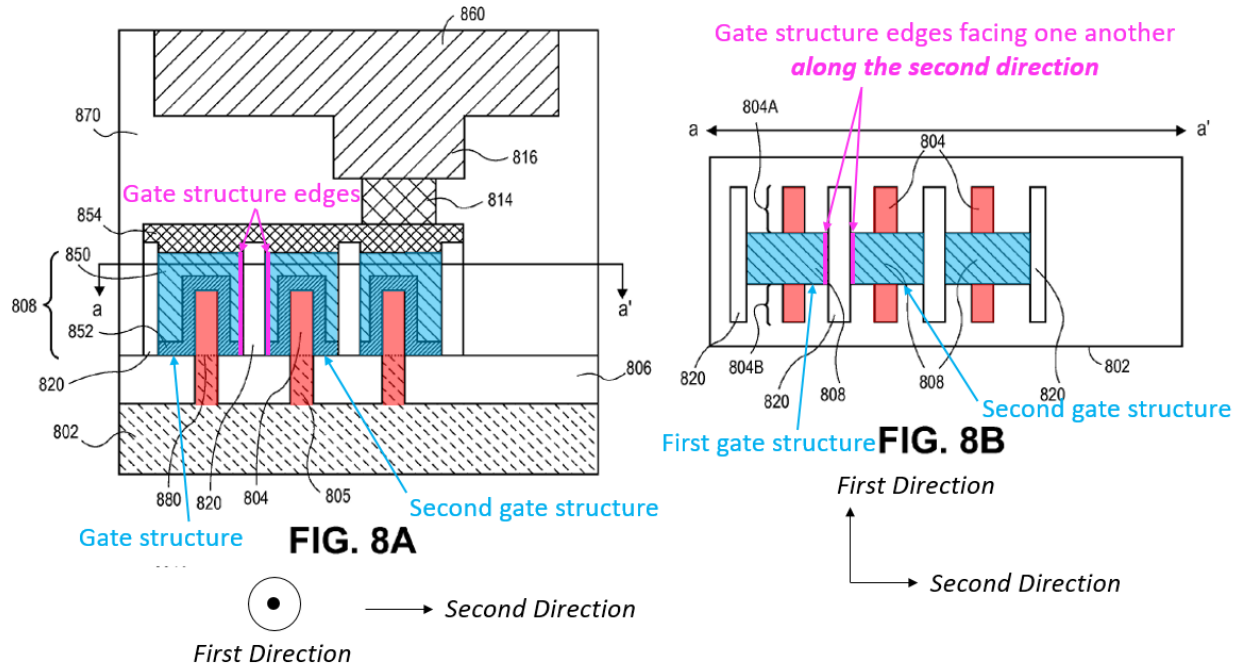
The Challenged Claims also recite that the gate structures have “a longest dimension *along a second direction* ... orthogonal to the first direction,” illustrated *infra*. SAMSUNG-1001, claim 26. The direction orthogonal to the length of the fins is the left-to-right direction in FIGS. 8A and 8B. A POSITA would have understood that this direction is the second direction, *e.g.*, given that the gate structure dimensions that appear to be longest are along this direction. *See id.*, Abstract, 13:49-52, 14:8-10; SAMSUNG-1003, ¶26.



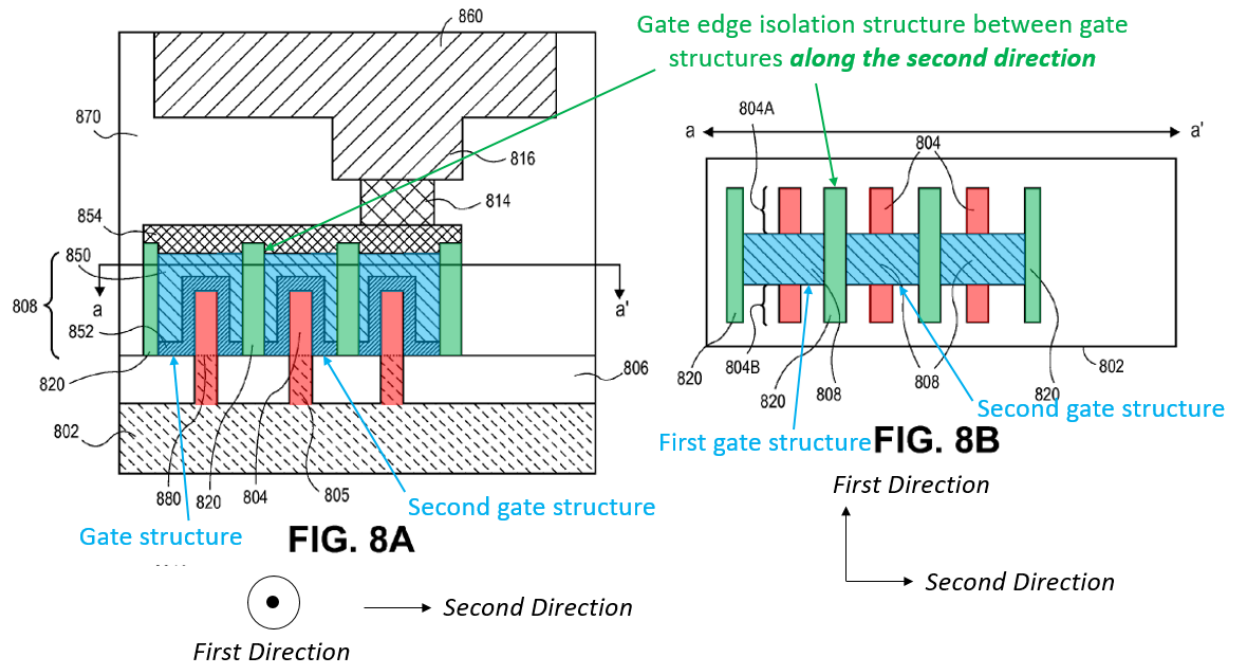
The Challenged Claims recite that a “second gate structure [is] discontinuous with [a] first gate structure *along the second direction*,” illustrated *infra*. SAMSUNG-1001, claim 26. This is revealed when viewing the structure starting from the first gate structure and *moving along the second direction* (left-to-right in both figures): a discontinuity exists (occupied by the gate edge isolation structure, discussed *infra*) before reaching the second gate structure. SAMSUNG-1003, ¶27.



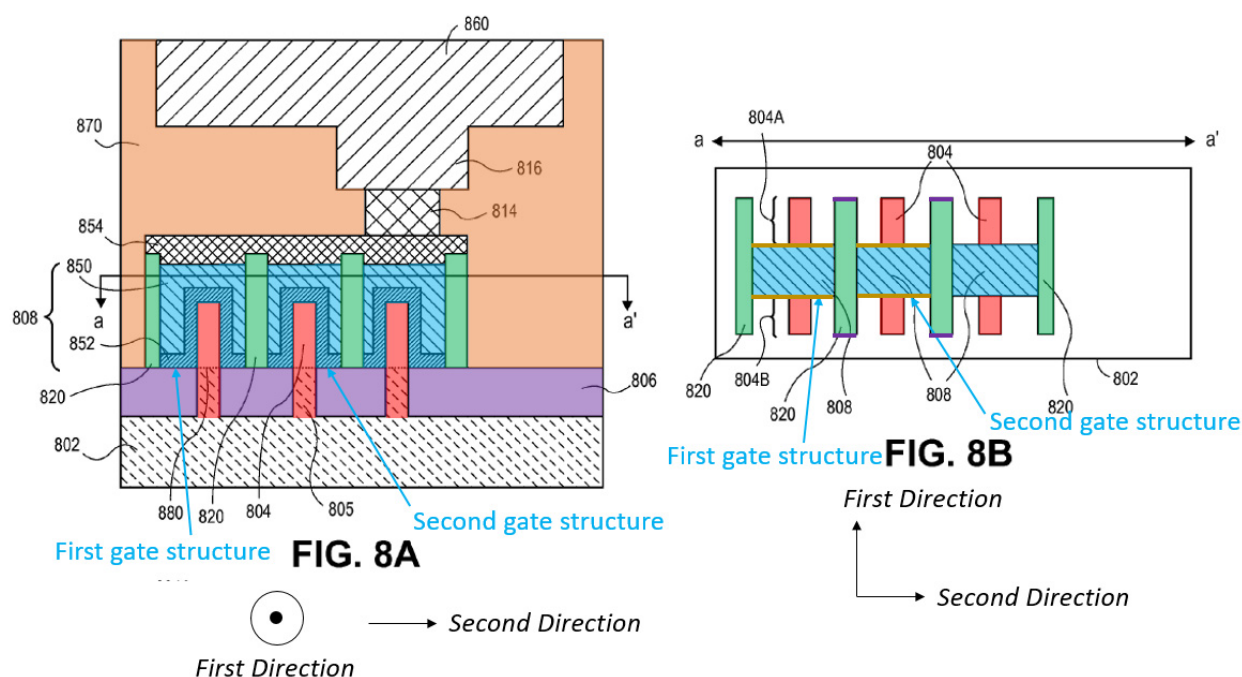
Similarly, the Challenged Claims recite that “an edge” of the second gate structure “fac[es] an edge of the first gate structure *along the second direction*,” illustrated *infra*. SAMSUNG-1001, claim 26. This too would have been understood by a POSITA when viewing the structure starting from the edge of the first gate structure (outlined in pink) and *moving along the second direction* to encounter the edge of the second gate structure (also in pink). SAMSUNG-1003, ¶28.



The gate edge isolation structure of the Challenged Claims is “between and in contact with the edge of the first gate structure and the edge of the second gate structure ***along the second direction***,” illustrated *infra*. SAMSUNG-1001, claim 26. Starting from the edge (pink) of the first gate structure (blue) and ***moving along the second direction***, one reaches first the gate edge isolation structure (green) and then the edge (pink) of the second gate structure (blue). SAMSUNG-1003, ¶29.



The Challenged Claims also recite that the “dielectric material [is] laterally adjacent to the first and second gate structures *along the first direction*” and “laterally adjacent to the gate edge isolation structure ... *along the first direction.*” SAMSUNG-1001, claim 26. For the purposes of this proceeding and without concession, Petitioner interprets these limitations consistent with the use of the phrase “along the second direction” (discussed *supra*). For instance, a dielectric material would be laterally adjacent to the gate structures (blue) *along the first direction* if it were at the sidewalls of the gate structures (outlined in brown in FIG. 8B, *infra*) and would be laterally adjacent to the gate edge isolation structure (green) *along the first direction* if it were at the short ends of the gate edge isolation structure (outlined in purple in FIG. 8B). SAMSUNG-1003, ¶30.



C. Prosecution History

The '306 Patent issued from U.S. Patent App. No. 15/024,750 (the '750 application). Claims 26-35 (corresponding to the Challenged Claims) were added by preliminary amendment. SAMSUNG-1002, 196-207. A first office action rejected some claims over Youn (US 2015/0056888); claims 26-35 were not addressed. *Id.*, 187-191. The applicant amended claim 1; no amendments were made to claims 26-35. *Id.*, 160-181. A Notice of Allowance was issued, with no reasons for allowance provided. *Id.*, 145-149.

D. Level of Ordinary Skill in the Art

A person of ordinary skill in the art relating to the subject matter of the '306 Patent as of the Critical Date (a “POSITA”) would have had a Master’s degree in

electrical engineering, physics, or a related field, and two years of work experience in integrated circuit design or manufacturing. SAMSUNG-1003, ¶¶19-20.

E. Claim Construction

Based on the prior art's description of the claimed elements being similar to that of the '306 Patent specification, no formal claim constructions are necessary in this proceeding because "claim terms need only be construed to the extent necessary to resolve the controversy." *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011).

Furthermore, Petitioner is not conceding that each challenged feature satisfies all statutory requirements such as 35 U.S.C. § 112. As this is an IPR petition, Petitioner is pursuing prior art-based grounds. Petitioner is not waiving any arguments concerning other grounds or claim scope.

IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. [GROUND 1] – CLAIMS 26-31 ARE OBVIOUS OVER XIE

The sections below provide a brief introduction to Xie.³

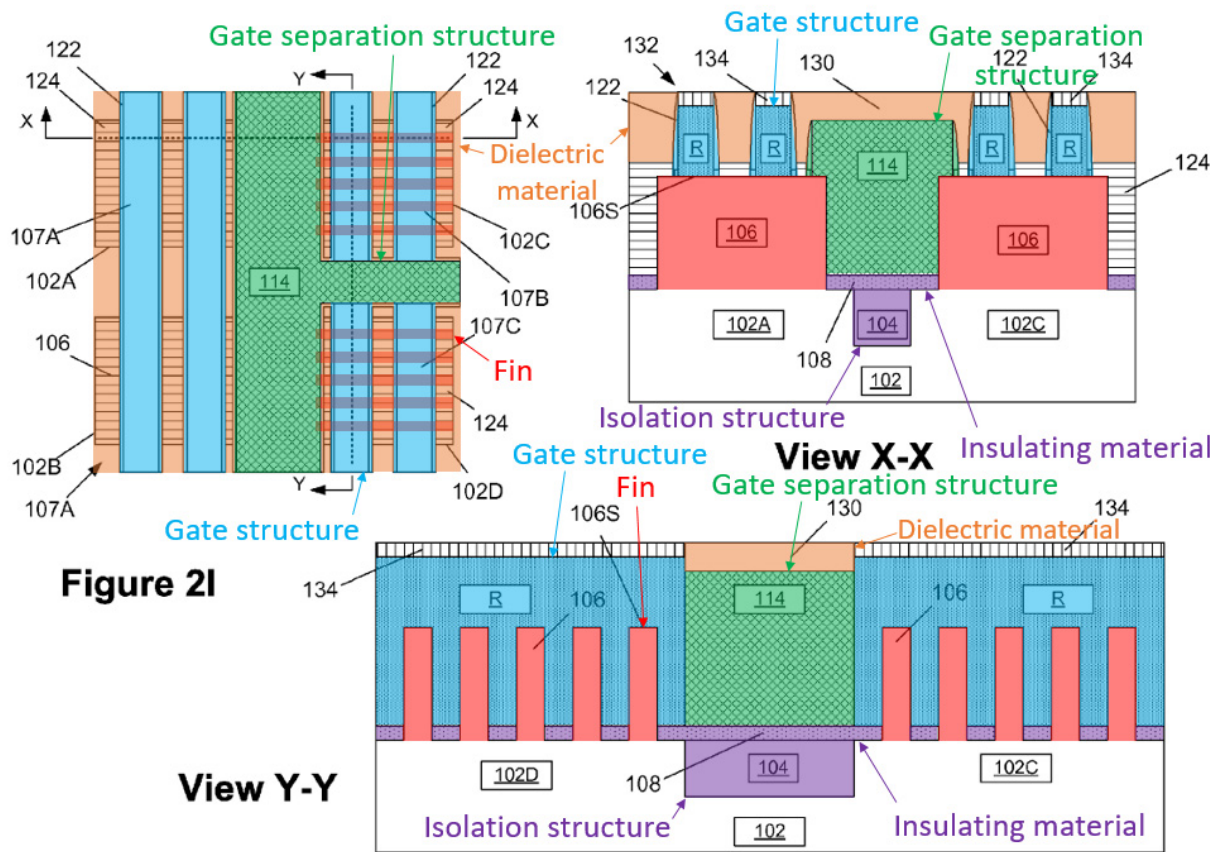
1. Xie describes FinFET devices having gate separation structures

Xie describes "methods ... for forming gate structures for FinFET devices." SAMSUNG-1004, [0027]. One such FinFET structure, illustrated in FIG. 2I, *infra*,

³ Petitioner incorporates this discussion into Grounds 1-2.

includes a substrate 102 having “active regions 102A-D” defined by “isolation structures 104,” purple. SAMSUNG-1004, [0028]. “[A] plurality of fins 106,” some of which are highlighted in red, are formed in the substrate.⁴ *Id.* The fins extend left to right in the top and X-X cross-sectional views, and into the page in the Y-Y cross-sectional view. *See id.*, [0027]. An insulating material 108, purple, “remains in the bottom of the trenches” between the fins “so as to locally isolate the fins 106 from one another.” *Id.*, [0028]; SAMSUNG-1003, ¶31.

⁴ The fins 106 are obscured by the epi semiconductor layer 124 in the top view. SAMSUNG-1004, [0035]. The exposed fins 106 can be seen, *e.g.*, in FIG. 2A. SAMSUNG-1003, ¶32.



Excerpt from Xie, FIG. 2I (annotated)

Gate structures, blue, cover the fins. *See* SAMSUNG-1004, [0016]-[0018], [0038]. Each gate structures is “a stack of material layers” that “may be formed using either gate-first or gate-last techniques.” *Id.*, [0017], [0030]; *see* claims 4-5; SAMSUNG-1003, ¶33.

A “gate separation structure 114,” green, is “positioned between the first and second spaced-apart gate structures.” SAMSUNG-1004, [0017], [0032]. A “layer of insulating material 130,” orange, is “blanket-deposited” onto the structure. SAMSUNG-1004, [0036]; *see* FIG. 2I; SAMSUNG-1003, ¶34.

2. A POSITA would have understood or found obvious that Xie's gate structures each includes a gate dielectric layer and a gate electrode

Xie's gate structures include "a stack of material layers" including "a high-k (k value greater than 10) gate insulation layer," "one or more metal layers," and "a bulk conductive metal layer." SAMSUNG-1004, [0038], claim 1; *see* claim 5, [0015]-[0016], [0040]; SAMSUNG-1003, ¶35. To the extent Xie does not explicitly disclose gate structures each having a gate dielectric layer and a gate electrode, a POSITA would have found this configuration obvious, as discussed in the following paragraphs. SAMSUNG-1003, ¶¶35-42.

It was well-known for a gate structure in a FinFET device to include a gate dielectric layer (*e.g.*, a high-k gate dielectric layer) and a gate electrode (*e.g.*, a metal gate electrode). *See, e.g.*, SAMSUNG-1005, 8:67-9:4 ("the gate-last process comprises ... fill[ing] the trench with ***a gate dielectric layer and a conductive gate electrode layer***"), 5:5-46, FIGS. 2 and 5A; SAMSUNG-1025, 4:39-5:3, Fig. 9A; SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1012, 4:46-48; SAMSUNG-1013, 3:45-46; SAMSUNG-1014, 7:8-22; SAMSUNG-1015, [0041], [0046]-[0047]; SAMSUNG-1003, ¶36.

In view of the state of the art and given Xie's description of the composition of its gate structures (*see* SAMSUNG-1004, [0038], [0015]-[0016], [0040], claims 1 and 5), a POSITA would have understood or found obvious that the "stack of

material layers” of Xie’s gate structures includes a gate dielectric layer (*e.g.*, Xie’s high-k gate insulation layer) and a gate electrode (*e.g.*, Xie’s bulk conductive metal layer). SAMSUNG-1004, [0038]; SAMSUNG-1003, ¶37.

A POSITA would have been motivated to implement Xie’s “high-k ... gate insulation layer” and “bulk conductive metal layer” as a high-k gate dielectric layer and metal gate electrode, respectively, for at least the following reasons.

SAMSUNG-1003, ¶¶38-42.

First, gate structures having high-k gate dielectric layers and metal gate electrodes were standard elements of FinFET transistors. *See, e.g.*, SAMSUNG-1005, 5:5-46; SAMSUNG-1025, 4:39-5:3; SAMSUNG-1011, 3:59-4:10; *see* SAMSUNG-1001, 3:49-4:49 (acknowledging that “a conventional finFET or tri-gate process fabrication scheme” makes use of gate electrodes and gate dielectric layers); SAMSUNG-1003, ¶39. The implementation of Xie’s gate insulation layer and bulk conductive material layer as a gate dielectric layer and gate electrode, respectively, is thus merely a comprehensive implementation of a structure already described by Xie. SAMSUNG-1003, ¶39.

Second, a POSITA would have been motivated to use a high-k gate dielectric layer and a metal gate electrode to obtain the performance advantages afforded by use of these materials, such as decreased threshold voltage, reduced fringe capacitance, and suppressed leakage current. *See* SAMSUNG-1011, 1:32-

35 (“There has been a desire to replace the gate oxide and polysilicon gate electrode with a high-k gate dielectric and metal gate electrode *to improve device performance as feature sizes continue to decrease.*”); SAMSUNG-1028, Abstract; SAMSUNG-1026, Abstract; SAMSUNG-1027, 1:38-46; SAMSUNG-1003, ¶40. Moreover, the use of a high-k gate dielectric layer provides the gate with finer control over the channel potential, enabling more effective on/off control, thus facilitating higher speed performance. *See* SAMSUNG-1028, Abstract; SAMSUNG-1003, ¶40.

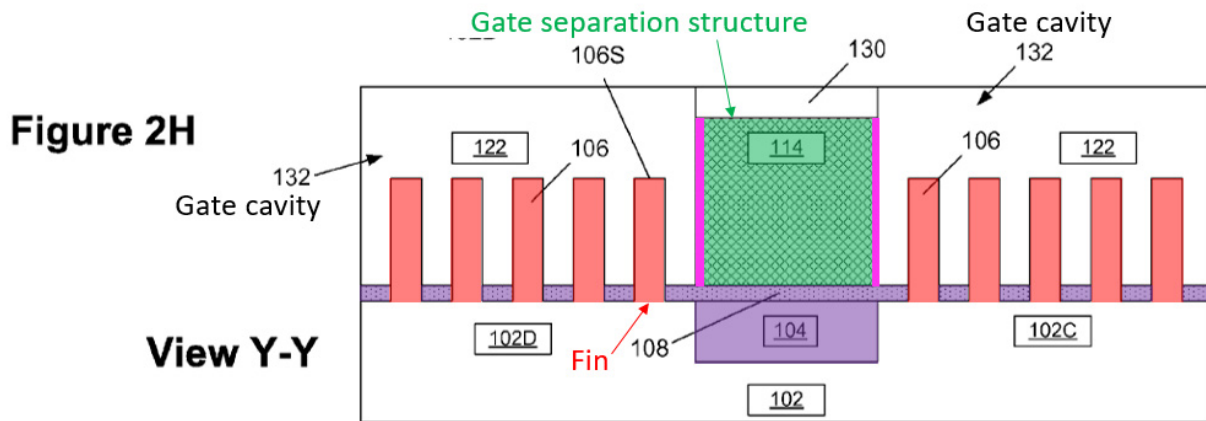
Third, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, high-k gate dielectric layers and metal gate electrodes) to a known structure (*e.g.*, Xie’s FinFET gate structure) to yield predictable results (*e.g.*, a gate structure having a high-k gate dielectric layer and a metal gate electrode). SAMSUNG-1003, ¶41; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (a supposed invention that “simply arranges old elements with each performing the same function it had been known to perform” is obvious).

A POSITA would have expected success because high-k gate dielectric layers and metal gate electrodes are consistent with the composition of Xie’s gate structures. *See* SAMSUNG-1004, [0038]; SAMSUNG-1003, ¶42. A POSITA also would have expected success because high-k gate dielectric layers and metal

gate electrodes are well-known elements of FinFET gate structures. *See* SAMSUNG-1005, 5:5-46, 8:67-9:4, FIG. 5A; SAMSUNG-1025, 4:39-5:3, FIG. 9A; SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1012, 4:46-54; SAMSUNG-1013, 3:45-46; SAMSUNG-1014, 7:8-22; SAMSUNG-1015, [0041], [0046]-[0047]; SAMSUNG-1003, ¶42.

3. Structure of Xie's gate structures when formed by a gate-last process

Xie's gate structures can be "replacement gate structure[s]." SAMSUNG-1004, [0038]; *see* [0030]. Replacement gate structures are formed by removing a sacrificial gate structure "to define a gate cavity 132 where the final gate structure ... will be formed." SAMSUNG-1004, [0034]-[0038], FIGS. 2E-2H. At least one end of the gate cavity 132 is defined by the sidewalls (outlined in pink) of Xie's gate separation structure 114. *See id.*, FIG. 2H, *infra*. A "replacement gate structure" is "formed in the gate cavities." *Id.*, [0038], FIG. 2I-2H; SAMSUNG-1003, ¶43.



Excerpt from Xie, FIG. 2H (annotated)

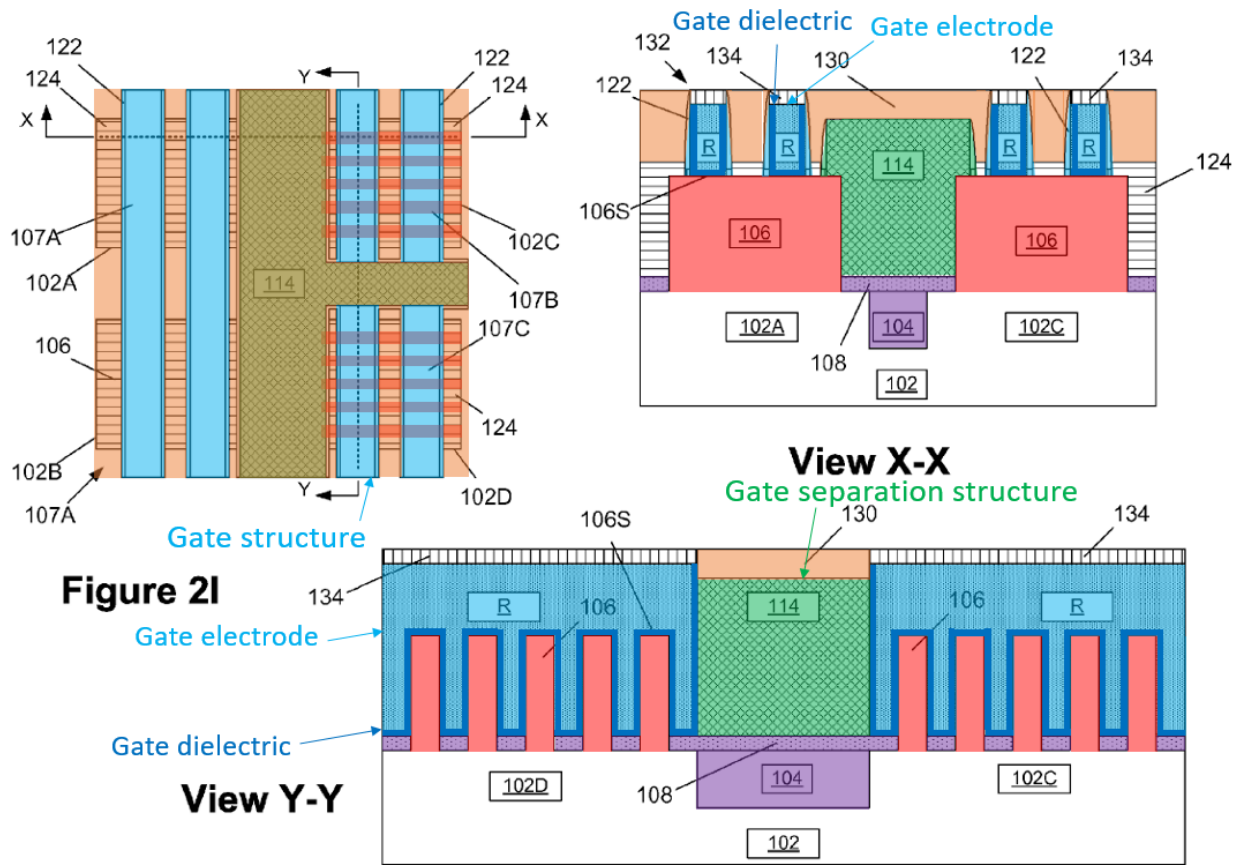
Given the implementation of Xie's gate structures to include a gate dielectric layer and a gate electrode (*see* §IV.A.2), a POSITA would have understood or found obvious that "forming the replacement gate structure" involves depositing first the gate dielectric layer and then the gate electrode into the gate cavity. SAMSUNG-1004, [0038], FIG. 2I; *see* SAMSUNG-1025, 4:39-5:56 ("First, gate dielectric layer 50 is formed in recess 44 ... and on the top surfaces and sidewalls of semiconductor fins 48. ... Next, conductive material 52 is formed over gate dielectric layer 50"), FIG. 8A); SAMSUNG-1005, 8:62-9:4; SAMSUNG-1015, [0045]-[0047]; SAMSUNG-1012, 11:4-14; SAMSUNG-1014, 7:8-42; SAMSUNG-1003, ¶44. Depositing the gate dielectric layer into the gate cavity coats the gate dielectric layer onto the fins and onto the sidewalls (pink) of the gate separation structure. *See* SAMSUNG-1025, 4:39-5:56; SAMSUNG-1040, 6:33-38, FIGS. 7A-7B (showing the gate dielectric layer 704 coating onto exposed

sidewalls of an opening formed by removing a dummy gate structure);

SAMSUNG-1036, [0023], FIG. 1F; SAMSUNG-1003, ¶¶44-45.

An example of a replacement gate structure is shown in the composite figure *infra*.⁵ The gate dielectric layer (dark blue) coats the fins (red) and on the sidewalls of the gate separation structure (green), and the gate electrode (light blue) is disposed on the gate dielectric layer. SAMSUNG-1003, ¶45.

⁵ This figure, as well as other composite figures herein, is just one example combination that a POSITA would have found obvious, and is provided for illustrative purposes only. Other, similar example configurations also would have been obvious and would render the challenged claims obvious for similar reasons as those discussed herein. SAMSUNG-1003, ¶46.



Xie composite figure – Replacement gate structure

4. Structure of Xie’s gate structures when formed by a gate-first process

Alternatively, Xie’s gate structure is “a stack of material layers” formed using “gate-first ... techniques.” SAMSUNG-1004, [0030], claim 1; *see* [0039]-[0040], claim 5. SAMSUNG-1003, ¶47.

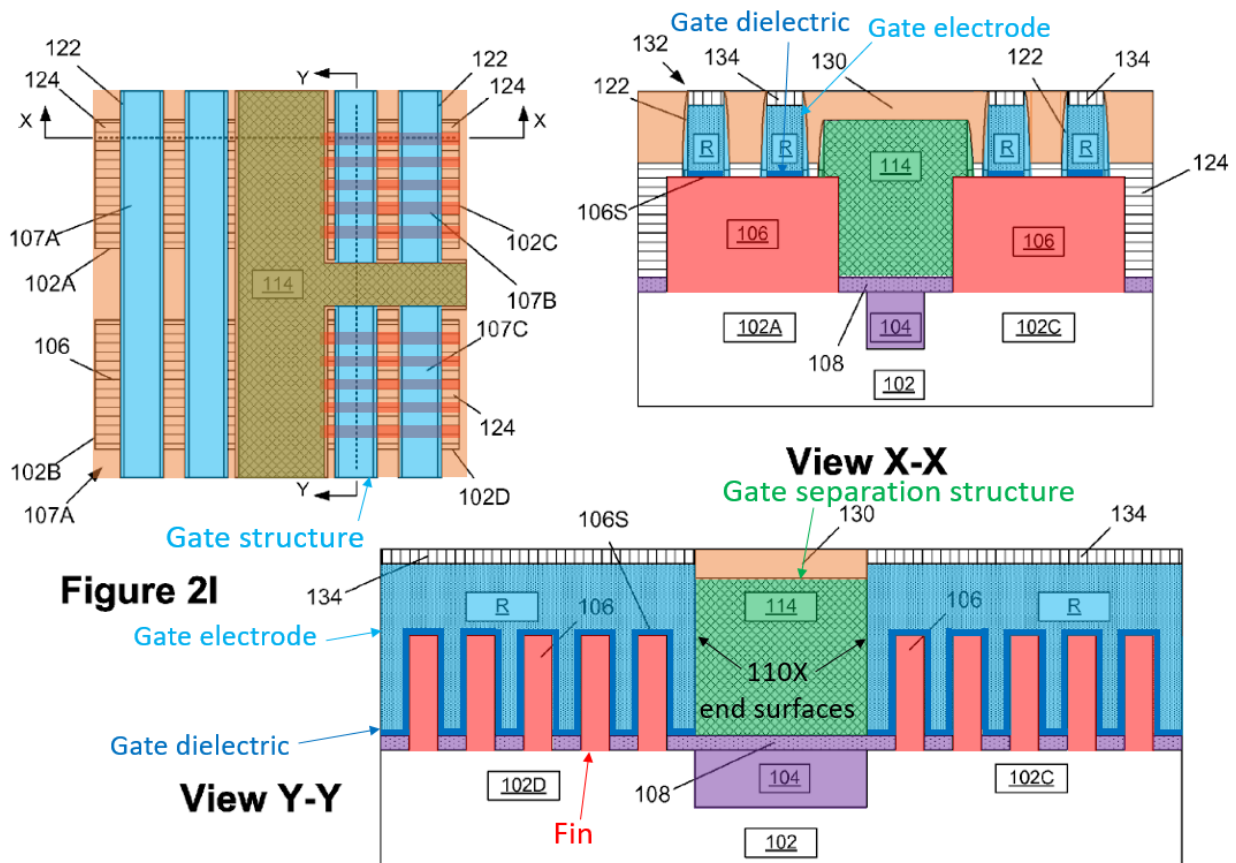
A gate-first fabrication process is similar to the process of forming sacrificial gate structures 107: “the stack of materials ... that will comprise the gate structure” “are blanket-deposited across all of the active regions.” SAMSUNG-1004, [0040]; *see* [0030]-[0035], FIGS. 2B-2F; SAMSUNG-1003, ¶48. Given that Xie’s gate

structures include a gate dielectric layer and a gate electrode (*see* §IV.A.2), a POSITA would have understood or found obvious depositing this stack of materials involves depositing first the gate dielectric layer and then the gate electrode. *See* SAMSUNG-1005, 5:12-14 (a “gate dielectric layer 212 and gate electrode layer 214 are sequentially deposited over the substrate”), 8:59-60; *see* SAMSUNG-1017, 4:7-35; SAMSUNG-1016, 11:37-12:20, 22:7-8; SAMSUNG-1003, ¶49. The gate stack then is etched “to form ... trenches 112 through the stack of materials,” thus “defin[ing] what will become the end surfaces 110X of the gate structures” and exposing both the gate dielectric layer and the gate electrode at these end surfaces. SAMSUNG-1004, [0040], FIG. 2C; *see* SAMSUNG-1005, 5:47-55, FIG. 5A; SAMSUNG-1016, FIG. 13 (showing gate dielectric 301 and gate conductor 302 exposed at the end of gate structure 300 fabricated “using a gate first process,” 22:7-8; *see* 19:41-20:16); SAMSUNG-1017, FIG. 2; SAMSUNG-1003, ¶50. The “gate separation structure 114” is “formed in the spaced apart trenches,” between the end surfaces 110X of the gate structures, and thus contacts the exposed gate dielectric layer and the gate electrode at these end surfaces. SAMSUNG-1004, [0040], FIG. 2D; SAMSUNG-1003, ¶51.

An example of a gate-first gate structure is shown in the composite figure *infra*. SAMSUNG-1003, ¶52. The gate dielectric layer (dark blue) and the gate electrode (light blue) are exposed at the gate structure end surfaces 110X. The gate

separation structure contacts these end surfaces, as shown in the Y-Y view.

SAMSUNG-1003, ¶52.



Xie composite figure – Gate-first gate structure

Although Xie’s description of the replacement gate process is more extensive than its description of the gate-first process, Xie can be relied on for its disclosure of both processes. *See Merck & Co v. Biocraft Labs.*, 874 F.2d 804, 807 (Fed. Cir. 1989) (holding that a reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill in the art, including non-preferred embodiments); *In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004) (“The

prior art's mere disclosure of more than one alternative does not constitute a teaching away from any ... alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed").

5. Analysis

(1) Claim 26

Limitation [26pre]

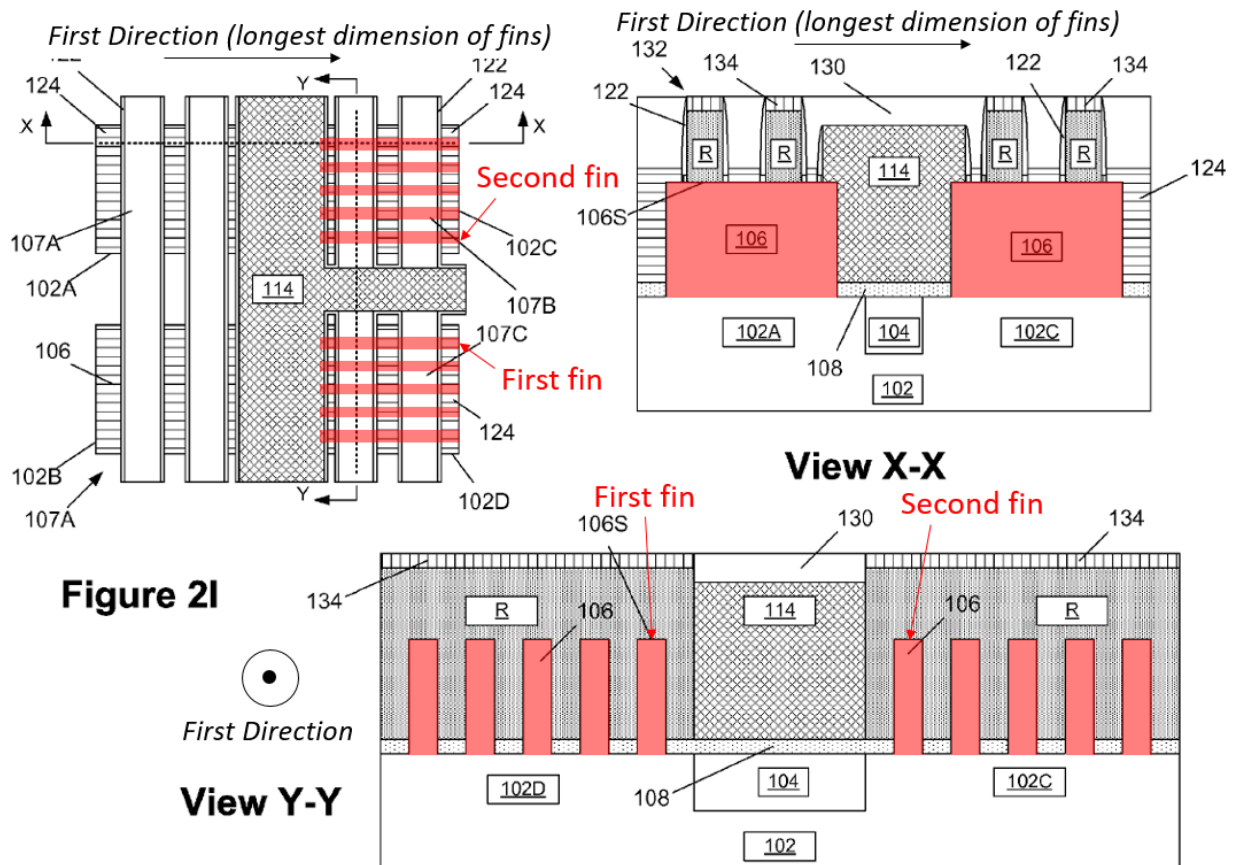
To the extent the preamble is deemed to be limiting, Xie renders it obvious. Xie describes an integrated circuit structure. *See* SAMSUNG-1004, [0002] ("The present disclosure generally relates to ... methods of forming *gate structures for FinFET devices and the resulting semiconductor devices.*"), [0026]-[0027], [0039], [0015]; SAMSUNG-1003, ¶53.

Limitations [26a] and [26b]

Xie renders obvious **first and second fins**, *e.g.*, Xie's fins 106, some of which are highlighted in red in FIG. 2I, *infra*.⁶ *See* SAMSUNG-1004, [0040]

⁶ The X-X view depicts fins other than those specifically identified here as the first and second fins. A POSITA would have understood that a cross-section taken through the identified first fin or the second fin, in a plane parallel to the X-X plane marked in FIG. 2I, would be substantially the same as the illustrated X-X view. SAMSUNG -1003, ¶54.

(“The active regions and *the fins 106* are depicted in dashed lines in FIGS. 2K-2N”), [0016]-[0018], [0027]-[0029]; claims 9, 11, 1; Figs. 2A-2O; SAMSUNG-1003, ¶54.



Excerpt from Xie, FIG. 2I (annotated)

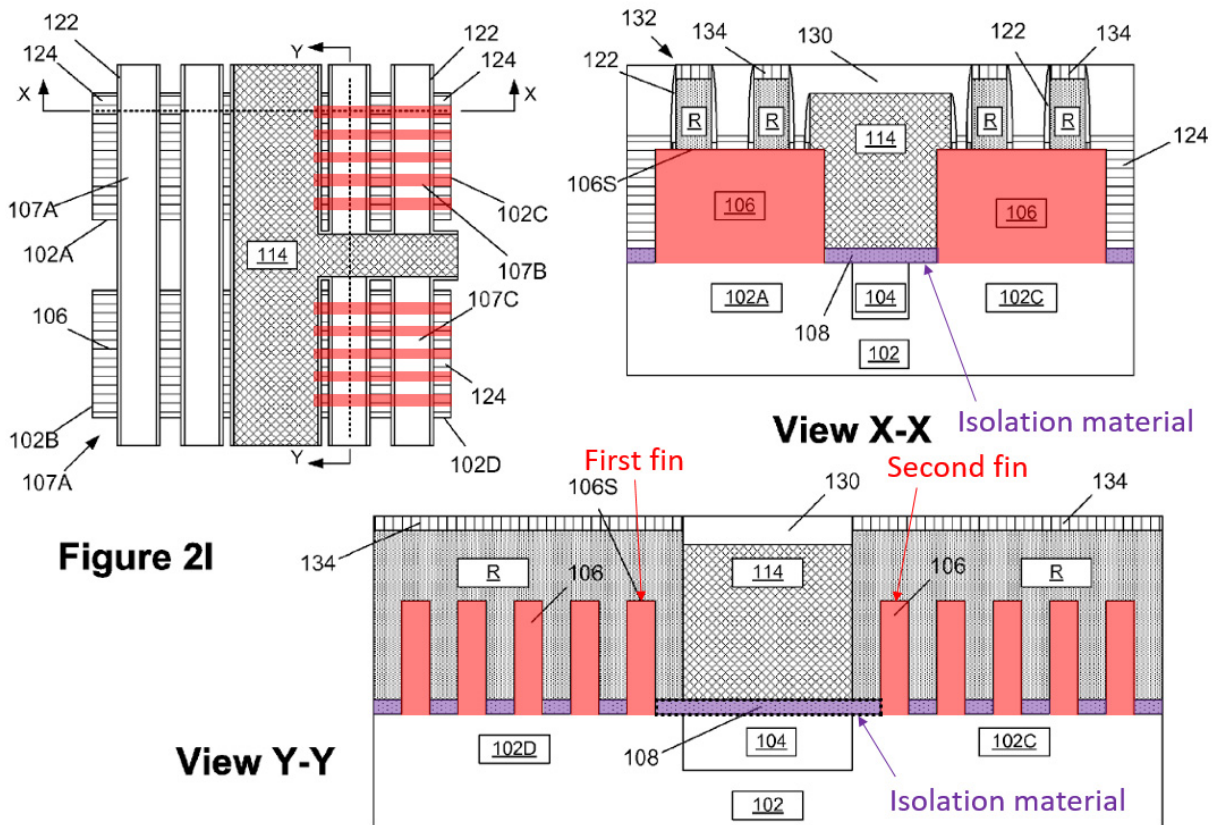
Each fin has a **longest dimension along a first direction**, marked in FIG. 2I. See SAMSUNG-1004, [0027] (“the view ‘Y-Y’ is a cross-section view that is taken transverse to *the long axis of the fins 106*.”). This longest dimension is **along the first direction**: the longest dimension of the fins is traversed *as one*

moves along the fins in the first direction, e.g., left to right in the top and X-X views, into the page in the Y-Y view. SAMSUNG-1003, ¶55.

Xie renders obvious that **the first and second fins comprise silicon**, e.g., as evidenced by Xie’s fabrication process. Xie’s integrated circuit is formed on a “bulk silicon” substrate. SAMSUNG-1004, [0037]. “[A] plurality of trenches 105 were formed in the substrate 102 to thereby define a plurality of fins 106.” SAMSUNG-1004, [0028], FIG. 2A. That is, the fins are formed from and thus have the same composition as the silicon substrate, *i.e.*, the fins include silicon. SAMSUNG-1003, ¶56.

Limitation [26c]

Xie renders obvious **an isolation material**, e.g., Xie’s isolation material 108, purple in FIG. 2I, *infra*. See SAMSUNG-1004, [0039] (“FIG. 2J depicts the device at a point in fabrication where the fins 106 and the *local isolation material* 108 have been formed.”), [0028], FIGS. 2A-2J. The isolation material 108 is **an isolation material** at least because it “locally isolate[s] the fins 106 from one another.” *Id.*, [0028]; SAMSUNG-1003, ¶57.

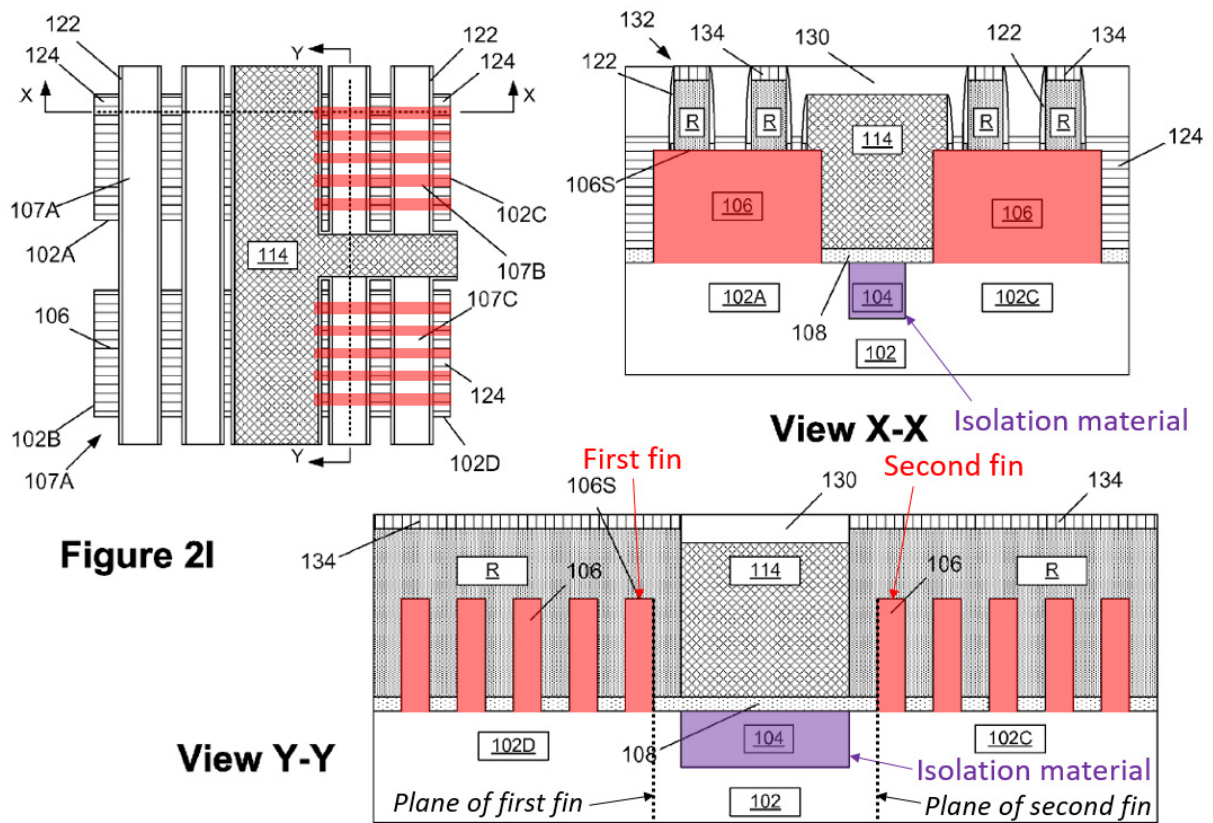


Excerpt from Xie, FIG. 2I (annotated)

Xie's **isolation material 108** is **between the first fin and the second fin**, as illustrated *supra*. At least the portion of the isolation material 108 that is outlined in dashed lines in the Y-Y view *supra* is **between the first and second fins** because it is disposed in the space separating the two fins. See SAMSUNG-1004, [0028], FIG. 2A; SAMSUNG-1003, ¶58.

Alternatively or additionally, Xie renders obvious **an isolation material**, e.g., Xie's isolation structure 104, purple in Xie's FIG. 2I, *infra*. See SAMSUNG-1004, [0028] ("a plurality of active regions 102A-D were defined in the substrate

102 by the formation of *isolation structures 104*"), [0039], FIGS. 2A-2I. The isolation structure is **isolation material** because it separates (*e.g.*, isolates) active regions. SAMSUNG-1003, ¶59.



Excerpt from Xie, FIG. 2I (annotated)

The isolation material, *e.g.*, Xie's isolation structure 104, is **between the first fin and the second fin**, as illustrated *supra*. The isolation structure 104 is between the first and second fins because it is disposed in the space separating the fins, *e.g.*, in the space separating a vertical plane defined by the first fin and a

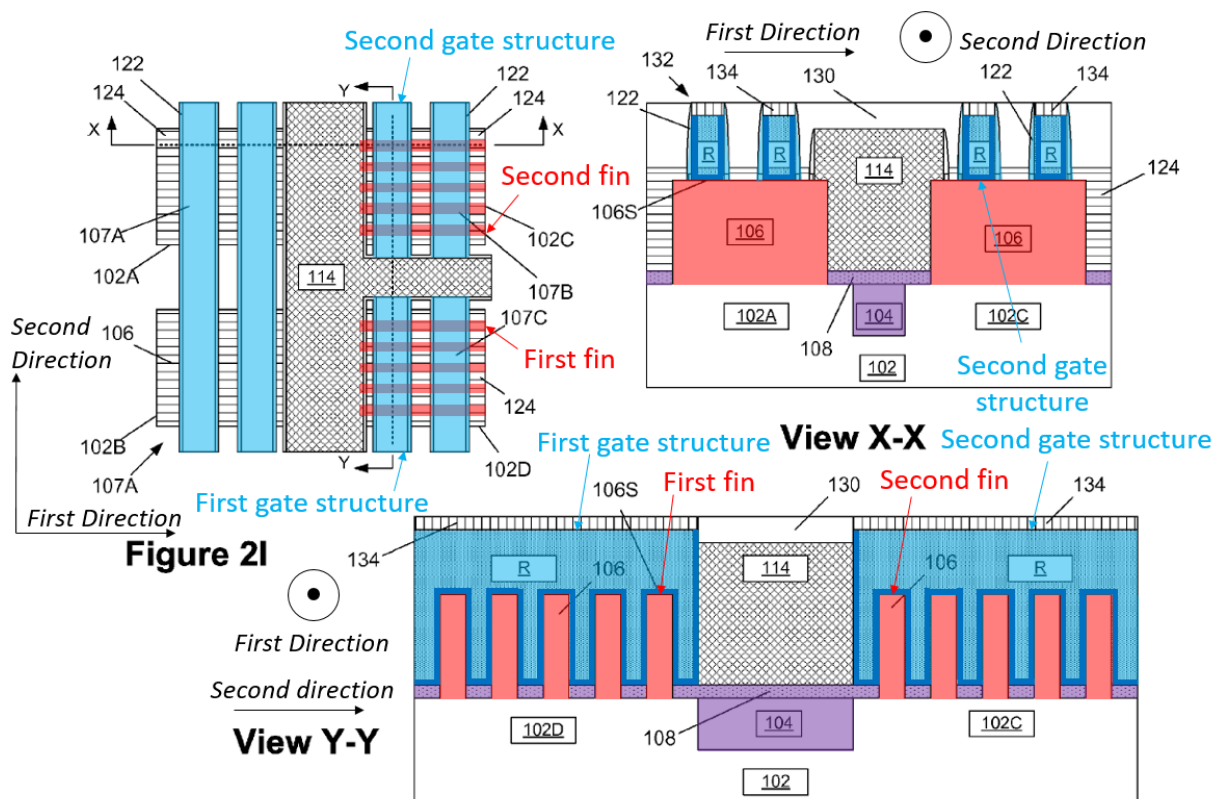
vertical plane defined by the second fin (denoted in dashed lines in the Y-Y view *supra*). SAMSUNG-1003, ¶60.

Limitations [26d] and [26e]

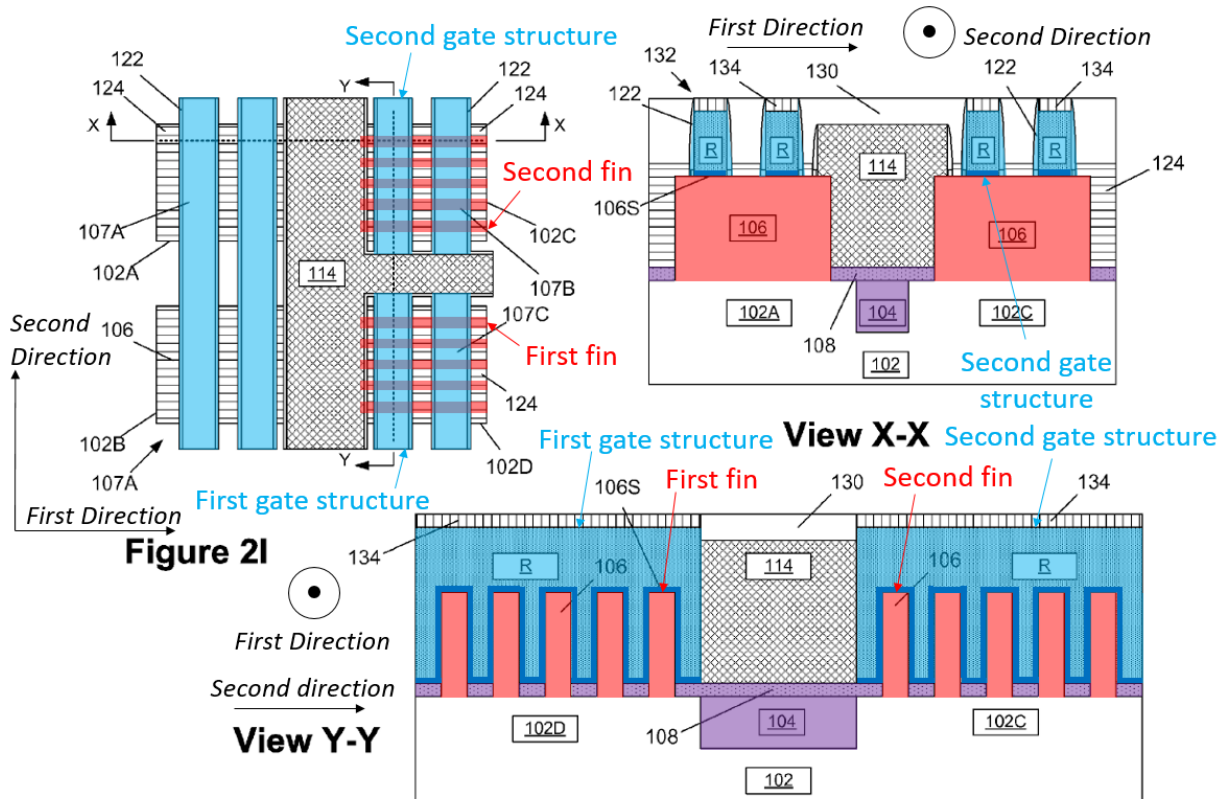
Xie renders obvious first and second gate structures

Xie renders obvious **first and second gate structures**, *e.g.*, Xie’s “**final gate structures**,” blue in the two composite figures *infra*. SAMSUNG-1004, [0030]; *see* [0017] (“**first and second spaced-apart gate structures**”). SAMSUNG-1003, ¶61.

The gate structures (*e.g.*, Xie’s “final gate structures”) “may be formed using either gate-first or gate-last techniques.” SAMSUNG-1004, [0030]. The first composite figure *infra* illustrates a “replacement gate structure” (SAMSUNG-1004, [0038]); the second composite figure illustrates a gate structure made by a gate-first process. SAMSUNG-1003, ¶62; *see* SAMSUNG-1004, [0040] (“the stack of materials 140S that will comprise **the gate structure 140** (be it a final gate structure or a sacrificial gate structure) are blanket-deposited”), claims 1 and 5, [0002], [0013]-[0016], [0027], [0041], FIG. 2I, FIGS. 2K-2O, claims 9, 11, and 16; SAMSUNG-1003, ¶62.

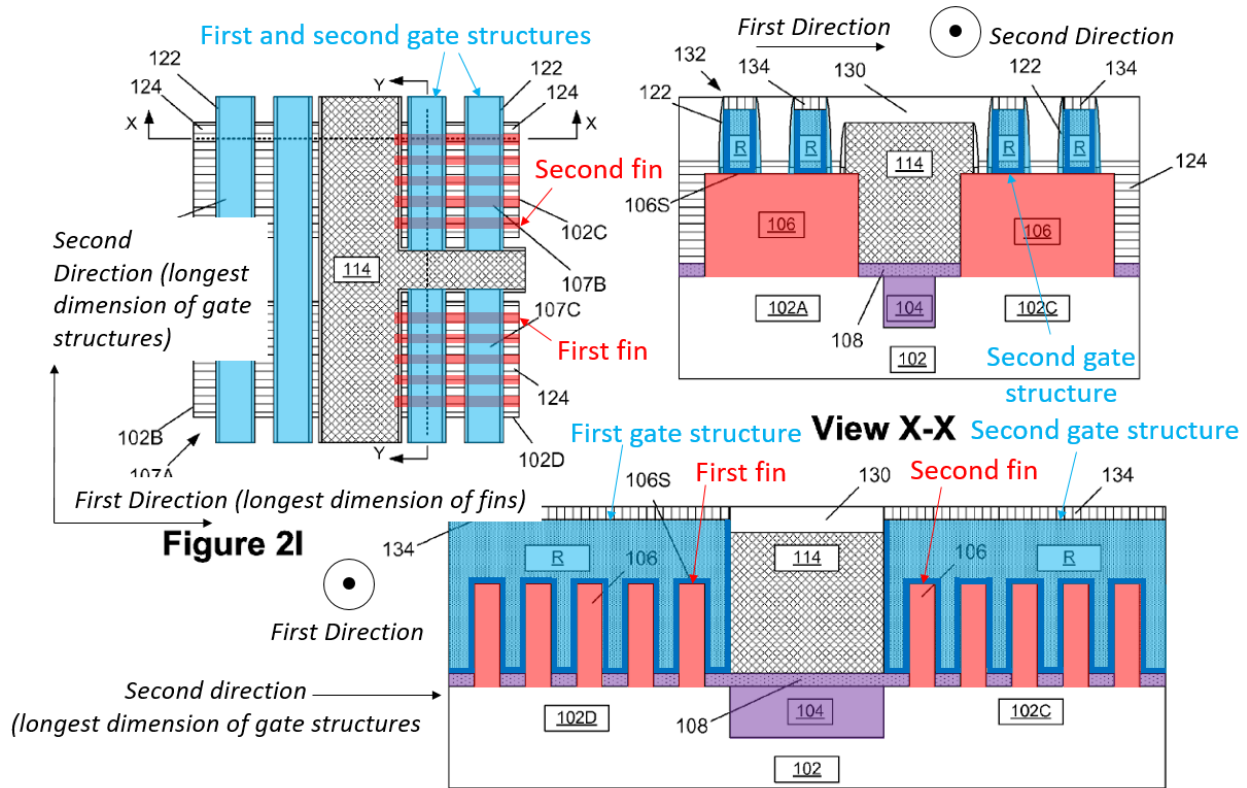


Xie composite figure – Replacement gate structure



Xie composite figure – Gate-first gate structure

As illustrated, the gate structures have a **longest dimension along a second direction**: the longest dimension of the gate structures is traversed *as one moves along the gate structures in the second direction* (top to bottom in the top view, left to right in the Y-Y view, into the page in the X-X view; *see infra*). See SAMSUNG-1004, FIG. 2I; SAMSUNG-1003, ¶63.



Xie composite figure⁷

The figures illustrate that **the second direction is orthogonal to the first direction**, *e.g.*, the gate structures extend orthogonal to the extension of the fins.

⁷ The applicability of Xie's gate-first implementation to the features of the Challenged Claims is identical to the applicability of the replacement gate implementation, except where stated otherwise. Where the applicability is identical, only the replacement gate implementation is discussed explicitly. However, Xie's gate-first implementation renders these features obvious for at least similar reasons. SAMSUNG -1003, ¶67.

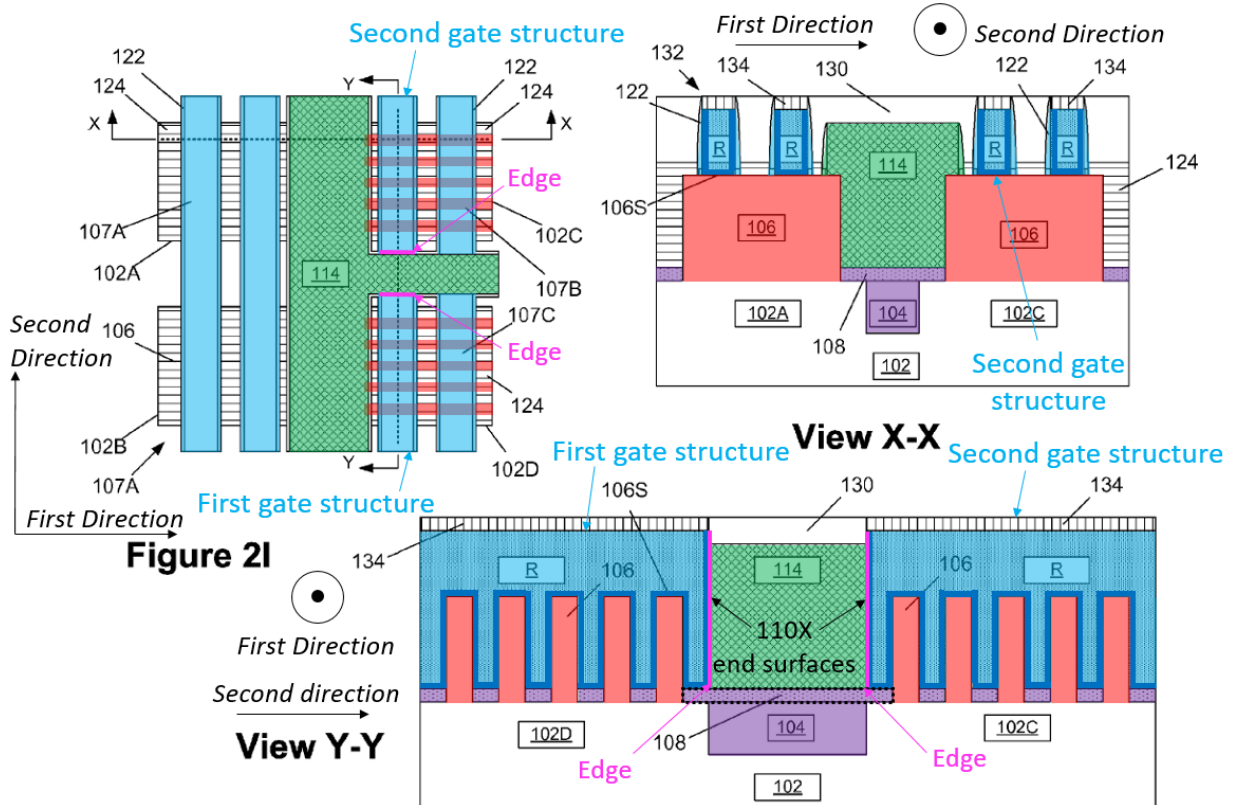
See SAMSUNG-1004, FIG. 2I; SAMSUNG-1003, ¶64. To the extent that Xie does not explicitly state this orthogonality, a POSITA would have understood this to be the case, or otherwise found this to be obvious, consistent with FIG. 2I and given that gate structures orthogonal to fins in FinFET devices was well-known. See, e.g., SAMSUNG-1030, Abstract (“The fin structures each comprise a semiconductor layer and extend in a first direction, and the gate stack extends in a second direction that is perpendicular.”); SAMSUNG-1008, [0053]; SAMSUNG-1029, [0042]; SAMSUNG-1003, ¶64.

Xie renders obvious the recited positioning of the gate structures

Xie renders obvious that **the first gate structure is over the first fin and the second gate structure is over the second fin**, as illustrated *supra*. Xie’s device includes “first and second spaced-apart active regions formed in a semiconductor substrate, wherein *each of the active regions includes at least one fin*, [and] first and second spaced-apart *gate structures positioned above said first and second active regions.*” SAMSUNG-1004, [0017]; see [0015]-[0018], [0040]-[0041], FIG. 2I, FIGS. 2K-2O; claims 9, 11, 16; SAMSUNG-1003, ¶65.

Moreover, as discussed by Dr. Liu, the positioning of the gate structures over the respective fins is confirmed by Xie’s replacement gate fabrication process. See SAMSUNG-1004, [0037]-[0038], FIG. 2H; SAMSUNG-1003, ¶66.

Moreover, Xie renders obvious that **the second gate structure is discontinuous with the first gate structure**, as illustrated *infra*. The first and second gate structures (blue) are **discontinuous** because they are separated by a gate separation structure (green; *see* [26f]). *See* SAMSUNG-1004, [0017] (“first and second *spaced-apart gate structures* ..., and a gate separation structure positioned between the first and second spaced-apart gate structures”), [0031]-[0032] (“a transverse ‘cut’ 115 of the gate stack material layer(s) is first performed to define the ends 110X of what will become the sacrificial gate structures 107” (in a replacement gate process; or final gate structures in a gate-first process), and “a gate separation structure 114 [is] formed in the opening”), [0040]-[0041], [0015]-[0016], [0018], FIG. 2I, FIGS. 2K-2O, claims 1, 9, 11, 16; SAMSUNG-1003, ¶67.



Xie composite figure – Replacement gate structure

The discontinuity is **along the second direction**: the discontinuity is reached *as one moves in the second direction* from one gate structure to the other (top to bottom in the top view, left to right in the Y-Y view). See SAMSUNG-1004, FIG. 2I; SAMSUNG-1003, ¶68.

Furthermore, Xie renders obvious that **the second gate structure has an edge** (outlined in pink) **that faces an edge** (also pink) **of the first gate structure**, *e.g.*, the edges of the gate structures that contact the gate separation structure face one another. Xie explains that “each of the gate structures has an end surface” (*e.g.*, **an edge**), where “first and second opposing surfaces of the gate separation

structure” “abut the end surfaces of first and second spaced-apart gate structures, respectively.” SAMSUNG-1004, [0016]; *see* [0032] (in FIG. 2D, “***the ends 110X*** of what will become the sacrificial gate structures 107 abut the horizontal portions 114H of the gate separation structure 114”), [0035], [0040]-[0041], FIG. 2I, FIGS. 2C-2E, FIGS. 2K-2O, claims 1, 11, and 16; SAMSUNG-1003, ¶¶69-70.

The edges (*e.g.*, end surfaces 110X) of the gate structures face one another **along the second direction**: from the edge of the second gate structure, the edge of the first gate structure is reached ***as one moves in the second direction*** (top to bottom in the top view, left to right in the Y-Y view). SAMSUNG-1003, ¶¶70-71.

Xie renders obvious that the gate structures each includes a gate dielectric layer and a gate electrode

Xie’s gate structures include “a high-k (k value greater than 10) gate insulation layer,” “one or more metal layers,” and “a bulk conductive metal layer.” SAMSUNG-1004, [0038]; *see* [0030]. As discussed *supra* in §IV.A.2, a POSITA would have understood or found obvious to implement the “gate insulation layer” and “bulk conductive metal layer” (*id.*, [0038]) of Xie’s gate structures as a **gate dielectric layer** and a **gate electrode**, respectively. *See* SAMSUNG-1005, 5:5-46, 8:67-9:4, FIG. 5A; SAMSUNG-1025, 4:39-5:3, FIG. 9A; SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1012, 4:46-54; SAMSUNG-

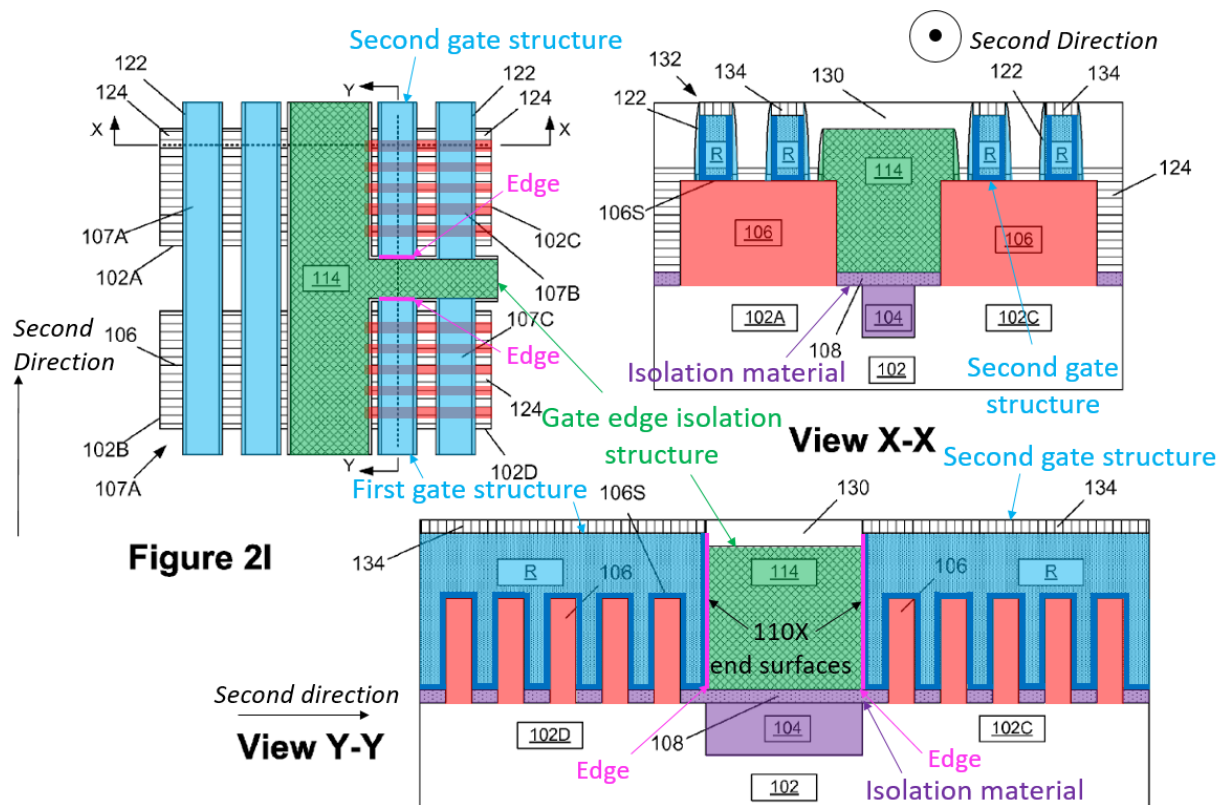
[illegible]

A cross-sectional view of a semiconductor device. The structure features a gate electrode (blue) and gate dielectric (light blue) layers. Below these, there are several layers and regions: a purple layer labeled 102, a purple layer labeled 104, a purple layer labeled 108, a purple layer labeled 106, a purple layer labeled 106S, a purple layer labeled 114, a purple layer labeled 130, and a purple layer labeled 134. The gate electrode is divided into two sections, each containing a region labeled 'R'. The gate dielectric is also divided into two sections, each containing a region labeled 'R'. The regions 102D and 102C are indicated by arrows pointing to the purple layer 102 on the left and right sides, respectively.

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Limitation [26f]

Xie renders obvious a **gate edge isolation structure**, *e.g.*, Xie's gate separation structure 114, green in the figure *infra*. See SAMSUNG-1004, [0032] (“a **gate separation structure** 114 was formed in the opening”), [0015]-[0018], [0041], claims 1-3, 6-7, 11-14, 16-17, Figs. 2D-2I, Figs. 2M-2O; SAMSUNG-1003, ¶74.



Xie composite figure – Replacement gate structure

A POSITA would have understood or found obvious that Xie’s gate separation structure is a **gate edge isolation structure**: it is disposed between and in contact with edges of gate structures (discussed *infra*), and isolates those gate

structures from one another (*e.g.*, physically and electrically).⁸ SAMSUNG-1003, ¶75.

Xie's gate separation structure *physically isolates* the gate structures, *e.g.*, separating them such that they are not in physical contact. *See* SAMSUNG-1004, SAMSUNG-1004, [0015]-[0018], [0031]-[0032]; SAMSUNG-1003, ¶76.

Additionally, a POSITA would have understood or found obvious that Xie's gate separation structure *electrically isolates* the gate structures. The gate separation structure is composed of an "insulating material." SAMSUNG-1004, [0032]. An insulating material disposed between two conductive elements (the first and second gate structures) electrically isolates those conductive elements from one another. SAMSUNG-1003, ¶77. More specifically, a POSITA would have recognized that an insulating gate separation structure disposed between two gate structures electrically isolates those two gate structures. *See* SAMSUNG-1009, [0035] ("The gates may be self-aligned to *isolation structures insulating*

⁸ The interpretation of "gate edge isolation structure" applied throughout this Petition is consistent with the interpretation of this phrase applied by Patent Owner in the pending ITC proceeding, as best understood from the infringement contentions. *See* SAMSUNG-1051, 16-17; SAMSUNG-1052, 22-23; SAMSUNG-1053, 12-14.

gates from each other”), [0007], [0039], claim 15; SAMSUNG-1010, 7:64-8:4; SAMSUNG-1003, ¶77.

Xie renders obvious that the **gate edge isolation structure** (*e.g.*, Xie’s gate separation structure) is **between and in contact with the edge of the first gate structure and the edge of the second gate structure**. The figure *supra* illustrates this positioning, with the edges of the gate structures (*e.g.*, the end surfaces 110X; *see* SAMSUNG-1004, [0035]) outlined in pink. SAMSUNG-1003, ¶78.

Specifically, Xie renders obvious that the gate edge isolation structure is **between** the first and second gate structures: Xie’s “gate separation structure [is] *positioned between the first and second spaced-apart gate structures.*” SAMSUNG-1004, [0017]; *see* [0031]-[0032], [0040], [0015]-[0016], [0018], [0041], FIG. 2I, FIGS. 2L-2O; SAMSUNG-1003, ¶79. Moreover, Xie also renders obvious that the gate edge isolation structure is **in contact with** the edges of the gate structures: “first and second opposing surfaces of the gate separation structure *abut the end surfaces* [*e.g.*, edges] *of first and second spaced-apart gate structures*, respectively.” SAMSUNG-1004, [0017]; *see* [0035] (“due to the presence of the gate separation structure 114 that *contacts the end surfaces 110X of the gate structures* 107B and 107C”), FIG. 2I, FIGS. 2L-2O; SAMSUNG-1003, ¶80. Moreover, as discussed by Dr. Liu, the positioning of the gate edge isolation structure **between and in contact with** the edges of the first and second gate

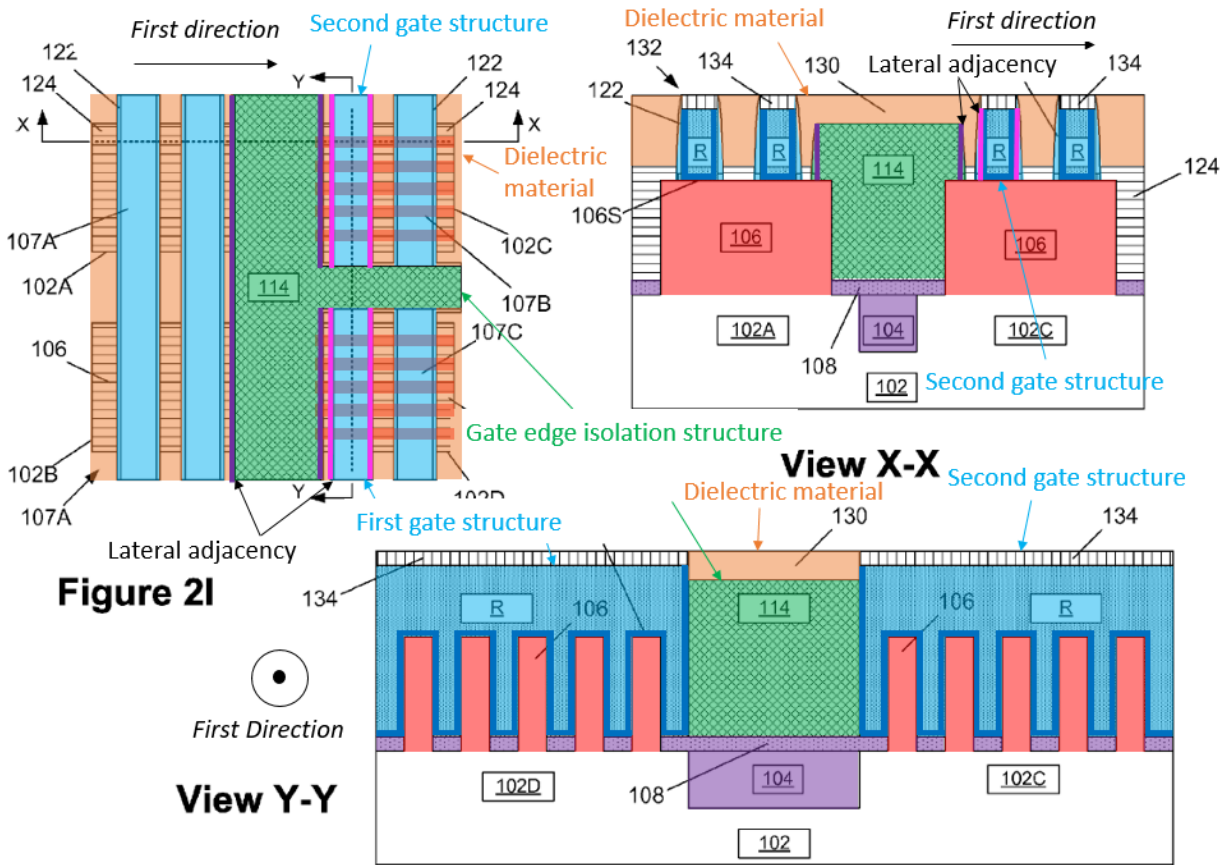
structures is confirmed by Xie's fabrication process. *See* SAMSUNG-1004, [0031], [0032], [0038], FIGS. 2C-2D, FIG. 2H; SAMSUNG-1003, ¶81.

The gate edge isolation structure is between and in contact with the edges of the gate structures **along the second direction: *as one moves in the second direction*** (top to bottom in the top view, left to right in the Y-Y view) starting from the edge of the first gate structure, one reaches first the gate edge isolation structure and then the edge of the second gate structure. SAMSUNG-1003, ¶82.

Xie also renders obvious that the gate edge isolation structure is **over the isolation material** (*e.g.*, Xie's isolation material 108 or isolation structure 104, both in purple), as illustrated *supra*. This positioning is confirmed by Xie's description of forming the gate separation structure in the opening 112 (*see* FIG. 2C, *supra*), where the isolation materials are disposed at the bottom of the opening. *See* SAMSUNG-1004, [0031]-[0032], [0039]-[0041], FIGS. 2C-2I; SAMSUNG-1003, ¶83.

Limitation [26g]

Xie renders obvious a **dielectric material**, *e.g.*, Xie's insulating material 130, orange in FIG. 2I, *infra*. *See* SAMSUNG-1004, [0036] ("a layer of ***insulating material 130***, *e.g.*, silicon dioxide, ... blanket-deposited above the epi semiconductor material"), FIG. 2I; SAMSUNG-1003, ¶84. An insulating material such as silicon dioxide is a dielectric material. SAMSUNG-1003, ¶84.



Xie composite figure – Replacement gate structure

The sidewalls of the gate structures are outlined in pink. These sidewalls extend into the page of the top-view figure, and the dielectric material is disposed next to these sidewalls, as can be seen from the X-X cross-section. **The dielectric material (orange) is laterally adjacent to each gate structure** at least at these pink-outlined sidewalls. For instance, the dielectric material contacts the spacers 122 (see SAMSUNG-1004, [0035]) that are disposed on those sidewalls. The dielectric material is thus **laterally adjacent** to the gate structures, *e.g.*, the

dielectric material is near (*e.g.*, next to) the sidewalls of the gate structures.

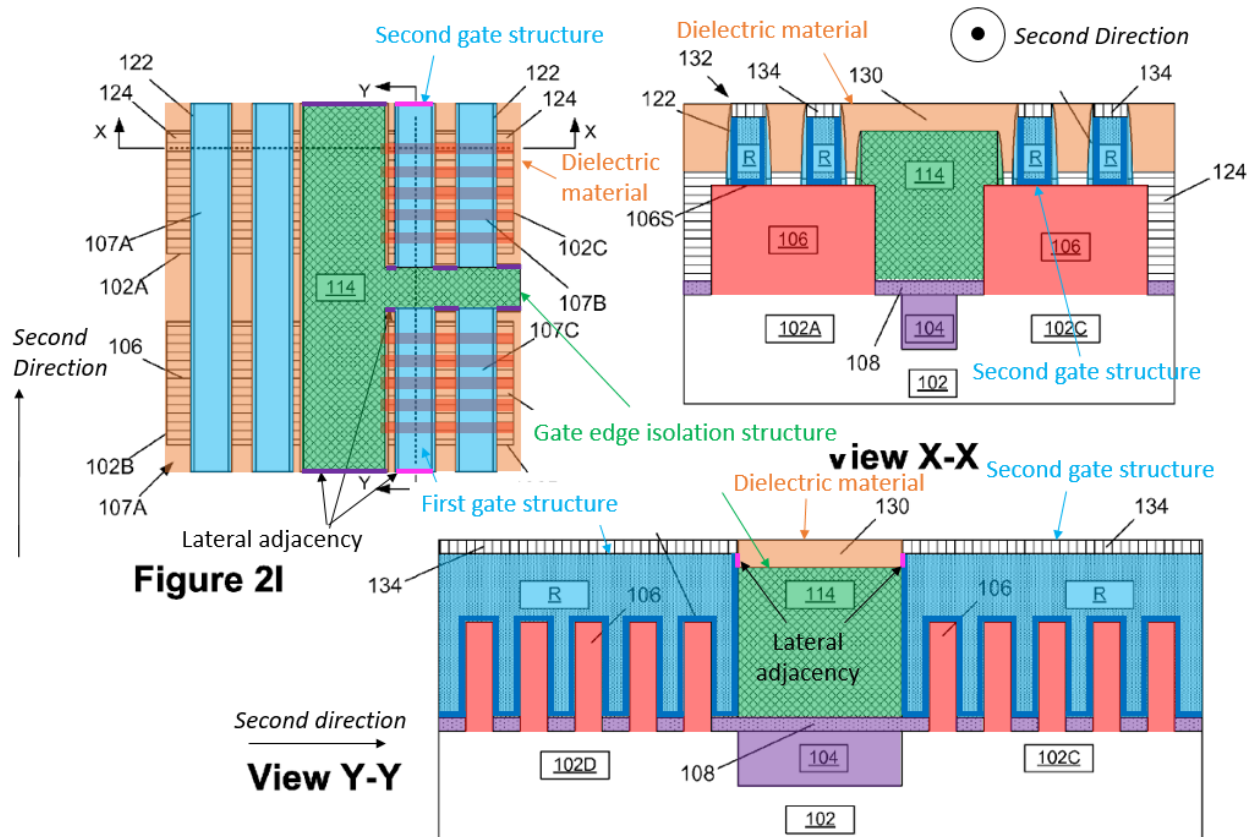
SAMSUNG-1003, ¶85.

The sidewalls of the gate edge isolation structure are outlined in purple in the figure *supra*. These sidewalls extend into the page of the top-view figure. As with the sidewalls of the gate structures, and as can be seen from the X-X cross-section, **the dielectric material (orange) is laterally adjacent to the gate edge isolation structure** at least at these purple-outlined sidewalls. For instance, the dielectric material contacts the spacers 122 (*see* SAMSUNG-1004, [0035]) that are disposed on those sidewalls. The dielectric material is thus **laterally adjacent** to the gate edge isolation structure, *e.g.*, the dielectric material is near (*e.g.*, next to) the sidewalls of the gate edge isolation structure. SAMSUNG-1003, ¶87.

The dielectric material is laterally adjacent to the gate structures and to the gate edge isolation structure **along the first direction**: viewing the structure starting from either gate structure or from the gate edge isolation structure and ***moving along the first direction*** (left to right in the top and X-X views), one reaches the dielectric material. SAMSUNG-1003, ¶¶86, 88.

Alternatively or additionally, the dielectric material is laterally adjacent to the gate structures and gate edge isolation structures at the pink-outlined and purple-outlined locations, respectively, in the alternative annotated version of Xie's FIG. 2I *infra*. SAMSUNG-1003, ¶¶89-90. To the extent this spatial relationship is

considered to be laterally adjacent **along the first direction**, the dielectric material is laterally adjacent to the gate structures and gate edge isolation structure along the first direction. *Id.*



Xie composite figure – Replacement gate structure (alternative)

Xie also renders obvious that **the dielectric material is discrete from the gate edge isolation structure**, *e.g.*, the layer of insulating material is discrete from the gate separation structure at least because *they are formed in two distinct processing steps*: the dielectric material is deposited after the gate separation structure has already been formed. *See* SAMSUNG-1004, [0032], [0036], FIGS. 2D and 2G; SAMSUNG-1003, ¶91. Moreover, Xie identifies the dielectric

material and the gate separation structure as distinct elements. *See* SAMSUNG-1004, [0032], [0036]; SAMSUNG-1003, ¶91.

(2) Claim 27

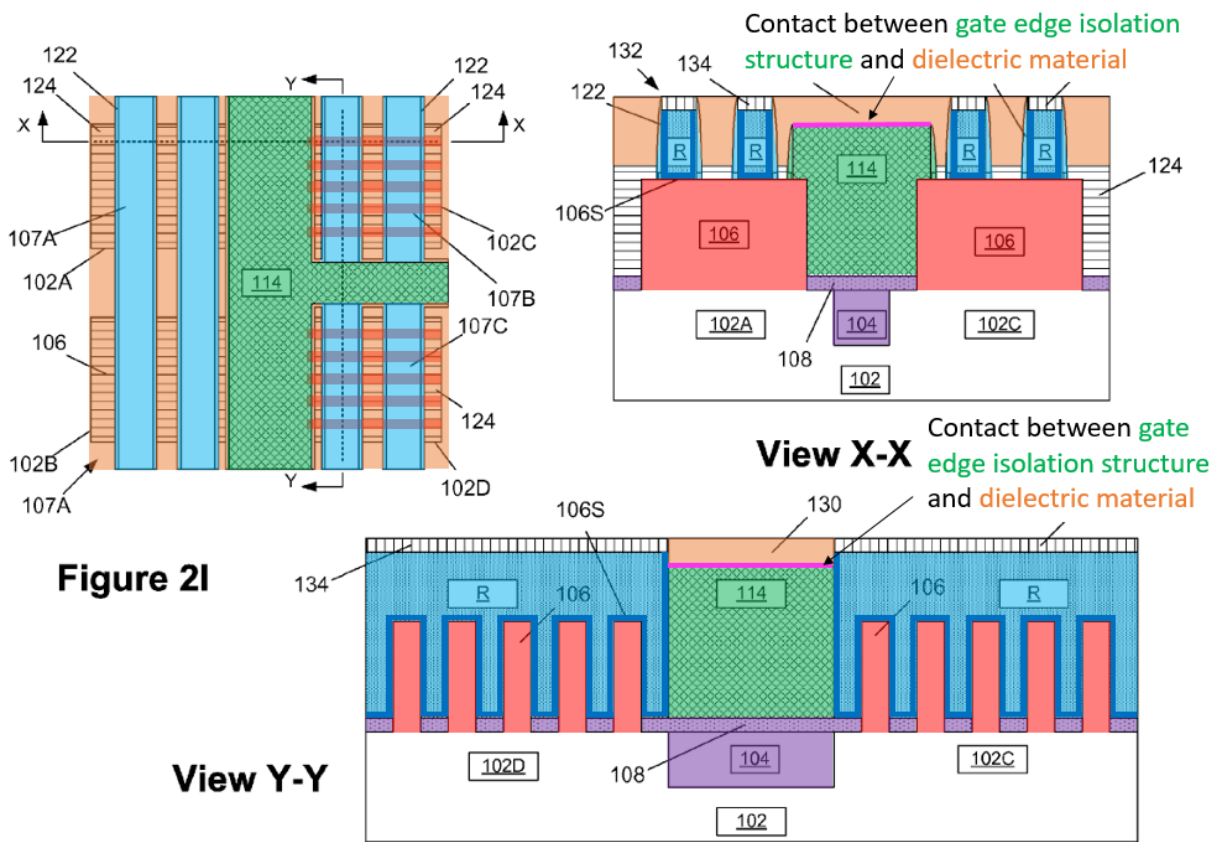
Limitation [27]

Xie renders obvious that the gate edge isolation structure (*e.g.*, Xie's gate separation structure) comprises silicon nitride, *i.e.*, **silicon and nitrogen**. *See* SAMSUNG-1004, [0032] (The gate separation structure 114 may be comprised of a variety of materials, *e.g.*, ... ***silicon nitride***"); SAMSUNG-1003, ¶92.

(3) Claim 28

Limitation [28]

Xie renders obvious that **the dielectric material** (*e.g.*, Xie's insulating material, orange) is **in contact with the gate edge isolation structure** (*e.g.*, Xie's gate separation structure, green). As illustrated *infra*, this contact is at least on the top surface of the gate edge isolation structure, outlined in pink. As discussed by Dr. Liu, this contact is confirmed by Xie's fabrication process. *See* SAMSUNG-1004, [0032], [0036]; SAMSUNG-1003, ¶¶93-94.



Xie composite figure – Replacement gate structure

(4) Claim 29

Limitation [29]⁹

Xie renders obvious that when the gate structures are fabricated by a replacement gate process (*see* SAMSUNG-1004, [0030]), **the gate edge isolation**

⁹ As best understood, Petitioner interprets the “gate dielectric layer of the first gate structure” and the “gate dielectric layer of the second gate structure” recited in claim 29 as being the first and second gate dielectric layers, respectively, of claim 26.

structure is in contact with a gate dielectric layer of each of the gate

structures. SAMSUNG-1003, ¶95. In a replacement gate fabrication process, the gate dielectric layer is deposited into the “gate cavities 132,” and thus is coated onto exposed surfaces in the gate cavities, including onto exposed sidewalls of the gate separation structure. *See* §IV.A.3; *see* SAMSUNG-1004, [0038], FIG. 2I; *see* SAMSUNG-1025, 4:39-5:56; SAMSUNG-1005, 8:62-9:4; SAMSUNG-1015, [0045]-[0047]; SAMSUNG-1012, 11:4-14; SAMSUNG-1014, 7:8-42; SAMSUNG-1003, ¶95. Thus, **the gate edge isolation structure** (*e.g.*, Xie’s gate separation structure) **is in contact with the gate dielectric layer** of each gate structure, *e.g.*, the gate dielectric layer of each gate structure coats the respective sidewall of the gate separation structure. SAMSUNG-1003, ¶95.

An example replacement gate structure is depicted *infra*, showing contact between the sidewalls of the gate edge isolation structure (green) and the gate dielectric layers (dark blue). SAMSUNG-1003, ¶96.



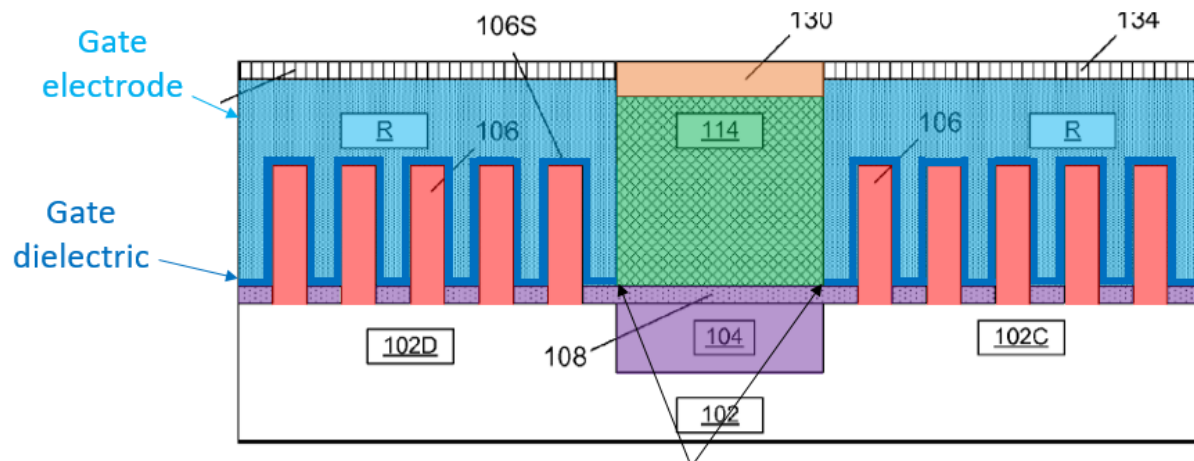
Xie composite figure – Replacement gate structure

fabricated by a gate-first process (*see* SAMSUNG-1004, [0030]), **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures.** SAMSUNG-1003, ¶97. In a gate-first fabrication process, a gate dielectric layer and gate electrode are deposited and then etched to form openings, defining the ends of the gate structures and exposing the gate dielectric layer and the gate electrode at these ends. SAMSUNG-1004, [0031]; *see* [0040]; SAMSUNG-1005, 4:59-5:55, FIG. 5A; SAMSUNG-1016, FIG. 13, 19:41-20:16, 22:7-8; SAMSUNG-1017, FIG. 2, 4:7-16; SAMSUNG-1003, ¶97; *see* §IV.A.4. The “gate separation structure 114” is then “formed in the opening,” thus contacting the exposed gate dielectric layer and gate electrode. SAMSUNG-1004, [0032]; *see* [0040]; *see* SAMSUNG-1005, 5:47-55; SAMSUNG-1003, ¶97. Thus, **the gate edge isolation structure (e.g., Xie’s gate separation structure) is in**

contact with the gate dielectric layers of the first and second gate structures.

SAMSUNG-1003, ¶97.

An example gate-first gate structure is depicted *infra*, showing contact between the sidewalls of the gate edge isolation structure (green) and both the gate dielectric layers (dark blue) and the gate electrodes (light blue). SAMSUNG-1003, ¶98.



Contact between gate dielectric and gate edge isolation structure

Xie composite figure – Gate-first gate structure

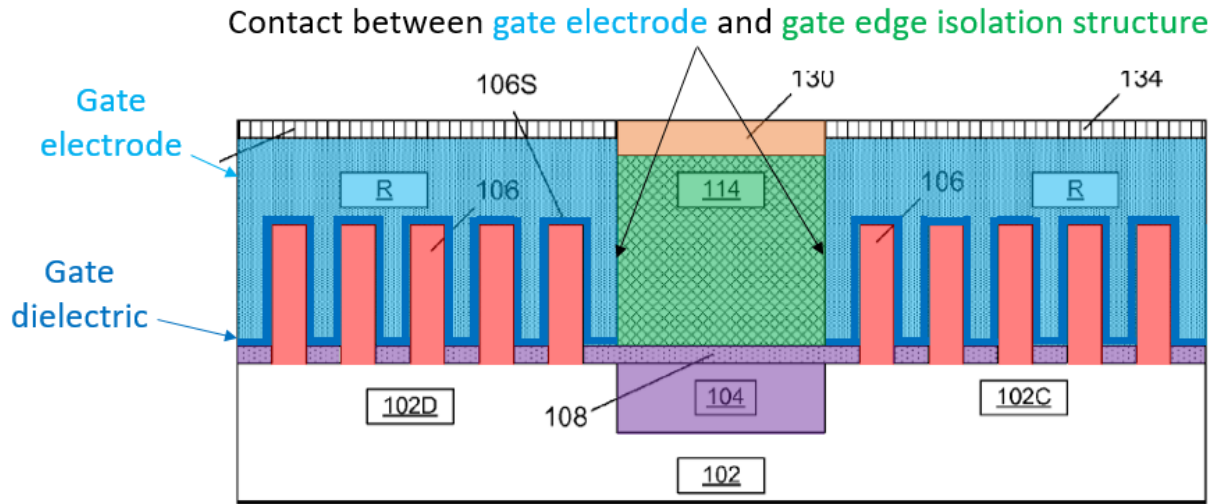
(5) Claim 30

Limitation [30]

First, as discussed in §IV.A.2, a POSITA would have understood or found obvious that Xie's gate structures each includes a gate dielectric layer (*e.g.*, a high-k gate dielectric layer) and a gate electrode (*e.g.*, a **metal gate electrode**). See SAMSUNG-1004, [0038]; SAMSUNG-1005, 5:5-46; SAMSUNG-1025, 4:39-5:3;

SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1014, 7:8-22; SAMSUNG-1015, [0047]; SAMSUNG-1003, ¶99. For instance, a POSITA would have understood or found obvious for Xie's "bulk conductive metal layer" to be a gate electrode, *e.g.*, a **metal gate electrode layer**. SAMSUNG-1004, [0038]; SAMSUNG-1003, ¶99.

Second, Xie renders obvious that when the gate structures are fabricated by a gate-first process (*see* SAMSUNG-1004, [0030]), **the gate edge isolation structure is in contact with the metal gate electrode layers of the first and second gate structures**, as discussed in [29]. *See* SAMSUNG-1004, [0031]-[0032], [0040]; SAMSUNG-1005, 4:59-5:55; SAMSUNG-1016, FIG. 13, 19:41-20:16, 22:7-8; SAMSUNG-1017, FIG. 2, 4:7-16; SAMSUNG-1003, ¶100; *see* §IV.A.4. The gate-first structure illustrated *infra* shows contact between the sidewalls of the gate edge isolation structure (green) and the gate electrodes (light blue). SAMSUNG-1003, ¶100.



Xie composite figure – Gate-first gate structure

(6) Claim 31

Limitation [31]

As discussed in §IV.A.2, a POSITA would have understood or found obvious that Xie’s gate structures each includes a gate dielectric layer (*e.g.*, a **high-k gate dielectric layer**) and a gate electrode (*e.g.*, a metal gate electrode). *See* SAMSUNG-1004, [0038]; SAMSUNG-1005, 5:5-46; SAMSUNG-1025, 4:39-5:3; SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1014, 7:8-22; SAMSUNG-1015, [0047]; SAMSUNG-1003, 101. For instance, a POSITA would have understood or found obvious for Xie’s “high-k ... gate insulation layer” to be a gate dielectric layer that includes a **high-k dielectric material**. SAMSUNG-1004, [0038]; SAMSUNG-1003, ¶101.

B. [GROUND 2] – CLAIMS 26-31 ARE OBVIOUS OVER XIE AND TSENG

The sections below provide a brief introduction to Tseng and the Xie-Tseng combination.¹⁰

Ground 2 is substantively identical to, and incorporates the analysis of, Ground 1 in all but the following respects. While Ground 1 demonstrates that the Element [26d] and [26e] features are obvious in view of Xie, Ground 2 relies on the even more explicit disclosure of Tseng to reach these features, as well as to reach dependent claims 29-31. Integration of Tseng does not disturb the mapping of Xie to other claim elements. To avoid repetition, and because the analysis of all other claim elements is identical, only the pertinent portions of Elements [26d]-[26e] and claims 29-31 are addressed in §IV.B. The unaddressed claim 26 elements, and claims 27-28, are obvious over the Xie-Tseng combination at least as demonstrated for Ground 1. SAMSUNG-1003, ¶102.

1. Tseng describes FinFET gate structures having a gate dielectric layer and a gate electrode

Tseng describes a FinFET having a “gate stack 210” including a “gate electrode layer 214 and [a] gate dielectric layer 212.” SAMSUNG-1005, 5:5-10; *see* 3:4-12, FIGS. 2, 5A. The gate dielectric layer can be a “high dielectric

¹⁰ Petitioner incorporates this discussion into Ground 2.

constant (high-k) dielectric,” and the gate electrode can include a “N-work function metal” or a “P-work function metal.” SAMSUNG-1005, 5:12-46. Tseng’s gate stack can be “fabricated using a gate-first process” or “using a gate-last process.” *Id.*, 8:59-62; SAMSUNG-1003, ¶103.

2. The Xie-Tseng combination

In the Xie-Tseng combination, Xie’s gate structures (*e.g.*, replacement gate structures or gate-first gate structures; *see* SAMSUNG-1004, [0030]) include gate dielectric layers and gate electrodes based on Tseng. *See* SAMSUNG-1005, 5:5-46; SAMSUNG-1003, ¶104. For instance, in the combination, Xie’s “high-k ... gate insulation layer” is implemented as a high-k gate dielectric layer, and Xie’s “bulk conductive metal layer” is implemented as a metal gate electrode layer. SAMSUNG-1004, [0038]; *see* SAMSUNG-1005, 5:5-46, 8:67-9:4, FIG. 5A; SAMSUNG-1003, ¶104.

The configurations of these Xie-Tseng gate structures are consistent with the replacement gate structure and gate-first gate structure illustrated in §§IV.A.3-4. SAMSUNG-1003, ¶105.

A POSITA would have been motivated to pursue this implementation, and would have expected success in doing so, at least as discussed in §IV.A.2. SAMSUNG-1003, ¶106. Moreover, a POSITA would have expected success specifically in the Xie-Tseng combination given that both Xie and Tseng relate to

FinFET fabrication processes that can be performed using gate-first or gate-last processes. *See* SAMSUNG-1004, [0030]; SAMSUNG-1005, 8:59-62; SAMSUNG-1003, ¶106.

3. Analysis

(1) Claim 26

Limitations [26d] and [26e]

Xie-Tseng renders obvious gate structures having the recited features, *e.g.*, in view of Xie's final gate structures (*e.g.*, replacement gate structures or gate-first gate structures). *See* [26d]-[26e] of Ground 1. SAMSUNG-1003, ¶107.

In the Xie-Tseng combination, the gate structures (*e.g.*, replacement gate structures or gate-first gate structures) include respective **gate dielectric layers** and respective **gate electrodes**, *e.g.*, based on Tseng's description of gate structures with gate dielectric layers and gate electrodes. *See* SAMSUNG-1005, 5:5-46, 3:4-12, FIGS. 2, 5A; SAMSUNG-1003, ¶108.

(2) Claim 29

Limitation [29]

When the Xie-Tseng gate structures are fabricated by a replacement gate process or by a gate-first process (*see* SAMSUNG-1004, [0030]), **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures**. *See* [29] of Ground 1. SAMSUNG-1003, ¶109.

(3) Claim 30

Limitation [30]

The Xie-Tseng gate electrodes include **metal gate electrode layers**. For instance, in the combination, Xie's "bulk conductive metal layer" is implemented as a **metal gate electrode layer** based on Tseng. SAMSUNG-1004, [0038]; *see* SAMSUNG-1005, 5:5-46; SAMSUNG-1003, ¶110.

When the Xie-Tseng gate structures are fabricated by a gate-first process (*see* SAMSUNG-1004, [0030]), **the gate edge isolation structure is in contact with the metal gate electrode layers of the first and second gate structures**.

See [30] of Ground 1. SAMSUNG-1003, ¶111.

(4) Claim 31

[31] The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

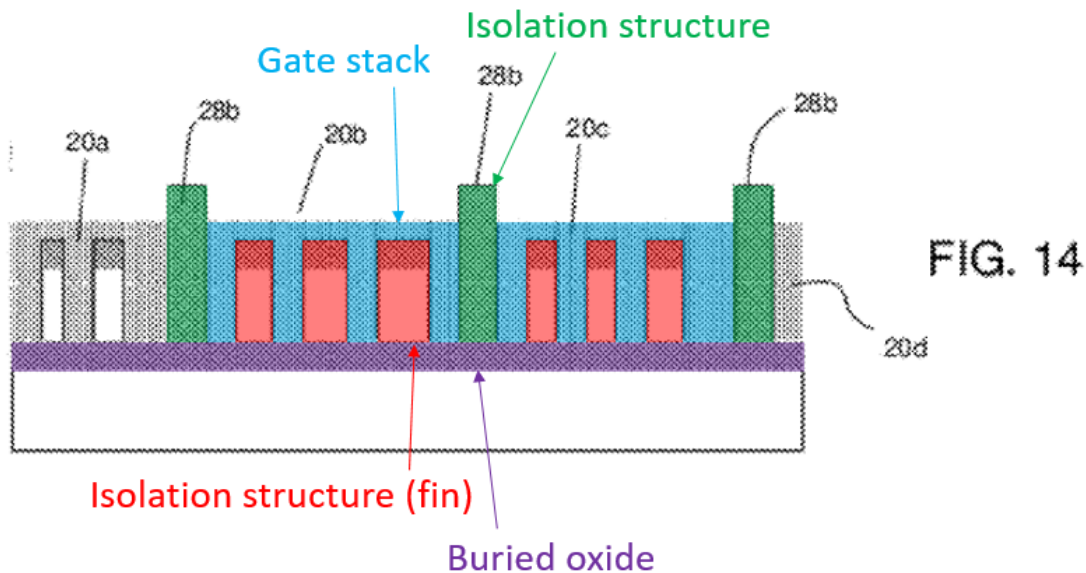
The gate dielectric layers of the Xie-Tseng gate structures include **a high-k dielectric material**. For instance, Xie's "high-k ... gate insulation layer" is implemented as a **gate dielectric layer** that includes **a high-k dielectric material** based on Tseng. SAMSUNG-1004, [0038]; *see* SAMSUNG-1005, 5:5-46; SAMSUNG-1003, ¶112.

**C. [GROUND 3A] – CLAIMS 26-29 AND 31-32 ARE OBVIOUS
OVER ANDERSON AND LIN**

The sections below provide a brief introduction to Anderson, Lin, and the combination thereof.¹¹

**1. Anderson describes gate-to-gate isolation structures for
FinFET devices**

Anderson describes “devices having gate-to-gate isolation structures,” *e.g.*, for use with FinFETs. SAMSUNG-1006, [0019]. These devices have “selectively raised isolation regions ... to provide isolation structures between adjacent gates.” *Id.* See the cross-sectional and top views in FIGS. 14 and 15, respectively, *infra*. See *id.*, [0040]; see [0050]-[0051] and FIGS. 23-26; SAMSUNG-1003, ¶113.



Excerpt from Anderson, FIG. 14 (annotated)

¹¹ Petitioner incorporates this discussion into Grounds 3A-3B.

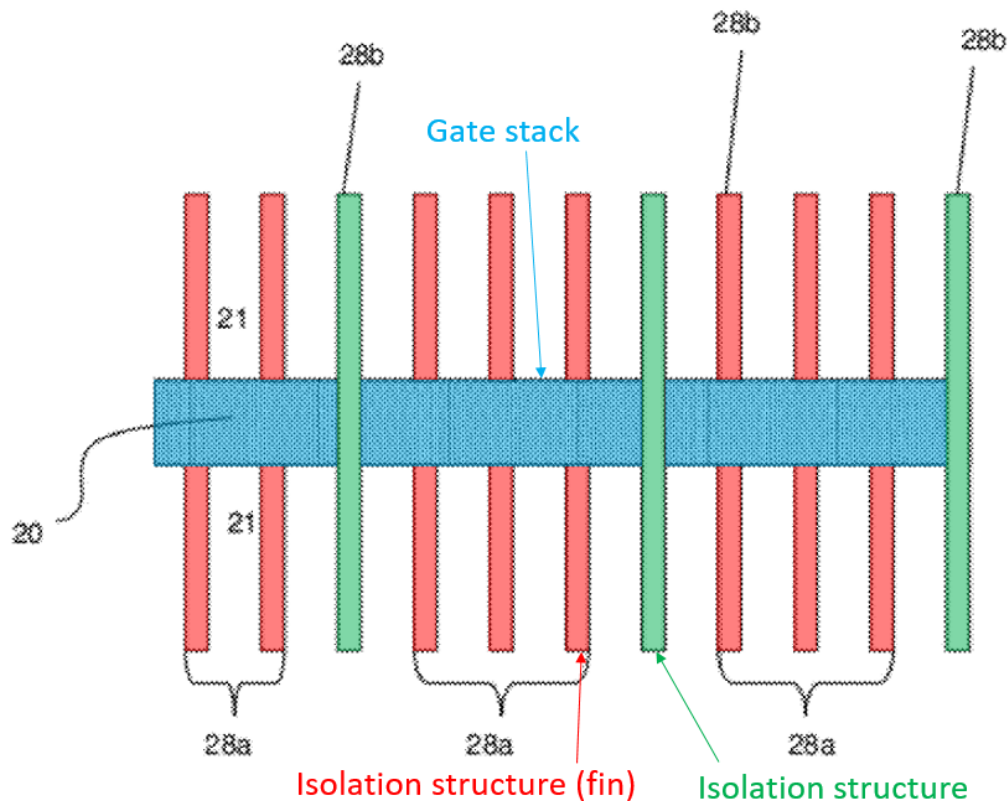


FIG. 15

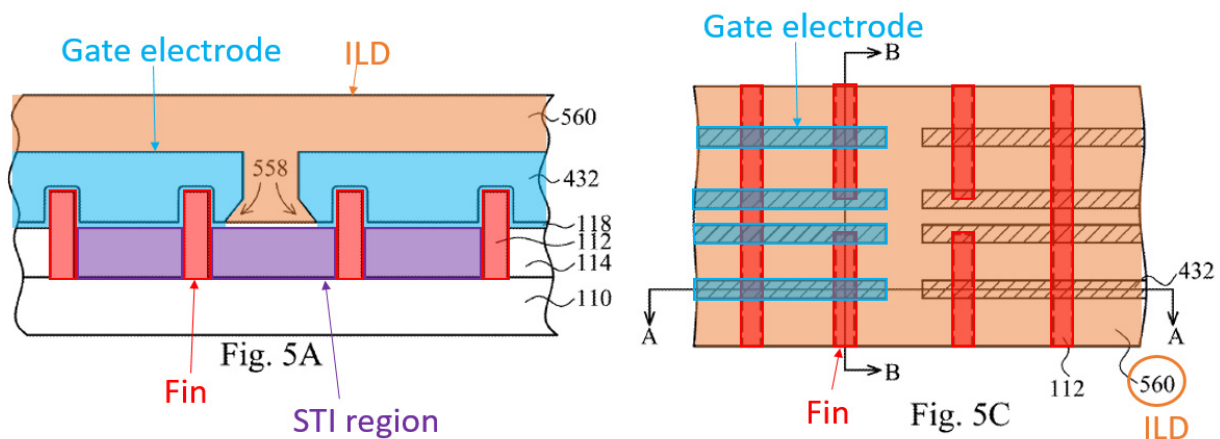
Excerpt from Anderson, FIG. 15 (annotated)

Anderson's device is formed on a "silicon on insulator (SOI) wafer" that includes "a buried oxide 10b" (purple) disposed on "a lower Si layer 10a." SAMSUNG-1006, [0032]; *see* FIG. 9. The device includes "dual height isolation structures 28a and 28b" (red and green, respectively) formed by etching the substrate. *Id.*, [0036]-[0037], FIG. 11; *see* [0047]-[0048], FIG. 20. "[T]he isolation structure 28b is taller than the surrounding isolation structures 28a." *Id.*, [0037]; *see* [0046]. A gate stack 20 (blue) including "a gate dielectric and a gate electrode material," is "formed over the isolation structures" and "partially etched

away to expose the isolation structure 28b,” while still “cover[ing] or bury[ing] the isolation structures 28a.” *Id.*, [0038]-[0039], FIGS. 13-14; *see* [0047]-[0048], FIGS. 22-23. The taller isolation structures 28b “provide a physical and electrical separation between the gates.” *Id.*, [0039]; *see* [0048], [0051], FIGS. 23-26; SAMSUNG-1003, ¶114.

2. Lin describes FinFET gate structures

Lin describes a “fin field-effect transistor (finFET)” that includes fins 112 (red in FIGS. 5A and 5C, *infra*), with a “dielectric layer 114” (purple) that “acts as a shallow trench isolation (STI) around the fins 112.” SAMSUNG-1007, Abstract, 2:55-58. Gate electrodes 432 (blue) are disposed over the fins and separated by “notches 558 in the ends of the gate electrodes 432.” *Id.*, 4:65-5:9. An “inter-layer dielectric (ILD) 560,” orange, is “formed over the gate electrodes 432 and in the notches 558.” *Id.*, 5:15-17; SAMSUNG-1003, ¶115.

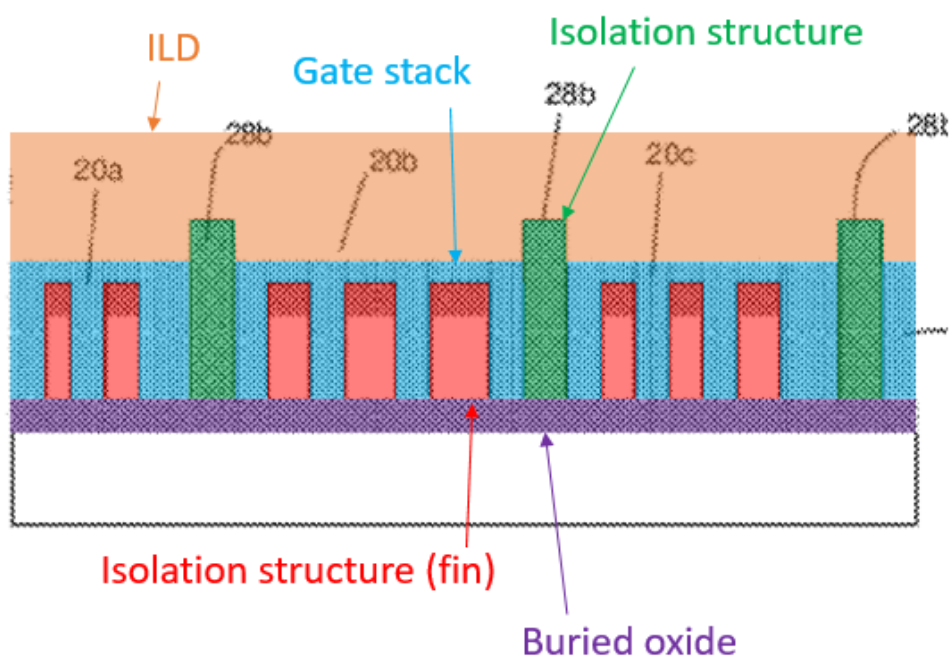


Excerpt from Lin, Figs. 5A and 5C (annotated)

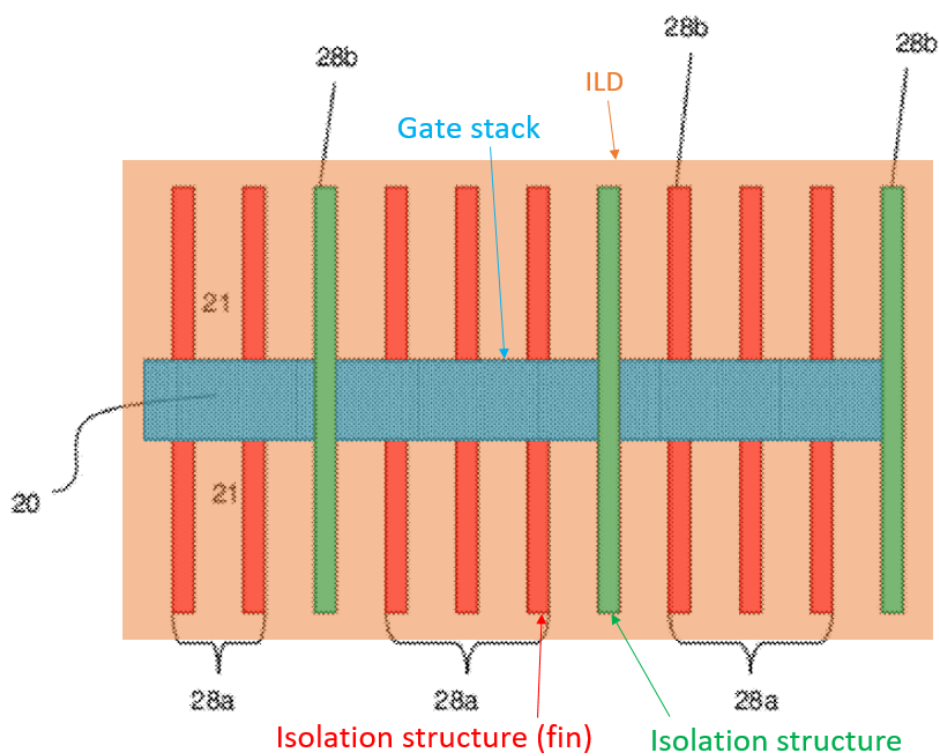
3. The Anderson-Lin combination

An Anderson-Lin combination FinFET is illustrated in the composite figures *infra*.¹² Based on Anderson, this FinFET is formed on an SOI wafer including a buried oxide (purple), and includes dual-height isolation structures: fins 28a (red) and taller isolation structures 28b (green). SAMSUNG-1006, [0036]-[0039]. Gates (blue) cover the fins, and the taller isolation structures are exposed above the top surface of the gates. *See id.*, [0007], [0038]-[0039]. The isolation structures 28b “provide a physical and electrical separation between the gates.” SAMSUNG-1006, [0039]; SAMSUNG-1003, ¶116.

¹² Anderson-Lin cross-sectional and top view composite figures are based on Anderson’s FIGS. 14 and 15, respectively, unless otherwise noted.



Anderson-Lin cross-sectional composite figure

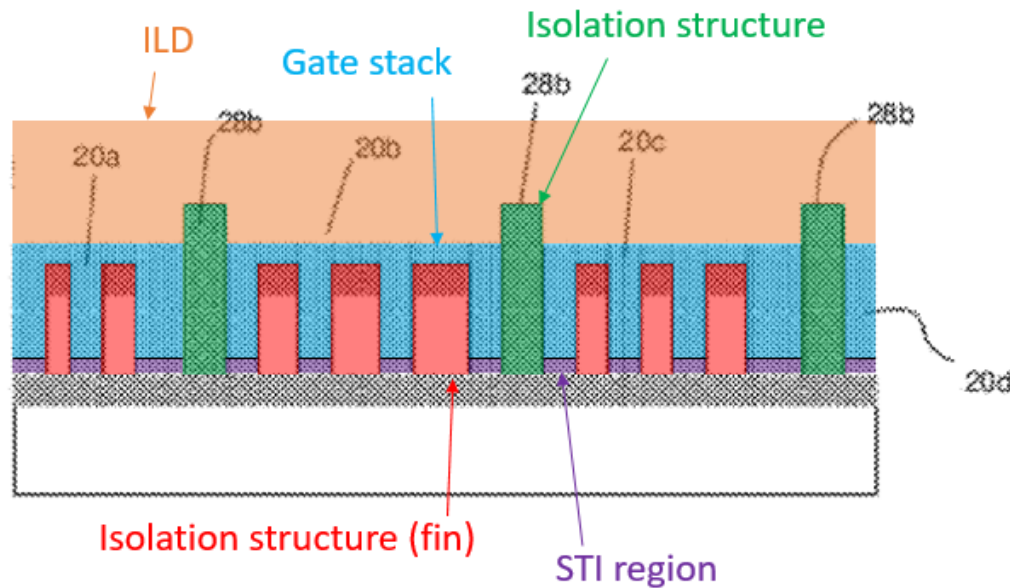


Anderson-Lin top-view composite figure

Based on Lin, an ILD (orange) is “formed over” the gates. SAMSUNG-1007, 5:15-17; SAMSUNG-1003, ¶117. The ILD buries the taller isolation structures 28b, filling the spaces next to the sidewalls and ends of the isolation structures 28b that protrude above the top surfaces of the gates and extend beyond the sidewalls of the gates. *See* SAMSUNG-1007, 5:15-17. The ILD also fills the spaces next to the short end walls of the gate electrodes.¹³ SAMSUNG-1003, ¶117.

Optionally, as shown *infra*, a “dielectric layer” (purple) is disposed on the substrate (*e.g.*, on Anderson’s buried oxide layer), thus “act[ing] as a shallow trench isolation (STI) around the fins” 28a. SAMSUNG-1007, 2:55-58; SAMSUNG-1003, ¶118.

¹³ The top view composite figure depicts the fins, gates, and isolation structures 28b for illustrative purposes only; the ILD covers all of these features.



Anderson-Lin figure

4. Reasons to combine Anderson and Lin

Incorporation of an interlayer dielectric

A POSITA would have been motivated to incorporate an interlayer dielectric (ILD) into the Anderson-Lin integrated circuit structure for at least the following reasons. SAMSUNG-1003, ¶¶119-123.

First, a POSITA would have been motivated to incorporate an ILD to provide electrical isolation between the FinFETs and overlying interconnect structures. See SAMSUNG-1008, [0068] (“An insulating fill 515 provides an interlayer insulator between the patterned gate conductor layer ... and overlying patterned conductor layers”); SAMSUNG-1017, 6:42-44; SAMSUNG-1039, 9:5-8; SAMSUNG-1003, ¶120. The presence of an ILD would enable “contacts [to] be

connected to the source/drain and gate electrodes using conventional etching and metal deposition processes,” as envisioned by Anderson. SAMSUNG-1006, [0050]; SAMSUNG-1003, ¶120.

Second, a POSITA would have been motivated to incorporate an ILD because the use of ILDs above transistor-level structures was a standard element of integrated circuits. *See* SAMSUNG-1004, [0036], FIG. 2I; SAMSUNG-1009, [0051], FIGS. 15A-18D; SAMSUNG-1007, 5:15-17, FIGS. 5A-5C; SAMSUNG-1008, [0068], FIG. 5; SAMSUNG-1017, 6:42-44, FIG. 5; SAMSUNG-1039, 9:5-8, FIG. 3F; SAMSUNG-1003, ¶121.

Third, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, ILD in an integrated circuit device) to a known structure (*e.g.*, a FinFET integrated circuit structure) to yield predictable results (*e.g.*, a FinFET-based integrated circuit having an ILD). SAMSUNG-1003, ¶122; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have expected success because an ILD is compatible with Anderson’s “contacts” fabricated “using conventional etching and metal deposition processes.” SAMSUNG-1006, [0050]; SAMSUNG-1003, ¶123. A POSITA also would have expected success given that the use of ILDs in FinFET-based devices was well-known. *See* SAMSUNG-1004, [0036], FIG. 2I; SAMSUNG-1009,

[0051], FIGS. 15A-18D; SAMSUNG-1007, 5:15-17, FIGS. 5A-5C; SAMSUNG-1008, [0068], FIG. 5; SAMSUNG-1017, 6:42-44, FIG. 5; SAMSUNG-1039, 9:5-8, FIG. 3F; SAMSUNG-1003, ¶123.

Incorporation of shallow trench isolation

A POSITA would have been motivated to incorporate shallow trench isolation (STI) around the base of the fins of the Anderson-Lin integrated circuit structure for at least the following reasons. SAMSUNG-1003, ¶¶124-128.

First, a POSITA would have been motivated to incorporate STI to isolate the fins from one another, thereby improving the electrical performance of the device, *e.g.*, by reducing leakage current. *See* SAMSUNG-1005, 4:25-27 (“the trenches 22 are filled with a dielectric material ... to define and electrically isolate the various fins of the fin structure 202.”); SAMSUNG-1010, 1:43-45; SAMSUNG-1031, 5:16-18; SAMSUNG-1003, ¶125.

Second, a POSITA would have been motivated to integrate STI regions specifically over Anderson’s buried oxide layer because STI used in conjunction with silicon-on-insulator (SOI) substrates was a conventional approach providing benefits of both SOI and STI. *See* SAMSUNG-1034, 2:24-36 (“The SOI substrate may allow a transistor to operate at a higher switching speed or with a lower power consumption when compared to a bulk semiconductor substrate. ... [S]hallow trench isolation (STI) that extends from a surface of the SOI substrate ... may

provide an electrical isolation around a periphery of the transistor primarily in a horizontal (or lateral) direction”); SAMSUNG-1035, 1:22-32 (“FinFET structures may be formed on a semiconductor-on-insulator (SOI) substrate, because of the low source/drain diffusion, low substrate capacitance, and ease of electrical isolation by shallow trench isolation structures”); SAMSUNG-1041, 3:46-56 (describing a device having SOI and STI isolation that “maintains [] manufacturing simplicity, and benefits from FD-SOI’s and FinFET’s immunity to floating-body effects”), 6:6-46; SAMSUNG-1036, 3:55-59; SAMSUNG-1037, 3:16-18; SAMSUNG-1038, [0074]; SAMSUNG-1003, ¶126.

Third, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, STI in an integrated circuit device) to a known structure (*e.g.*, a FinFET integrated circuit structure) to yield predictable results (*e.g.*, a FinFET-based integrated circuit having STI structures). SAMSUNG-1003, ¶127; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have expected success because of the compatibility of STI processing (*e.g.*, CVD; *see* SAMSUNG-1007, 2:55-58) with SOI structures. *See* SAMSUNG-1005, 4:25-27; SAMSUNG-1010, 1:43-45; SAMSUNG-1031, 5:16-18; SAMSUNG-1003, ¶128. A POSITA also would have expected success given that the use of STI in FinFET-based devices was well-known. *See* SAMSUNG-

1005, 4:25-27; SAMSUNG-1031, 5:16-18; SAMSUNG-1032, 1:50-53;
SAMSUNG-1003, ¶128.

5. Analysis

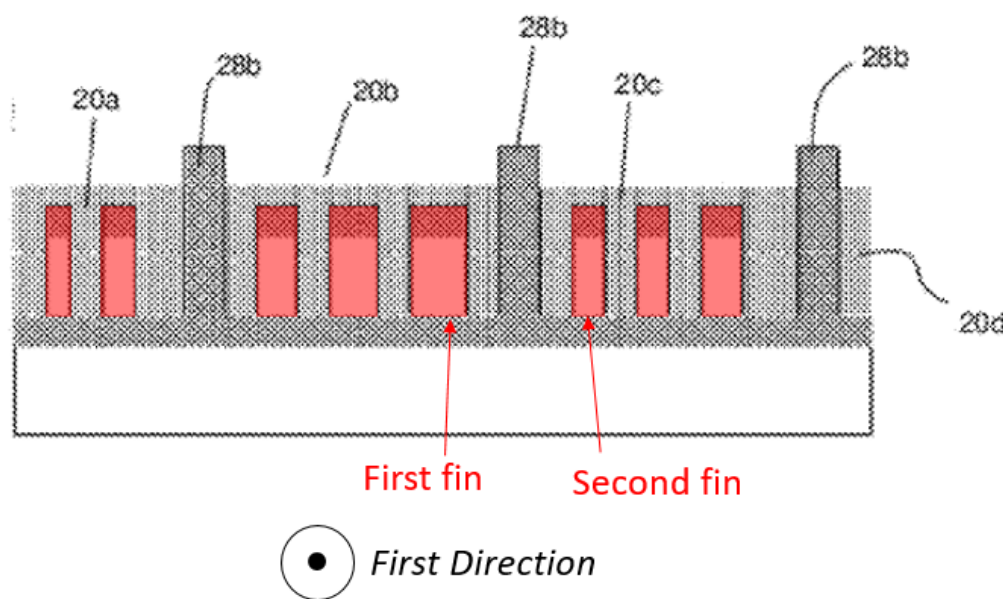
(1) Claim 26

Limitation [26pre]

To the extent the preamble is deemed to be limiting, Anderson-Lin renders it obvious. *See* SAMSUNG-1006, [0019] (“The present invention ... can be used for *FinFETs*”), [0051], [0001], [0007], claim 20; SAMSUNG-1003, ¶129.

Limitations [26a] and [26b]

The Anderson-Lin combination includes **first and second fins**, *e.g.*, Anderson’s *isolation structures 28a*, red in the figures *infra*. *See* SAMSUNG-1006, [0036] (“A RIE process is then performed to form trenches 26 and *fins 27a* and 27b (also isolation structures),” as shown in FIG. 11, and “the remaining portion of the pad film 22 is removed from the fins 27a, leaving *isolation structures 28a* and 28b.”), FIGS. 14-15. *See also* Anderson’s “isolation structures 28a” (*e.g.*, **fins**) in FIGS. 22-24 (*id.*, [0044]-[0046]) and isolation structures 38a (*e.g.*, **fins**) in FIGS. 25-26 (*see id.*, [0051]); *see* [0005]-[0007]; SAMSUNG-1003, ¶130.



Anderson-Lin cross-sectional figure

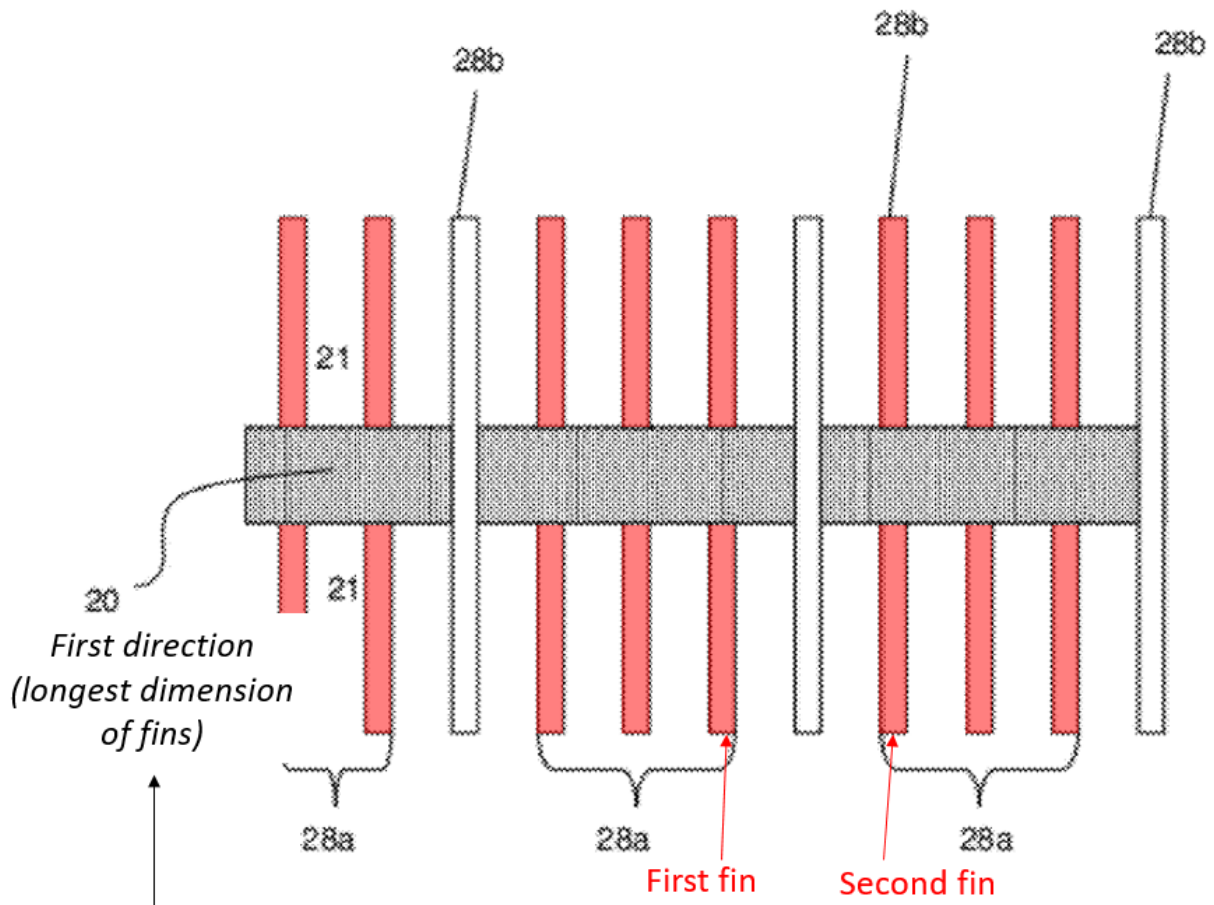
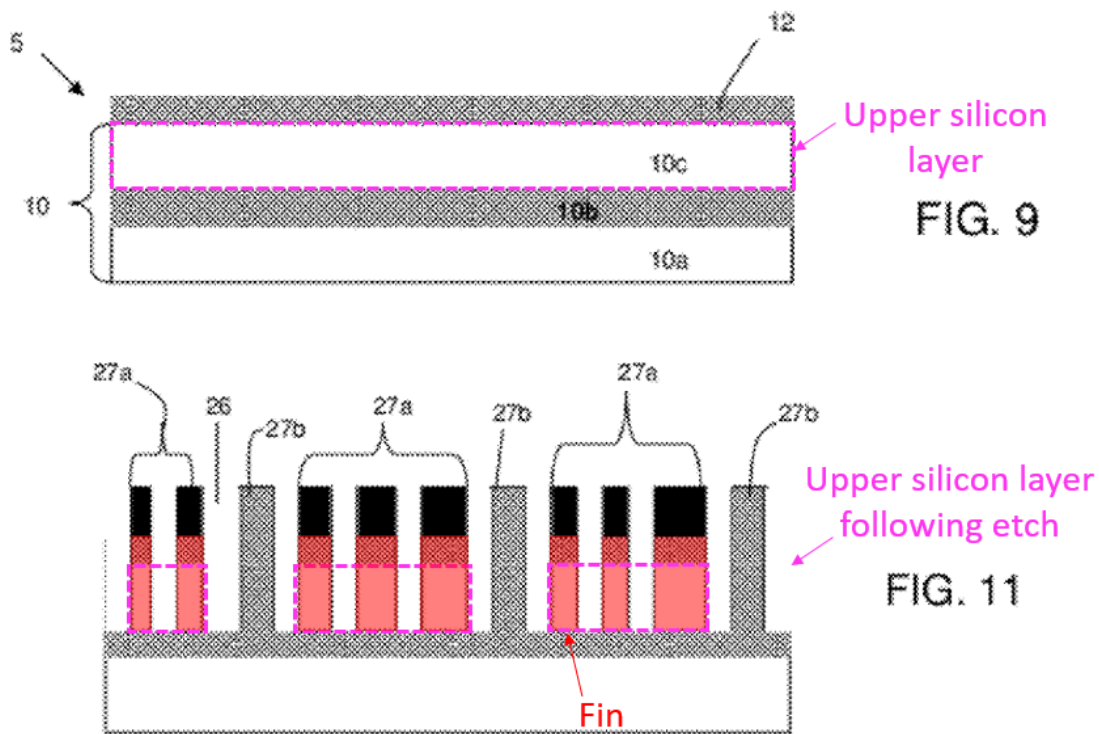


FIG. 15

Anderson-Lin top-view figure

Each fin has a **longest dimension along a first direction**, marked in the figures. This longest dimension is **along the first direction**: the longest dimension of the fins is traversed *as one moves along the fins in the first direction*, e.g., top to bottom in the top view, into the page in the cross-sectional view. SAMSUNG-1003, ¶131.

Also in the combination, **the fins comprise silicon**, as demonstrated by Anderson's fabrication process. SAMSUNG-1003, ¶132. Anderson's isolation structures 28a are formed on "a silicon on insulator (SOI) wafer" that includes "a buried oxide 10b sandwiched between a lower Si layer 10a and ***upper silicon layer 10c***." SAMSUNG-1006, [0032]-[0033], FIG. 9, *infra* (outlining the upper silicon layer in pink); *see* [0041]-[0042], FIG. 16. Trenches are etched through the upper silicon layer to the buried oxide. *See* SAMSUNG-1006, [0036], FIG. 11, *infra*. The remaining portions of the upper silicon layer following the etch and subsequent pad film removal constitute the isolation structures 28a (red). *See id.*, [0037], FIG. 12; *see* [0046], FIG. 21; claims 3, 15. That is, Anderson's isolation structures 28a (fins) include portions of a silicon layer, and thus they **include silicon**. SAMSUNG-1003, ¶132.

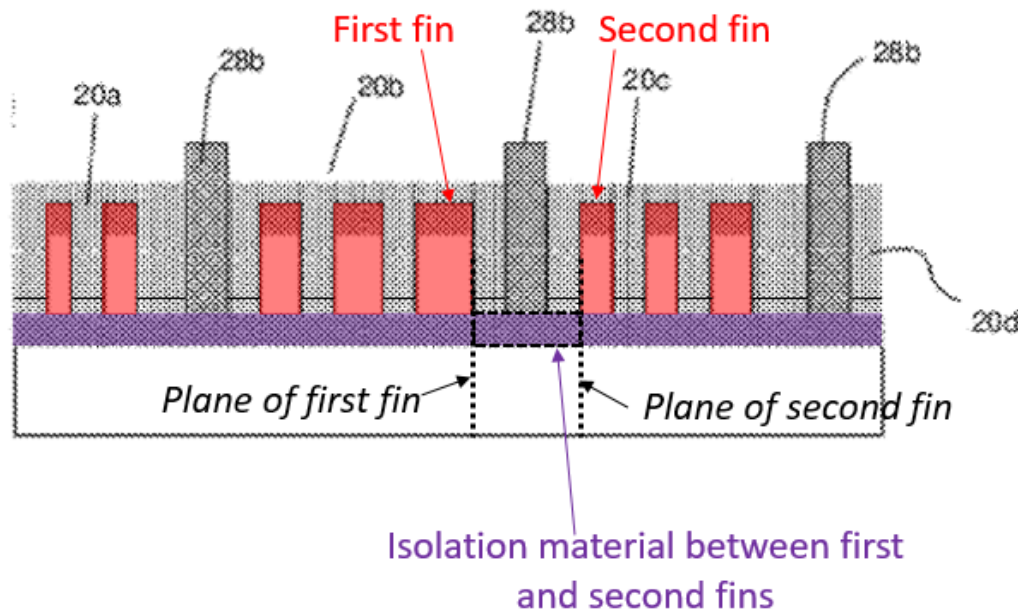


Excerpts from Anderson, FIGS. 9 and 11 (annotated)

Limitation [26c]

In the combination, Anderson's buried oxide layer is an isolation material

The Anderson-Lin combination includes **an isolation material**, e.g., Anderson's **buried oxide layer 10b**, purple in the figure *infra*. See SAMSUNG-1006, [0032] ("The SOI wafer can include **a buried oxide 10b** sandwiched between a lower Si layer 10 and upper silicon layer 10c"), [0036]-[0037], FIGS. 9-14. See Anderson's buried oxide layer 10b (e.g., **an isolation material**) of FIGS. 15-24 (*id.*, [0041]-[0045]); see FIG. 25, claims 3 and 15; SAMSUNG-1003, ¶133.



Anderson-Lin figure

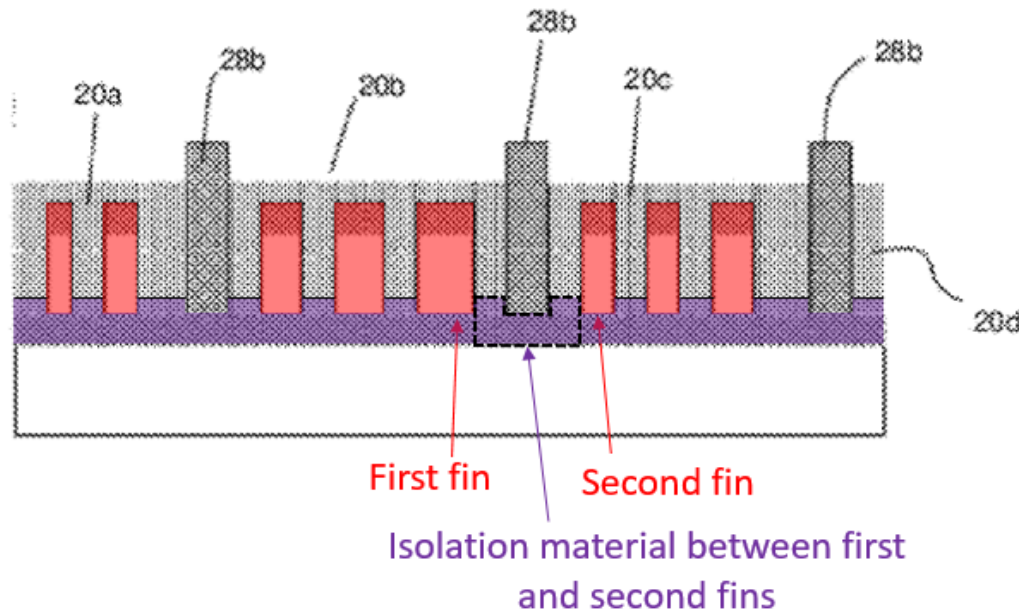
In the combination, the buried oxide layer 10b is **an isolation material** because it provides electrical isolation between fins. Anderson's buried oxide layer 10b is the oxide layer of an SOI wafer, and the fins are disposed on that oxide layer. *See* SAMSUNG-1006, [0032]-[0037], FIGS. 9-14; *see* [0041]-[0046], FIGS. 16-23. In FinFET devices, buried oxide layers of SOI wafers provide electrical isolation between fins. *See* SAMSUNG-1033, 2:19-21 ("Semiconductor devices are formed in and above the active layer of an SOI substrate. The fins are formed in the active layer and the buried insulation layer provides good isolation between adjacent fins"); SAMSUNG-1009, [0041]; SAMSUNG-1003, ¶134.

The buried oxide layer is **between the first fin and the second fin**: at least a portion of the buried oxide layer (outlined in dashes in the composite figure *supra*)

is disposed in the space separating the fins, *e.g.*, in the space between a vertical plane defined by the first fin and a vertical plane defined by the second fin (denoted in dotted lines *supra*). SAMSUNG-1003, ¶135.

In the combination, the buried oxide layer and the STI around the fins together are an isolation material

Alternatively or additionally, in the Anderson-Lin combination, a dielectric layer (*e.g.*, Lin's dielectric layer 114) is disposed on the buried oxide layer and around the base of the fins (*e.g.*, Anderson's isolation structures 28a) to provide STI. *See* SAMSUNG-1007, 2:55-62 ("The dielectric layer 114, which acts as a shallow trench isolation (STI) around the fins"), claim 1, claim 9, FIGS. 1A-5C; SAMSUNG-1003, ¶136. In the combination, the buried oxide layer and the dielectric layer, both purple in the figure *infra*, together are **an isolation material**. SAMSUNG-1003, ¶136.



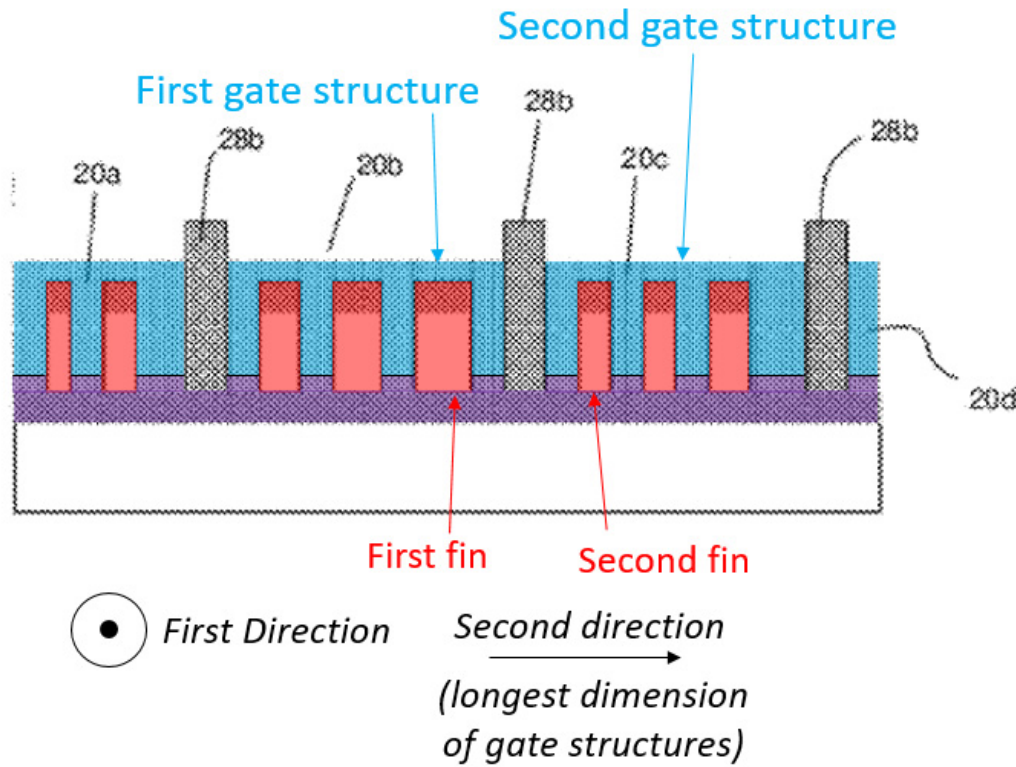
Anderson-Lin figure

The dielectric layer and the buried oxide layer are **an isolation material** because they electrically isolate fins. Lin describes that the dielectric layer “acts as a shallow trench isolation (STI) around the fins.” SAMSUNG-1007, 2:55-58. STI regions disposed around the base of fins in FinFET devices provide electrical isolation between those fins. *See* SAMSUNG-1005, 4:25-29 (“the trenches 22 are filled with a dielectric material to form the isolation regions 204 to define and electrically isolate the various fins of the fin structure 202. In one example, the isolation regions 204 include shallow trench isolation (STI) regions”); SAMSUNG-1010, 1:43-45; SAMSUNG-1031, 5:16-18; SAMSUNG-1034, 2:24-36; SAMSUNG-1035, 1:22-32; SAMSUNG-1003, ¶137. The buried oxide layer provides electrical isolation as discussed *supra*. SAMSUNG-1003, ¶137.

The isolation material (*e.g.*, the buried oxide layer and the STI material around the fins) is **between the first and second fin**: a portion of the isolation material (outlined in dashes in the figure *supra*) is disposed in the space separating the first and second fins, *e.g.*, in the space separating a vertical plane defined by the first fin and a vertical plane defined by the second fin. Specifically, the STI material is **between the fins**. *See* SAMSUNG-1007, 2:55-62 (“[t]he dielectric layer 114 ... acts as a shallow trench isolation (STI) *around the fins*”), claim 1, claim 9, Figs. 1A-5C. The buried oxide layer is also **between the fins** as discussed *supra*. SAMSUNG-1003, ¶138.

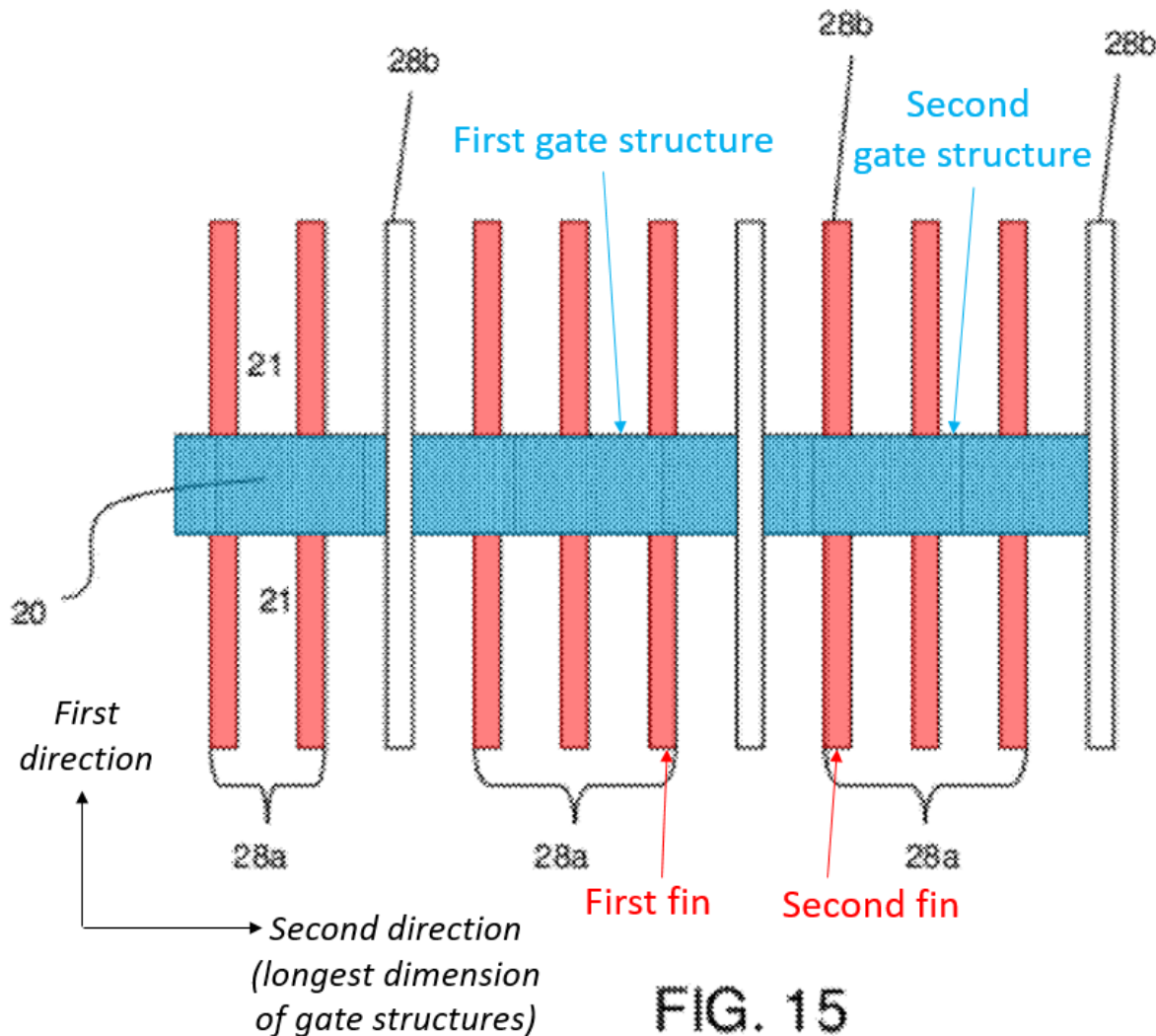
Limitations [26d] and [26e]

The Anderson-Lin combination includes **first and second gate structures**, *e.g.*, Anderson’s **gate stack 20**, blue in the figures *infra*. *See* SAMSUNG-1006, [0038]-[0039] (“**gate stack 20** is formed over the isolation structures 28a and 28b and the exposed portions of the wafer 10. ... [T]he gate electrode 20 is partially etched ... In this way, gates 20a-20d are formed on the wafer 20, separated by the isolation structures 28b.”), FIGS. 13-15. *See* Anderson’s “gate stack 20” (*e.g.*, **gate structures**) in FIGS. 23-24 (*id.*, [0047]-[0048]) and “electrically isolated gates 20e, 20f” (*e.g.*, **gate structures**) of FIGS. 25-26 (*id.*, [0051]); *see* [0005]-[0007], [0001], [0019]; SAMSUNG-1003, ¶139.



Anderson-Lin figure¹⁴

¹⁴ The cross-sectional composite figures in [26d] through [35] of Grounds 3A-3B identify both the buried oxide layer and the STI regions as isolation material by their purple highlighting. However, as discussed *supra*, the STI regions are an optional alternative and are not necessary to render obvious the features of the Challenged Claims. SAMSUNG -1003, ¶139.



Anderson-Lin figure

As illustrated *supra*, the gate structures have a **longest dimension along a second direction**: the longest dimension of the gate structures is traversed *as one moves along the gate structures in the second direction* (left to right in both figures). See SAMSUNG-1006, FIGS. 14-15, 23-26; SAMSUNG-1003, ¶140.

The composite figures also illustrate that **the second direction is orthogonal to the first direction**, *e.g.*, the gate stacks extend orthogonal to the

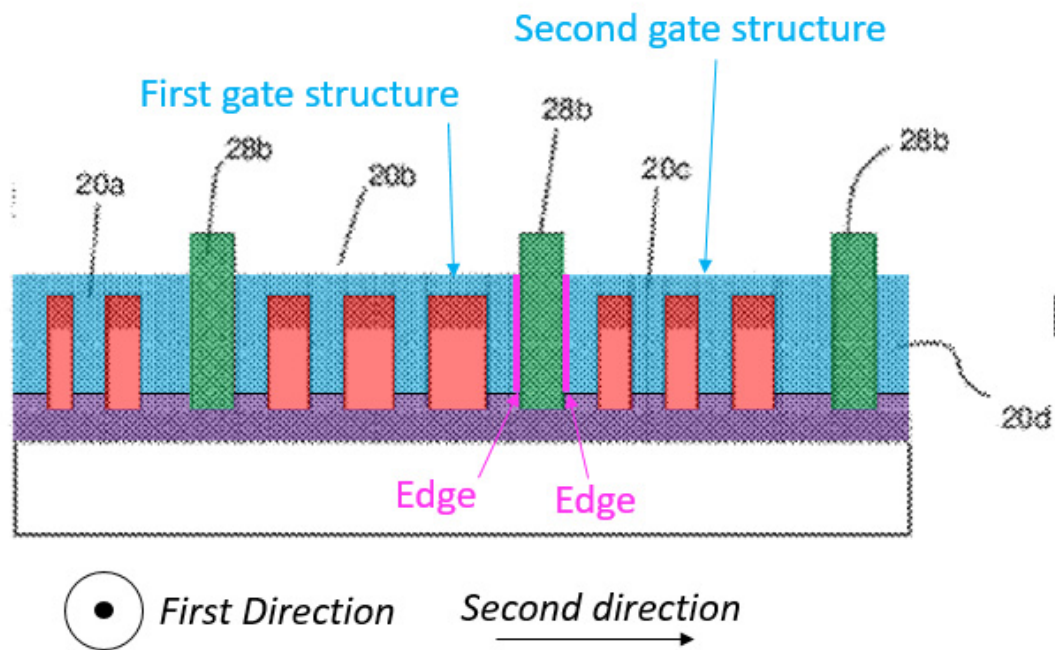
extension of the isolation structures 28a. *See* SAMSUNG-1006, FIGS. 14-15, 23-26; SAMSUNG-1003, ¶141. To the extent that Anderson does not explicitly state this orthogonality, a POSITA would have understood this to be the case, or otherwise found this to be obvious, consistent with the illustrations of Anderson's structure (*see* SAMSUNG-1006, FIGS. 14-15, 23-26) and given that gate structures orthogonal to fins in FinFET devices was well-known. *See, e.g.*, SAMSUNG-1008, [0053]; SAMSUNG-1029, [0042]; SAMSUNG-1030, Abstract; SAMSUNG-1003, ¶141.

The **first gate structure is over the first fin** and the **second gate structure is over the second fin**, as shown *supra*. Anderson describes that “gate stack 20 is formed *over the isolation structures 28a* and 28b ... The gate stack 20 can be, for example, a gate dielectric and a gate electrode material, *conformally deposited on the isolation structures 28a* and 28b.” SAMSUNG-1006, [0038]; *see* [0039] (“the gate electrode will *cover or bury the isolation structures 28a*”), [0047], [0005]-[0007], FIGS. 14-15, FIGS. 23-26; SAMSUNG-1003, ¶142.

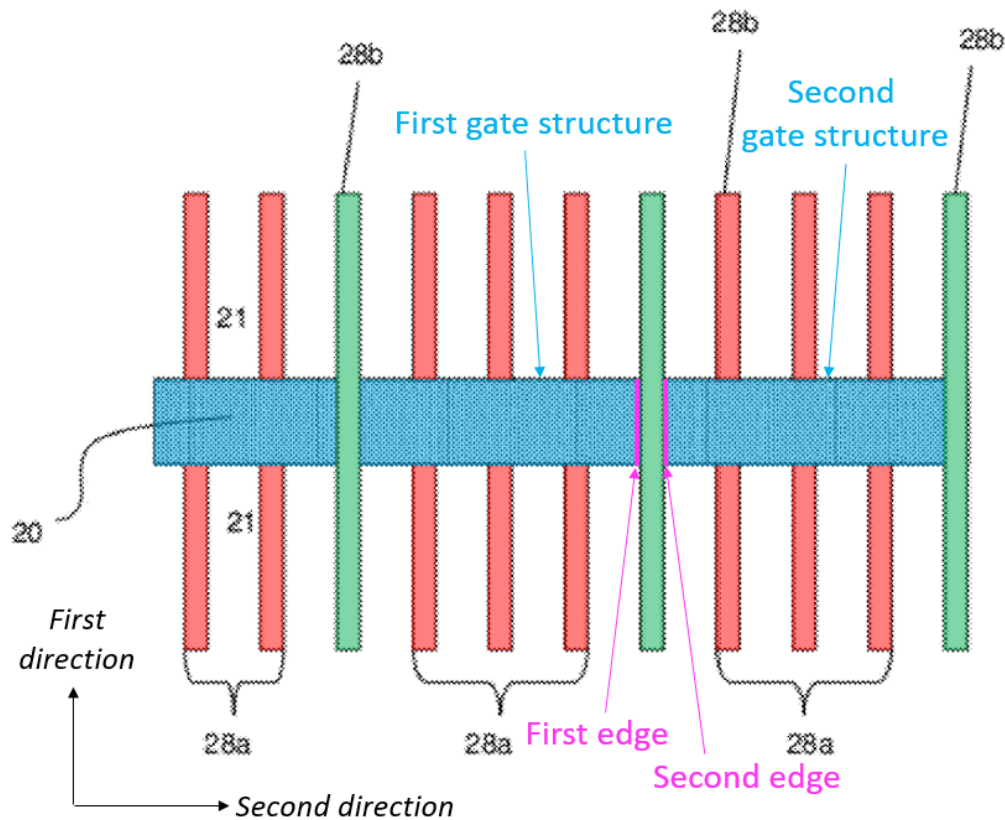
Moreover, in the combination, **the second gate structure is discontinuous with the first gate structure**, illustrated *infra*. The gate structures (*e.g.*, Anderson's gate stacks, blue) are **discontinuous** because they are separated by the isolation structure 28b (green; *see* [26f]): “gates 20a-20d are formed on the wafer 20, *separated by the isolation structures 28b*.” SAMSUNG-1006, [0039]; *see*

[0048]. Specifically, “the gates abut against the sides of the isolation structure 28b, which will provide *a physical and electrical separation between the gates.*”

Id., [0039]; *see* [0048], [0051], [0019], [0005]-, [0001], FIGS. 14-15, FIGS. 23-26; SAMSUNG-1003, ¶143.



Anderson-Lin figure



Anderson-Lin figure

The discontinuity between the gate structures is **along the second direction**: the discontinuity is reached *as one moves in the second direction* from one gate structure to the other (left to right in the figures). See SAMSUNG-1006, FIGS. 14-15, 23-26; SAMSUNG-1003, ¶144.

The figures *supra* also illustrate that **the second gate structure has an edge** (outlined in pink) **that faces an edge of the first gate structure** (also pink), *e.g.*, the edges of the gate structures that contact the isolation structure 28b face one another. See SAMSUNG-1006, [0039] (“*the gates abut against the sides of the*

isolation structure 28b”), FIGS. 14-15; *see* [0048], [0005]-[0007], [0031], FIGS. 23-26; SAMSUNG-1003, ¶145.

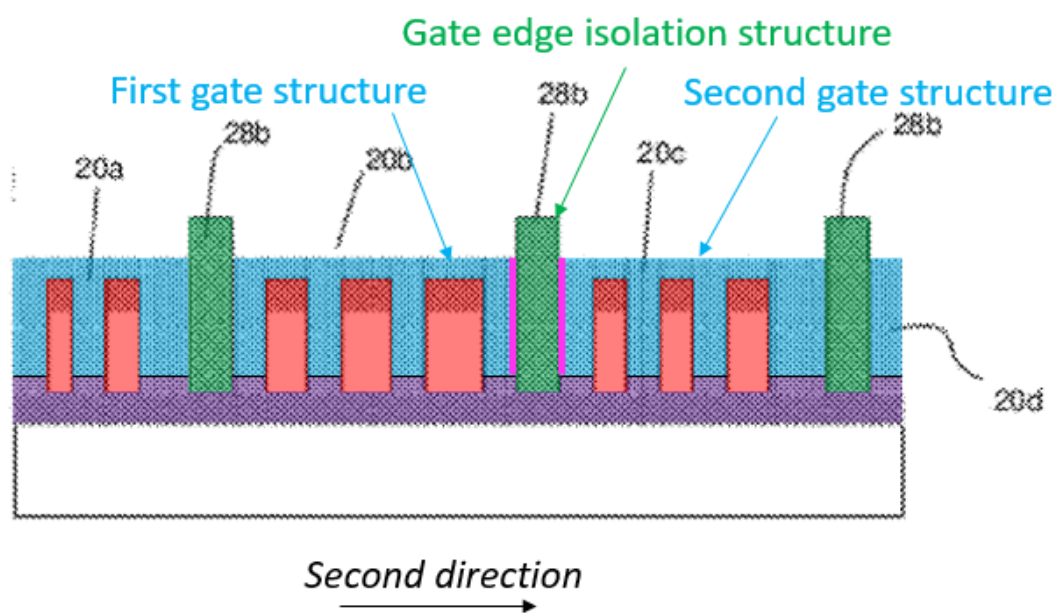
The edges face one another **along the second direction**: from the edge of the second gate structure, the edge of the first gate structure is reached *as one moves in the second direction* (left to right in the figures). SAMSUNG-1003, ¶146.

In the combination, Anderson describes that the gate structures (*e.g.*, Anderson’s gate stack) each includes **a gate dielectric layer and a gate electrode**. *See* SAMSUNG-1006, [0038] (“The gate stack 20 can be, for example, *a gate dielectric and a gate electrode material*”), [0047]; SAMSUNG-1003, ¶147.

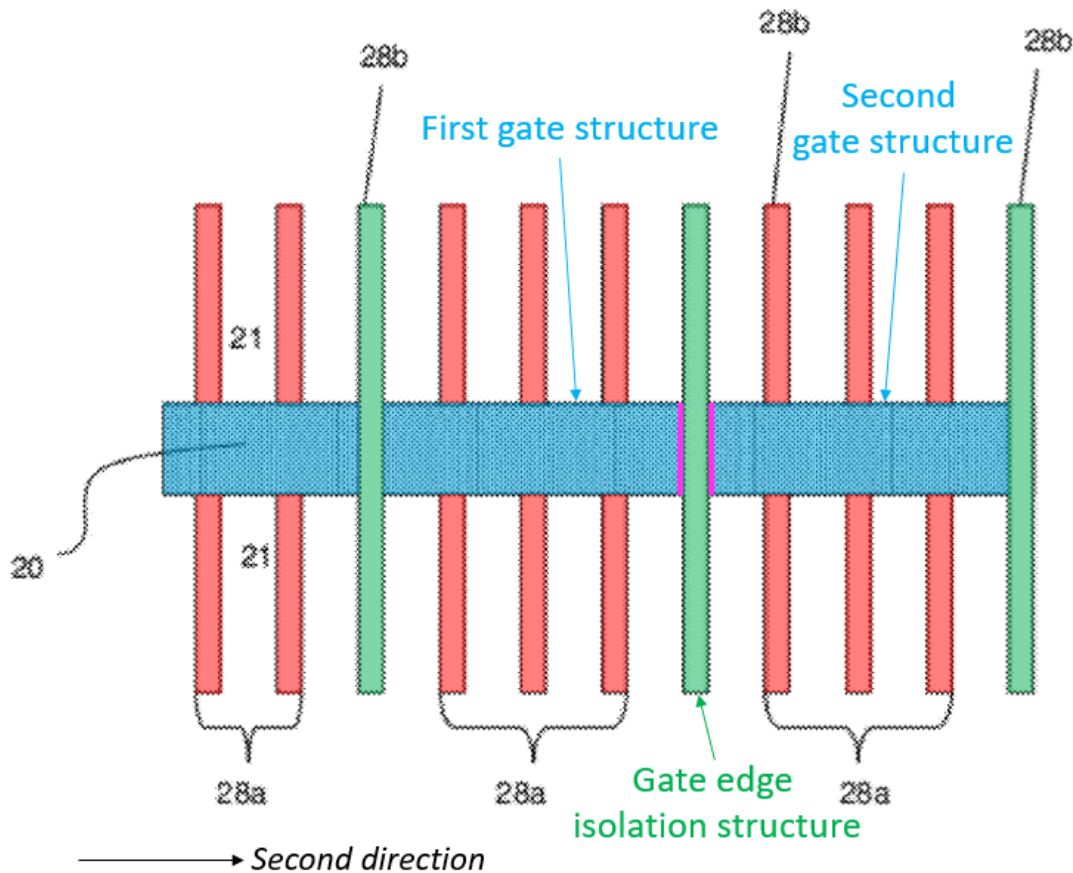
Limitation [26f]

The Anderson-Lin combination includes a gate edge isolation structure

The Anderson-Lin combination includes **a gate edge isolation structure**, *e.g.*, Anderson’s *isolation structure 28b*, green in the figures *infra*. *See* SAMSUNG-1006, [0037] (“dual height isolation structures 28a and 28b,” where “*the isolation structure 28b* is taller than the surrounding isolation structures 28a”), [0038]-[0040], FIGS. 11-15. *See* Anderson’s “isolation structure[] ... 28b” (*e.g.*, **a gate edge isolation structure**) in FIGS. 19-24 (*id.*, [0047]-[0048]) and “isolation structure 28b” (*e.g.*, **a gate edge isolation structure**) in FIGS. 25-26 (*see id.*, [0051]); *see* [0001], [0005]-[0007], [0019]; SAMSUNG-1003, ¶148.



Anderson-Lin figure



Anderson-Lin figure

In the combination, Anderson's isolation structure (*e.g.*, isolation structure 28b) is a **gate edge isolation structure**: it is disposed between the edges of the gate structures (discussed *infra*) and isolates those gate structures from one another (*e.g.*, physically and electrically). SAMSUNG-1003, ¶149.

Anderson's isolation structure 28b both ***physically isolates*** and ***electrically isolates*** the gate structures. Anderson describes that the isolation structure 28b provides "***a physical and electrical separation between the gates 20a-20d,***"

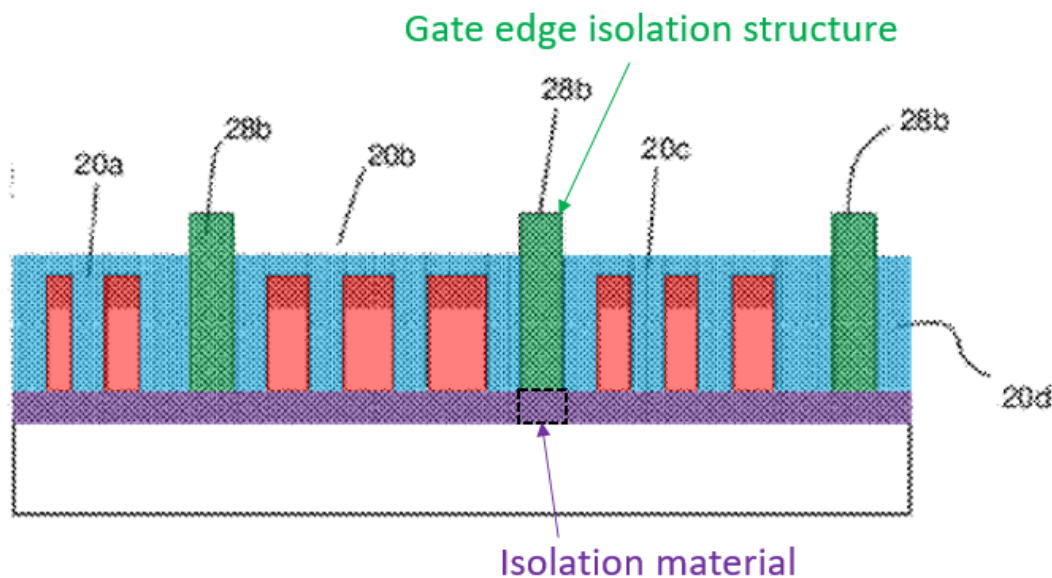
“allow[ing] adjacent gates to be isolated.” SAMSUNG-1006, [0039]; *see* [0048], [0051], [0001], [0019], [0040], [0050]; SAMSUNG-1003, ¶150.

As shown *supra*, the gate edge isolation structure is between and in contact with the edge of the first gate structure and the edge of the second gate structure, *e.g.*, Anderson’s isolation structure 28b (green) is between and in contact with the edges (pink) of the gates (blue). Anderson describes this configuration: “gates 20a-20d are ... *separated by the isolation structures* ... [and] the gates *abut against the sides of the isolation structure 28b*.” SAMSUNG-1006, [0039]; *see* [0048], [0006], [0007], FIGS. 14-15, 23-26; SAMSUNG-1003, ¶151. Moreover, as discussed by Dr. Liu, the positioning of the edge of Anderson’s isolation structure 28b is **in contact with the edges of the gate structures** in the combination is further revealed by Anderson’s fabrication process. *See* SAMSUNG-1006, [0036]-[0038], [0045]-[0047], FIGS. 11-14, FIGS. 23-26; SAMSUNG-1003, ¶152.

The gate edge isolation structure is between and in contact with the edges of the gate structures **along the second direction: *as one moves in the second direction*** (*e.g.*, left to right in the figures) starting from the edge of the first gate structure, one reaches first the gate edge isolation structure and then the edge of the second gate structure. SAMSUNG-1003, ¶153.

The gate edge isolation structure is over the isolation material

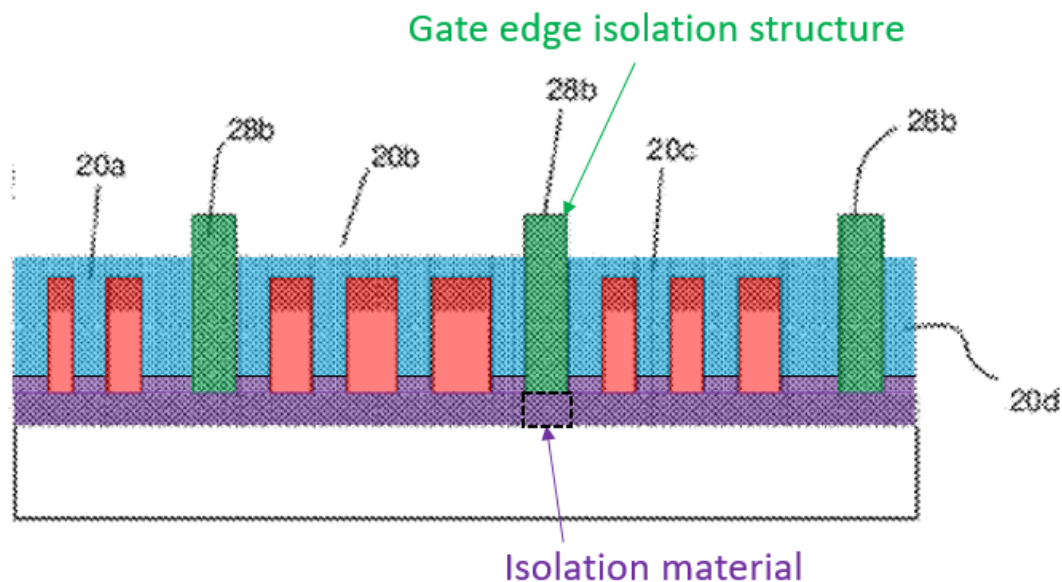
As shown *infra*, in the combination, when the isolation material (purple) is a buried oxide layer (*see* [26c]), **the gate edge isolation structure is over the isolation material**, *e.g.*, at least the portion of the isolation material outlined in dashes. SAMSUNG-1003, ¶154.



Anderson-Lin figure

The positioning of the gate edge isolation structure **over the isolation material** (*e.g.*, over the buried oxide layer) is further revealed by Anderson's fabrication process, in which the isolation structure 28b (*e.g.*, the gate edge isolation structure) are formed by etching trenches in a silicon layer that sits on the buried oxide layer 10b. *See id.*, [0032], [0036]-[0037], [0045]-[0046], FIGS. 9, 11, 16, FIGS. 20-21; SAMSUNG-1003, ¶155.

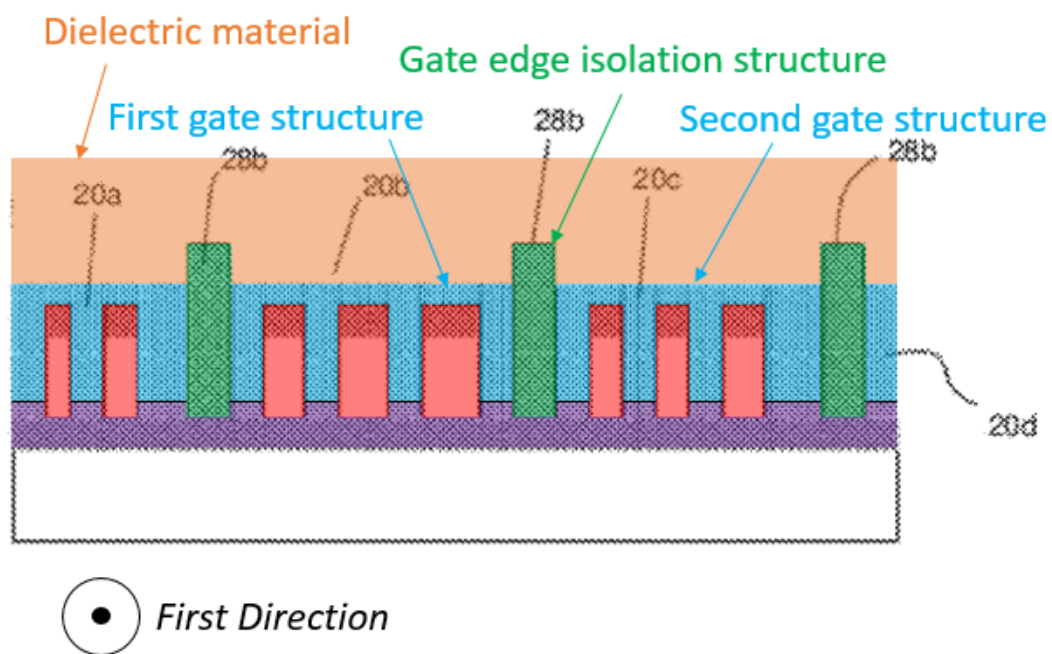
Alternatively or additionally, as shown *infra*, when the isolation material (purple) is both the buried oxide layer and the STI regions around the base of the fins (see [26c]), **the gate edge isolation structure is over the isolation material**, e.g., at least the portion of the isolation material outlined in dashes. SAMSUNG-1003, ¶156.



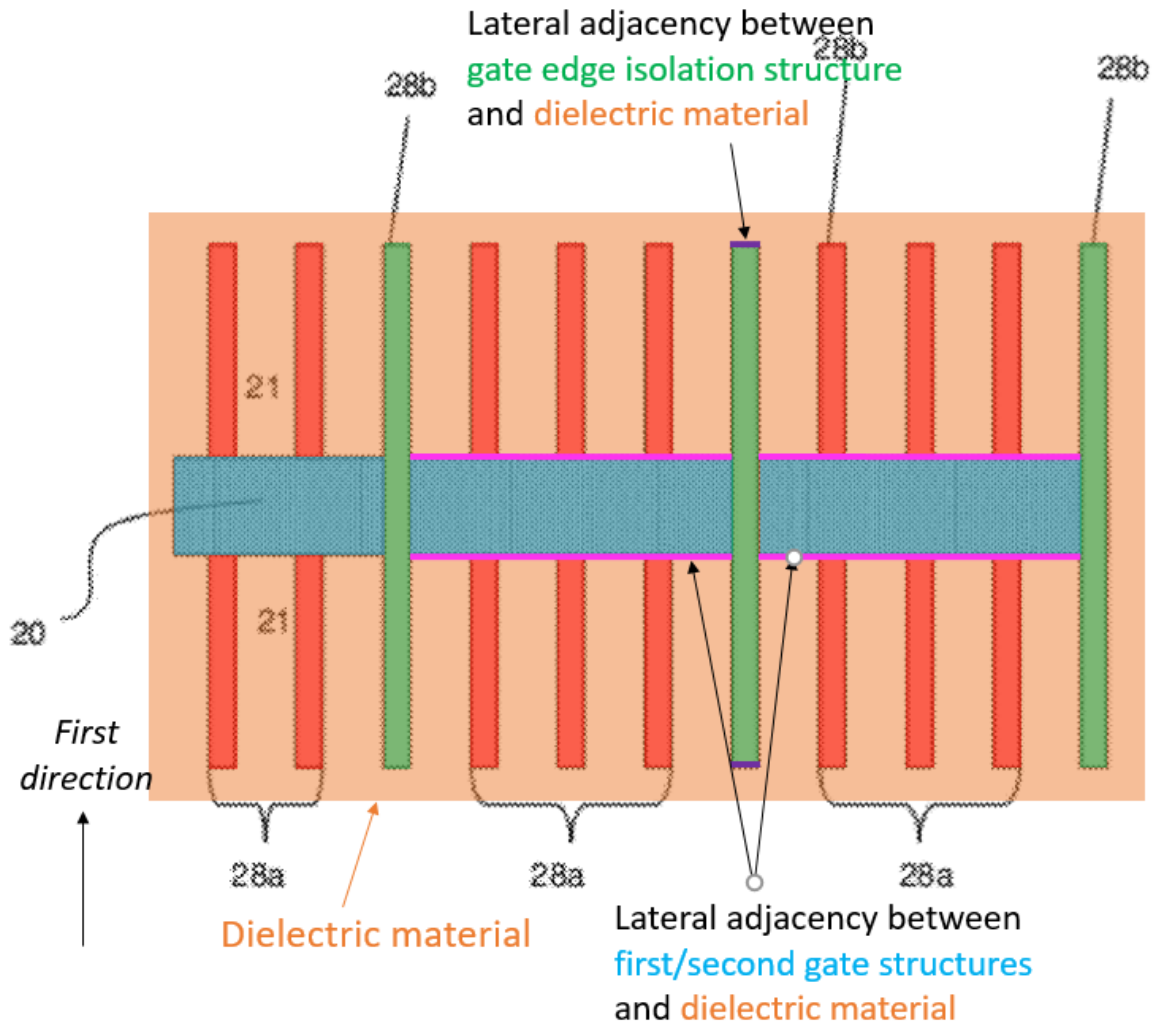
Anderson-Lin figure

Limitation [26g]

In the Anderson-Lin combination, based on Lin, “*an inter-layer dielectric (ILD)*,” orange in the figure *infra*, is “formed over the gate electrodes” (blue) and over the gate edge isolation structure (green). SAMSUNG-1007, 5:15-17; *see* claims 9-10, FIGS. 5A-5C; *see* SAMSUNG-1006, [0050]; SAMSUNG-1003, ¶157. In the combination, the ILD is **a dielectric material**. SAMSUNG-1003, ¶157.



Anderson-Lin figure



Anderson-Lin figure

The sidewalls of the gate structures are outlined in pink in the top view figure *supra*. See SAMSUNG-1006, FIG. 15; see FIGS 24, 26. These sidewalls extend into the page of the top view, and the dielectric material fills the space next to those sidewalls. See *id.*, FIG. 14; see FIGS. 23, 25; SAMSUNG-1003, ¶158. The **dielectric material is laterally adjacent to the first and second gate structures** at least at these pink-outlined sidewalls. See SAMSUNG-1006, FIGS.

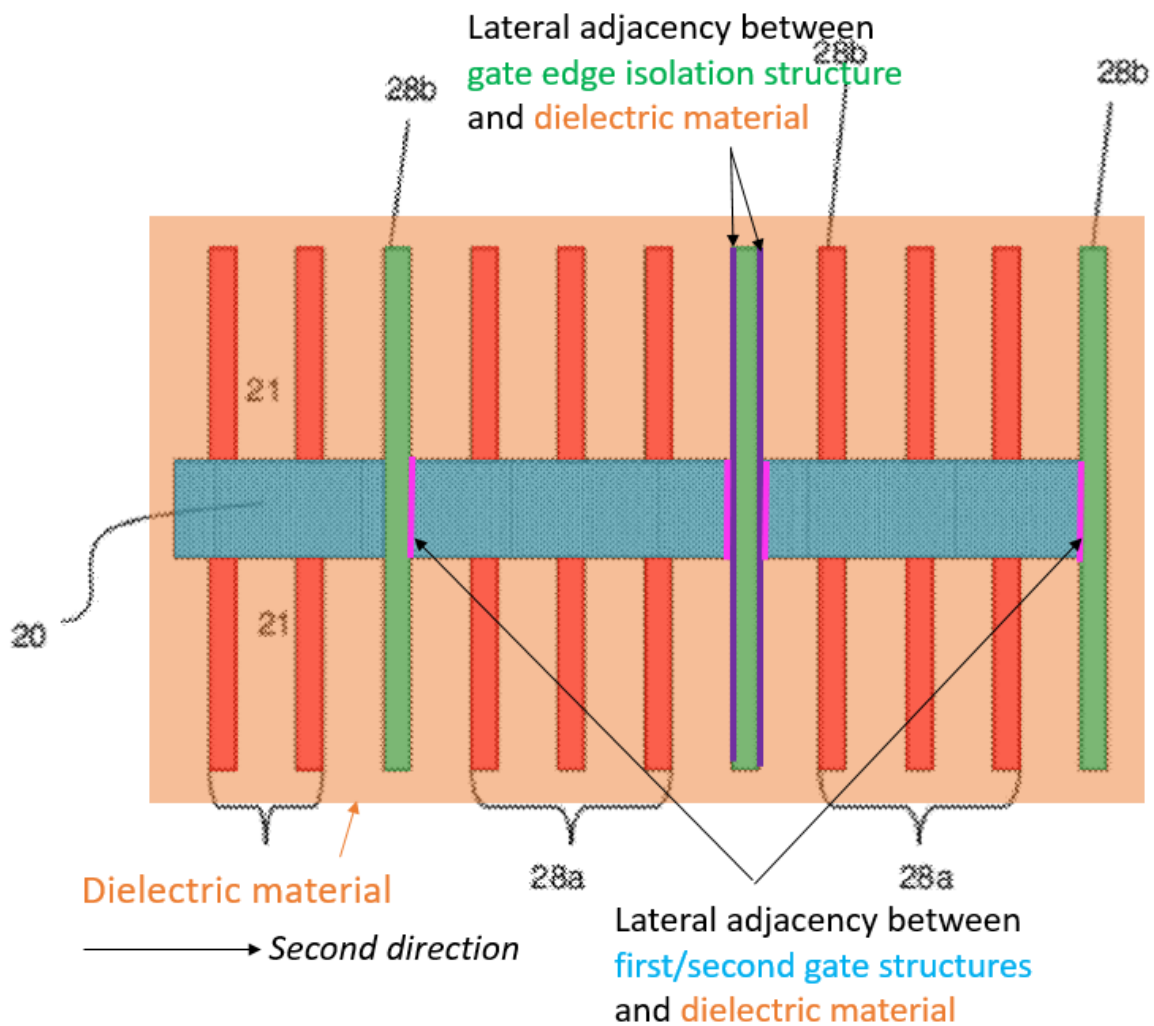
14-15, 23-26; SAMSUNG-1003, ¶158. For instance, the dielectric material is near (*e.g.*, next to) the gate structure sidewalls.

The short end walls of the gate edge isolation structure are outlined in purple in the top-view figure *supra*. See SAMSUNG-1006, FIG. 15; see FIGS 24, 26. These walls extend into the page of the top-view figure. As shown in the cross-sectional view, the dielectric layer fills the space next to these end walls. See *id.*, FIG. 14; see FIGS. 23, 25; SAMSUNG-1003, ¶160. The **dielectric material is laterally adjacent to the gate edge isolation structure** at least at these purple-outlined end walls. SAMSUNG-1003, ¶160.

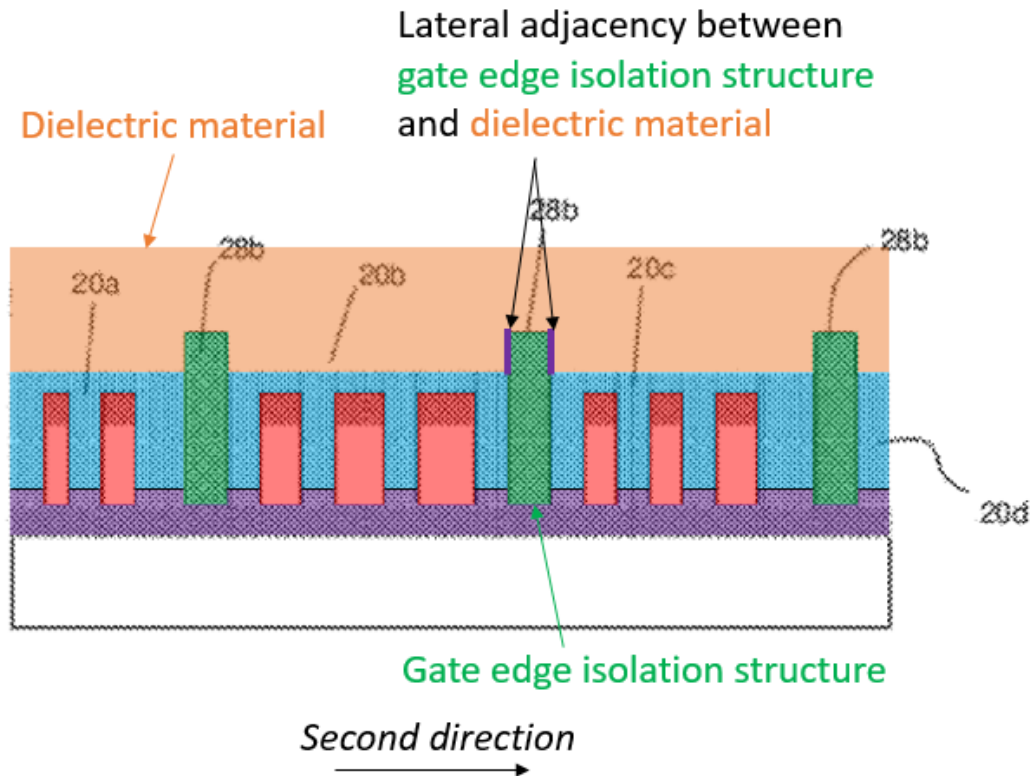
The dielectric material is laterally adjacent to the gate structures and gate edge isolation structure **along the first direction**: viewing the structure starting from either of the gate structures or from the gate edge isolation structure and ***moving along the first direction*** (top to bottom in the top-view figure), one reaches the dielectric material. See SAMSUNG-1006, FIGS. 14-15, 23-26; SAMSUNG-1003, ¶¶159, 161.

Alternatively or additionally, the dielectric material is laterally adjacent to the gate structures and the gate edge isolation structure at the pink-outlined and purple-outlined edges, respectively, in the alternative figures *infra*. SAMSUNG-1003, ¶¶162-163. To the extent this spatial relationship is considered to be laterally adjacent **along the first direction**, the dielectric material is laterally

adjacent to the gate structures and the gate edge isolation structure along the first direction. SAMSUNG-1003, ¶¶162-163.



Anderson-Lin figure (alternative)



Anderson-Lin figure (alternative)

Also in the combination, **the dielectric material** (e.g., the ILD) is **discrete from the gate edge isolation structure** (e.g., the isolation structure 28b) at least because *they are formed in two distinct processing steps*. The dielectric material is deposited over the gate structures (see SAMSUNG-1007, 5:15-17), which are formed after fabrication of the gate edge isolation structure (see SAMSUNG-1006, [0038]). See *id.*, [0032]-[0038], [0041]-[0047], [0050]; SAMSUNG-1003, ¶164.

Alternatively or additionally, **the dielectric material is discrete from the gate edge isolation structure** at least because *they are composed of two different materials*. The dielectric material (e.g., Lin's ILD 560) can be "formed of an

oxide such as phospho-silicate glass (PSG), boro-silicate glass (BSG), boron-doped phospho-silicate glass (BPSG), TEOS, or the like.” SAMSUNG-1007, 5:15-20.

The gate edge isolation structure (*e.g.*, Anderson’s isolation structure 28b) includes SiO₂—a different material. *See* SAMSUNG-1006, [0035] (“the trenches are filled with an insulator material to form isolation structures 24. In embodiments, the insulator material is SiO₂.”), [0036]-[0037], FIGS. 10-12; *see* [0041]-[0046] (describing a fabrication process in which the gate edge isolation structure includes silicon and silicon nitride); FIGS. 16-21; *see* [27]; SAMSUNG-1003, ¶165.

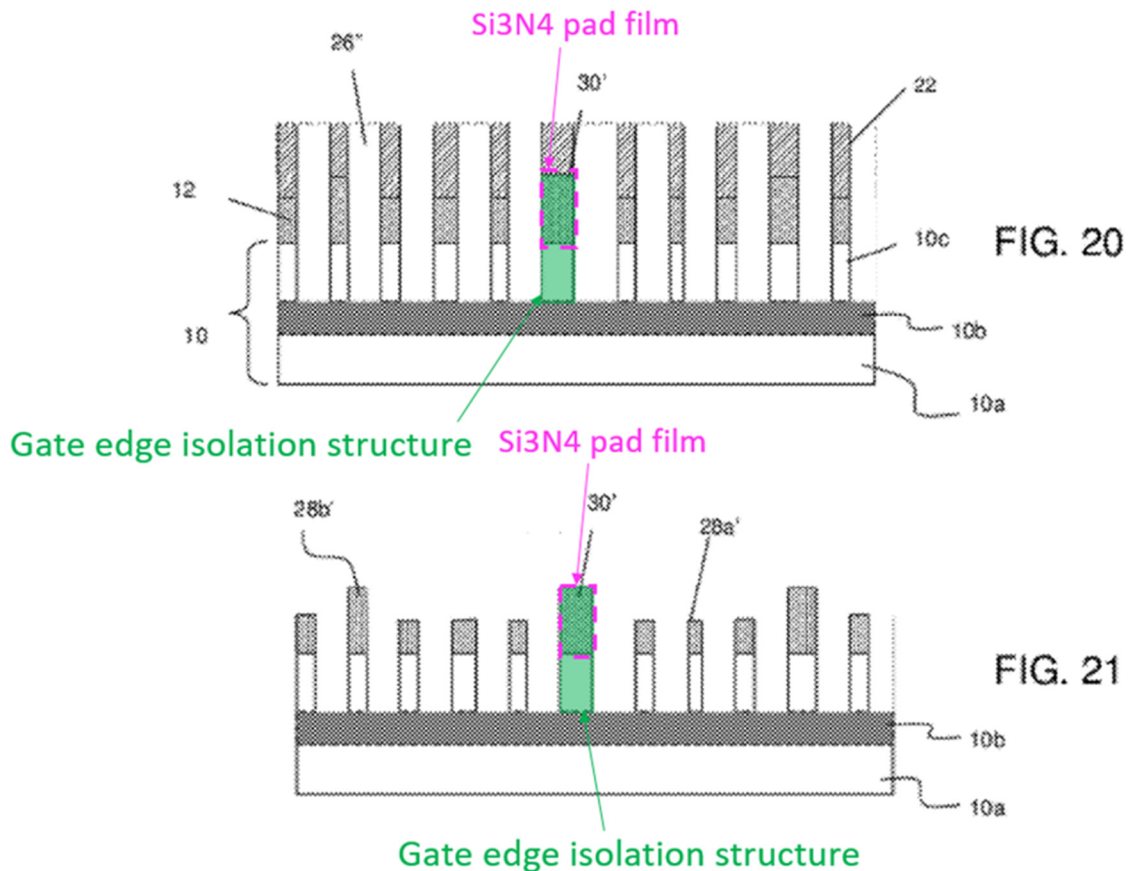
(2) Claim 27

Limitation [27]

In the combination, when the gate edge isolation structure is based on Anderson’s “isolation structure[] ... 28b” (SAMSUNG-1006, [0047]-[0048], FIGS. 19-24; *see* [26f]), **the gate edge isolation structure comprises silicon and nitrogen**, as demonstrated by Anderson’s description of the fabrication process. SAMSUNG-1003, ¶166.

As shown in FIG. 20, *infra*, “trenches 26’ are formed in [] pad films 12, 22,” where “the pad film 12 can be a stack material such as ... Si₃N₄.” SAMSUNG-1006, [0042], [0044]. A portion of the Si₃N₄ pad film 12 is outlined in pink. The trenches 26’ are separated by fins 27’, which are composed of the pad film 22, the Si₃N₄ pad film 12, and a silicon layer 10c. *See id.*, [0041], [0044]-[0045]. These

fins 27' ultimately become the isolation structures 28b' (e.g., the gate edge isolation structure, green). *Id.*, [0045]. Thus, the isolation structure 28b' (e.g., the gate edge isolation structure) includes Si_3N_4 , i.e., **silicon and nitrogen**. SAMSUNG-1003, ¶167.



Excerpt from Anderson, FIGS. 20-21 (annotated)

(3) Claim 28

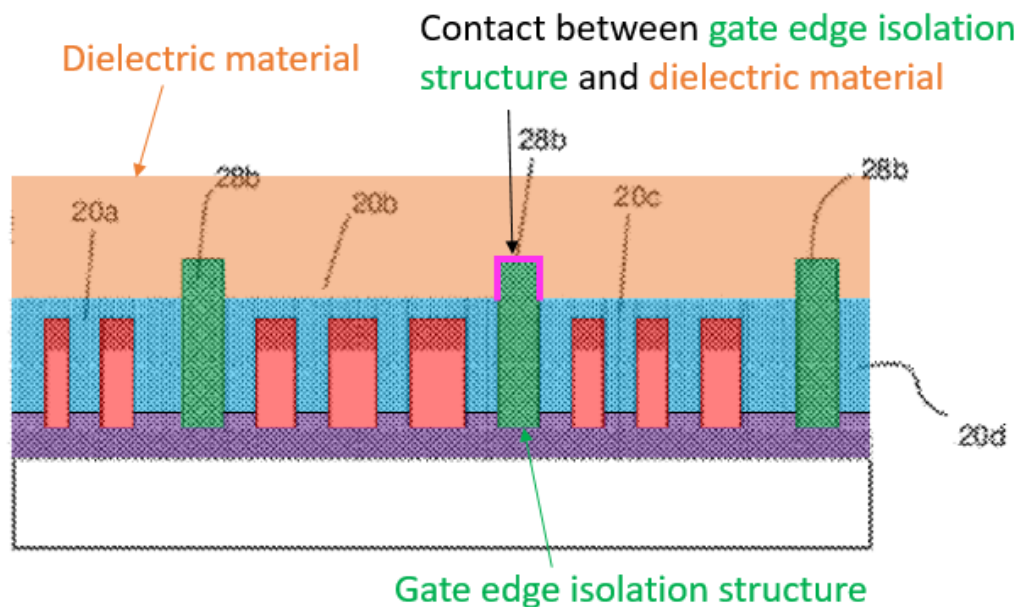
Limitation [28]

In the combination, the dielectric material (e.g., an ILD) is “formed over the gate electrodes” and over the gate edge isolation structure. SAMSUNG-1007,

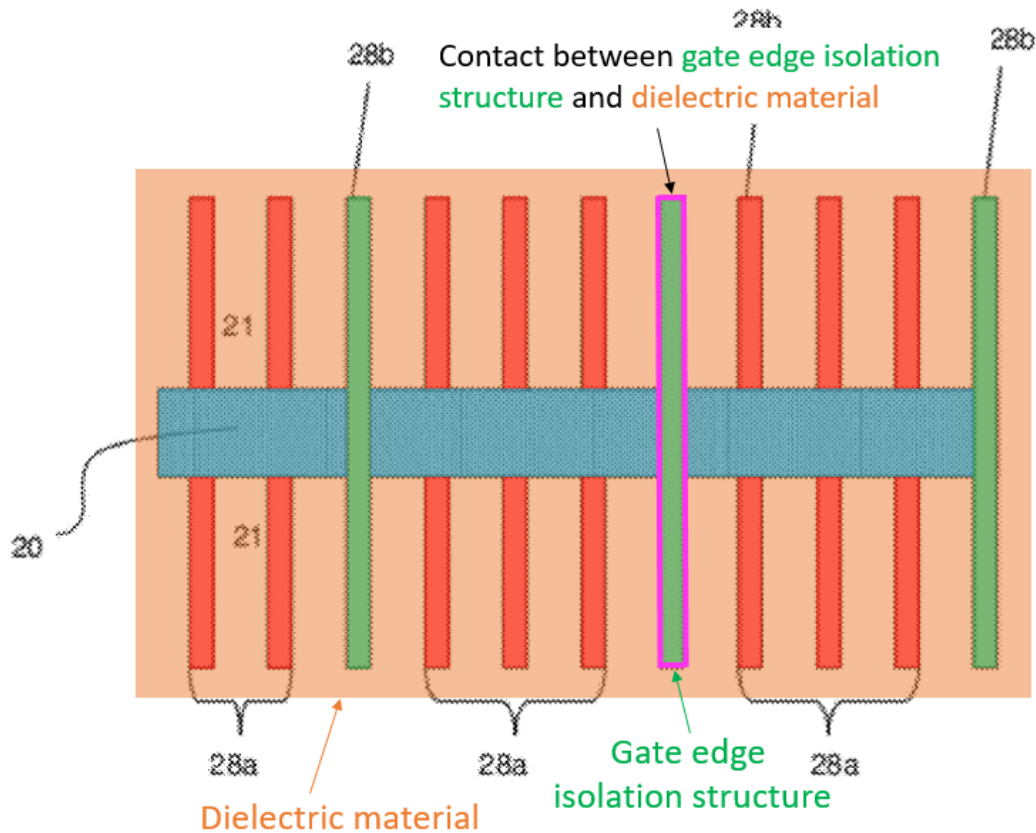
5:15-17. Thus, **the dielectric material is in contact with the gate edge isolation structure** at least on the top surface of the gate edge isolation structure and on the exposed sidewalls and end surfaces of the gate edge isolation structure. *See* [26g].

These surfaces of contact between the dielectric material (orange) and the gate edge isolation structure (green) are outlined in pink in the figures *infra*.

SAMSUNG-1003, ¶168.



Anderson-Lin figure



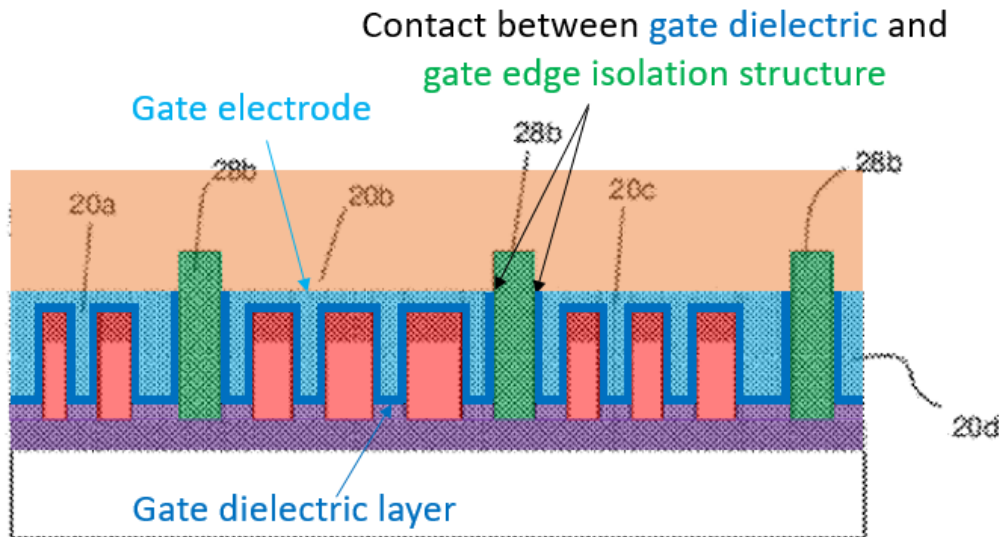
Anderson-Lin figure

(4) Claim 29

Limitation [29]

In the combination, the gate structure is a “gate stack” that includes “a gate dielectric and a gate electrode material, conformally deposited on the isolation structures ... 28b” and “partially etched away to expose the isolation structure 28b.” SAMSUNG-1006, [0038]-[0039]; *see* [0047]. A POSITA would have understood or found obvious that Anderson’s deposition of a gate stack involves first depositing the gate dielectric, resulting in the gate dielectric coating the exposed surfaces of the fins and the gate edge isolation structures 28b, followed by

deposition of the gate electrode. *See* SAMSUNG-1025, 4:39-5:56; SAMSUNG-1005, 8:62-9:4; SAMSUNG-1012, 11:4-14; SAMSUNG-1014, 7:8-42; SAMSUNG-1003, ¶169. As such, and as shown *infra*, **the gate edge isolation structure is in contact with the gate dielectric layer of each gate structure, e.g.,** at least a portion of the sidewall of the gate edge isolation structure is in contact with the gate dielectric layer. SAMSUNG-1003, ¶169.



Anderson-Lin composite figure

(5) Claim 31

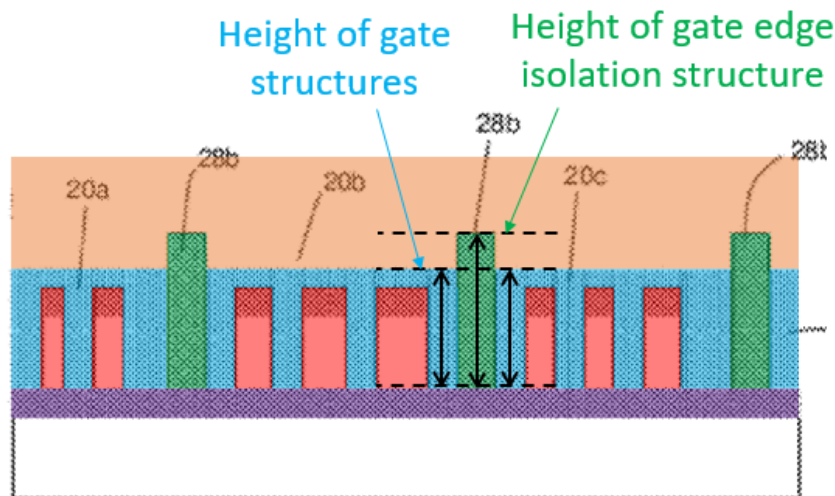
Limitation [31]

In the combination, the gate dielectric layers of the gate structures (*e.g.*, Anderson's gate stacks 20; *see* [26d]-[26e]) include **a high-k dielectric material**. *See* SAMSUNG-1006, [0038] ("the gate dielectric can be, for example, **a high-k dielectric material**"), [0047]; SAMSUNG-1003, ¶170.

(6) Claim 32

Limitation [32]

As illustrated *infra*, in the combination, **the gate edge isolation structure (green) has a height greater than the height of each of the gate structures (blue)**. The heights of the gate edge isolation structure and the gate structures are indicated from its interface with the buried oxide layer. With the inclusion of the STI regions (*see* [26c]), the vertical extent of the gate structures would be even less than that shown *infra*. Under either alternative, the height of the gate edge isolation structure is greater than the height of the gate structures. SAMSUNG-1003, ¶171.



Anderson-Lin figure

Moreover, Anderson describes that “the isolation structure 28b is taller than the surrounding isolation structures 28a.” SAMSUNG-1006, [0037], FIG. 14; *see* [0046], FIGS. 23 and 25. To form the gates, “the gate electrode 20 is partially

etched away to *expose the isolation structure 28b.*” SAMSUNG-1006, [0039]; *see* [0048]. Specifically, the “gate electrode structure [is] of a height greater than the short fin structure and *less than the tall fin structure,*” consistent with the relative heights of the structures illustrated in Anderson’s FIG. 14. SAMSUNG-1006, [0051]; *see* [0005]-[0007]; SAMSUNG-1003, ¶172.

**D. [GROUND 3B] – CLAIMS 33-35 ARE OBVIOUS OVER
ANDERSON, LIN, AND KAWA**

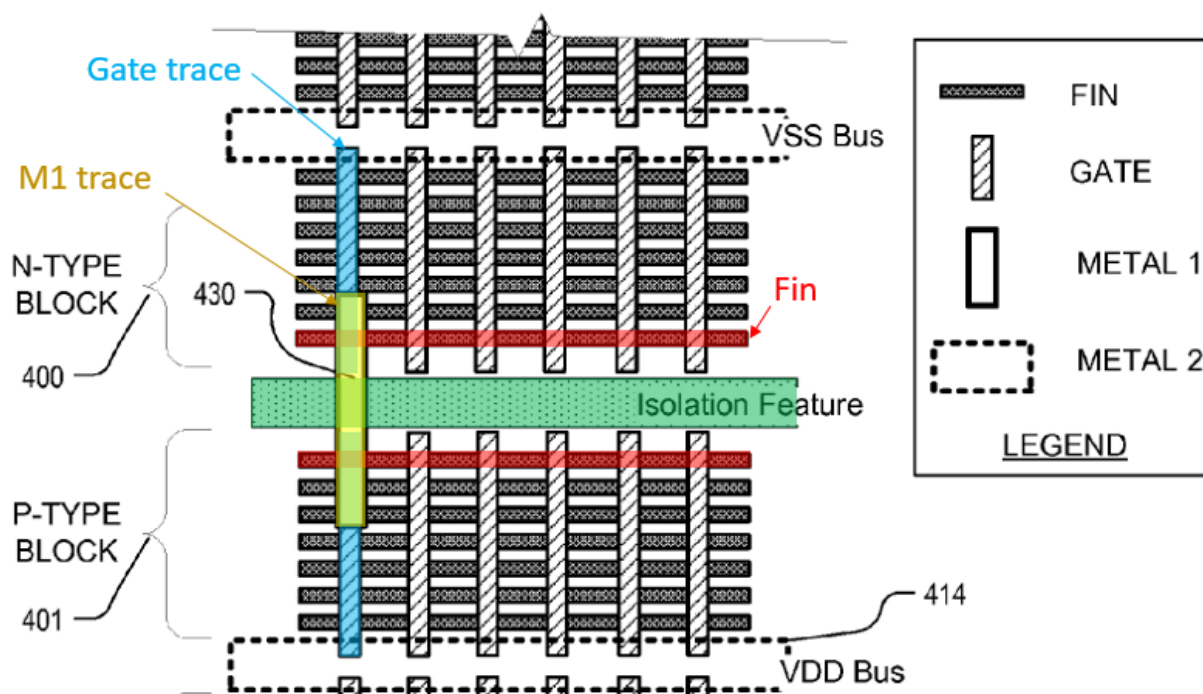
The sections below provide a brief introduction to Kawa and its combination with Anderson and Lin.¹⁵

**1. Kawa describes local interconnects connecting gates of
FinFET transistors**

Kawa describes “[i]ntegrated circuits including cells comprising finFET blocks.” SAMSUNG-1008, [0006]; *see* FIGS. 4-5, *infra*. FIG. 5 is a cross-sectional view “taken along the gate traces” in a region “spanning between a p-type block and an n-type block” of the top view FIG. 4. *Id.*, [0060]; *see* [0049]; SAMSUNG-1003, ¶173.

¹⁵ Petitioner incorporates this discussion into Ground 3B.

FIG. 4



Excerpt from Kawa, FIG. 4 (annotated)

Excerpt from Kawa, FIG. 5 (annotated)

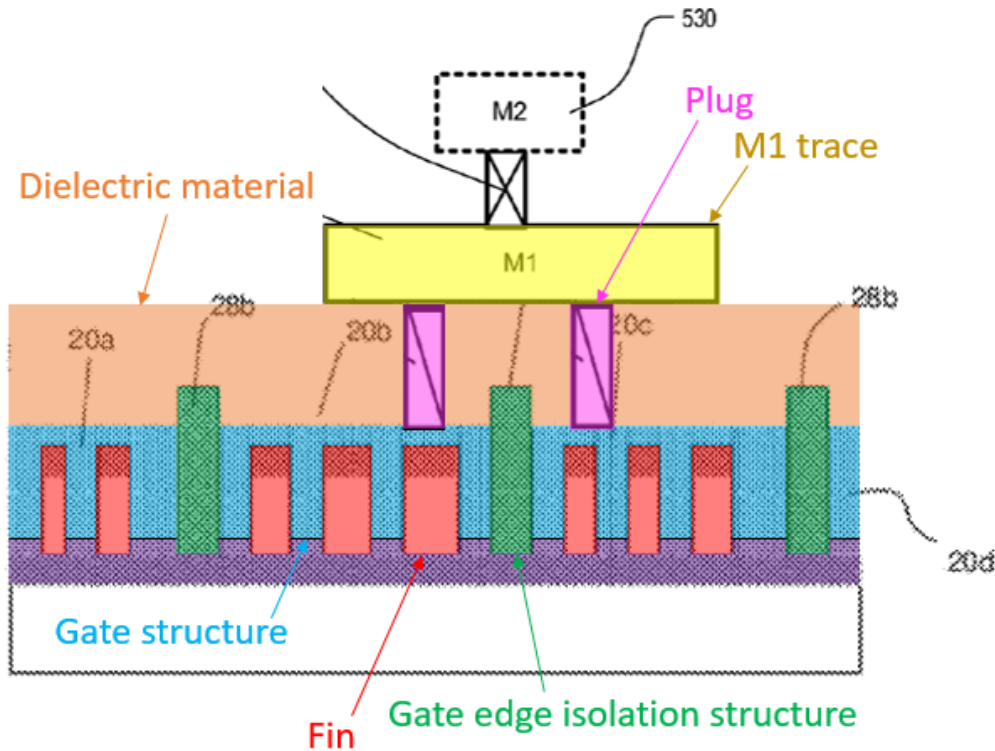
99

An “insulating fill 515,” orange, “provides an interlayer insulator layer between the patterned gate conductor layer ... and overlying patterned conductor layers.” SAMSUNG-1008, [0068]. These overlying layers include a “patterned conductor layer M1” (*e.g.*, M1 trace 520 in Fig. 5, M1 trace 430 in Fig. 4), yellow, that connects gate traces in different blocks, *e.g.*, gate traces 505, 506, “passing over the isolation structure.” *Id.*, [0057]; *see* [0068]. “[P]lugs 521 and 522,” pink, “extend through vias in the insulating fill 515 to connect gate traces 505 and 506, respectively,” to the M1 trace. *Id.*, [0068]; *see* [0057], Fig. 4 (showing M1 trace 430); SAMSUNG-1003, ¶175.

2. The Anderson-Lin-Kawa combination

In the Anderson-Lin-Kawa combination, Anderson describes that “contacts can be connected to the source/drain and gate electrodes using conventional etching and metal deposition processes.” SAMSUNG-1006, [0050]. These connections are implemented based on Kawa, as shown *infra*. SAMSUNG-1003, ¶176. The Anderson-Lin-Kawa combination includes a patterned M1 trace (yellow) that “overlie[s] the patterned gate conductor layer” (blue) and is “arranged parallel to the gate traces.” SAMSUNG-1008, [0057]; *see* [0068]. The M1 trace in the combination connects the first and second gate structures, “passing over” the isolation structure (green). SAMSUNG-1008, [0057]; *see* [0068]. “Inter-layer connectors, such as plugs” (pink), “extend through vias” in the ILD (orange) to

connect the gate structures to the M1 trace and thus to one another. SAMSUNG-1008, [0068]; *see* [0057]; SAMSUNG-1003, ¶176.



Anderson-Lin-Kawa figure

3. Reasons to combine Anderson, Lin, and Kawa

A POSITA would have been motivated to incorporate local interconnects and gate contact plugs into the combination for at least the following reasons. SAMSUNG-1003, ¶¶177-182.

First, a POSITA would have been motivated to pursue this implementation because doing so would enable formation of electrical connections to the gate structures, allowing creation of circuits including those transistors. *See*

SAMSUNG-1006, [0050] (“contacts can be connected to the source/drain and gate electrodes using conventional etching and metal deposition processes”); SAMSUNG-1020, 9:61-10:3; SAMSUNG-1021, [0027]-[0030]; SAMSUNG-1022, 3:39-4:12; SAMSUNG-1023, [0127]; SAMSUNG-1003, ¶178.

Second, a POSITA would have been motivated to incorporate M1 traces “parallel to the gate traces” because this arrangement “facilitates the use of the first patterned conductor layer for interconnecting gate traces and source/drain regions along columns in the adjacent blocks.” SAMSUNG-1008, [0057]; *see* [0097]; SAMSUNG-1003, ¶179. A POSITA would have recognized that this configuration provides design flexibility in allowing for interconnection of “traces in the gate conductor layer [and] traces in the first patterned gate conductor layer” “in any desired pattern.” SAMSUNG-1008, [0058]; *see* [0098]; SAMSUNG-1003, ¶179. A POSITA would have been motivated to pursue this arrangement to achieve advantages afforded by this flexibility, *e.g.*, “implementing engineering change orders ... during design verification processes.” SAMSUNG-1008, [0113]; *see* [0108], [0110]-[0111]; SAMSUNG-1003, ¶179.

Third, a POSITA would have been motivated to incorporate M1 traces, *e.g.*, in the arrangement described by Kawa, because this architecture advantageously “allows for very dense area utilization with flexible layout strategies,” *e.g.*, enabling use of the resulting integrated circuit structures for “multiple bit flip-flops

and sequential elements,” or “for implementation of ... high density and/or high performance integrated circuit structures.” SAMSUNG-1008, [0112]; SAMSUNG-1003, ¶180.

Fourth, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, interconnects and plugs in a FinFET-based device) to a known structure (*e.g.*, a FinFET structure) to yield predictable results (*e.g.*, a FinFET-based integrated circuit in which gates are electrically connected by interconnects and plugs). SAMSUNG-1003, ¶181; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have expected success because the incorporation of local interconnects and contacts is consistent with Anderson’s teachings that “contacts can be connected to the source/drain and gate electrodes.” SAMSUNG-1006, [0050]; SAMSUNG-1003, ¶182. A POSITA also would have expected success given that local interconnects and contacts were well-known elements of FinFET-based integrated circuits. *See* SAMSUNG-1020, 9:61-10:3; SAMSUNG-1021, [0027]-[0030]; SAMSUNG-1022, 3:39-4:12; SAMSUNG-1023, [0127]; SAMSUNG-1003, ¶182.

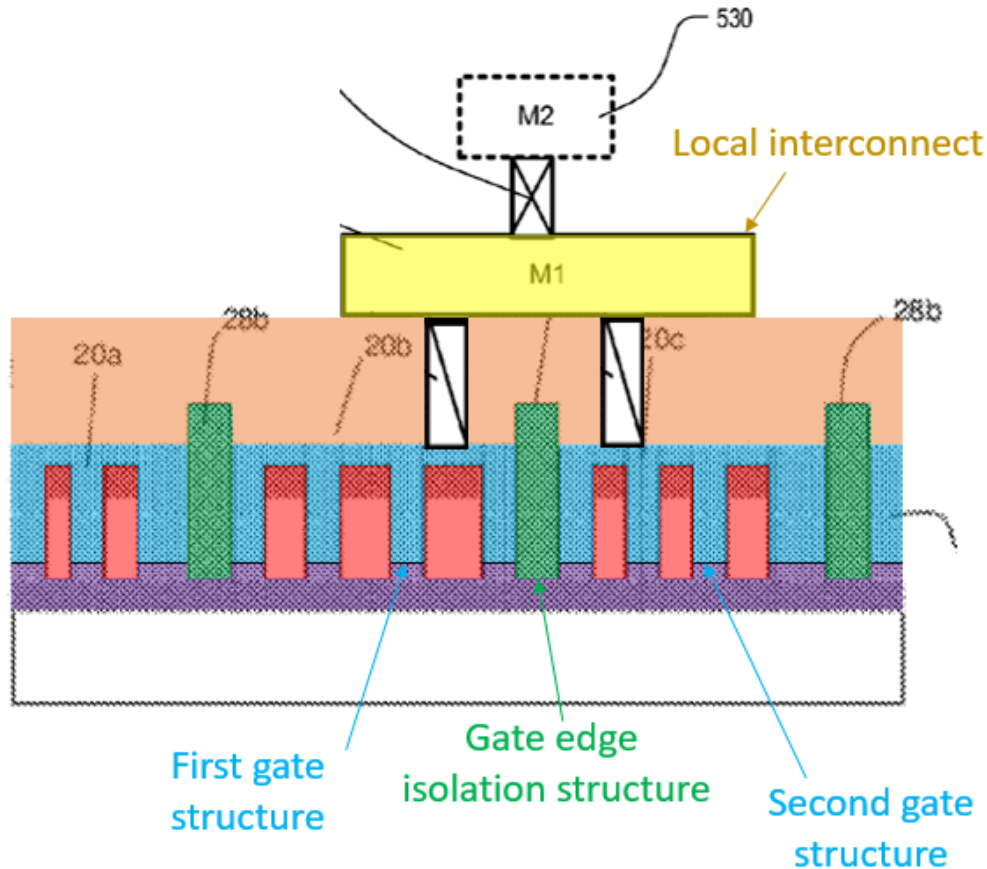
4. Analysis

(1) Claim 33

Limitation [33]

The Anderson-Lin-Kawa combination includes a local interconnect

The Anderson-Lin-Kawa combination includes **a local interconnect**, *e.g.*, Kawa's ***M1 trace*** (*e.g.*, M1 traces 430, 520 in Kawa's FIGS. 4 and 5), yellow in the figure *infra*. See SAMSUNG-1008, [0068] ("Connections between gate traces in adjacent blocks can be implemented using ***the first patterned conductor layer M1 by forming trace 520***"), [0057], [0073]-[0078], [0081], [0097]-[0098], FIGS. 4-5, FIGS. 7-11; SAMSUNG-1003, ¶183.



Anderson-Lin-Kawa figure

In the combination, Kawa's M1 trace is an **interconnect** because it electrically connects the first and second gate structures (blue). *See* SAMSUNG-1008, [0057], [0068]; SAMSUNG-1003, ¶184.

Moreover, Kawa's M1 trace is a **local interconnect** because it is an M1-level interconnect connecting gate structures over a short distance. It was well-known for local interconnects to be on the M1-level. *See* SAMSUNG-1020, 9:61-63 ("Standard processing follows, which includes formations of metallic contacts

and metallization for *the M1-level local interconnect wiring*"); SAMSUNG-1021, [0028] ("The resulting local interconnects are self-aligned, which ... allows *the local interconnect horizontal direction to be placed on the metal 1 pitch*"); SAMSUNG-1018, FIG. 6; SAMSUNG-1019, FIG. 2; SAMSUNG-1022, 3:52-4:1; SAMSUNG-1023, [0127]; SAMSUNG-1003, ¶185.

The local interconnect in the combination is disposed over the gate structures and the gate edge isolation structure

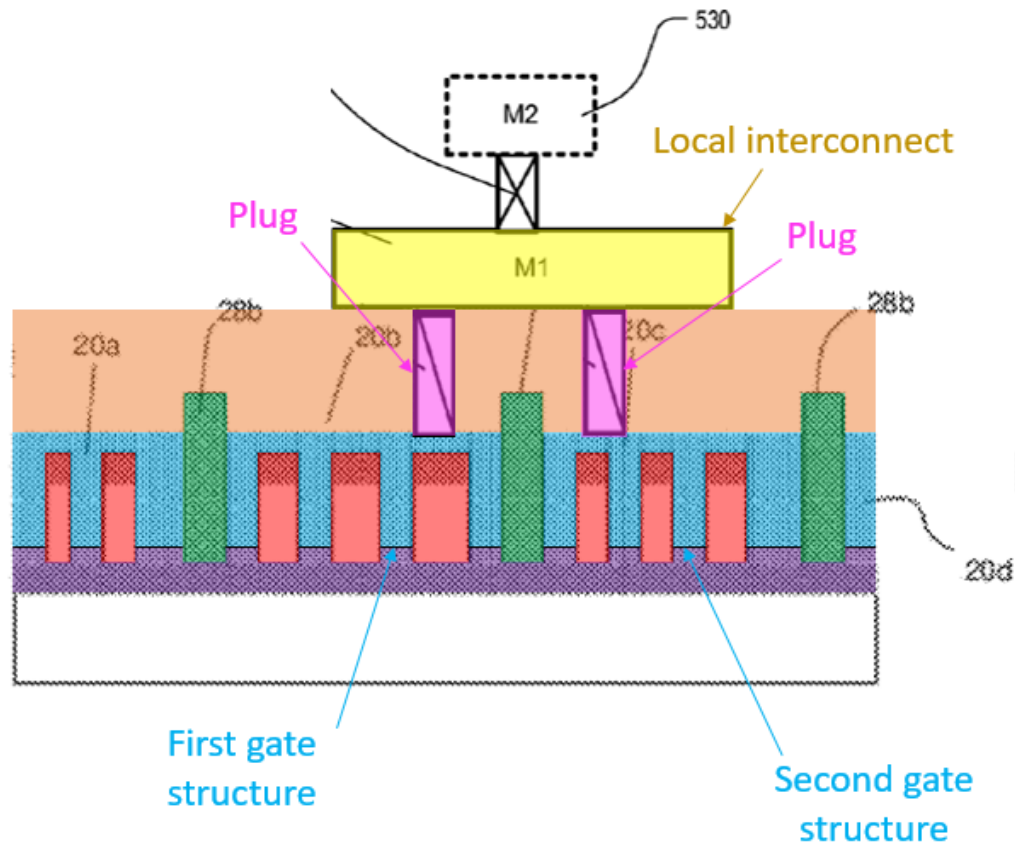
As shown in the figure *supra*, the local interconnect in the combination is **disposed over a portion of the first and second gate structures** (blue), based on Kawa's teachings that the M1 trace overlies portions of the gate traces (*e.g.*, gate traces 412, 422 of Fig. 4, gate traces 505, 506 of Fig. 5). *See* SAMSUNG-1008, [0057] ("a first patterned conductor layer (*metal 1*) **includes a plurality of traces ... which overlie the patterned gate conductor layer**"), [0068], FIGS. 4-5, FIGS. 7-11; SAMSUNG-1003, ¶¶186-187.

As shown *supra*, the local interconnect is disposed **over a portion of the gate edge isolation structure** (green), based on Kawa's teachings that the M1 trace overlies an isolation structure between the gate traces (*e.g.*, isolation structure 426 of Fig. 4, isolation structure 512 of Fig. 5). *See* SAMSUNG-1008, [0057] ("The trace 430 is an inter-block trace ... *passing over the isolation structure*"), FIGS. 4-5, FIGS. 7-11; SAMSUNG-1003, ¶188.

(2) Claim 34

Limitation [34]

In the Anderson-Lin-Kawa combination, **the local interconnect** (*e.g.*, the M1 trace, yellow in the figure *infra*) **electrically couples the first gate structure to the second gate structure** (blue) through plugs (pink), based on Kawa. *See* SAMSUNG-1008, [0068] (“*Connections between gate traces* in adjacent blocks *can be implemented using the first patterned conductor layer M1* by forming trace 520 ... Interlayer connectors, such as plugs 521 and 522 extend through vias in the insulating fill 515 to connect gate traces 505 and 506, respectively, to the trace 520”), [0057]-[0058] (“The trace 430 is an inter-block trace arranged to connect a gate trace in block 400 to a gate trace in block 401”), [0067], claim 1, [0073]-[0074], [0077]-[0078], [0081], [0097]-[0098]; SAMSUNG-1003, ¶189.



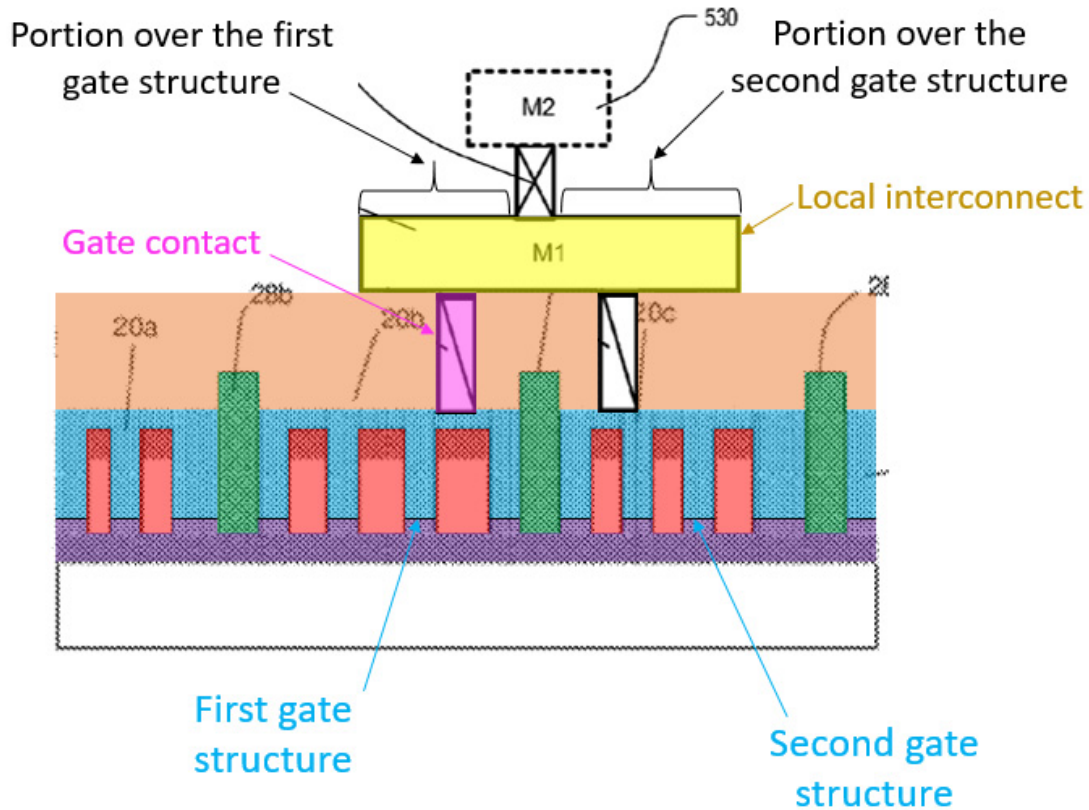
Anderson-Lin-Kawa figure

(3) Claim 35

Limitation [35]

The Anderson-Lin-Kawa combination includes **a gate contact**, *e.g.*, Kawa's plug 521 (pink in the figure *infra*). Kawa's plug is **a gate contact** in the combination: it acts as a contact (*e.g.*, provides electrical connection) between the local interconnect and the first gate structure: "*Interlayer connectors, such as plugs 521 and 522 extend through vias in the insulating fill 515 to connect gate traces 505 and 506, respectively, to the trace 520.*" SAMSUNG-1008, [0068]; *see*

[0058], [0073]-[0074], [0077]-[0078], [0081], [0097]-[0098], FIGS. 4-5, FIGS. 7-11; SAMSUNG-1003, ¶190.



Anderson-Lin-Kawa figure

As illustrated *supra*, the gate contact (*e.g.*, Kawa's plug) is **on** (*e.g.*, in contact with) **a portion of the local interconnect over the first gate structure,** **but not on** (*e.g.*, not in contact with) **a portion of the local interconnect over the second gate structure.** This positioning arises from the nature of Kawa's plugs as "vertical conductors." SAMSUNG-1008, [0058]. A vertical conductor connecting the first gate structure to the local interconnect extends vertically, but does not

extend diagonally (*e.g.*, does not extend to the portion of the local interconnect that is positioned directly above the second gate structure). SAMSUNG-1003, ¶191.

V. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

A. The *Fintiv* Factors Favor Institution—§314(a)

The '306 Patent is the subject of complaints filed by Patent Owner in both district court and ITC on September 12, 2022. The district court case is currently stayed pending resolution of the ITC matter, and thus only the ITC matter is proceeding at this time. Pursuant to the Interim Procedure For Discretionary Denials In AIA Post-Grant Proceedings (June 21, 2022), the “PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.” Accordingly, the *Fintiv* factors do not provide a reason to discretionarily deny institution based on the co-pending ITC proceeding.

B. The *Advanced Bionics* Test Favors Institution—§ 325(d)

This Petition presents new prior art and arguments against the Challenged Claims for which the file history contains no indication that the Office ever previously considered in connection with the '306 Patent. Indeed, none of Xie, Tseng, Anderson, Lin, or Kawa—the only references applied in this Petition against the Challenged Claims—were previously cited or applied in a rejection during prosecution of the '306 Patent.

VI. CONCLUSION AND FEES

The Challenged Claims are unpatentable. Petitioner authorizes charge of fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Samsung”) are the real parties-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

The '306 Patent is the subject of a civil action, *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00352, E.D. Tex., filed September 12, 2022 (SAMSUNG-1054) and *Semiconductor Devices, Mobile Devices Containing The Same, and Components Thereof*; 337-TA-1336 (ITC) filed September 12, 2022 (SAMSUNG-1050). Petitioner is not aware of any other disclaimers, reexamination certificates, or IPR petitions addressing the '306 Patent.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR39843-0151IP1@fr.com

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Respectfully submitted,

Dated January 19, 2023

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(Control No. IPR2023-00403)

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,768 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated January 19, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on January 19, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided by Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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