**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | |
|---|---|---|
| In re Patent of: | Milton Clair Webb, et al. | |
| U.S. Patent No.: | 9,831,306 | Attorney Docket No.: 39843-0151IP1 |
| Issue Date: | November 28, 2017 | |
| Appl. Serial No.: | 15/024,750 | |
| Filing Date: | December 19, 2013 | |
| Title: | SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME | |

# DECLARATION OF DAVID KUAN-YU LIU

# TABLE OF CONTENTS

I. QUALIFICATIONS AND BACKGROUND INFORMATION ..... 1
A. Educational Background ..... 1
B. Professional Experience ..... 1
II. OVERVIEW OF CONCLUSIONS FORMED ..... 8
III. LEVEL OF ORDINARY SKILL IN THE ART ..... 8
IV. SUMMARY OF THE ’306 PATENT ..... 9
A. Overview of the ’306 Patent ..... 9
B. Spatial Relationships of Elements of the Challenged Claims ..... 12
V. PRIOR ART ANALYSIS ..... 18
A. [GROUND 1] – CLAIMS 26-31 ARE OBVIOUS OVER XIE ..... 18
1. Xie describes FinFET devices having gate separation structures ..... 18
2. A POSITA would have understood or found obvious that Xie’s gate structures each includes a gate dielectric layer and a gate electrode ..... 23
3. Structure of Xie’s gate structures when formed by a gate-last process ..... 28
4. Structure of Xie’s gate structures when formed by a gate-first process ..... 32
5. Claim-by-Claim Analysis ..... 37
B. [GROUND 2] – CLAIMS 26-31 ARE OBVIOUS OVER XIE AND TSENG ..... 72
1. Tseng describes FinFET gate structures having a gate dielectric layer and a gate electrode ..... 72
2. The Xie-Tseng combination ..... 73
3. Analysis ..... 74
C. [GROUND 3A] – CLAIMS 26-29 AND 31-32 ARE OBVIOUS OVER ANDERSON AND LIN ..... 76
1. Anderson describes gate-to-gate isolation structures for FinFET devices ..... 76
2. Lin describes FinFET gate structures ..... 79
3. The Anderson-Lin combination ..... 80
4. Reasons to combine Anderson and Lin ..... 84
5. Analysis ..... 89

D. [GROUND 3B] – CLAIMS 33-35 ARE OBVIOUS OVER ANDERSON, LIN, AND KAWA ..... 128
1. Kawa describes local interconnects connecting gates of FinFET transistors ..... 128
2. The Anderson-Lin-Kawa combination ..... 131
3. Reasons to combine Anderson, Lin, and Kawa ..... 133
4. Analysis ..... 136

VI. LEGAL PRINCIPLES ..... 145
A. Anticipation ..... 145
B. Obviousness ..... 146

VII. ADDITIONAL REMARKS ..... 148

I, David Kuan-Yu Liu, declare the following:

## I. QUALIFICATIONS AND BACKGROUND INFORMATION

1. My education and experience are described more fully in the attached curriculum vitae. For ease of reference, I have highlighted certain information below.

### A. Educational Background

2. I received a Bachelor of Science degree in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

### B. Professional Experience

3. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

4. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5um and 0.35um Flash EPROM technology. My job responsibilities at AMD also included process integration,

device modeling, and development of triple-well process technology for accommodating x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

5. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

6. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

7. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm). The flash memory products I developed at Xilinx are used as the configuration memory for the FPGA, with the configuration interface between them being the JTAG interface.

8. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

9. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

10. I have 20 years of experience as an engineer and engineering manager/director of Complementary Metal Oxide Semiconductor (CMOS) technology development. During my career, I have worked at some of the leading technology companies in the world, such as Texas Instruments, Advanced Micro Devices, Altera Corporation (now a subsidiary of Intel Corp.), and Xilinx. At these companies, my work focused on various aspects of CMOS and semiconductor technology.

11. I hold over 99 U.S. patents, a large number of which are directed to logic CMOS processes technology and high voltage CMOS process technology. The vast majority of my patents are in the area of CMOS process technology and memory architecture. As such, I am intimately familiar with the implementation of integrated process flows that essentially are repetitive sequences of modules, each composed of a layer patterning step followed by selective deposition and etching of various semiconductor materials, with the area of selectivity dictated by the

layer patterning. I am also familiar with the different layout techniques, including the use of various interconnect layers, to achieve compact array density. I also have worked on FinFET technologies, and hold U.S. Patent No. 10,629,607, directed to FinFET technology for non-volatile memory.

12. I have been retained on behalf of Samsung Electronics Co., Ltd., to offer technical opinions relating to U.S. Patent No. 9,831,306 ("the '306 Patent") and prior art references related to its subject matter. I have reviewed the '306 Patent and the following references.

- U.S. Patent Pub. No. 2015/0054078 to Xie ("Xie") (SAMSUNG-1004)
- U.S. Patent No. 9,397,217 to Tseng ("Tseng") (SAMSUNG-1005)
- U.S. Patent Pub. No. 2012/0086055 to Anderson ("Anderson") (SAMSUNG-1006)
- U.S. Patent No. 9,041,125 to Lin ("Lin") (SAMSUNG-1007)
- U.S. Patent Pub. No. 2013/0026572 to Kawa ("Kawa") (SAMSUNG-1008)

13. I have also reviewed various supporting references, including the following, and other documentation as further noted in my opinions below.

- SAMSUNG-1009: U.S. Patent Pub. No. 2007/0080380 to Chang ("Chang")

- SAMSUNG-1010: U.S. Patent No. 9,324,790 to Akarvardar ("Akarvardar")
- SAMSUNG-1011: U.S. Patent No. 8,994,116 to Gan ("Gan")
- SAMSUNG-1012: U.S. Patent No. 11,037,923 to Bohr ("Bohr")
- SAMSUNG-1013: U.S. Patent No. 7,898,037 to Chuang ("Chuang")
- SAMSUNG-1014: U.S. Patent No. 9,166,053 to Kuo ("Kuo")
- SAMSUNG-1015: U.S. Patent Pub. No. 2013/0164924 to Shieh ("Shieh")
- SAMSUNG-1016: U.S. Patent No. 8,895,381 to Cheng ("Cheng")
- SAMSUNG-1017: U.S. Patent No. 9,196,613 to Basker ("Basker")
- SAMSUNG-1018: Robert H. Havemann and James A. Hutchby, "High-Performance Interconnects: An Integration Overview," Proceedings of the IEEE, vol. 89, no. 5, pp. 586-601, May 2001
- SAMSUNG-1019: Dick James, "Intel Ivy Bridge Unveiled – The First Commercial Tri-Gate, High-k, Metal-Gate CPU," Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, September 2012
- SAMSUNG-1020: U.S. Patent No. 8,492,841 to Anderson ("Anderson-841")
- SAMSUNG-1021: U.S. Patent Pub. No. 2012/0037996 to Schultz ("Schultz")

- SAMSUNG-1022: U.S. Patent No. 8,952,424 to Herberholtz ("Herberholtz")
- SAMSUNG-1023: U.S. Patent Pub. No. 2017/0186882 to Koldiaev ("Koldiaev")
- SAMSUNG-1025: U.S. Patent No. 9,281,378 to Ching ("Ching")
- SAMSUNG-1026: U.S. Patent No. 6,894,357 to Guo ("Guo")
- SAMSUNG-1027: U.S. Patent No. 7,586,159 to Lee ("Lee")
- SAMSUNG-1028: U.S. Patent Pub. No. 2006/0220090 to Metz ("Metz")
- SAMSUNG-1029: U.S. Patent Pub. No. 2015/0200275 to Zhu ("Zhu")
- SAMSUNG-1030: U.S. Patent No. 8,637,931 to Basker ("Basker-931")
- SAMSUNG-1031: U.S. Patent No. 8,697,515 to Yin ("Yin")
- SAMSUNG-1034: U.S. Patent No. 7,632,745 to Chen ("Chen-745")
- SAMSUNG-1035: U.S. Patent No. 9,246,003 to Cheng ("Cheng")
- SAMSUNG-1036: U.S. Patent No. 7,592,675 to Liaw ("Liaw")
- SAMSUNG-1037: U.S. Patent No. 9,214,529 to Chang ("Chang-529")

- SAMSUNG-1038: U.S. Patent Pub. No. 2011/0031552 to Iwamatsu ("Iwamatsu")
- SAMSUNG-1039: U.S. Patent No. 9,461,143 to Pethe ("Pethe")
- SAMSUNG-1040: U.S. Patent No. 8,901,665 to Kelly ("Kelly")
- SAMSUNG-1041: U.S. Patent No. 6,720,619 to Chen ("Chen-619")

14. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the '306 Patent at the time of the earliest possible priority date of the '306 Patent, and I have done so during my review of these materials. The '306 Patent claims the benefit of priority to a PCT application filed December 19, 2013 ("the Critical Date"). Counsel has informed me that the Critical Date represents the earliest possible priority date to which the challenged claims of '306 Patent are entitled, and I have therefore used that Critical Date in my analysis below.

15. I have no financial interest in the parties or in the outcome of this proceeding. I am being compensated for my work as an expert on an hourly basis. My compensation is not dependent on the outcome of these proceedings or the content of my opinions.

16. In writing this declaration, I have considered the following: my own knowledge and experience, including my work experience in the fields of mechanical engineering, computer science, biomedical engineering, and electrical

engineering; my experience in teaching those subjects; and my experience in working with others involved in those fields. In addition, I have analyzed various publications and materials, in addition to other materials I cite in my declaration.

17. My opinions, as explained below, are based on my education, experience, and expertise in the fields relating to the ’306 Patent. Unless otherwise stated, my testimony below refers to the knowledge of one of ordinary skill in the art as of the Critical Date, or before. Any figures that appear within this document have been prepared with the assistance of Counsel and reflect my understanding of the ’306 Patent and the prior art discussed below.

## II. OVERVIEW OF CONCLUSIONS FORMED

18. This declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions, based upon my knowledge and experience and my review of the prior art publications listed above, I believe that:

- Claims 26-31 are obvious over Xie;
- Claims 26-31 are obvious over Xie and Tseng;
- Claims 26-29 and 31-32 are obvious over Anderson and Lin; and
- Claims 33-35 are obvious over Anderson, Lin, and Kawa.

## III. LEVEL OF ORDINARY SKILL IN THE ART

19. In my opinion, one of ordinary skill in the art relating to, and at the time of, the invention of the ’306 Patent would have been a person with a Master’s

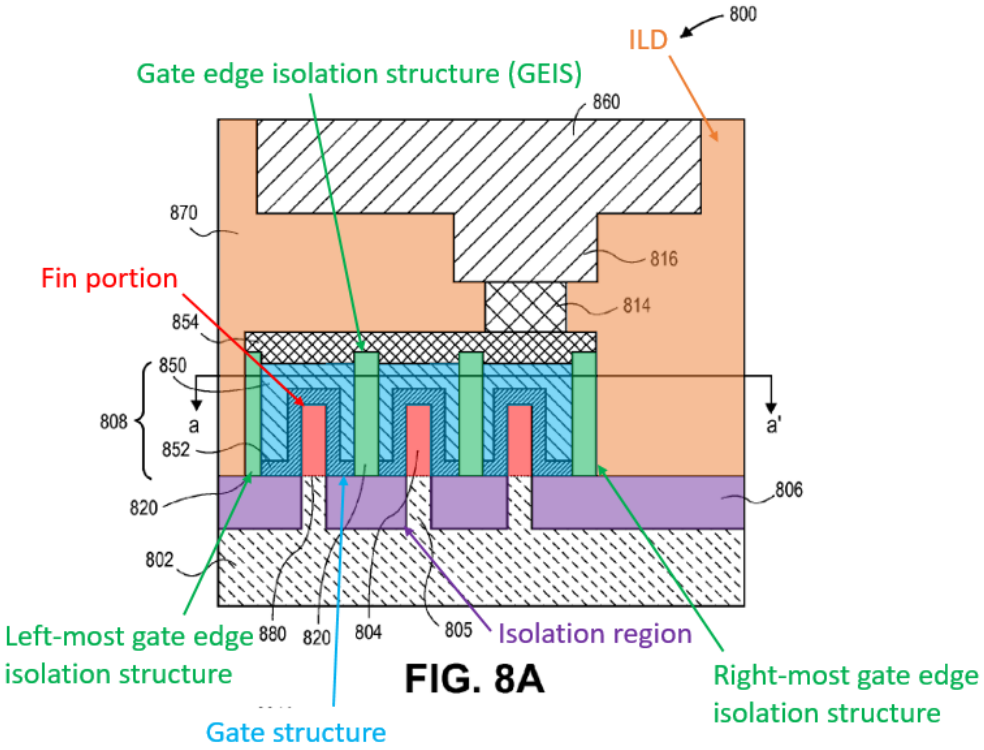
degree in electrical engineering, physics, or a related field, and two years of work experience in integrated circuit design or manufacturing. Greater education or greater experience could compensate for a deficiency in either of these criteria.

20. Based on my experiences, I have a good understanding of the capabilities of one of ordinary skill. Indeed, I have participated in organizations and worked closely with many such persons over the course of my career. Based on my knowledge, skill, and experience, I have an understanding of the capabilities of one of ordinary skill. For example, from my industry experience, I am familiar with what an engineer would have known and found predictable in the art. Furthermore, I possess those capabilities myself.

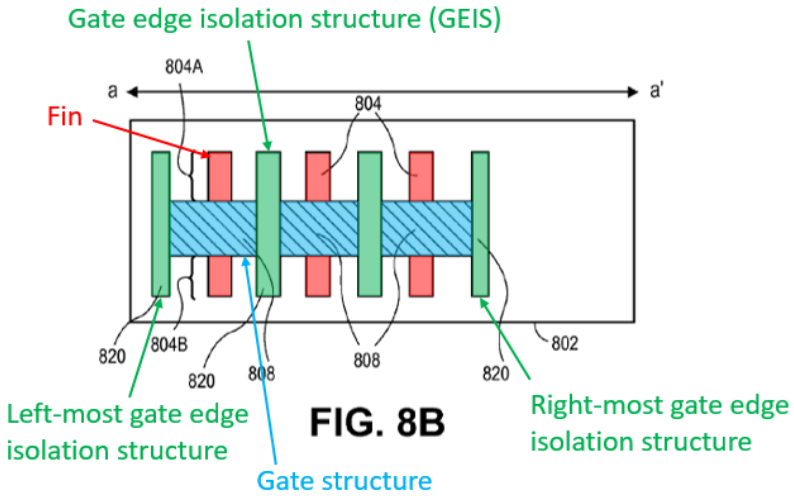
## IV. SUMMARY OF THE '306 PATENT

### A. Overview of the '306 Patent

21. The '306 Patent is said to describe "[s]elf-aligned gate edge and local interconnect structures." SAMSUNG-1001 ('306 Patent), Abstract. An example of such a structure—specifically, a "non-planar semiconductor device having self-aligned gate isolation"—is shown in "a cross-sectional view and a plan view" in FIGS. 8A-8B, *infra*. *Id.*, 9:27-30.




Excerpt from ’306 Patent, FIG. 8A (annotated)




Excerpt from ’306 Patent, FIG. 8B (annotated)

22. This semiconductor device includes “non-planar active regions (e.g., a fin structures [sic] including protruding fin portion 804 and sub-fin region 805)

formed from substrate 802, and within isolation region 806." SAMSUNG-1001 ('306 Patent), 9:34-37; *see* claim 26. I have highlighted the protruding fin portions 804 in red and the isolation region 806 in purple. "Gate structures 808," highlighted in blue, are "disposed over the protruding portions 804 of the non-planar active regions as well as over a portion of the isolation region 806." SAMSUNG-1001 ('306 Patent), 9:37-39; *see* claim 26. "Gate structures 808 are separated by self-aligned gate edge isolation structures 820," green. *Id.*, 9:43-44; *see* claim 26.

23. Interconnects 854, 860 and contacts 814 are "disposed in inter-layer dielectric stacks or layers 870," orange. SAMSUNG-1001 ('306 Patent), 9:45-49. As shown in cross-section, the inter-layer dielectric (ILD) 870 covers the gate structures and gate edge isolation structures, and fills the space next to the exposed outer sidewalls of the right-most and left-most gate edge isolation structures (labeled in the figures above *supra*).[1]

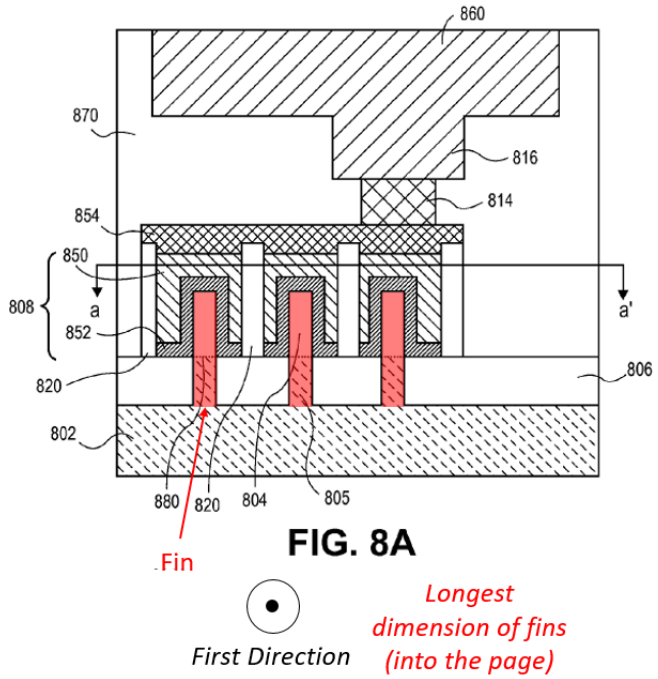
---

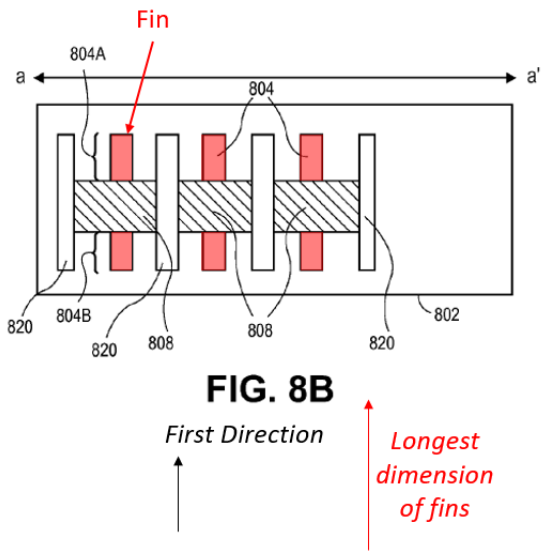
[1] I note that FIG. 8B does not specifically label the dielectric material 870. However, since FIG. 8B illustrates a top view through the a-a′ cut in FIG. 8A, it is my opinion that a POSITA at best would understand or find obvious that the dielectric material 870 is present at least next to the left-most and right-most gate edge isolation structures that are shown in FIG. 8B.

### B. Spatial Relationships of Elements of the Challenged Claims

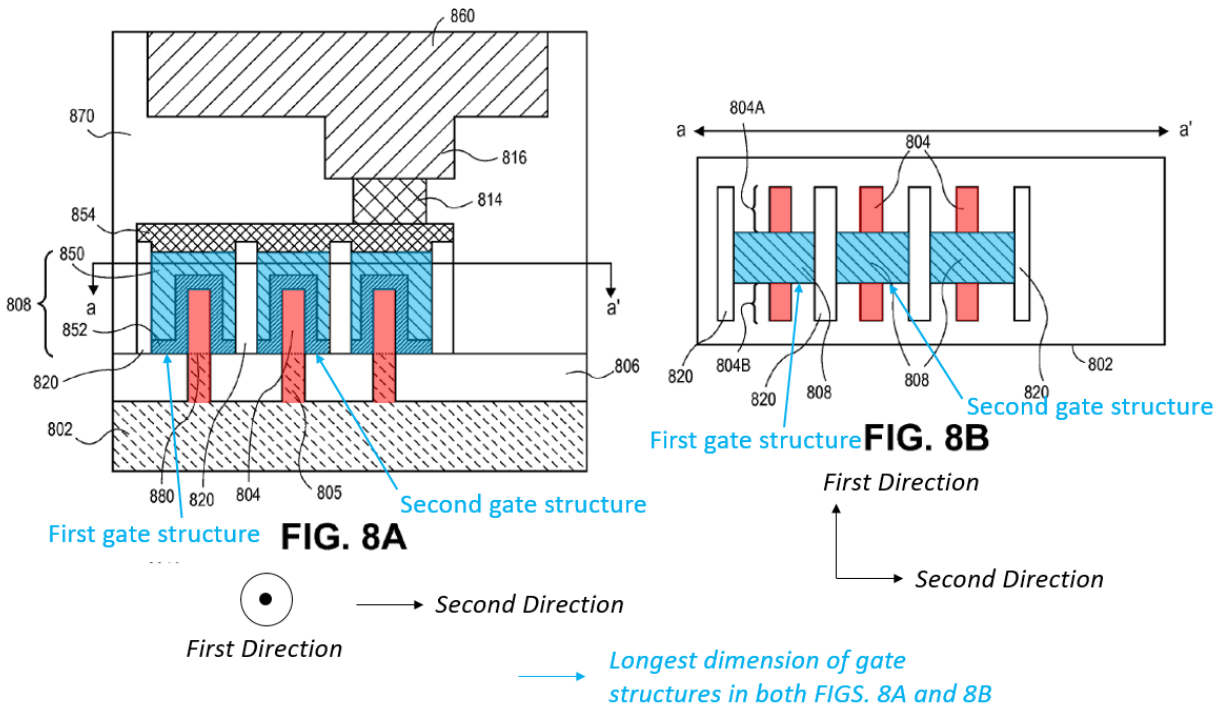
24. The Challenged Claims recite spatial relationships between various features of an integrated circuit structure. I have provided an overview of some of these features, and their relationships, in the following paragraphs, with reference to FIGS. 8A and 8B, reproduced throughout this section.

25. The Challenged Claims recite that the fins (red) have "a longest dimension ***along a first direction***," which I have marked in the figures below. SAMSUNG-1001 ('306 Patent), claim 26. That is, the claims indicate the orientation of the fins, and thus, the claims define an orientation that is along the first direction. Based on these figures and read in light of the specification, it is my opinion that a POSITA would understand or find obvious that the longest dimension of the fins extends from top to bottom in the top view (FIG. 8B), and correspondingly into the page in the cross-sectional view (FIG. 8A). *See id.*, Abstract, 13:47-49, 14:4-8. This direction is the first direction.

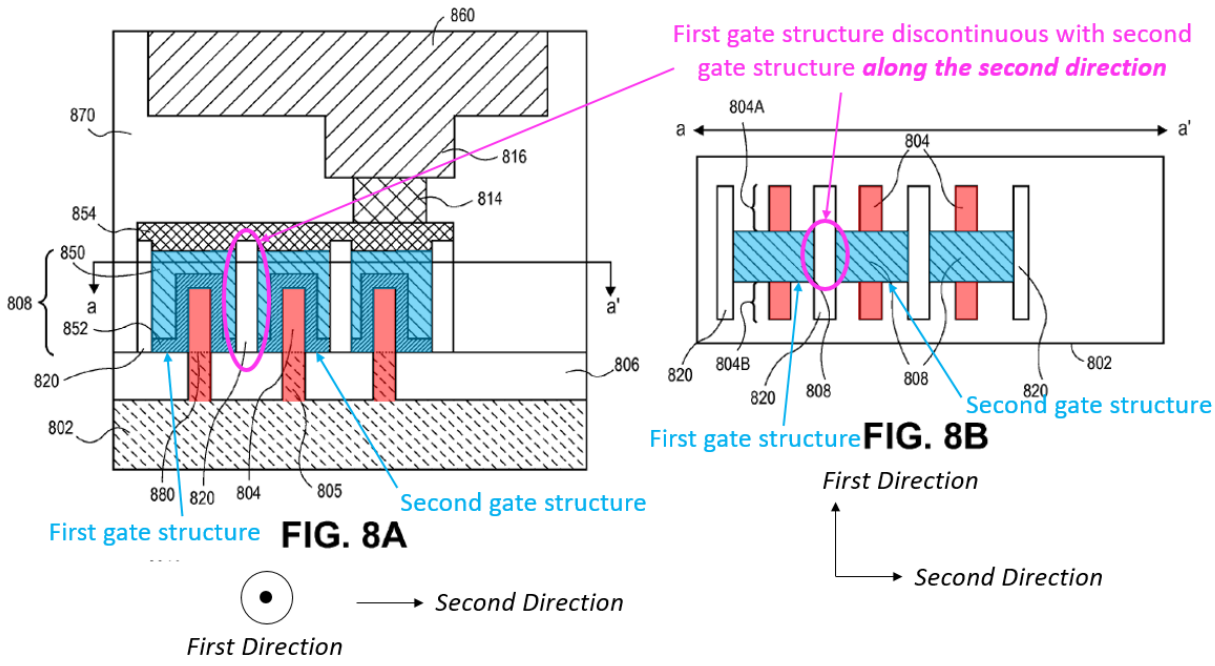


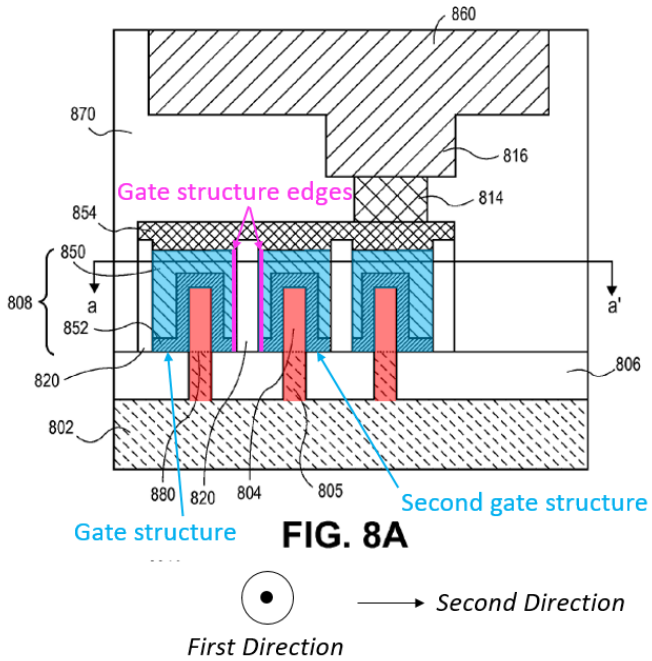

26. The Challenged Claims also recite that the gate structures have "a longest dimension ***along a second direction*** … orthogonal to the first direction." SAMSUNG-1001 ('306 Patent), claim 26. The direction orthogonal to the length of the fins (*i.e.*, orthogonal to the first direction) is the left-to-right direction in both the cross-sectional view (FIG. 8A) and top view (FIG. 8B), marked in the figures below. It is my opinion that a POSITA would have understood or found obvious that this direction is the second direction. For instance, I note that these figures illustrate gate structure dimension that appear to be longest along this direction. *See id.*, Abstract, 13:49-52, 14:8-10.

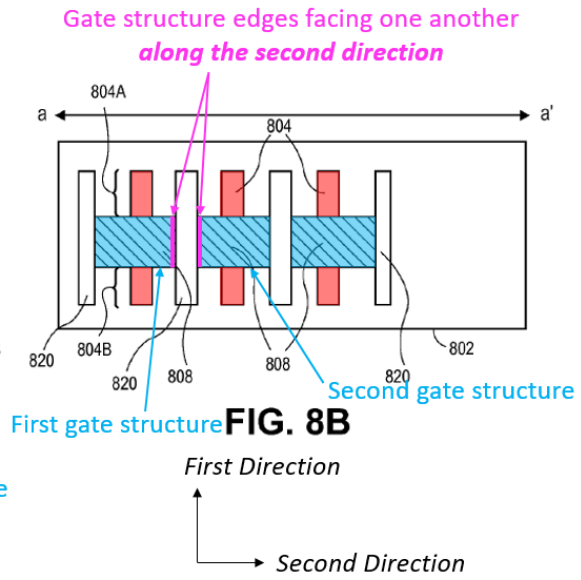



27. The Challenged Claims recite that a "second gate structure [is] discontinuous with [a] first gate structure ***along the second direction***." SAMSUNG-1001 ('306 Patent), claim 26. This discontinuity, and its orientation along the second direction, are shown in the figures below. For instance, when viewing the structure starting from the first gate structure and ***moving along the second direction*** (*i.e.*, moving from left to right in both the top view and the cross-sectional view), as a discontinuity exists (occupied by the gate edge isolation structure, discussed below) between the two gate structures before reaching the second gate structure.



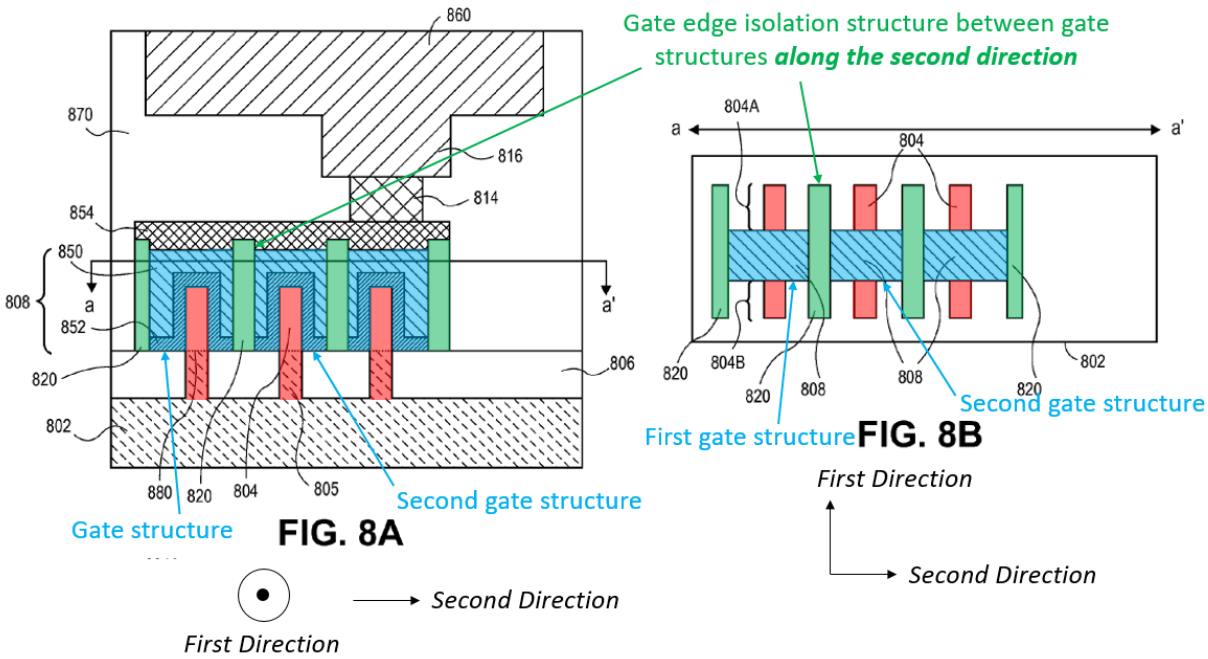

28. Similarly, the Challenged Claims recite that "an edge" of the second gate structure "fac[es] an edge of the first gate structure ***along the second direction***." It is my opinion that a POSITA would have understood or considered this to be obvious when viewing the structure starting from the edge of the first gate structure (which I have outlined in pink in the figures below) and ***moving along the second direction*** to encounter the edge of the second gate structure (also outlined in pink).



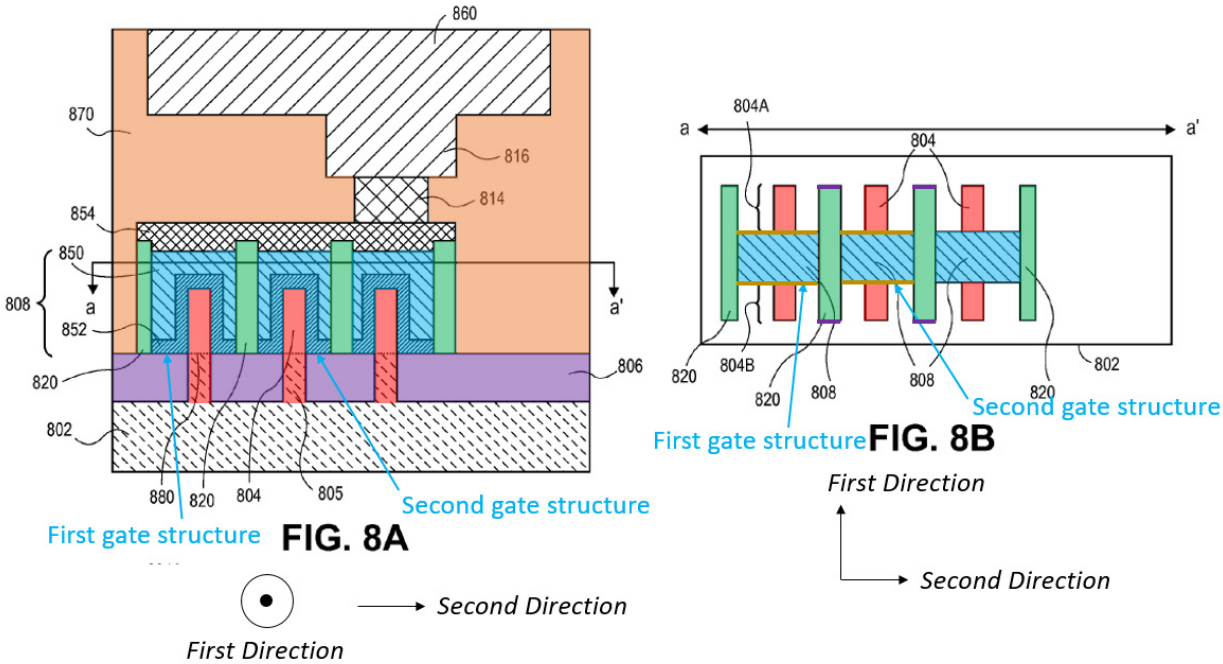

29. The gate edge isolation structure of the Challenged Claims is "between and in contact with the edge of the first gate structure and the edge of the second gate structure ***along the second direction***." SAMSUNG-1001 ('306 Patent), claim 26. As illustrated in the figures below, the gate edge isolation structure (which I have highlighted in green) is between and in contact with the edges (outlined in pink) of the gate structures ***along the second direction***: starting from the edge of the first gate structure and ***moving along the second direction***, one reaches first the gate edge isolation structure and then the edge of the second gate structure. Notably, the '306 Patent provides no illustration or description of a gate edge isolation structure between and in contact with edges of gate structures in an arrangement such that starting from the edge of the first gate structure and moving in the orthogonal direction (*e.g.*, from top to bottom in the top view

figure), one would reach first the gate edge isolation structure and then the edge of the second gate structure.




30. The Challenged Claims also recite that the "dielectric material [is] laterally adjacent to the first and second gate structures ***along the first direction***" and "laterally adjacent to the gate edge isolation structure … ***along the first direction***." SAMSUNG-1001 ('306 Patent), claim 26. For this proceeding, I interpret these limitations consistent with the use of the phrase "along the second direction" (discussed in the previous paragraphs). For instance, as shown in the figures below, a dielectric material would be laterally adjacent to the gate structures (blue) ***along the first direction*** if it were at the sidewalls of the gate structures (outlined in pink in FIG. 8B, reproduced again *infra*). Similarly, a dielectric material would be laterally adjacent to the gate edge isolation structure

(green) ***along the first direction*** if it were at the short ends of the gate edge isolation structure (outlined in purple in FIG. 8B).



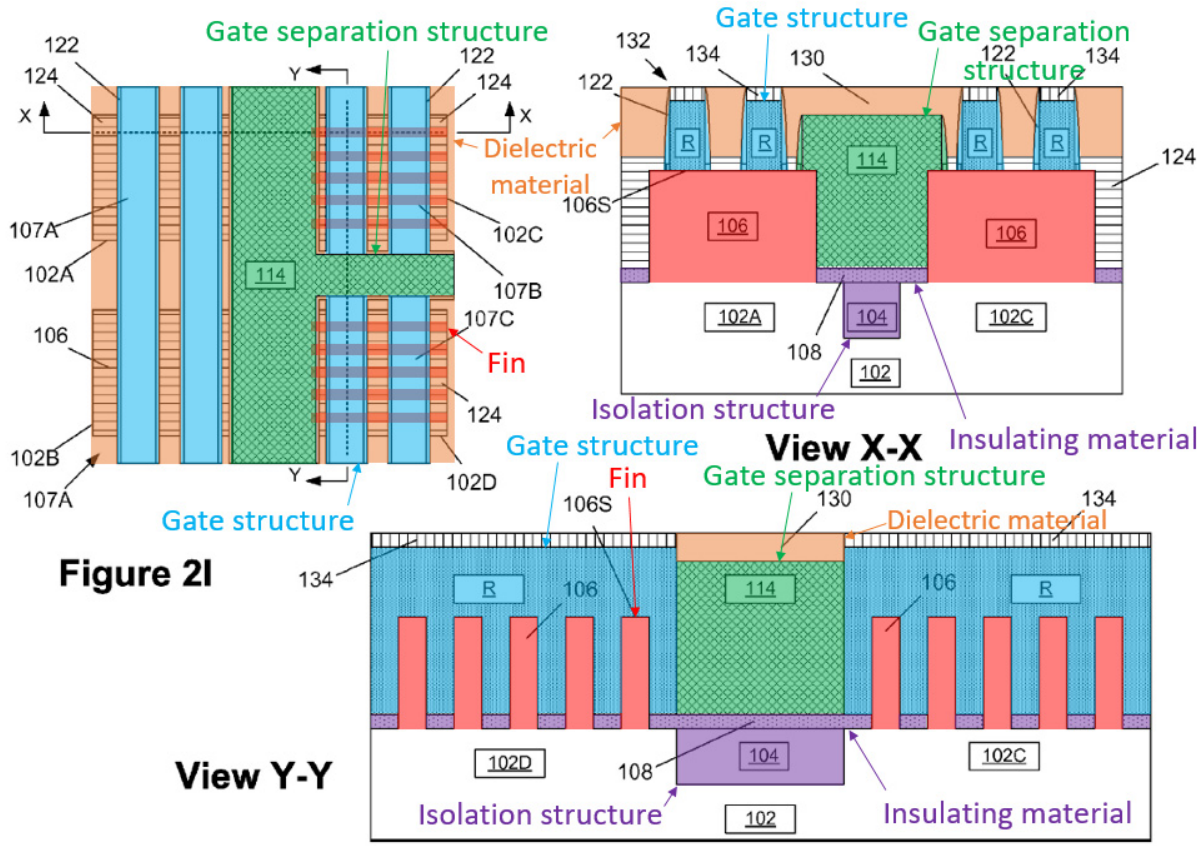

## V. PRIOR ART ANALYSIS_

### A. [GROUND 1] – CLAIMS 26-31 ARE OBVIOUS OVER XIE

#### 1. Xie describes FinFET devices having gate separation structures

31. Xie, in the field of FinFET devices, describes "methods … for forming gate structures for FinFET devices and resulting devices." SAMSUNG-1004 (Xie), [0027]. One such FinFET structure is illustrated Xie's FIG. 2I, which I have reproduced below. This structure includes a substrate 102 having "active regions 102A-D" defined by "isolation structures 104," highlighted in purple. *Id.*,

[0028]. "[A] plurality of fins 106," some of which are highlighted in red, are formed in the substrate. *Id.* The fins extend from left to right in the top view and X-X cross-sectional views of FIG. 2I, and into the page in the Y-Y cross-sectional view: "the view 'X-X is taken along a line that passes through the fins 106, while the view 'Y-Y' is a cross-section view that is taken transverse to ***the long axis of the fins 106***." *Id.*, [0027]. An insulating material 108, highlighted in purple, "remains in the bottom of the trenches" between the fins "so as to locally isolate the fins 106 from one another." *Id.*, [0028].




Excerpt from Xie, FIG. 2I (annotated)[2]

32. I note that in the top view of Xie's FIG. 2I, the fins 106 are covered with "an epi semiconductor 124" and as such, are obscured in the figure by the epi semiconductor layer 124. SAMSUNG-1004 (Xie), [0035]. A top view of the

[2] In the top view figure, the dielectric material 130 would cover the gate separation structure, as shown in the X-X and Y-Y views. I do not show the dielectric material as covering the gate separation structure in this (and other) reproductions of Xie's FIG. 2I in this document solely for clarity.

exposed fins 106 can be seen in FIG. 2A, the top view of which is reproduced below. FIG. 2A shows Xie's structure prior to deposition of the epi semiconductor 124 and confirms the presence of the fins.

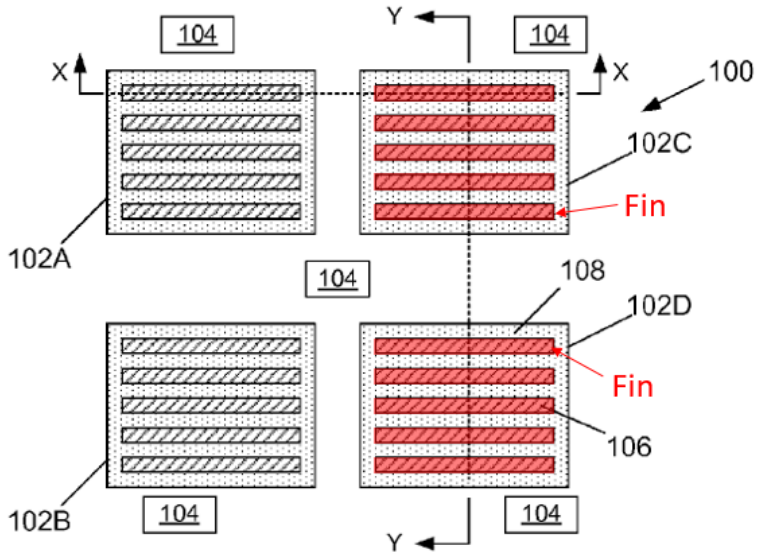



**Figure 2A**

Excerpt from Xie, FIG. 2A (annotated)

33. Returning to my discussion of Xie's FIG. 2I, gate structures, highlighted in blue, are disposed over the fins.[3] *See* SAMSUNG-1004 (Xie),

[3] I note that the top view of FIG. 2I includes reference numerals 107A-107C, which Xie identifies as sacrificial gate structures. *See* SAMSUNG-1004 (Xie), [0030]. It is my opinion that a POSITA would have understood that the features referred to by these reference numerals correspond to the replacement gate

[0016]-[0018], [0038]. Each gate structures is "a stack of material layers" that "may be formed using either gate-first or gate-last techniques." *Id.*, [0017], [0030]; *see* claims 4-5 ("wherein said plurality of gate structures are sacrificial gate structures" and "wherein said plurality of gate structures are final gate structures").

34. A "gate separation structure 114," which I have highlighted in green, is "positioned between the first and second spaced-apart gate structures" and over the insulating material 108. SAMSUNG-1004 (Xie), [0017], [0032]. A "layer of insulating material 130," highlighted in orange, is "blanket-deposited" onto the structure such that the insulating material is disposed on the gate separation structure 114 and to the sides of the gate separation structure and gate structures. SAMSUNG-1004 (Xie), [0036]; *see* FIG. 2I. For instance, in the top-view figure of FIG. 2I, the insulating material extends into the page to the sides of the gate separation structure and gate structures.

---

structures R and the gate cap layers 134, *e.g.*, based on the illustration in the X-X and Y-Y cross-sectional views and based on Xie's description of the fabrication process, in which the sacrificial gate structures 107 were previously removed and replacement gate structures R and gate cap layers 134 formed in the locations previously occupied by the sacrificial gate structures106. *See id.*, [0038].

### 2. A POSITA would have understood or found obvious that Xie's gate structures each includes a gate dielectric layer and a gate electrode

35. Xie's gate structures include "a stack of material layers" including "a high-k (k value greater than 10) gate insulation layer," "one or more metal layers … (e.g., layers of titanium nitride or TiAlC)," and "a bulk conductive metal layer … such as tungsten or aluminum." *Id.*, [0038], claim 1; *see* claim 5, [0015]-[0016], [0040]. It is my opinion that to the extent Xie does not explicitly disclose gate structures each having a gate dielectric layer and a gate electrode, a POSITA would have found this configuration obvious, as I discuss in the following paragraphs.

36. First, I note that it was well-known in the art as of the Critical Date for a gate structure in a FinFET device to include a gate dielectric layer (*e.g.*, a high-k gate dielectric layer) and a gate electrode (*e.g.*, a metal gate electrode). *See*, *e.g.*, SAMSUNG-1005 (Tseng), 5:5-46 (describing that the gate dielectric layer is a "high dielectric constant (high-k) dielectric" and the gate electrode includes an "N-work function metal" or a "P-work function metal"), 8:67-9:4 ("the gate-last process comprises … fill[ing] the trench with ***a gate dielectric layer and a conductive gate electrode layer***"), FIGS. 2 and 5A; SAMSUNG-1025 (Ching), 4:39-5:3 ("[t]he resulting remaining portions of the conductive material and gate dielectric layer 50 thus form the ***replacement gate, which includes gate electrode***

***52 and gate dielectric 50***," where "gate dielectric layer 50 comprises a high-k dielectric material" and "[c]onductive material 52 may comprise a metal-containing material such as TiN, TaN, TaC, Co, Ru, Al, combinations thereof"), Fig. 9A; SAMSUNG-1006 (Anderson), [0029] ("The gate stack 20 can be, for example, ***a gate dielectric and a gate electrode material***," where "the gate dielectric can be, for example, a high-k dielectric material" and "the gate electrode material being either a metal or a metal and polysilicon stack"); SAMSUNG-1011 (GAN), 3:59-4:10 ("The gate structure 110 includes a gate dielectric layer and a gate electrode. … The gate dielectric layer may further include … dielectric with a high dielectric constant (high-k) … The gate electrode may include … a metal including metal compounds such as, TiN, TaN, NiSi, CoSi, Mo, Cu, W, Al, Co"); SAMSUNG-1012 (Bohr), 4:46-48 ("The gate electrode 120 … is a portion of a gate electrode stack which further includes a gate dielectric layer 165"); SAMSUNG-1013 (Chuang), 3:45-46 ("Gate electrode strip 32 and gate dielectric 145 form the gate stack of FinFET 100"); SAMSUNG-1014 (Kuo), 7:8-22 ("a gate dielectric 230 and a gate structure 232 are formed over the second insulation layer 228"); SAMSUNG-1015 (Shieh), [0041] ("a substrate 1 with fins 4, shallow trench isolations (STIs) 6, a gate dielectric 9, and a gate electrode layer 8 formed thereon"), [0046]-[0047]. Indeed, the '306 Patent itself acknowledges that this was conventional: *see* SAMSUNG-1001, 3:49-4:49 (acknowledging that in "a

conventional finFET or tri-gate process fabrication scheme," "the dummy gate electrode … is replaced with permanent gate electrodes" and "a dummy gate dielectric layer may also be replaced by a permanent gate dielectric layer").

37. In view of the state of the art and given Xie's description of the composition of its gate structures (*see* SAMSUNG-1004 (Xie), [0038], [0015]-[0016], [0040], claims 1 and 5), it is my opinion that a POSITA would have understood or found obvious that Xie's gate structures each comprises "a stack of material layers" including a gate dielectric layer (*e.g.*, Xie's a high-k gate insulation layer) and a gate electrode (*e.g.*, Xie's bulk conductive metal layer). SAMSUNG-1004 (Xie), [0038].

38. It is my opinion that a POSITA would have been motivated to implement the "high-k … gate insulation layer" and "bulk conductive metal layer" of Xie's gate structure as a high-k gate dielectric layer and metal gate electrode, respectively, for at least the following reasons.

39. One reason why a POSITA would have been motivated to implement a high-k gate dielectric and a metal gate electrode is because gate structures having high-k gate dielectric layers and metal gate electrodes were standard elements of FinFET transistors, as I discussed above. *See*, *e.g.*, SAMSUNG-1005, 5:5-46; SAMSUNG-1025, 4:39-5:3; SAMSUNG-1011 (Gan), 3:59-4:10. The implementation of Xie's gate insulation layer and bulk conductive material layer as

a gate dielectric layer and gate electrode, respectively, is thus merely a comprehensive implementation of a structure already described by Xie.

40. Another reason why a POSITA would have been motivated to pursue the use of a high-k gate dielectric layer and a metal gate electrode is to obtain the performance advantages afforded by use of these materials. For instance, high-k gate dielectrics decrease threshold voltage, reduce fringe capacitance, and suppress leakage current. *See* SAMSUNG-1011 (Gan), 1:32-35 ("There has been a desire to replace the gate oxide and polysilicon gate electrode with a high-k gate dielectric and metal gate electrode ***to improve device performance as feature sizes continue to decrease***."); SAMSUNG-1026 (Guo), Abstract ("A high-k dielectric is used for the gate dielectric, providing increased inversion carrier density without having to resort to aggressive scaling of the thickness of the gate dielectric while at the same time preventing excessive gate leakage current from occurring.."); SAMSUNG-1027 (Lee), 1:38-46 ("methods have been sought to reduce leakage current while achieving a high gate capacitance. One method investigated by the industry is the use of materials having a high dielectric constant (high-k or high-∈) for the gate dielectric layer."); SAMSUNG-1028 (Metz), Abstract ("The high-k gate dielectric layer has off-state leakage characteristics that are superior to those of a silicon dioxide based gate dielectric, and on-state mobility characteristics that are superior to those of a high-k gate dielectric that comprises an isotropic material.).

Moreover, the use of a high-k gate dielectric layer provides the gate with finer control over the channel potential, enabling more effective on/off control to be achieved, thus facilitating higher speed performance. *See* SAMSUNG-1028 (Metz), Abstract.

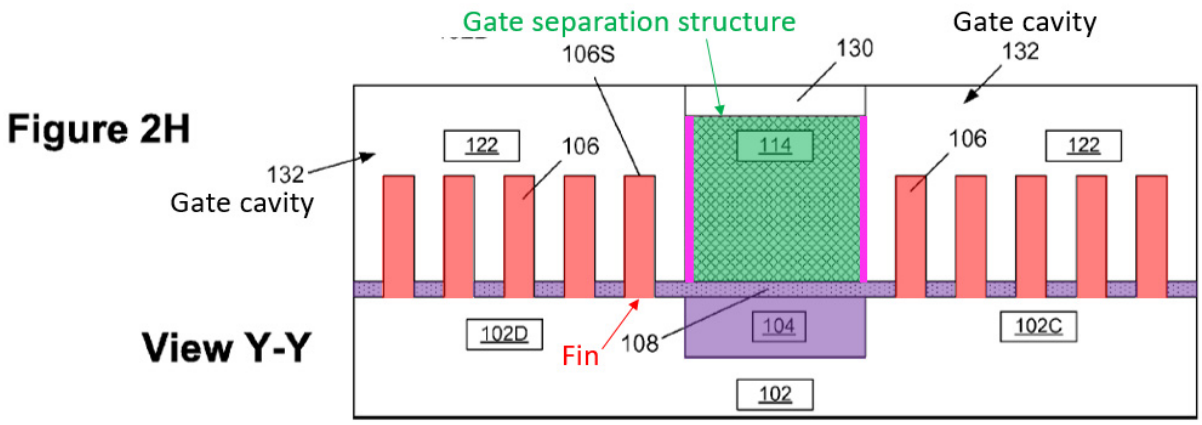
41. Additionally, a POSITA would have been motivated to use high-k gate dielectric layers and metal gate electrodes because this implementation is just the application of known techniques (*e.g.*, high-k gate dielectric layers and metal gate electrodes) to a known structure (*e.g.*, the gate insulation layer and bulk conductive metal layer of the gate structure of Xie's FinFET device) that results in a predictable outcome (*e.g.*, a gate structure having a high-k gate dielectric layer and a metal gate electrode).

42. It is my opinion that a POSITA would have expected success in high-k gate dielectric layers and metal gate electrodes because these materials are consistent with Xie's description of the composition of its gate structures. *See* SAMSUNG-1004 (Xie), [0038] ("a high-k (k value greater than 10) gate insulation layer," "one or more metal layers," and "a bulk conductive metal layer"). It is also my opinion that a POSITA also would have expected success given that high-k gate dielectric layers and metal gate electrodes are well-known elements of both replacement gate structures and gate-first gate structures for FinFET devices. *See* SAMSUNG-1005 (Tseng), 5:5-46, 8:67-9:4, FIG. 5A; SAMSUNG-1025 (Ching),

4:39-5:3, FIG. 9A; SAMSUNG-1006 (Anderson), [0029]; SAMSUNG-1011 (Gan), 3:59-4:10; SAMSUNG-1012 (Bohr), 4:46-48 SAMSUNG-1013 (Chuang), 3:45-46; SAMSUNG-1014 (Kuo), 7:8-22; SAMSUNG-1015 (Shieh), [0041], [0046]-[0047].

### 3. Structure of Xie's gate structures when formed by a gate-last process

43. Xie describes that its gate structures can be "replacement gate structure[s]" formed using "gate-last (replacement gate) manufacturing techniques." SAMSUNG-1004 (Xie), [0038]; *see* [0030]. As described by Xie, the replacement gate structures are formed by first removing a sacrificial gate structure "so as to define a gate cavity 132 where the final gate structure … will be formed." SAMSUNG-1004 (Xie), [0034]-[0038], FIGS. 2E-2H. At least one end of the gate cavity 132 is defined by the sidewalls (which I have outlined in pink) of Xie gate separation structure 114. *See id.*, FIG. 2H, reproduced below. Then, a "replacement gate structure" is "formed in the gate cavities. *Id.*, [0038], FIG. 2I-2H.

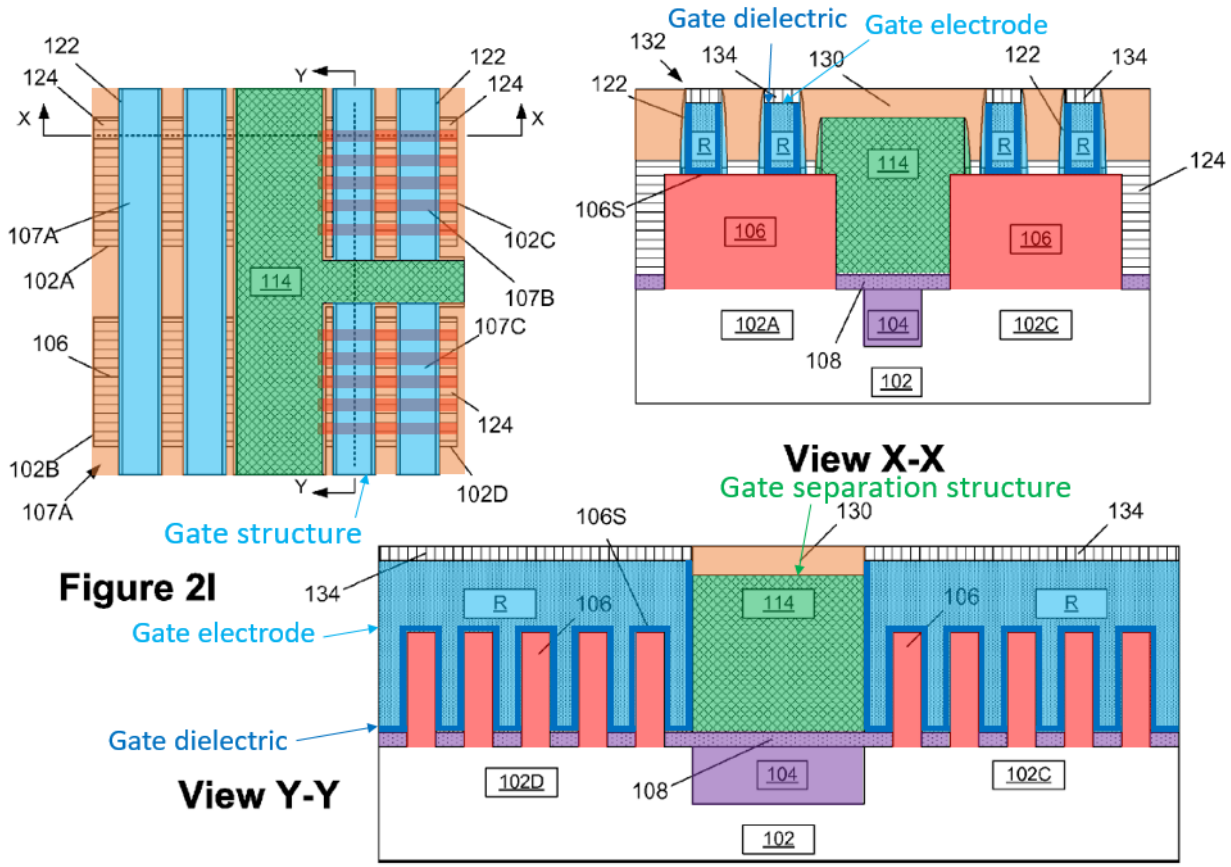



Excerpt from Xie, FIG. 2H (annotated)

44. Given that Xie's gate structures are implemented to include a gate dielectric layer and a gate electrode, as I discussed previously, it is my opinion that a POSITA would have understood or found obvious that formation of a replacement gate involves first depositing the gate dielectric layer into the gate cavity and then the gate electrode onto the gate dielectric layer. SAMSUNG-1004 (Xie), [0038], FIG. 2I; *see* SAMSUNG-1025 (Ching), 4:39-5:56 ("First, gate dielectric layer 50 is formed in recess 44 … and on the top surfaces and sidewalls of semiconductor fins 48. … Next, conductive material 52 is formed over gate dielectric layer 50, and fills the remaining recess 44."), FIG. 8A); SAMSUNG-1005 (Tseng), 8:62-9:4 ("the gate-last process comprises … fill[ing] the trench with a gate dielectric layer and a conductive gate electrode layer"); SAMSUNG-1015 (Shieh), [0045]-[0047] ("The gate dielectric 9 may be formed on the fins"

and "[t]he gate electrode layer 8 may be formed over the gate dielectric 9"); SAMSUNG-1012 (Bohr), 11:4-14; SAMSUNG-1014 (Kuo), 7:8-42; .

45. As illustrated in the composite figure below, when the gate dielectric layer (dark blue) is deposited into the gate cavity left by removal of the sacrificial gate material, the gate dielectric layer is coated onto exposed surfaces in the gate cavity, including onto the fins and onto the exposed sidewalls (pink in Xie's FIG. 2H above) of the gate separation structure. *See* SAMSUNG-1025 (Ching), 4:39-5:56; SAMSUNG-1040 (Kelly), 6:33-38, FIGS. 7A-7B (showing the gate dielectric layer 704 coating onto exposed sidewalls of an opening formed by removing a dummy gate structure); SAMSUNG-1036 (Liaw), [0023] ("a high-k dielectric layer 118 is formed over the upper portions 106 of the fin structures 104 as well as the rest of the opening 116 left by removal of the dummy gates 110, 111"), FIG. 1F. The gate electrode (light blue) is disposed on the gate dielectric layer.




Xie composite figure – Replacement gate structure

46. I note that this composite figure (as well as other composite figures I include in this declaration) is just one example that a POSITA would have found to be obvious. I provide such composite figures for illustrative purposes only. It is my opinion that other example configurations could be conceived that also would have been obvious and that would render the challenged claims obvious for similar reasons as those discussed herein.

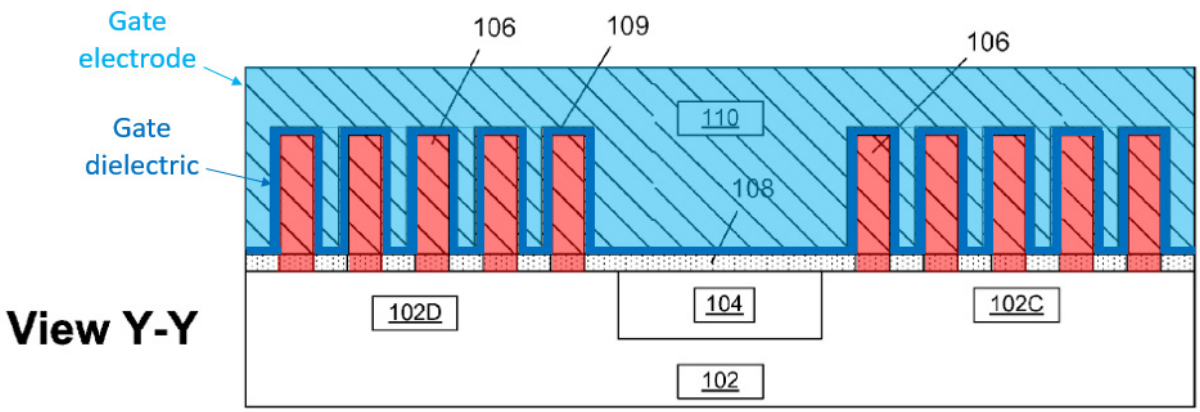
#### 4. Structure of Xie's gate structures when formed by a gate-first process

47. Xie alternatively indicates that its gate structure can be "a stack of material layers" formed using "gate-first … techniques." SAMSUNG-1004 (Xie), [0030], claim 1; *see* [0039]-[0040], claim 5 ("wherein said plurality of gate structures are final gate structures").

48. A gate-first fabrication process is similar to the process of forming a sacrificial gate structure, such as the process Xie describes for forming the sacrificial gate structures 107. *See* SAMSUNG-1004 (Xie), [0030]-[0035], FIGS. 2B-2F. "[T]he stack of materials … that will comprise the gate structure" "are blanket-deposited across all of the active regions." SAMSUNG-1004 (Xie), [0040], FIG. 2B.

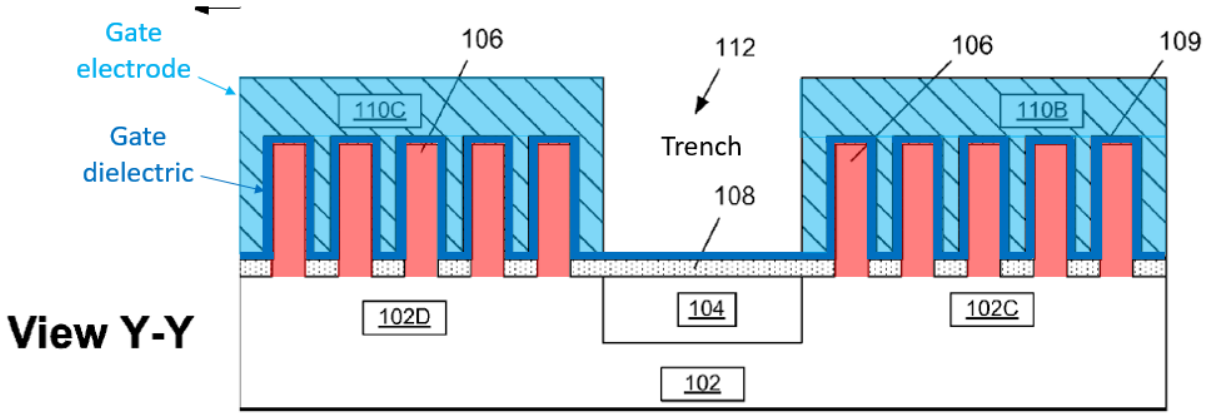
49. Given that Xie's gate structures are implemented to include a gate dielectric layer and a gate electrode, as I discussed previously, it is my opinion that a POSITA would have understood or found obvious that in the context of a gate-first process, depositing this stack of materials involves first depositing the gate dielectric layer and then depositing the gate electrode onto the gate dielectric layer. *See* SAMSUNG-1005 (Tseng), 5:12-14 (a "gate dielectric layer 212 and gate electrode layer 214 are sequentially deposited over the substrate,") 8:59-60 ("In the depicted embodiment, the gate stack 210 is fabricated using a gate-first process"); *see* SAMSUNG-1017 (Basker), 4:7-35 ("a gate structure 14 may be formed over a

portion of the first and second fins 102, 202. … The embodiment described below uses a gate first process flow. At this point of the manufacturing process, the gate structure 14 may include a gate dielectric 18, a metal gate 12 and a gate cap 16. … The metal gate 12 may be formed on top of the gate dielectric 18"), Fig. 2; SAMSUNG-1016 (Cheng), 11:37-12:20 ("Each of the gate structures 20a, 20b may be formed using deposition, photolithography, and etch processes. More specifically, in some embodiments, at least one gate dielectric layer for the gate dielectrics 21a, 21b may be deposited … In some embodiments, following the formation of the at least one gate dielectric layer, at least one gate conductor layer for the gate conductors 22a, 22b may be formed on the at least one gate dielectric layer to provide a gate stack"), 22:7-8 ("FIGS. 1-5 depict methods of forming a semiconductor devices using a gate first process"), Fig. 5. The first-deposited gate dielectric layer thus coats the fins as well as the insulating material 108 disposed on the surface of the substrate, and the gate electrode is disposed on top of that gate dielectric layer to form the gate stack. This interim structure is shown in the composite figure based on the Y-Y view of Xie's FIG. 2B, below.



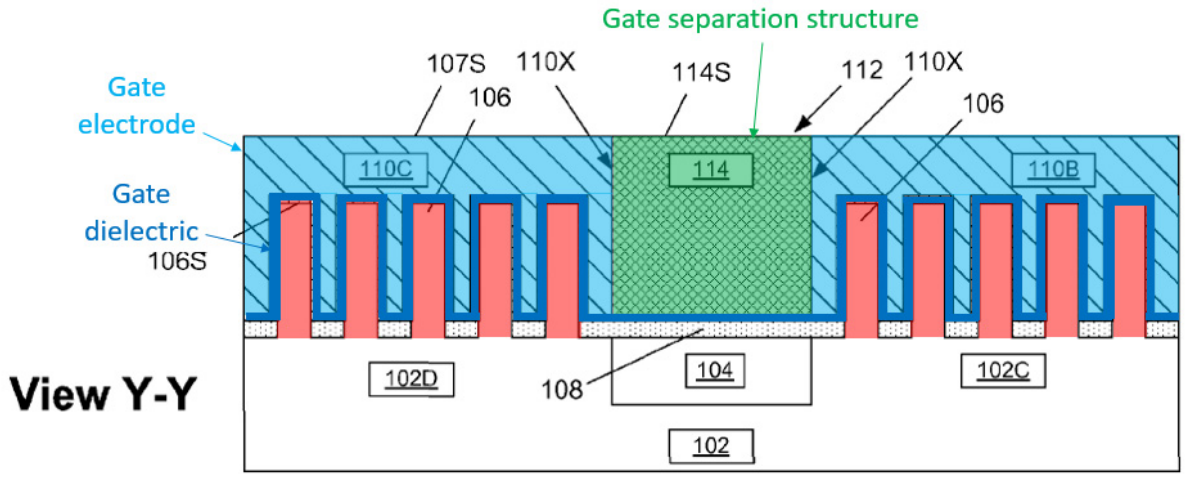

Composite figure based on Xie's FIG. 2B

50. The gate stack then is etched "to form … trenches 112 through the stack of materials," thus "defin[ing] what will become the end surfaces 110X of the gate structures." SAMSUNG-1004 (Xie), [0040], FIG. 2C; *see* SAMSUNG-1005 (Tseng), 5:47-55. The etch through the stack of materials exposes both the gate dielectric layer and the gate electrode at these end surfaces. This interim structure is shown in the composite figure below that is based on Xie's FIG. 2C. *See* SAMSUNG-1005 (Tseng), FIG. 5A; SAMSUNG-1016 (Cheng), FIG. 13 (showing gate dielectric 301 and gate conductor 302 exposed at the end of gate structure 300 fabricated "using a gate first process," 22:7-8; *see* 19:41-20:16); SAMSUNG-1017 (Basker), FIG. 2 (showing a gate dielectric 18 and metal gate 12 exposed at the end of gate structure 14 fabricated "using a gate first process flow," 4:7-16).



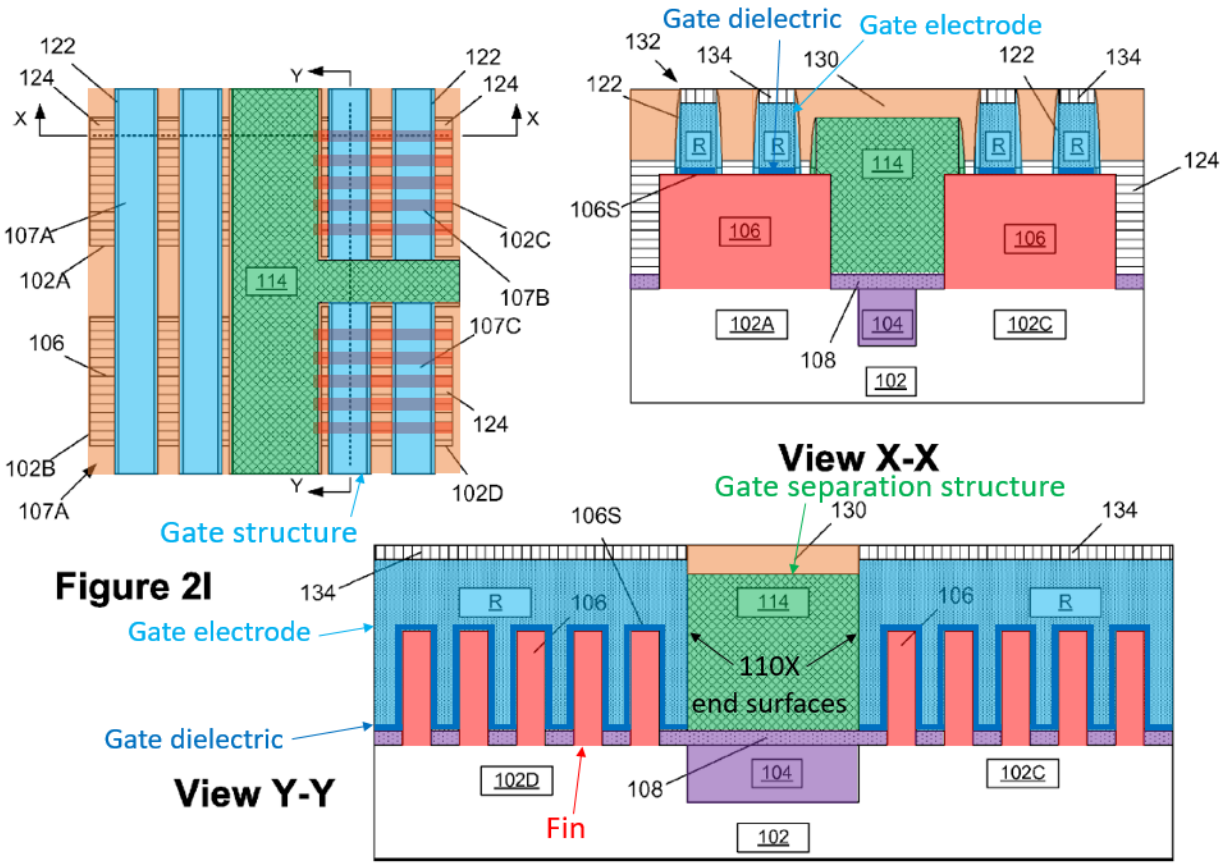

Composite figure based on Xie's FIG. 2C

51. The "gate separation structure 114" is "formed in the spaced apart trenches," between the end surfaces 110X of the gate structures, and thus contacts both the gate dielectric layer and the gate electrode that are exposed at these end surfaces. SAMSUNG-1004 (Xie), [0040], FIG. 2D. This is illustrated in the composite figure below that is based on Xie's FIG. 2D.




Composite figure based on Xie's FIG. 2D

52. An example of a resulting gate-first gate structure is shown in the composite figure below, which is based on Xie's FIG. 2. In this gate-first gate structure, the gate dielectric layer (dark blue) and the gate electrode (light blue) are exposed at the end surfaces 110X of the gate structures. The gate separation structure, disposed between the gate structures, contacts these end surfaces, as shown in the Y-Y cross-sectional view.




Xie composite figure – Gate-first gate structure

### 5. Claim-by-Claim Analysis

#### (1) Claim 26

**[26pre] An integrated circuit structure, comprising:**

53. To the extent the preamble is deemed to be limiting, it is my opinion that Xie renders it obvious. Xie describes an integrated circuit structure. *See* SAMSUNG-1004 (Xie), [0002] ("The present disclosure generally relates to the fabrication of ***integrated circuits***, and more particularly, to various methods of forming ***gate structures for FinFET devices and the resulting semiconductor devices***."), [0027] ("FIGS. 2A-2O depict various illustrative methods disclosed herein for forming ***gate structures for FinFET devices and resulting devices***. … The illustrative FinFET devices that are depicted in the attached drawings may be either ***NMOS or PMOS devices***."), [0027] ("The illustrative integrated circuit product 100 depicted in the drawings"), [0039] ("FIGS. 2J-2M depict one illustrative example where the methods disclosed herein may be employed to manufacture ***integrated circuit products***"), [0015], [0026].

**[26a] a first fin comprising silicon, the first fin having a longest dimension along a first direction;**

**[26b] a second fin comprising silicon, the second fin having a longest dimension along the first direction;**

54. Xie renders obvious [26a] and [26b]. For instance, Xie renders obvious **first and second fins**, *e.g.*, Xie's fins 106, some of which I have

highlighted in red in Xie's FIG. 2I, reproduced below.[4] *See* SAMSUNG-1004 (Xie), [0028] ("Next, a plurality of trenches 105 were formed in the substrate 102 to thereby define ***a plurality of fins 106***. The illustrative FinFET devices disclosed herein will be depicted as being comprised of five illustrative ***fins 106***."), [0029] ("the overall size, shape, and configuration of the trenches 105 and ***fins 106*** may vary depending on the particular application"), [0017] ("first and second spaced-apart active regions formed in a semiconductor substrate, wherein ***each of the active regions includes at least one fin***"), [0040] ("The active regions and ***the fins 106*** are depicted in dashed lines in FIGS. 2K-2N"), [0016], [0018], [0027]; claims 9, 11, 1; Figs. 2A-2O.

[4] The X-X cross-sectional view of FIG. 2I depicts fins 106 other than those I specifically identify as the first and second fins. It is my opinion that a POSITA would have understood that a cross-sectional view taken through the identified first fin or the second fin, in a plane parallel to the X-X plane marked in FIG. 2I, would be substantially the same as the illustrated X-X cross-sectional view.

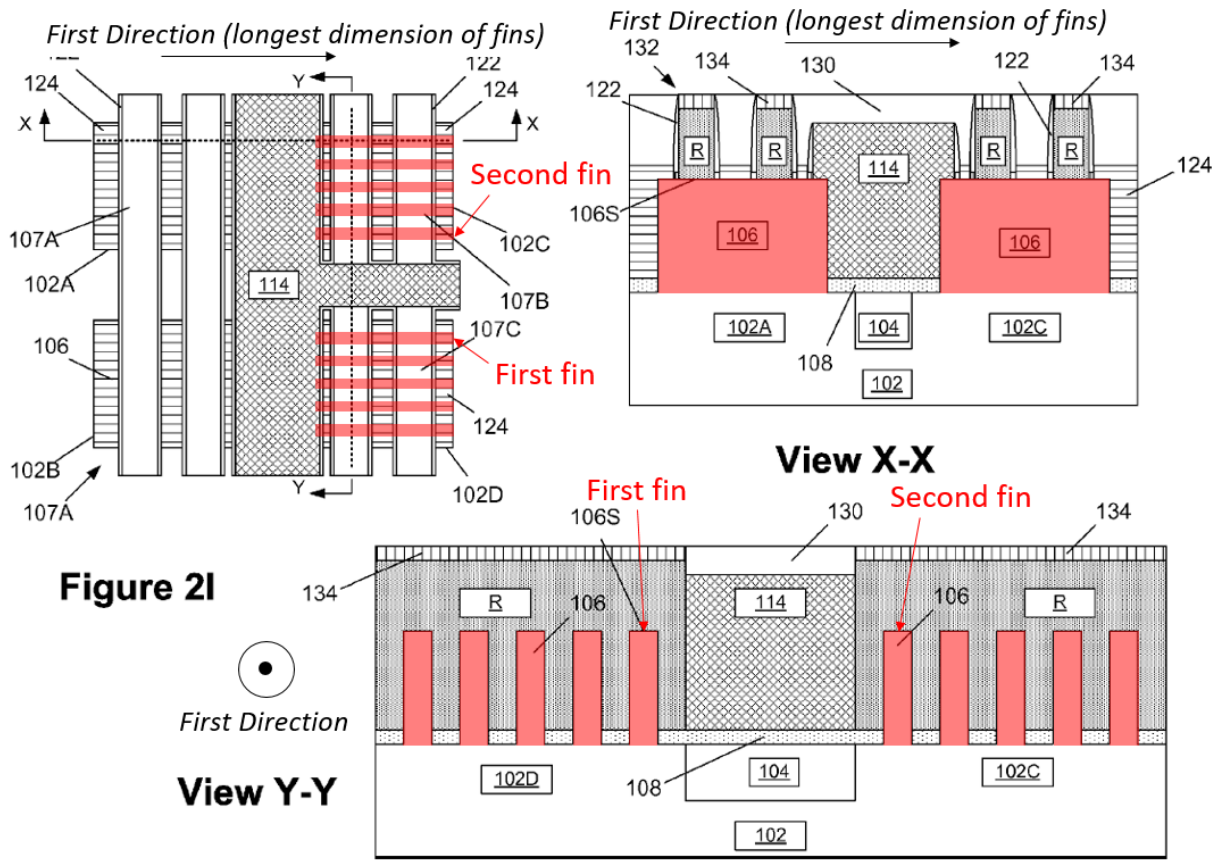



Figure 2I

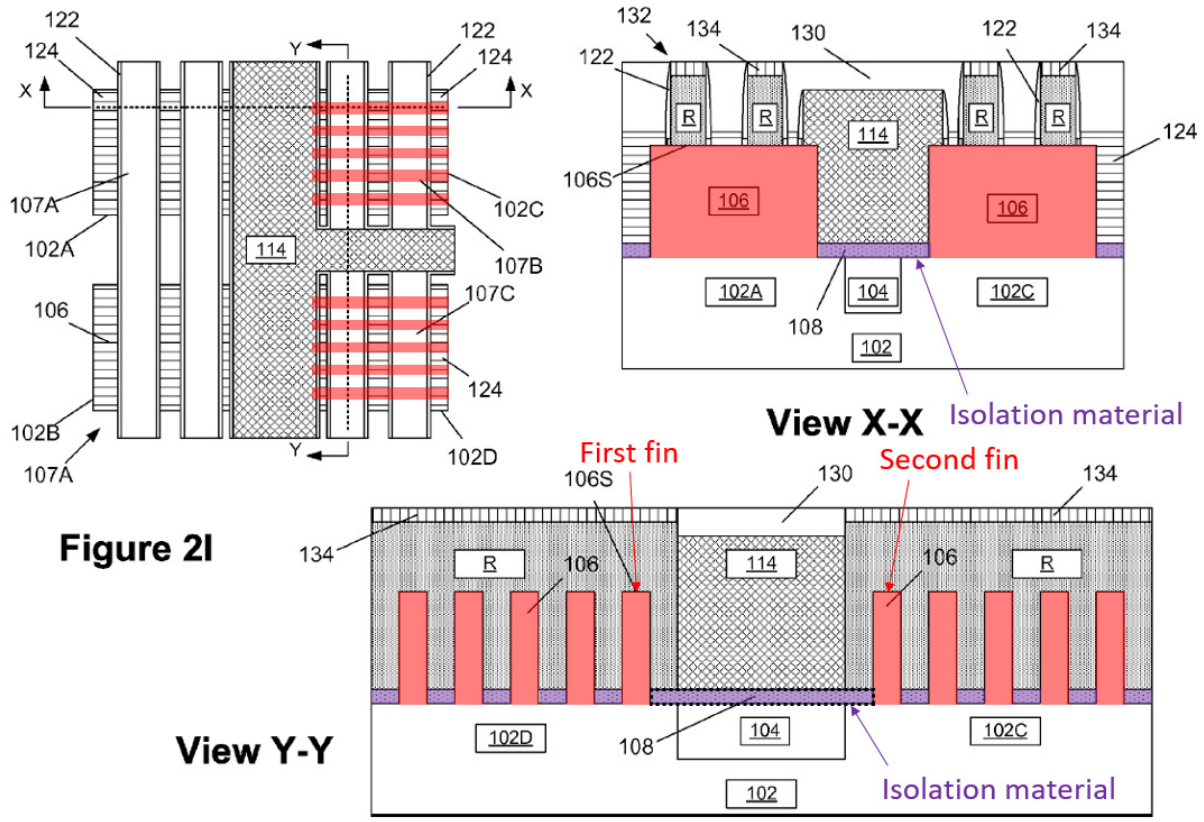
Excerpt from Xie, FIG. 2I (annotated)

55. Each fin has a longest dimension along a first direction, which I have marked in each of the views of FIG. 2I. *See* SAMSUNG-1004 (Xie), [0027] ("the view 'X-X is taken along a line that passes through the fins 106, while the view 'Y-Y' is a cross-section view that is taken transverse to the long axis of the fins 106."). As shown, the first direction extends left to right in the top view and X-X cross-sectional view, and into the page of the Y-Y cross-sectional view. This longest dimension is along the first direction in that the longest dimension of the fins is traversed as one moves along the fins in the first direction.

56. Xie renders obvious that **the first and second fins comprise silicon**, *e.g.*, as made apparent by Xie's fabrication process. Xie's "integrated circuit product 100 … is formed above an illustrative substrate 102" such as a "bulk silicon" substrate. SAMSUNG-1004 (Xie), [0037]; *see also id.* ("The substrate 102 may be made of silicon"). To form the fins 106, "a plurality of trenches 105 were formed in the substrate 102 to thereby define a plurality of fins 106." SAMSUNG-1004 (Xie), [0028], FIG. 2A. The remaining portions of the silicon substrate that are separated by the trenches constitute the fins. That is, the fins are formed from the silicon substrate and thus have the same composition as the substrate, *i.e.*, the fins include silicon.

**[26c] an isolation material between the first fin and the second fin;**

57. Xie renders obvious [26c]. For instance, Xie renders obvious **an isolation material**, *e.g.*, Xie's insulating material 108, which I have highlighted in purple in FIG. 2I, reproduced below. *See* SAMSUNG-1004 (Xie), [0028] ("***the insulating material 108*** only remains in the bottom of the trenches 105 so as to ***locally isolate the fins 106*** from one another"), [0039] ("FIG. 2J depicts the device at a point in fabrication where the fins 106 and the ***local isolation material*** 108 have been formed."), FIGS. 2A-2I, FIG. 2J. The insulating material 108 is **an isolation material** at least because it "locally isolate[s] the fins 106 from one another." *Id.*, [0028].

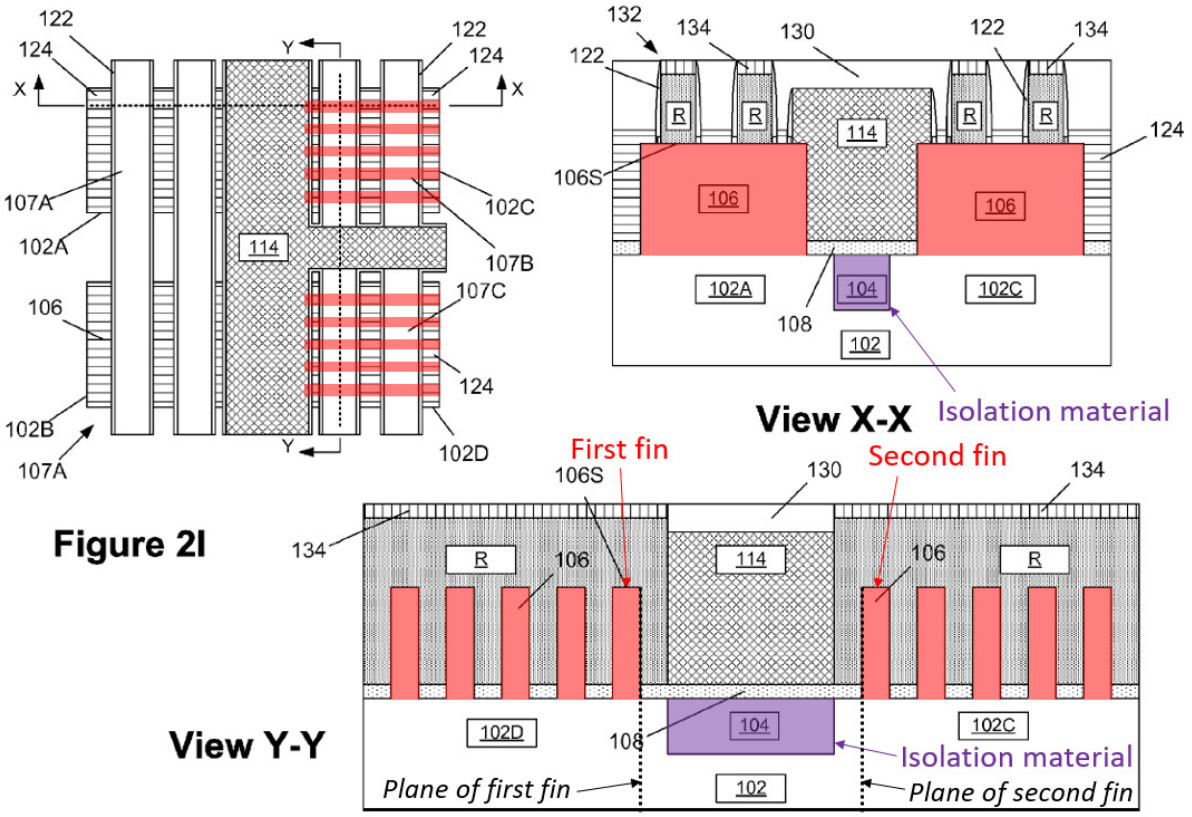



Excerpt from Xie, FIG. 2I (annotated)

58. Xie renders obvious that the **isolation material**, *e.g.*, Xie's insulating material 108, is **between the first fin and the second fin**, as illustrated in FIG. 2I, above. For instance, at least the portion of the insulating material 108 that is outlined in dashed lines in the Y-Y view is **between the first and second fin** in that it is disposed in the space separating the two fins. Moreover, the positioning of the isolation material between the first and second fins is confirmed by Xie's description of the manufacturing process. Specifically, Xie describes that the insulating material 108 is disposed in the trenches that separate the fins, and thus

the insulating material itself is in the space separating the fins, *i.e.*, between the fins. *See* SAMSUNG-1004 (Xie), [0028] ("a layer of insulating material 108 was deposited on the substrate 102 so as to over-fill the trenches 105. Then, a recess etching process was performed on the layer of insulating material 108 such that the insulating material 108 only remains in the bottom of the trenches 105 so as to locally isolate the fins 106 from one another"), FIG. 2A.

59. Alternatively or additionally, Xie renders obvious **an isolation material**, *e.g.*, in view of Xie's isolation structure 104, which I have highlighted in purple in Xie's FIG. 2I, reproduced again below. *See* SAMSUNG-1004 (Xie), [0028] ("a plurality of active regions 102A-D were defined in the substrate 102 by the formation of ***isolation structures 104***"), [0039], FIGS. 2A-2I. The isolation structure is **isolation material** in that it separates (*e.g.*, isolates) active regions.




Excerpt from Xie, FIG. 2I (annotated)

60. Xie renders obvious that the isolation material, *e.g.*, Xie's isolation structure 104, is **between the first fin and the second fin**, as illustrated in FIG. 2I. For instance, the isolation structure 104 is between the first and second fins because it is disposed in the space separating the fins. Specifically, each fin defines a plane, *e.g.*, the plane of its inward-facing edge. I have marked these planes in dotted lines in the Y-Y view of the FIG. 2I reproduction above. The isolation structure 104 is between the fins 104 in that the isolation structure 104 is disposed in the space separating the plane defined by the first fin and the plane defined by the second fin.

**[26d] a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;**

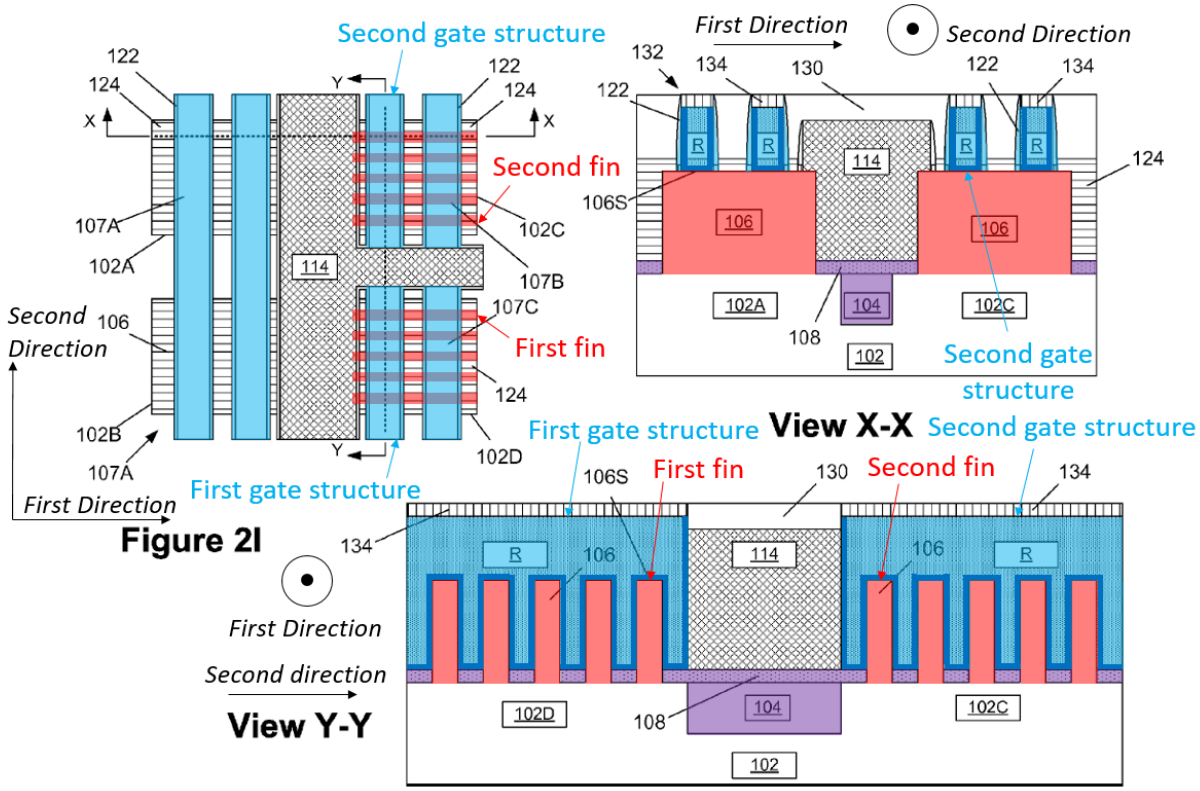
**[26e] a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;**

*Xie renders obvious first and second gate structures*

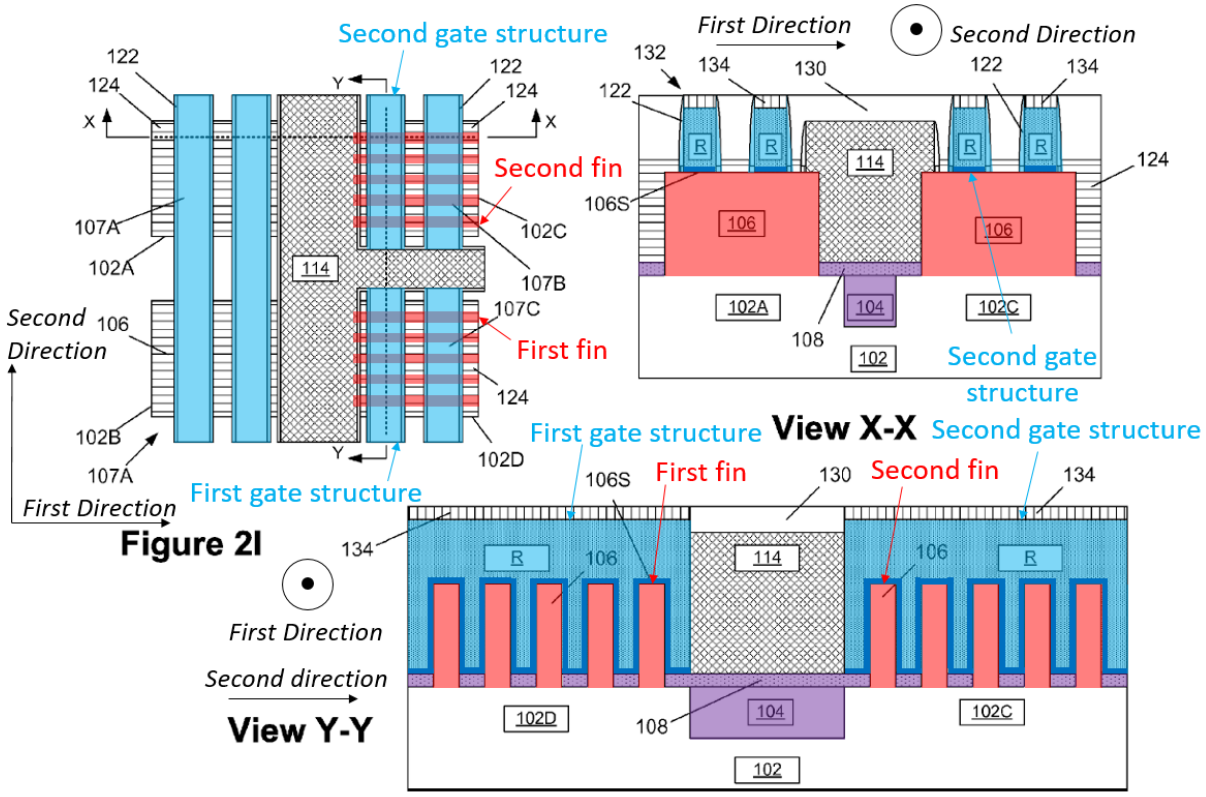
61. Xie renders obvious [26d] and [26e]. For instance, Xie renders obvious **first and second gate structures**, *e.g.*, Xie's "***final gate structures***," which I have highlighted in blue in the two composite figures below. SAMSUNG-1004 (Xie), [0030]; *see* [0017] ("***first and second spaced-apart gate structures***").

62. The first and second gate structures (*e.g.*, Xie's "final gate structures") "may be formed using either gate-first or gate-last techniques." *Id.* The first composite figure illustrates a "replacement gate structure" made by a gate-last technique (SAMSUNG-1004 (Xie), [0038]); the second composite figure illustrates a gate structure made by a gate-first process. *See also* SAMSUNG-1004 (Xie), [0040] ("the stack of materials 140S that will comprise ***the gate structure 140*** (be it a final gate structure or a sacrificial gate structure) are blanket-deposited," and "[t]he formation of the trenches 112 defines what will become the end surfaces 110X of the ***gate structures 140***"), claims 1 and 5 ("forming a stack

of material layers to form said plurality of gate structures," "wherein said plurality of gate structures are final gate structures"), [0002] ("methods of forming ***gate structures*** for FinFET devices"), [0013]-[0016], [0027], [0041], FIG. 2I, FIGS. 2K-2O, claims 9, 11, and 16.

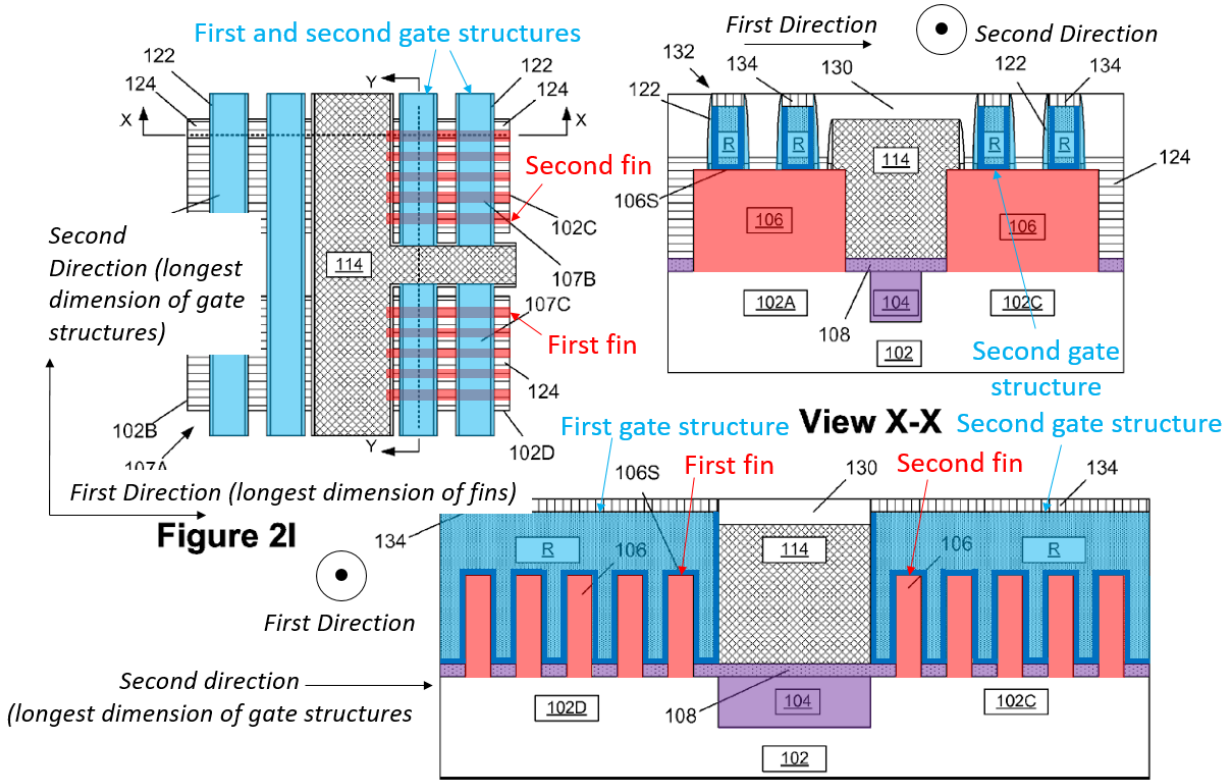



Xie composite figure – Replacement gate structure




Xie composite figure – Gate-first gate structure

63. As illustrated in these composite figures, the first and second gate structures have **a longest dimension along a second direction** in that the longest dimension of the gate structures is traversed ***as one moves along the gate structures in the second direction*** (from top to bottom in the top view, from left to right in the Y-Y cross-sectional view, and into the page in the X-X cross-sectional view). *See* SAMSUNG-1004 (Xie), FIG. 2I. I have specifically identified this longest dimension in the replacement gate structure composite figure, which I reproduce again here:




Xie composite figure

64. The composite figures also illustrate that **the second direction is orthogonal to the first direction**, *e.g.*, the gate structures extend in a direction orthogonal to the extension of the fins. *See* SAMSUNG-1004 (Xie), FIG. 2I. To the extent that Xie does not explicitly state this orthogonality, it is my opinion that a POSITA would have understood this to be the case, or otherwise found this to be obvious, consistent with the schematic depiction of Xie's structure in FIG. 2I and given that gate structures orthogonal to fins in FinFET devices was well-known in the art as of the Critical Date. *See*, *e.g.*, SAMSUNG-1008 (Kawa), [0053] ("gate traces … which are elements of the patterned gate conductor layer, and are

disposed over and orthogonal to the set of fins"); SAMSUNG-1029 ( Zhu), [0042] ("The patterned second gate conductor 106 intersects the semiconductor fin and extends, e.g., along a direction perpendicular to a length direction of the semiconductor fin 102."); SAMSUNG-1030 (Basker), Abstract ("The fin structures each comprise a semiconductor layer and extend in a first direction, and the gate stack extends in a second direction that is perpendicular.").

*Xie renders obvious the recited positioning of the gate structures*

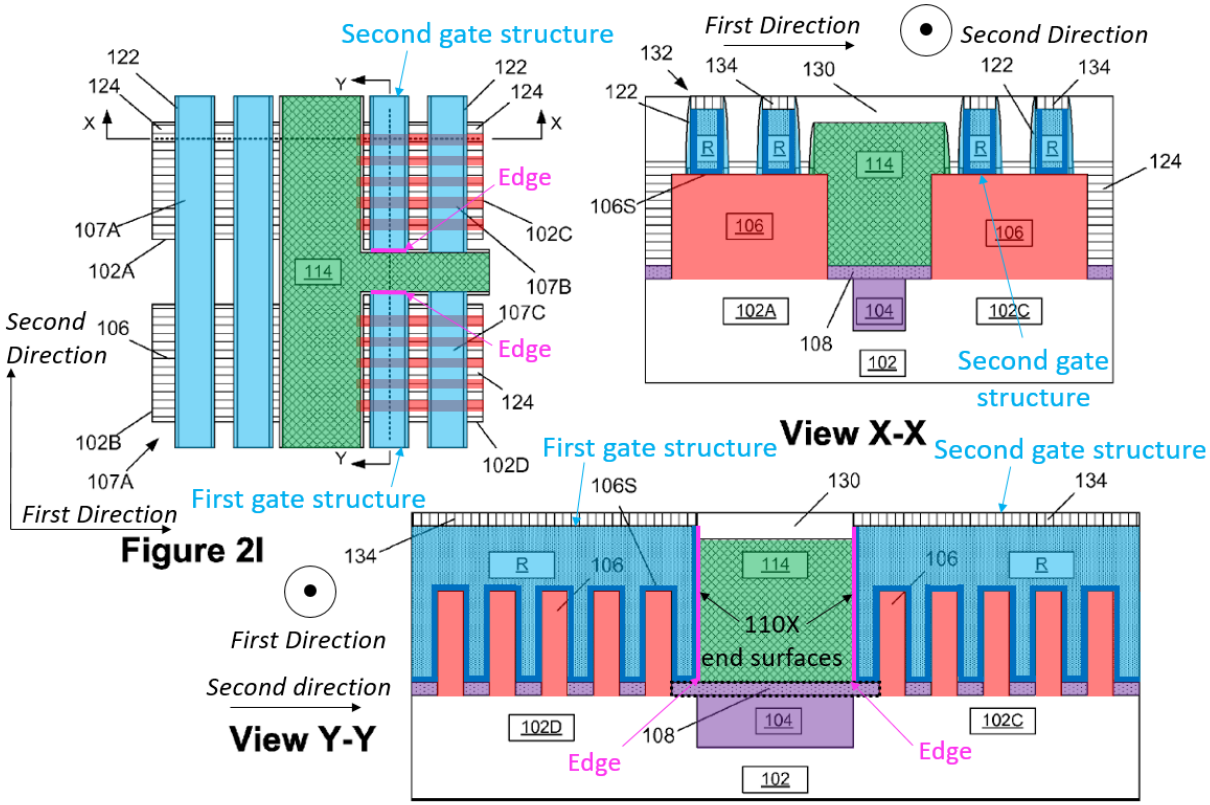
65. Xie renders obvious that **the first gate structure is over the first fin** and **the second gate structure is over the second fin**, as illustrated in the composite figures above. For instance, Xie describes its device as including "first and second spaced-apart active regions formed in a semiconductor substrate, wherein ***each of the active regions includes at least one fin***, [and] first and second spaced-apart ***gate structures positioned above said first and second active regions***." SAMSUNG-1004 (Xie), [0017]; *see also* [0016] ("forming a stack of material layers to form ***a plurality of gate structures above a plurality of spaced-apart active regions*** defined in a semiconductor substrate, wherein ***each of the active regions have at least one fin*** formed thereabove"), [0040] ("the stack of materials 140S that will comprise the gate structure 140 (be it a final gate structure or a sacrificial gate structure) are blanket-deposited across all of the active regions"), [0015], [0018], [0041], FIG. 2I, FIGS. 2K-2O; claims 9, 11, 16.

66. The positioning of the gate structures over the respective fins is also made apparent by Xie's description of the replacement gate fabrication process. Specifically, Xie describes that the gate structures are formed in cavities within which the fins are exposed. *See* SAMSUNG-1004 (Xie), [0037]-[0038], FIG. 2H. Thus, when the gate stack is deposited into the cavity, it is deposited over the fins that are exposed in that cavity.

67. Xie also renders obvious that **the second gate structure is discontinuous with the first gate structure**, as illustrated in the composite figure of the replacement gate structure, reproduced again below.[5] As shown, the first and second gate structures (blue) are **discontinuous** at least because they are separated by a gate separation structure 114 (green; *see* [26f]). *See* SAMSUNG-1004 (Xie), [0017] ("first and second ***spaced-apart gate structures*** …, and a gate separation structure positioned between the first and second spaced-apart gate

[5] The applicability of Xie's gate-first implementation to the features of the Challenged Claims is identical to the applicability of the replacement gate implementation, except where I state otherwise. Where the applicability is identical, I only discuss the replacement gate implementation explicitly. However, I note that Xie's gate-first implementation renders these features obvious for at least similar reasons.

structures"), [0031]-[0032] ("a transverse 'cut' 115 of the gate stack material layer(s) is first performed to define the ends 110X of what will become the sacrificial gate structures 107" (in a replacement gate process; or final gate structures in a gate-first process), and "a gate separation structure 114 [is] formed in the opening"), [0040] ("The formation of the trenches 112 defines what will become the end surfaces 110X of the gate structures 140. … [a] gate separation structure [is] formed in the spaced apart trenches"), [0015]-[0016], [0018], [0041], FIG. 2I, FIGS. 2K-2O, claims 1, 9, 11, 16.




Xie composite figure – Replacement gate structure

68. As shown in the composite figure above, the discontinuity between the first and second gate structures is **along the second direction**: the discontinuity is reached ***as one moves in the second direction*** from one gate structure to the other (top to bottom in the top view figure, or left to right in the Y-Y cross-sectional view). *See* SAMSUNG-1004 (Xie), FIG. 2I.

69. The composite figures also illustrate that **the second gate structure has an edge** (outlined in pink) **that faces an edge** (also outlined in pink) **of the first gate structure**. For instance, the edge (pink) of the second gate structure (blue) that contacts the gate separation structure (green) faces the edge (pink) of the first gate structure (blue) that also contacts the gate separation structure (green). Moreover, I note that Xie explains that "each of the gate structures has an end surface" (*e.g.*, **an edge**), where "first and second opposing surfaces of the gate separation structure" "abut the end surfaces of first and second spaced-apart gate structures, respectively." SAMSUNG-1004 (Xie), [0016]. These gate structure end surfaces abutting the gate separation structure disposed therebetween are edges that face one another. *See* SAMSUNG-1004 (Xie), [0032] (in FIG. 2D, "***the ends 110X*** of what will become the sacrificial gate structures 107 abut the horizontal portions 114H of the gate separation structure 114"), [0041] ("the formation of the continuous trench 112 defines what will become ***the end surfaces 110X of the gate structure***"). These end surfaces 110X are marked in the composite figure above

and are illustrated in the interim structure of FIG. 2D. *See also* SAMSUNG-1004 (Xie), [0035], [0040], FIG. 2I, FIGS. 2C-2E, FIGS. 2K-2O, claims 1, 11, and 16.

70. I note that while Xie refers to the end surfaces 110X specifically in the context of the sacrificial gate structure (SAMSUNG-1004 (Xie), [0031]), the final gate structures in a replacement gate process will also have end surfaces at the corresponding location.

71. The edges (*e.g.*, end surfaces 110X) of the gate structures face one another **along the second direction**: from the edge of the first gate structure, the edge of the second gate structure is reached ***as one moves in the second direction*** (top to bottom in the top view figure, or left to right in the Y-Y cross-sectional view).

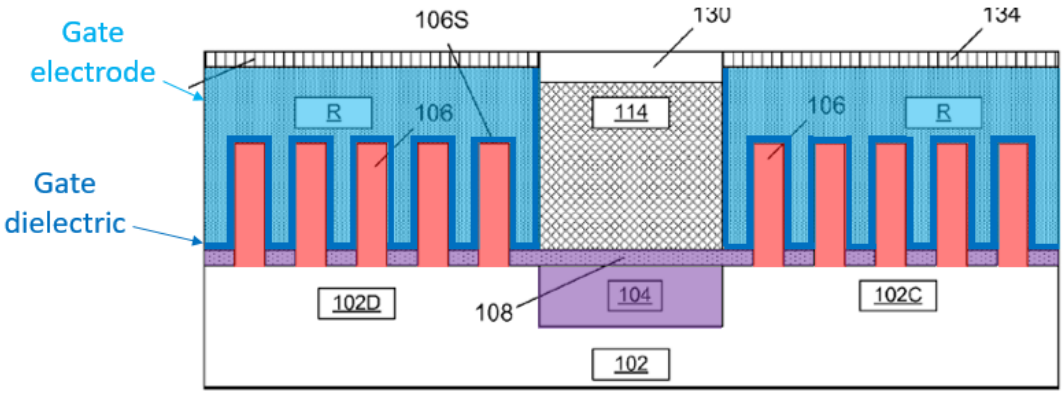
*Xie renders obvious that the gate structures each includes a gate dielectric layer and a gate electrode*

72. Xie describes that its gate structures include "a high-k (k value greater than 10) gate insulation layer," "one or more metal layers … (e.g., layers of titanium nitride or TiAlC)," and "a bulk conductive metal layer … such as tungsten or aluminum." *Id.*, [0038]; *see* [0030]. As I discussed previously, a POSITA would have understood or found obvious to implement the "gate insulation layer" and "bulk conductive metal layer" (*id.*, [0038]) of Xie's gate structures as a gate dielectric layer and a gate electrode, respectively, such that the gate structures each includes **a gate dielectric layer** and **a gate electrode**. *See* SAMSUNG-1005

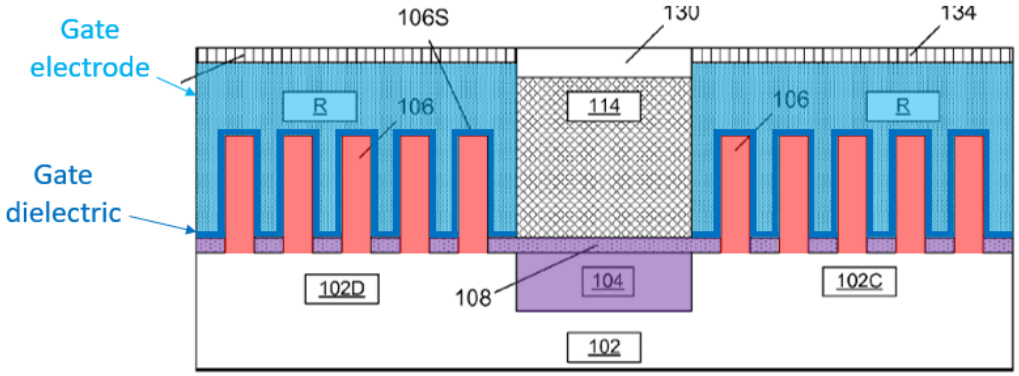
(Tseng), 5:5-46 ("The gate electrode layer 214 and the gate dielectric layer 212 form a gate stack 210"), 8:67-9:4 ("the gate-last process comprises … fill[ing] the trench with a gate dielectric layer and a conductive gate electrode layer"), FIG. 5A; SAMSUNG-1025 (Ching), 4:39-5:3 ("[t]he resulting remaining portions of the conductive material and gate dielectric layer 50 thus form the replacement gate, which includes gate electrode 52 and gate dielectric 50"), FIG. 9A; SAMSUNG-1006 (Anderson), [0029] ("The gate stack 20 can be, for example, a gate dielectric and a gate electrode material"); SAMSUNG-1011 (Gan), 3:59-4:10 ("The gate structure 110 includes a gate dielectric layer and a gate electrode"); SAMSUNG-1012 (Bohr), 4:46-54 ("The gate electrode … is a portion of a gate electrode stack which further includes a gate dielectric layer"); SAMSUNG-1013 (Chuang), 3:45-46 ("Gate electrode strip 32 and gate dielectric 145 form the gate stack of FinFET 100"); SAMSUNG-1014 (Kuo), 7:8-22 ("a gate dielectric 230 and a gate structure 232 are formed over the second insulation layer 228"); SAMSUNG-1015 (Shieh), [0041] ("a substrate 1 with fins 4, shallow trench isolations (STIs) 6, a gate dielectric 9, and a gate electrode layer 8 formed thereon"), [0046]-[0047].

73. Example implementations of the gate dielectric layer and gate electrode in a replacement gate structure and in a gate-first gate structure are shown in the two composite Y-Y cross-sectional views below. As a result of the different fabrication processes, the gate dielectric layer contacts the gate separation

structure 114 in the gate structure formed by a replacement gate process, while both the gate dielectric layer and the gate electrode contact the gate separation structure 114 in the gate structure formed by a gate-first process.




Xie composite figure – Replacement gate structure

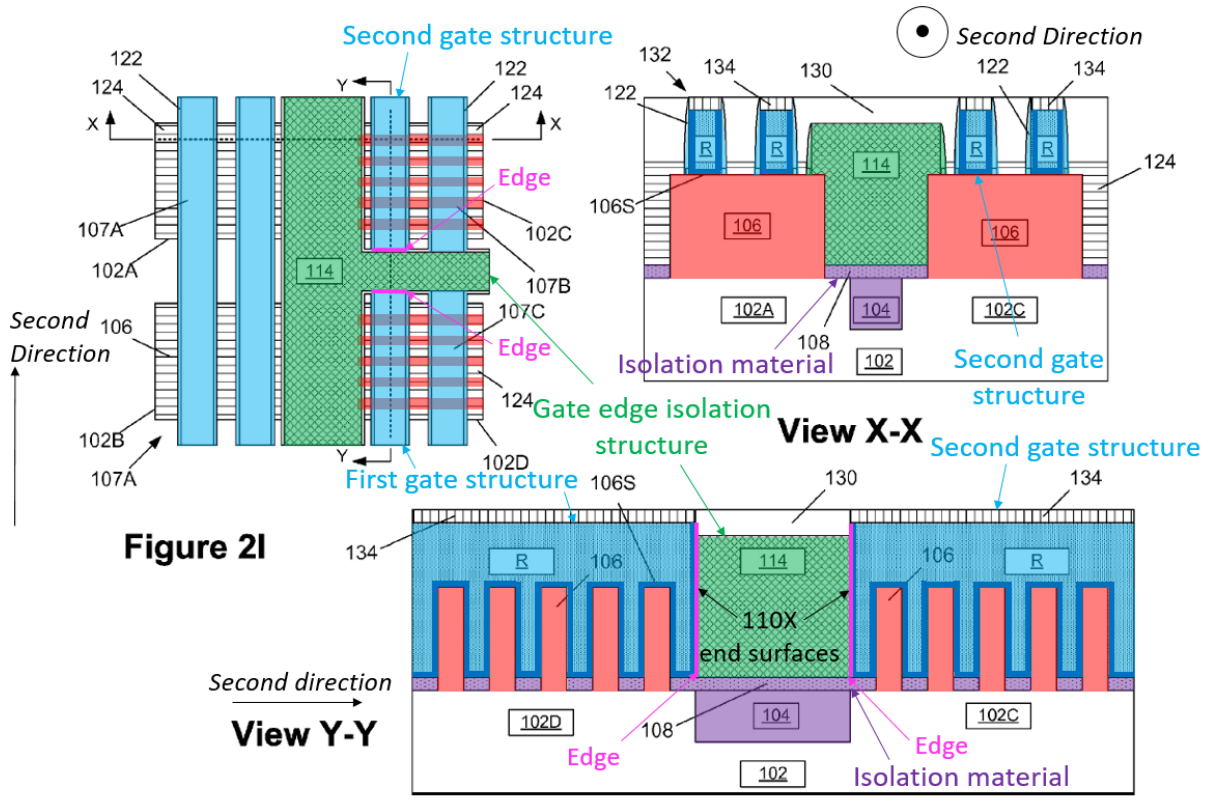



Xie composite figure – Gate-first gate structure

**[26f] a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and**

74. Xie renders obvious [26f]. For instance, Xie renders obvious **a gate edge isolation structure**, *e.g.*, Xie's gate separation structure 114, green in the

composite figure below. *See* SAMSUNG-1004 (Xie), [0032] ("a ***gate separation structure*** 114 was formed in the opening"), [0015]-[0018], [0041], claims 1-3, 6-7, 11-14, 16-17, Figs. 2D-2I, Figs. 2M-2O.




Xie composite figure – Replacement gate structure

75. A POSITA would have understood or found obvious that Xie's gate separation structure 114 is a **gate edge isolation structure**: it is disposed between and in contact with edges of gate structures (discussed below), and isolates those gate structures from one another (*e.g.*, physically and electrically).

76. For instance, Xie's gate separation structure 114 ***physically isolates*** the first and second gate structures in that it separates the two gate structures such

that the gate structures are not in physical contact. *See* SAMSUNG-1004 (Xie), [0015]-[0018], [0031]-[0032], [0035], FIGS. 2D-2I, claim 16.

77. Additionally, it is my opinion that a POSITA would have understood or found obvious that Xie's gate separation structure 114 ***electrically isolates*** the two gate structures. The gate separation structure 114 is composed of an "insulating material," such as "silicon dioxide, silicon nitride, etc." SAMSUNG-1004 (Xie), [0032]. An insulating material that is disposed between two conductive elements (the first and second gate structures) electrically isolates those conductive elements from one another. More specifically, I believe that a POSITA would recognize that an insulating gate separation structure disposed between two gate structures electrically isolates those two gate structures. *See* SAMSUNG-1009 (Chang), [0035] ("The gates may be self-aligned to isolation structures insulating gates from each other"), [0007], [0039], claim 15; SAMSUNG-1010 (Akarvardar), 7:64-8:4 ("the second isolation region 504 may electrically separate the first group of fins 104 from the second group of fins 204"). Moreover, the presence of the gate separation structure prevents "epi semiconductor material … from forming around the ends 110X of the gate structures … thereby reducing or eliminating the chance for undesirable bridging between the source/drain regions of the FinFET devices." SAMSUNG-1004 (Xie), [0035].

78. Xie renders obvious that **the gate edge isolation structure** (*e.g.*, Xie's gate separation structure 114) is **between and in contact with the edge of the first gate structure and the edge of the second gate structure**. The composite figure above illustrates this positioning, with the edges of the first and second gate structures (*e.g.*, the end surfaces 110X; *see* SAMSUNG-1004 (Xie), [0035]) outlined in pink.

79. Specifically, Xie renders obvious that the gate edge isolation structure is **between** the first and second gate structures: Xie's "gate separation structure [is] ***positioned between the first and second spaced-apart gate structures***." SAMSUNG-1004 (Xie), [0017]; *see* [0031]-[0032], [0040], [0015]-[0016], [0018], [0041], FIG. 2I, FIGS. 2L-2O.

80. Moreover, Xie also renders obvious that the gate edge isolation structure is **in contact with** the edges of the gate structures: "first and second opposing surfaces of the gate separation structure ***abut the end surfaces*** [e.g., edges] ***of first and second spaced-apart gate structures***, respectively." SAMSUNG-1004 (Xie), [0017]; *see* [0035] ("due to the presence of the gate separation structure 114 that ***contacts the end surfaces 110X of the gate structures*** 107B and 107C"), FIG. 2I, FIGS. 2L-2O.

81. The positioning of the gate edge isolation structure **between and in contact with** the edges of the first and second gate structures is further rendered

obvious by Xie's description of the fabrication process. Specifically, Xie describes that an opening is defined in a stack of gate materials, forming two discontinuous gate structures (either final gate structures or sacrificial gate structures for a replacement gate process) with exposed edges 110X. *See* SAMSUNG-1004 (Xie), [0031], FIG. 2C. The gate edge isolation structure (*e.g.*, Xie's gate separation structure 114) then is formed in that opening, *i.e.*, between the gate structures and in contact with their exposed edges. *See id.*, [0032], [0038], FIG. 2D, FIG. 2H.

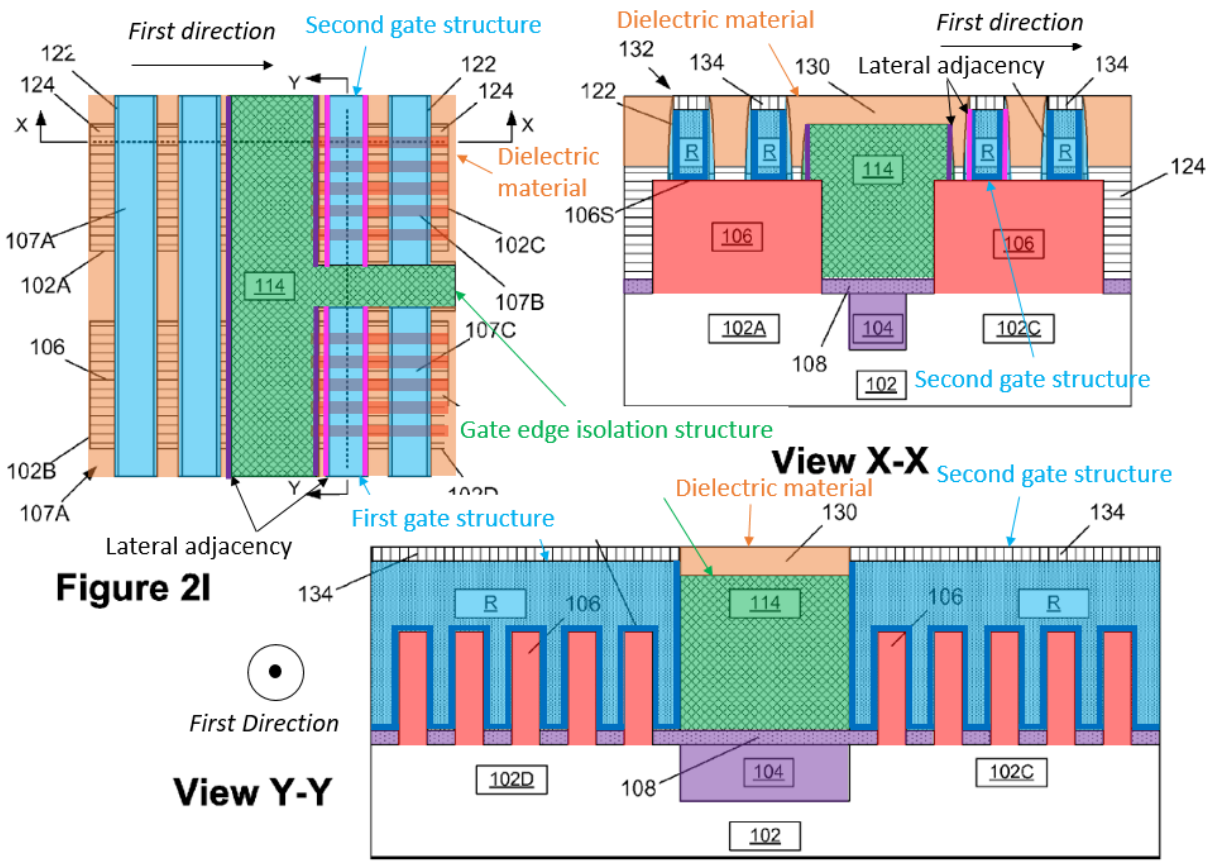
82. The gate edge isolation structure is between and in contact with the edges of the gate structures **along the second direction**: ***as one moves in the second direction*** (*e.g.*, from top to bottom in the top view composite figure, or from left to right in the Y-Y cross-sectional view) starting from the edge of the first gate structure, one reaches first the gate edge isolation structure and then the edge of the second gate structure.

83. Xie also renders obvious that the gate edge isolation structure is **over the isolation material** (*e.g.*, Xie's insulating material 108 or isolation structure 104, both highlighted in purple), as shown in the composite figure above. Indeed, Xie's description of forming the gate separation structure confirms this to be the case: Xie describes depositing material for the gate separation structure into the opening 112, where the insulating material 108 and isolation structure 104 are

disposed at the bottom of the opening. *See* SAMSUNG-1004 (Xie), [0031]-[0032], [0039]-[0041], FIGS. 2C-2I.

**[26g] a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.**

84. Xie renders obvious [26g]. For instance, Xie renders obvious a **dielectric material**, *e.g.*, in view of Xie's insulating material 130, highlighted in orange in FIG. 2I, reproduced again below. *See* SAMSUNG-1004 (Xie), [0036] ("a layer of ***insulating material 130***, *e.g.*, silicon dioxide, … blanket-deposited above the epi semiconductor material and … planarize[d]"), FIG. 2I. An insulating material such as silicon dioxide is a dielectric material.




Xie composite figure – Replacement gate structure

85. I have outlined the sidewalls of the gate structures in pink in the X-X cross-sectional figure above. These sidewalls extend into the page of the top-view figure, and the dielectric material is disposed next to these sidewalls, as can be seen from the X-X cross-section. That is, **the dielectric material** (orange) **is laterally adjacent to each gate structure** at least at these pink-outlined sidewalls. For instance, the dielectric material contacts the spacers 122 (*see* SAMSUNG-1004 (Xie), [0035]) that are disposed on those sidewalls. The dielectric material is thus **laterally adjacent** to the gate structures, *e.g.*, in that the dielectric material is near

(*e.g.*, next to) the sidewalls of the gate structures (*e.g.*, separated only by the spacers).

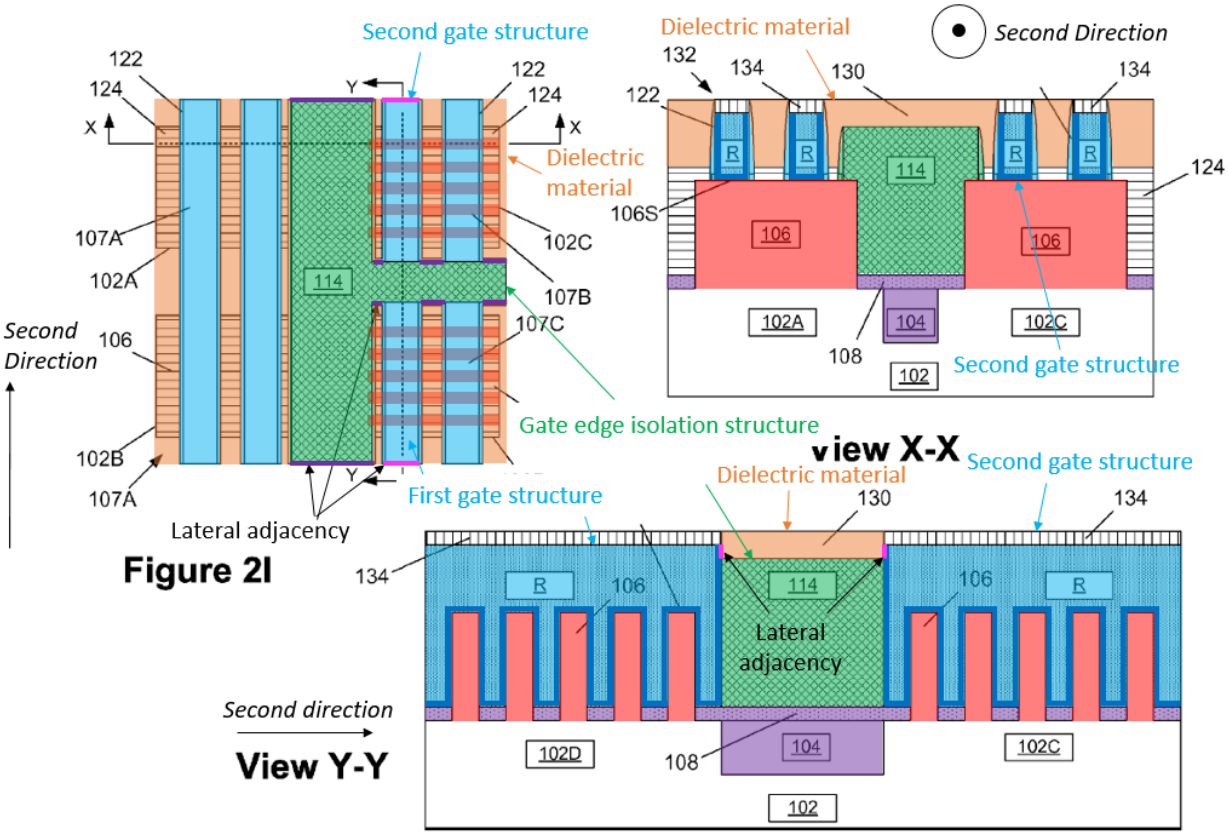
86. The dielectric material is laterally adjacent to the gate structures **along the first direction** at these pink-outlined sidewalls: viewing the structure starting from either of the gate structures and ***moving along the first direction*** (from left to right in the top view and X-X cross-sectional view), one reaches the dielectric material, passing through the spacers.

87. I have outlined the sidewalls of the gate edge isolation structure in purple in the X-X cross-section above. These sidewalls extend into the page of the top-view figure. As with the sidewalls of the gate structures, and as can be seen from the X-X cross-section, **the dielectric material** (orange) **is laterally adjacent to the gate edge isolation structure** at least at these purple-outlined sidewalls. For instance, the dielectric material contacts the spacers 122 (*see* SAMSUNG-1004 (Xie), [0035]) that are disposed on those sidewalls. The dielectric material is thus **laterally adjacent** to the gate edge isolation structure, *e.g.*, in that the dielectric material is near (*e.g.*, next to, although not necessarily in contact with) the sidewalls of the gate edge isolation structure (*e.g.*, separated only by the spacers).

88. The dielectric material is laterally adjacent to the gate edge isolation structure **along the first direction**: viewing the structure starting from the gate edge isolation structure and ***moving along the first direction*** (from left to right in

the top and X-X cross-sectional views), one reaches the dielectric material, passing through the spacer.

89. Moreover, alternatively or additionally, the dielectric material (*e.g.*, the layer of insulating material 130) also is laterally adjacent to the gate structures at the pink-outlined ends of the gate structures in the alternative annotated version of Xie's FIG. 2I that I have reproduced below. For instance, as shown in the Y-Y view, viewing the structure starting from, *e.g.*, the first gate structure and moving along the second direction (left to right), the dielectric material is reached. The dielectric material is also reached when moving along the second direction at the ends of the gate structures, as shown in the top view. To the extent this spatial relationship is considered to be laterally adjacent **along the first direction**, the dielectric material of the combination is laterally adjacent to the first and second gate structures along the first direction.




Xie composite figure – Replacement gate structure (alternative)

90. Similarly, the dielectric material is laterally adjacent to the gate edge isolation structure at the purple-outlined edges of the gate edge isolation structure in the alternative figure above. For instance, viewing the structure starting from the gate edge isolation structure and moving along the second direction, one reaches the dielectric material. To the extent this spatial relationship is considered to be laterally adjacent **along the first direction**, the dielectric material of the combination is laterally adjacent to the gate edge isolation structure along the first direction.

91. Xie also renders obvious that **the dielectric material is discrete from the gate edge isolation structure**, *e.g.*, the layer of insulating material 130 is discrete from the gate separation structure 114. For instance, the two structures are discrete at least in that ***they are formed in two distinct processing steps***: the dielectric material is deposited after the gate separation structure 114 has already been formed. *See* SAMSUNG-1004 (Xie), [0032] (describing the formation of the gate separation structure, with reference to FIG. 2D), [0036] (describing the deposition of the insulating material onto a structure already including the gate separation structure, with reference to FIG. 2G). I also note that Xie identifies the dielectric material 130 and the gate separation structure 114 as distinct elements. *See id.*, [0032], [0036].

**(2) Claim 27**

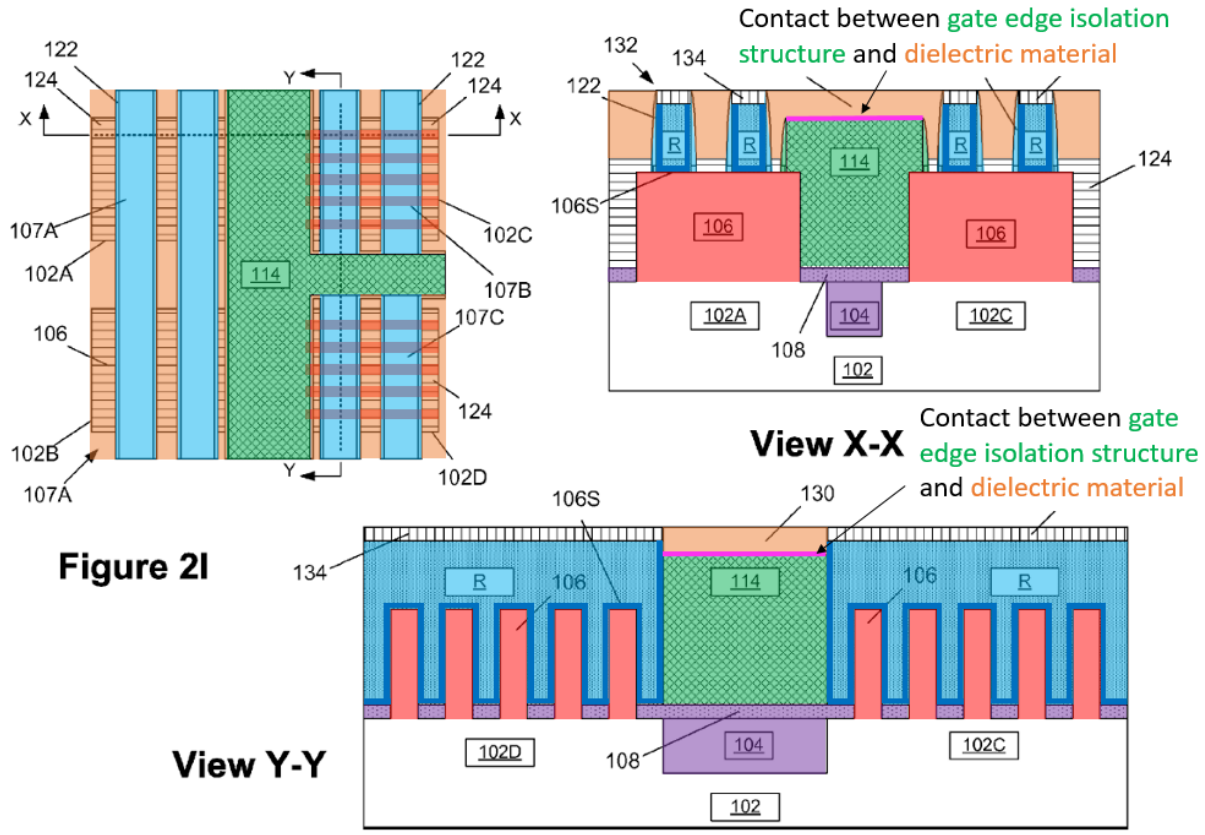
**[27] The integrated circuit structure of claim 26, wherein the gate edge isolation structure comprises silicon and nitrogen.**

92. Xie renders obvious that the gate edge isolation structure (*e.g.*, Xie's gate separation structure) comprises silicon nitride, *i.e.*, **silicon and nitrogen**. *See* SAMSUNG-1004 (Xie), [0032] (The gate separation structure 114 may be comprised of a variety of materials, *e.g.*, … ***silicon nitride***").

### (3) Claim 28

**[28] The integrated circuit structure of claim 26, wherein the dielectric material is in contact with the gate edge isolation structure.**

93. Xie renders obvious [28]. For instance, Xie renders obvious that **the dielectric material** (*e.g.*, Xie's insulating material 130, highlighted in orange in the composite figure below) is **in contact with the gate edge isolation structure** (*e.g.*, Xie's gate separation structure 114, green). This contact is at least on the top surface of the gate edge isolation structure, which I have outlined in pink in the X-X and Y-Y cross sectional views below.




Xie composite figure – Replacement gate structure

94. That there is contact at this interface between the gate edge isolation structure and the dielectric material is made apparent by Xie's description of its fabrication process. Specifically, Xie describes that after formation of the gate separation structure 114 (*see* SAMSUNG-1004 (Xie), [0032]), its top surface remains exposed until the "layer of insulating material 130 … [is] blanket-deposited" onto that surface. *Id.*, [0036].

**(4) Claim 29**

**[29] The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.**[6]

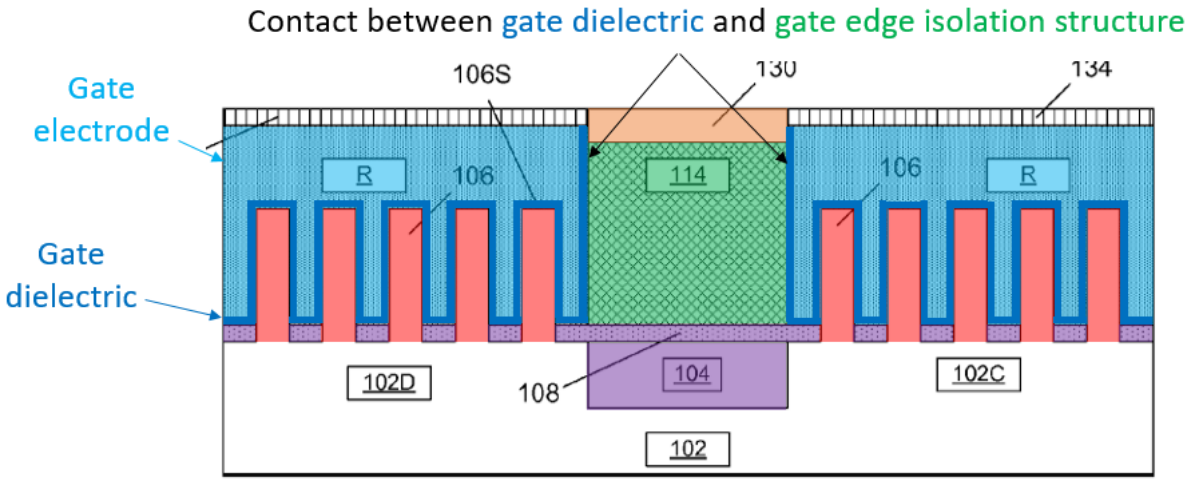
95. Xie renders obvious [29]. For instance, Xie renders obvious that when the gate structures are fabricated by a replacement gate process (*see* SAMSUNG-1004 (Xie), [0030]), **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures**. As I have discussed previously, in a replacement gate fabrication process, the gate dielectric layer is deposited into the "gate cavities 132." SAMSUNG-1004 (Xie), [0038], FIG. 2I.

---

[6] As best understood, I interpret the "gate dielectric layer of the first gate structure" and the "gate dielectric layer of the second gate structure" as being equivalent to the "first gate dielectric layer" and "second gate dielectric layer," respectively, of claim 26.

This results in the gate dielectric layer being coated onto exposed surfaces in the gate cavities, including onto the exposed sidewalls of the gate separation structure. *See* SAMSUNG-1025 (Ching), 4:39-5:56; SAMSUNG-1005 (Tseng), 8:62-9:4; SAMSUNG-1015 (Shieh), [0045]-[0047]; SAMSUNG-1012 (Bohr), 11:4-14; SAMSUNG-1014 (Kuo), 7:8-42. Thus, **the gate edge isolation structure** (*e.g.*, Xie's gate separation structure) **is in contact with the gate dielectric layer** of each gate structure, *e.g.*, at least because the gate dielectric layer of each of the first and second gate structures coats the respective sidewalls of the gate separation structure.

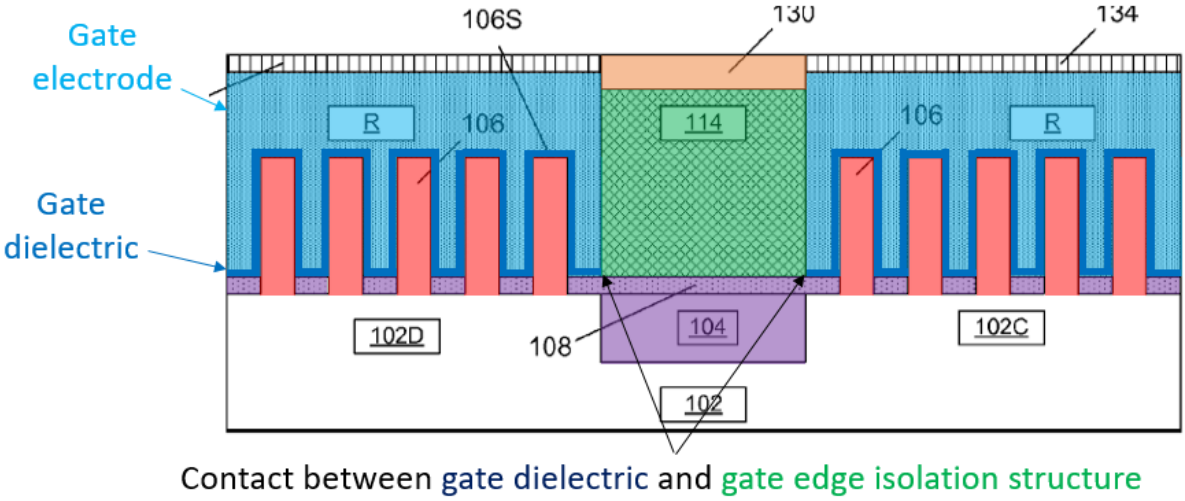
96. An example of a replacement gate structure is depicted in the composite figure below. As illustrated, the gate edge isolation structure (green) is in contact with the gate dielectric layer (dark blue) of the first and second gate structures on the sidewalls of the gate edge isolation structure.




Xie composite figure – Replacement gate structure

97. Alternatively, when Xie's gate structures are fabricated by a gate-first process (*see* SAMSUNG-1004 (Xie), [0030]), **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures**. As also discussed previously, in a gate-first fabrication process, a gate dielectric layer and gate electrode are deposited and then etched to form openings that "define the ends 110X" of the gate structures. SAMSUNG-1004 (Xie), [0031]; *see* [0040]; SAMSUNG-1005 (Tseng), 4:59-5:55. The etch exposes both the gate dielectric layer and the gate electrode at these end surfaces. *See* SAMSUNG-1005 (Tseng), FIG. 5A; SAMSUNG-1016 (Cheng), FIG. 13, 19:41-20:16, 22:7-8; SAMSUNG-1017 (Basker), FIG. 2, 4:7-16. The "gate separation structure 114" is then "formed in the opening," and thus the gate separation structure contacts both the gate dielectric layer and the gate electrode that are exposed at the end surfaces of the gate structures. SAMSUNG-1004 (Xie), [0032]; *see* [0040]; *see* SAMSUNG-1005 (Tseng), 5:47-55.

98. An example of a gate-first gate structure is depicted in the composite figure below. As illustrated, the gate edge isolation structure (green) is in contact with both the gate dielectric layer (dark blue) and the gate electrode (light blue) of the first and second gate structures on the sidewalls of the gate edge isolation structure.




Xie composite figure – Gate-first gate structure

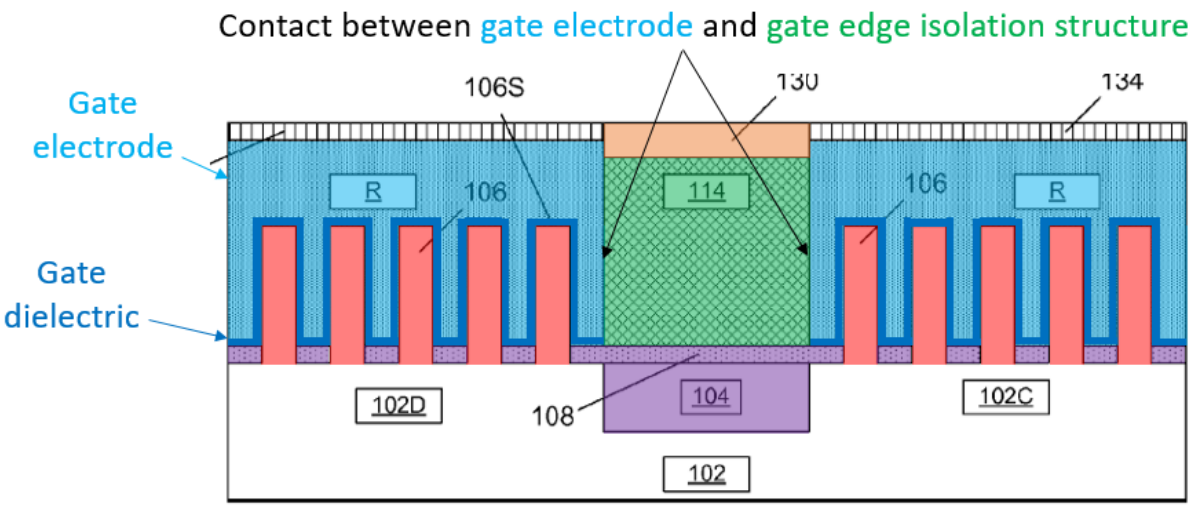
**(5) Claim 30**

**[30] The integrated circuit structure of claim 29, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.**

99. Xie renders obvious [30]. First, as I have discussed previously, it is my opinion that POSITA would have understood or found obvious that each of Xie's gate structures includes a gate dielectric layer (*e.g.*, a high-k gate dielectric layer) and a gate electrode (*e.g.*, **a metal gate electrode**). *See* SAMSUNG-1004 (Xie), [0038]; SAMSUNG-1005 (Tseng), 5:5-46; SAMSUNG-1025 (Ching), 4:39-5:3; SAMSUNG-1006 (Anderson), [0029]; SAMSUNG-1011 (Gan), 3:59-4:10; SAMSUNG-1014 (Kuo), 7:8-22; SAMSUNG-1015 (Shieh), [0047]. For instance, a POSITA would have understood or found obvious for Xie's "bulk conductive

metal layer" to be a gate electrode, *e.g.*, a **metal gate electrode layer**. SAMSUNG-1004 (Xie), [0038].

100. Second, Xie renders obvious that when the gate structures are fabricated by a gate-first process (*see* SAMSUNG-1004 (Xie), [0030]), **the gate edge isolation structure is in contact with the metal gate electrode layers of the first and second gate structures**, as discussed in [29]. *See* SAMSUNG-1004 (Xie), [0031]-[0032], [0040]; SAMSUNG-1005 (Tseng), 4:59-5:55; SAMSUNG-1016 (Cheng), FIG. 13, 19:41-20:16, 22:7-8; SAMSUNG-1017 (Basker), FIG. 2, 4:7-16. For instance, as illustrated below, when a gate-first process is used (described above for [29]), the gate edge isolation structure (green) is in contact with both the gate dielectric layer (dark blue) and the gate electrode (light blue) of the first and second gate structures on the sidewalls of the gate edge isolation structure.




Xie composite figure – Gate-first gate structure

**(6) Claim 31**

**[31] The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.**

101. Xie renders obvious [31]. For instance, as I discussed previously, it is my opinion that a POSITA would have understood or found obvious that Xie's gate structures each includes a gate dielectric layer (*e.g.*, **a high-k gate dielectric layer**) and a gate electrode (*e.g.*, a metal gate electrode). *See* SAMSUNG-1004 (Xie), [0038]; SAMSUNG-1005 (Tseng), 5:5-46; SAMSUNG-1025 (Ching), 4:39-5:3; SAMSUNG-1006 (Anderson), [0029]; SAMSUNG-1011 (Gan), 3:59-4:10; SAMSUNG-1014 (Kuo), 7:8-22; SAMSUNG-1015 (Shieh), [0047]. Specifically, a POSITA would have understood or found obvious for Xie's "high-k … gate

insulation layer" to be a gate dielectric layer that includes **a high-k dielectric material**. SAMSUNG-1004 (Xie), [0038].

### B. [GROUND 2] – CLAIMS 26-31 ARE OBVIOUS OVER XIE AND TSENG

102. Ground 2 is substantively identical to Ground 1 in all but the following respects. Ground 1 demonstrated that the Element [26d] and [26e] features that each gate structure includes a respective gate dielectric layer and gate electrode are obvious in view of Xie. In Ground 2, I rely on the even more explicit disclosure of Tseng to reach these features, as well as to reach dependent claims 29-31. I note that my reliance on Tseng in Ground 2 does not affect the mapping of Xie to other claim elements, and so for brevity, I have addressed only the pertinent portions of Elements [26d]-[26e] and claims 29-31 in Ground 2. The unaddressed claim 26 elements, and dependent claims 27-28, are obvious over the Xie-Tseng combination at least as I discussed above for Ground 1.

#### 1. Tseng describes FinFET gate structures having a gate dielectric layer and a gate electrode

103. Tseng, in the field of FinFET devices, describes a FinFET having a "gate stack 210" including a "gate electrode layer 214 and [a] gate dielectric layer 212." SAMSUNG-1005 (Tseng), 5:5-10; *see* 3:4-12, FIGS. 2, 5A. The gate dielectric layer can be a "high dielectric constant (high-k) dielectric," and the gate electrode can include a "N-work function metal" or a "P-work function metal."

SAMSUNG-1005 (Tseng), 5:12-46. Tseng's gate stack can be "fabricated using a gate-first process" or "using a gate-last process performed by first forming a dummy gate stack." *Id.*, 8:59-62.

**2. The Xie-Tseng combination**

104. In the Xie-Tseng combination, Xie's gate structures (*e.g.*, replacement gate structures or gate-first gate structures; *see* SAMSUNG-1004 (Xie), [0030]) include gate dielectric layers and gate electrodes based on the teachings of Tseng. *See* SAMSUNG-1005 (Tseng), 5:5-46. For instance, in the combination, Xie's "high-k … gate insulation layer" is implemented as a high-k gate dielectric layer, and Xie's "bulk conductive metal layer" is implemented as a metal gate electrode layer, based on the teachings of Tseng. SAMSUNG-1004 (Xie), [0038]; *see* Tseng, 5:5-46, 8:67-9:4, FIG. 5A.

105. The configurations of these Xie-Tseng gate structures are consistent with the replacement gate structure and gate-first gate structure illustrated in the composite figures I presented above.

106. A POSITA would have been motivated to pursue this implementation, and would have expected success in doing so, for at least similar reasons as those I discussed for Ground 1. Moreover, a POSITA would have expected success specifically in the Xie-Tseng combination given that both Xie and Tseng relate to FinFET fabrication processes that can be performed using gate-first or gate-last

processes. *See* SAMSUNG-1004 (Xie), [0030]; SAMSUNG-1005 (Tseng), 8:59-62.

### 3. Analysis

#### (1) Claim 26

**[26d] a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;**

**[26e] a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;**

107. The Xie-Tseng combination renders obvious first and second gate structures having the recited features, *e.g.*, in view of Xie's final gate structures (*e.g.*, replacement gate structures or gate-first gate structures). *See* [26d]-[26e] of Ground 1.

108. In the Xie-Tseng combination, the first and second gate structures (*e.g.*, replacement gate structures or gate-first gate structures) include respective **gate dielectric layers** and respective **gate electrodes**, *e.g.*, based on Tseng's description of gate structures with gate dielectric layers and gate electrodes. *See* SAMSUNG-1005 (Tseng), 5:5-46, 3:4-12, FIGS. 2, 5A.

### (2) Claim 29

**[29] The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.**

109. When the Xie-Tseng gate structures are fabricated by a replacement gate process (*see* SAMSUNG-1004 (Xie), [0030]), **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures**. Alternatively, when the Xie-Tseng gate structures are fabricated by a gate-first process (*see* SAMSUNG-1004 (Xie), [0030]), **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures**. *See* [29] of Ground 1.

### (3) Claim 30

**[30] The integrated circuit structure of claim 29, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.**

110. The gate electrodes of the Xie-Tseng gate structures include **metal gate electrode layers**. For instance, in the combination, Xie's "bulk conductive metal layer" is implemented a **metal gate electrode layer** based on the teachings of Tseng. SAMSUNG-1004 (Xie), [0038]; *see* SAMSUNG-1005 (Tseng), 5:5-46.

111. When the Xie-Tseng gate structures are fabricated by a gate-first process (*see* SAMSUNG-1004 (Xie), [0030]), **the gate edge isolation structure is**

**in contact with the metal gate electrode layers of the first and second gate structures**. *See* [30] of Ground 1.

#### (4) Claim 31

**[31] The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.**

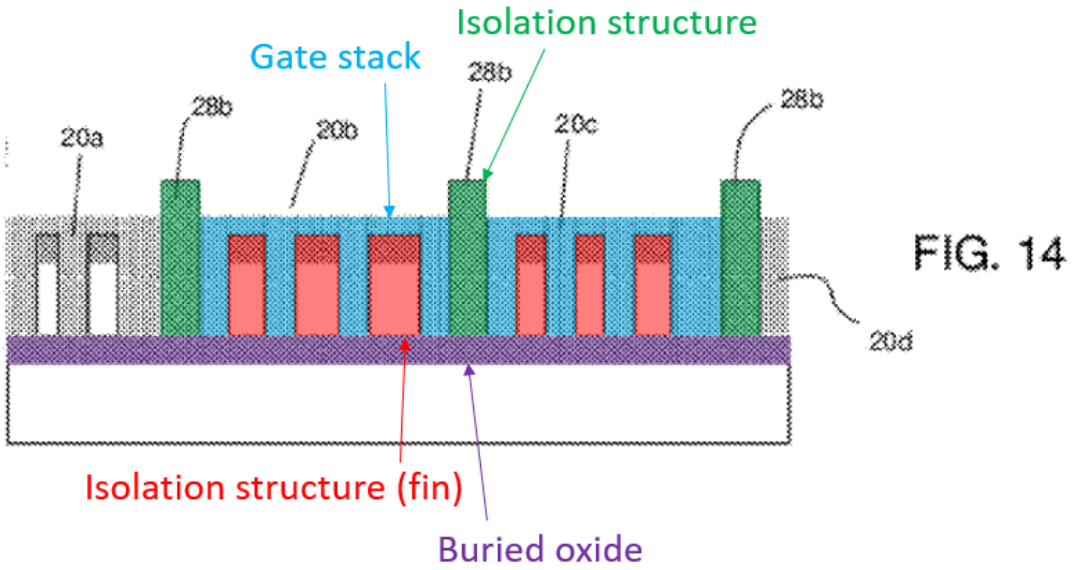
112. The gate dielectric layers of the Xie-Tseng gate structures include **a high-k dielectric material**. For instance, in the combination, Xie's "high-k … gate insulation layer" is implemented as a **gate dielectric layer** that includes **a high-k dielectric material** based on the teachings of Tseng. SAMSUNG-1004 (Xie), [0038]; *see* SAMSUNG-1005 (Tseng), 5:5-46.

## C. [GROUND 3A] – CLAIMS 26-29 AND 31-32 ARE OBVIOUS OVER ANDERSON AND LIN

### 1. Anderson describes gate-to-gate isolation structures for FinFET devices

113. Anderson, in the field of FinFET devices, describes "devices having gate-to-gate isolation structures," *e.g.*, for use with FinFETs. SAMSUNG-1006 (Anderson), [0019]. For instance, these devices have "selectively raised isolation regions at desired gate isolation points to provide isolation structures between adjacent gates (transistors)." *Id.* An example device is illustrated in cross-sectional and top views in FIGS. 14 and 15, respectively, reproduced below. *See id.*, [0040]; *see also* [0050]-[0051] and FIGS. 23-26. I note that FIGS. 14-15,

FIGS. 23-24, and FIGS. 25-26 belong to different embodiments of Anderson's disclosure. These embodiments all contain relevant disclosure, except where I note otherwise.




Excerpt from Anderson, FIG. 14

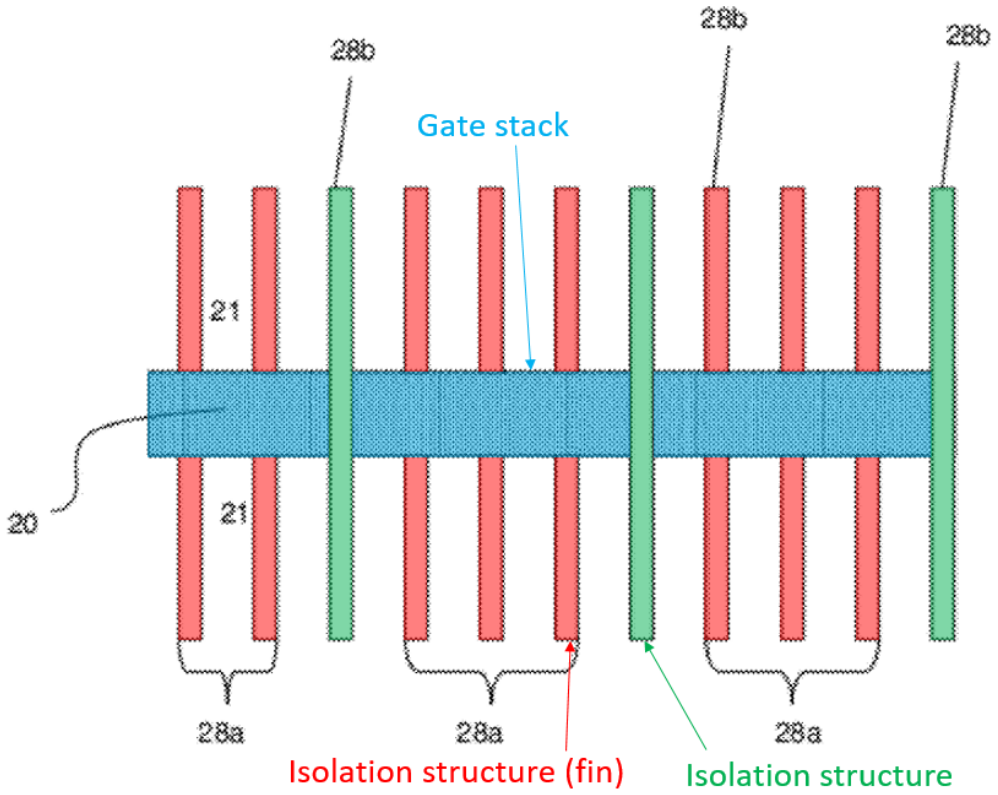



FIG. 15

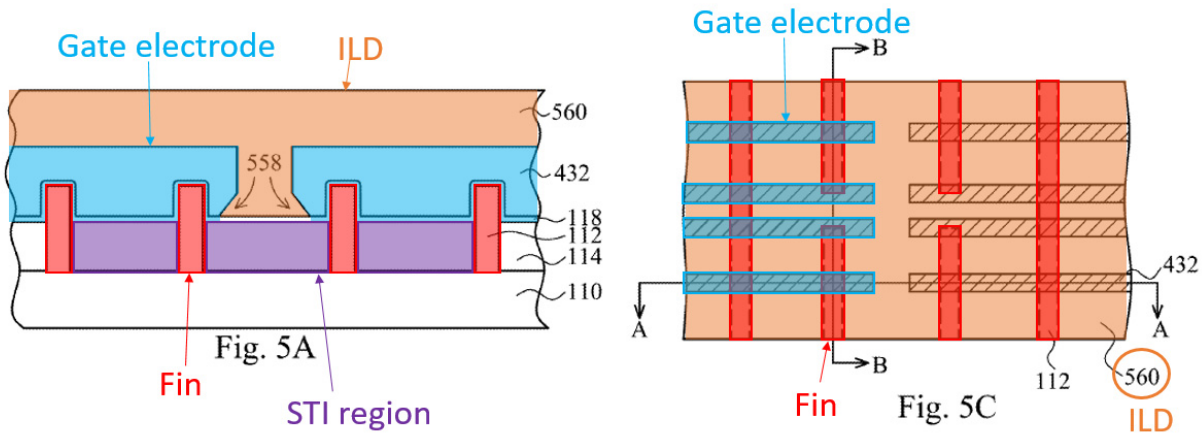
Excerpt from Anderson, FIG. 15

114. Anderson's device is formed on a "silicon on insulator (SOI) wafer" that includes "a buried oxide 10b" (highlighted in purple) disposed on "a lower Si layer 10a." SAMSUNG-1006 (Anderson), [0032]; *see* FIG. 9. The device also includes "dual height isolation structures 28a and 28b" (highlighted in red and green, respectively), both of which are formed by etching the substrate to form trenches and fins. *Id.*, [0036]-[0037], FIG. 11; *see* [0047]-[0048], FIG. 20. "[T]he isolation structure 28b is taller than the surrounding isolation structures 28a." *Id.*, [0037]; *see* [0046]. A gate stack 20 (highlighted in blue) including "a gate

dielectric and a gate electrode material," is "formed over the isolation structures 28a and 28b" and "partially etched away to expose the isolation structure 28b," while still "cover[ing] or bury[ing] the isolation structures 28a." *Id.*, [0038]-[0039], FIGS. 13-14; *see* [0047]-[0048], FIGS. 22-23. The taller isolation structures 28b thus "provide a physical and electrical separation between the gates 20a-20d." *Id.*, [0039]; *see* [0048], [0051], FIGS. 23-26.

**2. Lin describes FinFET gate structures**

115. Lin, also in the field of FinFET devices, describes a "fin field-effect transistor (finFET)." SAMSUNG-1007 (Lin), Abstract. As shown in FIGS. 5A and 5C, *infra*, Lin's device includes fins 112 (highlighted in red), with a "dielectric layer 114" (highlighted in purple) that "acts as a shallow trench isolation (STI) around the fins 112." *Id.*, 2:55-58. Gate electrodes 432 (highlighted in blue) are disposed over the fins and separated at by "notches 558 in the ends of the gate electrodes 432." *Id.*, 4:65-5:9. An "inter-layer dielectric (ILD) 560," highlighted in orange, is "formed over the gate electrodes 432 and in the notches 558. *Id.*, 5:15-17. The ILD 560 buries the gate electrodes, contacting their top surfaces and filling the spaces next to their sidewalls and ends.



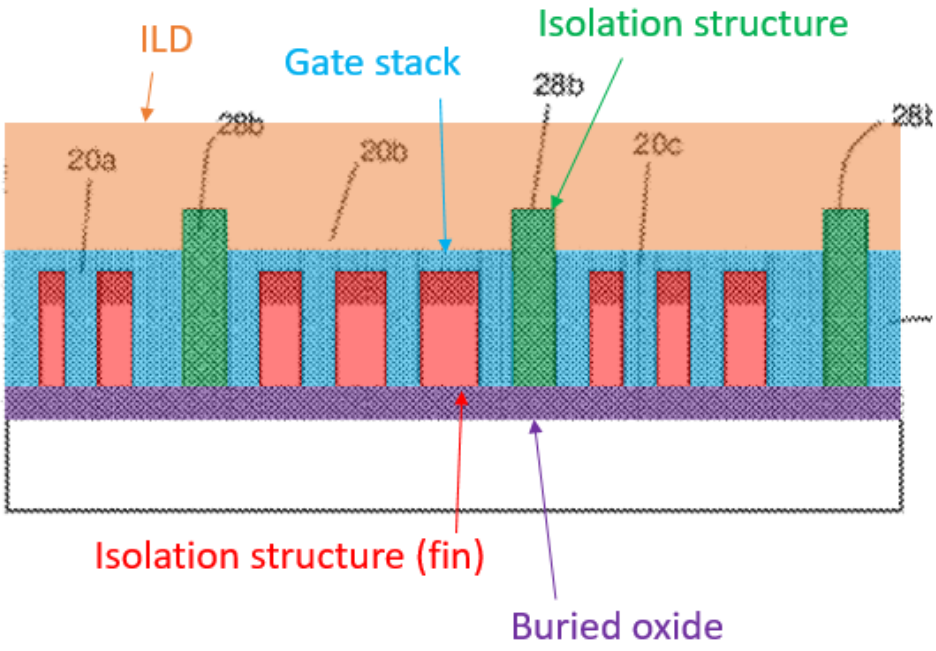

Excerpt from Lin, Figs. 5A and 5C (annotated)

### 3. The Anderson-Lin combination

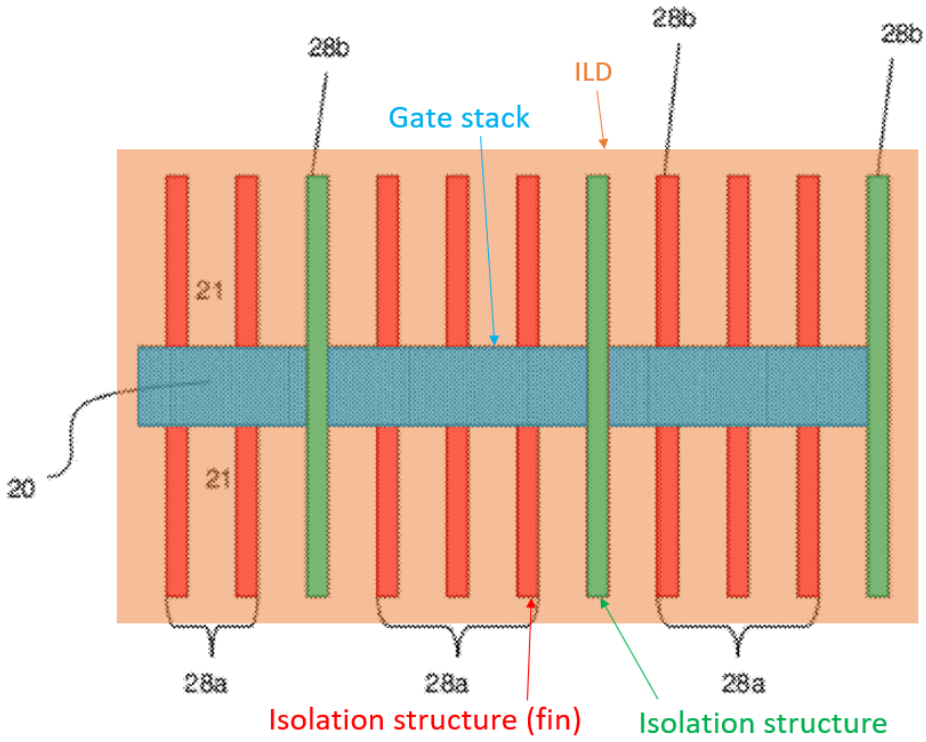
116. A FinFET based on the Anderson-Lin combination is illustrated in the composite figures *infra*.[7] Based on the teachings of Anderson, this FinFET is formed on an SOI wafer including a buried oxide (highlighted in purple), and includes dual-height isolation structures: fins 28a (highlighted in red) and taller isolation structures 28b (highlighted in green). SAMSUNG-1006 (Anderson), [0036]-[0039]. Gates 20a-20d cover the fins 28a, and the taller isolation structures 28b are exposed above the top surface of the gates. *See id.*, [0007], [0038]-[0039].

[7] Although Anderson's relevant disclosure spans multiple embodiments, as I noted previously, the Anderson-Lin cross-sectional and top view composite figures I present here are based on Anderson's FIGS. 14 and 15, respectively, unless otherwise noted.

The isolation structures 28b "provide a physical and electrical separation between the gates 20a-20d." SAMSUNG-1006 (Anderson), [0039].




Anderson-Lin cross-sectional composite figure



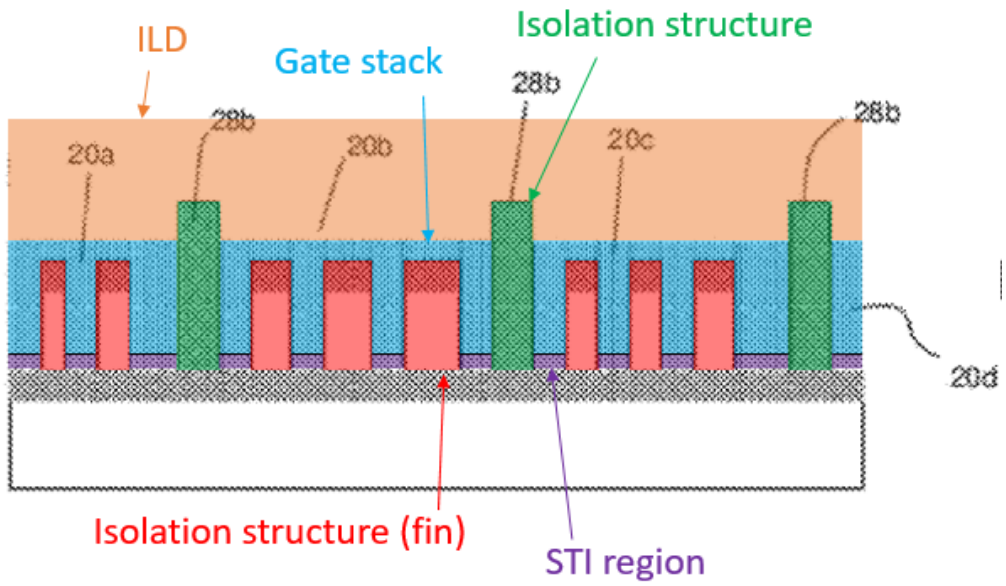

Anderson-Lin top-view composite figure

117. Based on the teachings of Lin, an ILD (highlighted in orange) is "formed over" the gates. SAMSUNG-1007 (Lin), 5:15-17. The ILD buries the taller isolation structures 28b, contacting their top surfaces and filling the spaces next to the sidewalls and ends of the isolation structures 28b that protrude above the top surfaces of the gates and extend beyond the sidewalls of the gates. *See*

SAMSUNG-1007 (Lin), 5:15-17. The ILD also fills the spaces next to the short end walls of the gate electrodes.[8]

118. Optionally, as shown in the composite figure *infra*, a "dielectric layer" (highlighted in purple) is disposed on the substrate (*e.g.*, on Anderson's buried oxide layer), thus "act[ing] as a shallow trench isolation (STI) around the fins" 28a. SAMSUNG-1007 (Lin), 2:55-58. For instance, the dielectric layer "may be formed by chemical vapor deposition (CVD) techniques using tetra-ethyl-ortho-silicate (TEOS) and oxygen as a precursor." *Id.*, 2:55-58.

[8] The top view composite figure depicts the fins, gates, and isolation structures 28b for illustrative purposes only; in the top view of the combination, the ILD covers all of these features.




Anderson-Lin composite figure

### 4. Reasons to combine Anderson and Lin

*Incorporation of an interlayer dielectric*

119. It is my opinion that a POSITA would have been motivated to incorporate an interlayer dielectric (ILD) into the Anderson-Lin integrated circuit structure for at least the following reasons.

120. One reason why a POSITA would have been motivated to incorporate an ILD into the combination is to provide electrical isolation between the transistor-level structures (*e.g.*, the FinFETs) and overlying interconnect structures. *See* SAMSUNG-1008 (Kawa), [0068] ("An insulating fill 515 provides an interlayer insulator between the patterned gate conductor layer including the gate traces 505 and 506, and overlying patterned conductor layers, including the first patterned conductor layer M1"); SAMSUNG-1017 (Basker), 6:42-44 ("The ILD

layer 20 may fill the gaps between gate structures and other existing devices within the semiconductor structure 300"); SAMSUNG-1039 (Pethe), 9:5-8 ("The inter-layer dielectric (ILD) 330 may be composed of a material suitable to electrically isolate metal features ultimately formed therein while maintaining a robust structure between front end and back end processing"). For instance, the presence of an ILD would enable the structures envisioned by Anderson to be achieved: "contacts can be connected to the source/drain and gate electrodes using conventional etching and metal deposition processes." SAMSUNG-1006 (Anderson), [0050].

121. Another reason why a POSITA would have been motivated to incorporate an ILD into the combination is because the use of ILDs above transistor-level structures was a standard element of integrated circuits. *See* SAMSUNG-1004 (Xie), [0036], FIG. 2I; SAMSUNG-1009 (Chang), [0051], FIGS. 15A-18D; SAMSUNG-1007 (Lin), 5:15-17, FIGS. 5A-5C; SAMSUNG-1008 (Kawa), [0068], FIG. 5; SAMSUNG-1017 (Basker), 6:42-44, FIG. 5; SAMSUNG-1039 (Pethe), 9:5-8, FIG. 3F.

122. Additionally, a POSITA would have been motivated to incorporate an ILD simply because this implementation is just the application of known techniques (*e.g.*, ILD in an integrated circuit device) to a known structure (*e.g.*, a

FinFET integrated circuit structure) resulting in a predictable outcome (*e.g.*, a FinFET-based integrated circuit having an ILD disposed on the gate structures).

123. It is my opinion that a POSITA would have expected success in pursuing the incorporation of an ILD into the combination because the use of an ILD is compatible with "contacts" fabricated "using conventional etching and metal deposition processes" that Anderson suggests are to be implemented with its devices. SAMSUNG-1006 (Anderson), [0050]. I also believe that a POSITA would have expected success given that the use of ILDs in integrated circuits, such as FinFET-based devices, was well-known as of the Critical Date. *See* SAMSUNG-1004 (Xie), [0036], FIG. 2I; SAMSUNG-1009 (Chang), [0051], FIGS. 15A-18D; SAMSUNG-1007 (Lin), 5:15-17, FIGS. 5A-5C; SAMSUNG-1008 (Kawa), [0068], FIG. 5; SAMSUNG-1017 (Basker), 6:42-44, FIG. 5; SAMSUNG-1039 (Pethe), 9:5-8, FIG. 3F.

*Incorporation of shallow trench isolation*

124. It is my opinion that a POSITA would have been motivated to incorporate shallow trench isolation (STI) around the base of the fins of the Anderson-Lin integrated circuit structure for at least the following reasons.

125. One reason why a POSITA would have been motivated to incorporate STI around the fins is to isolate the fins from one another, which a POSITA would have recognized as a way to improve the electrical performance of the device, *e.g.*,

by reducing leakage current between neighboring fins. *See* SAMSUNG-1005 (Tseng), 4:25-27 ("the trenches 22 are filled with a dielectric material to form the isolation regions 204 to define and electrically isolate the various fins of the fin structure 202. In one example, the isolation regions 204 include shallow trench isolation (STI) regions"); SAMSUNG-1010 (Akarvardar), 1:43-45 ("In bulk FinFET technology, isolation regions may be used to electrically insulate adjacent devices or to electrically separate the fins of a given device from one another"); SAMSUNG-1031, 5:16-18 ("The isolation regions 440 utilize isolation technology, such as STI, to define and electrically isolate various regions of the FinFET device 400.").

126. Another reason why a POSITA would have been motivated to integrate STI regions specifically over Anderson's buried oxide layer is because a POSITA would have recognized that STI used in conjunction with silicon-on-insulator (SOI) substrates was a conventional approach providing benefits of both SOI and STI. *See* SAMSUNG-1034 (Chen-745), 2:24-36 ("The SOI substrate may allow a transistor to operate at a higher switching speed or with a lower power consumption when compared to a bulk semiconductor substrate. … [S]hallow trench isolation (STI) that extends from a surface of the SOI substrate … may provide an electrical isolation around a periphery of the transistor primarily in a horizontal (or lateral) direction"); SAMSUNG-1035 (Cheng), 1:22-32 ("FinFET

structures may be formed on a semiconductor-on-insulator (SOI) substrate, because of the low source/drain diffusion, low substrate capacitance, and ease of electrical isolation by shallow trench isolation structures"); SAMSUNG-1041 (Chen-619), 3:46-56 (describing a device having SOI and STI isolation that "maintains [] manufacturing simplicity, and benefits from FD-SOI's and FinFET's immunity to floating-body effects"), 6:6-46; SAMSUNG-1036, 3:55-59; SAMSUNG-1037, 3:16-18; SAMSUNG-1038, [0074].

127. Additionally, a POSITA would have been motivated to incorporate STI into the combination because this implementation is just the application of known techniques (*e.g.*, STI in an integrated circuit device) to a known structure (*e.g.*, a FinFET integrated circuit structure) resulting in a predictable outcome (*e.g.*, a FinFET-based integrated circuit having STI around the fins).

128. It is my opinion that a POSITA would have expected success given that the use of STI in integrated circuits, such as FinFET-based devices, was well-known as of the Critical Date. *See* SAMSUNG-1005 (Tseng), 4:25-27; SAMSUNG-1031 (Yin), 5:16-18; SAMSUNG-1032, 1:50-53. I also believe that a POSITA would have expected success because the processing used to form STI regions (*e.g.*, CVD; *see* SAMSUNG-1007 (Lin), 2:55-58) is compatible with SOI structures such as those described by Anderson. *See* SAMSUNG-1005, 4:25-27; SAMSUNG-1010, 1:43-45; SAMSUNG-1031, 5:16-18.

### 5. Analysis

#### (1) Claim 26

**[26pre] An integrated circuit structure, comprising:**

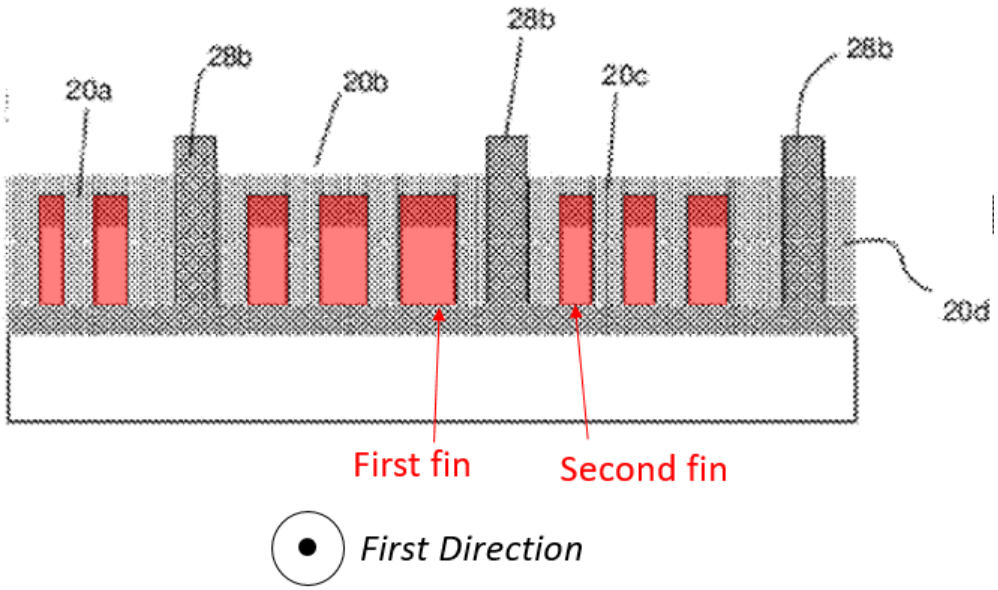
129. To the extent the preamble is deemed to be limiting, the Anderson-Lin combination renders it obvious. *See* SAMSUNG-1006 (Anderson), [0019] ("The present invention also allows for flexible circuit design, and can be used for ***FinFETs as well as other devices***"), [0051] ("a split gate finFET can be formed using the processes of the present invention"), [0001] ("The invention relates to semiconductor structures … and, more particularly, to devices having gate-to-gate isolation structures"), [0007], claim 20.

**[26a] a first fin comprising silicon, the first fin having a longest dimension along a first direction;**

**[26b] a second fin comprising silicon, the second fin having a longest dimension along the first direction;**

130. The Anderson-Lin combination renders obvious [26a] and [26b]. For instance, the Anderson-Lin combination structure includes **first and second fins**, *e.g.*, based on Anderson's ***isolation structures 28a***, highlighted in red in the figures *infra*. *See* SAMSUNG-1006 (Anderson), [0036] ("A RIE process is then performed to form trenches 26 and ***fins 27a*** and 27b (also isolation structures)," as shown in FIG. 11, and "the remaining portion of the pad film 22 is removed from the fins 27a, leaving ***isolation structures 28a*** and 28b."), FIGS. 14-15. *See also* Anderson's "isolation structures 28a′" (*e.g.*, **fins**) in FIGS. 22-24 (*id.*, [0044]-

[0046]) and isolation structures 38a (*e.g.*, **fins**) in FIGS. 25-26 (*see id.*, [0051]); *see* [0005] ("forming a plurality of fins comprising the raised portions and ***a second plurality of fins*** comprising the hard mask … resulting in a dual height fin array"), [0006] ("creating an array of fins comprising: first fins …; and ***second fins*** … resulting in a dual height array of fins, wherein the first fins are higher than the second fins"), [0007] ("a structure comprises ***an array of semiconductor fins*** comprising a plurality of ***first … height fin structures***"), [0007] ("the double gate finFET comprises ***a short fin structure***").




Anderson-Lin cross-sectional composite figure

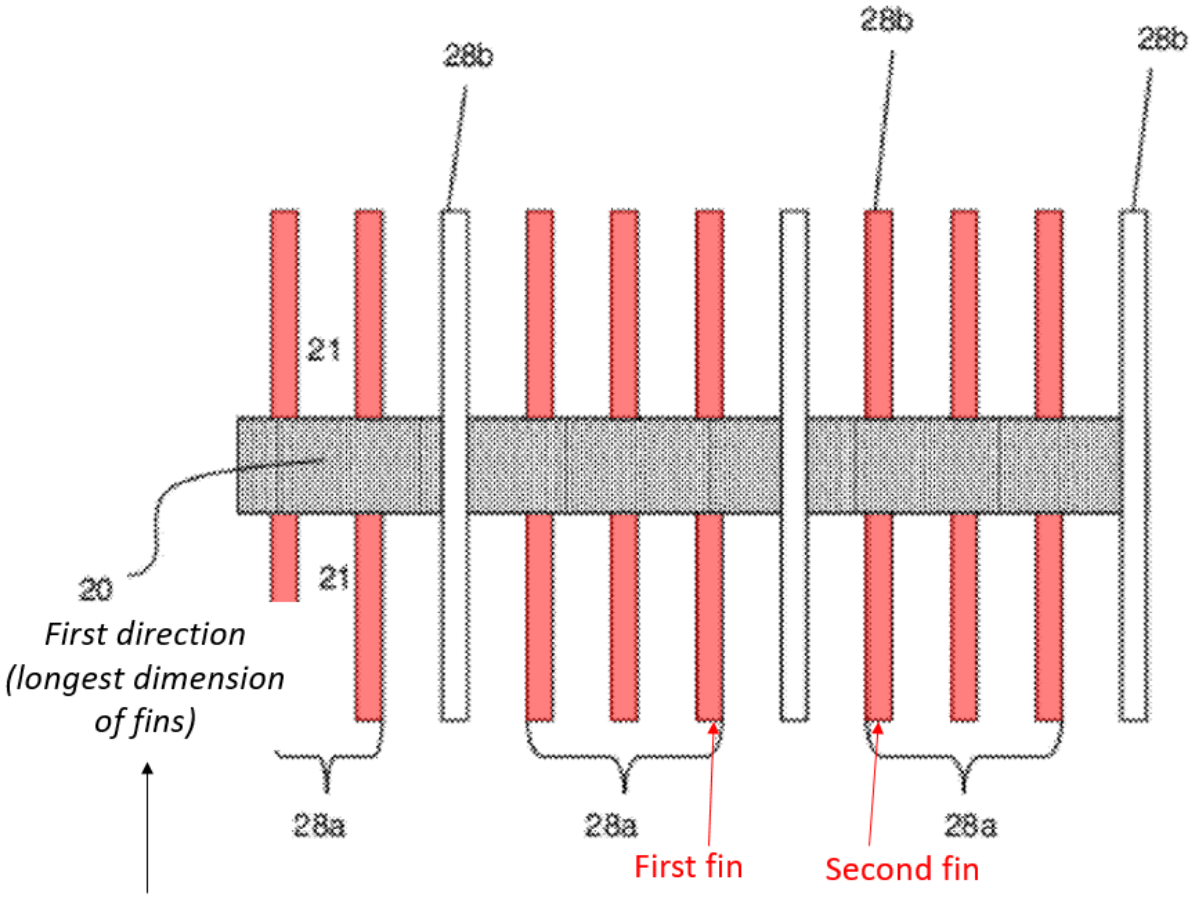


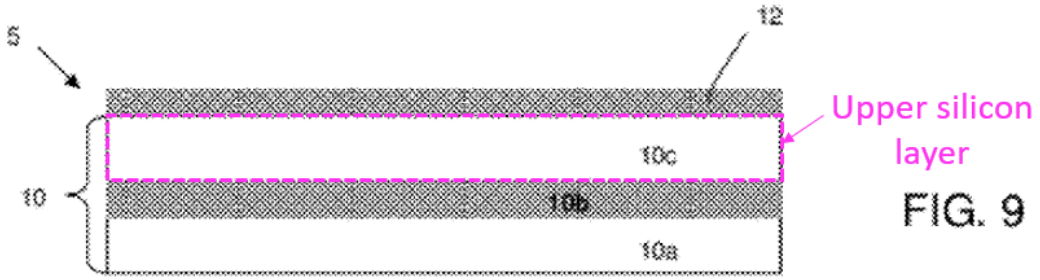

FIG. 15

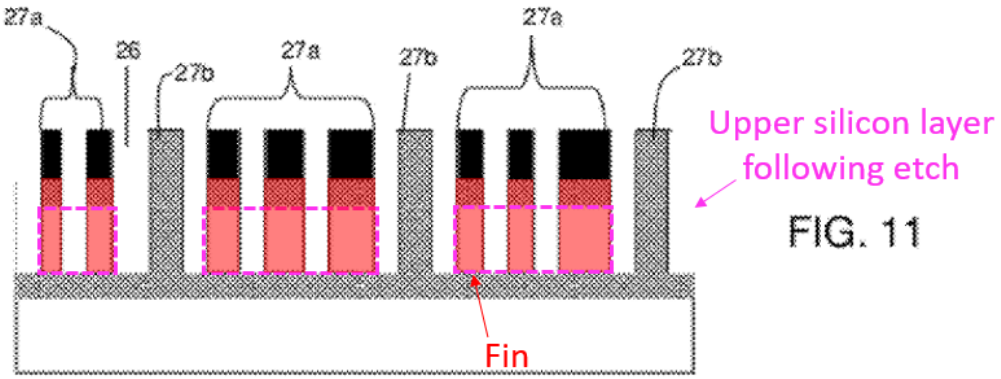
Anderson-Lin top-view composite figure

131. In the Anderson-Lin combination structure, each fin has **a longest dimension along a first direction**, which I have marked in the figures. This longest dimension is **along the first direction**: the longest dimension of the fins is traversed ***as one moves along the fins in the first direction***, *e.g.*, from top to

bottom in the top view composite figure, and into the page in the cross-sectional composite figure.

132. Also in the Anderson-Lin combination structure, **the fins comprise silicon**. This is made apparent by Anderson's description of the process of fabricating the isolation structures 28a. For instance, Anderson's isolation structures 28a are formed on a "wafer 10," which can be "a BULK SI wafer or a silicon on insulator (SOI) wafer" that includes "a buried oxide 10b sandwiched between a lower Si layer 10a and ***upper silicon layer 10c***." SAMSUNG-1006 (Anderson), [0032]-[0033], FIG. 9, *infra* (outlining the upper silicon layer in pink); *see also* [0041]-[0042], FIG. 16. Following additional process steps, trenches are etched through the upper silicon layer to the buried oxide 10b, such that the upper silicon layer is no longer continuous. *See* SAMSUNG-1006 (Anderson), [0036], FIG. 11, *infra*. The portions of the upper silicon layer that remain following the etch, and following other steps including removal of a pad film 22 (the black elements in FIG. 11) are the isolation structures 28a (highlighted in red in FIG. 11, below). *See id.*, [0037], FIG. 12; *see also* [0046], FIG. 21; claims 3, 15. That is, because Anderson's isolation structures 28a (fins) include unetched portions of the upper silicon layer, they **include silicon**.



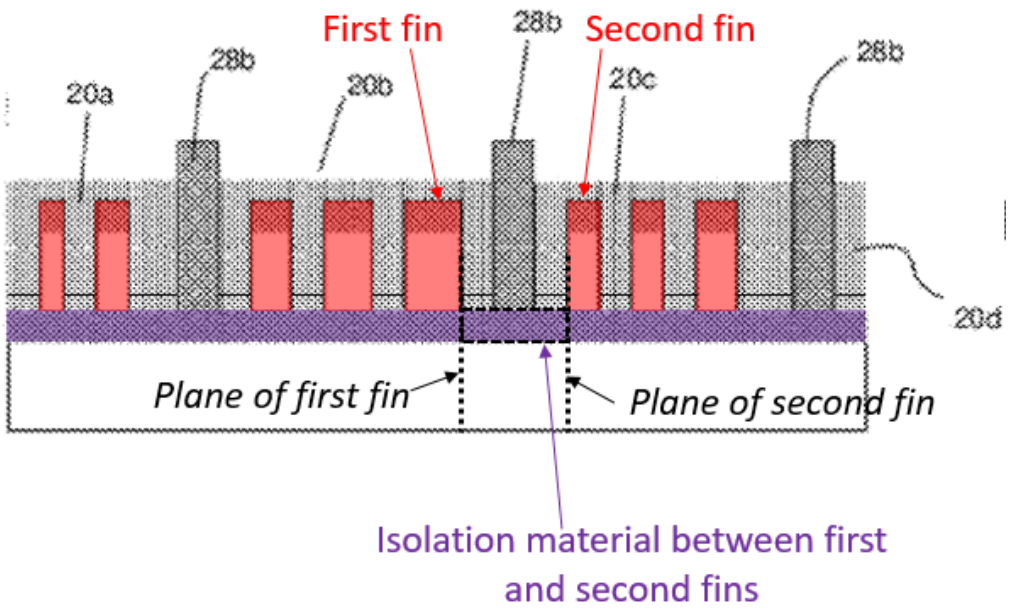




Excerpts from Anderson, FIGS. 9 and 11 (annotated)

**[26c] an isolation material between the first fin and the second fin;**

*In the combination, Anderson's buried oxide layer is an isolation material*

133. The Anderson-Lin combination renders obvious [26c]. For instance, the Anderson-Lin combination structure includes **an isolation material**, *e.g.*, based on Anderson's ***buried oxide layer 10b***, which I have highlighted in purple in the composite figure below. *See* SAMSUNG-1006 (Anderson), [0032] ("The SOI wafer can include ***a buried oxide 10b*** sandwiched between a lower Si layer 10 and upper silicon layer 10c"), [0036]-[0037], FIGS. 9-14. *See also* Anderson's buried oxide layer 10b (*e.g.*, **an isolation material**) of FIGS. 15-24 (*id.*, [0041]-[0045]); *see* FIG. 25, claims 3 and 15.




Anderson-Lin cross-sectional composite figure

134. In the Anderson-Lin combination structure, the buried oxide layer 10b is **an isolation material** because it provides electrical isolation between fins. Anderson's buried oxide layer 10b is the oxide layer of an SOI wafer, and the fins are disposed directly on that oxide layer. *See* SAMSUNG-1006 (Anderson), [0032]-[0037], FIGS. 9-14; *see also* [0041]-[0046], FIGS. 16-23. In FinFET devices, buried oxide layers of SOI wafers provide electrical isolation between fins. *See* SAMSUNG-1009 (Chang), [0041] ("diffusions 104, each isolated from each other in embodiments where the substrate 102 is an SOI substrate. In other embodiments, such as when the substrate 102 is a bulk substrate, the formed diffusions 104 may not be isolated from each other by the buried oxide layer 502"); SAMSUNG-1033, 2:19-21 ("Semiconductor devices are formed in and

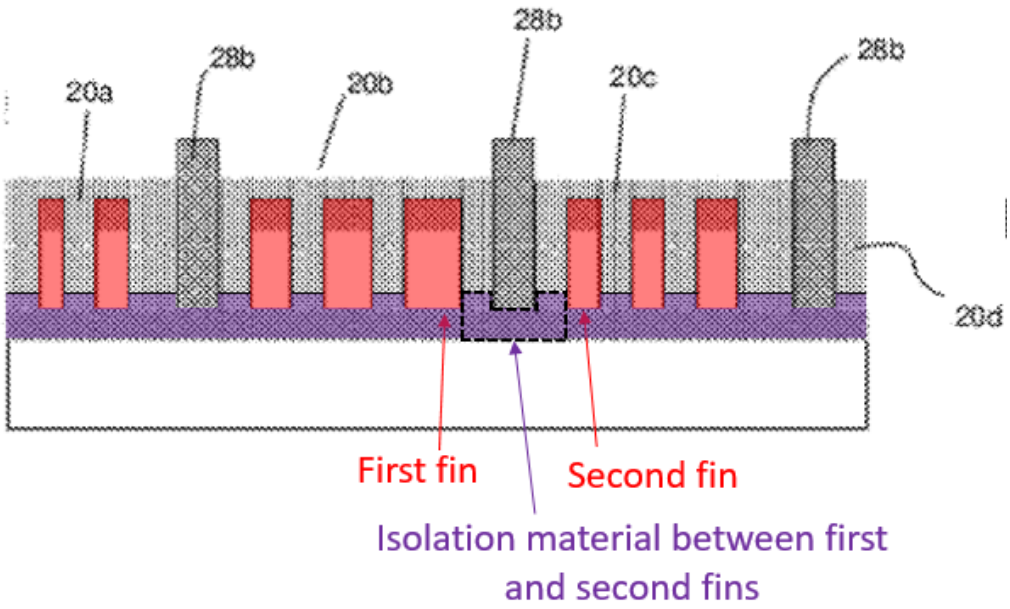
above the active layer of an SOI substrate. The fins are formed in the active layer and the buried insulation layer provides good isolation between adjacent fins") .

135. The buried oxide layer is **between the first fin and the second fin** in the combination because at least a portion of the buried oxide layer (outlined in dashes in the composite figure above) is disposed in the space separating the fins. Specifically, each fin defines a plane, *e.g.*, the plane of its inward-facing edge. I have marked these planes in dotted lines in the composite figure above. The buried oxide layer is between the fins in that a portion of the buried oxide layer is disposed in the space separating the plane defined by the first fin and the plane defined by the second fin.

*In the combination, the buried oxide layer and the STI around the fins together are an isolation material*

136. Alternatively or additionally, in the Anderson-Lin combination structure, a dielectric layer (*e.g.*, Lin's dielectric layer 114) is disposed on the buried oxide layer and around the base of the fins (*e.g.*, Anderson's isolation structures 28a) to provide STI around the fins. *See* SAMSUNG-1007 (Lin), 2:55-62 ("The dielectric layer 114, which acts as a shallow trench isolation (STI) around the fins"), claim 1 ("forming a first dielectric layer between adjacent fins"), claim 9 ("forming a first dielectric layer between ends of the two fins"), FIGS. 1A-5C. In the combination structure, the buried oxide layer and the dielectric layer disposed

around the base of the fins, both of which I have highlighted in purple in the composite figure below, together are **an isolation material**.




Anderson-Lin cross-sectional composite figure

137. The dielectric layer and the buried oxide layer are **an isolation material** because they provide electrical isolation between fins. For instance, Lin describes that the dielectric layer "acts as a shallow trench isolation (STI) around the fins." SAMSUNG-1007 (Lin), 2:55-58. Indeed, it was well-known that STI regions disposed around the base of fins in FinFET devices provide electrical isolation between those fins. *See* SAMSUNG-1005 (Tseng), 4:25-29 ("the trenches 22 are filled with a dielectric material to form the isolation regions 204 to define and electrically isolate the various fins of the fin structure 202. In one example, the isolation regions 204 include shallow trench isolation (STI) regions");

SAMSUNG-1010 (Akarvardar), 1:43-45 ("In bulk FinFET technology, isolation regions may be used to electrically insulate adjacent devices or to electrically separate the fins of a given device from one another"); SAMSUNG-1031, 5:16-18; SAMSUNG-1034, 2:24-36; SAMSUNG-1035, 1:22-32. Moreover, the buried oxide layer provides electrical isolation, as I have already discussed.

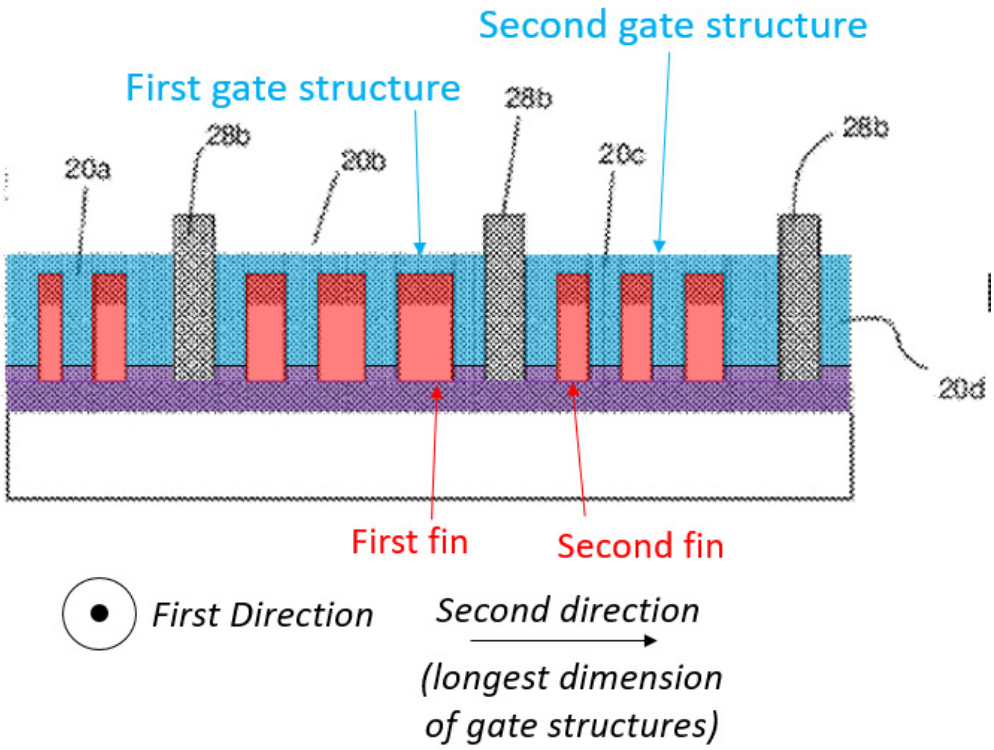
138. The isolation material (*e.g.*, the buried oxide layer and the STI material around the fins) is **between the first and second fin** in the combination structure at least because a portion of the isolation material (outlined in dashes in the composite figure above) is disposed in the space separating the first and second fins. Specifically, the STI material is **between the fins**, as can be seen from the figure and as described by Lin. *See* SAMSUNG-1007 (Lin), 2:55-62 ("[t]he dielectric layer 114 … acts as a shallow trench isolation (STI) ***around the fins***"), claim 1 ("forming a first dielectric layer ***between adjacent fins***"), claim 9 ("forming a first dielectric layer ***between ends of the two fins***"), Figs. 1A-5C. The buried oxide layer is also **between the fins** as discussed above.

**[26d] a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;**

**[26e] a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the**

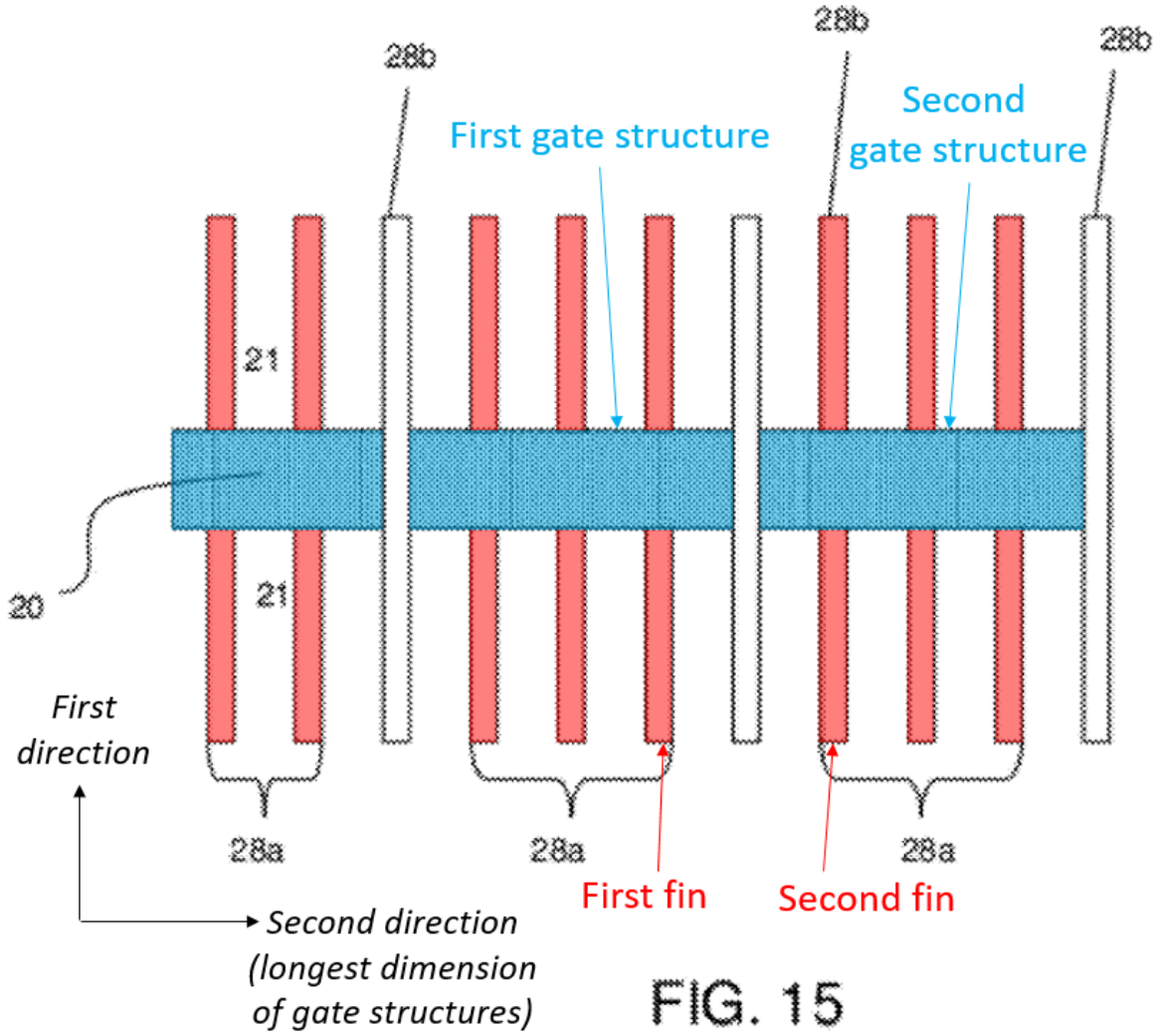
**first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;**

139. The Anderson-Lin combination renders obvious [26d] and [26e]. For instance, the Anderson-Lin combination structure includes **first and second gate structures**, *e.g.*, based on Anderson's ***gate stack 20***, blue in the composite figures below. *See* SAMSUNG-1006 (Anderson), [0038]-[0039] ("***gate stack 20*** is formed over the isolation structures 28a and 28b and the exposed portions of the wafer 10. … [T]he gate electrode 20 is partially etched … In this way, gates 20a-20d are formed on the wafer 20, separated by the isolation structures 28b."), FIGS. 13-15. *See also* Anderson's "gate stack 20" (*e.g.*, **gate structures**) in FIGS. 23-24 (*id.*, [0047]-[0048]) and "electrically isolated gates 20e, 20f" (*e.g.*, **gate structures**) of FIGS. 25-26 (*id.*, [0051]); *see* [0005] ("forming ***gate electrodes*** within each deep trench between each fin of the dual height fin array, burying the second plurality of fins and abutting sides of the plurality of fins comprising the raised portions"), [0006] ("forming gate electrodes within each trench of the plurality of trenches"), [0007] ("a plurality of gate stack regions"), [0001], [0019].




Anderson-Lin cross-sectional composite figure[9]

[9] The cross-sectional composite figures in [26d] through [35] of Grounds 3A-3B identify both the buried oxide layer and the STI regions around the fins as isolation material by their purple highlighting. However, as I have discussed, the STI regions are an optional alternative and are not necessary to render obvious the features of the Challenged Claims.




Anderson-Lin top-view composite figure

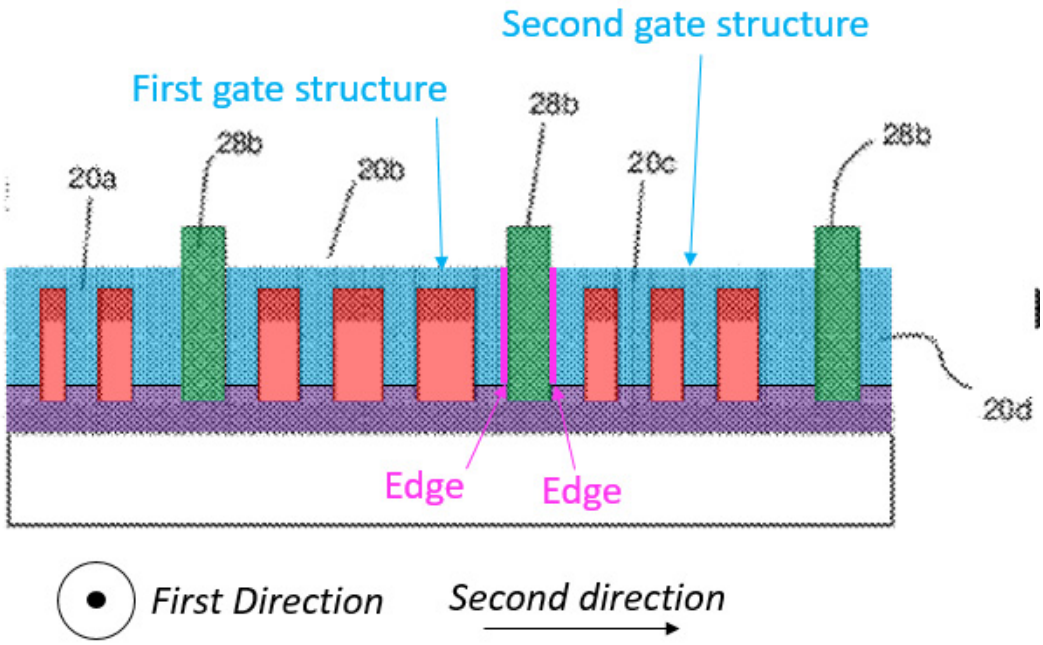
140. As illustrated in the figures above, the first and second gate structures have **a longest dimension along a second direction**: the longest dimension of the gate structures is traversed ***as one moves along the gate structures in the second direction*** (from left to right in both figures). *See* SAMSUNG-1006 (Anderson), FIGS. 14-15, 23-26.

141. The composite figures also illustrate that **the second direction is orthogonal to the first direction**, *e.g.*, the gate stacks 20 extend in a direction orthogonal to the extension of the isolation structures 28a. *See* SAMSUNG-1006 (Anderson), FIGS. 14-15, 23-26. To the extent that Anderson does not explicitly state this orthogonality, it is my opinion that a POSITA would have understood this to be the case, or otherwise found this to be obvious, consistent with the schematic depiction of Anderson's structure (*see* SAMSUNG-1006 (Anderson), FIGS. 14-15, 23-26) and given that gate structures orthogonal to fins in FinFET devices was well-known in the art as of the Critical Date. *See*, *e.g.*, SAMSUNG-1008 (Kawa), [0053]; SAMSUNG-1029, [0042]; SAMSUNG-1030, Abstract.

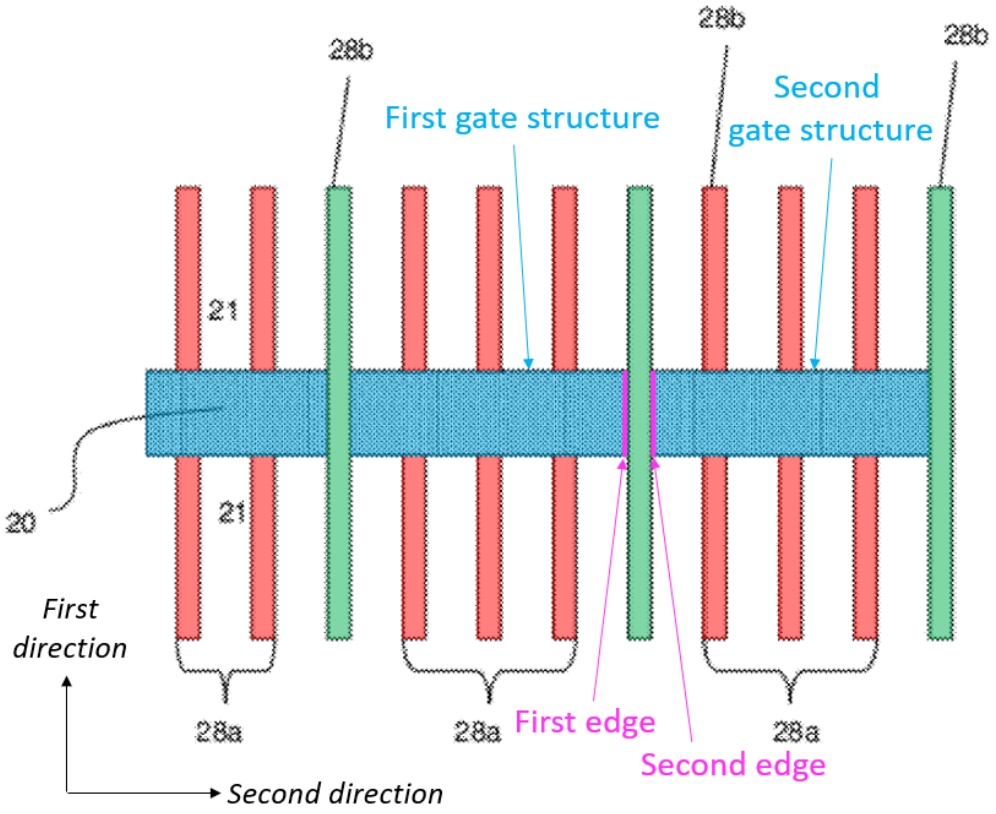
142. The **first gate structure is over the first fin** and **the second gate structure is over the second fin**, as shown in the composite figures above. Indeed, Anderson describes that "gate stack 20 is formed ***over the isolation structures 28a*** and 28b… The gate stack 20 can be, for example, a gate dielectric and a gate electrode material, ***conformally deposited on the isolation structures 28a*** and 28b." SAMSUNG-1006 (Anderson), [0038]; *see* [0039] ("the gate electrode will ***cover or bury the isolation structures 28a***"), [0047] ("gate stack 20 is formed over the isolation structures 28a′"), [0005] ("forming gate electrodes … ***burying the second plurality of fins***"), [0006] ("forming gate electrodes … which

bury the second fins"), [0007] ("a plurality of gate stack regions ***spanning over the plurality of first height fin structures***"), FIGS. 14-15, FIGS. 23-26.

143. Moreover, in the Anderson-Lin combination structure, **the second gate structure is discontinuous with the first gate structure**, as illustrated in the composite figures, which I have reproduced again below. For instance, the first and second gate structures (*e.g.*, Anderson's gate stacks 20, blue) are **discontinuous** in that they are separated by the isolation structure 28b (green; *see* [26f]). Anderson describes this discontinuity: "gates 20a-20d are formed on the wafer 20, ***separated by the isolation structures*** 28b." SAMSUNG-1006 (Anderson), [0039]; *see* [0048]. Specifically, Anderson describes that "the gates abut against the sides of the isolation structure 28b, which will provide ***a physical*** and electrical ***separation between the gates***." *Id.*, [0039]; *see* [0048] ("the isolation structure 28b′ … provide[s] a physical and electrical separation between the gates"), [0051] ("The electrically isolated gates 20e, 20f are also isolated from other gates 20′ by the isolation structures 28b′"), [0019] ("the present invention includes selectively raised isolation regions at desired gate isolation points to provide isolation structures between adjacent gates (transistors)"), [0005] ("The plurality of fins comprising the raised portions electrically and physically isolate adjacent gate electrodes"), [0007] ("the second height fin structure which separate the gate stacks"), [0001], [0006], FIGS. 14-15, FIGS. 23-26.




Anderson-Lin cross-sectional composite figure




Anderson-Lin top-view composite figure

144. The discontinuity between the first and second gate structures is **along the second direction**: the discontinuity is reached ***as one moves in the second direction*** from one gate structure to the other (*e.g.*, from left to right in the figures *supra*). *See* SAMSUNG-1006 (Anderson), FIGS. 14-15, 23-26.

145. The composite figures above also illustrate that **the second gate structure has an edge** (outlined in pink) **that faces an edge of the first gate structure** (also outlined in pink), *e.g.*, the edge (pink) of the second gate structure (blue) that contacts the isolation structure 28b (green) faces the edge (pink) of the first gate structure (blue) that also contacts that isolation structure (green). *See*

SAMSUNG-1006 (Anderson), [0039] ("***the gates abut against the sides of the isolation structure 28b***, which will provide a physical and electrical separation between the gates"), FIGS. 14-15; *see also* [0048], [0005]-[0007], [0031], FIGS. 23-26.

146. The edges face one another **along the second direction**: from the edge of the first gate structure, the edge of the second gate structure is reached ***as one moves in the second direction*** (*e.g.*, from left to right in the composite figures above).

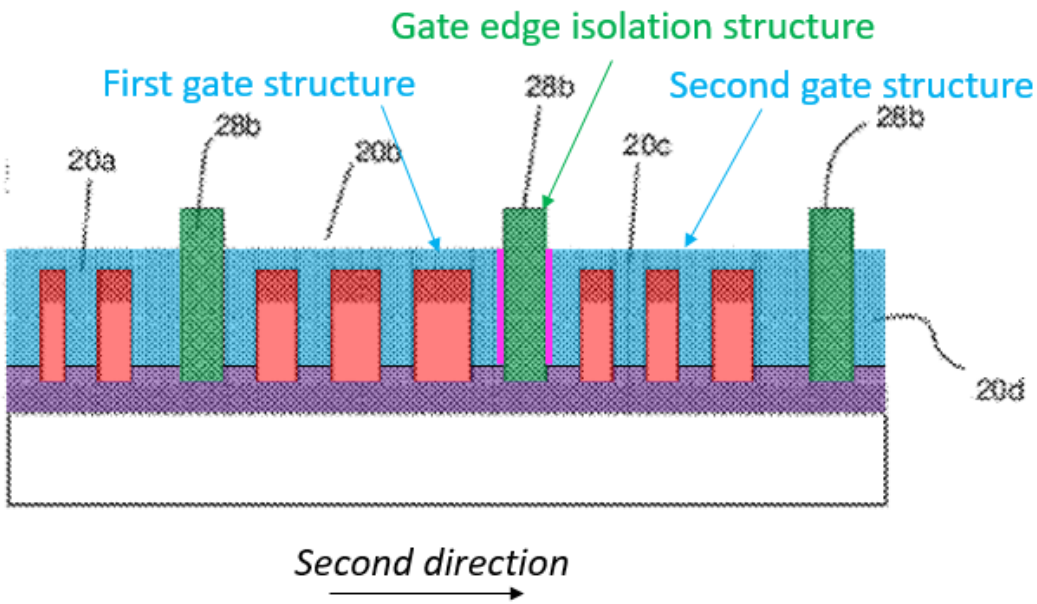
147. In the Anderson-Lin combination structure, Anderson describes that the first and second gate structures (*e.g.*, Anderson's gate stack 20) each includes **a gate dielectric layer and a gate electrode**. *See* SAMSUNG-1006 (Anderson), [0038] ("The gate stack 20 can be, for example, ***a gate dielectric and a gate electrode material***, conformally deposited on the isolation structures 28a and 28b and the exposed portions of the wafer 10"), [0047].

**[26f] a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and**

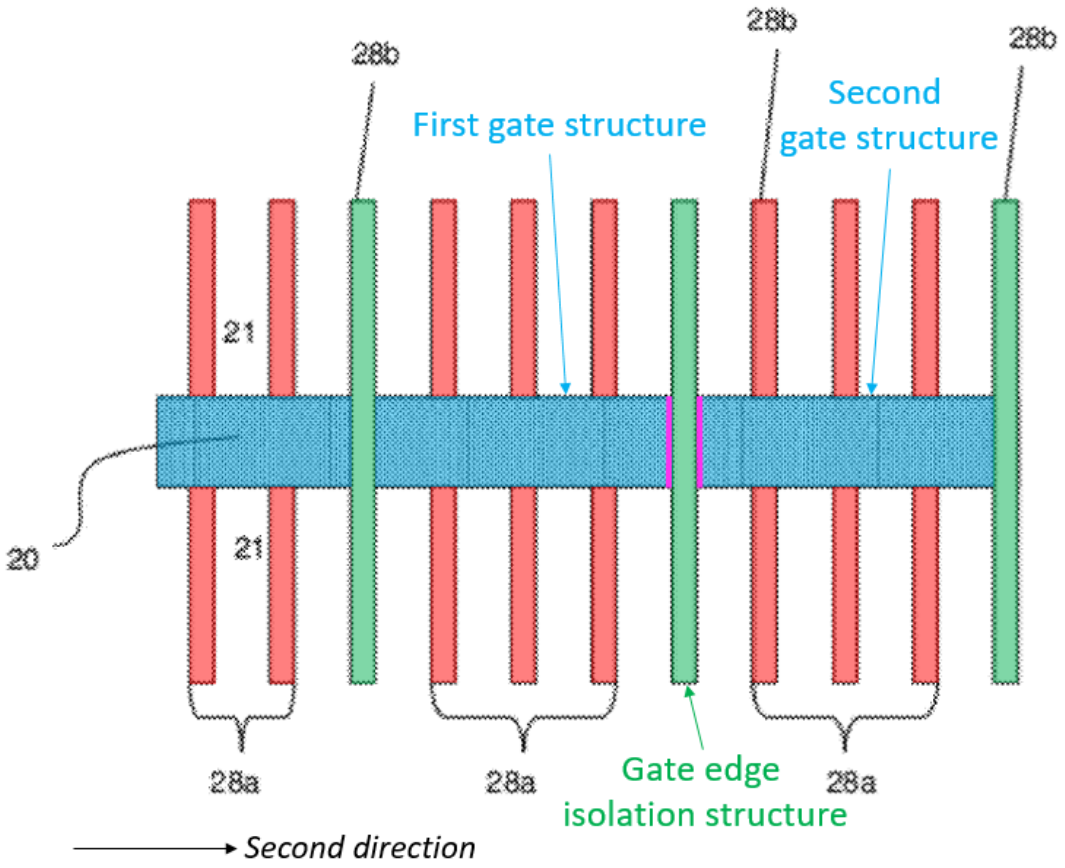
<u>*The Anderson-Lin combination includes a gate edge isolation structure*</u>

148. The Anderson-Lin combination renders obvious [26f]. For instance, the Anderson-Lin combination structure includes **a gate edge isolation structure**, *e.g.*, based on Anderson's ***isolation structure 28b***, which I have highlighted in

green in the composite figure below. *See* SAMSUNG-1006 (Anderson), [0037] ("dual height isolation structures 28a and 28b," where "***the isolation structure 28b*** is taller than the surrounding isolation structures 28a"), [0038]-[0040], FIGS. 11-15. See also Anderson's "isolation structure[] … 28b‴" (e.g., a gate edge isolation structure) in FIGS. 19-24 (id., [0047]-[0048]) and "isolation structure 28b⁗" (e.g., a gate edge isolation structure) in FIGS. 25-26 (see id. [0051]); see [0001] ("devices having gate-to-gate isolation structures"), [0005] ("the plurality of fins comprising the raised portions"), [0006] ("the first fins comprising the raised portions"), [0007] ("the second height fin structure which separate the gate stacks"), [0019] ("selectively raised isolation regions … to provide isolation structures between adjacent gates (transistors)").




Anderson-Lin cross-sectional composite figure




Anderson-Lin top-view composite figure

149. In the combination, Anderson's isolation structure (*e.g.*, isolation structure 28b) is a **gate edge isolation structure**: it is disposed between the edges of the gate structures (discussed below) and isolates those gate structures from one another (*e.g.*, physically and electrically).

150. First, Anderson's isolation structure 28b both ***physically isolates*** and ***electrically isolates*** the first and second gate structures. Anderson describes that the isolation structure 28b provides "***a physical and electrical separation between the gates 20a-20d***," "allow[ing] adjacent gates to be isolated." SAMSUNG-1006

(Anderson), [0039]; *see* [0048] ("the isolation structure 28b′ … will provide a physical and electrical separation between the gates 20a-20b"), [0051], [0001] ("gate-to-gate isolation structures"), [0019] ("isolation structures between adjacent gates (transistors)"), [0040], [0050].

151. As shown in the composite figures above, in the Anderson-Lin combination structure, the gate edge isolation structure is between and in contact with the edge of the first gate structure and the edge of the second gate structure, *e.g.*, Anderson's isolation structure 28b (green) is between and in contact with the edges (pink) of the gates (blue). Anderson describes this configuration with reference to FIGS. 14-15: "gates 20a-20d are … *separated by the isolation structures* … [and] the gates *abut against the sides of the isolation structure 28b*." SAMSUNG-1006 (Anderson), [0039]; *see* [0048] ("gates 20a-20b are … separated by the isolation structures 28b′," and particularly, "the gates abut against the sides of the isolation structure 28b′"), [0006] ("gate electrodes … which bury the second fins and abut sides of the first fins"), [0007] ("a plurality of gate stack regions … abutting the second height fin structure which separate the gate stacks"), FIGS. 23-26.

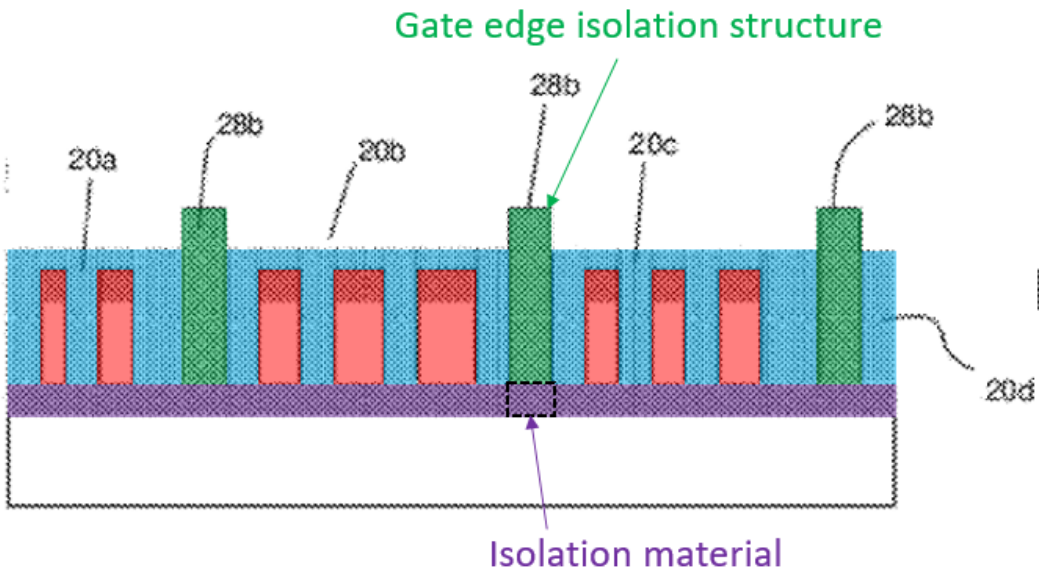
152. The positioning of the gate edge (*e.g.*, Anderson's isolation structure 28b) is **in contact with the edges of the gate structures** in the combination is also made apparent by Anderson's description of the fabrication process. Anderson

describes "form[ing] trenches 26 and fins 27a and 27b (isolation structures)," such that the sidewalls of the isolation structures are exposed. SAMSUNG-1006 (Anderson), [0036], FIG. 12; *see* [0044], FIG. 11. Following removal of a pad film, which "leav[es] isolation structures 28a and 28b," a "gate stack is formed over the isolation structures 28a and 28b." *Id.*, [0037]-[0038], FIGS. 12-14; *see* [0045]-[0047], FIGS. 23-26. No processing is performed to cover the exposed isolation structure sidewalls until the gate stack is deposited. Thus, the gate stack (*e.g.*, the gate structures) is deposited in contact with the sidewalls of the isolation structure 28b (*e.g.*, the gate edge isolation structure).

153. The gate edge isolation structure is between and in contact with the edges of the gate structures **along the second direction**: ***as one moves in the second direction*** (*e.g.*, from left to right in the composite figures) starting from the edge of the first gate structure, one reaches first the gate edge isolation structure and then the edge of the second gate structure.

*The gate edge isolation structure is over the isolation material*

154. As shown in the composite figure below, in the Anderson-Lin combination structure, when the isolation material (purple) is a buried oxide layer (*see* [26c]), **the gate edge isolation structure is over the isolation material** in that the gate edge isolation structure (green) is positioned over at least a portion of the isolation material (*e.g.*, the portion I have outlined in dashes).

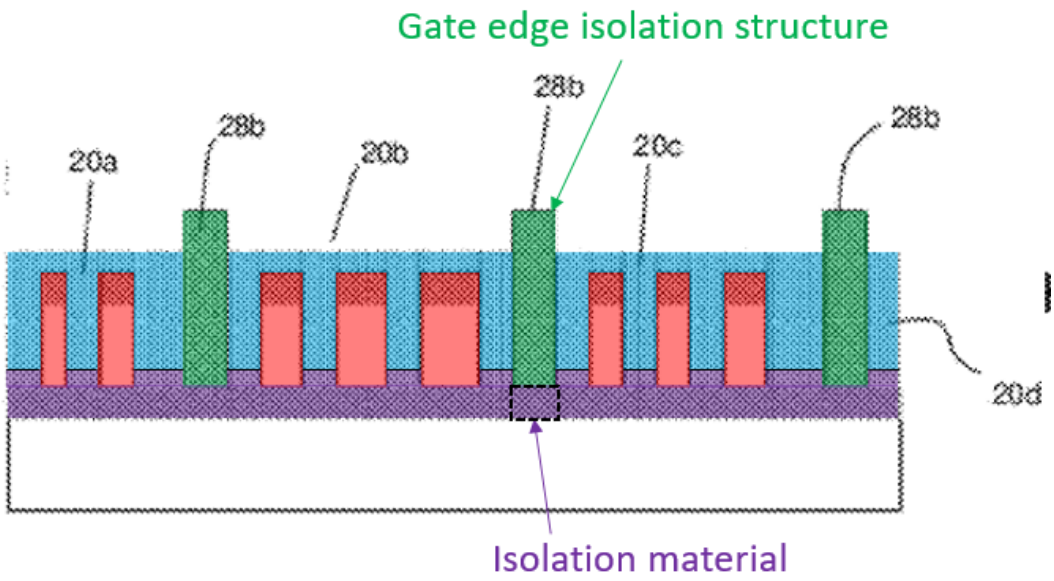



Anderson-Lin cross-sectional composite figure

155. The positioning of the gate edge isolation structure **over the isolation material** (*e.g.*, over the buried oxide layer) is also made apparent by Anderson's description of the fabrication process. Anderson's process begins with an SOI wafer including "a buried oxide 10b sandwiched between a lower Si layer 10a and an upper silicon layer 10c." SAMSUNG-1006 (Anderson), [0032], FIG. 9; *see* [0041], FIG. 16. Fins 27b (which will become the isolation structure 28b; *see* [0037]) are formed by etching trenches in the upper silicon layer 10c, which sits on the buried oxide layer 10b. *See id.*, [0036], FIG. 11; *see also* [0045]-[0046] and FIGS. 20-21. That is, Anderson's fabrication process demonstrates that **the gate**

**edge isolation structure** (*e.g.*, the isolation structure 28b) is **over the isolation material** (*e.g.*, the buried oxide layer).

156. Alternatively or additionally, as shown in the composite figure below, when the isolation material (purple) is the buried oxide layer and the STI regions around the base of the fins (*see* [26c]), **the gate edge isolation structure is over the isolation material** in that the gate edge isolation structure (green) is positioned over at least a portion of the isolation material (*e.g.*, the isolation material outlined in dashes). For instance, the gate edge isolation structure is at least **over** the buried oxide layer portion of the isolation material.

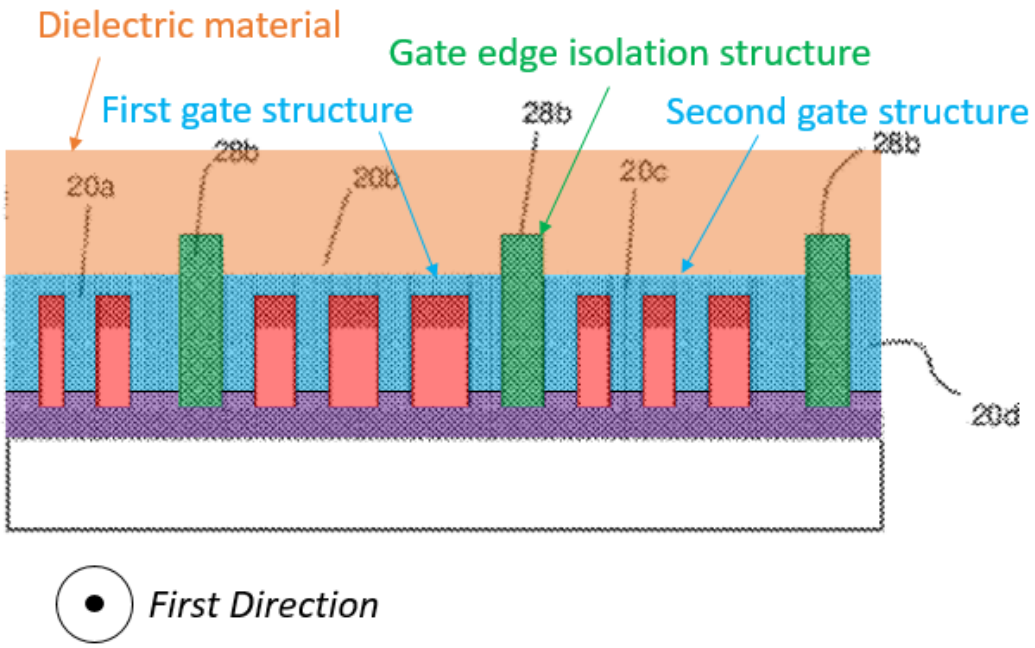



Anderson-Lin cross-sectional composite figure

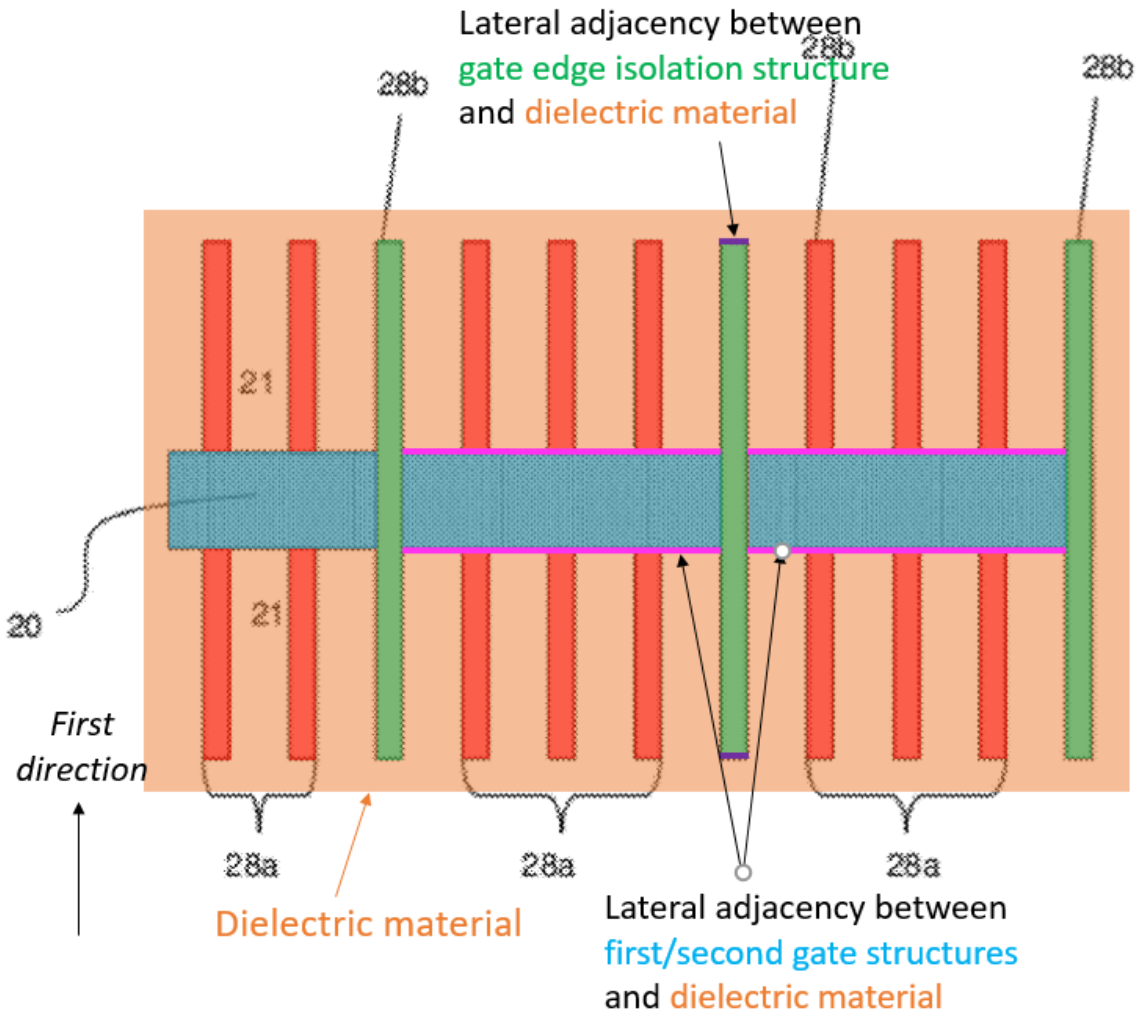
**[26g] a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to**

**the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.**

157. The Anderson-Lin combination renders obvious [26g]. For instance, in the Anderson-Lin combination structure, based on the teachings of Lin, "***an inter-layer dielectric (ILD)***," which I have highlighted in orange in the composite figures below, is "formed over the gate electrodes" (blue) and over the gate edge isolation structure (green). SAMSUNG-1007 (Lin), 5:15-17; *see* claim 9 ("after forming the first notch, forming a second dielectric layer in the first notch"), claim 10 ("wherein the second dielectric layer extends between the first gate electrode and the second gate electrode"), FIGS. 5A-5C; *see* SAMSUNG-1006 (Anderson), [0050]. In the combination, the ILD is **a dielectric material**. I note that the fins, gate structure, and gate edge isolation structures all appear in the top-view figure. These structures would be covered by the ILD, as shown in the cross-sectional view figure; I have shown these structures in top-view for illustrative purposes only.




Anderson-Lin cross-sectional composite figure




Anderson-Lin top-view composite figure

158. I have outlined the sidewalls of the first and second gate structures in pink in the top view figure above. *See* SAMSUNG-1006 (Anderson), FIG. 15; *see also* FIGS 24, 26. These sidewalls extend into the page of the top view, and the dielectric material fills the space next to those sidewalls. *See id.*, FIG. 14; *see also* FIGS. 23, 25. The **dielectric material is laterally adjacent to the first and second gate structures** at least at these pink-outlined sidewalls. *See* SAMSUNG-

1006 (Anderson), FIGS. 14-15, 23-26. For instance, the dielectric material is near (*e.g.*, next to) the gate structure sidewalls. Alternatively or additionally, to the extent that that a spacer is disposed on the sidewalls of the gate structures (*see* SAMSUNG-1006 (Anderson), [0029] ("Sidewall spacers and capping layers can also be formed using conventional deposition processes"), the dielectric material contacts those spacers. The dielectric material is thus laterally adjacent to the gate structures, *e.g.*, in that the dielectric material is near (*e.g.*, next to) the sidewalls of the gate structures (*e.g.*, separated only by the spacers).

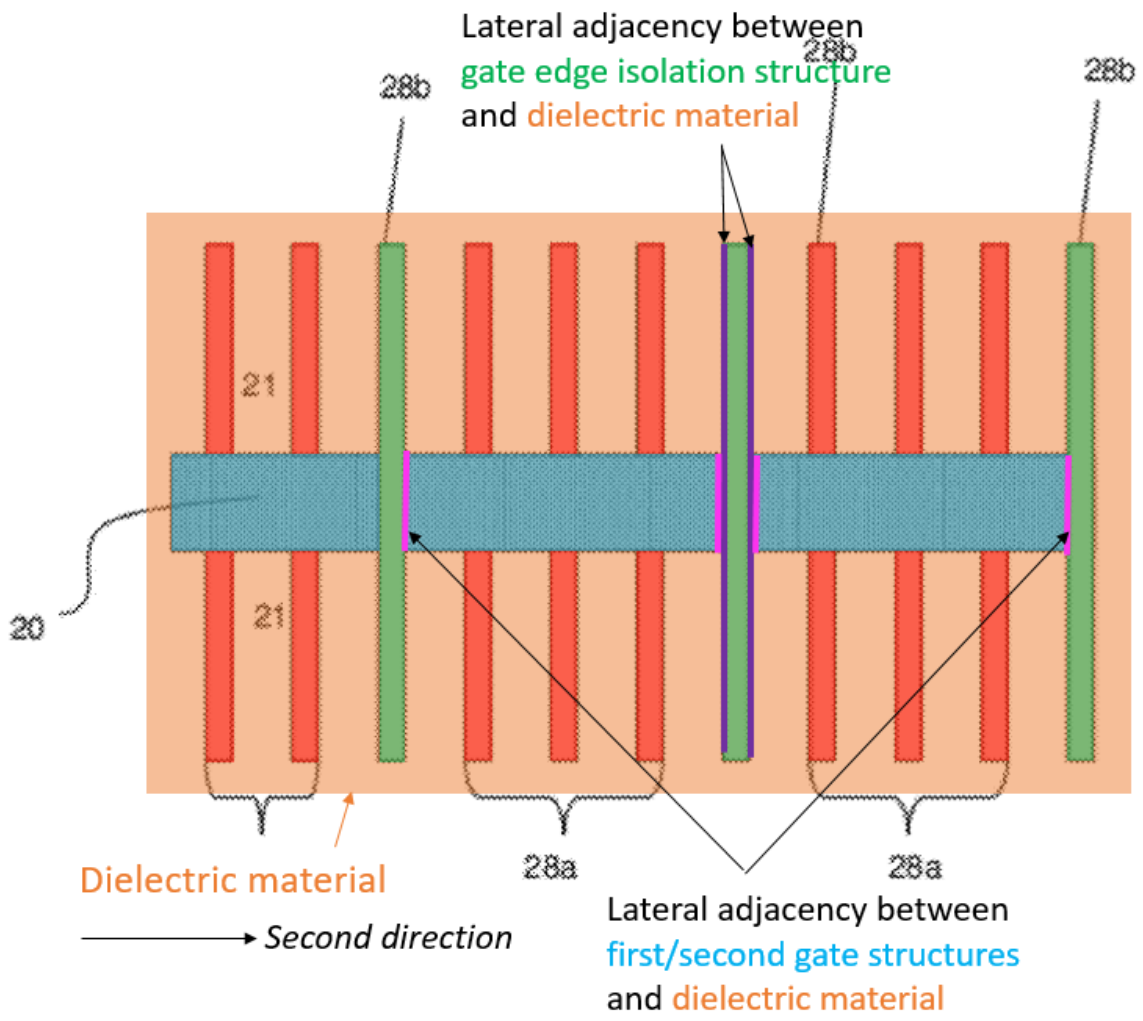
159. The dielectric material is laterally adjacent to the gate structures **along the first direction** at these pink-outlined sidewalls: viewing the structure starting from either of the gate structures and ***moving along the first direction*** (top to bottom in the top view figure), one reaches the dielectric material. *See* SAMSUNG-1006 (Anderson), FIGS. 14-15, 23-26.

160. I have outlined the short end walls of the gate edge isolation structure in purple in the top-view composite figure above. *See* SAMSUNG-1006 (Anderson), FIG. 15; *see also* FIGS 24, 26. These walls extend into the page of the top-view figure. As shown in the cross-sectional view, the dielectric layer fills the space next to these end walls. *See id.*, FIG. 14; *see also* FIGS. 23, 25. The **dielectric material is laterally adjacent to the gate edge isolation structure** at

least at these purple-outlined end walls. For instance, the dielectric material is near (*e.g.*, next to) the end walls of the gate edge isolation structure.

161. The dielectric material is laterally adjacent to the gate edge isolation structure **along the first direction** at these purple-outlined sidewalls: viewing the structure starting from the gate edge isolation structure and ***moving along the first direction*** (top to bottom in the top-view figure), one reaches the dielectric material. *See* SAMSUNG-1006 (Anderson), FIGS. 14-15, 23-26.

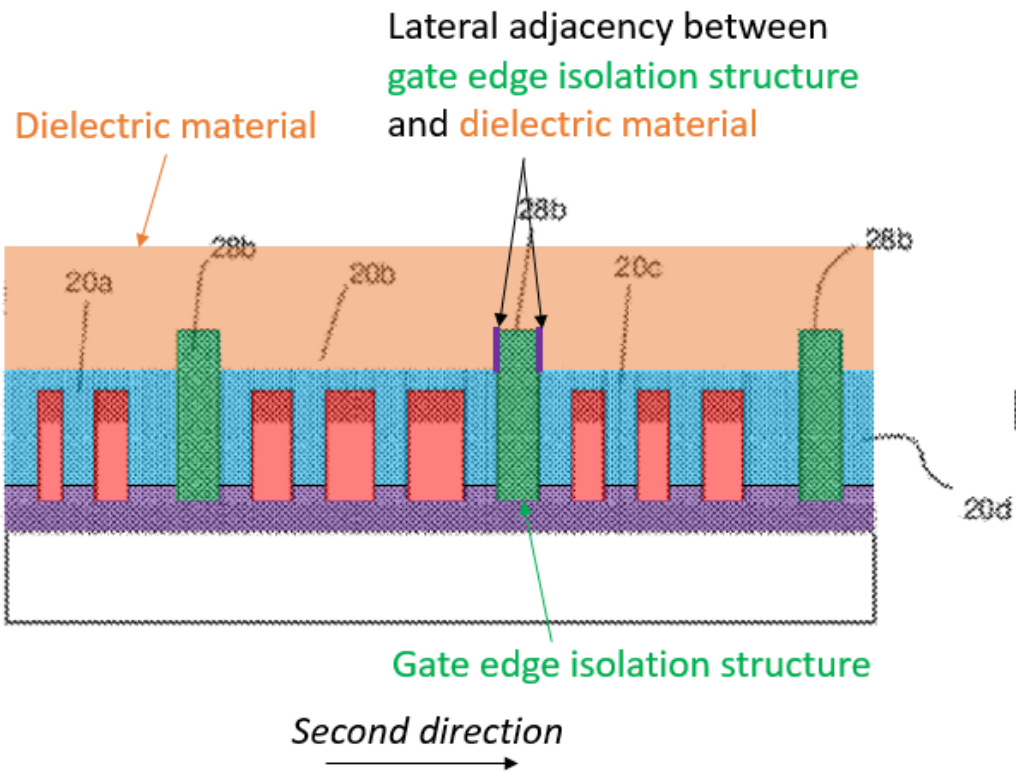
162. Alternatively or additionally, the dielectric material of the combination (*e.g.*, Lin's ILD) also is laterally adjacent to the gate structures at the pink-outlined edges of the gate structures in the alternative top-view composite figure below. For instance, viewing the structure starting from, *e.g.*, the second gate structure and moving along the second direction (left to right in the top-view figure), one reaches the dielectric material, passing through the end-most isolation structure 28b. To the extent this spatial relationship is considered to be laterally adjacent **along the first direction**, the dielectric material of the combination is laterally adjacent to the first and second gate structures along the first direction.




Anderson-Lin top-view composite figure (alternative)

163. Similarly, the dielectric material of the combination also is laterally adjacent to the gate edge isolation structure at the purple-outlined edges of the gate edge isolation structure in the alternative figure *supra* (*see also* the composite figure *infra*). For instance, viewing the structure starting from the gate edge isolation structure and moving along the second direction, one reaches the dielectric material. To the extent this spatial relationship is considered to be

laterally adjacent **along the first direction**, the dielectric material of the combination is laterally adjacent to the gate edge isolation structure along the first direction.




Anderson-Lin cross-sectional composite figure (alternative)

164. Also in the combination, **the dielectric material is discrete from the gate edge isolation structure**, *e.g.*, the ILD is discrete from the isolation structure 28b. For instance, the two structures are discrete at least in that ***they are formed in two distinct processing steps***: the dielectric material is deposited over the gate structures (*see* SAMSUNG-1007 (Lin), 5:15-17 ("an interlayer dielectric (ILD) 560 formed over the gate electrodes"), which are formed after the gate edge

isolation structure has already been fabricated (*see* SAMSUNG-1006 (Anderson), [0038] ("gate stack 20 is formed over the isolation structures 28a and 28b"). *See id.*, [0032]-[0038], [0041]-[0047], [0050].

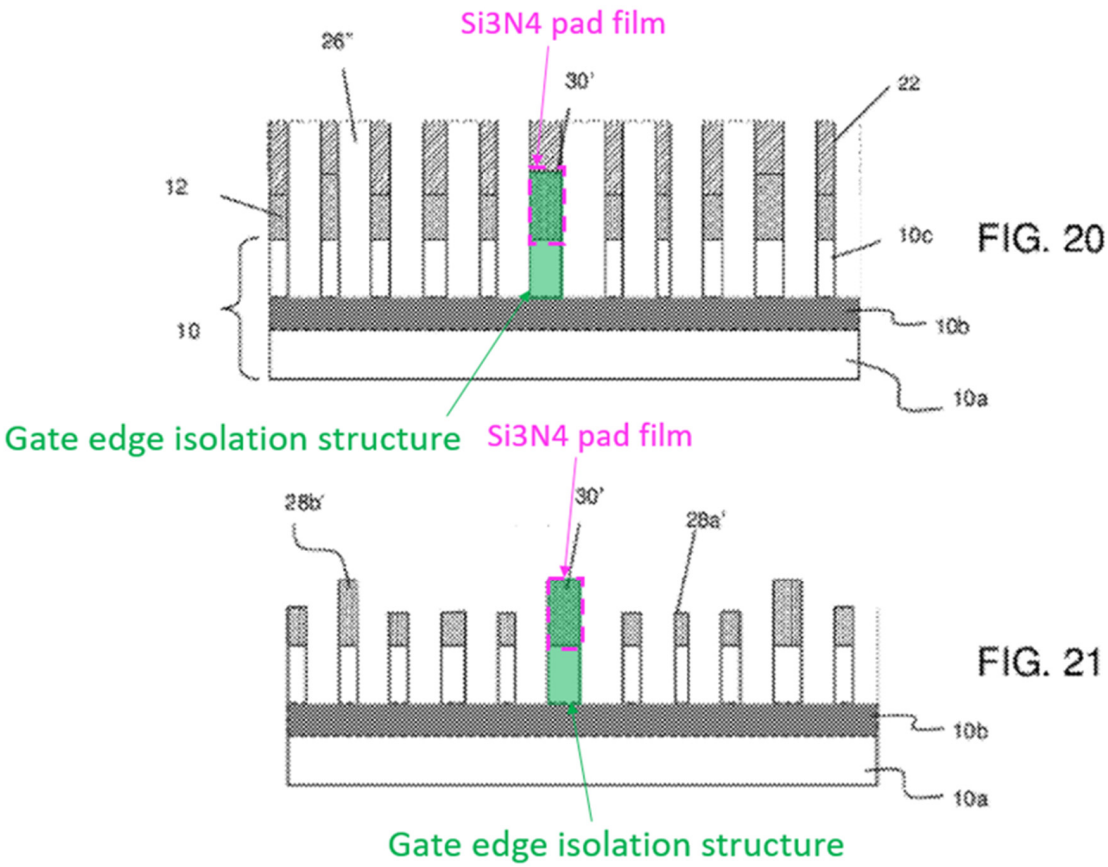
165. Alternatively or additionally, **the dielectric material is discrete from the gate edge isolation structure** at least in that ***they are composed of two different materials***. For instance, in the combination, the dielectric material (*e.g.*, Lin's ILD 560) can be "formed of an oxide such as phospho-silicate glass (PSG), boro-silicate glass (BSG), boron-doped phospho-silicate glass (BPSG), TEOS, or the like." SAMSUNG-1007 (Lin), 5:15-20. The gate edge isolation structure (is a different material and thus is distinct from the dielectric material. For instance, Anderson's isolation structure 28b (a gate edge isolation structure) includes $SiO_2$. *See* SAMSUNG-1006 (Anderson), [0035] ("the trenches are filled with an insulator material to form isolation structures 24. In embodiments, the insulator material is SiO2."), [0036]-[0037] (explaining the fabrication process by which the isolation structures 24 are formed into the isolation structures 28b), FIGS. 10-12. *See also* [0041]-[0046] (describing a fabrication process in which the isolation structure 28b′ (a gate edge isolation structure) is formed from portions of a silicon layer 10c and portions of a pad film containing $SiO_2$, $Si_3N_4$, or both; *e.g.*, the gate edge isolation structure includes silicon and silicon nitride); FIGS. 16-21; *see* [27].

### (2) Claim 27

**[27] The integrated circuit structure of claim 26, wherein the gate edge isolation structure comprises silicon and nitrogen.**

166. The Anderson-Lin combination renders obvious [27]. For instance, in the Anderson-Lin combination structure, when the gate edge isolation structure is based on Anderson's "isolation structure[] … 28b′" (SAMSUNG-1006 (Anderson), [0047]-[0048], FIGS. 19-24; *see* [26f]), **the gate edge isolation structure comprises silicon and nitrogen**, as demonstrated by Anderson's description of the process of fabricating the isolation structure 28b′.

167. As shown in FIG. 20, which I have reproduced and annotated below, "trenches 26′ are formed in [] pad films 12, 22," where "the pad film 12 can be a stack material such as … Si3N4." SAMSUNG-1006 (Anderson), [0042], [0044]. A portion of the $Si_3N_4$ pad film is outlined in pink. The trenches 26′ are separated by fins 27′, which are composed of the pad film 22, the $Si_3N_4$ pad film 12, and a silicon layer 10c. *See id.*, [0041], [0044]-[0045]. As shown in FIG. 21, also reproduced below, "the remaining portion of the pad film 22 is removed from the fins, leaving isolation structures 28a′ and 28b′." *Id.*, [0045]. The isolation structure 28b′ (green) is composed of the remaining material of the corresponding fin 27′, *i.e.*, ***the $Si_3N_4$ pad film*** and the silicon layer. That is, the isolation structure 28b′ (*e.g.*, the gate edge isolation structure) includes Si3N4, *i.e.*, **comprises silicon and nitrogen**.



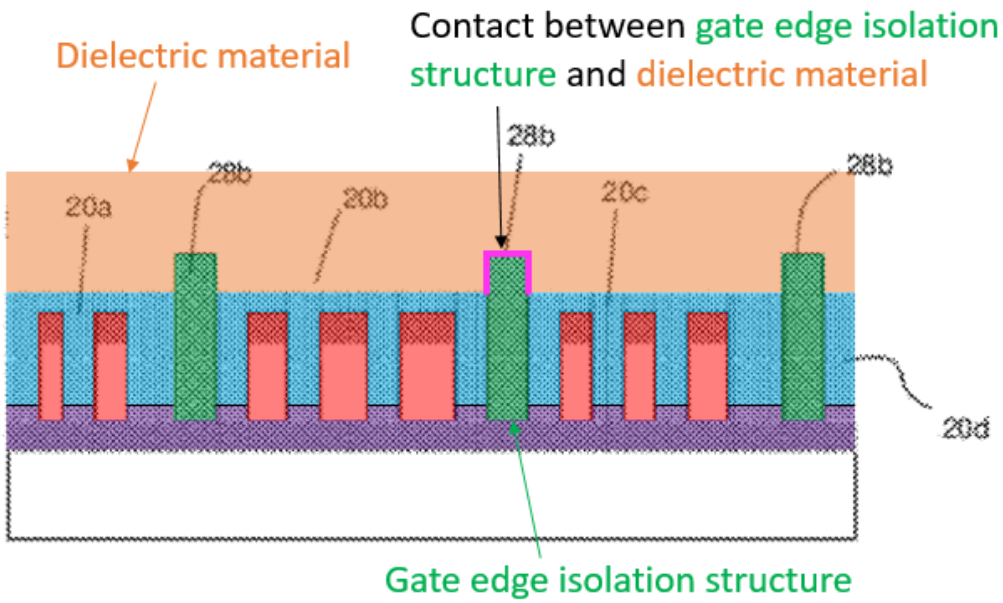

Excerpt from Anderson, FIGS. 20-21 (annotated)

**(3) Claim 28**

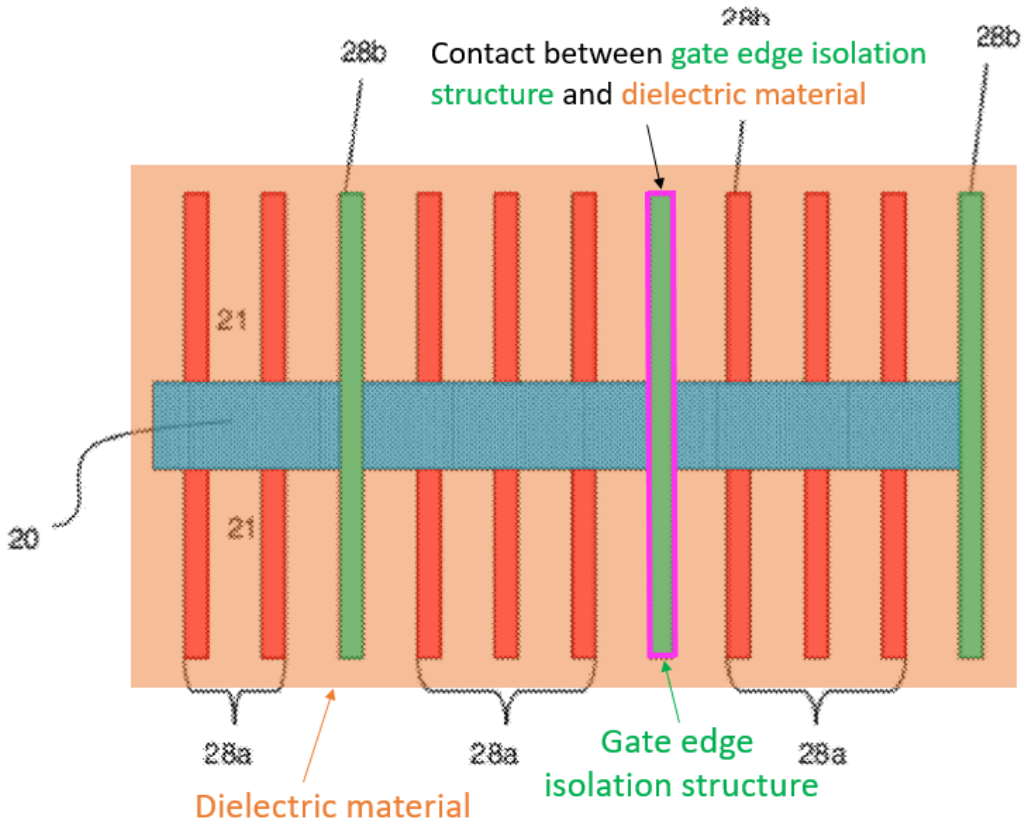
**[28] The integrated circuit structure of claim 26, wherein the dielectric material is in contact with the gate edge isolation structure.**

168. The Anderson-Lin combination renders obvious [28]. For instance, in the Anderson-Lin combination structure, the dielectric material (*e.g.*, an ILD as taught by Lin) is "formed over the gate electrodes" and over the gate edge isolation structure. SAMSUNG-1007 (Lin), 5:15-17. Thus, **the dielectric material is in contact with the gate edge isolation structure** at least on the top surface of the gate edge isolation structure. Moreover, the dielectric material also abuts, and thus

**is in contact with**, the exposed sidewalls and end surfaces of the gate edge isolation structure. *See* [26g]. I have outlined these surfaces of contact between the dielectric material (orange) and the gate edge isolation structure (green) in pink in the composite figures below.




Anderson-Lin composite figure



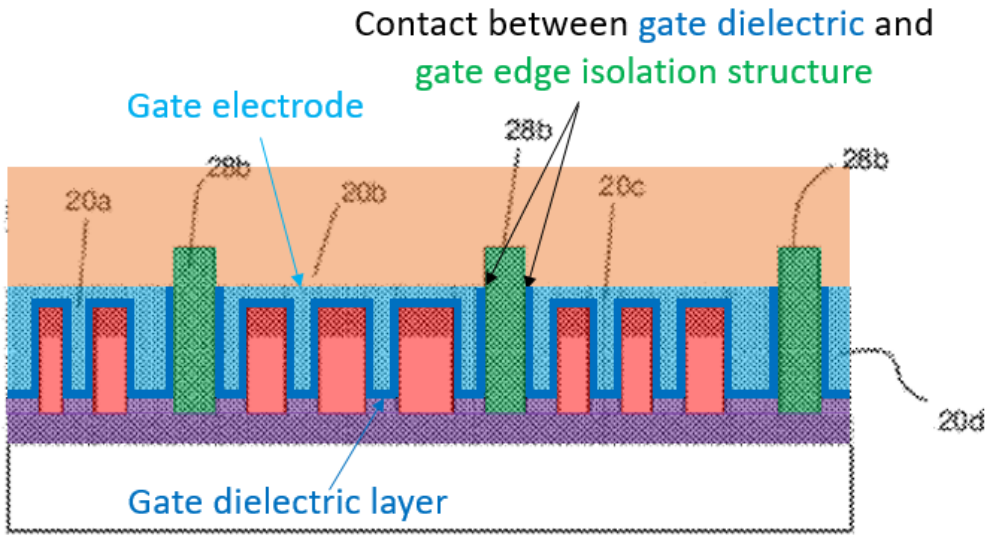

Anderson-Lin composite figure

**(4) Claim 29**

**[29] The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.**

169. The Anderson-Lin combination renders obvious [29]. For instance, in the Anderson-Lin combination structure, the gate structure is a "gate stack" that includes "a gate dielectric and a gate electrode material, conformally deposited on the isolation structures … 28b" and then "partially etched away to expose the isolation structure 28b." SAMSUNG-1006 (Anderson), [0038]; *see* [0038] ("gate stack 20 is formed over the isolation structures 28a and 28b"), [0047]. It is my

opinion that POSITA would have understood or found obvious that in deposition of a gate stack, the gate dielectric is deposited first, followed by deposition of the gate electrode, as was well-known in the art as of the Critical Date. *See* SAMSUNG-1025 (Ching), 4:39-5:56; SAMSUNG-1005 (Tseng), 8:62-9:4; SAMSUNG-1012 (Bohr), 11:4-14; SAMSUNG-1014 (Kuo), 7:8-42. This initial deposition of the gate dielectric coats the gate dielectric onto exposed surfaces, including the exposed sidewalls and tops of the fins (isolation structures 28a) and the isolation structures 28b. After deposition of the gate dielectric, the gate stack is etched away to expose the tops of the isolation structures 28b, but the gate dielectric remains in contact with the sidewalls of the isolation structures 28b. This is illustrated in the figure below, which shows the gate dielectric as a dark blue layer contacting the sidewalls of the isolation structures 28b. That is, Anderson's depositing of the gate stack "on the isolation structures … 28b," *e.g.*, on the gate edge isolation structure, involves first depositing the gate dielectric layer directly onto the gate edge isolation structure, and then depositing the gate electrode material onto the gate dielectric layer. SAMSUNG-1006 (Anderson), [0038]. As a result, **the gate edge isolation structure is in contact with the gate dielectric layer of each gate structure**.




Anderson-Lin composite figure

**(5) Claim 31**

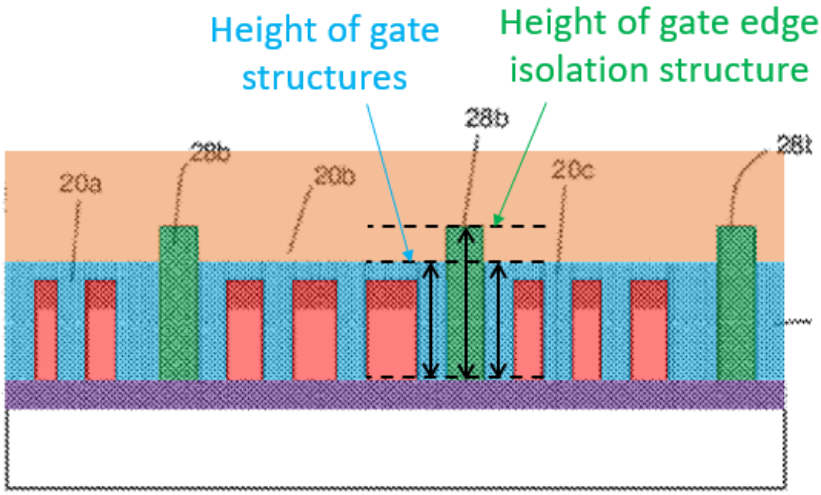
**[31] The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.**

170. The Anderson-Lin combination renders obvious [31]. For instance, in the Anderson-Lin combination structure, Anderson describes that the gate dielectric layers of the first and second gate structures (*e.g.*, Anderson's gate stacks 20; *see* [26d]-[26e]) include **a high-k dielectric material**. *See* SAMSUNG-1006 (Anderson), [0038] ("the gate dielectric can be, for example, ***a high-k dielectric material*** such as silicon oxy nitride"), [0047].

### (6) Claim 32

**[32] The integrated circuit structure of claim 26, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.**

171. The Anderson-Lin combination renders obvious [32]. For instance, as illustrated in the composite figure below, in the Anderson-Lin combination structure, **the gate edge isolation structure** (green) **has a height greater than the height of each of the gate structures** (blue). I have indicated the height of the gate edge isolation structure from its base at the interface with the buried oxide layer. I have also indicated the heights of the gate structures in their tallest alternative, which is from the top surface of the buried oxide layer. (I note that with the inclusion of the STI regions (*see* [26c]), the gate structures would be shorter.) Under either alternative (*i.e.*, measured with or without the STI regions), the height of the gate edge isolation structure is greater than the height of the gate structures.




Anderson-Lin composite figure

172. Moreover, in the combination, Anderson describes "dual height isolation structures 28a and 28b," where "the isolation structure 28b is taller than the surrounding isolation structures 28a." SAMSUNG-1006 (Anderson), [0037], FIG. 14; *see* [0046], FIGS. 23 and 25. To form the gates, "the gate electrode 20 is partially etched away to ***expose the isolation structure 28b***" such that "gates 20a-20d are … separated by the isolation structures 28b." SAMSUNG-1006 (Anderson), [0039]; *see* [0048]. Specifically, Anderson describes a structure "manufactured in accordance with aspects of the present invention" that includes "a gate electrode structure of a height greater than the short fin structure and ***less than the tall fin structure***," consistent with the relative heights of the structures illustrated in Anderson's FIG. 14. SAMSUNG-1006 (Anderson), [0051]; *see also* [0005] ("forming gate electrodes … between each fin of the dual height fin array,

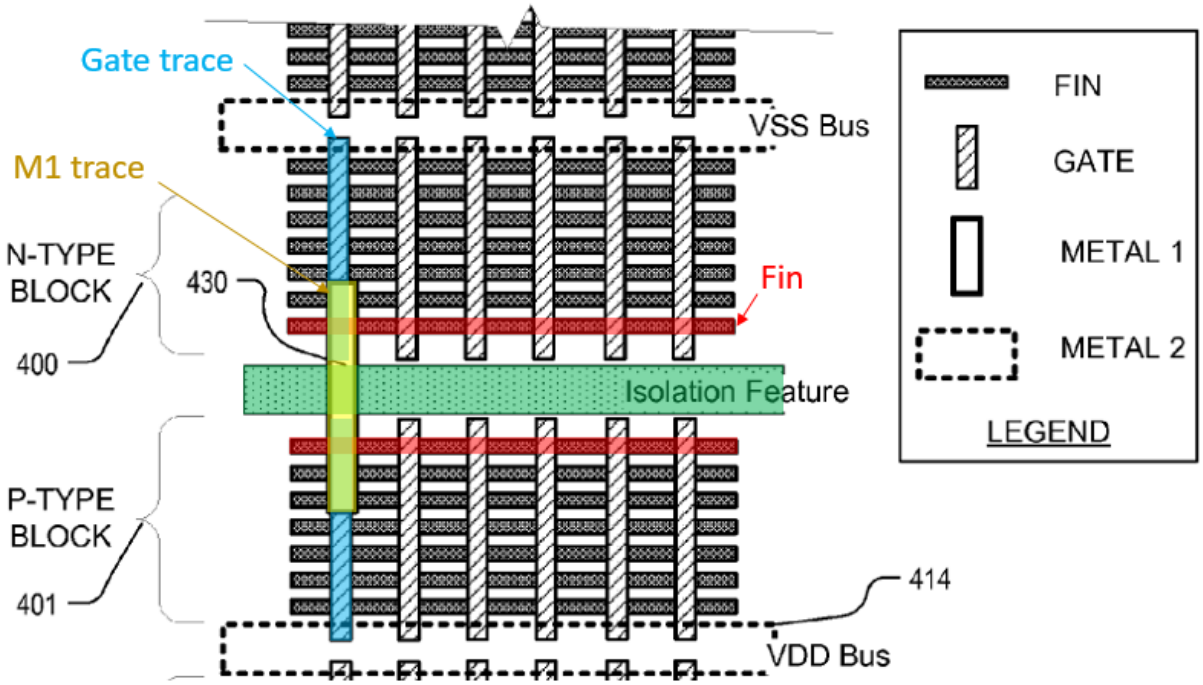
burying the second plurality of fins and abutting sides of the plurality of fins comprising the raised portions"), [0006]-[0007].

### D. [GROUND 3B] – CLAIMS 33-35 ARE OBVIOUS OVER ANDERSON, LIN, AND KAWA

#### 1. Kawa describes local interconnects connecting gates of FinFET transistors

173. Kawa describes "[i]ntegrated circuits including cells comprising finFET blocks." SAMSUNG-1008 (Kawa), [0006]. Kawa's FIGS. 4-5, which I have reproduced below, illustrate "a plurality of finFET blocks in which finFET transistors … can be arranged to implement cells of a flexible finFET cell library." *Id.*, [0049]. FIG. 5 is a cross-sectional view "taken along the gate traces" in a region "spanning between a p-type block and an n-type block" of the top view FIG. 4. *Id.*, [0060]; *see* [0049].

FIG. 4




Excerpt from Kawa, FIG. 4 (annotated)

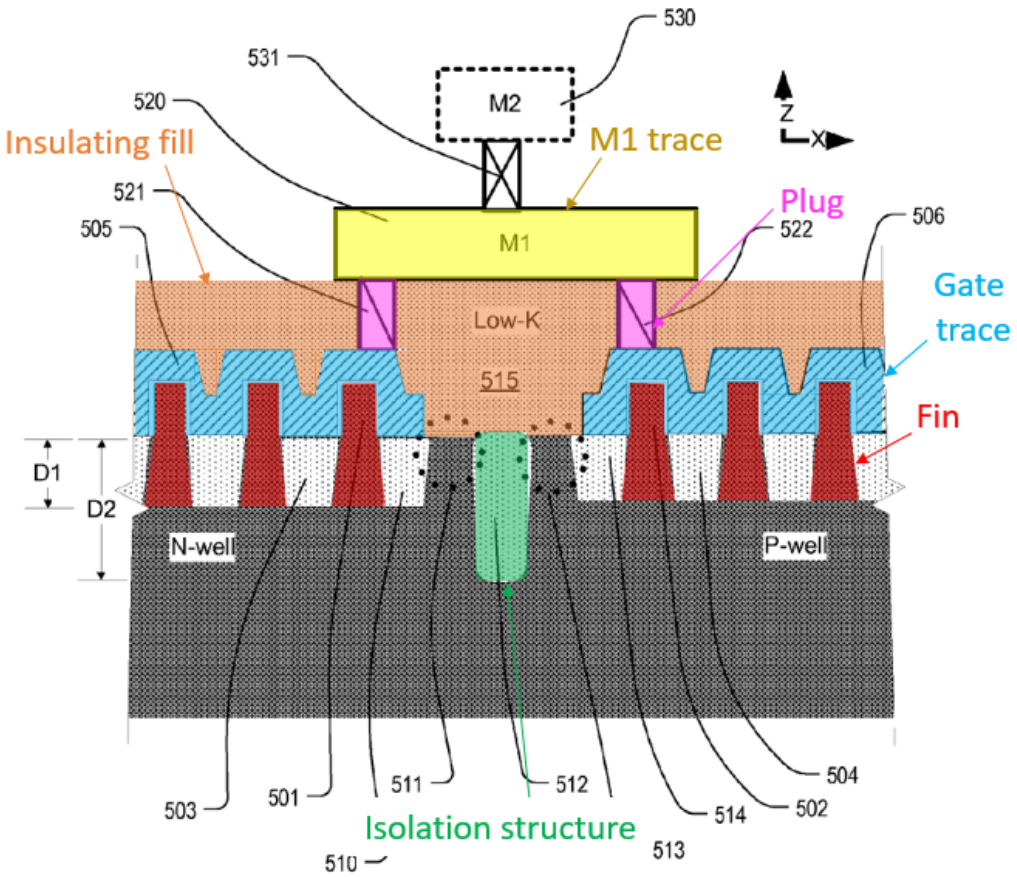



FIG. 5

Excerpt from Kawa, FIG. 5 (annotated)

174. Referring to FIG. 5, each p-type and n-type block includes fins 501, 502 (fins 501, 502; *see also* fins 410, 420 of FIG. 4), which I have highlighted in red. *See* SAMSUNG-1008 (Kawa), [0051]-[0052], [0060]. Each block also includes gate traces 505, 506, highlighted in blue, over and orthogonal to the fins (*see also* gate traces 412, 422 of Fig. 4). *See id.*, [0053]-[0054], [0061]. An insulating isolation structure 512 (*see also* isolation structure 426 of Fig. 4),

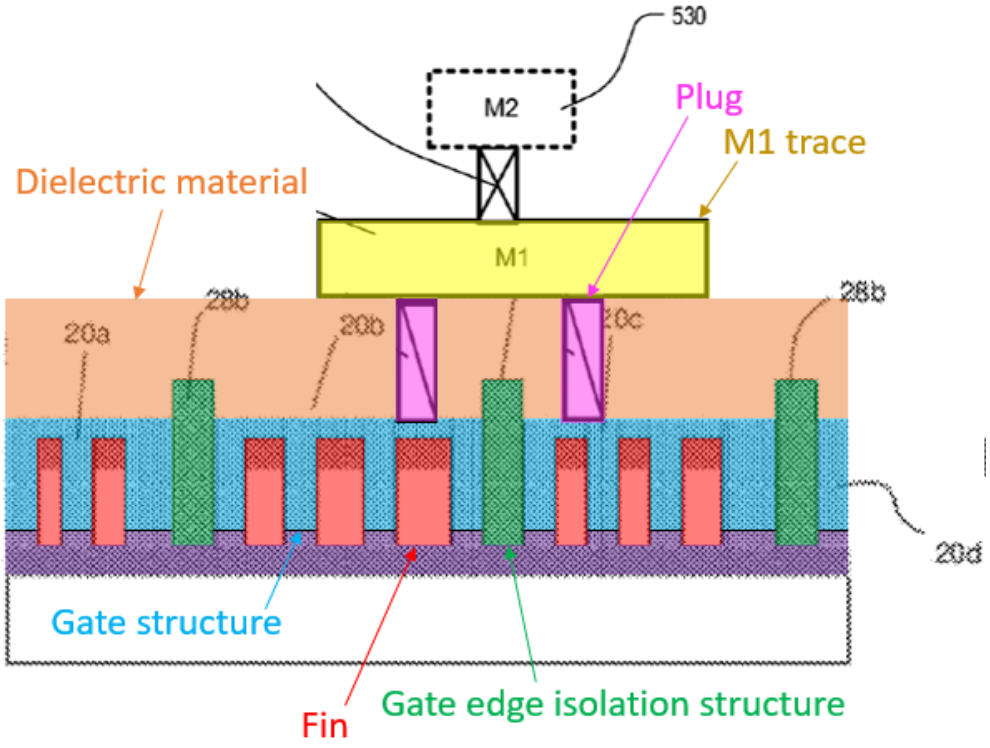
highlighted in green, is disposed between blocks. *See id.*, [0050], [0055], [0061]-[0064], [0067], [0055].

175. An "insulating fill 515," highlighted in orange, "provides an interlayer insulator layer between the patterned gate conductor layer including the gate traces 505 and 506, and overlying patterned conductor layers." SAMSUNG-1008 (Kawa), [0068]. For instance, the insulating fill 515 can be considered as corresponding to the ILD of the Anderson-Lin combination. These overlying layers include a "patterned conductor layer M1"(*e.g.*, M1 trace 520 in Fig. 5, M1 trace 430 in Fig. 4), highlighted in yellow. The M1 trace connects gate traces in different blocks, *e.g.*, gate traces 505, 506, "passing over the isolation structure." *Id.*, [0057]; *see* [0068]. For instance, "plugs 521 and 522," pink, "extend through vias in the insulating fill 515 to connect gate traces 505 and 506, respectively," to the M1 trace. *Id.*, [0068]; *see* [0057], Fig. 4 (showing M1 trace 430).

**2. The Anderson-Lin-Kawa combination**

176. In the Anderson-Lin-Kawa combination, Anderson describes that "contacts can be connected to the source/drain and gate electrodes using conventional etching and metal deposition processes." SAMSUNG-1006 (Anderson), [0050]. In the combination, these connections are implemented based on the teachings of Kawa, as shown in the composite figure *infra*. For instance, the Anderson-Lin-Kawa combination includes a patterned Metal-1 (M1) trace

(highlighted in yellow) that "overlie[s] the patterned gate conductor layer" (blue) and is "arranged parallel to the gate traces in the patterned gate conductor layer." SAMSUNG-1008 (Kawa), [0057]; *see* [0068]. For instance, the M1 trace in the combination is arranged to connect the first and second gate structures, and "passing over" the isolation structure (green). SAMSUNG-1008 (Kawa), [0057]; *see* [0068]. "Inter-layer connectors, such as plugs" (pink), "extend through vias" in the inter-layer dielectric of the combination (orange) to connect the first and second gate structures to the M1 trace and thus to one another. SAMSUNG-1008 (Kawa), [0068]; *see* [0057].




Anderson-Lin-Kawa composite figure

### 3. Reasons to combine Anderson, Lin, and Kawa

177. It is my opinion that a POSITA would have been motivated to incorporate local interconnects and gate contact plugs into the Anderson-Lin-Kawa integrated circuit structure for at least the following reasons.

178. One reason why a POSITA would have been motivated to incorporate local interconnects and plugs into the Anderson-Lin integrated circuit structure is because doing so would enable electrical connections to be formed to the gate structures of the FinFET transistors of the Anderson-Lin integrated circuit structure, allowing the creation of circuits including those transistors. See SAMSUNG-1006 (Anderson), [0050] ("contacts can be connected to the source/drain and gate electrodes using conventional etching and metal deposition processes"); SAMSUNG-1020 (Anderson-841), 9:61-10:3 ("Standard processing follows, which includes formation of metallic contacts and metallization for the M1-level local interconnect wiring, and formation of dielectric layers, conductive vias, and metallization for upper level (M2-level, M3-level, etc.) interconnect wiring coupled with the contacts 70, 72"); SAMSUNG-1021, [0027]-[0030] ("FIG. 2C illustrates the formation of local interconnect trenches 207, as by etching. … Once the gate hard mask is etched, the local interconnect trenches 207 are filled with a conductive material, such as tungsten."); SAMSUNG-1022, 3:39-4:12

("narrow metal lines 206 are used as a local interconnect above the active area 202"); SAMSUNG-1023, [0127].

179. Another reason why a POSITA would have been motivated specifically to incorporate M1 traces "arranged parallel to the gate traces in the patterned gate conductor layer," *e.g.*, as taught by Kawa, is because this arrangement "facilitates the use of the first patterned conductor layer for interconnecting gate traces and source/drain regions along columns in the adjacent blocks." SAMSUNG-1008 (Kawa), [0057]; *see* [0097]. In particular, it is my opinion that a POSITA would have recognized that this configuration provides design flexibility in allowing for interconnection of, among other elements, "traces in the gate conductor layer [and] traces in the first patterned gate conductor layer" "in any desired pattern." SAMSUNG-1008 (Kawa), [0058]; *see* [0098]. For instance, I believe a POSITA would have been motivated to pursue this arrangement to achieve advantages afforded by this design flexibility, *e.g.*, "implementing engineering change orders for size changes, or other modifications, during design verification processes during integrated circuit design and manufacturing." SAMSUNG-1008 (Kawa), [0113]; *see* [0108], [0110]-[0111].

180. Additionally, a POSITA would have been motivated to incorporate M1 traces, *e.g.*, in the arrangement described by Kawa, because this architecture advantageously "allows for very dense area utilization with flexible layout

strategies," *e.g.*, enabling the resulting integrated circuit structures for "multiple bit flip-flops and sequential elements," or "for implementation of gate arrays, field programmable gate arrays, 'sea of gates' architectures and other high density and/or high performance integrated circuit structures." SAMSUNG-1008 (Kawa), [0112].

181. It is also my opinion that a POSITA would have been motivated to incorporate M1 traces into the combination because this is just the implementation of known techniques (*e.g.*, interconnects and plugs in a FinFET-based integrated circuit device) to a known structure (*e.g.*, the Anderson-Lin integrated circuit structure) resulting in a predictable outcome (*e.g.*, a FinFET-based integrated circuit in which gates are electrically connected by interconnects and plugs).

182. Furthermore, it is my opinion that a POSITA would have expected success in pursuing this implementation because the incorporation of local interconnects and contacts is consistent with Anderson's teachings that "contacts can be connected to the source/drain and gate electrodes using conventional etching and metal deposition processes." SAMSUNG-1006 (Anderson), [0050]. I also believe that a POSITA also would have expected success given that local interconnects and contacts were well-known elements of FinFET-based integrated circuits as of the Critical Date. *See* SAMSUNG-1020, 9:61-10:3; SAMSUNG-1021, [0027]-[0030]; SAMSUNG-1022, 3:39-4:12; SAMSUNG-1023, [0127].

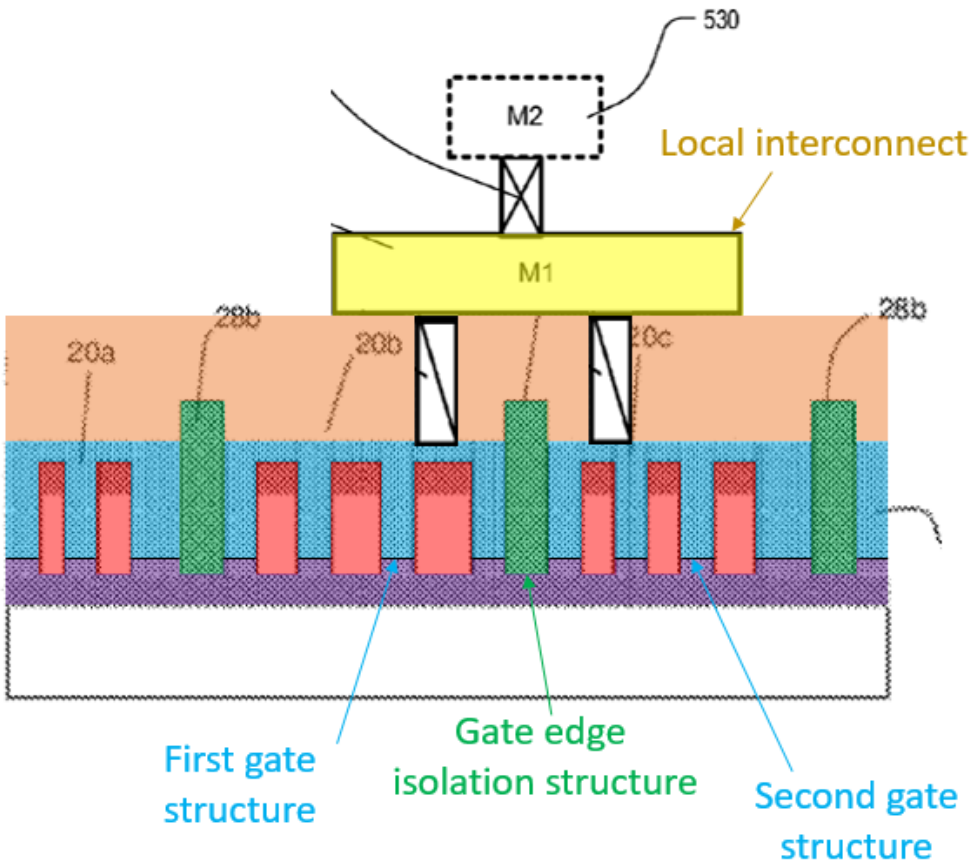
### 4. Analysis

#### (1) Claim 33

**[33] The integrated circuit structure of claim 32, further comprising: a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.**

*The Anderson-Lin-Kawa combination includes a local interconnect*

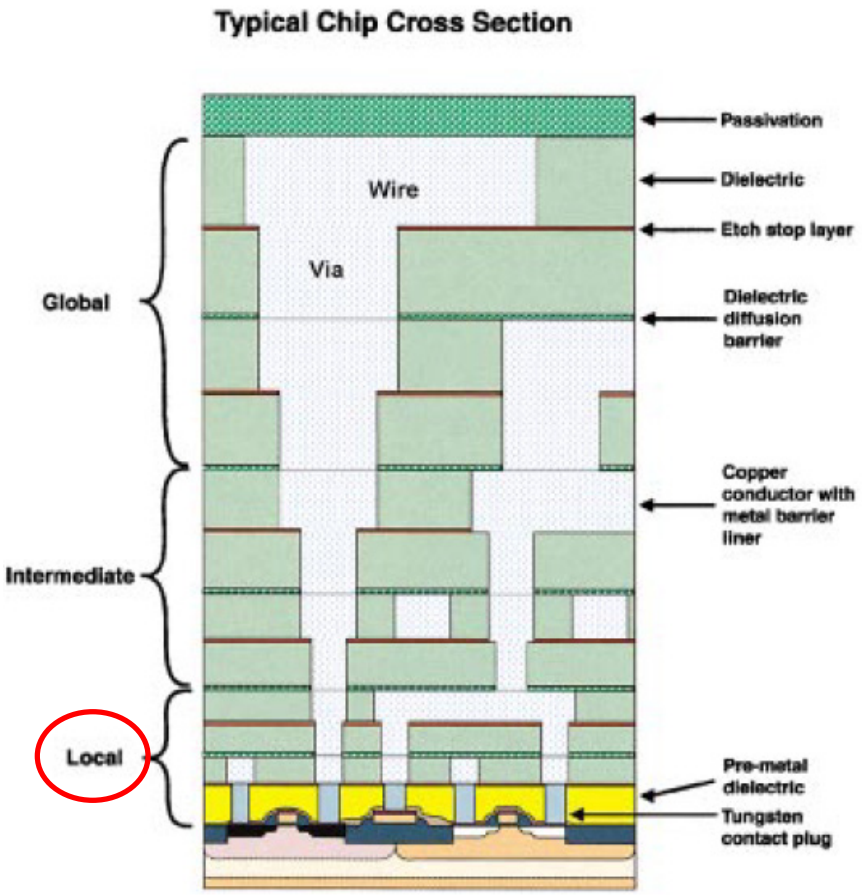
183. The Anderson-Lin-Kawa combination renders obvious [33]. For instance, the Anderson-Lin-Kawa combination structure includes **a local interconnect**, *e.g.*, based on Kawa's ***M1 trace*** (*e.g.*, M1 trace 520 in Kawa's FIG. 5, M1 trace 430 in FIG. 4), which I have highlighted in yellow in the composite figure below. *See* SAMSUNG-1008 (Kawa), [0057] ("The trace 430 is ***an inter-block trace*** arranged to connect a gate trace in block 400 to a gate trace in block 401"), [0068] ("Connections between gate traces in adjacent blocks can be implemented using ***the first patterned conductor layer M1 by forming trace 520***"), [0073] ("connect ***the traces in the first patterned conductor layer*** to gate traces"), [0074] ("trace 722 in the first patterned conductor layer … is connected to gate traces 720 and 721 in the p-type and n-type blocks"), [0073]-[0078], [0081], [0097]-[0098], FIGS. 4-5, FIGS. 7-11.




Anderson-Lin-Kawa composite figure

184. In the combination, Kawa's M1 trace is an **interconnect** in that it electrically connects different gate structures, *e.g.*, the first and second gate structures (blue). *See* SAMSUNG-1008 (Kawa), [0057] ("This facilitates the use of the first patterned conductor layer for interconnecting gate traces and source/drain regions … The trace 430 is an inter-block trace arranged to ***connect a gate trace in block 400 to a gate trace in block 401***"), [0068] ("***Connections between gate traces in adjacent blocks*** can be implemented using the first patterned conductor layer M1 by forming trace 520").

185. Moreover, Kawa's M1 trace is **a local interconnect** in the combination because it is an M1-level interconnect that connects gate structures over a short distance. Indeed, I note that it was well-known in the art as of the Critical Date for local interconnects to be on the M1-level of an integrated circuit. *See* SAMSUNG-1018 (Havemann), FIG. 6 (below); SAMSUNG-1019 (James), FIG. 2 (illustrating FinFET transistors and a "lower metal stack" including a "local interconnect layer," *id.*, p. 2); SAMSUNG-1006 (Anderson)-841, 9:61-63 ("Standard processing follows, which includes formations of metallic contacts and metallization for ***the M1-level local interconnect wiring***"); SAMSUNG-1021 (Schultz), [0028] ("The resulting local interconnects are self-aligned, which … allows ***the local interconnect horizontal direction to be placed on the metal 1 pitch***"); SAMSUNG-1022 (Herberholtz), 3:52-4:1 ("narrow metal lines 206 are used as a local interconnect … [that] may be formed from one or more metal layers which are close to the substrate, e.g. in metal-1 (the first metal layer)"); SAMSUNG-1023 (Koldiaev), [0127] ("Metal-01 and Metal-02 ***local interconnect layers***").




Excerpt from Havemann, FIG. 6 (annotated)

*The local interconnect in the combination is disposed over the gate structures and the gate edge isolation structure*

186. As shown in the composite figure above, the local interconnect in the combination is **disposed over a portion of the first and second gate structures** (blue). That is, for instance, the local interconnect overlies and is disposed at a higher level than the first and second gate structures. This arrangement is based on Kawa's teachings that the M1 trace overlies portions of the gate traces (*e.g.*, gate traces 412, 422 of Fig. 4, gate traces 505, 506 of Fig. 5). *See* SAMSUNG-1008

(Kawa), [0057] ("a first patterned conductor layer ***(metal 1) includes a plurality of traces … which overlie the patterned gate conductor layer***"), [0068] ("An insulating fill 515 provides an interlayer insulator between the patterned gate conductor layer including the gate traces 505 and 506, and ***overlying patterned conductor layers, including the first patterned conductor layer M1***"), FIGS. 4-5, FIGS. 7-11.

187. That the local interconnect in the combination is disposed over portions of the first and the second gate structures is also made apparent by Kawa's description of the layout of the M1 trace. Kawa describes that its M1 trace is "arranged parallel to the gate traces in the patterned gate conductor layer" and connected to gate traces that are separated by an isolation structure "using vertical conductors sometimes referred to as plugs." SAMSUNG-1008 (Kawa), [0057]-[0058]. For the M1 trace (*e.g.*, the local interconnect in the combination) to be connected to a gate trace (*e.g.*, the first or second gate structure in the combination) using a ***vertical*** conductor means that the local interconnect both is located at a higher level and is vertically overlies the gate trace, *i.e.*, the local interconnect **is disposed over** a portion of each gate structure.

188. As shown in the composite figure above, the local interconnect in the combination also is disposed **over a portion of the gate edge isolation structure** (green), *e.g.*, the local interconnect overlies and is disposed at a higher level than

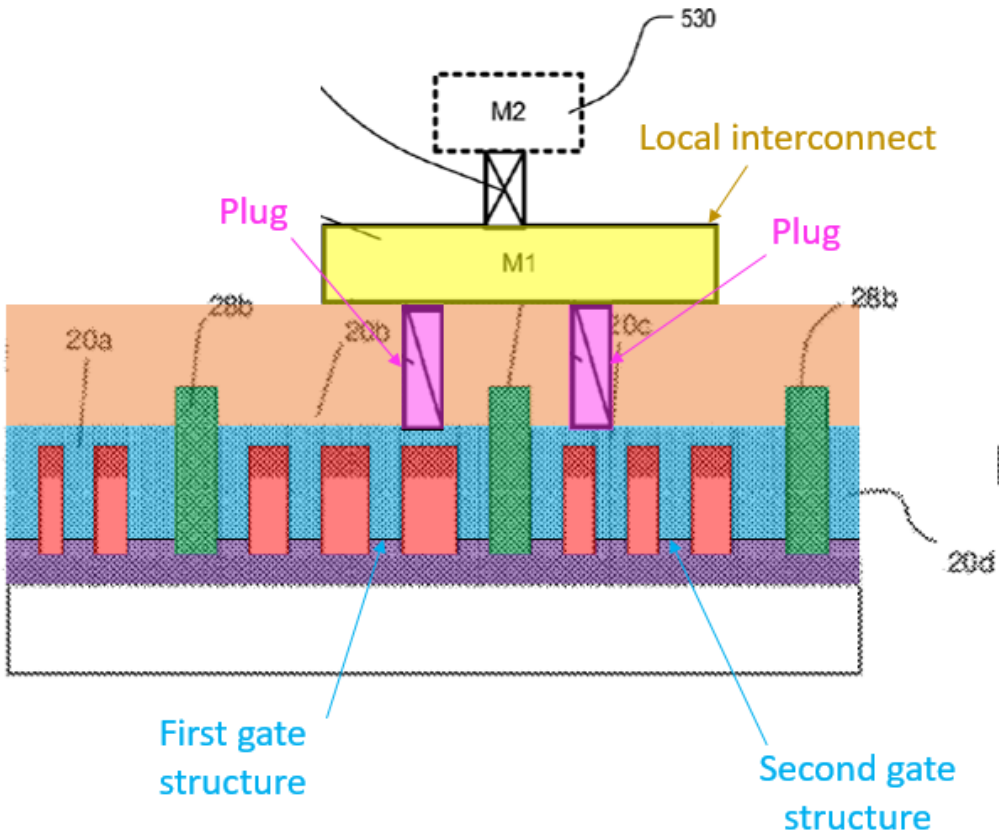
the gate edge isolation structure. This arrangement is based on Kawa's teachings that the M1 trace overlies an isolation structure between the gate traces (*e.g.*, isolation structure 426 of Fig. 4, isolation structure 512 of Fig. 5). *See* SAMSUNG-1008 (Kawa), [0057] ("The trace 430 is an inter-block trace … ***passing over the isolation structure***"), FIGS. 4-5, FIGS. 7-11.

**(2) Claim 34**

**[34] The integrated circuit structure of claim 33, wherein the local interconnect electrically couples the first gate structure to the second gate structure.**

189. The Anderson-Lin-Kawa combination renders obvious [34]. For instance, in the Anderson-Lin-Kawa combination structure, **the local interconnect** (*e.g.*, the M1 trace, highlighted in yellow in the composite figure below) **electrically couples the first gate structure to the second gate structure** (blue), *e.g.*, through plugs (pink), based on the teachings of Kawa. *See* SAMSUNG-1008 (Kawa), [0058] ("traces in the gate conductor layer [and] traces in the first patterned conductor layer … can be interconnected in any desired pattern using vertical conductors sometimes referred to as plugs in vias through interlayer insulators"), [0068] ("***Connections between gate traces*** in adjacent blocks ***can be implemented using the first patterned conductor layer M1*** by forming trace 520 … Interlayer connectors, such as plugs 521 and 522 extend through vias in the insulating fill 515 to connect gate traces 505 and 506, respectively, to the trace

520"), [0067] ("the connection of the gate traces 505 and 506 … is made using patterned metal layer"), [0057] ("The trace 430 is an inter-block trace arranged to connect a gate trace in block 400 to a gate trace in block 401"), claim 1 ("a plurality of inter-layer connectors that connect … gate traces [and] traces in the at least one patterned conductor layer"), [0073]-[0074], [0077]-[0078], [0081], [0097]-[0098].

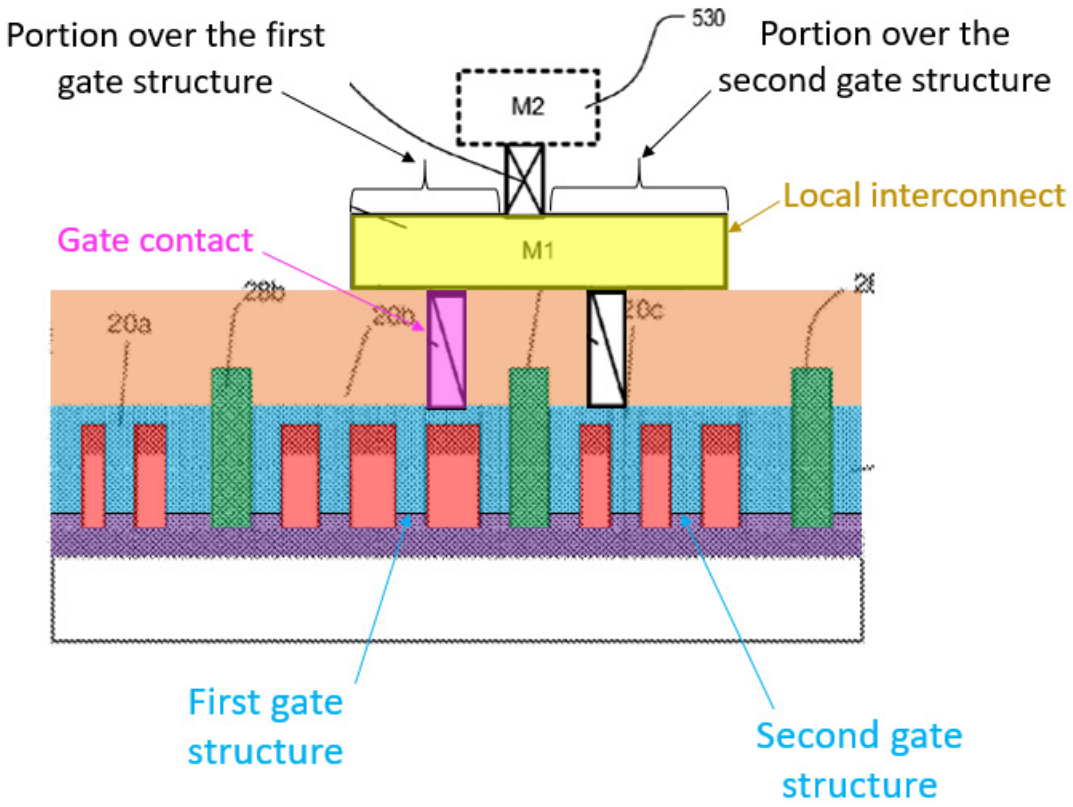



Anderson-Lin-Kawa composite figure

### (3) Claim 35

**[35] The integrated circuit structure of claim 33, further comprising: a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.**

190. The Anderson-Lin-Kawa combination renders obvious [35]. For instance, the Anderson-Lin-Kawa combination structure includes **a gate contact**, *e.g.*, based on Kawa's plug 521 (highlighted in pink in the composite figure below). Kawa's plug is **a gate contact** in the combination because it acts as a contact (*e.g.*, provides an electrical connection) between the local interconnect and the first gate structure: "***Interlayer connectors, such as plugs 521*** and 522 extend through vias in the insulating fill 515 to ***connect gate traces 505 and 506, respectively, to the trace 520***." SAMSUNG-1008 (Kawa), [0068]; *see* [0058] ("traces in the gate conductor layer [and] traces in the first patterned conductor layer … can be interconnected … using vertical conductors sometimes referred to as plugs in vias through interlayer insulators"), [0073]-[0074], [0077]-[0078], [0081], [0097]-[0098], FIGS. 4-5, FIGS. 7-11.




Anderson-Lin-Kawa composite figure

191. As I have illustrated in the composite figure, the gate contact in the combination (*e.g.*, Kawa's plug) is **on** (*e.g.*, in contact with) **a portion of the local interconnect over the first gate structure, but not on** (*e.g.*, not in contact with) **a portion of the local interconnect over the second gate structure**. For instance, it is my opinion that a POSITA would find it obvious that the location where a contact is placed is simply according to the mask pattern at the contact level (or plug level), and the contact mask pattern (as well as patterns for any mask) is implemented according to the circuit design. This positioning arises from the

nature of Kawa's plugs as "vertical conductors." SAMSUNG-1008 (Kawa), [0058]. A vertical conductor connecting the first gate structure to the overlying local interconnect extends vertically between the first gate structure and the portion of the local interconnect that is positioned directly above the first gate structure, but does not extend diagonally (*e.g.*, does not extend to the portion of the local interconnect that is positioned directly above the second gate structure).

## VI. LEGAL PRINCIPLES

### A. Anticipation

192. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates.

193. I have been informed by counsel that a claim is invalid under 35 U.S.C. § 102(a)(1) if the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(a)(2) if the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the

case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

**B. Obviousness**

194. I have been informed that a patent claim is invalid as "obvious" under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a POSITA, taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called "secondary considerations" of non-obviousness, which include: (i) "long felt need" for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) "copying" of the claimed invention by others.

195. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason to modify the single prior art reference, or combine two or more references, in order to achieve the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves, the knowledge or "common sense" of one skilled in the art, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the combination of

familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

## VII. ADDITIONAL REMARKS

196. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

197. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code.

Dated: 1/19/2023 By: _____

# APPENDIX A

# DAVID KUAN-YU LIU, Ph.D.

42063 Benbow Drive, Fremont, CA 94539 ● (510) 770-9449 or (510) 579-5029
www.davidkyliu.com davidkyliu@comcast.net


## PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 12 years of experience serving as expert consultant.
    - Named inventor on 99 US patents.
- Consultant and expert witness for past 15 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

## EDUCATION

**Stanford University, Palo Alto, California**

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

**University of California, Berkeley, California**

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

## KEY EXPERT WORK EXPERIENCE:

| | |
|---|---|
| **Case:** | **Netlist, Inc. vs. *Samsung Electronics Co. Ltd. et al.,*** |
| Jurisdiction: | Civil Action No. 2:21-cv-00463<br>Eastern District of Texas |
| Work Product: | Expert relating to memory modules. |
| Nature of Case: | Civil action. |
| Counsel: | Retained by Fish & Richardson (Contact: Tony Nguyen) |
| Date: | 8/22 – Current |

| | |
|---|---|
| **Case:** | **Vervain, LLC vs. *Micron Technology &* related IPR Petition** |
| Jurisdiction: | Action No. 6:21-cv-00487-ADA<br>Western District of Texas |
| Work Product: | Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents, all 4 petitions instituted, and deposed on both initial declaration and reply declaration. |
| Counsel: | Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared Bobrow) |
| Date: | 8/21 – Current |

| | |
|---|---|
| **Case:** | **Monterey Research vs. *Qualcomm* PTAB Matter** |
| Work Product: | Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration. |
| Counsel: | Retained by Jones Day (Contact: David Cochran) |
| Date: | 12/21 – Current |

| | |
|---|---|
| **Case:** | ***Semiconductor Energy Laboratory Co.,* OLED Patent Matters** |
| Jurisdiction: | Action No. 8:21-cv-00554-JAK-ADS<br>Central District of California |
| Work Product: | Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review. |
| Nature of Case: | Civil action. |
| Counsel: | Retained by Fish & Richardson (Contact: Bryan Basso) |
| Date: | 9/21 – 4/22 |

| | |
|---|---|
| **Case:** | ***Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505*** |
| Work Product: | Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration. |
| Counsel: | Retained by Erise IP (Contact: Paul Hart) |
| Date: | 8/21 – 9/21 |

| | |
|---|---|
| **Case:** | ***Texas Instruments IPR Petition*** |
| Work Product: | Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration. |
| Counsel: | Retained by Fish & Richardson (Contact: Josh Griswold) |
| Date: | 9/20 – 4/21 |

| | |
|---|---|
| **Case:** | ***Micron Technology* vs. UMC/JinHua** |
| Jurisdiction: | Case No. 4:17-CV-06932-MMC<br>United States District Court for the Northern District of California |
| Work Product: | Testifying expert, trade secret documents review, and declaration submission. |
| Nature of Case: | Trade secret contention of Micron confidential documents. |
| Counsel: | Retained by Jones Day (Contact: Randy Kay) |
| Date: | 3/17 – Current |

| | |
|---|---|
| **Case:** | ***SK Hynix* vs. BitMicro** |
| Jurisdiction: | Investigation No. 337-TA-1097<br>United States International Trade Commission |
| Work Product: | Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, deposition taken, issued witness statement. |
| Nature of Case: | ITC infringement case concerning module stacking of SDRAM. |
| Counsel: | Retained by Fish Richardson (Contact: Joseph Colaianni) |
| Date: | 11/18 – 4/19 |

| | |
|---|---|
| **Case:** | ***Rohm Company IPR Petition*** |
| Work Product: | Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration. |
| Counsel: | Retained by Fish & Richardson (Contact: Matt Colvin) |
| Date: | 4/18 – 8/18 |

| | |
|---|---|
| **Case:** | ***Apple Inc.,* vs. Qualcomm Incorporated** |
| Jurisdiction: | Case No. 3:17-CV-02402<br>United States District Court for the Southern District of California |
| Work Product: | Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, 2 depositions taken. |
| Counsel: | Fish & Richardson (Contact: Tony Nguyen) |
| Date: | 1/18 – 5/19 |

| | |
|---|---|
| **Case:** | ***Macronix* vs. Toshiba** |
| Jurisdiction: | Investigation No. 337-TA-1046<br>United States International Trade Commission |
| Work Product: | Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, deposition taken for 2 patents, issued witness statement and rebuttal witness statement, testified in ITC court on both infringement and invalidity. |
| Nature of Case: | ITC infringement case concerning advanced NAND Flash memory. |
| Counsel: | Retained by Fish Richardson (Contact: David Barken) |
| Date: | 4/17 – 10/18 |

| | |
|---|---|
| **Case:** | ***Novatek Microelecronics Corp. IPR Petition*** |
| Work Product: | Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration. |
| Counsel: | Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov) |
| Date: | 2/17 – 4/17 |

| | |
|---|---|
| **Case:** | ***Taiwan Semiconductor Manufacturing Company IPR Petition*** |
| Work Product: | Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration. |
| Counsel: | Retained by Fish & Richardson (Contact: John Goetz) |
| Date: | 7/15 – 4/17 |

| | |
|---|---|
| **Case:** | **Triune Systems, LLC vs. *Wayne Chen, et al.,*** |
| Jurisdiction: | Case No. 296-03209-2013,<br>District Court of Collin County, TX |
| Work Product: | Testifying expert, database viewing, expert report, video-taped testimony |
| Nature of Case: | Defending against trade secret contention. |
| Counsel: | Retained by Gordon & Rees LLP (Contact: Robert Bragalone) |
| Date: | 5/15 – 9/15 |

| | |
|---|---|
| **Case:** | ***Macronix* vs. Spansion** |
| Jurisdiction: | Investigation No. 337-TA-922<br>United States International Trade Commission |
| Work Product: | Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report. |
| Nature of Case: | ITC infringement case concerning Flash memory cell |
| Counsel: | Retained by Fish Richardson (Contact: David Barken) |
| Date: | 9/14 – 1/15 |

| | |
|---|---|
| **Case:** | ***Macronix* vs. Spansion** |
| Jurisdiction: | Investigation No. 337-TA-909<br>United States International Trade Commission |
| Work Product: | Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report. |
| Nature of Case: | ITC infringement case concerning Flash memory cell |
| Counsel: | Retained by Winston & Strawn (Contact Michael Murray) |
| Date: | 5/14 – 1/15 |

| | |
|---|---|
| **Case:** | ***Keranos, LLC* v. Analog Devices et. al.** |
| Jurisdiction: | Civil Case No. 2:10-CV-00207<br>United States District Court for the Eastern District of Texas |
| Work Product: | Claim Chart Generation and Claim Construction |
| Nature of Case: | Patent infringement case concerning split gate Flash memory cell |
| Counsel: | Retained by Agility IP (Contact Michelle Breit) |
| Date: | 2/09 – 2/14 |

| | |
|---|---|
| **Case:** | **Silicon Storage Technology, Inc. v. *Xicor, LLC*** |
| Jurisdiction: | Civil Case No. CV 10-01515<br>United States District Court for the Northern District of California |
| Work Product: | Expert report and declarations |
| Nature of Case: | Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell. |
| Counsel: | Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy) |
| Date: | 6/11 – 10/11 |

| | |
|---|---|
| **Case:** | ***Fast Memory Erase, LLC* v. Spansion et.al.** |
| Jurisdiction: | Civil Case No. 3:10CV-481<br>United States District Court for the Northern District of Texas |
| Work Product: | Declarations |
| Nature of Case: | Defending Motion for Attorney Fees. |
| Counsel: | Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy) |
| Date: | 2/10 – 6/10 |

| | |
|---|---|
| **Case:** | ***Fast Memory Erase, LLC* v. Spansion et.al.** |
| Jurisdiction: | Civil Case No. 3-08cv0977M<br>United States District Court for the Northern District of Texas |
| Work Product: | Testifying expert: issuing expert report, declarations, and deposition taken. |
| Nature of Case: | Patent infringement case concerning minimizing source current during erase of Flash memory cell. |
| Counsel: | Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy) |
| Date: | 2/09 – 5/10 |

**EXPERIENCE:**

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 6 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35μm and 0.18μm CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**

Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**

Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00 **Programmable Silicon Solutions, Sunnyvale, California**
Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98 **AMIC Technology, Santa Clara, California**
Director of Flash Technology. Responsible for developing 0.35μm ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97 **Altera Corp., San Jose, California**
Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35μm generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96 **Information Storage Devices, San Jose, California**
Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95 **Advanced Micro Devices, Sunnyvale, California**
Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5μm and 0.35μm flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92 **Texas Instruments, Dallas, Texas**

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

**AWARDS/HONORS**

U.C. Berkeley Certificate of Distinction Award, 1983
AEA Faculty Development Fellowship, 1983-1985
AMD Spotlight Award, 1995

**PATENTS**

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K-L. Chen and H. Tigelaar), issued April 21, 1992.

2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.

3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.

4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.

5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.

6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.

7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.

8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.

9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994

10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.

11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.

12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.

13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.

14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.

15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.

16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.

17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.

18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.

19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.

20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.

21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.

22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.

23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.

24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.

25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997

26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.

27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.

28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.

29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998

30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.

31. U.S. Patent 5,814,854, "Highly scalable FLASH EEPROM cell," Issued September 29, 1998.

32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.

33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.

34. U.S. Patent 5,930,174, "Circuit and Method for Erasing Flash Memory Array," Issued July 27, 1999.

35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.

36. U.S. Patent 5,995,418, "Circuit and Method for Erasing Flash Memory Array," Issued November 30, 1999.

37. U.S. Patent 6,026,017, "Compact nonvolatile memory," Issued February 15, 2000.

38. U.S. Patent 6,027,974, "Nonvolatile memory," Issued February 22, 2000.

39. U.S. Patent 6,088,263, "Non-volatile memory using substrate electrons," Issued July 11, 2000.

40. U.S. Patent 6,091,636, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued July 18, 2000.

41. U.S. Patent 6,127,225, "Memory cell having implanted region formed between select and sense transistors," Issued October 3, 2000.

42. U.S. Patent 6,159,800, "Method of forming memory cell," Issued December 12, 2000.

43. U.S. Patent 6,188,604, "Flash memory cell & array with improved pre-program and erase characteristics," Issued February 13, 2001.

44. U.S. Patent 6,185,133, "Flash EPROM using junction hot hole injection for erase," Issued February 6, 2001.

45. U.S. Patent 6,252,799, "Device with embedded Flash and EERPOM memories," Issued June 26, 2001.

46. U.S. Patent 6,326,265, "Device with Embedded Flash and EPROM Memories," Issued December 4, 2001.

47. U.S. Patent 6,417,550, "High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage," Issued July 9, 2002.

48. U.S. Patent 6,479,862, "Charge trapping device and method for implementing a transistor having a negative differential resistance mode," Issued November 12, 2002.

49. U.S. Patent 6,512,274, "CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same," Issued January 28, 2003.

50. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device," Issued July 22, 2003.

51. U.S. Patent 6,624,026, "Nonvolatile Memory," Issued September 23, 2003.

52. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process," Issued January 20, 2004.

53. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same," Issued February 3, 2004.

54. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR) characteristic," Issued February 17, 2004.

55. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold," Issued March 2, 2004.

56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.

57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.

58. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same," Issued November 29, 2005.

59. U.S. Patent 6,972,234, "High Voltage MOS Devices with High Gated-Diode Breakdown Voltage and Punch-through Voltage," Issued December 6, 2005.

60. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same," Issued December 6, 2005.

61. U.S. Patent 7,067,873, "Charge Trapping Device," Issued June 27, 2006.

62. U.S. Patent 7,091,077, "Method of directionally trimming polysilicon width," Issued August 15, 2006.

63. U.S. Patent 7,109,078, "CMOS compatible process for making a charge trapping device," Issued September 19, 2006.

64. U.S. Patent 7,301,194, "Shrinkable and highly coupled double poly EEPROM with Inverter," Issued November 27, 2007.

65. U.S. Patent 7,436,710, "EEPROM memory device with cell having NMOS in a P pocket as a control gate, PMOS program/erase transistor, and PMOS access transistor in a common well," Issued October 14, 2008.

66. U.S. Patent 7,535,758, "One or Multiple-Times Programming Device," Issued May 19, 2009.

67. U.S. Patent 7,782,668, "Integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 24, 2010.

68. U.S. Patent 7,787,295, "Integrated circuit embedded with Non-volatile Multiple-Time Programmable memory having variable coupling," Issued August 31, 2010.

69. U.S. Patent 7,787,304, "Method of making integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 31, 2010

70. U.S. Patent 7,787,309, "Method of operating integrated circuit embedded with Non-volatile One-Time Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.

71. U.S. Patent 7,791,955, "Method of erasing a block of memory cells," Issued September 7, 2010.

72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010

73. U.S. Patent 7,835,186, "Method of programming a selected memory cell," Issued November 16, 2010.

74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010

75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011

76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011

77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011

78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012

79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012

80. U.S. Patent 8,300,470, "Two Terminal Programmable Hot Channel Electron Non-Volatile Memory," Issued October 30, 2012

81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012

82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.

83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.

84. U.S. Patent 8,582,342, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued November 12, 2013.

85. U.S. Patent 8,599,612, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Related Application data," Issued December 3, 2013.

86. U.S. Patent 8,705,263, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued April 22, 2014.

87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.

88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.

89. U.S. Patent 9,224,739, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued December 29, 2015.

90. U.S. Patent 9,305,931, "Zero Cost NVM Cell Using High Voltage Devices in Analog Process," Issued April 5, 2016.

91. U.S. Patent 9,324,438, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued April 26, 2016.

92. U.S. Patent 9,558,813, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued January 31, 2017.

93. U.S. Patent 9,570,161, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.

94. U.S. Patent 9,570,175, "Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.

95. U.S. Patent 10,061,738, "Ephemeral Peripheral Device," Issued August 28, 2018.

96. U.S. Patent 10,115,467, "One time Accessible (OTA) Non-Volatile Memory," Issued October 30, 2018.

97. U.S. Patent 10,198,889, "Automatic Valid Vote Count Storage Using Secure Embedded Non-Volatile Memory," Issued February 5, 2019

98. U.S. Patent 10,559,700, "Zero Cost ANVM Cell Using High Voltage Devices in Analog Process," Issued February 11, 2020.

99. U.S. Patent 10,629,607, "Semiconductor CMOS Non-Volatile Memory Device," Issued April 21, 2020

**(additional patent applications pending)**

**PUBLICATIONS**


1. S.D. Leeke, D. K. Y. Liu and J. P. McVittie, "Plasma mode trench etching with direct hydrocarbon injection," *Materials Research Society Symposium Proceedings*, Vol. 68, pp. 21-27, 1986.
2. D. K. Y. Liu and J. D. Plummer, "A novel trench-injector power device with low ON-resistance and high switching speed," *IEEE Electron Device Letters*, Vol. 9, No. 7, pp. 321-323, 1988.
3. D. M. Boisvert, D. K. Y. Liu and J. D. Plummer, "Circuit approaches to increasing IGBT switching speed," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1276-1279, 1988.
4. D. K. Y. Liu and J. D. Plummer, "Device physics and optimization of conductivity-modulated power MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, pp. 2457-2458, 1988.
5. D. K. Y. Liu, K.-L. Chen, H. Tigelaar, J. Paterson and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 12, No. 4, pp. 151-153, 1991.
6. M. Wong, D. K. Y. Liu, M. M. Moslehi and D. W. Reed, "Preoxidation treatment using HCl/HF vapor," *IEEE Electron Device Letters*, Vol. 12, No. 8, pp. 425-426, 1991.
7. D. K. Y. Liu, C. Kaya, M. Wong, J. Paterson and P. Shah, "Optimization of a source-side injection FAMOS cell for flash EPROM applications," *International Electron Devices Meeting Technical Digest*, pp. 315-318, 1991.
8. K.-L. Chen, D. K. Y. Liu, G. Misium, W. M. Gosney, S.-J. Wang, J. Camp and H. Tigelaar, "A sublithographic antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 13, No. 1, pp. 53-55, 1992.
9. K. T. San, C. Kaya, D. K. Y. Liu, T. P. Ma, and P. Shah, "A new technique for determining capacitive coupling coefficients in flash EPROMs," *IEEE Electron Device Letters*, Vol. 13, No. 6, pp. 328-331, 1992.
10. C. Kaya, D. K. Y. Liu, J. Paterson and P. Shah, "Buried source-side injection (BSSI) for flash EPROM programming," *IEEE Electron Device Letters*, Vol. 13, No. 9, pp. 465-467, 1992.
11. M. Wong, D. K. Y. Liu and S. S.-W. Huang, "Analysis of the subthreshold slope and the linear transconductance techniques for the extraction of the capacitance coupling coefficients of floating-gate devices," *IEEE Electron Device Letters*, Vol. 13, No. 11, pp. 566-568, 1992.
12. D. K. Y. Liu and J. D. Plummer, "Design and analysis of a new conductivity-modulated power MOSFET," *IEEE Transactions on Electron Devices*, Vol. 40, No. 2, pp. 428-438, 1993.
13. J. Z. Peng, S. Haddad, H. Fang, C. Chang, S. Longcor, B. Ho, Y. Sun, D. Liu, Y. Tang, J. Hsu, S. Luan, J. Lien, "Flash EPROM endurance simulation using physics-based models," In *International Electron Devices Meeting Technical Digest*, pp. 295-298, 1994.
14. J. Chen, J. Hsu, S. Luan, Y. Tang, D. Liu, S. Haddad, C. Chang, S. Longcor, J. Lien, "Short Channel enhanced degradation during discharge of Flash EEPROM memory Cell," *International Electron Devices Meeting Technical Digest*, pp. 331-334, 1995.

15. V. H. Chan and D. Liu, "An Enhanced Erase Mechanism During Channel Fowler-Nordheim Tunneling in Flash EPROM Memory Devices," *IEEE Electron Devices Letters,* Vol. 20, No. 3, pp. 140-142, 1999.