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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/024,750	03/24/2016	Milton C. WEBB	P60397US

CONFIRMATION NO. 9490

POA ACCEPTANCE LETTER

164
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

OC00000012984781 3

Date Mailed: 11/18/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/11/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sleutchit/

SAMSUNG 1002

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/024,750	03/24/2016	Milton C. WEBB	P60397US

CONFIRMATION NO. 9490

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

POWER OF ATTORNEY NOTICE

OC000000129847715

Date Mailed: 11/18/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/11/2021.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sleutchit/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	15/024,750
Filing Date	December 19, 2013
First Named Inventor	Milton C. Webb
Title	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
Art Unit	2822
Examiner Name	Roy Karl Potter
Attorney Docket Number	D480-012009

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ian D. MacKinnon/	Date (Optional)	November 11, 2021
Name	Ian D. MacKinnon	Registration Number	34,660
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
15/024,750	December 19, 2013

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 00164

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	/Lisa Hopkinson/	Date (Optional)	November 8, 2018
Name	Lisa Hopkinson		
Title	Administrator of Patents		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
15/024,750	**11/11/2021 11:35:56 AM ET**	**P60397US**

Title of Invention

SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

Application Information

APPLICATION TYPE	Utility - U.S. National Stage under 35 USC 371	PATENT #	9831306
CONFIRMATION #	9490	FILED BY	Ian MacKinnon
PATENT CENTER #	60395417	FILING DATE	03/24/2016
CUSTOMER #	31817	FIRST NAMED INVENTOR	Milton C. WEBB
INTL. APPLICATION #	-	INTL. FILING DATE	-
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2021-11-11_POA_D480-012009.pdf	2	Power of Attorney	1218 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2021-11-11_POA_D480-012009.pdf	3C89638D88BFC2F13BF5DEC4C1CDCF9AF69D01A1F1D897C7E9EC61CD4911CB0EEE08DD0CEEF146F9C6307AEEF0846F18855E4AF2F2E29CFCF93B396F9974DBFF

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/024,750	11/28/2017	9831306	P60397US	9490

31817 7590 11/08/2017

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Milton C. WEBB, Aloha, OR;
INTEL CORPORATION, Santa Clara, CA;
Mark BOHR, Aloha, OR;
Tahir GHANI, Portland, OR;
Szuya S. LIAO, Hillsboro, OR;

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

Application Number	15/024,750
Filing Date	March 24, 2016
First Named Inventor	Milton C. Webb, et al.
Group Art Unit	2822
Examiner Name	Potter, Roy Karl
Attorney Docket No: P60397US	

Change(s) applied to document, /J.H./ 11/1/2017

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.K.P/		U.S. 20130214364	08-22-2013	JAGANNATHAN, HEMANTH, ET AT.	
/R.K.P/		U.S. 6,515,319	02-04-2003	~~INFINCON TECHNOLOGIES AG~~	Widmann et al.
/R.K.P/		U.S. 7,781,274	08-24-2010	NAKABAYASHI, YUKIO, ET AL.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
/R.K.P/		JP-2009260221	11-05-2009	TOSHIBA CORP		
/R.K.P/		JP-2004-356472	12-16-2004	RENESAS TECH CORP		
/R.K.P/		JP-2002-530872	09-17-2002	INFINCON TECHNOLOGIES AG		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		Notice of Reasons for Refusal from Japanese Patent Application No. 2016-526912 (Attorney Docket No. P60397JP) mailed July 26 2017, 10 pgs., English translation.	

EXAMINER /ROY K POTTER/ DATE CONSIDERED 10/20/2017

Based on PTO/SB/08A/08 (01) - Substitute Disclosure Statement Form (PTO-1449)

[1] EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [2] Applicant's unique citation designation number (optional) [3] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	Unknown
	Filing Date	December 19, 2013
	First Named Inventor	Webb, M.
	Group Art Unit	0
	Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No: P60397US	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.K.P/		US-2007/0054464	03/08/2007	ZHANG, Guowei	
/R.K.P/		US-2008/0080380	04/03/2008	LEE, Kwang il, et al.	
/R.K.P/		US-20110021027	01/27/2011	JOHNSON, Frank S.	
/R.K.P/		US-2013/0020615	01/24/2013	FAN, Su Chen, et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
/R.K.P/		KR-20050082099	08-2005	CHOI, Jung A., et al.		

Change(s) applied to document, /S.X.R./ 8/8/2017

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/R.K.P/		International Search Report and Written Opinion from PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) Mailed September 26, 2014, 10 pages.	

EXAMINER /ROY K POTTER/ DATE CONSIDERED 06/26/2017

Based on PTO/SB/08A(09-08) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/024,750	03/24/2016	Milton C. WEBB	P60397US	9490

31817 7590 10/25/2017

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
POTTER, ROY KARL	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
10/25/2017	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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U.S. Patent and Trademark Office
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Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
15/024,750	24 March, 2016	WEBB ET AL.	P60397US

		EXAMINER	
SCHWABE, WILLIAMSON & WYATT, P.C. 1211 SW 5th Avenue, Suite 1600 Portland, OR 97204		ROY POTTER	
		ART UNIT	PAPER
		2822	20171023

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

This communicaton is being sent with the considered Information Disclosure Statement of 9/22/17.

/ROY POTTER/
Primary Examiner, Art Unit 2822

PTO-90C (Rev.04-03)

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/024,750
	Filing Date	March 24, 2016
	First Named Inventor	Milton C. Webb, et al.
	Group Art Unit	2822
	Examiner Name	Potter, Roy Karl
Sheet 1 of 1	Attorney Docket No: P60397US	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.K.P/		U.S. 20130214364	08-22-2013	JAGANNATHAN, HEMANTH, ET AT.	
/R.K.P/		U.S. 6,515,319	02-04-2003	INFINCON TECHNOLOGIES AG	
/R.K.P/		U.S. 7,781,274	08-24-2010	NAKABAYASHI, YUKIO, ET AL.	

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/R.K.P/		JP-2004-356472	12-16-2004	RENESAS TECH CORP		
/R.K.P/		JP-2002-530872	09-17-2002	INFINCON TECHNOLOGIES AG		

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		Notice of Reasons for Refusal from Japanese Patent Application No. 2016-526912 (Attorney Docket No. P60397JP) mailed July 26 2017, 10 pgs., English translation.	

EXAMINER /ROY K POTTER/ DATE CONSIDERED 10/20/2017

Based on PTO/SB/08A/08 (01) - Substitute Disclosure Statement Form (PTO-1449)

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/024,750
	Filing Date	March 24, 2016
	First Named Inventor	Milton C. Webb, et al.
	Group Art Unit	2822
	Examiner Name	Potter, Roy Karl
Sheet 1 of 1	Attorney Docket No: P60397US	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		U.S. 20130214364	08-22-2013	JAGANNATHAN, HEMANTH, ET AT.	
		U.S. 6,515,319	02-04-2003	INFINCON TECHNOLOGIES AG	
		U.S. 7,781,274	08-24-2010	NAKABAYASHI, YUKIO, ET AL.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
		JP-2009260221	11-05-2009	TOSHIBA CORP		
		JP-2004-356472	12-16-2004	RENESAS TECH CORP		
		JP-2002-530872	09-17-2002	INFINCON TECHNOLOGIES AG		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Notice of Reasons for Refusal from Japanese Patent Application No. 2016-526912 (Attorney Docket No. P60397JP) mailed July 26 2017, 10 pgs., English translation.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(08-03) - Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

(19)日本国特許庁（ＪＰ）　(12)公表特許公報（Ａ）　(11)特許出願公表番号
特表2002－530872
（P2002－530872A）
(43)公表日　平成14年９月17日(2002.9.17)

(51)Int.Cl.'	識別記号	ＦＩ	ﾃｰﾏｺｰﾄﾞ(参考)
Ｈ０１Ｌ　29/78		Ｈ０１Ｌ　29/78	３０１Ｖ　５Ｆ１４０

審査請求　有　　予備審査請求　有　（全 23 頁）

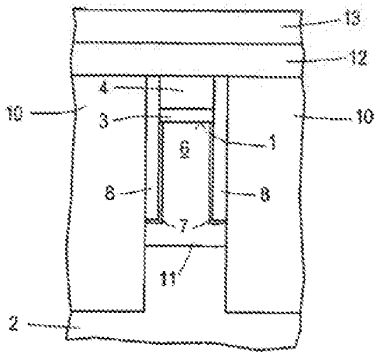
(21)出願番号　特願2000－583092(P2000－583092)
(86)(22)出願日　平成11年11月18日(1999.11.18)
(85)翻訳文提出日　平成13年５月18日(2001.5.18)
(86)国際出願番号　ＰＣＴ／ＤＥ９９／０３６７４
(87)国際公開番号　ＷＯ００／３０１８１
(87)国際公開日　平成12年５月25日(2000.5.25)
(31)優先権主張番号　１９８　５３　２６８．７
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最終頁に続く

(54)【発明の名称】　電界効果制御型トランジスタおよびその製造方法

(57)【要約】
半導体基板（２）に、それぞれ該半導体基板（２）の主表面（１）に接するソース領域、チャネル領域およびドレイン領域を有する活性領域が設けられている。半導体基板（２）の主表面に少なくとも１つのトレンチが設けられており、該トレンチはチャネル領域と接しており、該トレンチにゲート電極（８）の部分が配置されている。有利にはゲート電極は、それぞれチャネル領域に接している２つの互いに対向する部分（８）を有する。トランジスタの製造は、標準的プロセスステップを用いて行われる。



【特許請求の範囲】

【請求項１】　半導体基板（２）に、それぞれ該半導体基板（２）の主表面（１）に接するソース領域、ドレイン領域およびチャネル領域を有する活性領域（６）が設けられており，

前記半導体基板（２）の主表面（１）に少なくとも１つのトレンチが設けられており、該トレンチはチャネル領域（６）と接しており，該トレンチにゲート電極（８）の一部が配置されている、電界効果制御型トランジスタ。

【請求項２】　少なくとも前記トレンチの領域内で、前記チャネル領域の表面にゲート絶縁体（７）が設けられている、請求項１に記載の電界効果制御型トランジスタ。

【請求項３】　前記ソース領域（１５）および前記ドレイン領域（１５）の広がりが、前記主表面（１）に対して垂直に，トレンチの深さと比して小さいか又は同じである、請求項１又は２に記載の電界効果制御型トランジスタ。

【請求項４】　前記活性領域（６）および前記トレンチを囲むアイソレーション構造（１０）が設けられている、請求項１から３までのいずれか１項記載の電界効果制御型トランジスタ。

【請求項５】　前記主表面（１）に第１のトレンチ及び第２のトレンチが設けられており、当該２つのトレンチはチャネル領域の互いに対向する側壁に接しており、該２つのトレンチにそれぞれゲート電極の部分（８）が配置されている、請求項１から４までのいずれか１項記載の電界効果制御型トランジスタ。

【請求項６】　半導体基板（２）の主表面（１）に、活性領域（６）を側方に決定するトレンチが形成され，前記活性領域（６）は，それぞれ前記半導体基板（２）の主表面（１）に接するソース領域，チャネル領域およびドレイン領域を有しており、

前記トレンチに部分的に配置されているゲート電極（８，１２）が形成される，電界効果制御型トランジスタの製造方法。

【請求項７】　前記チャネル領域の表面にゲート絶縁体（７）が形成される、請求項６に記載の方法。

【請求項８】　前記ゲート電極の形成のために、第１の導電層がデポジット

され、該第１の導電層から、異方性エッチングにより導電性スペーサ（８）が、前記活性領域（６）の側壁に形成され、

前記活性領域（６）及び前記導電性スペーサ（８）を囲むアイソレーション構造（１０）が形成され、

前記導電性スペーサ（８）と接続されている第２の導電層（１２）がデポジットされ、

前記第２の導電層（１２）及び前記導電性スペーサ（８）の構造化によって、前記ゲート電極（８，１２）が形成される、請求項６又は７に記載の方法。

【請求項９】　前記導電性スペーサ（８）の構造化の際に、ソース領域（１６）及びドレイン領域（１６）の範囲内で、前記アイソレーション構造（１０）と前記活性領域（６）との間に中間空間が形成され、該中間空間にアイソレーション材料（１４）が充填される、請求項８に記載の方法。

【請求項１０】　前記ソース領域（１６）及びドレイン領域（１６）がインプランテーションにより、前記第２の導電層（１２）及び前記アイソレーション構造（１０）に対してセルフアライメントで形成される、請求項８又は９に記載の方法。

【発明の詳細な説明】

【０００１】

本発明は、チャネル長が５０ｎｍより小さい場合にも機能できる電界効果制御型トランジスタに関する。

【０００２】

プレーナＭＯＳトランジスタ及び接合トランジスタは約５０ｎｍのチャネル長で作動限界に達する。５０ｎｍ未満のゲート長領域に対して種々のトランジスタ構造が提案されている（例えば、H.Wong 他、IEDM 97、第４２７頁以降参照）。この場合、ＭＯＳトランジスタが２つのゲート電極を有しており、該ゲート電極は、チャネル領域の互いに対向する側に配置されており、よってチャネル領域の２つの表面に沿って電流を制御することを提案している。これは、ソース領域、チャネル領域およびドレイン領域が、シリコンウエハの主表面に対して垂直方向に配置されており、主表面より突出したスタックを形成する縦型構造も、ソース領域、チャネル領域およびドレイン領域が、シリコンウエハの主表面に対して平行に配置されている平坦型構造も可能である。

【０００３】

H.Wong 他、IEDM 97、第４２７頁以降において、プレーナＭＯＳトランジスタをＳＯＩ基板上で実現することが提案されており、ここではチャネル領域の上方のゲート電極とチャネル領域の下方のゲート電極とが設けられている。トランジスタの製造のために、シリコン基板上に厚いシリコン酸化物層，第１のシリコン窒化物層、第１の薄いシリコン酸化物層、アモルファスシリコンから成るスペーサ層，第２の薄いシリコン酸化物層および第２のシリコン窒化物層を設けて、ソースおよびドレイン領域の厚いシリコン酸化物層の表面が露出されるように構造化することが提案されている。また、ソース／ドレイン領域の一方において，厚いシリコン酸化物層に窓がシリコン基板の表面まで開けられる。アモルファスシリコンから成るスペーサ層は、ゲートスタックの領域で除去される。次に、選択的エピタキシーにより、シリコン基板の露出した表面から、ソース／ドレイン領域およびチャネル領域の範囲において単結晶シリコンを成長させる。構造化された第１のシリコン窒化物層および第２のシリコン窒化物層を除去し、ドーピング

された多結晶シリコンをデポジットすることにより、選択的エピタキシーにて成長したチャネル領域の上方および下方に２つのゲート電極が形成される。この方法は、半導体プロセス技術の標準的ステップとコンパチブルでない。

【０００４】

D.Hisamoto他、IEDM 89 第８３３～８３６頁に、ソース領域，チャネル領域およびドレイン領域をシリコンウェブに有しているプレーナＭＯＳトランジスタが提案されており、該シリコンウェブはフィールド酸化物領域により、その下に配置されているシリコン基板に対して絶縁分離されている。ゲート電極はチャネル領域の範囲内でシリコンウェブとオーバーラップしており、したがって、シリコンウェブの双方の側壁に沿ってチャネル電流を制御する。電流方向はシリコン基板の主表面に対して平行に流れる。当該トランジスタを製造するために、シリコン基板の表面に、シリコン窒化物層で覆われており、その側壁にシリコン窒化物スペーサが設けられているシリコンウェブを構造化することが提案されている。さらにシリコン基板の表面が、シリコン窒化物スペーサの下にアンダーエッチングされる。フィールド酸化物領域は、シリコン基板の表面の局部的な酸化（local oxidation）により形成される。その際、酸化は、ウェブの両側に形成されるフィールド酸化物領域が、生ずるバーズビークによってウェブの下方に達するまで続けられる。この製造プロセスも、半導体プロセス技術の標準的ステップとコンパチブルでない。

【０００５】

本発明の課題は、５０ｎｍ未満のゲート長の場合にも機能し、半導体プロセス技術の標準ステップを用いて製造可能である電界効果制御型トランジスタを提供することである。さらに、該トランジスタの製造方法が提案される。

【０００６】

上記課題は本発明により、請求項１に記載の電界効果制御型トランジスタおよび請求項６に記載の該トランジスタの製造方法により解決される。本発明の別の構成が従属請求項に記載されている。

【０００７】

電界効果制御型トランジスタが半導体基板にて実現される。半導体基板に、そ

れぞれ該半導体基板の主表面に接するソース領域、チャネル領域およびドレイン領域を有する活性領域が設けられており、したがって、ソース領域とドレイン領域との間で電流が半導体基板の主表面に対して平行に流れる。半導体基板の主表面に少なくとも１つのトレンチが設けられており，トレンチはチャネル領域と接しており、トレンチにゲート電極の一部が配置されている。トランジスタにおいて，ゲート電極の一部が半導体基板の深さに達する。したがって、ゲート電極を介して、サブストレートの主表面を切断するチャネル領域の側壁でサブストレートの主表面に対して平行に流れる電流を制御できる。よって、有効チャネル幅は、半導体基板の主表面におけるチャネル領域の幅に依存しない。

【０００８】

トランジスタはＭＯＳトランジスタとしても接合トランジスタとしても実現できる。ＭＯＳトランジスタの場合、少なくともトレンチの領域内で、チャネル領域の表面にゲート絶縁体が設けられている。

【０００９】

標準的シリコンプロセス技術において集積化を考慮して、少なくとも主表面の領域に単結晶シリコンを有する半導体基板を用いると有利である。半導体基板として有利には、単結晶シリコンウエハ、ＳＯＩ基板の単結晶シリコン層，ＳｉＧｅサブストレート又はＳｉＣサブストレートが適している。

【００１０】

有利には，チャネル領域の互いに対向する側壁に，それぞれゲート電極の部分が配置されており、したがって、トランジスタは有効に２つの互いに対向するゲート電極部分を有している。これらの部分はそれぞれ第１のトレンチ及び第２のトレンチに配置されている。２つのゲート電極部分を設けることにより，チャネル領域の互いに対向する側壁にて反転チャネルが制御される。この構成により，ドレイン電圧のチャネル領域に対するパンチスルー（Durchgriff）が低減され，したがって、文献から公知の制限的な”Drain Induced Barrier Lowering”は実際に作用しない。さらに、２つのゲート電極部分を設けることにより，サブストレート電圧がチャネル領域に与える好ましくない影響が低減される。

【００１１】

有利には、ソース領域およびドレイン領域の広がりが、半導体基板の主表面に対して垂直に、１つの又は複数のトレンチの深さと比して小さいか又は同じである。この構成により、それにわたって導電反転チャネルが形成される面は拡大される、したがって、平坦型装置に比して電流利得（Stromergiebigkeit）が増大する。さらにこのことにより、トランジスタの制御に重要であるトランジスタの相互コンダクタンスが増大する。

【００１２】

有利には、ゲート電極の寸法は主表面に対して平行にチャネル領域の寸法に制限される。よって、ドレイン・ゲートオーバーラップ容量が最小化される。このことにより、寄生容量が最小化され、トランジスタの相互コンダクタンスが高められる。これは、高速のスイッチング特性および良好な高周波特性のためにＧＨｚ領域では有利である。

【００１３】

集積回路の中のトランジスタのアイソレーションのために、活性領域および１つ又は複数のトレンチを囲むアイソレーション構造を設けることは有利である。

【００１４】

トランジスタの製造のために、半導体基板の主表面に、活性領域を側方に決定するトレンチが形成される。続いて、部分的にトレンチに配置されているゲート電極が形成される。

【００１５】

ＭＯＳトランジスタとしてトランジスタを製造するために、チャネル領域の表面にゲート絶縁体が形成される。

【００１６】

ゲート電極をセルフアライメントで形成するために、第１の導電層がデポジットされ、該第１の導電層から、異方性エッチングにより導電性スペーサが、活性領域の側壁に形成される。引続いて、活性領域及び導電性スペーサを囲むアイソレーション構造が形成される。この場合、半導体基板の主表面に対して平行な導電性スペーサの表面は露出される。導電性スペーサの露出表面を介して該導電性スペーサと接続されている第２の導電層がデポジットされる。第２の導電層及び

導電性スペーサの構造化によって、ゲート電極が形成される。導電層の材料として有利には、ドーピングされた多結晶又はアモルファスシリコン、金属珪化物及び／又は金属が適している。有利には、ゲート電極の製造のための構造化はマスクエッチングにより実施される。その際用いられるマスクはゲート長を決定する。この場合、微細構造化ステップ、例えば電子ビームリソグラフィを用いたり、インプリント方法にて、又はスペーサ技術を利用することにより、５０ｎｍ以下、有利には１０～５０ｎｍのゲート長が実現できる。

【００１７】

有利にはソース／ドレイン領域の製造が、インプランテーションにより、ゲート電極に対してセルフアライメントで行われる。

【００１８】

有利にはトレンチは、アイソレーション構造およびゲート電極の断面に相応する断面を有している。この場合、アイソレーション構造は例えば、トレンチを完全に充填するアイソレーション層をデポジットすること及び化学的機械研磨により形成される。

【００１９】

次に本発明を実施の形態に基づき図を用いて詳細に説明する。

【００２０】

図１は，第１のシリコン酸化物層および第２のシリコン酸化物層および活性領域を決定するマスクの形成のための半導体基板の断面略図を示す。

【００２１】

図２は、図１を上から見た平面略図である。

【００２２】

図３は，半導体基板の活性領域の構造化のため、ゲート絶縁体の形成および活性領域の側壁における導電性スペーサの形成のための半導体基板の断面略図を示す。

【００２３】

図４は、半導体基板の別のエッチングによる半導体基板の断面略図を示す。

【００２４】

図５は、アイソレーション構造の形成のため、ゲート電極の形成、ソース領域とドレイン領域との間の中間空間の充填、アイソレーション材料を用いたアイソレーション構造の形成のための半導体基板を上から見た平面略図である。

【００２５】

図６は、図５の一点鎖線VI－VIに沿った断面図である。

【００２６】

図７は、図５の一点鎖線VII－VIIに沿った断面図である。

【００２７】

図８は、図５の一点鎖線VIII－VIIIに沿った断面図である。

【００２８】

ドーピング材濃度が$10^{19}cm^{-3}$のｐドーピングされた単結晶シリコンから成る半導体基板２の主表面１の上に、熱酸化により第１のシリコン酸化物層３が被着される。第１のシリコン酸化物層３の厚さは５ｎｍである。第１のシリコン酸化物層３の上に、２０ｎｍの厚さを有する第１のシリコン窒化物層４がデポジットされる。第１のシリコン窒化物層４の表面上に、トレンチに囲まれた活性領域を決定するマスク５が形成される（図１及び図２参照）。マスク５は主表面１に対して平行に実質的に方形の横断面を有しており、その寸法は４０ｎｍ×５００ｎｍである。

【００２９】

異方性エッチングにより、第１のシリコン窒化物層４、第１のシリコン酸化物層３および半導体基板２がエッチングされ、その際、半導体基板２にトレンチに囲まれている活性領域６が形成される（図３参照）。エッチングガスとしてＣＦ$_4$およびＨ$_2$が用いられる。このエッチングは主表面１の下方に５００ｎｍの深さまで行われる。

【００３０】

熱酸化により、活性領域６の側壁に３ｎｍの層厚のＳｉＯ$_2$から成るゲート絶縁体７が形成される。

【００３１】

ドーピングされた多結晶シリコンから成る第１の導電層のデポジットおよび該

第１の導電層のエッチバックにより、活性領域６の側壁にドーピングされた多結晶シリコンから成る導電性スペーサ８が形成される（図３参照）。導電性スペーサ８は活性領域６をリング状に囲んでいる。

【００３２】

SiF_4およびH₂を用いた別の異方性エッチングプロセスにおいて、ゲート絶縁体７の露出部分が除去される。続いてCF_4を用いた異方性エッチングにより、半導体基板２がエッチングされる。したがって、活性領域６および導電性スペーサ８の側方に、主表面１を基準として１μｍの深さを有するアイソレーショントレンチ９が生ずる（図４参照）。

【００３３】

アイソレーショントレンチは第２のSiO_2層をデポジットすることにより充填される。第１のシリコン窒化物層４がエッチストップとして作用する引続いての化学的機械研磨によって、第２のシリコン酸化物層から、アイソレーショントレンチ９を充填するアイソレーション構造１０が形成される（図６参照）。

【００３４】

燐素をインプランテーションすることにより、活性領域６に、$5\times10^{17}cm^{-3}$のドーピング材濃度のチャネルドーピング部１１が形成される。

【００３５】

全く平面的に第２の導電層１２および第２のシリコン窒化物層１３がデポジットされ、マスクを用いて（図示せず）構造化される。構造化された第２の導電層１２および構造化された第２のSi_3N_4層１３は、ストリップ状の横断面を有しており、この横断面は活性領域６の長手方向広がりに対して横向きに延びており、活性領域６の長手方向広がりに対して平行に４０ｎｍの幅を有している。第２の導電層１２の構造化の際に、導電性スペーサ８の露出領域が同様に除去される。当該構造化はSiF_4およびH₂を用いた異方性エッチングにより実施される。

【００３６】

第３のシリコン窒化物層のデポジットおよび該第３のシリコン酸化物層のエッチバックにより、導電性スペーサ８の除去の際に構造化された第２の導電層１２

の外側に生ずる．活性領域６とアイソレーション構造１０との間の中間空間に、アイソレーション充填材１４が充填される（図７参照）。

【００３７】

構造化された第２の導電層１２および構造化された第２のシリコン窒化物層１３の側壁には、第３のシリコン窒化物層のデポジットおよび該第３のシリコン窒化物層の異方性エッチバックにより、シリコン窒化物スペーサ１５が形成される（図５及び図８参照）。Ａｓを５０ｋｅＶのエネルギー及び２×１０^{15}ｃｍ$^{-2}$のドーズ量にてインプランテーションすることにより、構造化された第２の導電層１２に対しセルフアライメントされて、ソース／ドレイン領域１６が形成される（図７及び図８参照）。この場合、主表面１の下方のソース／ドレイン領域１６の深さは、導電性スペーサ８が延在している深さよりも小さい。

【００３８】

導電性スペーサ８は構造化された第２の導電層１２を介して相互に接続されている。導電性スペーサ８およびこれを接続する第２の構造化された導電層１２の部分が、ゲート電極として作用する。導電性スペーサ８はソース／ドレイン領域１６より深く半導体基板１に延びているので、ゲート電極を相応して制御する際、該ソース／ドレイン領域１６の深さ全体にわたって、ソース／ドレイン領域１６の間に導電反転チャネルが形成される。したがって、ソース／ドレイン領域１６の間の活性領域６の範囲は、深さ全体にわたってチャネル領域として作用する。

【００３９】

当該トランジスタの製造のために、公知の方法（詳述せず）により多層メタライゼーションが行われる。

【００４０】

実施例ではｎチャネルトランジスタについて説明したが、本発明は同様にｐチャネルトランジスタとして実施可能である。さらに、導電層は別の導電性材料、有利には金属珪化物又は金属から構成できる。また、ゲート絶縁体７は活性領域の主表面１の領域に設けることも可能であり，したがって，主表面に沿って導電反転チャネルが形成できる。この場合、活性領域６と第２の導電層１２との間に

おいて、第１のシリコン酸化物層および第１のシリコン窒化物層は必要としない。技術的に必要であれば、ソース／ドレイン領域１６がＬＤＤプロファイルを用いて形成できる。

【図面の簡単な説明】

【図１】

第１のシリコン酸化物層および第２のシリコン酸化物層および活性領域を決定するマスクの形成のための半導体基板の断面略図を示す。

【図２】

図１を上から見た平面略図である。

【図３】

半導体基板の活性領域の構造化のため、ゲート絶縁体の形成および活性領域の側壁における導電性スペーサの形成のための半導体基板の断面略図を示す。

【図４】

半導体基板の別のエッチングによる半導体基板の断面略図を示す

【図５】

アイソレーション構造の形成のため、ゲート電極の形成、ソース領域とドレイン領域との間の中間空間の充填，アイソレーション材料を用いたアイソレーション構造の形成のための半導体基板を上から見た平面略図である。

【図６】

図５の一点鎖線VI－VIに沿った断面図である。

【図７】

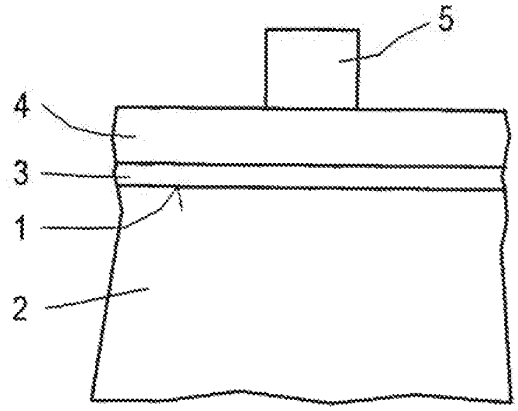
図５の一点鎖線VII－VIIに沿った断面図である。

【図８】

図５の一点鎖線VIII－VIIIに沿った断面図である。

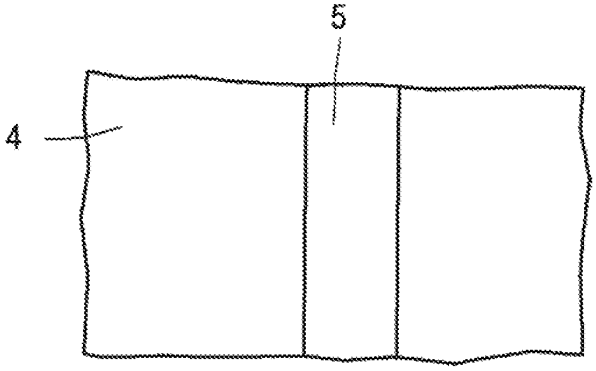
【図１】

FIG 1



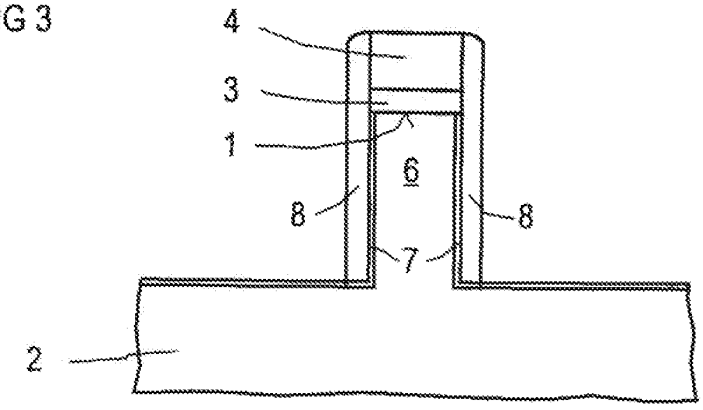
【図２】

FIG 2



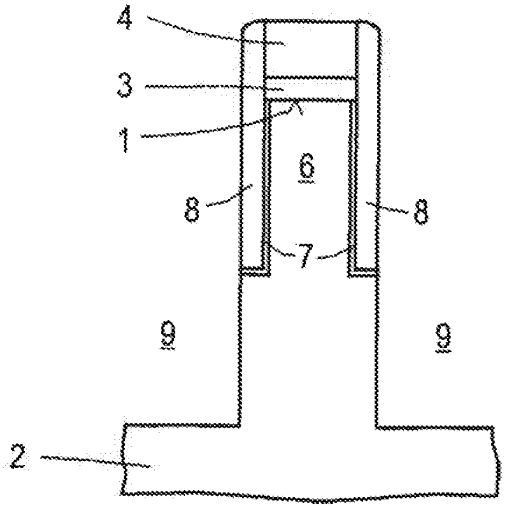
【図３】

FIG 3



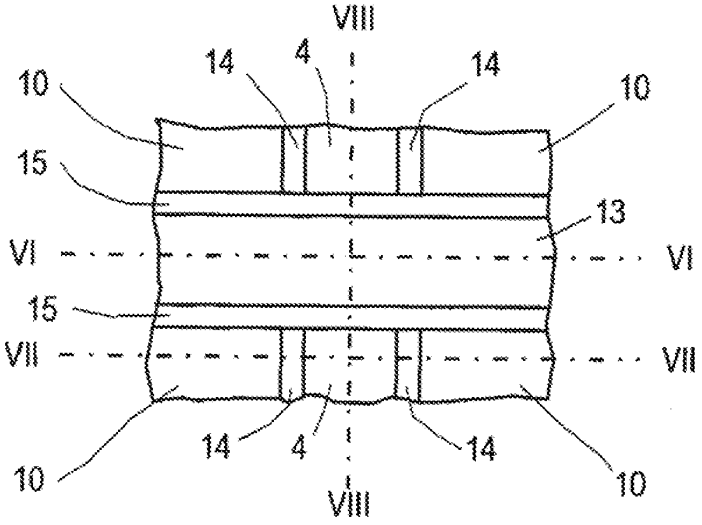
【図４】

FIG 4



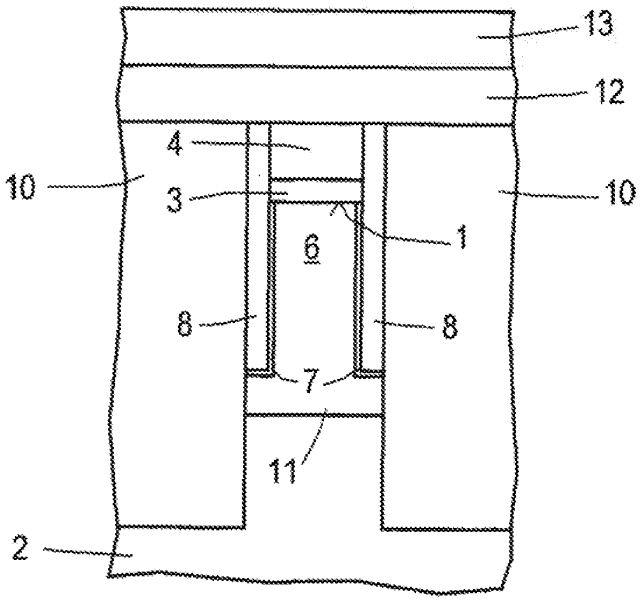
【図５】

FIG 5



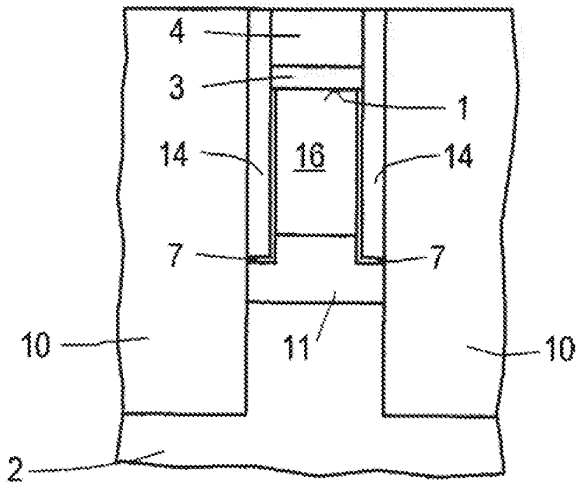
【図６】

FIG 6



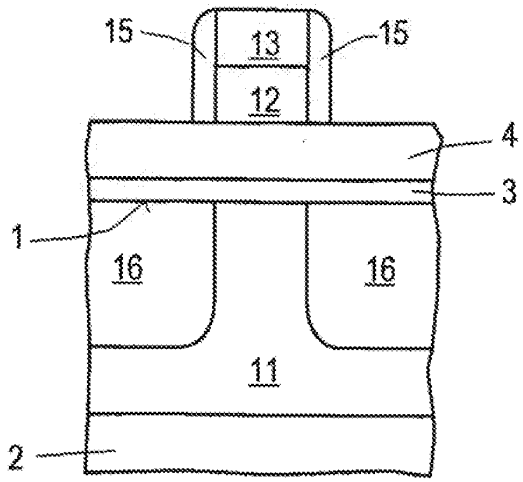
【図７】

FIG 7



【図８】

FIG 8



【手続補正書】特許協力条約第３４条補正の翻訳文提出書

【提出日】平成１３年１月５日（２００１．１．５）

【手続補正１】

【補正対象書類名】明細書

【補正対象項目名】特許請求の範囲

【補正方法】変更

【補正内容】

【特許請求の範囲】

【請求項１】　半導体基板（２）に、それぞれ該半導体基板（２）の主表面（１）に接するソース領域、ドレイン領域およびチャネル領域を有する活性領域（６）が設けられており、

前記主表面（１）に第１のトレンチ及び第２のトレンチが設けられており、当該２つのトレンチは前記活性領域（６）の互いに対向する側壁に接しており、該２つのトレンチにそれぞれゲート電極の部分（８）が配置されている、電界効果制御型トランジスタにおいて、

前記ゲート電極は、活性領域（６）の対向する側に設けられている２つの導電性スペーサ（８）と、当該導電性スペーサ（８）を接続する導電層（１２）の部分とから成り、

前記第１及び第２のトレンチはアイソレーション構造（１０）により充填されており、したがって、導電性スペーサ（８）は活性領域（６）とアイソレーション構造との間に配置されており、

前記活性領域とアイソレーション構造（１０）との間で該活性領域（６）の２つの側の互いに対向する側に形成される中空空間に、アイソレーション充填材（１４）が充填されていることを特徴とする、電界効果制御型トランジスタ。

【請求項２】　少なくとも第１及び第２のトレンチの領域内で、前記活性領域の表面にゲート絶縁体（７）が設けられていることを特徴とする、請求項１に記載の電界効果制御型トランジスタ。

【請求項３】　ソース領域（１０）およびドレイン領域（１６）の広がりが、前記主表面（１）に対して垂直に、トレンチの深さと比して小さいか又は同じ

であることを特徴とする、請求項１又は２に記載の電界効果制御型トランジスタ。

【請求項４】　前記アイソレーション構造（１０）が前記活性領域（６）を囲んでいることを特徴とする、請求項１から３までのいずれか１項記載の電界効果制御型トランジスタ。

【請求項５】　半導体基板（２）の主表面（１）に、活性領域（６）を側方に決定する第１及び第２のトレンチが形成され、前記活性領域（６）は、それぞれ前記半導体基板（２）の主表面（１）に接するソース領域（１６）、チャネル領域およびドレイン領域を有しており、

ゲート電極の形成のために、第１の導電層がデポジットされ、該第１の導電層から、異方性エッチングにより導電性スペーサ（８）が、前記活性領域（６）の２つの互いに対向する側に形成される、請求項１から４までのいずれか１項記載の電界効果制御型トランジスタの製造方法において、

前記活性領域（６）及び前記導電性スペーサ（８）を囲むアイソレーション構造（１０）が形成され、

前記導電性スペーサ（８）と接続されている第２の導電層（１２）がデポジットされ、

前記第２の導電層（１２）及び前記導電性スペーサ（８）の構造化によって、前記ゲート電極（８，１２）が形成され、

前記導電性スペーサ（８）の構造化の際に、ソース領域（１６）及びドレイン領域（１６）の範囲内で、前記アイソレーション構造（１０）と前記活性領域（６）との間に中間空間が形成され、該中間空間にアイソレーション材料（１４）が充填されることを特徴とする、電界効果制御型トランジスタの製造方法。

【請求項６】　前記ソース領域（１６）及びドレイン領域（１６）がインプランテーションにより、前記第２の導電層（１２）及び前記アイソレーション構造（１０）に対してセルフアライメントで形成されることを特徴とする、請求項５に記載の方法。

【手続補正書】特許協力条約第３４条補正の翻訳文提出書

【提出日】平成１３年２月２６日（２００１．２．２６）

【手続補正１】

【補正対象書類名】明細書

【補正対象項目名】請求項１

【補正方法】変更

【補正内容】

【請求項１】　半導体基板（２）に、それぞれ該半導体基板（２）の主表面（１）に接するソース領域、ドレイン領域およびチャネル領域を有する活性領域（６）が設けられており、

前記主表面（１）に第１のトレンチ及び第２のトレンチが設けられており、当該２つのトレンチは前記活性領域（６）の互いに対向する側壁に接しており、該２つのトレンチにそれぞれゲート電極の部分（８）が配置されている、電界効果制御型トランジスタにおいて、

前記ゲート電極は、チャネル領域の範囲内に且つ構造化された導電層（１２）の外側にある、活性領域（６）の対向する側に設けられている２つの導電性スペーサ（８）と、当該導電性スペーサ（８）を接続する導電層（１２）の部分とから成り、

前記第１及び第２のトレンチはアイソレーション構造（１０）により充填されており、したがって、導電性スペーサ（８）は活性領域（６）とアイソレーション構造との間に配置されており、導電層（１２）は充填部を越えて延在しており、

前記活性領域とアイソレーション構造（１０）との間で該活性領域（６）の２つの側の互いに対向する側に形成される中空空間に、アイソレーション充填材（１４）が充填されており，これは、ソース領域およびドレイン領域の範囲内に且つ構造化された導電層（１２）の外側に設けられていることを特徴とする、電界効果制御型トランジスタ。

【国際調査報告】

INTERNATIONAL SEARCH REPORT

Int. onal Application No
PCT/DE 99/03674

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7　H01L29/78　H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7　H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 09, 30 September 1996 (1996-09-30) & JP 08 139325 A (TOSHIBA CORP), 31 May 1996 (1996-05-31) abstract & US 5 844 278 A 1 December 1998 (1998-12-01) figures 12,13,21	1-7
X	US 4 979 014 A (WATANABE HIDEHIRO ET AL) 18 December 1990 (1990-12-18) the whole document	1-7
X	EP 0 510 667 A (CANON KK) 28 October 1992 (1992-10-28) figures 8-18	1-3,5-7

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[X] Further documents are listed in the continuation of box C.　[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search	Date of mailing of the international search report
25 October 2000	02/11/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gélébart, J

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page 1 of 2

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/DE 99/03674

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 563 082 A (MUKAI MIKIO) 8 October 1996 (1996-10-08) figures 1-10	18

1

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page 2 of 2

INTERNATIONAL SEARCH REPORT

Information on patent family members

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Form PCT/ISA/210 (patent family annex) (July 1992)

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BG14 BG27 BG40 BG45 BH05
BH25 BH28 BK13 CB04 CE05
CE07

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　JP 2004-356472 A 2004.12.16
(11)特許出願公開番号
特開2004-356472
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(43)公開日　平成16年12月16日(2004.12.16)

(51)Int.Cl.[7]	FI		テーマコード(参考)
Ｈ０１Ｌ　29/786	Ｈ０１Ｌ　29/78	６１７Ｋ	４Ｍ１０４
Ｈ０１Ｌ　21/336	Ｈ０１Ｌ　27/08	３３１Ｅ	５Ｆ０４８
Ｈ０１Ｌ　21/8234	Ｈ０１Ｌ　29/78	６１７Ｍ	５Ｆ１１０
Ｈ０１Ｌ　21/8238	Ｈ０１Ｌ　29/78	６１８Ｃ	
Ｈ０１Ｌ　27/08	Ｈ０１Ｌ　29/78	６２７Ａ	

審査請求　未請求　請求項の数23　ＯＬ　（全22頁）　最終頁に続く

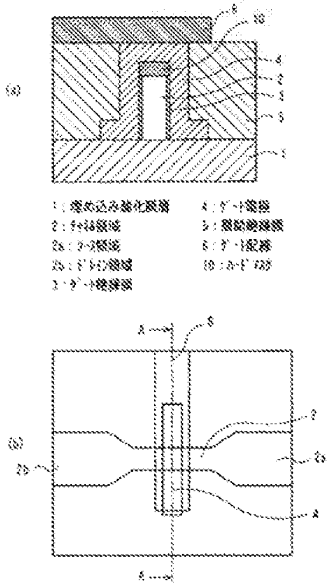
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最終頁に続く

(54)【発明の名称】半導体装置及びその製造方法

(57)【要約】
【課題】ゲート電極またはゲート配線あるいはその両方を低抵抗にすることができ、また、ＣＭＩＳ回路においても閾値電圧の制御が可能になる半導体装置及びその製造方法の提供を目的とするものである。
【解決手段】埋込み酸化層１に突出するように形成されたソース領域２ａ、チャネル領域２及びドレイン領域２ｂとなるシリコン層と、チャネル領域２をゲート絶縁膜３を介して３方向から覆うゲート電極４とを有するＦＥＴ、ゲート電極４の突出方向面が露出するように上記シリコン層を埋設する層間絶縁膜５、露出したゲート電極４の突出方向の面に電気的に接続されたゲート配線６を備えたものとする。
【選択図】　図１



【特許請求の範囲】
【請求項１】
基板上に突出するように形成されたソース領域、チャネル領域及びドレイン領域となるシリコン層と、上記シリコン層表面に形成された絶縁膜と、上記チャネル領域を上記絶縁膜を介して３方向から覆うゲート電極とを有するＦＥＴ、
上記ゲート電極の突出方向の面が露出するように上記シリコン層を埋設する層間絶縁膜、
上記露出したゲート電極の突出方向の面に電気的に接続されたゲート配線、を備えたことを特徴とする半導体装置。
【請求項２】
上記ゲート電極が、シリコンまたはシリコンとゲルマニウムとの合金からなることを特徴とする請求項１記載の半導体装置。
【請求項３】
上記ゲート電極が、金属シリサイドからなることを特徴とする請求項１記載の半導体装置。
【請求項４】
上記ゲート電極が、金属からなることを特徴とする請求項１記載の半導体装置。
【請求項５】
基板上に突出するように形成されたソース領域、チャネル領域及びドレイン領域となる第１のシリコン層と、上記第１のシリコン層の表面に形成された第１の絶縁膜と、上記第１のシリコン層のチャネル領域を上記第１の絶縁膜を介して３方向から覆う第１のゲート電極とを有するＮＭＩＳ領域のＦＥＴ、
上記基板上に突出するように形成されたソース領域、チャネル領域及びドレイン領域となる第２のシリコン層と、上記第２のシリコン層の表面に形成された第２の絶縁膜と、上記第２のシリコン層のチャネル領域を上記第２の絶縁膜を介して３方向から覆う第２のゲート電極とを有するＰＭＩＳ領域のＦＥＴ、
上記第１及び第２のゲート電極の突出方向面が露出するように上記ＮＭＩＳ領域のＦＥＴ及びＰＭＩＳ領域のＦＥＴを埋設する層間絶縁膜、
上記露出した第１のゲート電極の突出方向の面に電気的に接続されたゲート配線及び第２のゲート電極の突出方向の面に電気的に接続されたゲート配線、を備えたことを特徴とする半導体装置。
【請求項６】
上記第１のゲート電極と上記第２のゲート電極とが、互いに仕事関数が異なる金属シリサイドからなることを特徴とする請求項５記載の半導体装置。
【請求項７】
上記第１のゲート電極と上記第２のゲート電極とが、互いに仕事関数が異なる金属からなることを特徴とする請求項５記載の半導体装置。
【請求項８】
上記絶縁膜が高誘電率膜であることを特徴とする請求項１または５記載の半導体装置。
【請求項９】
基板上のシリコン層をパターニングして上記基板上に突出するソース領域、チャネル領域及びドレイン領域を有するＦＥＴを形成する第１の工程、
上記パターニングしたシリコン層表面に絶縁膜を形成する第２の工程、
上記チャネル領域の３方向を上記絶縁膜を介して覆うゲート電極を形成する第３の工程、
層間絶縁膜を成膜する第４の工程、
上記層間絶縁膜を平坦化し、上記ゲート電極の突出方向の面を上記層間絶縁膜から露出させる第５の工程、
導電性膜を成膜し、パターニングして上記露出したゲート電極の突出方向の面と電気的に接続されたゲート配線を形成する第６の工程、を備えたことを特徴とする半導体装置の製造方法。
【請求項１０】

第３の工程で形成するゲート電極をポリシリコンまたはアモルファスシリコンとし、上記第５の工程の後、上記第６の工程の前に、金属膜を成膜し、熱処理を施すことによって上記ポリシリコンまたはアモルファスシリコンと上記金属膜とを反応させて上記ゲート電極を金属シリサイドにすることを特徴とする請求項９記載の半導体装置の製造方法。

【請求項１１】

上記第２の工程の後、上記第３の工程の前に、上記ＦＥＴを埋め込むポリシリコンまたはアモルファスシリコンを成膜し、成膜した上記ポリシリコンまたはアモルファスシリコンを平坦化し、上記第３の工程において上記平坦化したポリシリコンまたはアモルファスシリコンをパターニングすることにより，上記ゲート電極を形成することを特徴とする請求項９記載の半導体装置の製造方法。

【請求項１２】

上記第５の工程の後、上記第６の工程の前に，上記ポリシリコンまたはアモルファスシリコンを除去し、除去した部分及び上記層間絶縁膜上に導電性膜を成膜することを特徴とする請求項１１記載の半導体装置の製造方法。

【請求項１３】

第３の工程で形成するゲート電極をポリシリコンまたはアモルファスシリコンとし、上記第５の工程の後、上記第６の工程の前に、上記ポリシリコンまたはアモルファスシリコンを除去し、除去した部分及び上記層間絶縁膜上に導電性膜を成膜することを特徴とする請求項９記載の半導体装置の製造方法。

【請求項１４】

上記ポリシリコンまたはアモルファスシリコンを除去する際に上記絶縁膜を除去し、上記除去した部分に導電性膜を成膜する前に，上記パターニングしたシリコン層表面に新たな絶縁膜を形成することを特徴とする請求項１２または１３記載の半導体装置の製造方法。

【請求項１５】

上記第１の工程の前に上記シリコン層上にエッチングマスク膜を成膜し、上記第１の工程において上記エッチングマスク膜とともにシリコン層をパターニングし，上記第５の工程の後，上記第６の工程の前に、上記ゲート電極、上記パターニングしたエッチングマスク膜及び上記絶縁膜を除去し，上記パターニングしたシリコン層表面に新たな絶縁膜を形成し、上記除去した部分及び上記層間絶縁膜上に導電性膜を成膜することを特徴とする請求項９記載の半導体装置の製造方法。

【請求項１６】

上記導電性膜が金属膜であることを特徴とする請求項１２ないし１５のいずれかに記載の半導体装置の製造方法。

【請求項１７】

上記層間絶縁膜が、シリコン窒化膜であることを特徴とする請求項１５記載の半導体装置の製造方法。

【請求項１８】

上記第１の工程の前に上記シリコン層上にエッチングマスク膜を成膜し、上記第１の工程において上記エッチングマスク膜とともにシリコン層をパターニングした後、上記第２の工程の前に、上記エッチングマスク膜を除去することを特徴とする請求項９記載の半導体装置の製造方法。

【請求項１９】

基板上のシリコン層をパターニングして上記基板上に突出するソース領域、チャネル領域及びドレイン領域を有するＮＭＩＳ領域及びＰＭＩＳ領域のシリコン層を形成する第１の工程、

上記パターニングしたシリコン層表面に絶縁膜を形成しする第２の工程、

上記チャネル領域の３方向を上記絶縁膜を介して覆うポリシリコンまたはアモルファスシリコンからなるゲート電極を形成する第３の工程、

層間絶縁膜を成膜する第４の工程、

上記層間絶縁膜を平坦化し，上記ゲート電極の突出方向の面を上記層間絶縁膜から露出さ

せる第５の工程、
上記ＮＭＩＳ領域またはＰＭＩＳ領域の一方のゲート電極をシリサイド防止膜で被覆し、さらに、第１の金属膜で他方のゲート電極を被覆し、熱処理によって上記第１の金属膜と上記他方のゲート電極のポリシリコンまたはアモルファスシリコンとを反応させて上記他方のゲート電極を金属シリサイドにする第６の工程、
上記シリサイド防止膜を除去して、上記ＮＭＩＳ領域またはＰＭＩＳ領域の上記他方のゲート電極をシリサイド防止膜で被覆し、さらに、上記第１の金属膜とは異なる種類の第２の金属膜で上記一方のゲート電極を被覆し、熱処理によって上記第２の金属膜と上記一方のゲート電極のポリシリコンまたはアモルファスシリコンとを反応させて上記一方のゲート電極を金属シリサイドにする第７の工程、
導電性膜を成膜し、パターニングして上記露出した各ゲート電極の突出方向の面と電気的に接続されたゲート配線を形成する第８の工程、を備えたことを特徴とする半導体装置の製造方法。
【請求項２０】
上記シリサイド防止膜は、シリコン酸化膜、シリコン窒化膜またはＴｉＮ膜であることを特徴とする請求項１９記載の半導体装置の製造方法。
【請求項２１】
基板上のシリコン層をパターニングして上記基板上に突出するソース領域，チャネル領域及びドレイン領域を有するＮＭＩＳ領域及びＰＭＩＳ領域のシリコン層を形成する第１の工程、
上記パターニングしたシリコン層表面に絶縁膜を形成する第２の工程、
上記チャネル領域の３方向を上記絶縁膜を介して覆うポリシリコンまたはアモルファスシリコンからなるダミーゲート電極を形成する第３の工程、
層間絶縁膜を成膜する第４の工程、
上記層間絶縁膜を平坦化し、上記ダミーゲート電極の突出方向の面を上記層間絶縁膜から露出させる第５の工程、
上記ＮＭＩＳ領域のＰＥＴまたはＰＭＩＳ領域の一方のダミーゲート電極を第１のエッチングマスクで被覆し、他方のダミーゲート電極を除去し、上記第１のエッチングマスクを除去し、上記他方のダミーゲート電極を除去した部分に第１の金属膜を埋め込み、ゲート電極を形成する第６の工程、
上記ＮＭＩＳ領域またはＰＭＩＳ領域の上記他方のダミーゲート電極を第２のエッチングマスクで被覆し、上記一方のダミーゲート電極を除去し、上記第２のエッチングマスクを除去し、上記一方のゲート電極を除去した部分に上記第１の金属膜とは異なる種類の第２の金属膜を埋め込み、ゲート電極を形成する第７の工程、
導電性膜を成膜し、パターニングして上記露出した各ゲート電極の突出方向の面と電気的に接続されたゲート配線を形成する第８の工程、を備えたことを特徴とする半導体装置の製造方法。
【請求項２２】
上記第６の工程及び上記第７の工程において、上記ゲート電極を除去後、上記絶縁膜を除去した後、上記第１及び第２の金属を埋め込む前に、新たな絶縁膜を上記パターニングしたシリコン層表面に形成することを特徴とする請求項２１記載の半導体装置の製造方法。
【請求項２３】
上記新たな絶縁膜が、高誘電率膜であることを特徴とする請求項１３ないし１５または２２のいずれかに記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
この発明は、半導体装置及びその製造方法に関し、特に、電界効果トランジスタの電極配線構造及びその形成方法に関するものである。
【０００２】

【従来の技術】
半導体集積回路に用いられているＭＩＳＦＥＴ（金属－絶縁物－半導体電界効果トランジスタ）は、素子寸法の微細化、特に、ゲート長の縮小によって高密度集積化と駆動力の増大を同時に達成してきた。しかしながら、従来のトレンドにしたがったプレーナ型の素子では、微細化とともに、高速化、低消費電力化するという課題を満足させる技術を確立するのが困難になりつつある。このような課題を達成させる技術として、近年、ＦｉｎＦＥＴが活発に研究されつつある。
【０００３】
従来のプレーナ型ＦＥＴは、単結晶Ｓｉ表面上に形成したチャネル上部に、ゲート絶縁膜を介してゲート電極を形成するものであるが、ＦｉｎＦＥＴは、基板上に形成されたチャネルを、ゲート絶縁膜を介して横方向から両側を挟み込むダブルゲートを有する構造で、主にＳＯＩ層で構成する例が報告されている。
【０００４】
例えば、埋込み酸化膜上のＳＯＩ（Ｓｉ）層にシリコン酸化膜、シリコン窒化膜の２層構造のハードマスクを形成し、このハードマスクの開口部にあるＳＯＩ層をエッチングすることによって、ソース領域－チャネル領域－ドレイン領域を構成する半導体層領域を形成する。その後、エッチングダメージ除去及びチャネル層の薄膜化を行うために、犠牲酸化を行い、さらに、犠牲酸化層を除去する。
その後、ゲート酸化膜を熱酸化等によって形成し、ポリシリコン等の導電性膜を形成し、パターニングすることによってゲート電極を形成する。この方法によって、ゲート長が１０ｎｍといった微細なゲート電極が形成される。通常微細なゲート電極を形成する場合、最も微細加工技術が発達したポリシリコンやアモルファスシリコンを用いる（例えば、非特許文献１参照）。
【０００５】
【非特許文献１】
Ｂｉｎ　Ｙｕ，Ｌｅｉａｎｄ　Ｃｈａｎｇ，ｅｔ　ａｌ，「ＦｉｎＦＥＴ　Ｓｃａｌｉｎｇ　ｔｏ　１０ｎｍ　Ｇａｔｅ　Ｌｅｎｇｔｈ」，ＩＥＤＭ　Ｔｅｃｈ．Ｄｉｇ．，Ｄｅｃ．２００２，ｐｐ２５１－２５４
【０００６】
【発明が解決しようとする課題】
従来、ゲート配線の抵抗上昇を防止するため、サリサイド法が使用されているが、ゲート長１０ｎｍ以下が用いられる世代のデバイスでは、更にゲート電極及び配線の抵抗を低くすることが必要とされる。
【０００７】
金属膜をゲート電極に用いる場合、耐酸化性、耐薬品性が要求される上、パターニング技術においては、実績のあるポリシリコンのパターニング技術に比べると、まだ確立されていないという問題がある。
【０００８】
また、金属膜または金属シリサイド膜をゲート電極に形成する場合、ＣＭＩＳ回路のようにＰＭＩＳとＮＭＩＳのＦＥＴを両方具備するするため、閾値電圧の最適化を必要とするが、ポリシリコン電極のように閾値電圧の制御ができないという問題がある。
【０００９】
本発明は、上記のような問題を解決するものであり、ゲート電極またはゲート配線あるいはその両方を低抵抗にすることができる半導体装置及びその製造方法の提供を目的とするものである。
【００１０】
また、ＣＭＩＳ回路においても閾値電圧の制御が可能になる半導体装置及びその製造方法の提供を目的とするものである。
【００１１】
【課題を解決するための手段】

本発明に係る半導体装置は、基板上に突出するように形成されたソース領域、チャネル領域及びドレイン領域となるシリコン層と、上記シリコン層表面に形成された絶縁膜と、上記チャネル領域を上記絶縁膜を介して３方向から覆うゲート電極とを有するＦＥＴ、
上記ゲート電極の突出方向の面が露出するように上記シリコン層を埋設する層間絶縁膜、
上記露出したゲート電極の突出方向の面に電気的に接続されたゲート配線、を備えたものである。

【００１２】

また、基板上に突出するように形成されたソース領域、チャネル領域及びドレイン領域となる第１のシリコン層と、上記第１のシリコン層の表面に形成された第１の絶縁膜と、上記第１のシリコン層のチャネル領域を上記第１の絶縁膜を介して３方向から覆う第１のゲート電極とを有するＮＭＩＳ領域のＦＥＴ、
上記基板上に突出するように形成されたソース領域、チャネル領域及びドレイン領域となる第２のシリコン層と、上記第２のシリコン層の表面に形成された第２の絶縁膜と、上記第２のシリコン層のチャネル領域を上記第２の絶縁膜を介して３方向から覆う第２のゲート電極とを有するＰＭＩＳ領域のＦＥＴ、
上記第１及び第２のゲート電極の突出方向面が露出するように上記ＮＭＩＳ領域のＦＥＴ及びＰＭＩＳ領域のＦＥＴを埋設する層間絶縁膜、
上記露出した第１のゲート電極の突出方向の面に電気的に接続されたゲート配線及び第２のゲート電極の突出方向の面に電気的に接続されたゲート配線、を備えたものである。

【００１３】

本発明に係る半導体装置の製造方法は、基板上のシリコン層をパターニングして上記基板上に突出するソース領域、チャネル領域及びドレイン領域を有するＦＥＴを形成する第１の工程、
上記パターニングしたシリコン層表面に絶縁膜を形成する第２の工程、
上記チャネル領域の３方向を上記絶縁膜を介して覆うゲート電極を形成する第３の工程、
層間絶縁膜を成膜する第４の工程、
上記層間絶縁膜を平坦化し、上記ゲート電極の突出方向の面を上記層間絶縁膜から露出させる第５の工程、
導電性膜を成膜し、パターニングして上記露出したゲート電極の突出方向の面と電気的に接続されたゲート配線を形成する第６の工程、を備えたものである。

【００１４】

また、基板上のシリコン層をパターニングして上記基板上に突出するソース領域、チャネル領域及びドレイン領域を有するＮＭＩＳ領域及びＰＭＩＳ領域のシリコン層を形成する第１の工程、
上記パターニングしたシリコン層表面に絶縁膜を形成しする第２の工程、
上記チャネル領域の３方向を上記絶縁膜を介して覆うポリシリコンまたはアモルファスシリコンからなるゲート電極を形成する第３の工程、
層間絶縁膜を成膜する第４の工程、
上記層間絶縁膜を平坦化し、上記ゲート電極の突出方向の面を上記層間絶縁膜から露出させる第５の工程、
上記ＮＭＩＳ領域またはＰＭＩＳ領域の一方のゲート電極をシリサイド防止膜で被覆し、さらに、第１の金属膜で他方のゲート電極を被覆し、熱処理によって上記第１の金属膜と上記他方のゲート電極のポリシリコンまたはアモルファスシリコンとを反応させて上記他方のゲート電極を金属シリサイドにする第６の工程、
上記シリサイド防止膜を除去して、上記ＮＭＩＳ領域またはＰＭＩＳ領域の上記他方のゲート電極をシリサイド防止膜で被覆し、さらに、上記第１の金属膜とは異なる種類の第２の金属膜で上記一方のゲート電極を被覆し、熱処理によって上記第２の金属膜と上記一方のゲート電極のポリシリコンまたはアモルファスシリコンとを反応させて上記一方のゲート電極を金属シリサイドにする第７の工程、
導電性膜を成膜し、パターニングして上記露出した各ゲート電極の突出方向の面と電気的

に接続されたゲート配線を形成する第８の工程、を備えたものである。
【００１５】
また、基板上のシリコン層をパターニングして上記基板上に突出するソース領域、チャネル領域及びドレイン領域を有するＮＭＩＳ領域及びＰＭＩＳ領域のシリコン層を形成する第１の工程、
上記パターニングしたシリコン層表面に絶縁膜を形成する第２の工程、
上記チャネル領域の３方向を上記絶縁膜を介して覆うポリシリコンまたはアモルファスシリコンからなるダミーゲート電極を形成する第３の工程、
層間絶縁膜を成膜する第４の工程、
上記層間絶縁膜を平坦化し、上記ダミーゲート電極の突出方向の面を上記層間絶縁膜から露出させる第５の工程、
上記ＮＭＩＳ領域のＰＥＴまたはＰＭＩＳ領域の一方のダミーゲート電極を第１のエッチングマスクで被覆し、他方のダミーゲート電極を除去し、上記第１のエッチングマスクを除去し、上記他方のダミーゲート電極を除去した部分に第１の金属膜を埋め込み、ゲート電極を形成する第６の工程、
上記ＮＭＩＳ領域またはＰＭＩＳ領域の上記他方のダミーゲート電極を第２のエッチングマスクで被覆し、上記一方のダミーゲート電極を除去し、上記第２のエッチングマスクを除去し、上記一方のゲート電極を除去した部分に上記第１の金属膜とは異なる種類の第２の金属膜を埋め込み、ゲート電極を形成する第７の工程、
導電性膜を成膜し、パターニングして上記露出した各ゲート電極の突出方向の面と電気的に接続されたゲート配線を形成する第８の工程、を備えたものである。
【００１６】
【発明の実施の形態】
実施の形態１、
図１は、本発明に係る半導体装置の実施の形態１を示す断面図（ａ）及び平面図（ｂ）であり、断面図（ａ）は平面図（ｂ）のＡ－Ａ断面を示している。
【００１７】
図１（ｂ）に示したように、埋込み酸化層１（基板）上にソース領域２ａ、チャネル領域２及びドレイン領域２ｂが突出したフィン型のシリコン（Ｓｉ）が形成されている。図１（ａ）に示したように、チャネル領域２の周囲（３方向の面）にはゲート絶縁膜３及びチャネル領域２の上部に形成されたハードマスク１０を介してポリシリコンまたはアモルファスシリコンからなるゲート電極４が形成されている。ゲート電極４は層間絶縁膜５に埋め込まれ、上面が層間絶縁膜５から露出しており、層間絶縁膜５上にゲート電極４の露出面に接続された金属からなるゲート配線６が形成されている。なお、埋込み酸化層１に代えてシリコン基板としてもよい。
【００１８】
この構成によれば、ゲート電極４とゲート電極４に接続されるゲート配線６とを独立に形成することができるので、ゲート配線６の抵抗を任意に低抵抗化することができる。
【００１９】
また、層間絶縁膜５を平坦化し、平坦化した層間絶縁膜５上にゲート配線６を形成することができるので、ゲート配線６のパターニングを容易に行うことができる。
【００２０】
図２及び図３は、本実施の形態の半導体装置を製造する製造工程を示す断面図である。同図に基づき製造方法を説明する。
【００２１】
まず、埋込み酸化膜１上のシリコン層２５にシリコン酸化膜２６、シリコン窒化膜２７の２層構造のハードマスクを形成し、このハードマスクの開口部にあるシリコン層２５をエッチングすることによって、ソース領域－チャネル領域－ドレイン領域を構成する半導体層領域が形成される。図２（ｂ）は、形成された半導体層領域を示している。
【００２２】

次に、図２（ａ）に示したように、シリコン窒化膜２７上にソース領域－チャネル領域－ドレイン領域に対応するフォトレジスト２８を形成し、図２（ｂ）に示したように、フォトレジスト２８をマスクとしてシリコン酸化膜２６、シリコン窒化膜２７及びシリコン層２５をエッチングしてソース領域－チャネル領域２－ドレイン領域を形成する。

【００２３】

次に、図２（ｃ）に示したように、エッチングダメージ除去及びチャネル層の薄膜化を行うために、犠牲酸化を行って犠牲酸化層２９を形成し、さらに、図２（ｄ）に示したように、犠牲酸化層２９を除去する。

【００２４】

次に、図２（ｅ）に示したように、ゲート酸化膜３を熱酸化等によって形成する。以上、上記非特許文献１に記載された方法と同様の方法によって、ゲート長が１０ｎｍといった微細なフィン型のゲート電極が形成される。

【００２５】

次に、図３（ａ）に示したように、チャネル領域２の周囲に、ゲート酸化膜３及びハードマスク１０（図２におけるシリコン酸化膜２６）を介してポリシリコン膜またはアモルファスシリコン膜をＣＶＤ法により５０～１００ｎｍ形成し、チャネル領域２の幅しにパターニングしてゲート電極４を形成する。

【００２６】

幅Ｌは、チャネル領域２であるシリコン層の膜厚、ゲート絶縁膜３の膜厚の２倍、ゲート電極４の膜厚の２倍を加えた値に、リソグラフィーの重ね合わせ精度を考慮した値の２倍を加えた値とする。また、幅Ｌと垂直方向の値（高さ）はゲート長の値とする。例えば、シリコン層の膜厚が１０ｎｍ、ゲート絶縁膜３の膜厚が１．７ｎｍ、ポリシリコン膜の膜厚が５０ｎｍ、リソグラフィーの重ね合わせ精度が３０ｎｍであれば、Ｌは１７３．４ｎｍとする。

【００２７】

次に、図３（ｂ）に示したように、層間絶縁膜５であるシリコン酸化膜をＣＶＤ法等により形成し、ＣＭＰ法（化学機械研磨法）により平坦化し、ゲート電極４の上面を露出させる。

【００２８】

次に、図３（ｃ）に示したように、スパッタ法またはＣＶＤ法により金属膜、例えば、Ｗ（タングステン）、Ａｌ－Ｃｕ合金（アルミニウム－銅合金）、Ｃｕを成膜し、パターニングして金属膜からなる低抵抗なゲート配線６を形成する。

【００２９】

なお、図３（ｃ）において金属膜を形成する際に、通常行われる通り、金属膜の下部にＴｉＮ（窒化チタン）膜、ＴｉＮとＴｉとの積層膜、ＴａＮ（窒化タンタル）膜、またはＴａＮとＴａとの積層膜を成膜してもよい。

【００３０】

また、図３（ａ）において、ポリシリコン、アモルファスシリコンの代わりにシリコンとゲルマニウムとの合金を用いてもよい。

【００３１】

以上のように、本実施の形態における製造方法は、ゲート電極４とゲート電極４に接続されるゲート配線６とを独立に形成するので、ゲート配線６の抵抗を任意に低抵抗化することができる。

【００３２】

また、層間絶縁膜５を平坦化し、平坦化した層間絶縁膜５上にゲート配線６を形成するので、ゲート配線６のパターニングを容易に行うことができる。

【００３３】

なお、本実施の形態では埋込み酸化層１上にフィン型ＦＥＴを形成する例を示したが、シリコン基板上にフィン型ＦＥＴを形成してもよい。

【００３４】

実施の形態２．
上記実施の形態１ではゲート電極４としてポリシリコンまたはアモルファスシリコンを使用したが、ポリシリコンまたはアモルファスシリコンの空乏化はトランジスタの性能向上の妨げになる。そこで、空乏化を防止するために、ゲート電極４をポリシリコン、アモルファスシリコンに代えて金属シリサイドとする。
【００３５】
図４は、本実施の形態の半導体装置を製造する製造工程を示す断面図である。
同図に基づきゲート電極４にポリシリコンを用いた場合の製造方法を説明する。
【００３６】
上記実施の形態１と同様に図３（ｂ）までの工程を経た後、図４（ａ）に示したように、金属膜７、例えば、コバルト、ニッケル、チタン、タンタル、パナジウム、白金等、またはこれらの合金膜を、例えば、ＰＶＤ法により１０～３０ｎｍ成膜する。
【００３７】
次に、熱処理を行う。熱処理は、例えば，４００～６００℃、６０秒、窒素ガスまたは不活性ガス雰囲気中で加熱することによって行う。この熱処理によって、金属膜７とポリシリコン８が反応して金属シリサイド膜９が形成される。
【００３８】
金属膜７は、ポリシリコン８と接しない領域ではシリサイド化反応を生じないため、金属膜７として残存するので、酸、例えば、硫酸と過酸化水素水との混合液や塩酸と過酸化水素水との混合液により、未反応の金属膜７を除去する。これによって，図４（ｂ）に示したように、ポリシリコン８は金属シリサイド９に置換される。
【００３９】
この後、図４（ｃ）に示したように、スパッタ法またはＣＶＤ法により金属膜、例えば、Ｗ（タングステン）、Ａｌ－Ｃｕ合金（アルミニウム－銅合金）、Ｃｕ（銅）を成膜し，パターニングして金属膜からなる低抵抗なゲート配線６を形成する。
【００４０】
実施の形態３．
上記実施の形態１及び２において、例えば，ポリシリコンにパターニングを施す場合、ポリシリコンはチャネル領域２上に形成されているため、チャネル領域２の高さ，例えば、５０～６０ｎｍの段差上でリソグラフィーを施すことになる。このような段差があるために、ポリシリコンのパターニングが困難になる。
【００４１】
図５は、本実施の形態の半導体装置を製造する製造工程を示す断面図である。
図５（ａ）に示したように、チャネル領域２を埋め込むようにポリシリコン８を厚く形成した後、ＣＭＰ法により平坦化する。ポリシリコン８の厚さは、少なくともチャネル領域２とハードマスク１０の総和より厚く形成する。例えば、チャネル領域２が５０ｎｍ、ハードマスク１０が３０ｎｍの場合、ポリシリコン８の厚さを１５０ｎｍとする。
【００４２】
次に、図５（ｂ）に示したように，平坦化されたポリシリコン８上にリソグラフィー技術によってフォトレジスト１１を形成し、フォトレジスト１１をマスクにしてポリシリコン８をパターニングする。なお、この時ポリシリコン８上にシリコン酸化膜またはシリコン窒化膜のハードマスクを形成し、その上にフォトレジストを形成してもよい。
【００４３】
次に、図５（ｃ）に示したように、ＣＶＤ法によりシリコン酸化膜を成膜し、ＣＭＰ法により平坦化し、ポリシリコン８の上面が露出するように層間絶縁膜５を形成する。
【００４４】
以降の工程は、上記実施の形態１と同様にゲート配線を形成する。あるいは上記実施の形態２と同様にポリシリコン８を金属シリサイド化した後ゲート配線を形成する。
【００４５】
本実施の形態によれば、平坦化されたポリシリコン８上でリソグラフィー技術を施すこと

ができるので、ポリシリコン８のパターニングが容易にできる。

【００４６】

実施の形態４．

本実施の形態では、ゲート電極４のポリシリコン等における空乏化を防止し、かつ、低抵抗化するため、ポリシリコンに代えて金属膜を用いる。

【００４７】

上記実施の形態２では、ポリシリコンに代えて金属シリサイドを用いたが、金属膜を用いることによって更に低抵抗化することができる。

【００４８】

図６は、本実施の形態の半導体装置を製造する製造工程を示す断面図である。図５（ｃ）に示したように、ポリシリコン８を形成した後、図６（ａ）に示したように、ポリシリコン８をドライエッチング法により除去する。この時、ポリシリコン８を除去するのが目的であるので、異方性エッチングを必要とせず、等方性エッチングであってもよい。

【００４９】

次に、図６（ｂ）に示したように、ＣＶＤ法によってＴｉＮ膜１２ａとＷ膜１２ｂとの２層膜からなる金属膜１２を、ポリシリコン８を除去した領域及び層間絶縁膜５上に埋め込む。

【００５０】

Ｗはシリコン酸化膜からなる層間絶縁膜５との密着性に乏しいため、密着層としてＴｉＮ膜１２ａをＷ膜１２ｂ下に形成する。また，ＴｉＮはシリコン酸化膜からなるゲート絶縁膜３と反応しないので、ゲート絶縁膜３の劣化も生じない。

Ｗ膜の下地膜としてはＴｉＮの他、シリコン酸化膜との密着性がよく、ゲート絶縁膜３と反応しない金属または金属化合物であれば使用することができる。

【００５１】

次に、図６（ｃ）に示したように，リソグラフィー技術によって金属膜１２をパターニングしてゲート配線を形成する。

【００５２】

上記本実施の形態は、図５（ｃ）の工程の後、ポリシリコン８を除去する工程について説明したが、図７（ａ）に示すように、図３（ｂ）の工程の後、ポリシリコンからなるゲート電極４を除去するようにしてもよい。この後の工程は図６と同様の工程を経て、図７（ｂ）に示したゲート電極４及びゲート配線６が得られる。

【００５３】

実施の形態５．

上記実施の形態１ないし４では，ゲート絶縁膜３として熱酸化膜を用いた。本実施の形態では、更にゲート絶縁膜の実効的薄膜化を狙い、高誘電率膜を用いるものである。

【００５４】

図８は、本実施の形態の高誘電率膜を形成する工程を示す断面図である。図６（ａ）の工程または図７（ａ）の工程の後、図８（ａ）に示したように，シリコン酸化膜からなるゲート酸化膜３を、例えば、フッ酸を用いて除去する。

【００５５】

次に，図８（ｂ）に示したように、ＣＶＤ法により誘電率の高い絶縁膜、例えば，ハフニウム酸化膜、アルミナ膜、ハフニウムシリコン酸化膜，またはタンタル酸化膜等の高誘電率膜１３を形成する。

【００５６】

この後、図６（ｂ）及び（ｃ）に示した工程によって、ゲート電極４及びゲート配線６を形成する。

【００５７】

本実施の形態では，ゲート絶縁膜に高誘電率膜１３を用いているので，ゲート絶縁膜の実効的薄膜化が可能になる。

【００５８】

実施の形態６．
上記実施の形態１ないし５では、ハードマスク１０を残置した。本実施の形態では、ハードマスク１０を除去し、チャネル領域２の上部もゲート電極４で囲み、チャネルの電界を制御し、トランジスタの性能向上を図るものである。
【００５９】
図９は、本実施の形態の製造工程を示す断面図である。図９（ａ）に示したように、図５（ｃ）の工程において、シリコン酸化膜に代えてシリコン窒化膜からなる層間絶縁膜１４をＣＶＤ法によって形成し、ＣＭＰ法によって平坦化し、ポリシリコンからなるゲート電極４の上面を露出させる。
【００６０】
次に、図９（ｂ）に示したように、ポリシリコンからなるゲート電極４，ハードマスク１０及びゲート絶縁膜３をフッ酸等で除去する。
【００６１】
次に、図９（ｃ）に示したように、ＣＶＤ法により、シリコン酸化膜または高誘電率膜からなるゲート絶縁膜１５を形成する。
【００６２】
その後、図６（ｂ）及び（ｃ）に示した工程によって、金属膜からなるゲート電極４及びゲート配線６を形成する。
【００６３】
実施の形態７．
上記実施の形態１ないし６では、ハードマスク１０を残置したままポリシリコンからなるゲート電極４形成したが、ハードマスク１０を除去した後、ポリシリコンからなるゲート電極４形成してもよい。
【００６４】
図１０は、本実施の形態のハードマスク１０を除去した後の工程を示す断面図である。図２（ｄ）の工程の後、ドライエッチング法により、ハードマスク１０を除去する。
【００６５】
次に、図１０（ａ）に示したように、熱酸化法やＣＶＤ法によってゲート絶縁膜３を形成し、その後、ＣＶＤ法によりポリシリコンを成膜し、リソグラフィー及びエッチングの組合せによって、ポリシリコンからなるゲート電極４を形成する。
【００６６】
次に、図１０（ｂ）に示したように、シリコン酸化膜からなる層間絶縁膜５及びゲート配線６を、図３（ｂ）及び（ｃ）の工程と同様にして形成する。
【００６７】
本実施の形態によれば、上記実施の形態６よりも簡単な工程で、チャネル領域２の上部もゲート電極４で囲むことができる。
【００６８】
実施の形態８．
Ｎ型及びＰ型ＭＩＳトランジスタを含むＣＭＩＳ回路において、Ｎ型及びＰ型ＭＩＳトランジスタのゲート電極に同一の金属を用いると、両トランジスタのゲート電極の仕事関数が同一になるため、Ｎ型及びＰ型ＭＩＳトランジスタそれぞれの閾値を適正化することができない。
【００６９】
本実施の形態は、ＣＭＩＳ回路のＰＭＩＳとＮＭＩＳのＰＥＴを両方とも具備する回路において、金属シリサイドからなるゲート電極の閾値電圧を制御可能にする製造方法を提供するものである。
【００７０】
図１１及び１２は、本実施の形態の製造工程を示す断面図である。まず、図３または図５の工程においてＰＭＩＳ領域とＮＭＩＳ領域のＰＥＴを形成した後，図１１（ａ）に示したように、ＰＭＩＳ領域のゲート電極４の上面を覆い、ＮＭＩＳ領域のゲート電極４の上

面が露出するようにシリサイド防止膜１６を形成する。シリサイド防止膜１６は、例えば、常圧ＣＶＤ法によりシリコン酸化膜を５０ｎｍ成膜し、リソグラフィー及びドライエッチングまたはウェットエッチングによって成膜したシリコン酸化膜のＮＭＩＳ領域を除去することによって形成する。

【００７１】

次に、図１１（ｂ）に示したように、第１の金属膜１７として、例えば、コバルト膜をＰＶＤ法により１０～１５ｎｍ成膜する。

【００７２】

次に、４００～６００℃で、６０秒間加熱する熱処理を施すことによって、ＮＭＩＳ領域のゲート電極４のポリシリコンと第１の金属膜１７のコバルトとを反応させ、図１１（ｃ）に示したように、ＮＭＩＳ領域のゲート電極をコバルトシリサイド膜からなる第１の金属シリサイド１８とし、未反応のコバルト膜及びシリサイド防止膜１６を、選択的に硫酸と過酸化水素水との混合液等により除去する。この時、ＰＭＩＳ領域ゲート電極４は、シリサイド防止膜１６によって、第１の金属膜１７のコバルトとの反応が防止される。

【００７３】

なお、第１の金属膜１７として、コバルトの他、ニッケル、白金を用いることができる。

【００７４】

次に、図１２（ａ）に示したように、シリサイド防止膜１６をＮＭＩＳ領域の第１の金属シリサイド１８上を覆い、ＰＭＩＳ領域のゲート電極４の上面が露出ように形成する。このシリサイド防止膜１６は、例えば、常圧ＣＶＤ法によりシリコン酸化膜を５０ｎｍ成膜し、リソグラフィー及びドライエッチングまたはウェットエッチングによって成膜したシリコン酸化膜のＰＭＩＳ領域のシリコン酸化膜を除去することによって形成する。

【００７５】

次に、第２の金属膜、例えば、チタン膜をＰＶＤ法によって１０～１５ｎｍ成膜し、６００～８００℃で６０秒間加熱する熱処理を施すことによってゲート電極４のポリシリコンと第２の金属膜のチタンとを反応させ、図１２（ｂ）に示したように、ゲート電極４をチタンシリサイドからなる第２の金属シリサイド１９とする。この時、ＮＭＩＳ領域の第１の金属シリサイド１８は、シリサイド防止膜１６によって、第２の金属膜のチタンとの反応が防止される。

【００７６】

なお、第２の金属膜は，チタンの他，タンタルあるいはタングステンを使用することができる。

【００７７】

また、シリサイド防止膜１６としては、シリコン酸化膜の他、シリコン窒化膜、窒化チタン（ＴｉＮ）のような化合物であってもよい。ＴｉＮの場合、金属膜をシリサイド化した後、選択的に金属膜を除去する工程で同時に除去することができる。

【００７８】

次に、未反応のチタン膜及びシリサイド防止膜１６を選択的に硫酸と過酸化水素水との混合液等により除去する。

【００７９】

次に，図１２（ｃ）に示したように、ゲート配線６を上記実施の形態１と同様にして形成する。

【００８０】

以上のように、本実施の形態によれば、ＮＭＩＳ領域ＰＭＩＳ領域で異なる材料からなるゲート電極を形成することができるので、仕事関数の異なる第１の金属シリサイド膜と第２の金属シリサイド膜をＮＭＩＳ及びＰＭＩＳのＦＥＴのゲート電極として任意に選択することにより、各導電型のＦＥＴの閾値電圧の制御が可能になる。

【００８１】

実施の形態９．

図１３及び図１４は本実施の形態の製造工程を示す断面図である。上記実施の形態８では

ＮＭＩＳ及びＰＭＩＳのＦＥＴのゲート電極として金属シリサイド膜を用いる場合を示したが、本実施の形態では、金属シリサイド膜に代えて金属膜を用いるものである。

【００８２】

まず、図３または図５の工程においてＰＭＩＳ領域とＮＭＩＳ領域のＦＥＴを形成した後、図１３（ａ）に示したように、ＰＭＩＳ領域のゲート電極４の上面を覆い、ＮＭＩＳ領域のゲート電極４の上面が露出するようにリソグラフィー法によってフォトレジスト２０からなるエッチングマスクを形成し、ＮＭＩＳ領域のダミーゲート電極をエッチング法で除去する。

【００８３】

次に、フォトレジスト２０を除去した後、図１３（ｂ）に示したように、スパッタ法またはＣＶＤにより、ＮＭＩＳ用の第１の金属膜２１を成膜する。第１の金属膜２１として、例えば、タンタルを成膜する。第１の金属膜２１として、タンタルの他には、ハフニウム、マグネシウム、ジルコニウムまたはアルミニウムを用いることができる。

【００８４】

次に、図１３（ｃ）に示したように、ＣＭＰ法またはエッチバック法により、ＮＭＩＳ領域のゲート電極部のみに第１の金属膜２１を残す。

【００８５】

次に、図１４（ａ）に示したように、ＮＭＩＳ領域の第１の金属膜２１（ゲート電極）の上面を覆い、ＰＭＩＳ領域のゲート電極部の上面が露出するようにリソグラフィー法によってフォトレジスト２０からなるエッチングマスクを形成し、ＰＭＩＳ領域のゲート電極部をエッチング法で除去する。

【００８６】

次に、フォトレジスト２０を除去し、スパッタ法またはＣＶＤにより、ＰＭＩＳ用の第２の金属膜２２、例えば、タングステンを成膜し、図１４（ｂ）に示したように、ＣＭＰ法またはエッチバック法により、ＰＭＩＳ領域のゲート電極部のみに第２の金属膜２２を残す。

【００８７】

なお、第２の金属膜２２は、タングステンの他、ルテニウム、レニウムあるいは白金を用いることができる。

【００８８】

次に、図１４（ｃ）に示したように、ゲート配線６を上記実施の形態１と同様にして形成する。

【００８９】

以上のように、本実施の形態によれば、ＮＭＩＳ領域とＰＭＩＳ領域で異なる材料からなるゲート電極を形成することができるので、仕事関数の異なる第１の金属膜と第２の金属膜をＮＭＩＳ及びＰＭＩＳのＦＥＴのゲート電極として任意に選択することにより、各導電型のＦＥＴの閾値電圧の制御が可能になる。

【００９０】

実施の形態１０．

本実施の形態は、上記実施の形態９において、ゲート絶縁膜として高誘電率膜を形成するものである。

【００９１】

図１５～図１７は本実施の形態の製造工程を示す断面図である。まず、図３または図５の工程においてＰＭＩＳ領域とＮＭＩＳ領域のＦＥＴを形成した後、図１５（ａ）に示したように、ＰＭＩＳ領域のゲート電極８の上面を覆い、ＮＭＩＳ領域のゲート電極の上面が露出するようにリソグラフィー法によってフォトレジスト２０からなるエッチングマスクを形成し、ＮＭＩＳ領域のダミーゲート電極をエッチング法で除去し、さらに、ゲート電極部のゲート絶縁膜をフッ酸等のウェットエッチングまたはＨＦガスによるドライエッチングにより除去する。

【００９２】

次に、フォトレジスト２０を除去した後、図１５（ｂ）に示したように、ＣＶＤ法により、ハフニウムオキサイド膜を１０～５０ｎｍ厚さ成膜して、第１のゲート絶縁膜２３を形成する。

【００９３】

なお、第１のゲート絶縁膜２３は、ハフニウムオキサイドの他、ジルコニウムオキサイド、タンタルオキサイド、アルミニウムオキサイドあるいはこれらとシリコンとの化合物を用いることができる。

【００９４】

また、第１のゲート絶縁膜２３は、高誘電率膜と熱酸化法やプラズマ酸化法によるシリコン酸化膜との積層膜であってもよい。

【００９５】

次に、スパッタ法またはＣＶＤ法により、ＮＭＩＳ用の第１の金属膜を成膜し、図１５（ｃ）に示したように、ＣＭＰ法またはエッチバック法により、ＮＭＩＳ領域のゲート電極部のみに第１の金属膜２１を残す。

【００９６】

次に、ＮＭＩＳ領域の第１の金属膜２１の上面を覆い、ＰＭＩＳ領域のゲート電極４の上面が露出するようにリソグラフィー法によってフォトレジスト２０からなるエッチングマスクを形成し、図１６（ａ）に示したように、ＰＭＩＳ領域のゲート電極４をエッチング法で除去し、さらに、ゲート電極部のゲート絶縁膜をフッ酸等のウェットエッチングまたはＨＦガスによるドライエッチングにより除去する。

【００９７】

次に、フォトレジスト２０を除去し、図１６（ｂ）に示したように、ＣＶＤ法により、ハフニウムオキサイド膜を１０～５０ｎｍ厚さ成膜して、第２のゲート絶縁膜２４を形成する。

【００９８】

なお、第２のゲート絶縁膜２４は、ハフニウムオキサイドの他、ジルコニウムオキサイド、タンタルオキサイド、アルミニウムオキサイドあるいはこれらとシリコンとの化合物を用いることができる。

【００９９】

また、第２のゲート絶縁膜２４は、高誘電率膜と熱酸化法やプラズマ酸化法によるシリコン酸化膜との積層膜であってもよい。

【０１００】

次に、スパッタ法またはＣＶＤにより、ＰＭＩＳ用の第２の金属膜２２，例えば、タングステンを成膜し、図１６（ｃ）に示したように、ＣＭＰ法またはエッチバック法により、ＰＭＩＳ領域のダミーゲート電極部のみに第２の金属膜２２を残す。

【０１０１】

なお、第２の金属膜２２は、タングステンの他、ルテニウム、レニウムあるいは白金を用いることができる。

【０１０２】

次に、図１７に示したように、ゲート配線６を上記実施の形態１と同様にして形成する。

【０１０３】

本実施の形態では、第１のゲート絶縁膜２３及び第２のゲート絶縁膜２４に高誘電率膜を用いているので、第１及び第２のゲート絶縁膜２３，２４の実効的薄膜化が可能になる。

【０１０４】

【発明の効果】

本発明に係る半導体装置によれば、基板上に突出するように形成されたソース領域、チャネル領域及びドレイン領域となるシリコン層と、上記シリコン層表面に形成された絶縁膜と，上記チャネル領域を上記絶縁膜を介して３方向から覆うゲート電極とを有するＦＥＴ，

上記ゲート電極の突出方向の面が露出するように上記シリコン層を埋設する層間絶縁膜、

上記露出したゲート電極の突出方向の面に電気的に接続されたゲート配線を備えたものであるので、ゲート配線の抵抗を任意に低抵抗化することができる。

【０１０５】

また、基板上に突出するように形成されたソース領域、チャネル領域及びドレイン領域となる第１のシリコン層と、上記第１のシリコン層の表面に形成された第１の絶縁膜と、上記第１のシリコン層のチャネル領域を上記第１の絶縁膜を介して３方向から覆う第１のゲート電極とを有するＮＭＩＳ領域のＦＥＴ、

上記基板上に突出するように形成されたソース領域、チャネル領域及びドレイン領域となる第２のシリコン層と、上記第２のシリコン層の表面に形成された第２の絶縁膜と、上記第２のシリコン層のチャネル領域を上記第２の絶縁膜を介して３方向から覆う第２のゲート電極とを有するＰＭＩＳ領域のＦＥＴ、

上記第１及び第２のゲート電極の突出方向面が露出するように上記ＮＭＩＳ領域のＦＥＴ及びＰＭＩＳ領域のＦＥＴを埋設する層間絶縁膜、

上記露出した第１のゲート電極の突出方向の面に電気的に接続されたゲート配線及び第２のゲート電極の突出方向の面に電気的に接続されたゲート配線、を備えたものであるので、ゲート配線の抵抗を任意に低抵抗化することができる。

【０１０６】

本発明に係る半導体装置の製造方法によれば、基板上のシリコン層をパターニングして上記基板上に突出するソース領域、チャネル領域及びドレイン領域を有するＦＥＴを形成する第１の工程、

上記パターニングしたシリコン層表面に絶縁膜を形成する第２の工程、

上記チャネル領域の３方向を上記絶縁膜を介して覆うゲート電極を形成する第３の工程、

層間絶縁膜を成膜する第４の工程、

上記層間絶縁膜を平坦化し、上記ゲート電極の突出方向の面を上記層間絶縁膜から露出させる第５の工程、

導電性膜を成膜し、パターニングして上記露出したゲート電極の突出方向の面と電気的に接続されたゲート配線を形成する第６の工程、を備えたものであるので、ゲート配線の抵抗を任意に低抵抗化することができる。

【０１０７】

また、基板上のシリコン層をパターニングして上記基板上に突出するソース領域、チャネル領域及びドレイン領域を有するＮＭＩＳ領域及びＰＭＩＳ領域のシリコン層を形成する第１の工程、

上記パターニングしたシリコン層表面に絶縁膜を形成しする第２の工程、

上記チャネル領域の３方向を上記絶縁膜を介して覆うポリシリコンまたはアモルファスシリコンからなるゲート電極を形成する第３の工程、

層間絶縁膜を成膜する第４の工程、

上記層間絶縁膜を平坦化し、上記ゲート電極の突出方向の面を上記層間絶縁膜から露出させる第５の工程、

上記ＮＭＩＳ領域またはＰＭＩＳ領域の一方のゲート電極をシリサイド防止膜で被覆し、さらに、第１の金属膜で他方のゲート電極を被覆し、熱処理によって上記第１の金属膜と上記他方のゲート電極のポリシリコンまたはアモルファスシリコンとを反応させて上記他方のゲート電極を金属シリサイドにする第６の工程、

上記シリサイド防止膜を除去して、上記ＮＭＩＳ領域またはＰＭＩＳ領域の上記他方のゲート電極をシリサイド防止膜で被覆し、さらに、上記第１の金属膜とは異なる種類の第２の金属膜で上記一方のゲート電極を被覆し、熱処理によって上記第２の金属膜と上記一方のゲート電極のポリシリコンまたはアモルファスシリコンとを反応させて上記一方のゲート電極を金属シリサイドにする第７の工程、

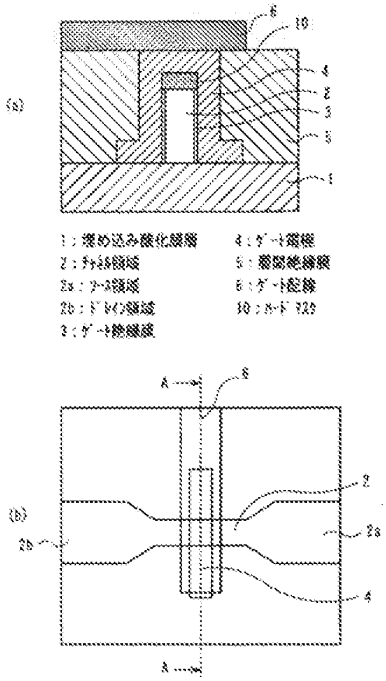
導電性膜を成膜し、パターニングして上記露出した各ゲート電極の突出方向の面と電気的に接続されたゲート配線を形成する第８の工程、を備えたものであるので、ゲート配線及びゲート電極の抵抗を任意に低抵抗化することができる。

【０１０８】
また、基板上のシリコン層をパターニングして上記基板上に突出するソース領域、チャネル領域及びドレイン領域を有するＮＭＩＳ領域及びＰＭＩＳ領域のシリコン層を形成する第１の工程、
上記パターニングしたシリコン層表面に絶縁膜を形成する第２の工程、
上記チャネル領域の３方向を上記絶縁膜を介して覆うポリシリコンまたはアモルファスシリコンからなるダミーゲート電極を形成する第３の工程、
層間絶縁膜を成膜する第４の工程、
上記層間絶縁膜を平坦化し、上記ダミーゲート電極の突出方向の面を上記層間絶縁膜から露出させる第５の工程、
上記ＮＭＩＳ領域のＰＥＴまたはＰＭＩＳ領域の一方のダミーゲート電極を第１のエッチングマスクで被覆し、他方のダミーゲート電極を除去し、上記第１のエッチングマスクを除去し、上記他方のダミーゲート電極を除去した部分に第１の金属膜を埋め込み、ゲート電極を形成する第６の工程、
上記ＮＭＩＳ領域またはＰＭＩＳ領域の上記他方のダミーゲート電極を第２のエッチングマスクで被覆し、上記一方のダミーゲート電極を除去し、上記第２のエッチングマスクを除去し、上記一方のゲート電極を除去した部分に上記第１の金属膜とは異なる種類の第２の金属膜を埋め込み、ゲート電極を形成する第７の工程、
導電性膜を成膜し、パターニングして上記露出した各ゲート電極の突出方向の面と電気的に接続されたゲート配線を形成する第８の工程、を備えたものであるので、ゲート配線及びゲート電極の抵抗を任意に低抵抗化することができる。

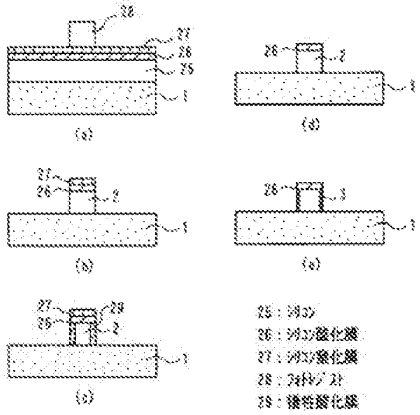
【図面の簡単な説明】
【図１】実施の形態１の半導体装置を示す断面図である。
【図２】実施の形態１の半導体装置の製造工程を示す断面図である。
【図３】実施の形態１の半導体装置の製造工程を示す断面図である。
【図４】実施の形態２の半導体装置の製造工程を示す断面図である。
【図５】実施の形態３の半導体装置の製造工程を示す断面図である。
【図６】実施の形態４の半導体装置の製造工程を示す断面図である。
【図７】実施の形態４の半導体装置の製造工程を示す断面図である。
【図８】実施の形態５の半導体装置の製造工程を示す断面図である。
【図９】実施の形態６の半導体装置の製造工程を示す断面図である。
【図１０】実施の形態７の半導体装置の製造工程を示す断面図である。
【図１１】実施の形態８の半導体装置の製造工程を示す断面図である。
【図１２】実施の形態８の半導体装置の製造工程を示す断面図である。
【図１３】実施の形態９の半導体装置の製造工程を示す断面図である。
【図１４】実施の形態９の半導体装置の製造工程を示す断面図である。
【図１５】実施の形態１０の半導体装置の製造工程を示す断面図である。
【図１６】実施の形態１０の半導体装置の製造工程を示す断面図である。
【図１７】実施の形態１０の半導体装置の製造工程を示す断面図である。

【符号の説明】
１　埋込み酸化層、２　チャネル領域、２ａ　ソース領域、
２ｂ　ドレイン領域、３，１５　ゲート絶縁膜、４　ゲート電極、
５，１４　層間絶縁膜、６　ゲート配線，７，１２　金属膜、
８　ポリシリコン、９　金属シリサイド、１０　ハードマスク、
１１，２０，２４，２８　フォトレジスト、１２ａ　ＴｉＮ膜、１２ｂ　Ｗ膜、
１３　高誘電率膜、１６　シリサイド防止膜、１７，２１　第１の金属膜、
１８　第１の金属シリサイド、１９　第２の金属シリサイド、
２２　第２の金属膜、２３　第１のゲート絶縁膜、２４　第２のゲート絶縁膜、
２５　シリコン，２６　シリコン酸化膜、２７　シリコン窒化膜、
２９　犠牲酸化膜。

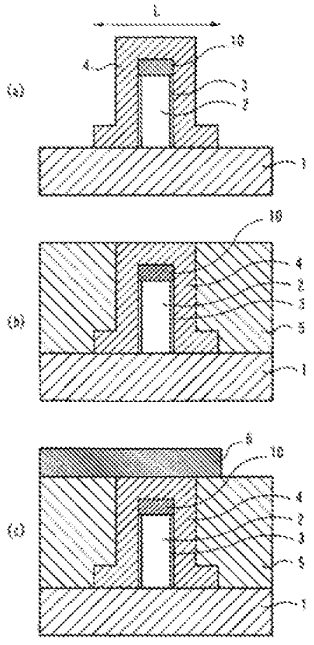
【図１】



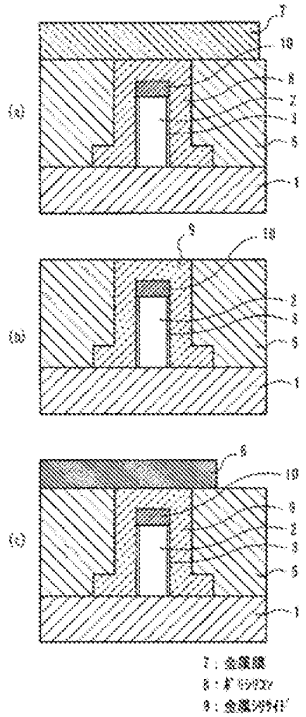
【図２】



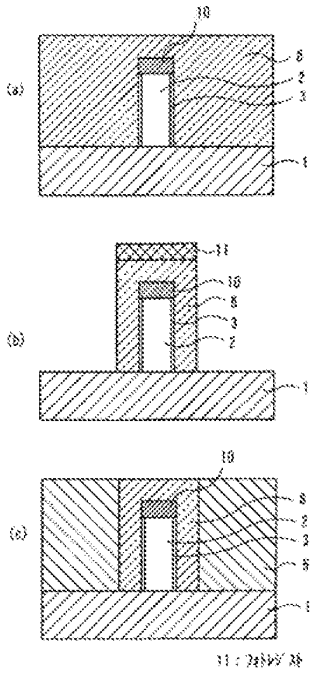
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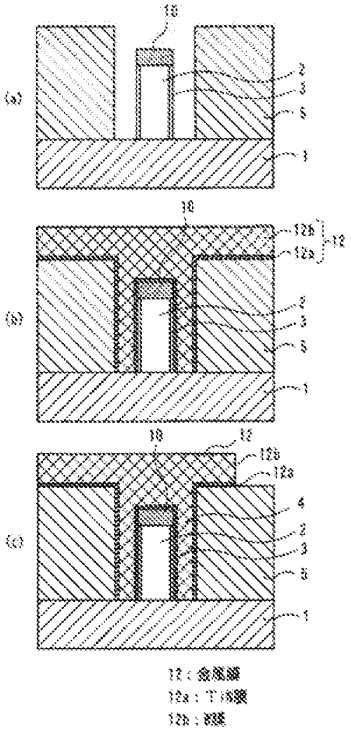
【図４】



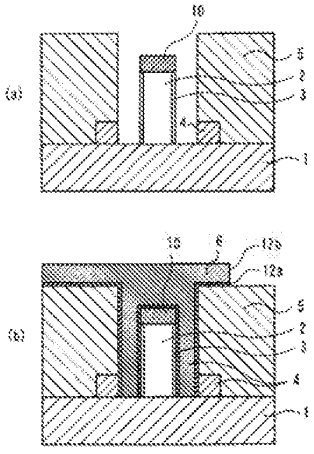
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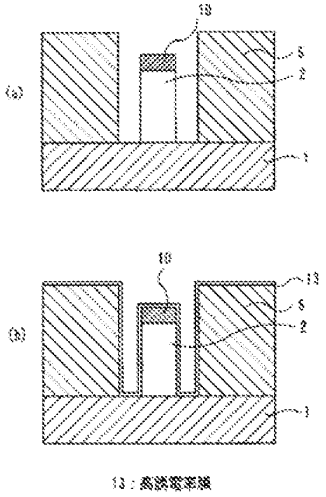
【図６】



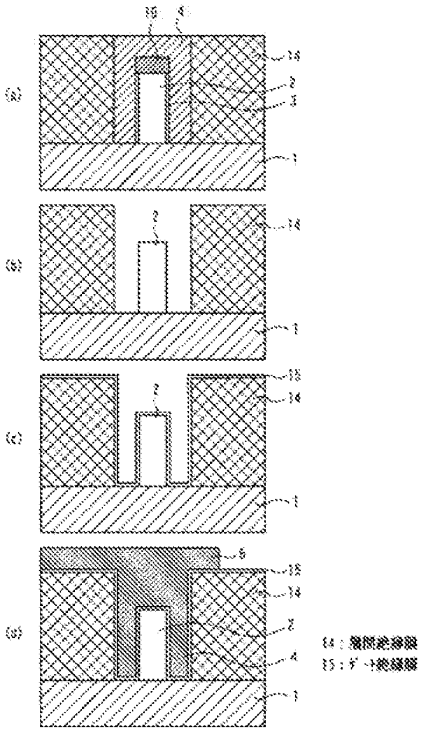
【図７】



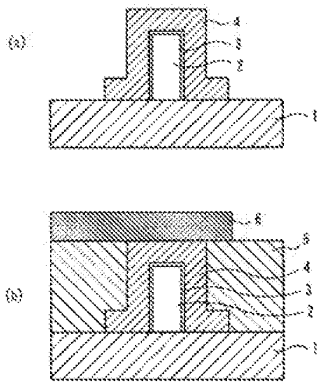
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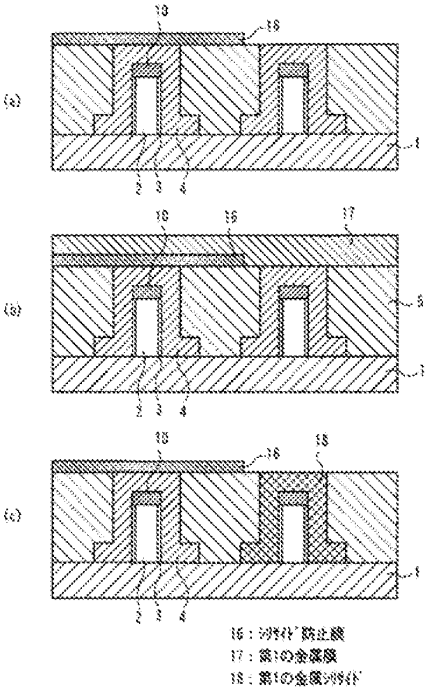
【図９】



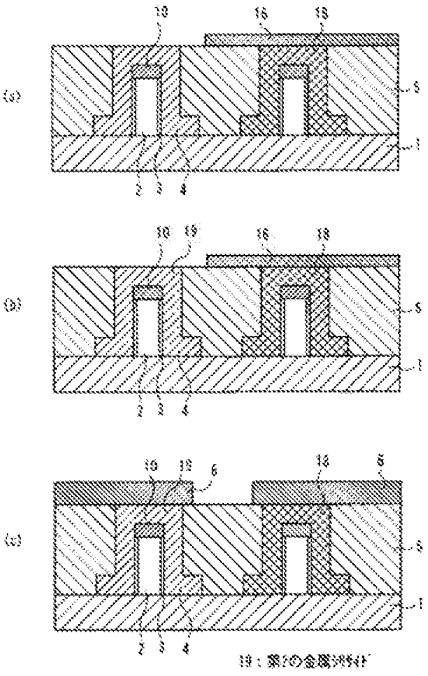
【図１０】



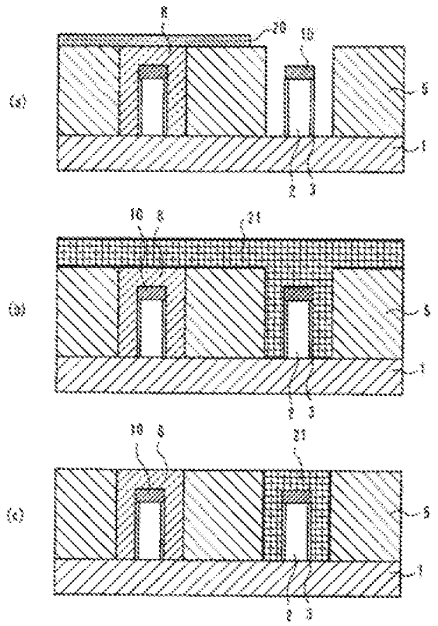
【図１１】



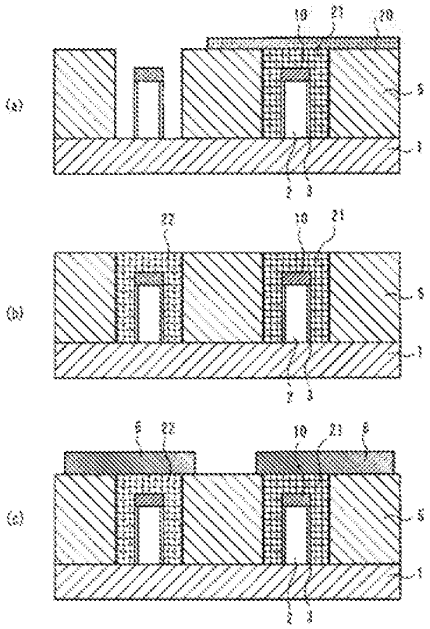
【図１２】



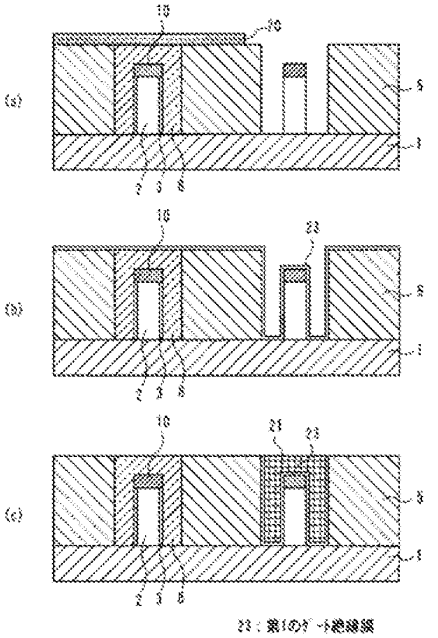
【図１３】



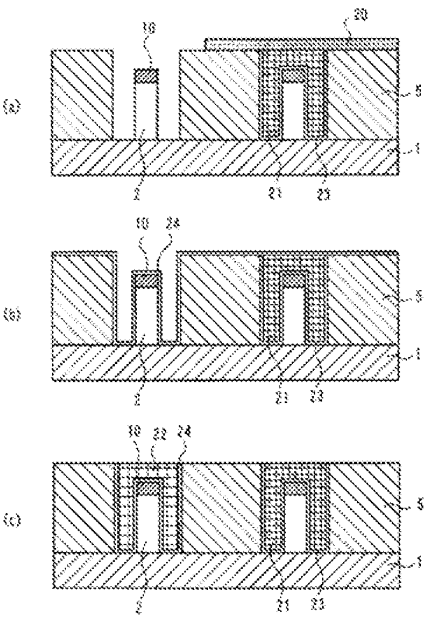
【図１４】



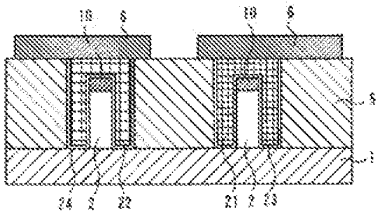
【図１５】



【図１６】



【図１７】



フロントページの続き

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H01L 27/092	H01L 27/08	321D	
H01L 29/423	H01L 27/08	102C	
H01L 29/49	H01L 29/58	G	

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BB21 BB22 BB24 BB25 BB27 BB30 CC05 DD33 DD43 DD63
DD75 DD84 EE03 EE09 EE16 FF01 FF18 GG09 GG10 GG14
HH16
5F048 AA01 AC01 AC03 BA02 BA16 BB05 BB08 BB09 BB10 BB11
BB12 BB15 BB06 BD07 BD09 BF15
5F110 AA03 AA08 BB04 CC09 CC10 DD05 DD13 EE01 EE02 EE04
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FF01 FF02 FF03 FF23 FF25 GG02 GG22 GG25 GG28 GG29
HL01 HL02 HL04 HL05 HL06 HL11 HL22 HL23 HL24 NN02
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Ｈ０１Ｌ　29/423	*(2006.01)*	Ｈ０１Ｌ	29/78	６１７Ｋ	５Ｆ０４８
Ｈ０１Ｌ　29/49	*(2006.01)*	Ｈ０１Ｌ	29/78	６１８Ｃ	５Ｆ１１０
Ｈ０１Ｌ　21/28	*(2006.01)*	Ｈ０１Ｌ	29/78	６１６Ｔ	

審査請求　未請求　請求項の数12　ＯＬ　（全20頁）　最終頁に続く

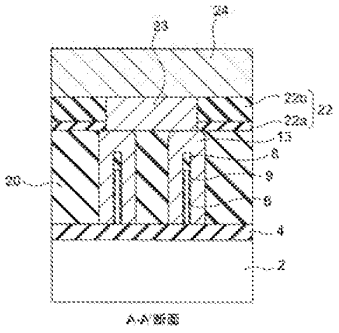
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最終頁に続く

(54)【発明の名称】マルチゲート型電界効果トランジスタおよびその製造方法

(57)【要約】
【課題】平坦化工程を行っても、金属汚染を防止することのできるマルチゲート型電界効果トランジスタおよびその製造方法を提供することを可能にする。
【解決手段】基板２上に並列するように設けられた第１導電型の複数の半導体層６と、複数の半導体層のそれぞれに、離間して設けられた第２導電型のソース／ドレイン領域６０ａ、６０ｂと、複数の半導体層のそれぞれに、ソース領域とドレイン領域との間に設けられるチャネル領域と、チャネル領域のそれぞれの上面に設けられた保護膜８と、チャネル領域のそれぞれの両側面に設けられたゲート絶縁膜９と、チャネル領域のそれぞれの両側面にゲート絶縁膜を挟むように設けられるとともにチャネル領域のそれぞれの上面に保護膜を挟むように設けられた金属元素を含む複数のゲート電極１０と、複数のゲート電極のそれぞれの側面を覆うように基板上に設けられた層間絶縁膜２０と、複数のゲート電極のそれぞれの上面を共通に接続する接続部２３と、接続部に接続されたゲート配線２４と、を備えている。
【選択図】図１７



【特許請求の範囲】
【請求項１】
基板上に複数の半導体層を並列して形成する工程と、
前記複数の半導体層の上面にそれぞれ保護膜を形成する工程と、
前記複数の半導体層のそれぞれに、各半導体層の両側面、前記保護膜の両側面および上面を覆う第１絶縁層を形成する工程と、
全面に第１層間絶縁膜を形成し、前記第１層間絶縁膜を平坦化することによって前記第１絶縁層それぞれの上面を露出させる工程と、
前記第１絶縁層をそれぞれ選択的に除去することによって前記第１絶縁層が除去された位置に複数の穴を形成する工程と、
複数の前記穴内の前記半導体層の両側面にゲート絶縁膜を形成する工程と、
複数の前記穴を埋め込むように第１ポリシリコン膜を全面に堆積する工程と、
前記第１ポリシリコン膜を平坦化することによって前記第１層間絶縁膜の上面を露出させるとともに前記第１ポリシリコン膜を複数の第２ポリシリコン膜に分離する工程と、
複数の前記第２ポリシリコン膜上にゲート電極形状のマスクを形成する工程と、
前記マスクを用いて複数の前記第２ポリシリコン膜をパターニングする工程と、
パターニングされた複数の前記第２ポリシリコン膜をゲート長方向に挟む絶縁体からなる側壁を形成する工程と、
前記マスクおよび前記側壁を用いて前記保護膜をパターニングし、複数の前記半導体層の上面を選択的に露出させる工程と、
選択的に露出した複数の半導体層に不純物を注入し、ソース／ドレイン領域を形成する工程と、
前記マスクを除去して複数の前記第２ポリシリコン膜の上面を露出させる工程と、
上面が露出された複数の前記第２ポリシリコン膜をそれぞれシリサイドに変える工程と、
全面に第２層間絶縁膜を形成し、前記シリサイドのそれぞれに通じる開口を前記第２層間絶縁膜に形成し、前記開口を埋め込むことにより前記シリサイドのそれぞれと共通に接続する金属の接続部を形成する工程と、
前記接続部に接続する配線を形成する工程と、
を備えていることを特徴とするマルチゲート型電界効果トランジスタの製造方法。
【請求項２】
基板上に複数の半導体層を並列して形成する工程と、
前記複数の半導体層の上面にそれぞれ保護膜を形成する工程と、
前記複数の半導体層のそれぞれに、各半導体層の側面、前記保護膜の側面および上面を覆う第１絶縁層を形成する工程と、
全面に第１層間絶縁膜を形成し、前記第１層間絶縁膜を平坦化することによって前記第１絶縁層それぞれの上面を露出させる工程と、
前記第１絶縁層をそれぞれ選択的に除去することによって前記第１絶縁層が除去された位置に複数の穴を形成する工程と、
複数の前記穴それぞれの中の前記半導体層の両側面にゲート絶縁膜を形成する工程と、
複数の前記穴のそれぞれの側面および底面と、前記穴内の前記ゲート絶縁膜ならびに前記保護膜とを覆うゲート金属膜を形成する工程と、
前記ゲート金属膜を覆うポリシリコン膜を形成する工程と、
複数の前記穴それぞれの中の前記ポリシリコン膜および前記ゲート金属膜を，前記保護膜上の前記ゲート金属膜が露出しないように、エッチングする工程と、
その後，複数の前記穴をそれぞれ埋め込むように再度ポリシリコン膜を堆積する工程と、
前記ポリシリコン膜を平坦化することにより前記第１層間絶縁膜の上面を露出させるとともに前記ポリシリコン膜を複数のポリシリコン層に分離する工程と，
複数の前記ポリシリコン層上にゲート電極形状のマスクを形成する工程と、

前記マスクを用いて複数の前記ポリシリコン層をパターニングする工程と、
パターニングされた複数の前記ポリシリコン層をゲート長方向に挟む絶縁体からなる側壁を形成する工程と、
前記側壁を用いて前記保護膜をパターニングし、複数の前記半導体層の上面を選択的に露出させる工程と、
選択的に露出した複数の半導体層に不純物を注入し、ソース／ドレイン領域を形成する工程と、
前記マスクを除去して複数の前記ポリシリコン層のそれぞれの上面を露出させる工程と、
全面に第２層間絶縁膜を形成し、複数の前記ポリシリコン層のそれぞれに通じる開口を前記第２層間絶縁膜に形成し、前記開口を埋め込むことにより前記ポリシリコン層のそれぞれと共通に接続する金属の接続部を形成する工程と、
前記接続部に接続する配線を形成する工程と、
を備えていることを特徴とするマルチゲート型電界効果トランジスタの製造方法。
【請求項３】
前記ソース／ドレイン領域を形成する前に、露出した前記半導体層を選択的にエッチングし、前記基板からの高さを低くする工程を更に備えていることを特徴とする請求項１または２記載のマルチゲート型電界効果トランジスタの製造方法。
【請求項４】
前記ソース／ドレイン領域を形成する工程は、前記基板の表面に垂直な方向から傾いた角度で前記不純物を注入することを特徴とする請求項１乃至３のいずれかに記載のマルチゲート型電界効果トランジスタの製造方法。
【請求項５】
基板上に並列するように設けられた第１導電型の複数の半導体層と、
前記複数の半導体層のそれぞれに、離間して設けられた第２導電型のソース／ドレイン領域と、
前記複数の半導体層のそれぞれに、前記ソース領域と前記ドレイン領域との間に設けられるチャネル領域と、
前記チャネル領域のそれぞれの上面に設けられた保護膜と、
前記チャネル領域のそれぞれの両側面に設けられたゲート絶縁膜と、
前記チャネル領域のそれぞれの両側面に前記ゲート絶縁膜を挟むように設けられるとともに前記チャネル領域のそれぞれの上面に前記保護膜を挟むように設けられた金属元素を含む複数のゲート電極と、
複数の前記ゲート電極のそれぞれの側面を覆うように前記基板上に設けられた層間絶縁膜と、
複数の前記ゲート電極のそれぞれの上面を共通に接続する接続部と、
前記接続部に接続されたゲート配線と、
を備えていることを特徴とするマルチゲート型電界効果トランジスタ。
【請求項６】
複数の前記ゲート電極はそれぞれシリサイドで形成されていることを特徴とする請求項５記載のマルチゲート型電界効果トランジスタ。
【請求項７】
前記層間絶縁膜の上面と、複数の前記ゲート電極のそれぞれの上面は略同一平面に位置することを特徴とする請求項６記載のマルチゲート型電界効果トランジスタ。
【請求項８】
複数の前記ゲート電極のそれぞれは、金属膜と、この金属膜を覆うポリシリコン膜との積層構造を有し、前記金属膜は、前記層間絶縁膜、前記基板の上面、前記ゲート絶縁膜、および前記保護膜のそれぞれと前記ポリシリコン膜との間に設けられていることを特徴とする請求項５記載のマルチゲート型電界効果トランジスタ。
【請求項９】

前記ポリシリコン膜と前記層間絶縁膜との間に設けられた金属膜部分の上端の前記基板からの高さは、前記保護膜上に位置する前記金属膜の上面の前記基板からの高さよりも高いことを特徴とする請求項８記載のマルチゲート型電界効果トランジスタ。
【請求項１０】
前記ポリシリコン膜の上面は，前記層間絶縁膜の上面と略同一平面に位置することを特徴とする請求項８または９記載のマルチゲート型電界効果トランジスタ。
【請求項１１】
前記ソース／ドレイン領域の上面の前記基板からの高さは、前記チャネル領域の上面の前記基板からの高さよりも低いことを特徴とする請求項５乃至１０のいずれかに記載のマルチゲート型電界効果トランジスタ。
【請求項１２】
前記基板はＳＯＩ基板であり，前記半導体層は、ＳＯＩ層であることを特徴とする請求項５乃至１１のいずれかに記載のマルチゲート型電界効果トランジスタ。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、マルチゲート型電界効果トランジスタおよびその製造方法に関する。
【背景技術】
【０００２】
ＬＳＩの高集積化と高性能化は、その基本構成素子である電界効果トランジスタ（ＦＥＴ(Field Effect Transistor)）の微細化とそれに伴う性能向上によって実現されてきた。ＦＥＴの性能はオン動作時の駆動電流の大きさとオフ時のチャネルのリーク電流の小ささで決定される。国際半導体ロードマップによると４５ｎｍ世代以降においては大駆動電流、小リーク電流を達成するために複数のブレークスルー技術が必要とされている。
【０００３】
リーク電流の低減に関しては，短チャネル効果に対する耐性が高いことから、チャネル領域を完全空乏化したＦＤ(Fully-Depleted)デバイスが次世代の基本素子構造として期待されている。中でも注目されているのは，マルチゲート型電界効果トランジスタである。例えば特許文献１に示されているようなチャネルの表面上に形成されたゲート電極のみで一方向からチャネル内のポテンシャルを制御するシングルゲート型電界効果トランジスタと異なり、マルチゲート型電界効果トランジスタは、微小なチャネル領域をゲート電極で取り囲む構造を有している。その構造の利点は、チャネル領域のポテンシャルの制御性を高め、デバイスの短チャネル化によるポテンシャル障壁の低下を抑え，オフ時のリーク電流を低減できることである。
【０００４】
ここで、重要となるのは，デバイスのしきい値制御である。ＦＤデバイスはバルク型のデバイスと比較して、反転電荷が生成される電圧が低いという特徴がある。このため、従来のゲート電極材料をＦＤデバイスに用いるとオフ状態（０ボルト）でのリーク電流が大きくなり過ぎ、新たなゲート電極材料が必要となる。現在，その候補として挙げられているのは、金属そのものをゲート電極として用いるタイプ（メタルゲート）と、金属と半導体の化合物（半導体がシリコンの場合シリサイドと呼ぶ）を用いるタイプ（シリサイドゲート）である。
【特許文献１】特開２００５－８６０２４号公報
【発明の開示】
【発明が解決しようとする課題】
【０００５】
このメタルゲートとシリサイドゲートを立体形マルチゲート電界効果トランジスタに適用する場合には幾つかの製造プロセス上の課題がある。特に、問題になるのは、金属汚染である。極微細なゲート長を実現するためには、ゲート電極の加工前のリソグラフィには十分平坦な表面が必要となる。しかしながら、メタルゲートやシリサイドに用いられる金

層が、母体半導体（シリコン等）やゲート絶縁膜に取り込まれると、キャリアの生成再結合の中心や電荷トラップまたはリーク電流のパスになり得るため、デバイスの性能を著しく劣化させる恐れがある。従って、メタルゲート電極やシリサイド電極に対して、ＣＭＰ(Chemical Mechanical Polishing)を用いて直接に平坦化することはできない。また、ゲート電極をシリサイド化する際に自然酸化膜の存在が障害となるが、従来の製造方法では、この自然酸化膜を取り除くことができない。

【０００６】

本発明は、上記事情を考慮してなされたものであって、平坦化工程を行っても、金属汚染を防止することが可能なマルチゲート型電界効果トランジスタおよびその製造方法を提供することを目的とする。

【課題を解決するための手段】

【０００７】

本発明の第１の態様によるマルチゲート型電界効果トランジスタの製造方法は、基板上に複数の半導体層を並列して形成する工程と、前記複数の半導体層の上面にそれぞれ保護膜を形成する工程と、前記複数の半導体層のそれぞれに、各半導体層の両側面、前記保護膜の両側面および上面を覆う第１絶縁層を形成する工程と、全面に第１層間絶縁膜を形成し、前記第１層間絶縁膜を平坦化することによって前記第１絶縁層それぞれの上面を露出させる工程と、前記第１絶縁層をそれぞれ選択的に除去することによって前記第１絶縁層が除去された位置に複数の穴を形成する工程と、複数の前記穴内の前記半導体層の両側面にゲート絶縁膜を形成する工程と、複数の前記穴を埋め込むように第１ポリシリコン膜を全面に堆積する工程と、前記第１ポリシリコン膜を平坦化することによって前記第１層間絶縁膜の上面を露出させるとともに前記第１ポリシリコン膜を複数の第２ポリシリコン膜に分離する工程と、　複数の前記第２ポリシリコン膜上にゲート電極形状のマスクを形成する工程と、前記マスクを用いて複数の前記第２ポリシリコン膜をパターニングする工程と、パターニングされた複数の前記第２ポリシリコン膜をゲート長方向に挟む絶縁体からなる側壁を形成する工程と、前記マスクおよび前記側壁を用いて前記保護膜をパターニングし、複数の前記半導体層の上面を選択的に露出させる工程と、選択的に露出した複数の半導体層に不純物を注入し、ソース／ドレイン領域を形成する工程と、前記マスクを除去して複数の前記第２ポリシリコン膜の上面を露出させる工程と、上面が露出された複数の前記第２ポリシリコン膜をそれぞれシリサイドに変える工程と、全面に第２層間絶縁膜を形成し、前記シリサイドのそれぞれに通じる開口を前記第２層間絶縁膜に形成し、前記開口を埋め込むことにより前記シリサイドのそれぞれと共通に接続する金属の接続部を形成する工程と、前記接続部に接続する配線を形成する工程と、を備えていることを特徴とする。

【０００８】

また、本発明の第２の態様によるマルチゲート型電界効果トランジスタの製造方法は、基板上に複数の半導体層を並列して形成する工程と、前記複数の半導体層の上面にそれぞれ保護膜を形成する工程と、前記複数の半導体層のそれぞれに、各半導体層の側面、前記保護膜の側面および上面を覆う第１絶縁層を形成する工程と、全面に第１層間絶縁膜を形成し、前記第１層間絶縁膜を平坦化することによって前記第１絶縁層それぞれの上面を露出させる工程と、前記第１絶縁層をそれぞれ選択的に除去することによって前記第１絶縁層が除去された位置に複数の穴を形成する工程と、複数の前記穴それぞれの中の前記半導体層の両側面にゲート絶縁膜を形成する工程と、複数の前記穴のそれぞれの側面および底面と、前記穴内の前記ゲート絶縁膜ならびに前記保護膜とを覆うゲート金属膜を形成する工程と、前記ゲート金属膜を覆うポリシリコン膜を形成する工程と、複数の前記穴それぞれの中の前記ポリシリコン膜および前記ゲート金属膜を、前記保護膜上の前記ゲート金属膜が露出しないように、エッチングする工程と、その後、複数の前記穴をそれぞれ埋め込むように再度ポリシリコン膜を堆積する工程と、前記ポリシリコン膜を平坦化することにより前記第１層間絶縁膜の上面を露出させるとともに前記ポリシリコン膜を複数のポリシリコン層に分離する工程と、複数の前記ポリシリコン層上にゲート電極形状のマスクを形

成する工程と、前記マスクを用いて複数の前記ポリシリコン層をパターニングする工程と、パターニングされた複数の前記ポリシリコン層をゲート長方向に挟む絶縁体からなる側壁を形成する工程と、前記側壁を用いて前記保護膜をパターニングし、複数の前記半導体層の上面を選択的に露出させる工程と、選択的に露出した複数の半導体層に不純物を注入し、ソース／ドレイン領域を形成する工程と、前記マスクを除去して複数の前記ポリシリコン層のそれぞれの上面を露出させる工程と、全面に第２層間絶縁膜を形成し、複数の前記ポリシリコン層のそれぞれに通じる開口を前記第２層間絶縁膜に形成し、前記開口を埋め込むことにより前記ポリシリコン層のそれぞれと共通に接続する金属の接続部を形成する工程と、前記接続部に接続する配線を形成する工程と、を備えていることを特徴とする。

【０００９】

また、本発明の第３の態様によるマルチゲート型電界効果トランジスタは、基板上に並列するように設けられた第１導電型の複数の半導体層と、前記複数の半導体層のそれぞれに、離間して設けられた第２導電型のソース／ドレイン領域と、前記複数の半導体層のそれぞれに、前記ソース領域と前記ドレイン領域との間に設けられるチャネル領域と、前記チャネル領域のそれぞれの上面に設けられた保護膜と、前記チャネル領域のそれぞれの両側面に設けられたゲート絶縁膜と、前記チャネル領域のそれぞれの両側面に前記ゲート絶縁膜を挟むように設けられるとともに前記チャネル領域のそれぞれの上面に前記保護膜を挟むように設けられた金属元素を含む複数のゲート電極と、複数の前記ゲート電極のそれぞれの側面を覆うように前記基板上に設けられた層間絶縁膜と、複数の前記ゲート電極のそれぞれの上面を共通に接続する接続部と、前記接続部に接続されたゲート配線と、を備えていることを特徴とする。

【発明の効果】

【００１０】

本発明によれば、平坦化工程を行っても、金属汚染を防止することが可能なマルチゲート型電界効果トランジスタおよびその製造方法を提供することができる。

【発明を実施するための最良の形態】

【００１１】

本発明の実施形態によるマルチゲート型電界効果トランジスタを説明する前に、このマルチゲート型電界効果トランジスタの特徴をより明確にするために、従来の問題点について図１Ａ～図６Ｂを参照して詳細に説明する。以下の説明では、ｎ型チャネルトランジスタを例にとって説明するが、ｐ型チャネルトランジスタにも適用できる。

【００１２】

図１Ａ、１Ｂ、１Ｃに示すように、支持基板２上に絶縁膜４が形成され、絶縁膜４上にＳＯＩ層６が形成されたＳＯＩ基板上に、チャネルの保護膜８として窒化シリコンをＬＰＣＶＤ(Low Pressure Chemical Vapor Deposition)などで１００ｎｍ程度堆積し、公知の素子分離技術によって、素子分離を行う。更に、既存のパターニング技術により、ＳＯＩ層６をパターニングし、チャネルを形成する。チャネル幅は例えば２０ｎｍである。なお、図１Ａは平面図、図１Ｂは図１Ａに示す切断線Ａ－Ａ’で切断したときの断面図、図１Ｃは図１Ａに示す切断線Ｂ－Ｂ’で切断したときの断面図である。

【００１３】

次いで、図２Ａ、２Ｂ、２Ｃに示すように、ゲート絶縁膜９として、１ｎｍほど二酸化シリコンをＲＴＯ(Rapid Thermal Oxidation)法などを用いて形成し、その後、プラズマ窒化して誘電率を大きくする。さらにゲート電極となるポリシリコン膜１０ＡをＬＰＣＶＤなどで２５０ｎｍ堆積する。ここで、表面を平坦化するために、窒化シリコン膜８をエッチングストッパーとしてＣＭＰを行い、再度ポリシリコン膜１０Ｂを６０ｎｍ堆積する。この時、先に形成したポリシリコン膜１０Ａの表面に自然酸化膜１００が形成されてしまう。なお、図２Ａは平面図、図２Ｂは図２Ａに示す切断線Ａ－Ａ’で切断したときの断面図、図２Ｃは図２Ａに示す切断線Ｂ－Ｂ’で切断したときの断面図である。

【００１４】

続いて、図３Ａ、３Ｂ、３Ｃに示すように、その上に窒化シリコン膜からなるハードマスク層（図示せず）を堆積する。そして、フォトリソグラフィ技術などを用いて上記ハードマスク層をパターニングする。その後、パターニングされたハードマスク層をマスクとしてＲＩＥ等でポリシリコン膜１０Ｂをパターニングするとゲート電極部分が形成される。ここで、さらにオフセットスペーサーなどを形成する場合もあるが図示していない。

【００１５】

このゲート電極の形成においてゲート長が５０ｎｍ以下のパターニングをフォトリソグラフィで行うためには、十分平坦な表面が必要となる。そのために、図２Ａ、２Ｂ、２Ｃに用いたようなＣＭＰ工程が用いられるが、フルシリサイドゲートやメタルゲートを適用しようとするとプロセス上の問題が発生する。例えば、フルシリサイドゲートの場合、図４Ａに示すように、ポリシリコン膜１０Ｂ上に金属（例えば、Ｎｉ等）１１をスパッタにより堆積し、４００℃～５００℃で熱処理することによりポリシリコン膜１０Ｂをシリサイド化する。しかし、図４（Ｂ）に示すように、自然酸化膜１００が均一に形成されていないため、自然酸化膜１００が形成されている領域では、自然酸化膜１００が金属１１の拡散のバリアとなり、自然酸化膜１００より下に位置するポリシリコン膜１０Ａの領域ではシリサイド化の反応が不均一となってしまう。その結果、図４Ｂに示すように、シリサイドとなる部分１３とポリシリコン膜１０Ａのまま残ってしまう部分とに分かれる。この場合、図４Ｂにおいて左に位置するチャネル６を有するトランジスタにおいては、チャネル６の両側はシリサイド１３となるので、チャネル６の両側のしきい値は揃う。しかし、右に位置するチャネル６を有するトランジスタにおいては、チャネル６の左側はシリサイド１３、右側はポリシリコン膜１０Ａとなるので、ポリシリコンとシリサイドの仕事関数の差だけしきい値が異なる状態になる。

【００１６】

ＬＳＩにおいては、トランジスタ間のしきい値のバラツキは深刻な問題となるため、個々のトランジスタの複数のチャネルにおいてしきい値が異なるのは致命的な欠点である。また、このような状態では、ゲート電極の抵抗にもバラツキを生じ、高周波動作時において障害となる。

【００１７】

一方、ゲート電極にメタルを用いた場合は、図５Ａに示すように、チャネル領域となる半導体層６を囲むようにメタル電極１７とポリシリコン膜１０を堆積後、層間絶縁膜１８を堆積すると、層間絶縁膜１８の上面が凹凸形状となるため、微細なリソグラフィを行うためには、図５Ｂに示すように平坦化する必要がある。このとき平坦化に、ＣＭＰ法を用いたときのストッパーは窒化シリコン膜８しかない構造になっているため、メタル電極１７までエッチングされてしまう。ＣＭＰ法によってメタル電極１７をエッチングすると、メタルの粒子をウェハ全面に引き伸ばしてしまい、ウェハを金属で汚染することになる。このことは、ＬＳＩ製造上、到底許容できない。したがって、メタルゲートを用いた場合は、平坦化を行わず、ゲート電極のリソグラフィを行わなければならず、微小なゲートを形成することができないという問題がある。

【００１８】

本発明者達は、鋭意研究に努めた結果、これらの問題を解決するマルチゲート型電界効果トランジスタを得ることができた。これを以下に、実施形態として説明する。

【００１９】

（第１実施形態）

本発明の第１実施形態によるマルチゲート型電界効果トランジスタの平面図を図６に示す。本実施形態のマルチゲート型電界効果トランジスタは、図６に示すように、２本のフィン５０１、５０２と、これらのフィンの一方の端部に形成されたｎ型のソース領域６０ａおよび他方の端部に形成されたｎ型のドレイン領域６０ｂと、２本のフィン５０１，５０２とを跨ぐように形成されたゲート７０とを備えている。フィン５０１，５０２のそれぞれは、チャネル領域となるｐ型の半導体層と、このチャネル領域の側面に形成されたゲート絶縁膜と、上記半導体層の上面に形成された保護膜と、を備えている。なお、各フィ

ンのチャネル領域の両側の半導体層にはｎ型半導体層が形成され、これらのｎ型半導体層はｎ型ソース領域６０ａまたはｎ型ドレイン領域６０ｂに接続されており、ｎ型ソース領域６０ａまたはｎ型ドレイン領域６０ｂとも呼ばれる。ゲート７０はチャネル領域上のゲート絶縁膜を覆うように形成される。

【００２０】

次に、本実施形態のマルチゲート型電界効果トランジスタの製造方法を図７Ａ乃至図１９Ｄを参照して説明する。本実施形態では、ｎ型チャネル電界効果トランジスタについて説明するが、イオン注入するイオン種を変えるなどすればｐ型チャネル電界効果トランジスタについても同様に作製できる。図７Ａ，図８Ａ，図９Ａ，図１０Ａ，図１１Ａ，図１２Ａ，図１３Ａ，図１４Ａ，図１５，図１６，図１７，図１８，図１９Ａは、図６に示す切断線Ａ－Ａ’で切断した断面図、図７Ｂ，図８Ｂ，図９Ｂ，図１０Ｂ，図１１Ｂ，図１２Ｂ，図１３Ｂ，図１４Ｂ，図１９Ｂは、図６に示す切断線Ｂ－Ｂ’で切断した断面図、図７Ｃ，図８Ｃ，図９Ｃ，図１０Ｃ，図１１Ｃ，図１２Ｃ，図１３Ｃ，図１４Ｃ，図１９Ｃは、図６に示す切断線Ｃ－Ｃ’で切断した断面図、図７Ｄ，図８Ｄ，図９Ｄ，図１０Ｄ，図１１Ｄ，図１２Ｄ，図１３Ｄ，図１４Ｄ，図１９Ｄは、図６に示す切断線Ｄ－Ｄ’で切断した断面図である。

【００２１】

まず、図７Ａ、７Ｂ、７Ｃ、７Ｄに示すように、支持基板２上に絶縁膜４が形成され、絶縁膜４上にＳＯＩ層６が形成されたＳＯＩ基板上に、チャネルの保護膜８として窒化シリコンをＬＰＣＶＤ(Low Pressure Chemical Vapor Deposition)などで１００ｎｍ程度堆積し、この保護膜８上に例えばＴＥＯＳ(Tetra Ethyl Ortho Silicate)からなる絶縁膜１９を堆積する。その後、公知の素子分離技術によって、素子分離を行う。更に、既存のパターニング技術により、ＳＯＩ層６をパターニングし、チャネルを形成する。チャネル幅は例えば２０ｎｍである。チャネル６の上面には保護膜８と、絶縁膜１９とが形成されている。

【００２２】

次に、図８Ａ、８Ｂ、８Ｃ、８Ｄに示すように、絶縁膜１９を更に堆積し、ＲＩＥによりエッチングすることによりチャネル６および保護膜８の側面に絶縁膜１９からなる側壁１９ａを形成する。この側壁となる絶縁膜１９ａは、保護膜８の上面も覆っている。この作業を数回繰り返すことにより、側壁１９ａの幅（チャネル６の側面からこの側面に直交する方向の側壁の厚さ）をできるだけ厚く（例えば５０ｎｍ～１００ｎｍ）、高さ（保護膜８からの高さ）をできるだけ高く（例えば３００ｎｍ）する。このとき、側壁１９ａとなる絶縁膜１９ａは、上面が丸まった形状となっている。

【００２３】

続いて、図９Ａ、９Ｂ、９Ｃ、９Ｄに示すように、側壁となる絶縁膜１９ａを覆うように絶縁膜２０を堆積し、この絶縁膜２０をＣＭＰにより平坦化することにより、絶縁膜１９ａの上面を露出させる。このとき、絶縁膜１９ａの上面でエッチングを止めるのではなく、多少オーバーエッチングすることにより、絶縁膜１９ａの頂上付近の丸まった部分を削り、開口部を広くする。

【００２４】

次に、図１０Ａ、１０Ｂ、１０Ｃ、１０Ｄに示すように、チャネル６および保護膜８の側面ならびに上面を覆っている絶縁膜１９ａを例えば溶液でエッチングすることにより完全に除去し、穴を形成する。このとき、希ＨＦなどを用いると絶縁膜４まで多少エッチングされるが、絶縁膜４の厚さが１μｍなどの場合は、希ＨＦによるＴＥＯＳ（絶縁膜１９ａの材料）とシリコン熱酸化膜（絶縁膜４）とのエッチングレートの違いを利用し、エッチング時間を調整することで、絶縁膜４を十分な厚さとなるように残すことができる。その後、上記穴が形成された状態で、チャネル領域６の側面に、ゲート絶縁膜９となる膜厚が１ｎｍほど二酸化シリコンを例えばＲＴＯ法を用いて形成し、その後、プラズマ窒化をしてゲート絶縁膜９の誘電率を大きくする。更にゲート電極となるポリシリコン膜１０をＬＰＣＶＤなどで堆積する。このとき、ＬＰＣＶＤの炉の温度を低く設定し、反応律速に

よりポリシリコンを堆積することにより上記穴を完全に埋め込む。これは、高温で堆積させると原料の供給律速によりポリシリコン膜が形成されてしまい、絶縁膜２０上に優先的にポリシリコン膜が堆積するため、穴の部分にボイドが残ってしまうからである。その後、ＣＭＰ法を用いて、ポリシリコン膜１０を平坦化することにより、ゲートリソグラフィに適した平坦な表面を得る。

【００２５】

次に、図１１Ａ、１１Ｂ、１１Ｃ、１１Ｄに示すように、ゲートマスク材を堆積し、リソグラフィ技術を用いてこのゲートマスク材をパターニングしてマスク２１を形成する。その後、このマスク２１を用いてポリシリコン膜１０パターニングするとともに、スリミングを行って、ゲート電極形状のポリシリコン膜１０を形成する。このとき、ソース／ドレイン領域となる半導体層６上のポリシリコン膜１０およびゲート絶縁膜９をＲＩＥにより除去する（図１１Ｂ、１１Ｃ）。

【００２６】

次に、例えばＳｉＮからなるゲート側壁材１２を全面に堆積する。その後、このゲート側壁材にＲＩＥを行うことにより、ポリシリコン膜の側部に側壁１２を形成する（図１２Ｃ、１２Ｄ）。この時、オーバーエッチングすることにより、ゲート電極１０とソース／ドレイン領域となる半導体層６との高さの差を利用して、ポリシリコン膜１０の側壁は残し（図１２Ｃ）、ソース／ドレイン領域となる半導体層６の側壁は除去する（図１２Ｂ）。また、このオーバーエッチングにより、ソース／ドレイン領域となる半導体層６上のチャネル保護膜８も同時に除去することにより、ソース／ドレイン領域となる半導体層６を露出させる（図１２Ｂ、１２Ｃ）。また、このオーバーエッチングにより、図１２Ｄに示すように、マスク１２によって覆われていない領域の絶縁膜２０もリセスエッチングされ、その高さが低くなる。

【００２７】

次に、図１３Ｂ、１３Ｃに示すように、その側壁１２をマスクとして、露出した半導体層６を選択的にエッチングし、絶縁膜４からの高さを低くする。続いて、ｎ型ソース／ドレイン領域形成用ドーパントとしてＰ（リン）を斜め方向から、例えば、膜面に垂直方向から７度以上傾いた角度でイオン注入する（図１３Ｃ）。これにより、ｎ型ソース領域およびドレイン領域６０ａ、６０ｂが形成され、ソース領域６０ａとドレイン領域６０ｂとの間のｐ型半導体領域６がチャネル領域となる。このとき、図１３Ａ、１３Ｃ、１３Ｄに示すように、マスク２１は除去されていない。なお、ｐ型ソース／ドレイン領域を形成する場合は、ドーパントとしてＢ（ボロン）が用いられる。

【００２８】

次に、図１４Ａ、１４Ｂ、１４Ｃ、１４Ｄに示すように、ゲートマスク材２１を除去した後、Ｎｉなどの金属スパッタ、熱処理を行うことにより、ポリシリコン膜１０を完全にフルシリサイド化したゲート電極１３を形成する。このとき、ポリシリコン膜１０には自然酸化膜が形成されていないため、Ｎｉの拡散は均一に起こり、ゲート電極１３全体がフルシリサイド化する。また、このとき、ソース領域６０ａおよびドレイン領域６０ｂもシリサイド化される（図１４Ｂ、１４Ｃ）。

【００２９】

この状態では、図１４Ａに示すように、２本のゲート電極１３が分断されており、このままではゲート電極１３に電圧を印加することができない。そのため、上層配線を用いてゲート電極間を接続する必要がある。そこで、図１４Ａ乃至１４Ｄで説明したシリサイド工程が終了した後、コンタクトのエッチングストッパーとしてＳｉＮ膜２２ａを数十ｎｍ堆積する。その後、このＳｉＮ膜２２ａ上に層間絶縁膜２２ｂを堆積し、ＣＭＰを行い平坦化する（図１５）。ＣＭＰを行う前の層間絶縁膜２２ｂの上面の凹凸が大きくても、ＣＭＰを行うときには、ＳｉＮ膜２２ａがエッチングストッパーとして働く。

【００３０】

続いて、リソグラフィ技術とＲＩＥを用いて、層間絶縁膜２２ｂおよびＳｉＮ膜２２ａからなる絶縁膜２２に、ゲート電極１３に通じるコンタクトホール（図示せず）を開ける

。そして、このコンタクトホールをＴｉＮ－Ｗなどを埋め込み、プラグ２３を形成する（図１６）。更に、層間絶縁膜（図示せず）を堆積し、リソグラフィ技術とＲＩＥを用いて、この層間絶縁膜に配線加工用溝を形成し、この溝にＡｌ－Ｃｕなどの金属配線２４を埋め込み、プラグ２３および金属配線２４を介してゲート電極１３と電圧印加端子（図示せず）を接続する（図１７）。これにより、本実施形態のマルチゲート型ＦＥＴが完成する。

【００３１】

このようにして形成された本実施形態のマルチゲート型ＦＥＴと、通常のＦＵＳＩゲートＦｉｎＦＥＴにおけるゲート配線抵抗を比較すると、通常のＦＵＳＩゲートＦｉｎＦＥＴでは、非常に細い幅のゲート電極を信号が伝播するのに対して、本実施形態では太い金属配線２４を伝播するため、トランジスタを駆動するために高周波信号が印加されるゲート電極への配線抵抗の悪影響を大幅に緩和することができる。例えば、図１８（ａ）、１８（ｂ）に示すように、幅（ゲート長）を２０ｎｍ、ＦＵＳＩ電極のＦｉｎ上部を覆っている高さを６０ｎｍ、Ａｌ－Ｃｕ配線の幅１２０ｎｍ、高さ１μｍとすると、信号が伝播する面積Ｓとして２桁大きくすることができ、抵抗率の違いを考慮すると更にゲート抵抗を低くすることができる。

【００３２】

なお、本実施形態中のチャネル保護絶縁膜８をＴＥＯＳ、絶縁膜１９をＳｉＮ、絶縁膜２０をＴＥＯＳ、ゲートマスク材２１をＳｉＮで形成してもよい。

【００３３】

また、本実施形態でフィンの本数は２個として説明したが、３個以上のフィンとすることもできる。

以上説明したように、本実施形態によれば、平坦化工程を行っても、金属汚染を防止することができる。また，ゲート抵抗を低減することができる。

【００３４】

（第２実施形態）

次に、本発明の第２実施形態によるマルチゲート型ＦＥＴの製造方法を図１９Ａ乃至図２１Ｄを参照して説明する。本実施形態の製造方法によって製造されるマルチゲート型ＦＥＴは、メタルゲート型である。図１９Ａ、図２０Ａ、図２１Ａは図６に示す切断線Ａ－Ａ’で切断した断面図、図１９Ｂ、２０Ｂ、２１Ｂは図６に示す切断線Ｂ－Ｂ’で切断した断面図，図１９Ｃ、２０Ｃ、２１Ｃは図６に示す切断線Ｃ－Ｃ’で切断した断面図、図１９Ｄ、２０Ｄ、２１Ｄは図６に示す切断線Ｄ－Ｄ’で切断した断面図である。

【００３５】

まず、第１実施形態のフルシリサイドゲートＦＥＴで説明した図７Ａ乃至図９Ｄまでの製造工程と同じ工程を用いて行う。図９Ａ乃至図９Ｄに示す絶縁膜１９ａを除去することにより形成された穴の表面に、図１９Ａ，１９Ｂ、１９Ｃ、１９Ｄに示すように，メタルゲート用金属膜１７をＭＯＣＶＤ(Metal-Organic Chemical Vapor Deposition)で形成した後、上記穴を、ＬＰＣＶＤ法を用いてポリシリコン膜１０で埋め込む。このとき、上記穴内のゲート絶縁膜９およびチャネル保護膜８の表面はメタルゲート用金属膜１７で覆われ、その外側にポリシリコン膜１０が形成される。また、絶縁膜２０上にもメタルゲート用金属膜１７およびポリシリコン膜１０が付着する。このため、この状態でＣＭＰを行うと金属汚染をウェハ全体に広めてしまうことになる。

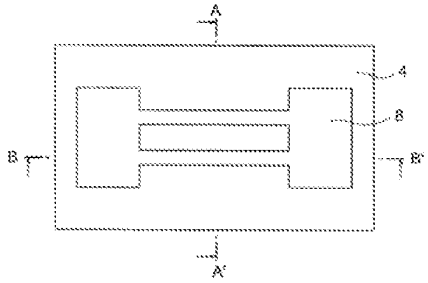
【００３６】

そこで、図２０Ａ、２０Ｂ、２０Ｃ、２０Ｄに示すように、ポリシリコン膜１０と金属膜１７をＲＩＥ法でエッチングすることにより、絶縁膜２０の上面のポリシリコン膜１０および金属膜１７を除去する。この時、フィンとなる半導体層６、保護膜８はポリシリコン膜１０で覆われており、上記ＲＩＥ法によってエッチングされていない。このため、制御性よく絶縁膜２０の上面の金属膜１７を制御することができる。このように、保護膜８と埋め込み絶縁膜２０の絶縁膜４からの高さの差を利用して、保護膜８およびゲート絶縁膜９の側面の金属膜１７とポリシリコン膜１０は残ることになる。

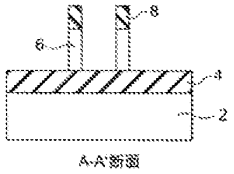
【００３７】
その後、図２１Ａ、２１Ｂ、２１Ｃ、２１Ｄに示すように、再度、ポリシリコン１０を堆積し、ＣＭＰを行うことにより、金属汚染を起こさずに、ゲートリソグラフィに適した平坦な表面を得る。以後は、第１実施形態で説明した図１１Ａ乃至図１７に示す工程と同様の工程を行い、マルチゲート型ＦＥＴを完成する。ただし、図１１Ａ以降で示すポリシリコン膜１０を形成する工程は不要であり、また、シリサイドする工程も不要である。このようにして形成された本実施形態のマルチゲート型電界効果トランジスタの断面図を図２２に示す。
【００３８】
なお、この実施形態中のチャネル保護絶縁膜８をＴＥＯＳ、絶縁膜１９をＳｉＮ、絶縁膜２０をＴＥＯＳ、ゲートマスク材２１をＳｉＮで形成してもよいことは第１実施形態と同様である。
【００３９】
以上説明したように、本実施形態によれば、平坦化工程を行っても、金属汚染を防止することができる。
【図面の簡単な説明】
【００４０】
【図１】従来のマルチゲート型ＦＥＴの製造工程を示す図。
【図２】従来のマルチゲート型ＦＥＴの製造工程を示す図。
【図３】従来のマルチゲート型ＦＥＴの製造工程を示す図。
【図４】従来のマルチゲート型ＦＥＴの製造工程の問題点を示す図。
【図５】従来のマルチゲート型ＦＥＴの製造工程の問題点を示す図。
【図６】本発明の第１実施形態によるマルチゲート型ＦＥＴの平面図。
【図７】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図８】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図９】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図１０】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図１１】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図１２】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図１３】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図１４】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図１５】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図１６】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図１７】第１実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図１８】第１実施形態によるマルチゲート型ＦＥＴの効果を説明する図。
【図１９】第２実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図２０】第２実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図２１】第２実施形態によるマルチゲート型ＦＥＴの製造工程を示す断面図。
【図２２】第２実施形態によるマルチゲート型ＦＥＴの断面図。
【符号の説明】
【００４１】
２　支持基板
４　絶縁膜
６　半導体層（ＳＯＩ層）
８　チャネル保護膜
９　ゲート絶縁膜
１０　ポリシリコン膜
１１　シリサイド用金属
１２　ゲート側壁
１３　ゲート電極（シリサイド）

１７　メタルゲート用金属
１８　層間絶縁膜
１９　絶縁膜
２０　絶縁膜
２１　ゲートマスク材
２２　絶縁膜
２２ａ　ＳｉＮ膜
２２ｂ　層間絶縁膜
２３　プラグ
２４　金属配線
５０１、５０２　フィン
６０ａ　ソース領域
６０ｂ　ドレイン領域
７０　ゲート
１００　自然酸化膜

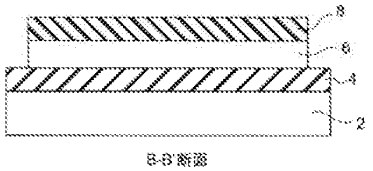
【図１Ａ】



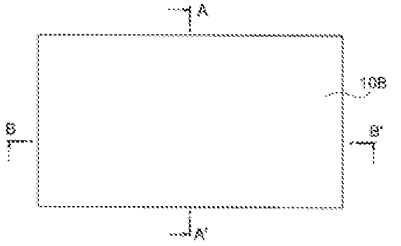
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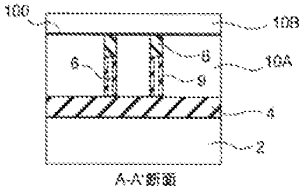
【図１Ｃ】



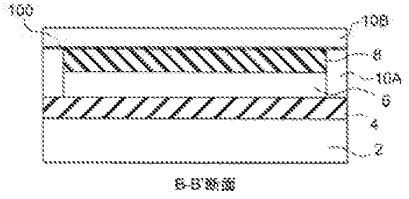
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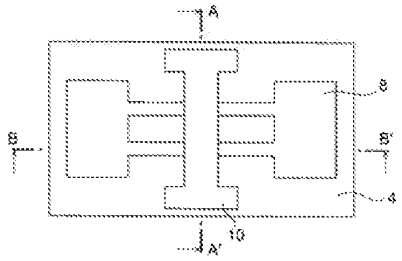
【図２Ｂ】



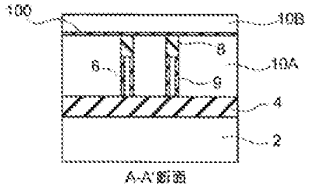
【図２Ｃ】



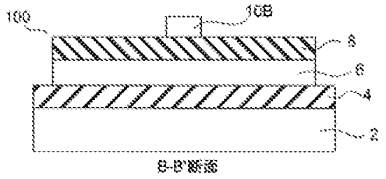
【図３Ａ】



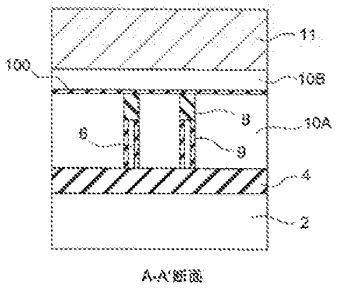
【図３Ｂ】



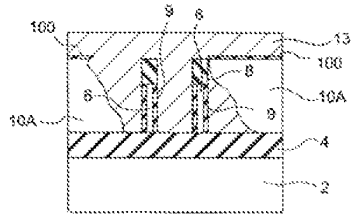
【図３Ｃ】



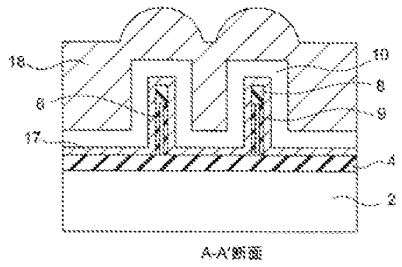
【図４Ａ】



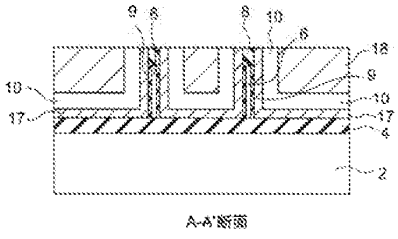
【図４Ｂ】



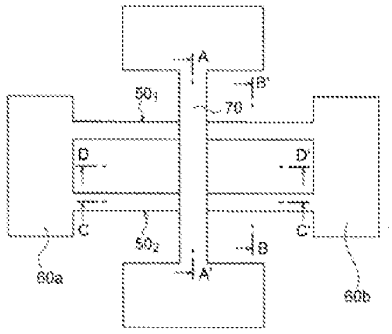
【図５Ａ】



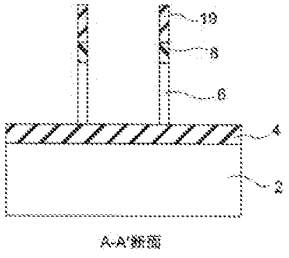
【図５Ｂ】



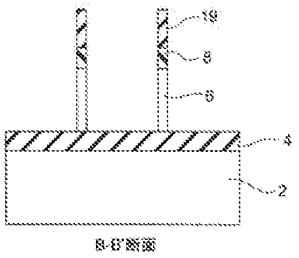
【図６】



【図７Ａ】

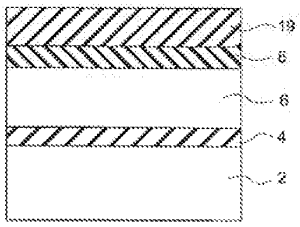


【図７Ｂ】



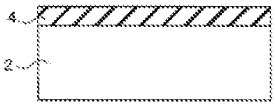
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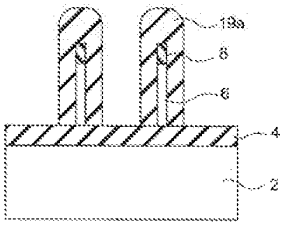
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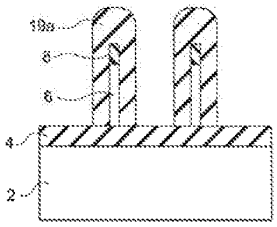
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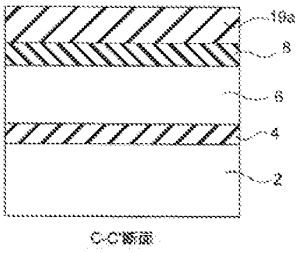
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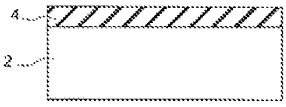
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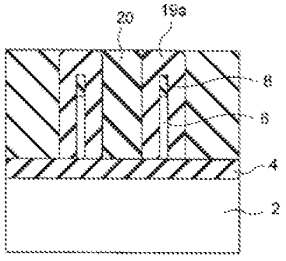
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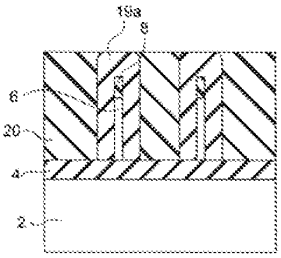
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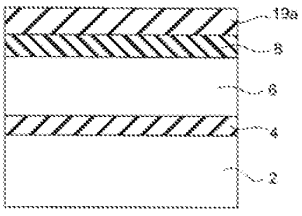
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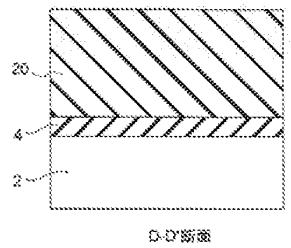
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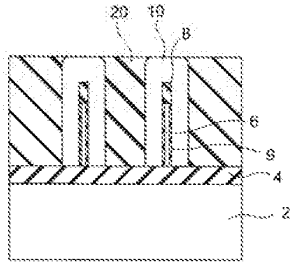
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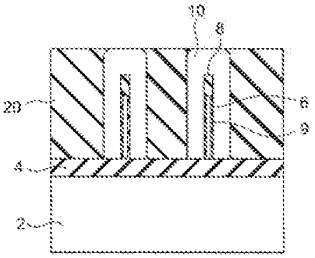
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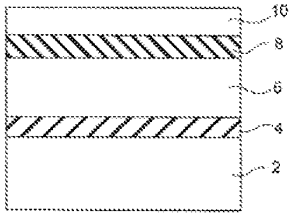
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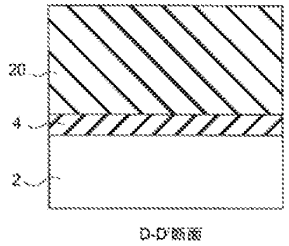
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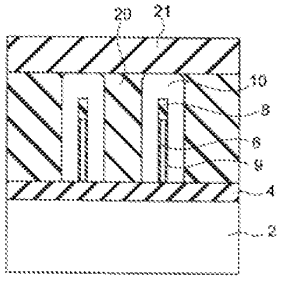
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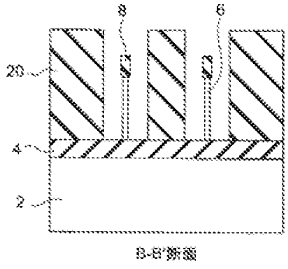
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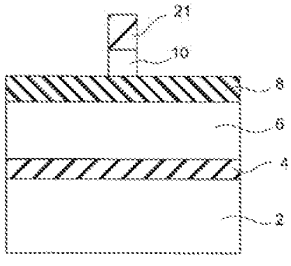
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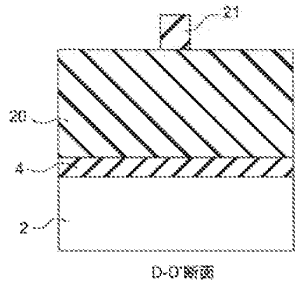
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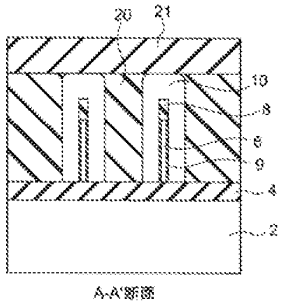
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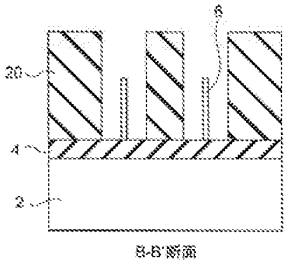
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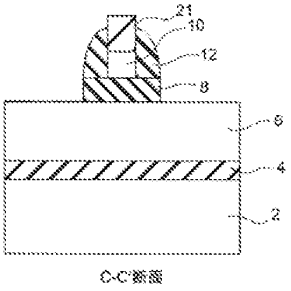
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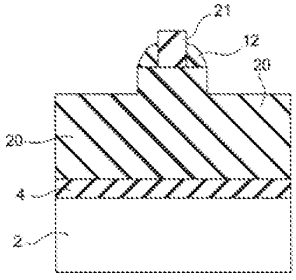
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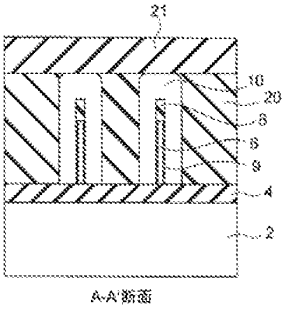
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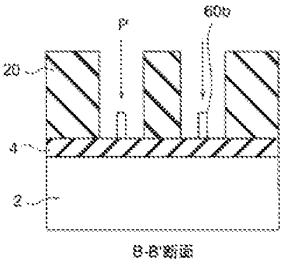
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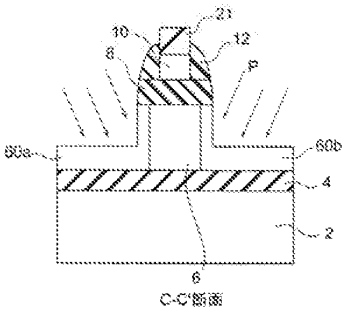
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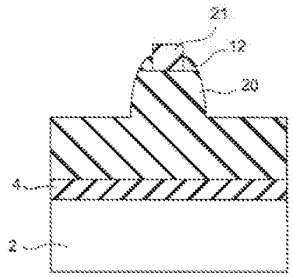
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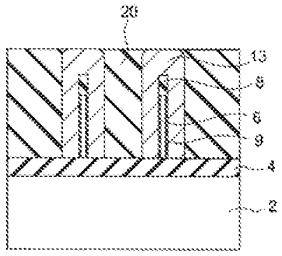
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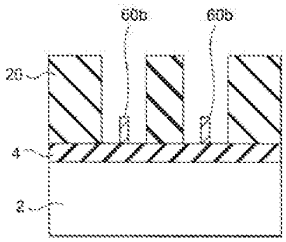
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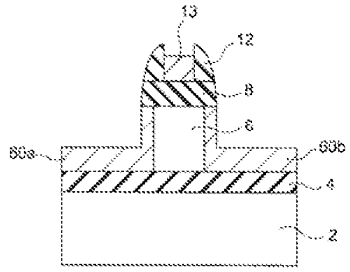
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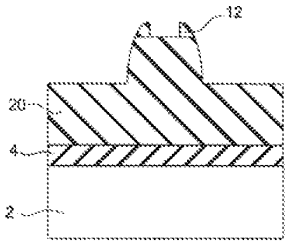
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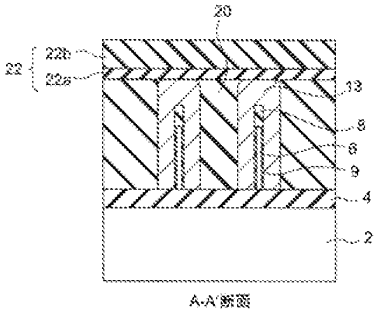
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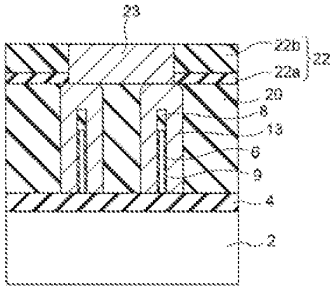
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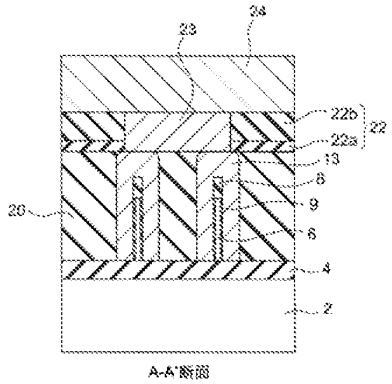
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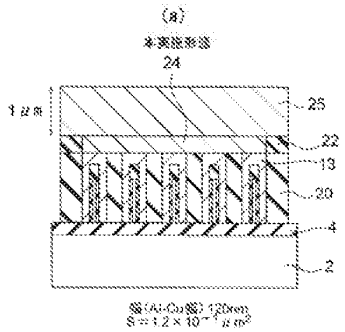
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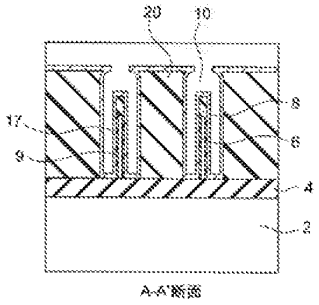


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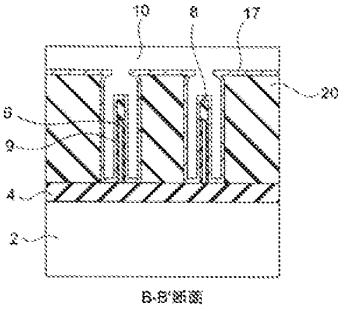
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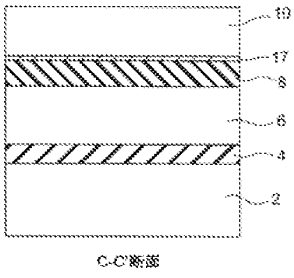
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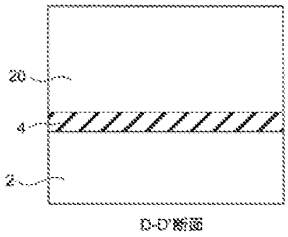
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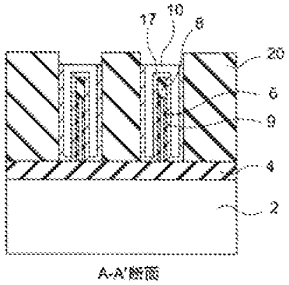
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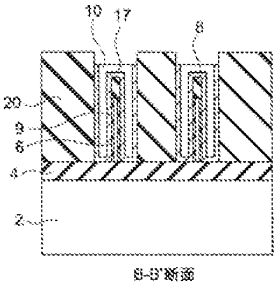
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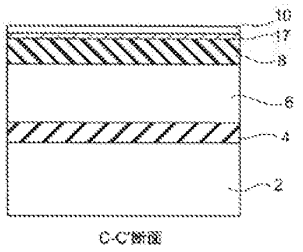
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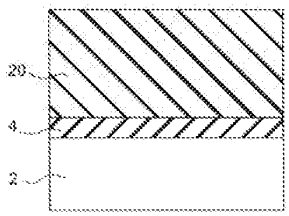


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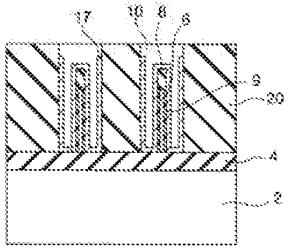
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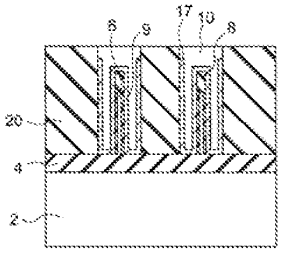
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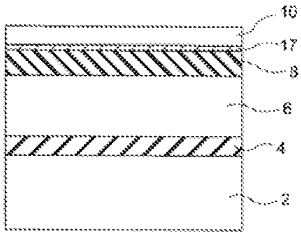
A-A'断面

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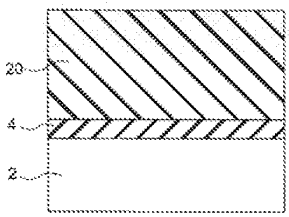
B-B'断面

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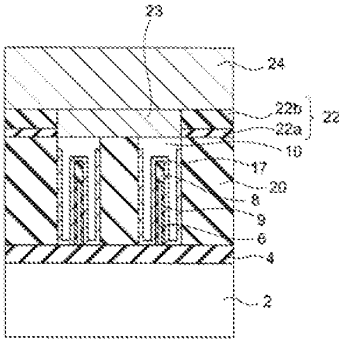
C-C'断面

【図２１Ｄ】



D-D'断面

【図２２】



A-A'断面

フロントページの続き

(51)Int.Cl.		F I		テーマコード（参考）
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H01L 27/08	*(2006.01)*	H01L 21/90	A	
H01L 21/8238	*(2006.01)*	H01L 21/90	B	
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		H01L 27/08	331E	
		H01L 27/08	321G	
		H01L 29/78	617N	

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DD43 DD65 DD78 DD84 EE17 FF04 GG09 GG10 GG14 HH20
5F033 HH09 JJ01 JJ31 KK04 KK25 PP00 PP11 PP15 QQ08 QQ09
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QQ19

Electronic Patent Application Fee Transmittal

Application Number:	15024750
Filing Date:	24-Mar-2016
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton C. WEBB
Filer:	Justin K. Brask/Sheri Villarreal
Attorney Docket Number:	P60397US

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**1140**

Electronic Acknowledgement Receipt	
EFS ID:	30451380
Application Number:	15024750
International Application Number:	
Confirmation Number:	9490
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First Named Inventor/Applicant Name:	Milton C. WEBB
Customer Number:	31817
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1	Issue Fee Payment (PTO-85B)	P60397US_Issue_Fee_09_22_17.pdf	1635274 b1b6f3759bff8b57a7d09c06a50bee716c23cf8c	no	1
Warnings:					
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6	Non Patent Literature	P60397JP_OA_07_26_17.pdf	144602 d4c528cdcf80ad2b5e479771aab58dd81dc7f8d8	no	10
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7		P60397US_IDS_09_22_17.pdf	973558 65919c7c7c0cf1d5de7603ec423eec550ba61422	yes	2
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	Transmittal Letter		1	1	
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8	Foreign Reference	JP2002-530872_cited_in_JP.pdf	4908951 049b6a482fefce55ab1f8d602451c2cde8d865d7	no	23
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9	Foreign Reference	JP2004-356472_cited_in_JP.pdf	9677797 73e94774e55f79553fd84a27261267204 0d73866	no	22
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10	Foreign Reference	JP2009-260221_cited_in_JP.pdf	7804689 06986eda45033ff6b54f7da28b62e870c53e62a6	no	20
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11	Fee Worksheet (SB06)	fee-info.pdf	32642 52dabd35210b9fe481835f678e2a652c5b21f9b1	no	2
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Sheri Villarreal	(Depositor's name)
/Sheri Villarreal/	(Signature)
September 22, 2017	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/024,750	03/24/2016	Milton C. WEBB	P60397US	9490

TITLE OF INVENTION: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/06/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
POTTER, ROY KARL	2822	257-369000

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Authorized Signature /Justin K. Brask/ Date September 22, 2017
Typed or printed name Justin K. Brask Registration No. 61,080

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PATENT NUMBER (if known)	APPLICATION NUMBER
	15/024,750

Completed by (check one):

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☑ Attorney or Agent of record 61,080 (Reg. No.) — Justin K. Brask (Typed or printed name)

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JP,2002-530872,A

Detail Image
CLAIMS DETAILED DESCRIPTION
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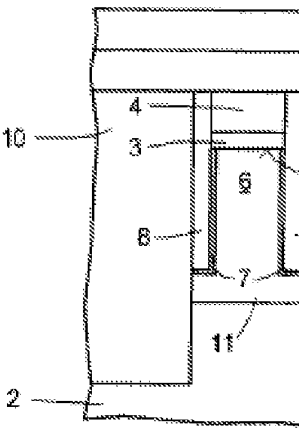
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
The present invention relates to the electric field effect control type transistor which can function also when channel length is smaller than 50 nm.
[0002]
A planar MOS transistor and a junction transistor reach an operation limit in about 50-nm channel length. Various transistor structures are proposed to the gate length region below 50 nm (see after IEDM 97 and the 427th page besides for example, H.Wong). In this case, a MOS transistor has two gate electrodes and the gate electrode is arranged at a side to which channel regions oppose each other.
Therefore, it has proposed controlling current along the two surfaces of channel regions.
As for this, the source region, channel regions, and a drain area are perpendicularly arranged to the main surface of a silicon wafer.
The source region, channel regions, and a drain area are possible also for vertical mold structure which forms a stack projected from the main surface, and flat mold structure arranged in parallel to the main surface of a silicon wafer.

[0003]
H. Realizing a planar MOS transistor on a SOI substrate after IEDM 97 and the 427th page besides Wong is proposed, and the gate electrode above channel regions and the lower gate electrode of channel regions are provided here. A silicon oxide layer thick on a silicon substrate for manufacture of a transistor, A first silicon nitride layer, a first thin silicon oxide layer, the spacer layer that comprises an amorphous silicon, Providing a second thin silicon oxide layer and second silicon nitride layer, and structurizing so that the surface of the thick silicon oxide layer of a source and a drain area may be exposed is proposed. In either a sourceora drain area, a window can open in a thick silicon oxide layer to the surface of a silicon substrate. The spacer layer which comprises an amorphous silicon is removed in the region of a gate stack. Next, in the range of a source / drain area, and channel regions, single crystal silicon is grown up by alternative epitaxy from the surface which the silicon substrate exposed. Two gate electrodes are formed in the upper part of channel regions and a lower part grown-up in alternative epitaxy by removing the structurized first silicon nitride layer and a second silicon nitride layer, and carrying out the deposit of the doped polycrystalline silicon. This method is not compatible with the standard step of semiconductor process technique.
[0004]
D. IEDM 89 besides Hisamoto -- the 833-836th page -- the source region -- The planar MOS transistor which has channel regions and a drain area in the silicon web is proposed, and insulated separation of the silicon web is carried out by field field oxide to the silicon substrate arranged under it. The gate electrode overlaps the silicon web within the scope of channel regions, therefore controls channel current in accordance with the side wall of the both sides of a silicon web. It flows through a current direction in parallel to the main surface of a silicon substrate. In order to manufacture the transistor concerned, on the surface of the silicon substrate, it is covered by the silicon nitride layer and structurizing the silicon web by which the silicon nitride spacer is provided by the side wall is proposed. Furthermore, underetching of the surface of a silicon substrate is carried out under a silicon nitride spacer. Field field oxide is formed by local oxidation (local oxidation) of the surface of a silicon substrate. In that case, oxidation is continued until the field field oxide formed in the both sides of a web reaches under the web by the arising bird's beak. This manufacturing process is not compatible with the standard step of semiconductor process technique, either.
[0005]
The problem given to the present invention is functioning also in the case of the gate length below 50 nm, and providing the electric field effect control type transistor which can be manufactured using the standard step of semiconductor process technique. The manufacturing

CLOSE



Representative dr

Representative drawing | 1 | 2

Previous Document 3/7

method of the transistor is proposed.
[0006]
An aforementioned problem is solved by the present invention with the manufacturing method of the electric field effect control type transistor according to claim 1 and the transistor according to claim 6. Another composition of the present invention is described in dependent claim.
[0007]
An electric field effect control type transistor is realized by the semiconductor substrate. The active region which has the source region, the channel regions, and the drain area which touch the main surface of the semiconductor substrate, respectively is provided by the semiconductor substrate, therefore current flows in parallel to the main surface of a semiconductor substrate between the source region and a drain area. At least one trench is provided by the main surface of the semiconductor substrate, the trench is in contact with channel regions, and some gate electrodes are arranged at the trench. In a transistor, some gate electrodes reach the depth of a semiconductor substrate. Therefore, the current which flows in parallel to the main surface of a substrate by the side wall of channel regions from which the main surface of a substrate is cut is controllable via a gate electrode. Therefore, effective channel width is not dependent on the width of the channel regions in the main surface of a semiconductor substrate.
[0008]
A transistor is realizable also as a junction transistor also as a MOS transistor. In the case of the MOS transistor, the gate insulator is provided on the surface of channel regions in the region of a trench at least.
[0009]
It is advantageous if the semiconductor substrate which has single crystal silicon to the region of the main surface at least in consideration of integration in standard silicon process technology is used. The single crystal silicon wafer, the single crystal silicon layer of a SOI substrate, the SiGe substrate, or the SiC substrate is suitable advantageously as a semiconductor substrate.
[0010]
The portion of the gate electrode is arranged advantageously at the side wall of channel regions which opposes each other, respectively, therefore the transistor has effectively two gate electrode parts which oppose each other. These portions are arranged at a first trench and second trench, respectively. By providing two gate electrode parts, a reversal channel is controlled by the side wall of channel regions which opposes each other. By this composition, the punch through (Durchgriff) to the channel regions of drain voltage is reduced, therefore publicly known restrictive "Drain InducedBarrier Lowering" does not actually act from document. The influence which substrate voltage has on channel regions and which is not preferable is reduced by providing two gate electrode parts.
[0011]
or [that the breadth of the source region and a drain area is small vertically advantageously as compared with the depth of one or a plurality of trenches to the main surface of a semiconductor substrate] -- or it is the same. By this composition, therefore the surface in which an electric conduction reversal channel is formed over it is expanded, current gain (Stromergiebigkeit) increases as compared with flat molding equipment. Furthermore by this, the mutual conductance of a transistor important for control of a transistor increases.
[0012]
Advantageously, the dimension of a gate electrode is restricted to the dimension of channel regions in parallel to the main surface, is depended, and drain gate overlap capacity is minimized. Parasitic capacitance is minimized by this and the mutual conductance of a transistor is raised. This is advantageous in a GHz region because of a high-speed switching characteristic and a good high frequency characteristic.
[0013]
It is advantageous to provide the isolation structure surrounding an active region and one or more trenches for the isolation of the transistor in an integrated circuit.
[0014]
The trench which determines an active region to the main surface of a semiconductor substrate in the side for manufacture of a transistor is formed. Then, the gate electrode arranged partially at the trench is formed.
[0015]
In order to manufacture a transistor as a MOS transistor, a gate insulator is formed on the surface of channel regions.
[0016]
In order to form a gate electrode by self-alignment, the deposit of the first conductive layer is carried out, and conductive spacers are formed in the side wall of an active region by anisotropic etching from the first conductive layer. Then, the isolation structure surrounding an active region and conductive spacers is formed. In this case, the surface of a parallel conductive spacer is exposed to the main surface of a semiconductor substrate. The deposit of the second conductive layer connected with the conductive spacers via the exposed surface of conductive spacers is carried out. A gate electrode is formed by structure of a second conductive layer and conductive spacers. The polycrystal or the amorphous silicon, metallic silicide, and/or metal which were doped are suitable advantageously as a material of a conductive layer. Advantageously, structure for manufacture of a gate electrode is carried out by mask etching. The mask used in that case determines gate length. In this case, 50 nm or less of 10-50-nm gate length can be advantageously realized by using a fine structure-ized step, for example, electron beam lithography, or using an imprint method or spacer technology.
[0017]
Manufacture of a source/drain area is advantageously performed by implantation by self-alignment to a gate electrode.
[0018]
The trench has advantageously a section which suits to the section of isolation structure and a gate electrode. In this case, isolation structure is formed by carrying out the deposit of the isolation layer completely filled up with a trench, and chemical mechanical polishing.

[0019]
Next, the present invention is described in detail using the figures based on an embodiment.
[0020]
Fig.1 shows the section schematic illustration of the semiconductor substrate for formation of the mask which determines a first silicon oxide layer, a second silicon oxide layer, and an active region.
[0021]
Fig.2 is the plane schematic illustration which looked at Fig.1 from the top.
[0022]
Fig.3 shows the section schematic illustration of the semiconductor substrate for formation of a gate insulator, and formation of the conductive spacers in the side wall of an active region for structure of the active region of a semiconductor substrate.
[0023]
Fig.4 shows the section schematic illustration of the semiconductor substrate by another etching of a semiconductor substrate.
[0024]
Fig.5 is the plane schematic illustration which looked at the semiconductor substrate for formation of a gate electrode, the filling of the intermediate space between the source region and a drain area, and formation of the isolation structure which used isolation material from the top for formation of isolation structure.
[0025]
Fig.6 is a cross sectional view in alignment with dash-dotted line VI-VI of Fig.5.
[0026]
Fig.7 is a cross sectional view in alignment with dash-dotted line VII-VII of Fig.5.
[0027]
Fig.8 is a cross sectional view in alignment with dash-dotted line VIII-VIII of Fig.5.
[0028]
The first silicon oxide layer 3 is laminated by thermal oxidation on the main surface 1 of the semiconductor substrate 2 in which doping material concentration comprises the single crystal silicon in which p doping of 10 $^{15}cm^{-3}$ was done. The thickness of the first silicon oxide layer 3 is 5 nm. The deposit of the first silicon nitride layer 4 that has a thickness of 20 nm on the first silicon oxide layer 3 is carried out. On the surface of the first silicon nitride layer 4, the mask 5 which determines the active region surrounded by the trench is formed (refer to Fig.1 and Fig.2). The mask 5 has a rectangular cross section substantially in parallel to the main surface 1, and the dimension is 40 nm x 500 nm.
[0029]
The first silicon nitride layer 4, the first silicon oxide layer 3, and the semiconductor substrate 2 are etched by anisotropic etching, and the active region 6 surrounded by the semiconductor substrate 2 at the trench is formed in that case (refer to Fig.3). CF_4 and H_2 are used as etching gas. This etching is performed by 500-nm Fukashi under the main surface 1.
[0030]
The gate insulator 7 which changes from SiO_2 of 3-nm thickness to the side wall of the active region 6 is formed by thermal oxidation.
[0031]
The conductive spacers 8 which comprise the polycrystalline silicon doped by the side wall of the active region 6 with the deposit of the first conductive layer that comprises the doped polycrystalline silicon, and the etchback of the first conductive layer are formed (refer to Fig.3). The conductive spacers 8 have surrounded the active region 6 to ring shape.
[0032]
The exposed portion of the gate insulator 7 is removed in another anisotropic etching process using SiF_4 and H_2. Then, the semiconductor substrate 2 is etched by the anisotropic etching using CF_4. Therefore, the isolation trench 9 which has a depth of 1 micrometer on the basis of the main surface 1 in the active region 6 and the side of the conductive spacers 8 arises (refer to Fig.4).
[0033]
It fills up with an isolation trench by carrying out the deposit of the second SiO_2 layer. The isolation structure 10 filled up with the isolation trench 9 is formed from a second silicon oxide layer by continuing chemical mechanical polishing on which the first silicon nitride layer 4 acts as an etch stop (refer to Fig.6).
[0034]
By carrying out implantation of the boron, the channel doping part 11 of the doping material concentration of 5x10 $^{17}cm^{-3}$ is formed in the active region 6.
[0035]
Superficially, the deposit of the second conductive layer 12 and the second silicon nitride layer 13 is carried out, and they are completely structurized using a mask (not shown). The structurized second conductive layer 12 and the structurized second Si_3N_4 layer 13 have a strip cross section.
This cross section is sideways extended to longitudinal direction breadth of the active region 6, and has a width of 40 nm in parallel to longitudinal direction breadth of the active region 6.
In the case of structure of the second conductive layer 12, the exposed region of the conductive spacers 8 is removed similarly. The structure concerned is carried out by the anisotropic etching which used SiF_4 and H_2.
[0036]
With the deposit of the 3rd silicon nitride layer, and the etchback of the 3rd silicon oxide layer, The intermediate space between the active region 6 and the isolation structure 10 which arise on the outside of the second conductive layer 12 structurized at the time of removal of the conductive spacers 8 is filled up with the isolation filler 14 (refer to Fig.7).
[0037]
The silicon nitride spacer 15 is formed in the side wall of the structurized second conductive layer 12 and the structurized second silicon nitride layer 13 with the deposit of the 3rd silicon nitride layer, and the anisotropic etchback of the 3rd silicon nitride layer (refer to Fig.5 and Fig.8). By carrying out implantation of the As with the energy of 50keV, and the dose of 2x10 $^{15}cm^{-2}$, self-alignment is carried out to the structurized second conductive layer 12, and a

source / drain area 16 is formed (refer to Fig.7 and Fig.8). In this case, the depth of lower source / drain area 16 of the main surface 1 is smaller than the depth in which the conductive spacers 8 have extended.
[0038]
The conductive spacers 8 are mutually connected via the structurized second conductive layer 12. The portion of the structurized second conductive layer 12 which connects the conductive spacers 8 and this acts as a gate electrode. Since the conductive spacers 8 are extended to the semiconductor substrate 1 more deeply than a source / drain area 16, when suiting and controlling a gate electrode, the whole depth of the source / drain area 16 is covered, and an electric conduction reversal channel is formed between a source / drain area 16. Therefore, the range of the active region 6 between a source / drain area 16 acts as channel regions covering the whole depth.
[0039]
Multilayer metallization is performed by the method (it does not explain in full detail) that it is publicly known for manufacture of the transistor concerned.
[0040]
Although described about the n-channel transistor in the working example, the present invention is feasible as a p channel transistor similarly. conductive material with an another conductive layer -- it can constitute from metallic silicide or metal advantageously. The gate insulator 7 is possible also for providing to the region of the main surface 1 of an active region, therefore can form an electric conduction reversal channel over the main surface. In this case, a first silicon oxide layer and first silicon nitride layer do not need between the active region 6 and the second conductive layer 12. If technically required, a source / drain area 16 can form using a LDD profile.
[Brief Description of the Drawings]
[Drawing 1]
The section schematic illustration of the semiconductor substrate for formation of the mask which determines a first silicon oxide layer, a second silicon oxide layer, and an active region is shown.
[Drawing 2]
It is the plane schematic illustration which looked at Fig.1 from the top.
[Drawing 3]
The section schematic illustration of the semiconductor substrate for formation of a gate insulator and formation of the conductive spacers in the side wall of an active region is shown for structure of the active region of a semiconductor substrate.
[Drawing 4]
The section schematic illustration of the semiconductor substrate by another etching of a semiconductor substrate is shown. [Drawing 5]
It is the plane schematic illustration which looked at the semiconductor substrate for formation of a gate electrode, the filling of the intermediate space between the source region and a drain area, and formation of the isolation structure using isolation material from the top because of formation of isolation structure.
[Drawing 6]
It is a cross sectional view in alignment with dash-dotted line VI-VI of Fig.5.
[Drawing 7]
It is a cross sectional view in alignment with dash-dotted line VII-VII of Fig.5.
[Drawing 8]
It is a cross sectional view in alignment with dash-dotted line VIII-VIII of Fig.5.

[Translation done.]

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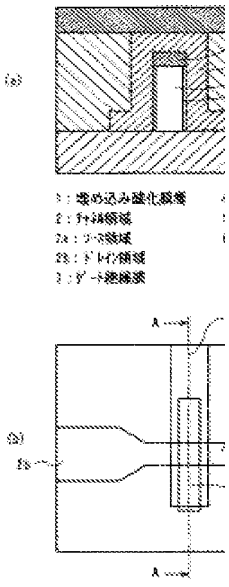
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]
Especially this invention relates to electrode wiring structure of a field effect transistor, and a formation method for the same about a semiconductor device and a manufacturing method for the same.
[0002]
[Description of the Prior Art]
MISFET (metal-insulating material-semiconductor field effect transistors) used for the semiconductor integrated circuit has attained increase of high-density integration and driving force simultaneously by micronization of an element size, especially gate length's reduction. However, in the planar type element according to the conventional trend, it is becoming difficult to establish the technology on which it accelerates with micronization and satisfies the problem that power consumption reduction is carried out. As technology of making such problem attaining, FinFET is being studied actively in recent years.
[0003]
Although a gate electrode is formed in the channel upper part formed on the single crystal Si surface via gate dielectric film, conventional planar type FET, FinFET is the structure of having DABURUGETO which puts both sides for the channel formed on the substrate from a transverse direction via gate dielectric film, and the example mainly constituted from a SOI layer has been reported.
[0004]
For example, the semiconductor layer region which constitutes a source region-channel-regions-drain area is formed by forming the hard surface mask blank of the two-layer structure of a silicon oxide film and a silicon nitride film in the SOI (Si) layer on an embedding oxide film, and etching the SOI layer in the opening of this hard surface mask blank. Then, in order to perform etching damage removal and reduction in thickness of a channel layer, sacrifice oxidation is performed and a sacrifice oxidation layer is removed further.
Then, a gate oxide film is formed by thermal oxidation etc., and a gate electrode is formed by forming and patterning conductive films, such as polysilicon. By this method, a gate electrode [gate length] as minute as 10 nm is formed. Usually, when forming a minute gate electrode, polysilicon and the amorphous silicon from which ultra-fine processing technology developed most are used (for example, see nonpatent literature 1).
[0005]
[Nonpatent literature 1]
Bin Yu, Leland Chang, et al, and "FinFET Scaling to 10nm Gate Length,", IEDM Tech.Dig., Dec.2002, pp251-254
[0006]
[Problem to be solved by the invention]
In order to prevent a resistance rise of a gate wire conventionally, the Salicide method is used, but in the device of the generation by whom 10 nm or less of gate length is used, to make resistance of a gate electrode and wiring low further is needed.
[0007]
When using a metal film for a gate electrode, oxidation resistance and chemical resistance are required, and also in patterning technology, there is a problem that it has not been established yet compared with the patterning technology of polysilicon with a track record.
[0008]
When forming a metal film or a metal silicide film in a gate electrode, in order [which possesses both of FET of PMIS and NMIS like a CMIS circuit] to carry out, optimization of threshold voltage is needed, but there is a problem that control of threshold voltage cannot be performed like a polysilicon electrode.
[0009]

CLOSE



Representative dr

Representative drawing | 1 | 2 | 3 | 11 | 12 | 13 | 14 | 15

Previous Document 4/7

The present invention solves the above problems and aims at offer of a semiconductor device which can make low resistance a gate electrode, a gate wire, or its both, and a manufacturing method for the same.
[0010]
Control of threshold voltage aims at offer of a semiconductor device which becomes possible, and a manufacturing method for the same also in a CMIS circuit.
[0011]
[Means for solving problem]
FET which has a silicon layer used as the source region, the channel regions, and the drain area which were formed so that the semiconductor device concerning the present invention might be projected on a substrate, the insulator layer formed in the above-mentioned silicon layer surface, and a gate electrode which covers the above-mentioned channel regions from three directions via the above-mentioned insulator layer,
The interlayer insulation film which embeds the above-mentioned silicon layer so that the surface of the projection direction of the above-mentioned gate electrode may be exposed,
It has the gate wire electrically connected to the surface of the projection direction of the gate electrode which was [above-mentioned] exposed.
[0012]
The first silicon layer used as the source region, the channel regions, and the drain area which were formed so that it might project on a substrate, FET of a NMIS region which has the first insulator layer formed in the surface of the 1st silicon layer of the above, and a first gate electrode that covers the channel regions of the 1st silicon layer of the above from three directions via the 1st insulator layer of the above,
The second silicon layer used as the source region, the channel regions, and the drain area which were formed so that it might project on the above-mentioned substrate, FET of a PMIS region which has the second insulator layer formed in the surface of the 2nd silicon layer of the above, and a second gate electrode which covers the channel regions of the 2nd silicon layer of the above from three directions via the 2nd insulator layer of the above,
The interlayer insulation film which embeds FET of the above-mentioned NMIS region, and FET of a PMIS region so that the above 1st and the projection direction surface of a second gate electrode may be exposed,
It has the gate wire electrically connected to the surface of the projection direction of the gate wire electrically connected to the surface of the projection direction of the first gate electrode that was [above-mentioned] exposed, and a second gate electrode.
[0013]
The first process of forming FET which has the source region, the channel regions, and the drain area which the manufacturing method of the semiconductor device concerning the present invention patterns the silicon layer on a substrate, and it projects on the above-mentioned substrate,
The second process of forming an insulator layer in the silicon layer surface which patterned [above-mentioned],
The 3rd process of forming the gate electrode which covers the three directions of the above-mentioned channel regions via the above-mentioned insulator layer,
The 4th process of forming an interlayer insulation film,
The fifth process which flattens the above-mentioned interlayer insulation film and at which it exposes the surface of the projection direction of the above-mentioned gate electrode from the above-mentioned interlayer insulation film,
It has the sixth process of forming the gate wire electrically connected with the surface of the projection direction of the gate electrode which formed the conductive film, and patterned and was [above-mentioned] exposed.
[0014]
The first process of forming the silicon layer of a NMIS region and a PMIS region which has the source region, the channel regions, and the drain area which pattern the silicon layer on a substrate and it projects on the above-mentioned substrate,
The second process of forming and making an insulator layer the silicon layer surface which patterned [above-mentioned],
The 3rd process of forming the gate electrode which consists of polysilicon or an amorphous silicon which covers the three directions of the above-mentioned channel regions via the above-mentioned insulator layer,
The 4th process of forming an interlayer insulation film,
The fifth process which flattens the above-mentioned interlayer insulation film and at which it exposes the surface of the projection direction of the above-mentioned gate electrode from the above-mentioned interlayer insulation film,
One gate electrode of the above-mentioned NMIS region or a PMIS region is covered with a silicide preventing film, The sixth process of covering the gate electrode of another side with a first metal film, making polysilicon or the amorphous silicon of the 1st metal film of the above, and the gate electrode of above-mentioned another side reacting by heat treatment, and making the gate electrode of above-mentioned another side into metal silicide,
Remove the above-mentioned silicide preventing film and it covers the gate electrode of above-mentioned another side of the above-mentioned NMIS region or a PMIS region with a silicide preventing film, The seventh process of covering above-mentioned one gate electrode with the second metal film of a different kind from the 1st metal film of the above, making above-mentioned one [the 2nd metal film of the above, and] polysilicon or amorphous silicon of a gate electrode reacting by heat treatment, and making above-mentioned one gate electrode into metal silicide,
It has the eighth process of forming the gate wire electrically connected with the surface of the projection direction of each gate electrode which formed the conductive film, and patterned and was [above-mentioned] exposed.
[0015]
The first process of forming the silicon layer of a NMIS region and a PMIS region which has the source region, the channel regions, and the drain area which pattern the silicon layer on a substrate and it projects on the above-mentioned substrate,
The second process of forming an insulator layer in the silicon layer surface which patterned

[above-mentioned],
The 3rd process of forming the dummy gate electrode which consists of polysilicon or an amorphous silicon which covers the three directions of the above-mentioned channel regions via the above-mentioned insulator layer,
The 4th process of forming an interlayer insulation film,
The fifth process which flattens the above-mentioned interlayer insulation film and at which it exposes the surface of the projection direction of the above-mentioned dummy gate electrode from the above-mentioned interlayer insulation film,
One dummy gate electrode of FET of the above-mentioned NMIS region or a PMIS region is covered with a first etching mask, The sixth process of embedding a first metal film into the portion which removed the dummy gate electrode of another side, removed the 1st etching mask of the above, and removed the dummy gate electrode of above-mentioned another side, and forming a gate electrode,
The dummy gate electrode of above-mentioned another side of the above-mentioned NMIS region or a PMIS region is covered with a second etching mask, The seventh process of embedding the second metal film of a different kind from the 1st metal film of the above into the portion which removed above-mentioned one dummy gate electrode, removed the 2nd etching mask of the above, and removed above-mentioned one gate electrode, and forming a gate electrode,
It has the eighth process of forming the gate wire electrically connected with the surface of the projection direction of each gate electrode which formed the conductive film, and patterned and was [above-mentioned] exposed.
[0016]
[Mode for carrying out the invention]
Embodiment 1.
Fig.1 is the cross sectional view (a) and plan view (b) showing the embodiment 1 of the semiconductor device concerning the present invention, and the cross sectional view (a) shows the A-A section of the plan view (b).
[0017]
As shown in Fig.1 (b), the fin type silicon (Si) which the source region 2a, the channel regions 2, and drain area 2b projected is formed on the embedding oxidizing zone 1 (substrate). As shown in Fig.1 (a), the gate electrode 4 which consists of polysilicon or an amorphous silicon is formed in the circumference (surface of three directions) of the channel regions 2 via the hard surface mask blank 10 formed in the upper part of the gate dielectric film 3 and the channel regions 2. The gate electrode 4 was embedded at the interlayer insulation film 5, the top surface has exposed it from the interlayer insulation film 5, and the gate wire 6 which consists of the metal connected to the exposed surface of the gate electrode 4 is formed on the interlayer insulation film 5. It is good also as a silicon substrate to replace with the embedding oxidizing zone 1.
[0018]
Since the gate wire 6 connected to the gate electrode 4 and the gate electrode 4 can be formed independently according to this composition, resistance of the gate wire 6 can be low-resistance-ized arbitrarily.
[0019]
Since the interlayer insulation film 5 is flattened and the gate wire 6 can be formed on the flattened interlayer insulation film 5, the gate wire 6 can be patterned easily.
[0020]
Fig.2 and Fig.3 are the cross sectional views showing the manufacturing process which manufactures the semiconductor device of this embodiment. A manufacturing method is described based on the figures.
[0021]
First, by forming the hard surface mask blank of the two-layer structure of the silicon oxide film 26 and the silicon nitride film 27 in the silicon layer 25 on the embedding oxide film 1, and etching the silicon layer 25 in the opening of this hard surface mask blank, The semiconductor layer region which constitutes a source region-channel-regions-drain area is formed. Fig.2 (b) shows the formed semiconductor layer region.
[0022]
Next, as were shown in Fig.2 (a), and the photoresist 28 corresponding to a source region-channel-regions-drain area is formed on the silicon nitride film 27 and it was shown in Fig.2 (b). The silicon oxide film 26, the silicon nitride film 27, and the silicon layer 25 are etched by using photoresist 28 as a mask, and a source region-channel-regions 2-drain area is formed.
[0023]
Next, as shown in Fig.2 (c), in order to perform etching damage removal and reduction in thickness of a channel layer, sacrifice oxidation is performed, the sacrifice oxidation layer 29 is formed, and as shown in Fig.2 (d), the sacrifice oxidation layer 29 is removed further.
[0024]
Next, as shown in Fig.2 (e), the gate oxide film 3 is formed by thermal oxidation etc. As mentioned above, a fin type gate electrode [gate length] as minute as 10 nm is formed by the method described in the above-mentioned nonpatent literature 1, and the same method.
[0025]
Next, as shown in Fig.3 (a), a polysilicon film or 50-100 nm of amorphous silicon films are formed in the circumference of the channel regions 2 with a CVD method via the gate oxide film 3 and the hard surface mask blank 10 (silicon oxide film 26 in Fig.2), It patterns after the width L of the channel regions 2, and forms the gate electrode 4.
[0026]
Let width L be the value which added the twice in consideration of the superposition accuracy of lithography of the value to the value which added the twice of the film thickness of the silicon layer which is the channel regions 2, and the film thickness of the gate dielectric film 3, and the twice of the film thickness of the gate electrode 4. Let the width L and the vertical value (height) be gate length's values. For example, the film thickness of a silicon layer will set L to 173.4 nm, if the film thickness of 1.7 nm and a polysilicon film is [the superposition accuracy of 50 nm and lithography of the film thickness of 10 nm and the gate dielectric film 3] 30 nm.
[0027]

Next, as shown in Fig.3 (b), the silicon oxide film which is the interlayer insulation film 5 is formed with a CVD method etc., and it flattens by the CMP method (chemical machinery grinding method), and exposes the top surface of the gate electrode 4.
[0028]
Next, as shown in Fig.3 (c), a metal film (tungsten), for example, W, Al-Cu alloy (aluminum copper alloy), and Cu are formed with a sputtering method or a CVD method, and it patterns and forms the low resistance gate wire 6 which consists of a metal film.
[0029]
A TiN (titanium nitride) film, the cascade screen of TiN and Ti, a TaN (tantalum nitride) film, or the cascade screen of TaN and Ta may be formed in the lower part of a metal film as it is usually carried out, when forming a metal film in Fig.3 (c).
[0030]
In Fig.3 (a), the alloy of silicon and germanium may be used instead of polysilicon and an amorphous silicon.
[0031]
As mentioned above, since the manufacturing method in this embodiment forms independently the gate wire 6 connected to the gate electrode 4 and the gate electrode 4, it can low-resistance-ize resistance of the gate wire 6 arbitrarily.
[0032]
Since the interlayer insulation film 5 is flattened and the gate wire 6 is formed on the flattened interlayer insulation film 5, the gate wire 6 can be patterned easily.
[0033]
Although this embodiment showed the example which embeds and forms fin type FET on the oxidizing zone 1, fin type FET may be formed on a silicon substrate.
[0034]
Embodiment 2.
Although polysilicon or an amorphous silicon was used as the gate electrode 4 in the above-mentioned embodiment 1, depletion of polysilicon or an amorphous silicon becomes the hindrance of the improved efficiency of a transistor. Then, in order to prevent depletion, the gate electrode 4 is replaced with polysilicon and an amorphous silicon, and it is considered as metal silicide.
[0035]
Fig.4 is a cross sectional view showing the manufacturing process which manufactures the semiconductor device of this embodiment.
The manufacturing method at the time of using polysilicon for the gate electrode 4 based on the figure is described.
[0036]
After passing through the process to Fig.3 (b) like the above-mentioned embodiment 1, as shown in Fig.4 (a), the metal film 7, for example, cobalt, nickel, titanium, tantalum, vanadium, platinum, etc. form 10-30 nm of these alloy films with a PVD method, for example.
[0037]
Next, it heat-treats. Heat treatment is performed by heating in nitrogen gas or inert gas atmosphere for 400-600 degrees C and 60 seconds, for example. The polysilicon 8 reacts to the metal film 7, and the metal silicide film 9 is formed by this heat treatment.
[0038]
Since a silicide formation reaction is not produced in the region which does not touch the polysilicon 8 and the metal film 7 remains as the metal film 7, it removes the unreacted metal film 7 by mixed liquor with acid, for example, sulfuric acid, and hydrogen peroxide solution, or the mixed liquor of chloride and hydrogen peroxide solution. As shown in Fig.4 (b), the polysilicon 8 is replaced by the metal silicide 9 by this.
[0039]
Then, as shown in Fig.4 (c), a metal film (tungsten), for example, W, Al-Cu alloy (aluminum copper alloy), and Cu (copper) are formed with a sputtering method or a CVD method, and it patterns and forms the low resistance gate wire 6 which consists of a metal film.
[0040]
Embodiment 3.
In the above-mentioned embodiment 1 and 2, since polysilicon is formed on the channel regions 2 when patterning after polysilicon, lithography will be given on the height of the channel regions 2, for example, the level difference of 50-60 nm. Since there is such a level difference, patterning of polysilicon becomes difficult.
[0041]
Fig.5 is a cross sectional view showing the manufacturing process which manufactures the semiconductor device of this embodiment.
After forming the polysilicon 8 thickly so that the channel regions 2 may be embedded as shown in Fig.5 (a), it flattens by the CMP method. The thickness of the polysilicon 8 is formed at least more thickly than the total of the channel regions 2 and the hard surface mask blank 10. For example, when the channel regions 2 are 50 nm and the hard surface mask blank 10 is 30 nm, the thickness of the polysilicon 8 shall be 150 nm.
[0042]
Next, as shown in Fig.5 (b), the photoresist 11 is formed with a lithography technology on the flattened polysilicon 8, photoresist 11 is used as a mask, and the polysilicon 8 is patterned. The hard surface mask blank of a silicon oxide film or a silicon nitride film may be formed on the polysilicon 8 at this time, and photoresist may be formed on it.
[0043]
Next, as shown in Fig.5 (c), a silicon oxide film is formed with a CVD method, and it flattens by the CMP method, and the interlayer insulation film 5 is formed so that the top surface of the polysilicon 8 may be exposed.
[0044]
Subsequent processes form a gate wire like the above-mentioned embodiment 1. Or the rear gate wiring which metal-silicide-ized the polysilicon 8 like the above-mentioned embodiment 2 is formed.
[0045]
Since a lithography technology can be given on the flattened polysilicon 8 according to this

embodiment, patterning of the polysilicon 8 can be performed easily.
[0046]
Embodiment 4.
According to this embodiment, in order to prevent and low-resistance-ize depletion in polysilicon of the gate electrode 4, etc., it replaces with polysilicon and uses a metal film.
[0047]
Although it replaced with polysilicon and metal silicide was used in the above-mentioned embodiment 2, it can low-resistance-ize further by using a metal film.
[0048]
Fig.6 is a cross sectional view showing the manufacturing process which manufactures the semiconductor device of this embodiment. As shown in Fig.5 (c), after forming the polysilicon 8, as shown in Fig.6 (a), the polysilicon 8 is removed by the dry etching method. Since it is the object at this time to remove the polysilicon 8, anisotropic etching may not be needed but it may be isotropic etching.
[0049]
Next, as shown in Fig.6 (b), the metal film 12 which consists of the two-layer film of TiN film 12a and the W film 12b is embedded with a CVD method on the region which removed the polysilicon 8, and the interlayer insulation film 5.
[0050]
Since it is lacking in adhesion with the interlayer insulation film 5 which consists of a silicon oxide film, W forms TiN film 12a under the W film 12b as an adhesion layer. Since TiN does not react to the gate dielectric film 3 which consists of a silicon oxide film, degradation of the gate dielectric film 3 does not arise, either.
As a ground film of W film, adhesion with a silicon oxide film besides TiN is good, and it can be used if it is the metal or metallic compounds which does not react to the gate dielectric film 3.
[0051]
Next, as shown in Fig.6 (c), with a lithography technology, the metal film 12 is patterned and a gate wire is formed.
[0052]
Although this above-mentioned embodiment described about the process of removing the polysilicon 8, it may be made to remove the gate electrode 4 which consists of polysilicon after the process of Fig.3 (b) after the process of Fig.5 (c), as shown in Fig.7 (a). The gate electrode 4 and the gate wire 6 which were shown in Fig.7 (b) are obtained through the process as Fig.6 that a next process is the same.
[0053]
Embodiment 5.
In the above-mentioned embodiment 1 thru/or 4, the oxidizing film was used as the gate dielectric film 3. According to this embodiment, effective reduction in thickness of gate dielectric film is aimed at further, and a high dielectric constant film is used.
[0054]
Fig.8 is a cross sectional view showing the process of forming the high dielectric constant film of this embodiment. As shown in Fig.8 (a) after the process of Fig.6 (a), or the process of Fig.7 (a), the gate oxide film 3 which consists of a silicon oxide film is removed using fluoric acid, for example.
[0055]
Next, as shown in Fig.8 (b), the high dielectric constant films 13, such as an insulator layer with a high dielectric constant, for example, a hafnium oxide film, alumina membrane, a hafnium silicon oxide film, or a tantalum oxide film, are formed with a CVD method.
[0056]
Then, the gate electrode 4 and the gate wire 6 are formed by the process shown in Fig.6 (b) and (c).
[0057]
According to this embodiment, since the high dielectric constant film 13 is used for gate dielectric film, effective reduction in thickness of gate dielectric film is attained.
[0058]
Embodiment 6.
The hard surface mask blank 10 was saved in the above-mentioned embodiment 1 thru/or 5. The hard surface mask blank 10 is removed, the upper part of the channel regions 2 is also surrounded with the gate electrode 4, the electric field of a channel are controlled by this embodiment, and improved efficiency of a transistor is planned.
[0059]
Fig.9 is a cross sectional view showing the manufacturing process of this embodiment. As shown in Fig.9 (a), in the process of Fig.5 (c), it replaces with a silicon oxide film, the interlayer insulation film 14 which consists of a silicon nitride film is formed with a CVD method, and it flattens by the CMP method, and exposes the top surface of the gate electrode 4 which consists of polysilicon.
[0060]
Next, as shown in Fig.9 (b), the gate electrode 4 which consists of polysilicon, the hard surface mask blank 10, and the gate dielectric film 3 are removed by fluoric acid etc.
[0061]
Next, as shown in Fig.9 (c), a silicon oxide film or the gate dielectric film 15 which consists of a high dielectric constant film is formed with a CVD method.
[0062]
Then, the gate electrode 4 and the gate wire 6 which consists of a metal film are formed by the process shown in Fig.6 (b) and (c).
[0063]
Embodiment 7.
having saved the hard surface mask blank 10 in the above-mentioned embodiment 1 thru/or 6 -- polysilicon although formed gate electrode 4, after [which consists of polysilicon] removing the hard surface mask blank 10 -- which consists of -- it may form gate electrode 4.
[0064]
Fig.10 is a cross sectional view showing the process after removing the hard surface mask blank 10 of this embodiment. The hard surface mask blank 10 is removed by the dry etching

method after the process of Fig.2 (d).
[0065]
Next, as shown in Fig.10 (a), the gate dielectric film 3 is formed with a thermal oxidation method or a CVD method, after that, polysilicon is formed with a CVD method and the gate electrode 4 which consists of polysilicon is formed with lithography and the combination of etching.
[0066]
Next, as shown in Fig.10 (b), the interlayer insulation film 5 and the gate wire 6 which consists of a silicon oxide film are formed like Fig.3 (b) and the process of (c).
[0067]
According to this embodiment, the upper part of the channel regions 2 can also be surrounded with the gate electrode 4 at a easier process than the above-mentioned embodiment 6.
[0068]
Embodiment 8.
Since the work function of the gate electrode of both transistors will become the same in the CMIS circuit containing N type and a P type MIS transistor if the same metal is used for the gate electrode of N type and a P type MIS transistor, The threshold value of N type and each P type MIS transistor cannot be rationalized.
[0069]
In the circuit possessing FET of PMIS of a CMIS circuit, and NMIS both, this embodiment provides the manufacturing method which makes controllable threshold voltage of the gate electrode which consists of metal silicide.
[0070]
Fig.11 and 12 are the cross sectional views showing the manufacturing process of this embodiment. First, after forming FET of a PMIS region and a NMIS region in the process of Fig.3 or Fig.5, the top surface of the gate electrode 4 of a PMIS region is covered, and as shown in Fig.11 (a), the silicide preventing film 16 is formed so that the top surface of the gate electrode 4 of a NMIS region may be exposed. The silicide preventing film 16 is formed by removing the NMIS region of the silicon oxide film which formed 50 nm of silicon oxide films with the ordinary pressure CVD method, and formed membranes by lithography and dry etching, or wet etching, for example.
[0071]
Next, as shown in Fig.11 (b), 10-15 nm of cobalt films are formed with a PVD method as the first metal film 17, for example.
[0072]
Next, by performing heat treatment heated for 60 seconds at 400-600 degrees C, As polysilicon of the gate electrode 4 of a NMIS region and cobalt of the first metal film 17 are made to react and it was shown in Fig.11 (c). The gate electrode of a NMIS region is made into the first metal silicide 18 which consists of a cobalt silicide film, and the mixed liquor of sulfuric acid and hydrogen peroxide solution, etc. remove selectively an unreacted cobalt film and the silicide preventing film 16. As for the PMIS region gate electrode 4, at this time, a reaction with cobalt of the first metal film 17 is prevented by the silicide preventing film 16.
[0073]
Nickel and platinum besides cobalt can be used as the first metal film 17.
[0074]
next -- covering the first metal silicide 18 top of a NMIS region for the silicide preventing film 16, as shown in Fig.12 (a) -- the top surface of the gate electrode 4 of a PMIS region is exposure -- it forms like. This silicide preventing film 16 is formed by removing the silicon oxide film of the PMIS region of the silicon oxide film which formed 50 nm of silicon oxide films with the ordinary pressure CVD method, and formed membranes by lithography and dry etching, or wet etching, for example.
[0075]
Next, 10-15 nm of second metal films, for example, a titanium film, are formed with a PVD method, By performing heat treatment heated for 60 seconds at 600-800 degrees C, polysilicon of the gate electrode 4 and titanium of a second metal film are made to react, and as shown in Fig.12 (b), let the gate electrode 4 be the second metal silicide 19 which consists of titanium silicides. As for the first metal silicide 18 of a NMIS region, at this time, a reaction with titanium of a second metal film is prevented by the silicide preventing film 16.
[0076]
Tantalum or tungsten besides titanium can be used for a second metal film.
[0077]
As the silicide preventing film 16, it may be a silicon nitride film and a compound like titanium nitride (TiN) besides a silicon oxide film. After carrying out silicide formation of the metal film in TiN, it is simultaneously removable at the process of removing a metal film selectively.
[0078]
Next, the mixed liquor of sulfuric acid and hydrogen peroxide solution, etc. remove selectively an unreacted titanium film and the silicide preventing film 16.
[0079]
Next, as shown in Fig.12 (c), the gate wire 6 is formed like the above-mentioned embodiment 1.
[0080]
As mentioned above, since the gate electrode which consists of material which is different in a NMIS region PMIS region can be formed according to this embodiment, By choosing arbitrarily the first metal silicide film that differs in a work function, and a second metal silicide film as a gate electrode of FET of NMIS and PMIS, control of the threshold voltage of FET of each conductivity type is attained.
[0081]
Embodiment 9.
Fig.13 and Fig.14 are the cross sectional views showing the manufacturing process of this embodiment. Although the above-mentioned embodiment 8 showed the case where a metal silicide film was used as a gate electrode of FET of NMIS and PMIS, in this embodiment, it replaces with a metal silicide film and uses a metal film.
[0082]

First, after forming FET of a PMIS region and a NMIS region in the process of Fig.3 or Fig.5, as shown in Fig.13 (a). The top surface of the gate electrode 4 of a PMIS region is covered, the etching mask which consists of the photoresist 20 is formed by the lithography method so that the top surface of the gate electrode 4 of a NMIS region may be exposed, and the dummy gate electrode of a NMIS region is removed with an etching method.
[0083]
Next, after removing the photoresist 20, as shown in Fig.13 (b), the first metal film 21 for NMIS is formed by a sputtering method or CVD. As the first metal film 21, tantalum is formed, for example. As the first metal film 21, hafnium, magnesium, a zirconium, or aluminum other than tantalum can be used.
[0084]
Next, as shown in Fig.13 (c), it leaves the first metal film 21 only to the gate electrode part of a NMIS region by the CMP method or the etchback method.
[0085]
Next, as shown in Fig.14 (a), the top surface of the first metal film 21 (gate electrode) of a NMIS region is covered, The etching mask which consists of the photoresist 20 is formed by the lithography method so that the top surface of the gate electrode part of a PMIS region may be exposed, and the gate electrode part of a PMIS region is removed with an etching method.
[0086]
Next, as the photoresist 20 was removed, and the second metal film 22 for PMIS, for example, tungsten, is formed and it was shown in Fig.14 (b) by a sputtering method or CVD, it leaves the second metal film 22 only to the gate electrode part of a PMIS region by the CMP method or the etchback method.
[0087]
A ruthenium and a rhenium, or platinum besides tungsten can be used for the second metal film 22.
[0088]
Next, as shown in Fig.14 (c), the gate wire 6 is formed like the above-mentioned embodiment 1.
[0089]
As mentioned above, since the gate electrode which consists of material which is different in a NMIS region and a PMIS region can be formed according to this embodiment, By choosing arbitrarily the first metal film that differs in a work function, and a second metal film as a gate electrode of FET of NMIS and PMIS, control of the threshold voltage of FET of each conductivity type is attained.
[0090]
Embodiment 10.
This embodiment forms a high dielectric constant film as gate dielectric film in the above-mentioned embodiment 9.
[0091]
Fig.15 - Fig.17 are the cross sectional views showing the manufacturing process of this embodiment. First, after forming FET of a PMIS region and a NMIS region in the process of Fig.3 or Fig.5, as shown in Fig.15 (a). Cover the top surface of the gate electrode 8 of a PMIS region, and the etching mask which consists of the photoresist 20 is formed by the lithography method so that the top surface of the gate electrode of a NMIS region may be exposed, The dummy gate electrode of a NMIS region is removed with an etching method, and wet etching, such as fluoric acid, or the dry etching by HF gas removes the gate dielectric film of a gate electrode part further.
[0092]
Next, after removing the photoresist 20, as shown in Fig.15 (b), with a CVD method, 10-50-nm thickness film formation of the hafnium oxide film is carried out, and the first gate dielectric film 23 is formed.
[0093]
A compound with these, zirconium oxide, tantalum oxide and aluminum oxide, or silicon besides hafnium oxide can be used for the first gate dielectric film 23.
[0094]
The first gate dielectric film 23 may be a cascade screen of a high dielectric constant film and the silicon oxide film by the thermal oxidation method or a plasma oxidation method.
[0095]
Next, as the first metal film for NMIS is formed and it was shown in Fig.15 (c) with the sputtering method or the CVD method, it leaves the first metal film 21 only to the gate electrode part of a NMIS region by the CMP method or the etchback method.
[0096]
Next, as the top surface of the first metal film 21 of a NMIS region is covered, the etching mask which consists of the photoresist 20 is formed by the lithography method so that the top surface of the gate electrode 4 of a PMIS region may be exposed, and shown in Fig.16 (a). The gate electrode 4 of a PMIS region is removed with an etching method, and wet etching, such as fluoric acid, or the dry etching by HF gas removes the gate dielectric film of a gate electrode part further.
[0097]
Next, as the photoresist 20 is removed and it was shown in Fig.16 (b), with a CVD method, 10-50-nm thickness film formation of the hafnium oxide film is carried out, and the second gate dielectric film 24 is formed.
[0098]
A compound with these, zirconium oxide, tantalum oxide and aluminum oxide, or silicon besides hafnium oxide can be used for the second gate dielectric film 24.
[0099]
The second gate dielectric film 24 may be a cascade screen of a high dielectric constant film and the silicon oxide film by the thermal oxidation method or a plasma oxidation method.
[0100]
Next, as the second metal film 22 for PMIS, for example, tungsten, is formed and it was shown in Fig.16 (c) by a sputtering method or CVD, it leaves the second metal film 22 only to the dummy gate electrode part of a PMIS region by the CMP method or the etchback method.

[0101]
A ruthenium and a rhenium, or platinum besides tungsten can be used for the second metal film 22.
[0102]
Next, as shown in Fig.17, the gate wire 6 is formed like the above-mentioned embodiment 1.
[0103]
According to this embodiment, since the high dielectric constant film is used for the first gate dielectric film 23 and the second gate dielectric film 24, effective reduction in thickness of the 1st and the second gate dielectric film 23 and 24 is attained.
[0104]
[Effect of the Invention]
FET which has a silicon layer used as the source region, the channel regions, and the drain area which according to the semiconductor device concerning the present invention were formed so that it might project on a substrate, the insulator layer formed in the above-mentioned silicon layer surface, and a gate electrode which covers the above-mentioned channel regions from three directions via the above-mentioned insulator layer,
Since it has an interlayer insulation film which embeds the above-mentioned silicon layer, and the gate wire electrically connected to the surface of the projection direction of the gate electrode which was [above-mentioned] exposed so that the surface of the projection direction of the above-mentioned gate electrode may be exposed, resistance of a gate wire can be low-resistance-ized arbitrarily.
[0105]
The first silicon layer used as the source region, the channel regions, and the drain area which were formed so that it might project on a substrate, FET of a NMIS region which has the first insulator layer formed in the surface of the 1st silicon layer of the above, and a first gate electrode that covers the channel regions of the 1st silicon layer of the above from three directions via the 1st insulator layer of the above,
The second silicon layer used as the source region, the channel regions, and the drain area which were formed so that it might project on the above-mentioned substrate, FET of a PMIS region which has the second insulator layer formed in the surface of the 2nd silicon layer of the above, and a second gate electrode which covers the channel regions of the 2nd silicon layer of the above from three directions via the 2nd insulator layer of the above,
The interlayer insulation film which embeds FET of the above-mentioned NMIS region, and FET of a PMIS region so that the above 1st and the projection direction surface of a second gate electrode may be exposed,
Since it has the gate wire electrically connected to the surface of the projection direction of the gate wire electrically connected to the surface of the projection direction of the first gate electrode that was [above-mentioned] exposed, and a second gate electrode, resistance of a gate wire can be low-resistance-ized arbitrarily.
[0106]
The first process of forming FET which has the source region, the channel regions, and the drain area which according to the manufacturing method of the semiconductor device concerning the present invention pattern the silicon layer on a substrate and it projects on the above-mentioned substrate,
The second process of forming an insulator layer in the silicon layer surface which patterned [above-mentioned],
The 3rd process of forming the gate electrode which covers the three directions of the above-mentioned channel regions via the above-mentioned insulator layer,
The 4th process of forming an interlayer insulation film,
The fifth process which flattens the above-mentioned interlayer insulation film and at which it exposes the surface of the projection direction of the above-mentioned gate electrode from the above-mentioned interlayer insulation film,
A conductive film is formed, and since it has the sixth process of forming the gate wire electrically connected with the surface of the projection direction of the gate electrode which patterned and was [above-mentioned] exposed, resistance of a gate wire can be low-resistance-ized arbitrarily.
[0107]
The first process of forming the silicon layer of a NMIS region and a PMIS region which has the source region, the channel regions, and the drain area which pattern the silicon layer on a substrate and it projects on the above-mentioned substrate,
The second process of forming and making an insulator layer the silicon layer surface which patterned [above-mentioned],
The 3rd process of forming the gate electrode which consists of polysilicon or an amorphous silicon which covers the three directions of the above-mentioned channel regions via the above-mentioned insulator layer,
The 4th process of forming an interlayer insulation film,
The fifth process which flattens the above-mentioned interlayer insulation film and at which it exposes the surface of the projection direction of the above-mentioned gate electrode from the above-mentioned interlayer insulation film,
One gate electrode of the above-mentioned NMIS region or a PMIS region is covered with a silicide preventing film, The sixth process of covering the gate electrode of another side with a first metal film, making polysilicon or the amorphous silicon of the 1st metal film of the above, and the gate electrode of above-mentioned another side reacting by heat treatment, and making the gate electrode of above-mentioned another side into metal silicide,
Remove the above-mentioned silicide preventing film and it covers the gate electrode of above-mentioned another side of the above-mentioned NMIS region or a PMIS region with a silicide preventing film, The seventh process of covering above-mentioned one gate electrode with the second metal film of a different kind from the 1st metal film of the above, making above-mentioned one [the 2nd metal film of the above, and] polysilicon or amorphous silicon of a gate electrode reacting by heat treatment, and making above-mentioned one gate electrode into metal silicide,
A conductive film is formed, and since it has the eighth process of forming the gate wire electrically connected with the surface of the projection direction of each gate electrode which

patterned and was [above-mentioned] exposed, resistance of a gate wire and a gate electrode can be low-resistance-ized arbitrarily.
[0108]
The first process of forming the silicon layer of a NMIS region and a PMIS region which has the source region, the channel regions, and the drain area which pattern the silicon layer on a substrate and it projects on the above-mentioned substrate,
The second process of forming an insulator layer in the silicon layer surface which patterned [above-mentioned],
The 3rd process of forming the dummy gate electrode which consists of polysilicon or an amorphous silicon which covers the three directions of the above-mentioned channel regions via the above-mentioned insulator layer,
The 4th process of forming an interlayer insulation film,
The fifth process which flattens the above-mentioned interlayer insulation film and at which it exposes the surface of the projection direction of the above-mentioned dummy gate electrode from the above-mentioned interlayer insulation film,
One dummy gate electrode of FET of the above-mentioned NMIS region or a PMIS region is covered with a first etching mask, The sixth process of embedding a first metal film into the portion which removed the dummy gate electrode of another side, removed the 1st etching mask of the above, and removed the dummy gate electrode of above-mentioned another side, and forming a gate electrode,
The dummy gate electrode of above-mentioned another side of the above-mentioned NMIS region or a PMIS region is covered with a second etching mask, The seventh process of embedding the second metal film of a different kind from the 1st metal film of the above into the portion which removed above-mentioned one dummy gate electrode, removed the 2nd etching mask of the above, and removed above-mentioned one gate electrode, and forming a gate electrode,
A conductive film is formed, and since it has the eighth process of forming the gate wire electrically connected with the surface of the projection direction of each gate electrode which patterned and was [above-mentioned] exposed, resistance of a gate wire and a gate electrode can be low-resistance-ized arbitrarily.
[Brief Description of the Drawings]
[Drawing 1]It is a cross sectional view showing the semiconductor device of embodiment 1.
[Drawing 2]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 1.
[Drawing 3]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 1.
[Drawing 4]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 2.
[Drawing 5]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 3.
[Drawing 6]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 4.
[Drawing 7]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 4.
[Drawing 8]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 5.
[Drawing 9]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 6.
[Drawing 10]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 7.
[Drawing 11]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 8.
[Drawing 12]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 8.
[Drawing 13]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 9.
[Drawing 14]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 9.
[Drawing 15]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 10.
[Drawing 16]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 10.
[Drawing 17]It is a cross sectional view showing the manufacturing process of the semiconductor device of embodiment 10.
[Explanations of letters or numerals]
1 An embedding oxidizing zone, 2 channel regions, 2a source region,
2b A drain area, 3, 15 gate dielectric film, 4 gate electrodes,
5 and 14 An interlayer insulation film, 6 gate wires, and 7 and 12 Metal film,
8 Polysilicon, 9 metal silicide, and 10 Hard surface mask blank,
11, 20, 24, and 28 Photoresist, 12a TiN film, 12b W film,
13 A high dielectric constant film and 16 A silicide preventing film, and 17 and 21 The 1st metal film,
18 First metal silicide and 19 The 2nd metal silicide,
22 A second metal film and 23 The 1st gate dielectric film and 24 The 2nd gate dielectric film,
25 Silicon, 26 silicon oxide films, 27 silicon nitride films,
29 Sacrificing oxide film.

[Translation done.]

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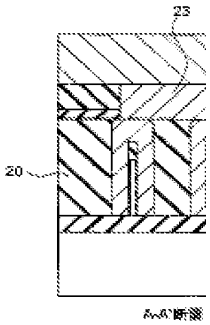
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention]
[0001]
The present invention relates to a multi-gated mode field effect transistor and a manufacturing method for the same.
[Background of the Invention]
[0002]
High integration and highly-efficient-izing of LSI have been realized by micronization of the field effect transistor (FET (Field Effect Transistor)) which is the basic constitution element, and the improved efficiency accompanying it. The performance of FET is determined by the smallness of the leakage current of the size of the driving current at the time of ON operation, and the channel at the time of OFF. In order to attain large driving current and small leakage current after a 45-nm generation according to the international semiconductor road map, a plurality of breakthrough technology is needed.
[0003]
About reduction of leakage current, since the tolerance over a short channel effect is high, FD (Fully-Depleted) device which depleted channel regions completely is expected as a next-generation basic element structure. The multi-gated mode field effect transistor is observed especially. For example, it differs from the single gate type field effect transistor which controls the potential within a channel only by the gate electrode formed on the surface of a channel as shown in the Patent document 1 from one way, The multi-gated mode field effect transistor has the structure which encloses minute channel regions with a gate electrode. The advantage of the structure is improving the potential controllability of channel regions, suppressing deterioration of the potential barrier by short channelization of a device, and being able to reduce the leakage current at the time of OFF.
[0004]
It is threshold value control of a device to become important here. There are the characteristics that FD device has the low voltage by which a reversal electric charge is generated as compared with a bulk type device. For this reason, when the conventional gate electrode material is used for FD device, the new gate electrode material in which the leakage current in an OFF state (0 volt) enlarges too much is needed. Now, the type (metal gate) which uses metal itself as a gate electrode, and the type (silicide gate) using the compound (it is called a silicide when a semiconductor is silicon) of metal and a semiconductor are mentioned as the candidate.
[Patent document 1] Japanese Published Patent Application No. 2005-86024 (JP2005-86024A)
[Description of the Invention]
[Problem to be solved by the invention]
[0005]
In applying this metal gate and a silicide gate to a cubic shape multi-gate field effect transistor, the problem on some manufacturing processes occurs. In particular, it is metallic contamination to become a problem. In order to realize very minute gate length, sufficient flat surface is needed for the lithography before processing of a gate electrode. However, since the metal used for a metal gate or a silicide can become the center of the generation recombination of a carrier, and a path of charge trapping or leakage current if it is incorporated into parent semiconductors (silicon etc.) or gate dielectric film, there is a possibility of degrading the performance of a device remarkably. Therefore, it cannot flatten directly to a metal gate electrode or a silicide electrode using CMP (Chemical Mechanical Polishing). When carrying out silicide formation of the gate electrode, existence of a natural oxide film becomes an obstacle, but this natural oxide film cannot be removed in the conventional manufacturing method.
[0006]
The present invention is made in consideration of the above-mentioned situation.
Even if the object performs a flattening process, it is providing a multi-gated mode field effect

CLOSE



Representative dr

Representative drawing

Previous Document 5/7

transistor which can prevent metallic contamination, and a manufacturing method for the same.

[Means for solving problem]
[0007]
It is characterized by a manufacturing method of a multi-gated mode field effect transistor by a first modes of the present invention comprising the following.
A process of arranging in parallel and forming a plurality of semiconductor layers on a substrate.
A process of forming a protective film in a top surface of said plurality of semiconductor layers, respectively.
The process of forming in each of said plurality of semiconductor layers the 1st insulating layer that covers the both side surfaces of each semiconductor layer, the both side surfaces of the aforementioned protective film, and a top surface, A process at which a top surface of each of 1st above-mentioned insulating layer is exposed by forming the 1st interlayer insulation film in the whole surface, and flattening the 1st above-mentioned interlayer insulation film, A process of forming a plurality of holes in a position where the 1st above-mentioned insulating layer was removed by removing the 1st above-mentioned insulating layer selectively, respectively, A process of forming gate dielectric film in both side surfaces of the aforementioned semiconductor layer in a plurality of aforementioned holes, A process of depositing the 1st polysilicon film on the whole surface so that a plurality of aforementioned holes may be embedded, A process of separating the 1st above-mentioned polysilicon film into a plurality of 2nd polysilicon films while exposing a top surface of the 1st above-mentioned interlayer insulation film by flattening the 1st above-mentioned polysilicon film, A process of forming a gate electrode-shaped mask on a plurality of 2nd above-mentioned polysilicon films, A process of patterning a plurality of 2nd above-mentioned polysilicon films using the aforementioned mask, A process of forming a side wall which consists of an insulator which inserts a plurality of 2nd patterned above-mentioned polysilicon films into a gate length direction, and a process, at which the aforementioned protective film is patterned using the aforementioned mask and the aforementioned side wall, and a top surface of a plurality of aforementioned semiconductor layers is exposed selectively, The process of injecting an impurity into a plurality of semiconductor layers exposed selectively, and forming a source/drain area, A process which removes the aforementioned mask and at which it exposes a top surface of a plurality of 2nd above-mentioned polysilicon films, A process of changing into a silicide a plurality of 2nd above-mentioned polysilicon films in which a top surface was exposed, respectively, A process of forming the 2nd interlayer insulation film in the whole surface, forming in the 2nd above-mentioned interlayer insulation film an opening which leads to each of the aforementioned silicide, and forming a connection part of metal connected with each of the aforementioned silicide in common by embedding the aforementioned opening, and a process of forming wiring linked to the aforementioned connection part.

[0008]
It is characterized by a manufacturing method of a multi-gated mode field effect transistor by a second modes of the present invention comprising the following.
A process of arranging in parallel and forming a plurality of semiconductor layers on a substrate.
A process of forming a protective film in a top surface of said plurality of semiconductor layers, respectively.
The process of forming in each of said plurality of semiconductor layers the 1st insulating layer that covers the side surface of each semiconductor layer, the side surface of the aforementioned protective film, and a top surface, A process at which a top surface of each of 1st above-mentioned insulating layer is exposed by forming the 1st interlayer insulation film in the whole surface, and flattening the 1st above-mentioned interlayer insulation film, A process of forming a plurality of holes in a position where the 1st above-mentioned insulating layer was removed by removing the 1st above-mentioned insulating layer selectively, respectively, A process of forming gate dielectric film in both side surfaces of the aforementioned semiconductor layer in each of a plurality of aforementioned holes, A process of forming a gate metal film which covers each side surface and bottom surface of a plurality of aforementioned holes, and the aforementioned gate dielectric film and the aforementioned protective film in the aforementioned hole, So that the aforementioned gate metal film on the aforementioned protective film may not expose a process of forming a polysilicon film which covers the aforementioned gate metal film, and the aforementioned polysilicon film and the aforementioned gate metal film in each of a plurality of aforementioned hole. A process to etch, a process of depositing a polysilicon film again after that so that a plurality of aforementioned holes may be embedded, respectively, and a process of separating the aforementioned polysilicon film into a plurality of polysilicon layers while exposing a top surface of the 1st above-mentioned interlayer insulation film by flattening the aforementioned polysilicon film, The process of forming a gate electrode-shaped mask on a plurality of aforementioned polysilicon layers, A process of patterning a plurality of aforementioned polysilicon layers using the aforementioned mask, A process of forming a side wall which consists of an insulator which inserts a plurality of patterned aforementioned polysilicon layers into a gate length direction, A process at which the aforementioned protective film is patterned using the aforementioned side wall, and a top surface of a plurality of aforementioned semiconductor layers is exposed selectively, A process of injecting an impurity into a plurality of semiconductor layers exposed selectively, and forming a source/drain area, A process which removes the aforementioned mask and at which it exposes each top surface of a plurality of aforementioned polysilicon layers, A process of forming the 2nd interlayer insulation film in the whole surface, forming in the 2nd above-mentioned interlayer insulation film an opening which leads to each of a plurality of aforementioned polysilicon layers, and forming a connection part of metal connected with each of the aforementioned polysilicon layer in common by embedding the aforementioned opening, and a process of forming wiring linked to the aforementioned connection part.

[0009]

A multi-gated mode field effect transistor by the 3rd modes of the present invention is provided with the following.
A plurality of semiconductor layers of the 1st conductivity type provided so that it might stand in a row on a substrate.
The source/drain area of the 2nd conductivity type separated and provided by each of said plurality of semiconductor layers
The channel regions provided between the aforementioned source region and the aforementioned drain area by each of said plurality of semiconductor layers, A protective film provided by each top surface of the aforementioned channel regions, and gate dielectric film provided by each both side surfaces of the aforementioned channel regions, A plurality of gate electrodes which contain a metallic element provided so that each top surface of the aforementioned channel regions might pinch the aforementioned protective film while providing so that the aforementioned gate dielectric film may be inserted into each both side surfaces of the aforementioned channel regions, A gate wire connected to an interlayer insulation film provided on the aforementioned substrate so that each side surface of a plurality of aforementioned gate electrodes might be covered, a connection part which connects each top surface of a plurality of aforementioned gate electrodes in common, and the aforementioned connection part.

[Effect of the Invention]
[0010]
According to the present invention, even if it performs a flattening process, a multi-gated mode field effect transistor which can prevent metallic contamination, and a manufacturing method for the same can be provided.
[Best Mode of Carrying Out the Invention]
[0011]
Before describing the multi-gated mode field effect transistor by the embodiment of the present invention, in order to clarify more the characteristics of this multi-gated mode field effect transistor, with reference to Fig.1 A - Fig.5 B, it describes in detail about the conventional problem. In the following descriptions, although described taking the case of a n type channel transistor, it is applicable also to a p type channel transistor.
[0012]
As shown in Fig.1 A, and 1B and 1C, the insulator layer 4 is formed on the support substrate 2, By LPCVD (Low Pressure Chemical Vapor Deposition) etc., on the SOI substrate by which SOI layer 6 was formed on the insulator layer 4, deposit about 100 nm of silicon nitride as the protective film 8 of a channel, and by publicly known element isolation technology, Element isolation is performed. By the existing patterning technology, SOI layer 6 is patterned and a channel is formed. Channel width is 20 nm. They are a cross sectional view when it cuts by cutting-plane-line A-A' which shows Fig.1 A in a plan view and shows Fig.1 B to Fig.1 A, and a cross sectional view when Fig.1 C is cut by cutting-plane-line B-B' shown in Fig.1 A.
[0013]
Subsequently, as shown in Fig.2 A, 2B, and 2C, about 1 nm of silicon dioxide is formed using the RTO (Rapid Thermal Oxidation) method etc. as the gate dielectric film 9, after that, plasma nitriding is carried out and a dielectric constant is enlarged. 250 nm of polysilicon films 10A which furthermore serve as a gate electrode are deposited in LPCVD etc. Here, in order to flatten the surface, CMP is performed by using the silicon nitride film 8 as an etching stopper, and 60 nm of polysilicon films 10B are deposited again. The natural oxide film 100 will be formed in the surface of the polysilicon film 10A formed previously at this time. They are a cross sectional view when it cuts by cutting-plane-line A-A' which shows Fig.2 A in a plan view and shows Fig.2 B to Fig.2 A, and a cross sectional view when Fig.2 C is cut by cutting-plane-line B-B' shown in Fig.2 A.
[0014]
Then, as shown in Fig.3 A, 3B, and 3C, the hard surface mask blank layer (not shown) which consists of a silicon nitride film is deposited on it. And the above-mentioned hard surface mask blank layer is patterned using photolithography technique etc. Then, if the polysilicon film 10B is patterned by RIE etc. by using the patterned hard surface mask blank layer as a mask, a gate electrode part will be formed. Here, although offset spacers etc. may be formed further, it is not illustrating.
[0015]
In order for gate length to perform patterning of 50 nm or less by a photolithography in formation of this gate electrode, sufficient flat surface is needed. Therefore, although Fig.2 A, 2B, and a CMP process that was used for 2C are used, if it is going to apply a full silicide gate and a metal gate, the problem of a process will occur. For example, in the case of a full silicide gate, as shown in Fig.4 A, the metal (for example, nickel etc.) 11 is deposited by a sputtering on the polysilicon film 10B, and silicide formation of the polysilicon film 10B is carried out by heat-treating at 400 degrees C - 500 degrees C. However, since the natural oxide film 100 is not uniformly formed as shown in Fig.4 (B), in the region in which the natural oxide film 100 is formed, The natural oxide film 100 will be the barrier of diffusion of the metal 11, and it will become uneven reacting it of silicide formation in the region of the polysilicon film 10A which is placed below the natural oxide film 100. As a result, it is divided into the portion 13 used as a silicide, and the portion which remains with the polysilicon film 10A as shown in Fig.4 B. In this case, in the transistor which has the channel 6 which is placed at the left in Fig.4 B, since the both sides of the channel 6 serve as the silicide 13, the threshold value of the both sides of the channel 6 gathers. However, in the transistor which has the channel 6 which is placed at the right, since the left-hand side of the channel 6 serves as the silicide 13 and right-hand side serves as the polysilicon film 10A, only the difference of the work function of polysilicon and a silicide will be in the state where threshold values differ.
[0016]
In LSI, since the variation in the threshold value between transistors poses a serious problem, it is a fatal defect that threshold values differ in a plurality of channels of each transistor. In such a state, variation is produced also in resistance of a gate electrode and it becomes an obstacle at the time of high frequency operation.
[0017]

On the other hand, if the interlayer insulation film 18 is deposited after depositing the metal electrode 17 and the polysilicon film 10 so that the semiconductor layer 6 used as channel regions may be surrounded as shown in Fig.5 A when a metal is used for a gate electrode, Since the top surface of the interlayer insulation film 18 serves as uneven shape, in order to perform minute lithography, as shown in Fig.5 B, it is necessary to flatten. At this time, since the stopper has structure only with the silicon nitride film 8 when the CMP method is used for flattening, he will be etched to the metal electrode 17. When the metal electrode 17 is etched by the CMP method, the particles of a metal will be extended to an entire wafer surface, and a wafer will be polluted with metal.
This is nonpermissible at all on LSI manufacture. Therefore, when a metal gate is used, it must not flatten, but lithography of a gate electrode must be performed, and there is a problem that a minute gate cannot be formed.
[0018]
The inventors were able to get the multi-gated mode field effect transistor which solves these problems, as a result of striving for research intensively. Below, this is described as an embodiment.
[0019]
(A 1st embodiment)
The plan view of the multi-gated mode field effect transistor by a 1st embodiment of the present invention is shown in Fig.6. The multi-gated mode field effect transistor of this embodiment, As shown in Fig.6, two fin 50_1 and 50_2, It has the gate 70 formed so that the n type drain area 60b formed in the n type source region 60a formed in one end of these fins and the end of another side, and two fin 50_1 and 50_2 might be straddled. Each of fin 50_1 and 50_2 is provided with the p type semiconductor layer used as channel regions, the gate dielectric film formed in the side surface of these channel regions, and the protective film formed in the top surface of the above-mentioned semiconductor layer. A n type semiconductor layer is formed in the semiconductor layer of the both sides of the channel regions of each fin, it is connected to the n type source region 60a or the n type drain region 60b, and these n type semiconductor layers are also called the n type source region 60a or the n type drain region 60b. The gate 70 is formed so that the gate dielectric film on channel regions may be covered.
[0020]
Next, the manufacturing method of the multi-gated mode field effect transistor of this embodiment is described with reference to Fig.7 A thru/or Fig.19 D. According to this embodiment, although described about an n-type channel field effect transistor, if the ionic species which carry out an ion implantation are changed, it is producible similarly about a p type channel field effect transistor. Fig.7 A, Fig.8 A, Fig.9 A, Fig.10 A, Fig.11 A, Fig.12 A, Fig.13 A, Fig.14 A, Fig.15, Fig.16, Fig.17, Fig.18, and Fig.19 A, The cross sectional view cut by cutting-plane-line A-A' shown in Fig.6, Fig.7 B, Fig.8 B, Fig.9 B, Fig.10 B, Fig.11 B, Fig.12 B, Fig.13 B, Fig.14 B, and Fig.19 B, The cross sectional view cut by cutting-plane-line B-B' shown in Fig.6, Fig.7 C, Fig.8 C, Fig.9 C, Fig.10 C, Fig.11 C, Fig.12 C, Fig.13 C, Fig.14 C, and Fig.19 C, The cross sectional view cut by cutting-plane-line C-C' shown in Fig.6, Fig.7 D, Fig.8 D, Fig.9 D, Fig.10 D, Fig.11 D, Fig.12 D, Fig.13 D, Fig.14 D, and Fig.19 D are the cross sectional views cut by cutting-plane-line D-D' shown in Fig.6.
[0021]
First, as shown in Fig.7 A, and 7B, 7C and 7D, the insulator layer 4 is formed on the support substrate 2, On the SOI substrate by which SOI layer 6 was formed on the insulator layer 4, about 100 nm of silicon nitride is deposited in LPCVD (Low Pressure Chemical Vapor Deposition) etc. as the protective film 8 of a channel, The insulator layer 19 which consists of TEOS (Tetra Ethyl Ortho Silicate) is deposited on this protective film 8. Then, publicly known element isolation technology performs element isolation. By the existing patterning technology, SOI layer 6 is patterned and a channel is formed. Channel width is 20 nm. The protective film 8 and the insulator layer 19 are formed in the top surface of the channel 6.
[0022]
Next, as shown in Fig.8 A, and 8B, 8C and 8D, the insulator layer 19 is further deposited and the side wall 19a which consists of the insulator layer 19 is formed in the side surface of the channel 6 and the protective film 8 by etching by RIE. The insulator layer 19a used as this side wall has also covered the top surface of the protective film 8. By repeating this work several times, height (height from the protective film 8) is made as high (for example, 300 nm) as possible as thickly (for example, 50 nm - 100 nm) as possible for the width (thickness of the side wall of the direction which intersects perpendicularly with this side surface from the side surface of the channel 6) of the side wall 19a. At this time, the insulator layer 19a used as the side wall 19a serves as the form where the top surface was round.
[0023]
Then, as shown in Fig.9 A, and 9B, 9C and 9D, the insulator layer 20 is deposited so that the insulator layer 19a used as a side wall may be covered, and the top surface of the insulator layer 19a is exposed by flattening this insulator layer 20 by CMP. At this time, by carrying out over etching somewhat on the top surface of the insulator layer 19a, rather than stopping etching, the portion into which near the summit of the insulator layer 19a was round is deleted, and an opening is made wide.
[0024]
Next, as shown in Fig.10 A, and 10B, 10C and 10D, by etching with a solution the insulator layer 19a which has covered the side surface and top surface of the channel 6 and the protective film 8, it removes completely and forms a hole. At this time, if rare HF etc. are used, even some insulator layers 4 will be etched, but. In the case of 1 micrometer etc., the thickness of the insulator layer 4 can use the difference of an etching rate from TEOS (material of the insulator layer 19a) and the silicon oxidizing film (insulator layer 4) by rare HF, and by adjusting etching time, it can leave the insulator layer 4 so that it may become sufficient thickness. Then, where the above-mentioned hole is formed, the film thickness used as the gate dielectric film 9 forms about 1 nm of silicon dioxide in the side surface of the channel regions 6 for example, using the RTO method, after that, plasma nitriding is carried out and the dielectric constant of the gate dielectric film 9 is enlarged. The polysilicon film 10 used as a gate electrode is deposited in LPCVD etc. setting up the temperature of the furnace of LPCVD low at this time -- a reaction -- the above-mentioned hole is completely embedded by depositing

polysilicon more rate-limiting. if this is made to deposit at an elevated temperature -- supply of a raw material -- it is because a polysilicon film will be formed more rate-limiting, a polysilicon film accumulates preferentially on the insulator layer 20, so a void will remain in the portion of a hole. Then, the flat surface suitable for gate lithography is obtained by flattening the polysilicon film 10 using the CMP method.

[0025]

Next, as shown in Fig.11 A, and 11B, 11C and 11D, gate mask material is deposited, this gate mask material is patterned using a lithography technology, and the mask 21 is formed. Then, while patterning polysilicon film 10 using this mask 21, slimming is performed and the gate electrode-shaped polysilicon film 10 is formed. At this time, RIE removes the polysilicon film 10 and the gate dielectric film 9 on the semiconductor layer 6 used as a source/drain area (Fig.11 B, 11C).

[0026]

Next, the gate sidewall material 12 which consists of SiN is deposited on the whole surface, for example. Then, the side wall 12 is formed in the side part of a polysilicon film by performing RIE to this gate sidewall material (Fig.12 C, 12D). By carrying out over etching, using the difference of height with the semiconductor layer 6 used as the gate electrode 10, and a source/drain area, it leaves the side wall of the polysilicon film 10 (Fig.12 C), and removes the side wall of the semiconductor layer 6 used as a source/drain area at this time (Fig.12 B). The semiconductor layer 6 used as a source/drain area is exposed by removing simultaneously the channel protection film 8 on the semiconductor layer 6 used as a source/drain area by this over etching (Fig.12 B, 12C). As shown in Fig.12 D, recess etching also of the insulator layer 20 of the region which is not covered with the mask 12 is carried out by this over etching, and that height becomes low by it.

[0027]

Next, as shown in Fig.13 B and 13C, the exposed semiconductor layer 6 is selectively etched by using the side wall 12 as a mask, and the height from the insulator layer 4 is made low. Then, the ion implantation of the P (phosphorus) is carried out to a film surface at the angle leaning from vertical direction 7 times or more from an oblique direction as a n type source / a dopant for drain area formation, for example (Fig.13 C). Thereby, a n type source region and the drain areas 60a and 60b are formed, and the p type semiconductor region 6 between the source region 60a and the drain area 60b turns into channel regions. At this time, as shown in Fig.13 A, and 13C and 13D, the mask 21 is not removed. When forming a p type source / drain area, B (boron) is used as a dopant.

[0028]

Next, as shown in Fig.14 A, and 14B, 14C and 14D, after removing the gate mask material 21, the gate electrode 13 which carried out full silicide formation of the polysilicon film 10 completely is formed by performing metal sputters, such as nickel, and heat treatment. Since the natural oxide film is not formed in the polysilicon film 10 at this time, diffusion of nickel takes place uniformly and the gate electrode 13 whole carries out full silicide formation. Silicide formation also of the source region 60a and the drain area 60b is carried out at this time (Fig.14 B, 14C).

[0029]

As shown in Fig.14 A in this state, the two gate electrodes 13 are divided and, the way things stand, voltage cannot be applied to the gate electrode 13. Therefore, it is necessary to connect between gate electrodes using upper wiring. Then, after the silicide process described by Fig.14 A thru/or 14D is completed, tens of nm SiN film 22a is deposited as an etching stopper of contact. Then, the interlayer insulation film 22b is deposited on this SiN film 22a, and it flattens by performing CMP (Fig.15). Even if unevenness of the top surface of the interlayer insulation film 22b before performing CMP is large, when performing CMP, SiN film 22a works as an etching stopper.

[0030]

Then, the contact hole (not shown) which leads to the interlayer insulation film 22b and the insulator layer 22 which consists of SiN film 22a at the gate electrode 13 is opened using a lithography technology and RIE. And this contact hole is embedded for TiN-W etc., and the plug 23 is formed (Fig.16). Deposit an interlayer insulation film (not shown) and it uses a lithography technology and RIE, The slot for wiring processing is formed in this interlayer insulation film, the metallic wiring 24, such as Al-Cu, is embedded in this slot, and a voltage impressing terminal (not shown) is connected with the gate electrode 13 via the plug 23 and the metallic wiring 24 (Fig.17). Thereby, multi-gated mode FET of this embodiment is completed.

[0031]

Thus, if the gate wire resistance in the usual FUSI gate FinFET is compared with multi-gated mode FET of this formed embodiment, At the usual FUSI gate FinFET, since the metallic wiring 24 thick in this embodiment is spread to a signal spreading the gate electrode of very thin width, and a transistor is driven, the adverse effect of the wiring resistance to the gate electrode in which a high frequency signal is applied can be eased substantially. For example, if the height which has covered the Fin upper part of 20 nm and a FUSI electrode for width (gate length) shall be 120 nm in width of 60 nm and Al-Cu wiring, and 1 micrometer in height as shown in Fig.18 (a) and 18 (b), Double digit can be enlarged as the area S which a signal spreads, and if the difference in resistivity is taken into consideration, gate resistance can be further made low.

[0032]

TEOS and the insulator layer 19 may be formed by SiN, and TEOS and the gate mask material 21 may be formed [the channel supplementary insulation film 8 in this embodiment] for the insulator layer 20 by SiN.

[0033]

Although the number of the fin was described as two pieces by this embodiment, it can also be considered as three or more fins.

As described above, according to this embodiment, metallic contamination can be prevented even if it performs a flattening process. Gate resistance can be reduced.

[0034]

(A 2nd embodiment)

Next, the manufacturing method of multi-gated mode FET by a 2nd embodiment of the present invention is described with reference to Fig.19 A thru/or Fig.21 D. Multi-gated mode FET manufactured by the manufacturing method of this embodiment is a metal gate type. Fig.19 A, Fig.20 A, and Fig.21 A are the cross sectional views cut by cutting-plane-line A-A' shown in Fig.6. Fig.19 -- B -- 20 -- B -- 21 -- B -- Fig.6 -- being shown -- a cutting plane line -- B-B -- ' -- having cut -- a cross sectional view -- Fig.19 -- C -- 20 -- C -- 21 -- C -- Fig.6 -- being shown -- a cutting plane line -- C-C -- ' -- having cut -- a cross sectional view -- Fig.19 -- D -- 20 -- D -- 21 -- D -- Fig.6 -- being shown -- a cutting plane line -- D-D -- ' -- having cut -- a cross sectional view -- it is .

[0035]

First, it carries out using the same process as the manufacturing process to Fig.7 A thru/or Fig.9 D described by full silicide gate FET of a 1st embodiment. As shown in the surface of the hole formed by removing the insulator layer 19a shown in Fig.9 A thru/or Fig.9 D at Fig.19 A, and 19B, 19C and 19D. After forming the metal film 17 for metal gates by MOCVD (Metal-Organic Chemical Vapor Deposition), the above-mentioned hole is embedded with the polysilicon film 10 using an LPCVD method. At this time, the surface of the gate dielectric film 9 in the above-mentioned hole and the channel protection film 8 is covered with the metal film 17 for metal gates, and the polysilicon film 10 is formed in that outside. The metal film 17 for metal gates and the polysilicon film 10 adhere also on the insulator layer 20. For this reason, when CMP is performed in this state, metallic contamination will be spread to the whole wafer.

[0036]

Then, as shown in Fig.20 A, and 20B, 20C and 20D, the polysilicon film 10 on top and the metal film 17 of the insulator layer 20 are removed by etching the polysilicon film 10 and the metal film 17 by a RIE method. At this time, the semiconductor layer 6 and the protective film 8 used as a fin are covered with the polysilicon film 10, and are not etched by the above-mentioned RIE method. For this reason, the metal film 17 of the top surface of the insulator layer 20 is controllable with sufficient controllability. Thus, it will embed with the protective film 8 and the protective film 8, and the metal film 17 and the polysilicon film 10 of a side surface of the gate dielectric film 9 will remain using the difference of the height from the insulator layer 4 of the insulator layer 20.

[0037]

Then, as shown in Fig.21 A, and 21B, 21C and 21D, again, the polysilicon 10 is deposited and the flat surface suitable for gate lithography is obtained by performing CMP, without causing metallic contamination. Henceforth, henceforth the process shown in Fig.11 A thru/or Fig.17 described by a 1st embodiment and the same process are performed, and multi-gated mode FET is completed. However, the process of forming the polysilicon film 10 shown henceforth [Fig.11 A] is unnecessary, and is unnecessary. [of the process which carries out a silicide] Thus, the cross sectional view of the multi-gated mode field effect transistor of this formed embodiment is shown in Fig.22.

[0038]

It is the same as that of a 1st embodiment that TEOS and the insulator layer 19 may be formed by SiN, and TEOS and the gate mask material 21 may be formed [the channel supplementary insulation film 8 in this embodiment] for the insulator layer 20 by SiN.

[0039]

As described above, according to this embodiment, metallic contamination can be prevented even if it performs a flattening process.

[Brief Description of the Drawings]

[0040]

[Drawing 1]The figure showing the manufacturing process of conventional multi-gated mode FET.

[Drawing 2]The figure showing the manufacturing process of conventional multi-gated mode FET.

[Drawing 3]The figure showing the manufacturing process of conventional multi-gated mode FET.

[Drawing 4]The figure showing the problem of the manufacturing process of conventional multi-gated mode FET.

[Drawing 5]The figure showing the problem of the manufacturing process of conventional multi-gated mode FET.

[Drawing 6]The plan view of multi-gated mode FET by a 1st embodiment of the present invention.

[Drawing 7]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 8]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 9]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 10]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 11]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 12]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 13]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 14]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 15]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 16]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 17]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 1st embodiment.

[Drawing 18]The figure which describes the effect of multi-gated mode FET by a 1st

embodiment.
[Drawing 19]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 2nd embodiment.
[Drawing 20]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 2nd embodiment.
[Drawing 21]The cross sectional view showing the manufacturing process of multi-gated mode FET by a 2nd embodiment.
[Drawing 22]The cross sectional view of multi-gated mode FET by a 2nd embodiment.
[Explanations of letters or numerals]
[0041]
2 Support substrate
4 Insulator layer
6 Semiconductor layer (SOI layer)
8 Channel protection film
9 Gate dielectric film
10 Polysilicon film
11 Metal for silicides
12 Gate side wall
13 Gate electrode (silicide)
17 Metal for metal gates
18 Interlayer insulation film
19 Insulator layer
20 Insulator layer
21 Gate mask material
22 Insulator layer
22a SiN film
22b Interlayer insulation film
23 Plug
24 Metallic wiring
50_1, 50_2 fin
60a Source region
60b Drain area
70 Gate
100 Natural oxide film

Notices on Issues | Privacy Policy | Questionnaire

[Translation done.]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/024,750
Filing Date	March 24, 2016
First Inventor	Milton C. Webb, et al.
Art Unit	2822
Examiner Name	Potter, Roy Karl
Attorney Docket No.	P60397US Conf. No. 9490

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted concurrently with the payment of the Issue Fee. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The references listed were cited in a communication in a counterpart Japan application on July 26, 2017. (Copy enclosed herewith).

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OR

☐ None

☒ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	09-22-2017
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal */Sheri Villarreal/* *Date* *09-22-17*

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15/024,750	03/24/2016	Milton C. WEBB	P60397US

CONFIRMATION NO. 9490

31817
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POA ACCEPTANCE LETTER

OC000000093439628

Date Mailed: 08/15/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/12/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

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15/024,750	03/24/2016	2822	4880	P60397US	25	4

CONFIRMATION NO. 9490

CORRECTED FILING RECEIPT

31817
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OC000000093439699

Date Mailed: 08/15/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

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Applicant(s)

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Power of Attorney: The patent practitioners associated with Customer Number 31817

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US2013/076673 12/19/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/024,750**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 31817

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 31817

OR

☐

Firm or Individual Name			
Address			
City			
Country			
Telephone		Email	

Assignee Name and Address: Intel Corporation
2200 Mission College Boulevard
Santa Clara, California 95054

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Lisa Hopkinson	Date	24 June 2016
Name	Lisa Hopkinson	Telephone	480.715.9827
Title	Administrator of Patents		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: INTEL CORPORATION

Application No./Patent No.: 15/024,750 Filed/Issue Date: 03-24-2016

Titled: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

INTEL CORPORATION, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 032781, Frame 0116, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Al AuYeung/	08/12/2017
Signature	Date
Al AuYeung	Reg. No. 35,432
Printed or Typed Name	Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Milton	~~C.~~ Clair	WEBB	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Aloha	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	20180 SW Inglis Drive
Address 2	

City	Aloha	State/Province	OR
Postal Code	97007	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Mark		BOHR	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Aloha	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	19475 SW Suncrest Lane
Address 2	

City	Aloha	State/Province	OR
Postal Code	97007	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tahir		GHANI	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	14191 NW Stonebridge Drive		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country i	US

Remove

Inventor 4

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Szuya	S.	LIAO	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Hillsboro	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	7214 NE Shaleen Street		
Address 2			
City	Hillsboro	State/Province	OR
Postal Code	97124	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	~~45209~~ 31817		
Email Address	intelpatent@schwabe.com	Add Email	Remove Email

Application Information:

Title of the Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same		
Attorney Docket Number	P60397US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	~~45209~~ 31817		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	a 371 of international	PCT/US13/76673	2013-12-19

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. [X] INTEL CORPORATION

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Applicant:

Address 1	2200 Mission College Boulevard		
Address 2			
City	Santa Clara	**State/Province**	CA
Country	US	Postal Code	95054
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	~~/Justin K. Brask/~~ /Al AuYeung/			Date (YYYY-MM-DD)	2017-08-12
First Name	~~Justin K.~~ Al	Last Name	~~Brask~~ AuYeung	Registration Number	~~61080~~ 35432

Additional Signature may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (S U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	30062920
Application Number:	15024750
International Application Number:	
Confirmation Number:	9490
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton C. WEBB
Customer Number:	45209
Filer:	Aloysius T.C. Auyeung
Filer Authorized By:	
Attorney Docket Number:	P60397US
Receipt Date:	12-AUG-2017
Filing Date:	24-MAR-2016
Time Stamp:	19:43:35
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	P60397US_POA.pdf	313213 23e8a85954533c13fe1bb6aee06a5bb81315e45f	no	1
Warnings:					

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	P60397US_373c.pdf	118585 70cb4ff8b032889d709e73d0158eb591f809 87ad	no	3
Warnings:					
Information:					
3	Application Data Sheet	P60397US_Supp_ADS.pdf	1915131 b3dbd213ecec3a3d8ab1b87d0dda7a0352f 517a9	no	9
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
			Total Files Size (in bytes):	2346929	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/024,750
	Filing Date	3/24/2016
	First Named Inventor	Webb, Milton C.
	Group Art Unit	2822
	Examiner Name	Feeney, Brett A.
Sheet 1 of 1	Attorney Docket No: P60397US	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.K.P/		US-20070080380	04/12/2007	CHANG, PETER	
/R.K.P/		US-20110291188	12/01/2011	CHENG, KANGGUO, et al.	
/R.K.P/		US-20130134506	05/30/2013	YAGISHITA, ATSUSHI	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
/R.K.P/		TW-201017772	05/01/2010	WEI, ANDY, et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/R.K.P/		International Preliminary Report on Patentability for PCT Application No. PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) mailed June 30, 2016, 7 pages.	
/R.K.P/		Non-Final Office Action and Search Report for Taiwan Patent Application No. 103137443 (Attorney Docket No. P60397TW) mailed June 3, 2016, 3 pgs.	

EXAMINER /ROY K POTTER/ DATE CONSIDERED 05/28/2017

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/024,750	03/24/2016	Milton C. WEBB	P60397US	9490

45209 7590 08/08/2017

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER
POTTER, ROY KARL

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
08/08/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

inteldocs_docketing@cpaglobal.com
Database_Group@bstz.com

UNITED STATES DEPARTMENT OF COMMERCE
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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
15/024,750	24 March, 2016	WEBB ET AL.	P60397US

		EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 1279 Oakmead Parkway Sunnyvale, CA 94085-4040		ROY POTTER	
		ART UNIT	PAPER
		2822	20170802

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

.This communication is being sent with an initialed copy of the Information Disclosure Statement of 9/28/16	
	/ROY POTTER/ Primary Examiner, Art Unit 2822

PTO-90C (Rev.04-03)

Doc Code: N572

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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/024,750	03/24/2016	Milton C. WEBB	P60397US

CONFIRMATION NO. 9490

OC000000093179054

45209
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

Cc:
SCHWABE, WILLIAMSON & WYATT, P.C.
C/O CPA GLOBAL
900 2ND AVENUE SOUTH, SUITE 600
MINNEAPOLIS, MN 55402

08/03/2017

DENIAL OF REQUEST FOR POWER OF ATTORNEY

The request for Power of Attorney filed 07/31/17 is acknowledged. However, the request cannot be granted at this time for the reason stated below.

☐ The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.

☐ The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.

☐ The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73(c) has not been received.

☐ The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.

☐ The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.

The signature(s) of ____, a co-inventor in this application, has been omitted Power of Attornny will be entered upon receipt of confirmation signed by said co-inventor(s).

☐ The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent and Trademark Office.

☐ Only one Customer Number can be designated for the Power of Attorney in an application. The Customer Number that was captured is the first Customer Number provided on the Power of Attorney document.

☐ A request under 37 CFR 1.48 to add an inventor was granted in this application, however, no power of attorney consistent with the power of attorney granted by the originally named inventive entity has been

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received. Thus, the addition of the inventor has resulted in the loss of power of attorney in the application. See 37 CFR 1.32(e).

☑ The power of attorney has not been accepted because the party who is giving power of attorney has not been identified. Power of attorney may only be signed by the applicant for patent (37 CFR 1.42) or the patent owner. A patent owner who was not the applicant must appoint any power of attorney in compliance with 37 CFR 3.71 and 3.73. See 37 CFR 1.32(b)(4).

☐ The power of attorney from the inventors has not been accepted because it is a copy from a prior national application for which benefit is claimed and the continuing application names an inventor who was not named as an inventor in the prior application.

☐ The power of attorney from the inventors has not been accepted because the power of attorney must be signed by the applicant for patent. See 37 CFR 1.32(b)(4).

☑ Any request to correct or update the name of the applicant must include an application data sheet (ADS) in compliance with 37 CFR 1.76 specifying the correct or updated name of the applicant in the applicant information section. Any request to change the applicant after an original applicant has been specified under 37 CFR 1.46(b) must include a new ADS in compliance with 37 CFR 1.76 specifying the applicant in the applicant information section and comply with 37 CFR 3.71 and 3.73. See 37 CFR 1.46(c).

Any inquiries regarding this notice should be directed to the Application Assistance Unit at 571-272-4200.

Application Assistance Unit
571-272-4200

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/024,750	03/24/2016	Milton C. WEBB	P60397US

CONFIRMATION NO. 9490

45209
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

MISCELLANEOUS NOTICE



Date Mailed: 08/03/2017

A communication which cannot be delivered in electronic form has been mailed to the applicant.

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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/024,750	03/24/2016	2822	4880	P60397US	25	4

CONFIRMATION NO. 9490

CORRECTED FILING RECEIPT

45209
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

OC000000093148598

Date Mailed: 08/01/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Milton C. WEBB, Aloha, OR;
Mark BOHR, Aloha, OR;
Tahir GHANI, Portland, OR;
Szuya S. LIAO, Hillsboro, OR;

Applicant(s)

INTEL CORPORATION, Santa Clara, CA;
Milton Clair Webb, Aloha, OR
Mark Bohr, Alhoa, OR
Tahir Ghani, Portland, OR
Szuya S. Liao, Hillsboro, OR

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US2013/076673 12/19/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/04/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/024,750**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

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PTO/AIA/80 (07-12)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 31817

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 31817

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

Assignee Name and Address: Intel Corporation
2200 Mission College Boulevard
Santa Clara, California 95054

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Lisa Hopkinson	Date	24 June 2016
Name	Lisa Hopkinson	Telephone	480.715.9827
Title	Administrator of Patents		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: INTEL CORPORATION

Application No./Patent No.: 15/024,750 Filed/Issue Date: 03-24-2016

Titled: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

INTEL CORPORATION, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 032781, Frame 0116, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Michael A. Bernadicou/	07-31-2017
Signature	Date
Michael A. Bernadicou	Reg. No. 35,934
Printed or Typed Name	Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	29933263
Application Number:	15024750
International Application Number:	
Confirmation Number:	9490
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton C. WEBB
Customer Number:	45209
Filer:	Michael A. Bernadicou/Lynn Scardina
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P60397US
Receipt Date:	31-JUL-2017
Filing Date:	24-MAR-2016
Time Stamp:	13:36:03
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	P60397US_POA.pdf	313213 23e8a85954533c13fe1bb6aee06a5bb81315e45f	no	1

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	P60397US_373c.pdf	118647 b2977f688cfb7274aea64f89bb46f406e9385ee6	no	3
Warnings:					
Information:					
			Total Files Size (in bytes):	431860	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

45209 7590 07/06/2017

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER
POTTER, ROY KARL

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/06/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/024,750	03/24/2016	Milton C. WEBB	P60397US	9490

TITLE OF INVENTION: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/06/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

45209 7590 07/06/2017
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/024,750	03/24/2016	Milton C. WEBB	P60397US	9490

TITLE OF INVENTION: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/06/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
POTTER, ROY KARL	2822	257-369000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/024,750	03/24/2016	Milton C. WEBB	P60397US	9490

45209 7590 07/06/2017

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER	
POTTER, ROY KARL	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/06/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/024,750	Applicant(s) WEBB ET AL.	
	Examiner ROY POTTER	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amedment of 5/12/17*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-45*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 3/24/16
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ROY POTTER/
Primary Examiner, Art Unit 2822

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15024750	WEBB ET AL.
	Examiner	Art Unit
	ROY POTTER	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/07/2017	06/26/2017							
1	1	✓	=							
2	2	O	=							
3	3	O	=							
4	4	O	=							
5	5	O	=							
6	6	O	=							
7	7	O	=							
8	8	✓	=							
9	9	=	=							
10	10	=	=							
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31	31		=							
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34	34		=							
35	35		=							
36	36		=							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15024750	WEBB ET AL.
	Examiner	Art Unit
	ROY POTTER	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/07/2017	06/26/2017							
37	37		=							
38	38		=							
39	39		=							
40	40		=							
41	41		=							
42	42		=							
43	43		=							
44	44		=							
45	45		=							

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BIB DATA SHEET

CONFIRMATION NO. 9490

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/024,750	03/24/2016 RULE	257	2822	P60397US

APPLICANTS
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INVENTORS
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Mark BOHR, Aloha, OR;
Tahir GHANI, Portland, OR;
Szuya S. LIAO, Hillsboro, OR;

**** CONTINUING DATA ***************************
This application is a 371 of PCT/US2013/076673 12/19/2013

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
05/04/2016

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/ Roy Potter / Examiner's Signature	☐ Initials	OR	15	25	4

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Sunnyvale, CA 94085-4040
UNITED STATES

TITLE
Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same

FILING FEE RECEIVED		
4880	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15024750	WEBB ET AL.
	Examiner	Art Unit
	ROY POTTER	2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/66628 or H01L29/66795 or H01L29/785	2/7/2017	RP
H01L29/0649 or H01L29/785 or H01L29/66545 or H01L29/66795 or H01L29/41791 or H01L23/535 or H01L27/0924 or H01L21/823821 or H01L21/76895 or H01L21/823878	6/26/2017	RP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	H01L29/0649 or H01L29/785 or H01L29/66545 or H01L29/66795 or H01L29/41791 or H01L23/535 or H01L27/0924 or H01L21/823821 or H01L21/76895 or H01L21/823878	6/26/2017	RP

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	Unknown
	Filing Date	December 19, 2013
	First Named Inventor	Webb, M.
	Group Art Unit	0
	Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No: P60397US	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.K.P/		US-2007/0054464	03/08/2007	ZHANG, Guowei	
/R.K.P/		US-2008/0080380	04/03/2008	LEE, Kwang il, et al.	
/R.K.P/		US-20110021027	01/27/2011	JOHNSON, Frank S.	
/R.K.P/		US-2013/0020615	01/24/2013	FAN, Su Chen, et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
/R.K.P/		KR-20050082099		CHOI, Jung A., et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/R.K.P/		International Search Report and Written Opinion from PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) Mailed September 26, 2014, 10 pages.	

EXAMINER /ROY K POTTER/	DATE CONSIDERED	06/26/2017

Based on PTO/SB/08A(09-08) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4154	high with dielectric same gate same fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 13:03
L2	62398	(H01L29/0649 or H01L29/785 or H01L29/66545 or H01L29/66795 or H01L29/41791 or H01L23/535 or H01L27/0924 or H01L21/823821 or H01L21/76895 or H01L21/823878).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 13:03
L3	3458	L1 and L2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 13:03
L4	656	self with aligned and L3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/26 13:03

6/26/2017 1:03:48 PM

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	29634	(H01L29/0649 or H01L29/785 or H01L29/66545 or H01L29/66795 or H01L29/41791 or H01L23/535 or H01L27/0924 or H01L21/823821 or H01L21/76895 or H01L21/823878).cpc.	US-PGPUB; USPAT	OR	ON	2017/06/26 11:34
L8	3869	high with dielectric same gate same fin	US-PGPUB; USPAT	OR	ON	2017/06/26 11:35
L9	3297	l7 and l8	US-PGPUB; USPAT	OR	ON	2017/06/26 11:35

6/26/2017 11:36:14 AM

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15024750	WEBB ET AL.
	Examiner	**Art Unit**
	ROY POTTER	2822

CPC						
Symbol					**Type**	**Version**
H01L		29	/	0649	F	2013-01-01
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H01L		29	/	66795	I	2013-01-01
H01L		29	/	785	I	2013-01-01
H01L		21	/	76895	I	2013-01-01
H01L		21	/	823821	I	2013-01-01
H01L		21	/	823878	I	2013-01-01
H01L		23	/	535	I	2013-01-01
H01L		27	/	0924	I	2013-01-01
H01L		29	/	41791	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
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NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 45	
/ROY POTTER/ Primary Examiner.Art Unit 2822 (Primary Examiner)	06/26/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 7D

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15024750	WEBB ET AL.
	Examiner	**Art Unit**
	ROY POTTER	2822

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
		H 0 1 L 29 / 06 (2006.01.01)	
CROSS REFERENCE(S)		H 0 1 L 29 / 66 (2006.01.01)	
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	45	
/ROY POTTER/ Primary Examiner.Art Unit 2822	06/26/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7D

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15024750	WEBB ET AL.
	Examiner	**Art Unit**
	ROY POTTER	2822

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

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15	15	31	31												
16	16	32	32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 45	
/ROY POTTER/ Primary Examiner.Art Unit 2822 (Primary Examiner)	06/26/2017 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 7D

U.S. Patent and Trademark Office Part of Paper No. 20170528

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Webb, et al.	Examiner: Potter, Roy Karl
Application No.: 15/024,750	Art Unit: 2822
Filed: March 24, 2016	Confirmation No.: 9490
For: Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 CFR §1.111

Dear Examiner:

This is in response to the Office Action mailed February 13, 2017. Applicants respectfully request the Examiner to enter this Amendment and consider the following remarks.

The Listing of Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 15 of this paper.

I hereby certify that this correspondence is being deposited via EFS Web on the date below:

May 12, 2017
Date of Deposit

/Lisa Puccinelli/
Lisa Puccinelli

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application. Please enter new claims 36-45.

Listing of Claims:

1. (Currently Amended) A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length in a first direction;

a gate structure disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction, wherein the gate structure has an uppermost surface; and

a pair of gate edge isolation structures centered with the semiconductor fin, wherein a first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure, and wherein the pair of gate edge isolation structures has an uppermost surface co-planar with or above the uppermost surface of the gate structure.

2. (Original) The semiconductor structure of claim 1, further comprising:

source and drain regions disposed in the semiconductor fin, on either side of the gate structure; and

a first trench contact disposed over the source region and a second trench contact disposed over the drain region, each of the first and second trench contacts having a first end opposite a second end in the second direction, wherein the first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the first trench contact and to the first end of the second trench contact, and the second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.

3. (Original) The semiconductor structure of claim 1, further comprising:

a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin;

a second gate structure disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction, wherein the second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure; and

a third gate edge isolation structure disposed directly adjacent to the second end of the second gate structure, wherein the third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.

4. (Original) The semiconductor structure of claim 3, further comprising:

a local interconnect disposed above and electrically coupling the first and second gate structures.

5. (Original) The semiconductor structure of claim 4, wherein the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

6. (Original) The semiconductor structure of claim 3, wherein the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.

7. (Original) The semiconductor structure of claim 1, wherein the gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

8. (Original) The semiconductor structure of claim 1, wherein the pair of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

9. (Original) A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length;

alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact

disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and

a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and

a gate local interconnect disposed above one of the gate structures and between a pair of the plurality of gate edge isolation structures.

10. (Original) The semiconductor structure of claim 9, further comprising:

a dielectric cap disposed on the gate local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

11. (Original) The semiconductor structure of claim 9, further comprising:

a trench contact local interconnect disposed above one of the trench contacts and between a second pair of the plurality of gate edge isolation structures.

12. (Original) The semiconductor structure of claim 11, further comprising:

a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the second pair of the plurality of gate edge isolation structures.

13. (Original) The semiconductor structure of claim 9, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

14. (Original) The semiconductor structure of claim 9, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

15. (Original) A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length;

alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and

a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and

a trench contact local interconnect disposed above one of the trench contacts and between a pair of the plurality of gate edge isolation structures.

16. (Original) The semiconductor structure of claim 15, further comprising:

a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

17. (Original) The semiconductor structure of claim 15, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

18. (Original) The semiconductor structure of claim 15, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

19. (Original) A method of fabricating a semiconductor structure, the method comprising:

forming first and second parallel semiconductor fins above a substrate;

forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins, wherein the dummy spacers of the first semiconductor fin are non-continuous with the dummy spacers of the second semiconductor fin;

forming an isolation structure between the dummy spacers of the first and second semiconductor fins;

removing the dummy spacers; and

forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure.

20. (Original) The method of claim 19, further comprising:

forming a first pair of trench contacts over the first semiconductor fin and a second pair of trench contacts over the second semiconductor fin, wherein the first and

pairs of trench contacts are directly adjacent to, and separated from one another by, the isolation structure.

21. (Original) The method of claim 19, further comprising:

subsequent to forming an isolation structure and prior to removing the dummy spacers, recessing the first and second semiconductor fins.

22. (Original) The method of claim 19, wherein forming the dummy spacers comprises forming and etching a polycrystalline silicon layer.

23. (Original) The method of claim 19, wherein forming the isolation structure comprises depositing and planarizing a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

24. (Original) The method of claim 19, wherein forming one or both of the first and second replacement gate structures comprises forming a high-k gate dielectric layer and a metal gate electrode.

25. (Original) The method of claim 19, further comprising:

forming a local interconnect above and electrically coupling the first and second replacement gate structures.

26. (Previously Presented) An integrated circuit structure, comprising:

a first fin comprising silicon, the first fin having a longest dimension along a first direction;

a second fin comprising silicon, the second fin having a longest dimension along the first direction;

an isolation material between the first fin and the second fin;

a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;

a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;

a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and

a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation

structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.

27. (Previously Presented) The integrated circuit structure of claim 26, wherein the gate edge isolation structure comprises silicon and nitrogen.

28. (Previously Presented) The integrated circuit structure of claim 26, wherein the dielectric material is in contact with the gate edge isolation structure.

29. (Previously Presented) The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

30. (Previously Presented) The integrated circuit structure of claim 29, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.

31. (Previously Presented) The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

32. (Previously Presented) The integrated circuit structure of claim 26, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.

33. (Previously Presented) The integrated circuit structure of claim 32, further comprising:

a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.

34. (Previously Presented) The integrated circuit structure of claim 33, wherein the local interconnect electrically couples the first gate structure to the second gate structure.

35. (Previously Presented) The integrated circuit structure of claim 33, further comprising:

a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

36. (New) The semiconductor structure of claim 1, wherein the uppermost surface of the pair of gate edge isolation structures is co-planar with the uppermost surface of the gate structure.

37. (New) The semiconductor structure of claim 1, wherein the uppermost surface of the pair of gate edge isolation structures is above the uppermost surface of the gate structure.

38. (New) A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length in a first direction;

a gate structure disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction, wherein the gate structure comprises a high-k gate dielectric layer and a metal gate electrode; and

a pair of gate edge isolation structures centered with the semiconductor fin, wherein a first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

39. (New) The semiconductor structure of claim 38, further comprising:

source and drain regions disposed in the semiconductor fin, on either side of the gate structure; and

a first trench contact disposed over the source region and a second trench contact disposed over the drain region, each of the first and second trench contacts having a first end opposite a second end in the second direction, wherein the first of the pair of gate edge isolation structures is disposed directly adjacent to the first end

of the first trench contact and to the first end of the second trench contact, and the second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.

40. (New) The semiconductor structure of claim 38, further comprising:

a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin;

a second gate structure disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction, wherein the second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure; and

a third gate edge isolation structure disposed directly adjacent to the second end of the second gate structure, wherein the third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.

41. (New) The semiconductor structure of claim 40, further comprising:

a local interconnect disposed above and electrically coupling the first and second gate structures.

42. (New) The semiconductor structure of claim 41, wherein the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

43. (New) The semiconductor structure of claim 40, wherein the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.

44. (New) The semiconductor structure of claim 38, wherein the gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

45. (New) The semiconductor structure of claim 38, wherein the pair of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

REMARKS

The following remarks are provided in response to the office action mailed February 13, 2017 ("Office Action") in which the Office Action:

- rejected claims 1 and 8 under 35 U.S.C. §102(a)(2) as being anticipated by US Pub. 2005/0056888 to Youn et al. (hereinafter Youn).
- allowed claims 9-25.
- objected to claims 2-7 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- did not address claims 26-35 added by preliminary amendment on January 20, 2017.

The Applicants respectfully request reconsideration of the above referenced patent application for the following reasons:

Claims 1 and 8 rejection under 35 U.S.C. §102(a)(2)

Claims 1 and 8 are rejected under 35 U.S.C. §102(a)(2) as being anticipated by Youn.

Independent claim 1, from which claim 8 depend, is herein amended. Applicants respectfully request reconsideration of claims 1 and 8 in view of the amendments and the following arguments.

Amended independent claim 1 is directed to a semiconductor structure. The semiconductor structure includes the features, "*a semiconductor fin disposed above a*

substrate and having a length in a first direction," "*a gate structure disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction, wherein the gate structure has an uppermost surface*," and "***a pair of gate edge isolation structures centered with the semiconductor fin**, wherein a first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure, and **wherein the pair of gate edge isolation structures has an uppermost surface co-planar with or above the uppermost surface of the gate structure***." (Emphasis added.)

That is, Applicants teach, and claim in claims 1 and 8, a semiconductor structure having a pair of gate edge isolation structures centered with a semiconductor fin, where the pair of gate edge isolation structures has an uppermost surface co-planar with or above the uppermost surface of a gate structure. (*See* Applicants' specification, e.g., Figure 3D, shown below: a semiconductor structure having a pair of gate edge isolation structures 314 (left two 314 structures) centered with a semiconductor fin 302A, where the pair of gate edge isolation structures 314 has an uppermost surface above the uppermost surface of a gate structure 320. *See also* Applicants' specification, e.g., Figure 4F, shown below: a semiconductor structure having a pair of gate edge isolation structures 406 (left two 406 structures) centered with a semiconductor fin 402 (left 402 structure), where the pair of gate edge isolation structures 406 has an uppermost surface co-planar with the uppermost surface of a gate structure 412/410.)

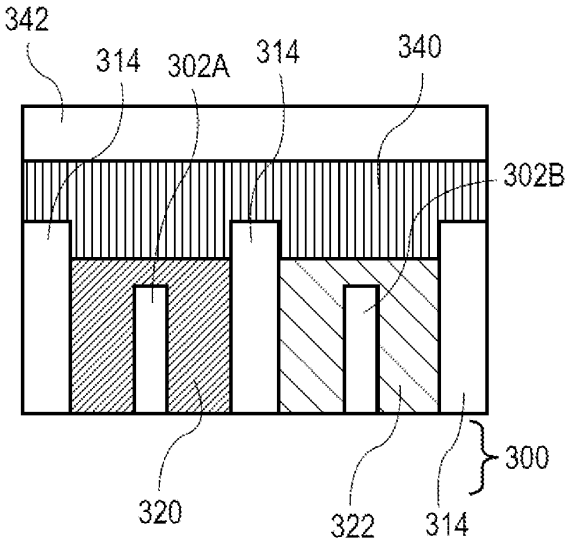


FIG. 3D

Figure 3D of Applicants' specification.

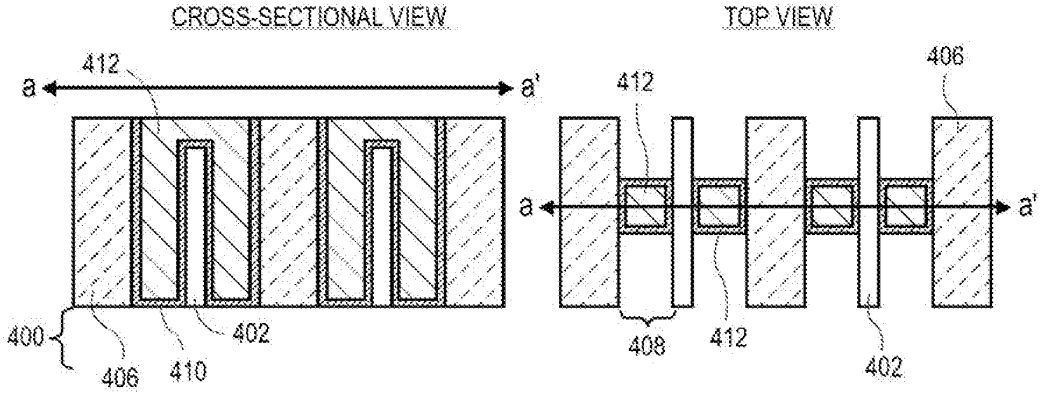


FIG. 4F

Figure 4F of Applicants' specification.

Applicants do not understand Youn as disclosing a semiconductor structure having a pair of gate edge isolation structures centered with a semiconductor fin, where the pair of gate edge isolation structures has an uppermost surface co-planar with or above the uppermost surface of a gate structure, as is taught and claimed by Applicants.

Applicants understand Youn as disclosing a double gate field effect transistor. In particular, Youn discloses a double gate field effect transistor protruded fins 102 of a bulk silicon substrate 100b. Device isolation films such as shallow trench isolation (STI) films 170a are formed in a device isolation region. A gate line 190 is formed over the protruded fins 102 and over the STI films 170a. (*See* Youn, e.g., paragraphs 0020-0026, and Figure 1B, shown below; *note that the Office Action incorrectly points to pad insulating layer 110a as being a gate structure*.)

FIG. 1B

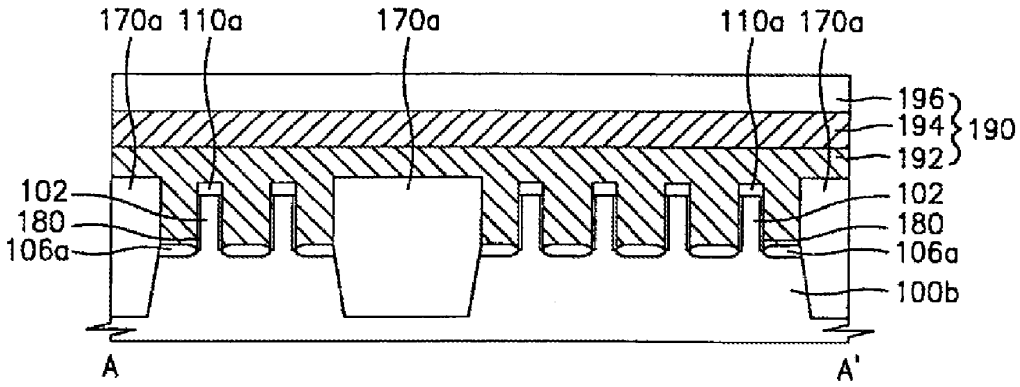


Figure 1B of Youn.

However, Applicants understand the STI films 170a of Youn as having an uppermost surface below an uppermost surface of the gate line 190 of Youn. By contrast, Applicants teach and claim gate edge isolation structures having an uppermost surface co-planar with or above an uppermost surface of a gate structure.

As such, Applicants do not understand Youn as disclosing at least, "*wherein the pair of gate edge isolation structures has an uppermost surface co-planar with or above the uppermost surface of the gate structure*," as is taught by Applicants and claimed in claims 1 and 8. Accordingly, the Applicants respectfully request that the Examiner remove the rejection of claims 1 and 8.

Allowance of claims 9-25

The Office Action allowed claims 9-25.

The Applicants respectfully acknowledge the allowance of claims 9-25.

Objection to claims 2-7

The Office Action objected to claims 2-7 as being dependent upon a rejected base claim, but indicated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-7 depend from amended independent claim 1. Applicants respectfully request that the Examiner remove the rejection of claims 2-7 at least in view of the amendments to and above arguments regarding independent claim 1.

Office Action did not address Claims 26-35

The Office Action did not address claims 26-35 added by preliminary amendment on January 20, 2017.

Independent claim 26, from which claims 26-35 depend, is directed to an integrated circuit structure. The integrated circuit structure includes the features, "*a first fin comprising silicon, the first fin having a longest dimension along a first direction*," "*a second fin comprising silicon, the second fin having a longest dimension along the first direction*," "*an isolation material between the first fin and the second fin*," "*a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode*," "*a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode*," "*a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material*," and "*a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure*."

Applicants do not understand Youn as disclosing Applicants' invention as taught and claimed in claims 26-35. Accordingly, the Examiner should find claims 26-35 in condition for allowance.

New Claims 36-45

New claim 36 depends from amended independent claim 1. New claim 36 adds the feature, "*wherein the uppermost surface of the pair of gate edge isolation structures is co-planar with the uppermost surface of the gate structure*." (*See* Applicants' specification, e.g., Figure 4F, shown above.) Applicants respectfully request consideration of new claim 36 at least in view of the amendments to and above arguments regarding independent claim 1.

New claim 37 depends from amended independent claim 1. New claim 37 adds the feature, "*wherein the uppermost surface of the pair of gate edge isolation structures is above the uppermost surface of the gate structure*." (*See* Applicants' specification, e.g., Figure 3D, shown above.) Applicants respectfully request consideration of new claim 37 at least in view of the amendments to and above arguments regarding independent claim 1.

New independent claim 38, from which new claims 39-45 depend, represents the allowable subject matter of claim 7 as rewritten in independent form. Accordingly, Applicants respectfully request consideration of new claims 38-45.

CONCLUSION

The Applicants submit that they have overcome the Office Action's objections to and rejections of the claims and that they have the right to claim the invention as set forth in the listed claims. The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN, L.L.P.

May 12, 2017
Date

/Justin K. Brask/
Justin K. Brask
Reg. No. 61,080

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Sunnyvale, CA 94085-4040
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Facsimile: (503) 439-6073

Electronic Patent Application Fee Transmittal

Application Number:	15024750
Filing Date:	24-Mar-2016
Title of Invention:	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same
First Named Inventor/Applicant Name:	Milton C. WEBB
Filer:	Justin K. Brask
Attorney Docket Number:	P60397US

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1615	10	80	800
INDEPENDENT CLAIMS IN EXCESS OF 3	1614	1	420	420
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1220**

Electronic Acknowledgement Receipt	
EFS ID:	29197163
Application Number:	15024750
International Application Number:	
Confirmation Number:	9490
Title of Invention:	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same
First Named Inventor/Applicant Name:	Milton C. WEBB
Customer Number:	45209
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US
Receipt Date:	12-MAY-2017
Filing Date:	24-MAR-2016
Time Stamp:	17:46:34
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1220
RAM confirmation Number	051517INTEFSW00004777504238
Deposit Account	504238
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.17 (Patent application and reexamination processing fees) 37 CFR 1.19 (Document supply fees)	

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

37 CFR 1.492 (National application filing, search, and examination fees)

37 CFR 1.492(a) (Basic national fee only)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Intel_P60397US_response_to_OA_05-12-17.pdf	314755 fa495b8b3072756753828 3cef418330740c46141	yes	22

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	14
	Applicant Arguments/Remarks Made in an Amendment	15	22

Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32309 ef605d0e0422dd7a963b3ad91cf352af62bf19ca	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	347064		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/024,750	03/24/2016	Milton C. WEBB	P60397US	9490

45209 7590 02/13/2017

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER
POTTER, ROY KARL

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
02/13/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

inteldocs_docketing@cpaglobal.com
Database_Group@bstz.com

Office Action Summary	Application No. 15/024,750	Applicant(s) WEBB ET AL.	
	Examiner ROY POTTER	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) 1-25 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) 9-25 is/are allowed.

7)☒ Claim(s) 1 and 8 is/are rejected.

8)☒ Claim(s) 2-7 is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claims 1 – 25 are pending.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

Claims 1 and 8 are rejected under 35 U.S.C. 102(a) (2) as being anticipated by Youn et al.

Youn et al., U.S. Patent Application Publication 2015/0056888 discloses a double gate FINFET. A substrate 100b supports the device. Semiconductor fins 102 are disposed over a substrate. A gate structure 110a is disposed over each semiconductor fin. As shown in Figure 18, STI film 170a are formed between two sets of fins 102. These act as isolation structures. These films are parallel with the fins and centered on them. The material of the isolation structures are silicon oxide.

Allowable Subject Matter

Claims 2 – 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9 – 25 are allowed.

The prior art does not disclose a trench contact disposed over each of the source region and the drain region.

The prior art does not disclose or suggest the recited method comprising forming dummy spacers adjacent to semiconductor FINS, removing the dummy spacers and forming gate structures separated by an isolation structure located between the dummy spacers and the fins.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROY POTTER whose telephone number is (571)272-1842. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571 270 5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ROY POTTER/
Primary Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 15/024,750	Applicant(s)/Patent Under Reexamination WEBB ET AL.	
	Examiner ROY POTTER	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2005/0056888 A1	03-2005	Youn, Jae-Man	H01L21/823437	257/331
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15024750	WEBB ET AL.
	Examiner	Art Unit
	ROY POTTER	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/07/2017								
	1	✓								
	2	O								
	3	O								
	4	O								
	5	O								
	6	O								
	7	O								
	8	✓								
	9	=								
	10	=								
	11	=								
	12	=								
	13	=								
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	16	=								
	17	=								
	18	=								
	19	=								
	20	=								
	21	=								
	22	=								
	23	=								
	24	=								
	25	=								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L19	1	trench with endcap with contact and finfet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/01/02 21:00
L20	2	trench with endcap with contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/01/02 21:00

1/2/2017 9:01:31 PM

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15024750	WEBB ET AL.
	Examiner	Art Unit
	ROY POTTER	2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/66628 or H01L29/66795 or H01L29/785	2/7/2017	RP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Webb, et al.	Examiner: Potter, Roy Karl
Application No.: 15/024,750	Art Unit: 2822
Filed: March 24, 2016	Confirmation No.: 9490
For: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Examiner:

This Preliminary Amendment is being filed in the above matter before the mailing of a first Office Action from the United States Patent and Trademark Office. Applicants respectfully request the Examiner to enter this Amendment and consider the following remarks.

The Listing of Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 11 of this paper.

I hereby certify that this correspondence is being deposited via EFS Web on the date below:

January 20, 2017
Date of Deposit

/Gigi Hoover/
Gigi Hoover

Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length in a first direction;

a gate structure disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction; and

a pair of gate edge isolation structures centered with the semiconductor fin, wherein a first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

2. (Original) The semiconductor structure of claim 1, further comprising:

source and drain regions disposed in the semiconductor fin, on either side of the gate structure; and

a first trench contact disposed over the source region and a second trench contact disposed over the drain region, each of the first and second trench contacts having a first end opposite a second end in the second direction, wherein the first of the

pair of gate edge isolation structures is disposed directly adjacent to the first end of the first trench contact and to the first end of the second trench contact, and the second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.

3. (Original) The semiconductor structure of claim 1, further comprising:

a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin;

a second gate structure disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction, wherein the second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure; and

a third gate edge isolation structure disposed directly adjacent to the second end of the second gate structure, wherein the third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.

4. (Original) The semiconductor structure of claim 3, further comprising:

a local interconnect disposed above and electrically coupling the first and second gate structures.

5. (Original) The semiconductor structure of claim 4, wherein the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

6. (Original) The semiconductor structure of claim 3, wherein the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.

7. (Original) The semiconductor structure of claim 1, wherein the gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

8. (Original) The semiconductor structure of claim 1, wherein the pair of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

9. (Original) A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length;

alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and

a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and

a gate local interconnect disposed above one of the gate structures and between a pair of the plurality of gate edge isolation structures.

10. (Original) The semiconductor structure of claim 9, further comprising:

a dielectric cap disposed on the gate local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

11. (Original) The semiconductor structure of claim 9, further comprising:

a trench contact local interconnect disposed above one of the trench contacts and between a second pair of the plurality of gate edge isolation structures.

12. (Original) The semiconductor structure of claim 11, further comprising:

a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the second pair of the plurality of gate edge isolation structures.

13. (Original) The semiconductor structure of claim 9, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

14. (Original) The semiconductor structure of claim 9, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

15. (Original) A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length;

alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and

a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and

a trench contact local interconnect disposed above one of the trench contacts and between a pair of the plurality of gate edge isolation structures.

16. (Original) The semiconductor structure of claim 15, further comprising:

a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

17. (Original) The semiconductor structure of claim 15, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

18. (Original) The semiconductor structure of claim 15, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

19. (Original) A method of fabricating a semiconductor structure, the method comprising:

forming first and second parallel semiconductor fins above a substrate;

forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins, wherein the dummy spacers of the first semiconductor fin are non-continuous with the dummy spacers of the second semiconductor fin;

forming an isolation structure between the dummy spacers of the first and second semiconductor fins;

removing the dummy spacers; and

forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure.

20. (Original) The method of claim 19, further comprising:

forming a first pair of trench contacts over the first semiconductor fin and a second pair of trench contacts over the second semiconductor fin, wherein the first and

pairs of trench contacts are directly adjacent to, and separated from one another by, the isolation structure.

21. (Original) The method of claim 19, further comprising:

subsequent to forming an isolation structure and prior to removing the dummy spacers, recessing the first and second semiconductor fins.

22. (Original) The method of claim 19, wherein forming the dummy spacers comprises forming and etching a polycrystalline silicon layer.

23. (Original) The method of claim 19, wherein forming the isolation structure comprises depositing and planarizing a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

24. (Original) The method of claim 19, wherein forming one or both of the first and second replacement gate structures comprises forming a high-k gate dielectric layer and a metal gate electrode.

25. (Original) The method of claim 19, further comprising:

forming a local interconnect above and electrically coupling the first and second replacement gate structures.

26. (New) An integrated circuit structure, comprising:

a first fin comprising silicon, the first fin having a longest dimension along a first direction;

a second fin comprising silicon, the second fin having a longest dimension along the first direction;

an isolation material between the first fin and the second fin;

a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;

a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;

a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and

a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.

27. (New) The integrated circuit structure of claim 26, wherein the gate edge isolation structure comprises silicon and nitrogen.

28. (New) The integrated circuit structure of claim 26, wherein the dielectric material is in contact with the gate edge isolation structure.

29. (New) The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

30. (New) The integrated circuit structure of claim 29, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.

31. (New) The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

32. (New) The integrated circuit structure of claim 26, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.

33. (New) The integrated circuit structure of claim 32, further comprising:

a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.

34. (New) The integrated circuit structure of claim 33, wherein the local interconnect electrically couples the first gate structure to the second gate structure.

35. (New) The integrated circuit structure of claim 33, further comprising:

a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

REMARKS

Please replace the previous listing of claims with the present listing of claims.

CONCLUSION

The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN, L.L.P.

January 20, 2017
Date

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Electronic Patent Application Fee Transmittal

Application Number:	15024750
Filing Date:	24-Mar-2016
Title of Invention:	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same
First Named Inventor/Applicant Name:	Milton C. WEBB
Filer:	Justin K. Brask/Gigi Hoover
Attorney Docket Number:	P60397US

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1615	10	80	800
INDEPENDENT CLAIMS IN EXCESS OF 3	1614	1	420	420
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1220**

Electronic Acknowledgement Receipt	
EFS ID:	28121172
Application Number:	15024750
International Application Number:	
Confirmation Number:	9490
Title of Invention:	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same
First Named Inventor/Applicant Name:	Milton C. WEBB
Customer Number:	45209
Filer:	Justin K. Brask/Gigi Hoover
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US
Receipt Date:	20-JAN-2017
Filing Date:	24-MAR-2016
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Payment information:

Submitted with Payment	yes
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Payment was successfully received in RAM	$1220
RAM confirmation Number	012317INTEFSW00011031504238
Deposit Account	504238
Authorized User	Gigi Hoover
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.17 (Patent application and reexamination processing fees) 37 CFR 1.19 (Document supply fees)	

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

37 CFR 1.492 (National application filing, search, and examination fees)

37 CFR 1.492(a) (Basic national fee only)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		42P60397US_Preliminary_Amendment_012017.pdf	99927 9a88ff2eb20411961413f74cc6e6f5cdf824aaf6	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	10
	Applicant Arguments/Remarks Made in an Amendment	11	12

Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32430 506f6b33e9f8dad7251afec78e1f0df997ba11ea	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	132357		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/024,750
	Filing Date	3/24/2016
	First Named Inventor	Webb, Milton C.
	Group Art Unit	2822
	Examiner Name	Feeney, Brett A.
Sheet 1 of 1	Attorney Docket No: P60397US	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-20070080380	04/12/2007	CHANG, PETER	
		US-20110291188	12/01/2011	CHENG, KANGGUO, et al.	
		US-20130134506	05/30/2013	YAGISHITA, ATSUSHI	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**
		TW-201017772	05/01/2010	WEI, ANDY, et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		International Preliminary Report on Patentability for PCT Application No. PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) mailed June 30, 2016, 7 pages.	
		Non-Final Office Action and Search Report for Taiwan Patent Application No. 103137443 (Attorney Docket No. P60397TW) mailed June 3, 2016, 3 pgs.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Espacenet

Bibliographic data: TW201017772 (A) — 2010-05-01

Double gate and tri-gate transistor formed on a bulk substrate and method for forming the transistor

Inventor(s): WEI ANDY [US]; MULFINGER ROBERT [DE]; SCHEIPER THILO [DE]; KAMMLER THORSTEN [DE] + (WEI, ANDY, ; MULFINGER, ROBERT, ; SCHEIPER, THILO, ; KAMMLER, THORSTEN)

Applicant(s): ADVANCED MICRO DEVICES INC [US] + (ADVANCED MICRO DEVICES, INC)

Classification: - international: ***H01L21/336; H01L21/76***
- cooperative: **H01L29/66628**; **H01L29/66636**; **H01L29/66795**; **H01L29/7833**; **H01L29/7848**; **H01L29/7851**; H01L29/165; H01L29/66545

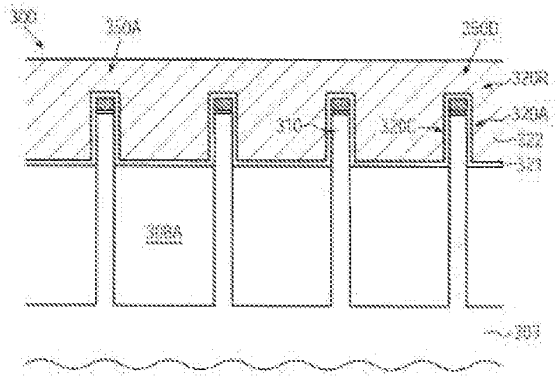
Application number: TW20090121967 20090630

Priority number (s): DE20081030864 20080630 ; US20090473610 20090528

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Abstract of TW201017772 (A)

Three-dimensional transistor structures such as FinFETS and tri-gate transistors may be formed on the basis of an enhanced masking regime, thereby enabling the formation of drain and source areas, the fins and isolation structures in a self-aligned manner within a bulk semiconductor material. After defining the basic fin structures, highly efficient manufacturing techniques of planar transistor configurations may be used, thereby even further enhancing overall performance of the three-dimensional transistor configurations.



(19)中華民國智慧財產局
(12)發明說明書公開本 (11)公開編號：TW 201017772 A1
(43)公開日： 中華民國 99 (2010) 年 05 月 01 日

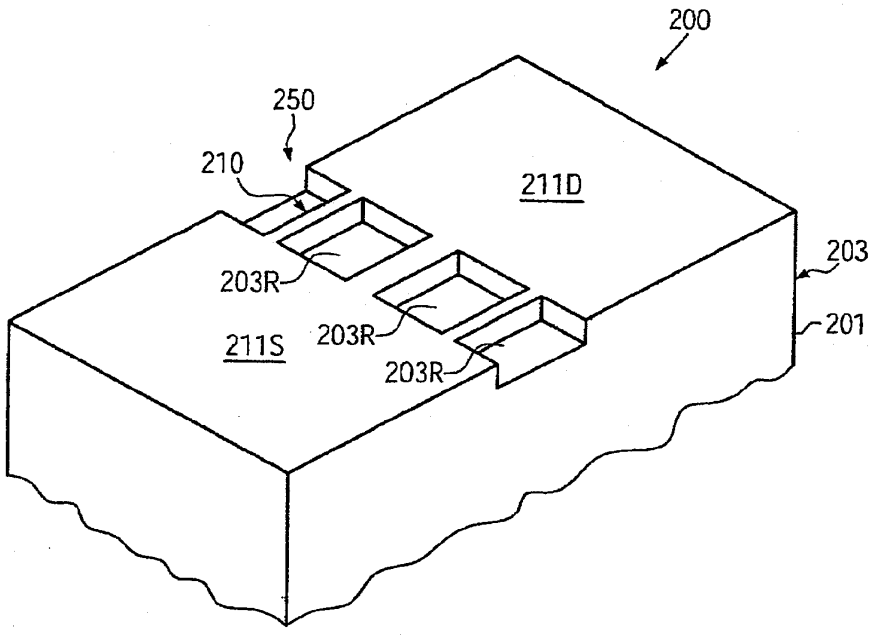
(21)申請案號：098121967 (22)申請日： 中華民國 98 (2009) 年 06 月 30 日
(51)Int. Cl.： *H01L21/336 (2006.01)* *H01L21/76 (2006.01)*
(30)優先權：2008/06/30 德國 102008030864.1
2009/05/28 美國 12/473,610
(71)申請人：高級微裝置公司 (美國) ADVANCED MICRO DEVICES, INC. (US)
美國
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申請實體審查：無 申請專利範圍項數：25 項 圖式數：3 共 57 頁

(54)名稱

形成在塊狀基板上之雙閘極與三閘極電晶體及形成該電晶體之方法
DOUBLE GATE AND TRI-GATE TRANSISTOR FORMED ON A BULK SUBSTRATE AND METHOD FOR FORMING THE TRANSISTOR

(57)摘要

如鰭形電晶體(FinFET)和三閘極電晶體之三維電晶體結構可基於增強之遮罩方式而形成，藉此在塊狀半導體材料中以自我校準的方式形成汲極和源極區域、該等鰭和隔離結構。在定義基本的鰭結構之後，可使用高效率之平面電晶體組構製造技術，藉此進一步增強該三維電晶體組構之總體效能。



200：半導體裝置
201：基板
203：半導體層
203R：凹陷
210：鰭
211D：汲極區
211S：源極區
250：雙閘極或三閘極電晶體

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(43)公開日： 中華民國 99 (2010) 年 05 月 01 日

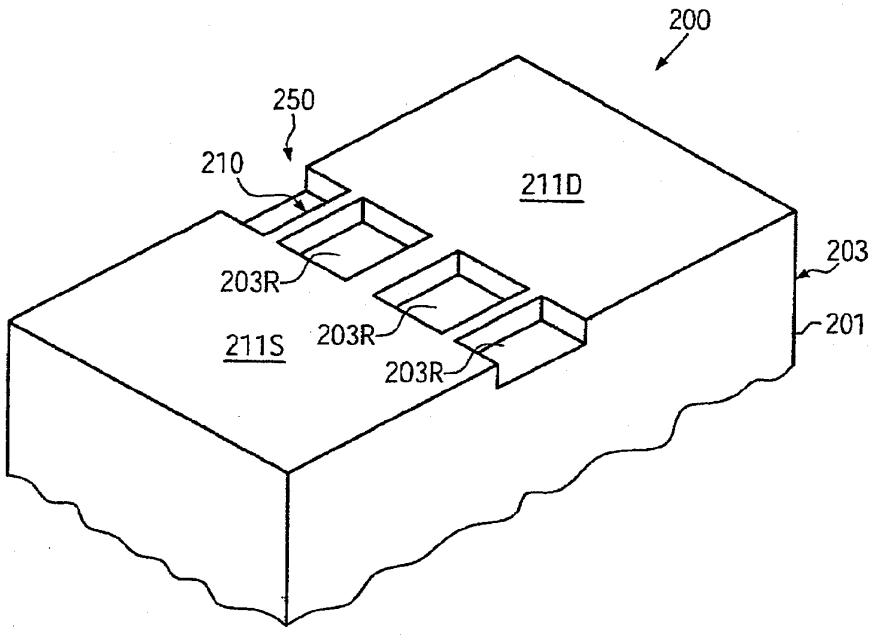
(21)申請案號：098121967 (22)申請日： 中華民國 98 (2009) 年 06 月 30 日
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(30)優先權：2008/06/30 德國 102008030864.1
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美國
(72)發明人：韋 安迪 WEI, ANDY (US)；邦夫葛爾 羅伯特 MULFINGER, ROBERT (DE)；
史奇佩爾 史羅 SCHEIPER, THILO (DE)；坎姆勒 索斯頓 KAMMLER, THORSTEN (DE)
(74)代理人：洪武雄；陳昭誠
申請實體審查：無 申請專利範圍項數：25 項 圖式數：3 共 57 頁

(54)名稱

形成在塊狀基板上之雙閘極與三閘極電晶體及形成該電晶體之方法
DOUBLE GATE AND TRI-GATE TRANSISTOR FORMED ON A BULK SUBSTRATE AND METHOD FOR FORMING THE TRANSISTOR

(57)摘要

如鰭形電晶體(FinFET)和三閘極電晶體之三維電晶體結構可基於增強之遮罩方式而形成，藉此在塊狀半導體材料中以自我校準的方式形成汲極和源極區域、該等鰭和隔離結構。在定義基本的鰭結構之後，可使用高效率之平面電晶體組構製造技術，藉此進一步增強該三維電晶體組構之總體效能。



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210：鰭
211D：汲極區
211S：源極區
250：雙閘極或三閘極電晶體

六、發明說明：

【發明所屬之技術領域】

一般而言，本發明係關於製造包含具有雙閘極(鰭形場效電晶體(FinFET))或三閘極架構之高微縮電晶體元件之高度精密的積體電路。

【先前技術】

先進積體電路(如 CPU、儲存裝置、特殊應用積體電路(ASIC)等)之製造必須根據特定電路佈局(circuit layout)於給定晶片區域上形成大量的電路元件，其中場效電晶體代表了實質決定該積體電路效能之一種重要的電路元件類型。一般而言，目前實際使用有複數種製程技術，其中，對於許多複雜的電路系統類型(包含場效電晶體)而言，由於MOS技術在操作速度及/或功率消耗及/或成本效益上之優越特性，使得 MOS 技術係目前最具前景之其中一種製程技術。在利用例如 MOS 技術製造複雜之積體電路的期間，於包含結晶半導體層之基板上形成數百萬個電晶體，例如N通道電晶體及/或P通道電晶體。場效電晶體(不論是N通道電晶體或P通道電晶體)典型上包括所謂的PN接面(PN junction)，其係由高度摻雜區(稱作為汲極和源極區)與輕微摻雜或無摻雜區(例如通道區)之介面所形成，其中，該輕微摻雜或無摻雜區係配置成鄰接該等高度摻雜區。在場效電晶體中，該通道區之導電性(亦即導電通道的電流驅動能力)係由鄰接該通道區而形成之閘極電極所控制，且該閘極電極係藉由薄絕緣層(insulating layer)與該通

道區分隔開。在因為施加適當控制電壓至該閘極電極而形成導電通道時，該通道區之導電性取決於摻雜物濃度、電荷載子移動率以及(對於平面電晶體架構而言)該汲極和源極區之間的距離(又稱作為通道長度)。

目前，由於矽幾乎能夠無限量的取得、矽和相關材料和製程之習知特性、以及在過去 50 年期間所累積之經驗，所以絕大多數的積體電路係以矽為基礎。因此，矽很可能仍將是未來電路世代用以量產之材料選擇。矽在半導體裝置之製造上具有主導性地位的一個原因係矽/二氧化矽介面之優越特性，使得半導體不同區彼此之間能夠具有可靠的電性絕緣(electrical insulation)。該矽/二氧化矽介面在高溫下相當穩定，而因此(如果需要的話)能夠接著實施高溫製程，例如，實施退火循環(anneal cycle)以活化摻雜物並且修復晶體損傷而不會犧牲該介面之電性特性。

對於上文中所指出之原因，二氧化矽較佳係用在場效電晶體中作為閘極絕緣層來將該閘極電極(通常由多晶矽或其他含金屬材料所組成)與該矽通道區分隔開。在不斷地改善場效電晶體裝置效能的過程中，該通道區長度持續地縮減以改善切換速度和電流驅動能力。由於該電晶體效能係由施加至該閘極電極之電壓所控制，其中，該電壓係用以將該通道區表面反轉(invert)成為夠高的電荷密度(charge density)以針對給定供應電壓提供所期望之驅動電流，所以必須要維持某種程度之電容耦合(該電容耦合係由以該閘極電極、該通道區及配置於兩者間之二氧化矽所

形成之電容所提供者)。而情況是，對於平面電晶體組構縮減其通道長度需要增加電容耦合，以避免於電晶體操作期間發生所謂的短通道行為(short channel behavior)。該短通道行為可能導致漏電流增加並導致臨限電壓(threshold voltage)對於該通道長度的依賴。大幅微縮尺寸且具有相對較低之供應電壓及因此降低之臨限電壓的電晶體裝置可能會面對漏電流呈指數增加的問題，而必須增強該閘極電極至該通道區之電容耦合。因此，該二氧化矽層之厚度必須相對應地縮減，以提供該閘極和該通道區之間所需之電容。舉例而言，大約 0.08μm 之通道長度可能需要厚度大約 1.2nm 之二氧化矽製成的閘極介電質。雖然，一般而言，具有極短通道之高速電晶體元件可能較佳用於高速應用，反之具較長通道之電晶體元件可用於較不具關鍵性之應用(如儲存電晶體元件)，惟電荷載子直接穿隧(tunneling)通過極薄二氧化矽閘極絕緣層所造成之相對高之漏電流對於厚度範圍 1 至 2nm 之氧化物而言可能達到無法符合效能驅動電路(performance driven circuit)之需求之數值。

因此，已經考慮取代二氧化矽作為閘極絕緣層之材料，特別是對於極薄二氧化矽閘極層而言。可能的替代材料包含顯現出明顯較高介電常數之材料，使得實際上相對應地形成之具有較大厚度之閘極絕緣層能夠提供極薄二氧化矽層所得到之電容耦合。一般而言，以二氧化矽達到特定電容耦合所需之厚度稱作為電容等效厚度(capacitance equivalent thickness；CET)。

因此已經有建議以具有高介電常數之材料來代替二氧化矽，如 k 值大約 25 之氧化鉭(tantalum oxide)(Ta_2O_5)、k 值大約 150 之氧化鍶鈦(strontium titanium oxide)($SrTiO_3$)、氧化鉿(hafnium oxide)(HfO_2)、$HfSiO_2$、氧化鋯(zirconium oxide)(ZrO_2)等。

雖然基於上述特定策略之精密平面電晶體架構可於效能和可控制性上得到明顯優勢，但是有鑑於進一步的裝置微縮，已提出新的電晶體組構，其中可設置"三維(three-dimensional)"架構以試圖在得到所期望之通道寬度的同時，維持對於流過該通道區之電流之良好可控制性。為此目的，已提出所謂的 FinFET，其中矽之薄片(sliver)或鰭(fin)可形成於絕緣體上矽(silicon-on-insulator；SOI)基板之薄主動層(thin active layer)中，其中，閘極介電材料和閘極電極材料可設置於兩側壁上，藉此實現雙閘極電晶體，其通道區可被完全空乏化(fully depleted)。典型上，在精密應用中，該矽鰭之寬度係 10nm 的等級而該矽鰭之高度係 30nm 等級。在基本雙閘極電晶體架構的修改版本中，也可於該鰭之頂部表面上形成閘極介電材料和閘極電極，藉此實現三閘極電晶體架構。參考第 1a 至 1b 圖，可進一步詳述傳統 FinFET 的基本組構及有關於傳統製造技術之特性。

第 1a 圖示意地描繪包括傳統之雙閘極或鰭形場效電晶體(FinFET)150 之半導體裝置 100 之透視圖。如圖中所描繪，該裝置 100 可包括具有形成於其上之埋置絕緣層

(buried insulating layer)102(例如：以二氧化矽材料之形式)之基板 101(如矽基板)。此外，在第 1a 圖中，所描繪的鰭 110 代表形成於該埋置絕緣層 102 上之矽層(未顯示)之殘留部位，藉此定義 SOI 組構。該鰭 110 可包括汲極和源極區 111 之一部分以及通道區(未顯示)，該通道區可被閘極電極結構 120A、120B 覆蓋，該等閘極電極結構 120A、120B 可分別形成於該鰭 110 之側壁 110A、110B 上並且可包括適當之閘極介電材料(如二氧化矽)以及電極材料(如多晶矽)。該鰭 110 之頂部表面可被罩蓋層(cap layer)112 覆蓋，該罩蓋層 112 可能由氮化矽和類似材料所組成。如圖中所描繪，可藉由形成於該罩蓋層 112 上之電極材料連接閘極電極結構 120A、120B 兩者。該鰭 110 可具有對應於該總體裝置需求之高度 111H、寬度 111W 及長度 111L，其中該鰭 110 內之有效通道長度大致上可由該閘極電極結構 120A、120B 沿著該鰭 110 之長度方向之延伸所決定。

典型上，包括該 FinFET 150 之半導體裝置 100 係藉由對形成於該埋置絕緣層 102 上之主動矽層進行圖案化所形成，且之後實施經過適當設計之製造程序以形成該閘極電極結構 120A、120B 及定義汲極和源極區 111 和通道區之適當的摻雜物分佈，接著形成適當的接觸層(contact layer)。

於操作期間，可藉由施加適當之供應電壓並且也施加適當之控制電壓至該等閘極電極 120A、120B 來建立由汲極至源極之電流。因此，可自該鰭 110 之兩側控制該通道

區(亦即，該鰭 110 被該等閘極電極結構 120A、120B 所包圍之部位)，藉此得到預期可提供增強的通道控制之完全空乏組構。

第 1b 圖示意地描繪該裝置 100 之頂部視圖，其中該裝置 100 設置有三個 FET 電晶體 150。如圖中所描繪，可藉由磊晶再生長之矽材料(epitaxially re-grown silicon material)來連接該等電晶體 150 之汲極區和源極區，藉此分別於該汲極側和該源極側形成矽層 130。典型上，於該汲極側和該源極側之矽材料可藉由選擇性磊晶生長技術來形成，因此也需要間隔件元件 104 以提供對於各種雙閘極結構 120A、120B 之閘極電極材料所需之偏移(offset)。雖然該等半導體層 103 可設置於該汲極側和該源極側，作為個別電晶體單元 150 之汲極和源極區，不過由於存在有該間隔件元件 104，因此可能必須設置該汲極和源極區之一部份(如該等區 111)(如第 1a 圖所示者)，因此，由於該等鰭中有限之矽容積(silicon volume)和由於摻雜物向外擴散(out-diffusion)進入該埋置氧化物而產生普通高的串聯電阻(series resistance)。因此，雖然這些電晶體由於該通道之完全空乏化及由於來自兩個或三個閘極的控制而提供優越的短通道行為，但是當省略罩蓋層 112 並且以閘極介電材料代替該罩蓋層 112(如第 1a 圖所示)時，驅動電流會受到每一個個別電晶體 150 之鰭 110 中之汲極和源極區之高串聯電阻所限制，使得此技術目前無法與可設置於塊體組構(bulk configuration)或局部空乏 SOI 組構中的標準平面電

晶體架構競爭。

本發明係有關於可避免或至少減少上述問題所產生之一個或多個影響之各種方法和裝置。

【發明內容】

為了提供對於本發明某些態樣的基本了解，下文中描述本發明之簡化概要。此發明內容並非本發明之徹底概觀。而此發明內容並非意圖識別本發明之重要或關鍵元件，或者描述本發明之範疇。此發明內容之唯一目的係以簡化的形式來提出某些概念，作為稍後所討論之更詳細之說明書內容之前言。

一般而言，本發明係關於半導體裝置和用以形成該半導體裝置之技術，其中在矽材料中形成電晶體單元之對應鰭之後可利用廣為接受之常見"二維"製程技術於矽塊狀基板上形成雙閘極或三閘極電晶體。因此，可於該等鰭中設置增加的矽量，同時在形成該等鰭之後可採用廣為接受之二維製程技術，藉此提供有效率降低總體串聯電阻之方法，同時提供高效率之總體製造流程，其出發點係成本明顯較低之基板材料。

本文中所揭示之一個例示方法包括於半導體裝置之半導體層上方形成層堆疊，其中該層堆疊包括形成於該半導體層上方之蝕刻停止層以及形成於該蝕刻停止層上方之第一遮罩層。該方法復包括圖案化該第一遮罩層以得到遮罩特徵，以及於該遮罩特徵之側壁上形成間隔件元件。此外，相對於該側壁間隔件元件選擇性地移除該遮罩特徵，

並且設置具有暴露該側壁間隔件元件之一部份之第一開口之第二遮罩層，以便定義通道區域和汲極和源極區域。該方法復包括利用該側壁間隔件元件和該第二遮罩層作為蝕刻遮罩從而於該半導體層中形成溝槽，以於該半導體層中形成鰭，其中該鰭對應於該通道區域。再者，至少於該鰭之側壁上形成閘極電極結構，並且於該汲極和源極區域中形成汲極和源極區，其中該汲極和源極區連接至該鰭。

本文中進一步揭示之例示方法係關於形成電晶體。該方法包括於半導體層上方形成遮罩特徵，其中該遮罩特徵定義欲形成於該半導體層中之鰭之側向尺寸。該方法另外包括形成具有第一開口和第二開口之遮罩層，其中該第一開口定義該鰭之長度，而該第二開口定義隔離結構之側向尺寸和位置。再者，利用該遮罩層作為蝕刻遮罩而以共同的蝕刻製程於該半導體層中形成該鰭和隔離溝槽。該方法復包括於該鰭之第一側壁之一部份上形成第一閘極電極結構，以及於該鰭之第二側壁之一部份上形成第二閘極電極結構。最終，該方法包括於鄰接該鰭之末端部位之該半導體層中形成汲極和源極區。

本文中所揭示之一個例示半導體裝置包括半導體層以及形成於該半導體層中之第一凹陷和第二凹陷，其中該第一凹陷和第二凹陷具有共同的邊界，以便定義高度小於該半導體層厚度之鰭。該半導體裝置復包括形成於該鰭之第一側壁上之第一閘極電極結構以及形成於該鰭之第二側壁上之第二閘極電極結構。最終，該半導體裝置包括連接

至該鰭之汲極和源極區。

【實施方式】

本發明之各種例示實施例係描述於下文中。為了清楚起見，並未在本說明書中描述實際實作之所有特徵。當然將體會到在任何此類實際實施例之發展中，必須做出許多實作特定之決定以達到研發人員所期望之特定目標(如符合與系統相關及與商業相關的約束)，而這些目標將隨著不同實作而變化。此外，將體會到此類研發所做之努力可能相當複雜且耗時，但是這對於獲益於本揭示內容之熟習本領域者而言仍將只是例行工作。

本發明現在將參考附加圖式進行描述。各種結構、系統及裝置僅為了說明且避免以熟習本領域者所熟知之細節模糊本發明而示意地描述於該等圖式中。但是，所包含之該等附加圖式係用以描述並說明本發明所描繪之範例。本文中所使用之字詞和措辭應該了解並解釋成為與熟習本領域者所了解之字詞和措辭具有相同之意義。未有特別定義之字詞和措辭(亦即，具有不同於熟習本領域者所習知且慣用之意義者)被意指與本文中所使用者之字詞和措辭一致。在一定程度上，字詞和措辭係意圖具有特別定義(亦即，不同於熟習本領域之技藝者所了解之意義者)，此特別定義將特別於本說明書中以定義模式提出，直接且明確地提供該字詞和措辭之特別定義。

一般而言，本發明係關於方法和半導體裝置，其中雙閘極電晶體(亦可稱作為 FinFET)或三閘極電晶體可形成於

塊狀基板(bulk substrate)上。也就是說，用以容置該等電晶體之通道區之鰭元件可形成於半導體層內，其中該等鰭之高度係小於對應之半導體層之厚度。因此，意思是說，可於實際鰭元件之下設置額外半導體容積(如矽容積)的任何電晶體組構均可認為是塊狀組構，不論任何另外的埋置絕緣層是否可設置於該塊狀半導體層之"深度(depth)"中。在完成該等鰭和該兩個或三個閘極電極結構以及該等低電阻汲極和源極區域之基本結構(在一些例示實施例中，可以自我校準(self-aligned)製造順序來完成)之後，可利用廣為接受的平面製程技術(planar process technique)，例如藉由施加應變引發(strain-inducing)機制等，來調整該汲極和源極之摻雜物分佈、增強該通道區之總體串聯電阻。因此，可在維持三維電晶體組構優點之同時，明顯地降低傳統FinFET或三閘極電晶體之驅動電流限制，同時提供高效率之總體製造流程。

第2a圖示意地描繪半導體裝置200之透視圖，該半導體裝置200可包括基板201(如矽基板或用以於其上形成半導體層203之其他任何適當載體材料)，該基板201可代表可能包括額外組成物(如鍺、碳等)之矽層，同時在其他案例中可使用其他任何適當之半導體化合物。在一個例示實施例中，該半導體層203可代表一矽基材料(silicon-based material)，其可代表該基板201之實質結晶材料之一部份，其至少局部位於裝置區域中，且其中將形成複數個雙閘極或三閘極電晶體250。應了解到，視總體

需求而定，該半導體裝置200可於其他裝置區域中具有SOI組構。如圖中所描繪，該一個或多個電晶體250可具有形成於該半導體層203中之共同汲極區211D和共同源極區211S，其中該汲極和源極區211D、211S可藉由個別鰭210連接，該等個別鰭210之每一者均可代表該等電晶體250之其中一者之通道區。因此，該等鰭210也可藉由在鄰接鰭210之間設置個別凹陷203R而形成於該半導體層203中，藉此定義該等鰭210之三維尺寸(dimension)，如高度、寬度及長度。再者，該等凹陷203R也可至少於該等鰭210之側壁上定義欲形成之個別閘極電極結構之位置，在一些例示實施例中，也可定義於該等鰭210之頂部表面上。如同將於稍後詳述者，該汲極和源極區211D、211S、該等鰭210以及該等凹陷203R中和該等鰭210上方之個別電極結構可利用自我校準的方式而與個別隔離結構(未顯示)一起設置，該等個別隔離結構可包圍該一個或多個電晶體250且亦可針對欲形成於該等凹陷內之閘極電極材料提供該等凹陷之絕緣，如將於稍後所詳述者。

第2b圖示意地描繪於較早製造階段之半導體裝置200。如圖中所描繪，層堆疊204可形成於該半導體層203上，且可由形成於於該半導體層203上之蝕刻停止層204A及形成於該蝕刻停止層204A上之遮罩層204B所組成。舉例而言，該蝕刻停止層204A可以二氧化矽材料的形式設置，而該遮罩層204B可由矽所組成。再者，光阻劑特徵(resist feature)205可依據所考慮之技術標準以具有寬度和

間距之線狀結構(line-like feature)形式來設置。也就是說，該等光阻劑特徵 205 所定義之寬度和間距可代表對應技術標準之關鍵尺寸，其可基於對應之微影技術而一致且可重複產生地進行圖案化。

如第 2b 圖中所示之半導體裝置 200 可基於下列製程而形成。可以例如矽塊狀基板形式來設置包括該半導體層 203 之基板 201，同時如先前所說明，在其他案例中，對於該基板 201 和該層 203 可採用不同之組構。其後，可藉由例如基於廣為接受之技術生長具有適當厚度(如大約 2 至 5nm)之氧化物層來形成該蝕刻停止層 204A。其後，可利用廣為接受之電漿輔助或者熱活化沉積配方(thermally activated deposition recipe)以(例如)矽材料之形式來沉積厚度(例如)大約 60 至 80nm 之遮罩層 240B。藉由在該層堆疊 204 中使用二氧化矽材料和矽，當形成適當硬遮罩以提供遮罩特徵，而用於將被形成在半導體層 203 中之鰭時，可使用用於圖案化該堆疊 204 之廣為接受的配方(recipe)。應體會到，只要能夠於進一步製程期間得到所需要之蝕刻停止能力，則可將其他材料用於該層堆疊 204。當該蝕刻停止層 204A 係由二氧化矽所組成時，其可設置有適當之厚度，以便當例如該遮罩層 204B 罩蓋該層 204A 時，避免因接觸濕式化學蝕刻藥劑(如氫氟酸(HF))所造成之側向蝕刻(lateral etching)。以此方式，可抑制個別特徵於個別濕式化學蝕刻製程期間所不希望的任何蝕刻不足(under-etching)。另一方面，由於這些鰭可基於在稍後製造

階段中將以共形方式形成在遮罩特徵之側壁上(該遮罩特徵係將從遮罩層 204B 所形成)之側壁間隔件元件而形成，所以該遮罩層 204B 之厚度可設置成相等於或大於該等鰭 210 所期望之最終寬度。再者，在設置該層堆疊 204 之後，可基於廣為接受之微影技術設置該光阻劑特徵 205。

第 2c 圖示意地描繪具遮罩特徵 204M 之半導體裝置 200，該遮罩特徵 204M 於其側向尺寸大致上可對應於該等光阻劑特徵 205(第 2b 圖)，同時該等特徵 204M 之高度係由該遮罩層 204B(第 2b 圖)之初始厚度所定義。該等特徵 204M 可基於經適當設計之蝕刻製程而形成，其中，在一些例示實施例中，當該等層 204B、204A 分別係由矽和二氧化矽所組成時，可使用廣為接受且用於圖案化多晶矽閘極電極之蝕刻配方來作為基礎。其後，可基於任何適當之技術將該等光阻劑特徵 205 移除。

第 2d 圖示意地描繪具有形成於該遮罩特徵 204M 之暴露側壁部位上之側壁間隔件元件 206 之裝置 200。舉例而言，該等間隔件元件 206 可由氮化矽所組成，同時只要可確認所期望之蝕刻選擇性程度以及與後續製程之相容性，則可使用其他適當的材料(如碳化矽、含氮碳化矽等)。可藉由沉積氮化矽材料(例如：藉由熱活化化學氣相沉積(CVD)技術)來形成該等間隔件 206，同時控制該沉積厚度，其中，該沉積厚度大致上對應於基於該等間隔件 206 而將形成之鰭的期望之最終寬度。在沉積該間隔件材料之後，可實施非等向性蝕刻製程(anisotropic etch process)，

其對於該蝕刻停止層 204A 具有選擇性。在一些例示實施例中，可使用對該等遮罩特徵 204M 具有選擇性之蝕刻配方，且可利用習知之製程技術來完成，而在其他案例中，只要維持該層 204A 之高度蝕刻停止能力，則亦可使用對該間隔件材料和該遮罩特徵 204M 未具有選擇性之蝕刻配方。

第 2e 圖示意地描繪在選擇性移除該等遮罩特徵 204M 之後的裝置 200，其可藉由適當地選擇可針對該蝕刻停止層 204A 和該間隔件元件 206 提供夠高的選擇性之蝕刻化學藥劑來完成。舉例而言，可使用基於溴化氫(hydrogen bromide)之複數種電漿輔助蝕刻配方，而在其他案例中可採用濕式化學蝕刻技術，例如當使用二氧化矽、氮化矽及矽作為蝕刻停止材料層 204A、間隔件 206 及遮罩特徵 204M 之材料時，可使用基於氫氧化四甲基銨(Tetra Methyl Ammonium Hydroxide)(TMAH)之蝕刻配方。氫氧化四甲基銨對於氧化物(2000-3000：1)和氮化物(10000：1)具有高度選擇性，藉此有效率地移除暴露之遮罩特徵 204M，同時避免過度地消耗該等間隔件 206 之材料，其中該等間隔件 206 代表用以在該半導體層 203 中形成該等鰭之硬遮罩元件。例如基於 TMAH 之濕式化學蝕刻製程也可結合電漿輔助製程，用以移除可能形成於該等遮罩特徵 204M 之暴露表面部份上之天然氧化物。

第 2f 圖示意地描繪在進一步之製造階段中之半導體裝置 200，該進階之製造階段形成用以於通道區域之半導

體層 203 中形成鰭之另外的遮罩，同時定義個別汲極和源極區域(如第 2a 圖所示)。如圖中所描繪，遮罩層 207 可包括可對應於汲極和源極區域(如第 2a 圖中所描繪之汲極和源極區 211D、211S)之遮罩元件 207A、207B。再者，遮罩元件 207C 可代表通道區域和其中欲形成用於雙閘極或三閘極電晶體之閘極電極結構之區，同時，遮罩特徵 207D 可代表其中欲形成在半導體層 203 中之隔離溝槽之個別區域。一方面的遮罩特徵 207A、207B 和另一方面的遮罩特徵 207C、207D 可由不同材料所組成，以便能夠在稍後的製造階段中選擇性移除該等遮罩元件 207C、207D。舉例而言，該等特徵 207A、207B 可由氮化矽所組成，而該等特徵 207C、207D 可由矽材料所組成。

該遮罩層 207 可藉由沉積適當之材料層(如矽)而形成，其厚度可選擇為大於或等於必要的最終閘極高度，其中該必要之最終閘極高度係為了從該等鰭(其係將形成於該半導體層 203 內)頂部阻擋源極/汲極佈植種類所必需者。舉例而言，該遮罩層 207 之厚度可為大約 70 至 90nm。其後，可藉由微影製程圖案化該層 207，其中可同時定義該等遮罩特徵 207C、207D 之位置，也藉此以自我校準的方式提供該汲極和源極區域、該等閘極電極及隔離結構之側向尺寸和位置。在實施對應之微影製程後，可利用廣為接受之蝕刻配方非等向性蝕刻該遮罩層 207，如先前所說明，例如，相對於二氧化矽而言選擇性地蝕刻矽。其後，可沉積用以形成該等遮罩元件 207A、207B 之適當填充材

料(例如：以氮化矽的形式)，其中藉由實施平面化製程(如化學機械研磨(CMP))可平面化對應產生之表面形貌(topography)，其中，殘留的遮罩特徵 207C、207D 可使用為化學機械研磨停止層以提供該平面化製程之增強控制。接下來，可選擇性地移除對應於該等閘極電極和通道區域和該等隔離結構之遮罩元件 207C、207D，例如利用如先前所述之類似製程技術。舉例而言，為了選擇性地相對於氮化物和氧化物而有效率地移除矽，可使用 TMAH。

第 2g 圖示意地描繪在上述製程順序結束之後之半導體裝置 200。因此，個別開口 207N、207M 形成於該遮罩層 207 中，藉此定義通道區域(亦即於其中將形成該等鰭之區域)和隔離溝槽區域，而殘留的遮罩元件 207A、207B 可代表將形成之汲極和源極區域。可基於該等開口 207N、207M 實施非等向性蝕刻製程，以便首先蝕刻通過該蝕刻停止層 204A 並且蝕刻進入該半導體層 203 達期望之深度，如形成隔離溝槽所需之深度。舉例而言，可使用大約 250 至 350nm 之蝕刻深度，其中可基於廣為接受之電漿輔助配方實施蝕刻製程。其後，可藉由適當介電材料(如二氧化矽)來填充形成於該半導體層 200 中之對應溝槽，其中亦可填充該等開口 207N、207M。另外，為了密實(densify)該介電填充材料，可實施退火製程(anneal process)，並且可藉由 CMP 移除任何過量之材料，藉此提供平面化表面形貌，其中該等遮罩元件 207A、207B 可作為 CMP 停止層。

第 2h 圖示意地描繪在上述製程順序結束之後之半導

體裝置 200。如圖中所描繪，於對應於該等開口 207M(如第 2g 圖中所示)之該半導體層 203 中可形成隔離結構 208，其中，在此製造階段中，該等隔離結構 208 之介電材料可向上延伸至該等遮罩元件 207A、207B 所定義之表面。同樣地，由於在基於該遮罩層 207 所實施之先前的溝槽蝕刻製程中，該等間隔件元件 206(如第 2e 圖所示)亦可作為該等開口 207N 中之硬遮罩，故隔離結構 208A 可形成為鄰接於將形成之該等鰭之個別下側部位 210L，藉此提供該等"深"鰭 210L。

第 2i 圖示意地描繪在進一步之製造階段中之半導體裝置 200。如圖中所描繪，可移除形成於該等隔離結構 208 上方及該等隔離結構 208A 和該等深鰭 210L 上方之介電材料(參照第 2h 圖)，同時亦藉由定義該等結構 208、208A 中介電材料之凹陷程度，而於該等隔離結構 208、208A 中產生為了實際形成鰭 210 之期望之凹陷 208R。利用經高度稀釋之氫氟酸溶液，可完成對應受控之材料移除，其中，對於給定之蝕刻速率，為了調整該等鰭 210 之高度 210H(其代表該等深鰭 210L 之上側部位)，可調整凹陷 208R 之深度。此外，在一些例示實施例中，為了暴露該等鰭 210 之上側表面，可基於(例如)選擇性非等向性蝕刻製程來移除該"罩蓋層"(亦即，如第 2e 圖所示之該等間隔件元件 206)。在此案例中，該等鰭 210 可代表三閘極電晶體元件之通道區。

第 2j 圖示意地描繪沿著該開口 207C(如第 2i 圖中所

示)之剖面圖。如圖中所描繪，該等隔離區 208A 係形成於該半導體層 203 內，以便延伸達到如該等隔離結構 208(如第 2i 圖中所示)所需之特定深度，其中該等深鰭 210A 將各個隔離區 208A 分隔開。再者，在一些例示實施例中，定義該等鰭 210 之有效高度之凹陷 208R 可選擇成為大約 20 至 30nm，視總體裝置需求而定。另一方面，該等間隔件元件 206(如第 2i 圖中所示)可決定該等鰭 210 之寬度 210W，其中該等間隔件元件 206 可於該等凹陷 208R 之形成期間作為蝕刻遮罩。另一方面，該等開口 207C 之寬度(如第 2i 圖中所示)可決定該等鰭 210 之長度(亦即，第 2j 圖中垂直於圖示平面之尺寸)。再者，在此製造階段中，所殘留之蝕刻停止層 204A 仍然可設置於該等鰭 210 之頂部表面上。因此，可以該等鰭 210 之形式設置該等電晶體元件之基本組構，其中應體會到的是，與第 2a 圖所描繪之基本組構不同的是，該等凹陷 208R 可設置於個別隔離區 208A 中，而非設置於該半導體材料層 203 中。

第 2k 圖示意地描繪在進一步之製造階段中之半導體裝置 200，其中可應用經適當設計之"平面"製程技術以完成該三閘極電晶體組構。在第 2k 圖中，為了定義 N 通道電晶體和 P 通道電晶體之基本電晶體特性，可實施佈植順序 209。對於 N 通道電晶體而言，可引進 P 型摻雜物種類以避免擊穿(punch through)，其可藉由在 0° 傾斜角度下實施該佈植 209 來完成，其中可依據廣為接受之微影技術以光阻劑遮罩作為其他類型電晶體之遮罩。在一些例示實施

例中，該佈植製程 209 可包含傾斜佈植步驟(tilted implantation step)209A，其中該離子束(ion beam)可對應於大致上平行於該等鰭 210 寬度方向之轉動軸而傾斜。因此，於該傾斜佈植步驟 209A 期間，可將代表 N 通道電晶體之逆摻雜物(counter dopant)之 P 型摻雜物混入該汲極和源極區域 211D、211S 的暴露側壁 211F。另一方面，可利用 5 至 10° 之傾斜角度和利用適當之佈植掃描方式(implantation scan regime)來抑制摻雜物種類明顯混入該等鰭 210。同樣地，可將 N 型摻雜物種類引入 P 通道電晶體，同時遮罩對應之 N 通道電晶體。於該汲極和源極區域 211D、211S 的暴露側壁部位 211F 混合該等逆摻雜物種類可因此針對可在稍後製造階段中形成於該等凹陷 208R 內之閘極介電材料和閘極電極材料提供增加之"隔離區域"，使得所增加之隔離區域可提供縮減之寄生閘極-源極/汲極電容(parasitic gate-source/drain capacitance)。因此，可使該佈植製程 209 和 209A 之劑量(dose)和能量適當地適應於將於稍後製造階段中實施之對應源極/汲極佈植製程。

第 21 圖示意地描繪該裝置 200 在該佈植製程 209 後之剖面圖。如圖中所描繪，可將該等井佈植種類(如 209W 所指示者)依據該裝置之需求而混入該深鰭 210L 中，並且向下達到所期望之深度。應體會到，也可將對應之井佈植 209W 引入該隔離區 208A。接下來，該裝置 200 可藉由實施廣為接受之清潔製程(cleaning processes)而準備形成閘極介電材料(如閘極氧化物)，並接著進行該介電材料之沉

積及/或氧化(如於該等鰭 210 之暴露表面部位上生長二氧化矽材料)。其後，可基於廣為接受之"平面"製程配方(以例如多晶矽之形式)來沉積閘極電極材料。

第 2m 圖示意地描繪在上述製程順序之後、在藉由移除任何過量閘極電極材料(例如基於 CMP)和利用遮罩元件 207A、207B 作為 CMP 停止材料來平面化所產生之表面形貌之後之半導體裝置 200。因此，可包括複數個個別閘極電極結構(未顯示)之閘極電極結構 220 可形成於遮罩元件 207A、207B 之間，同時該等個別犧牲"閘極電極結構"220S 可形成於該等隔離結構 208 上方。應體會到，在一些例示實施例中，該閘極電極結構 220 可代表結合閘極介電質(dielectrics)之實際閘極電極，並且可選擇關於該介電材料和類似材料厚度之適當參數。在其他案例中，如第 2m 圖所示之閘極電極結構 220 可用以作為定位件(place holder)，並且可在稍後之製造階段中以基於含金屬電極材料和高 k 介電材料的精密閘極電極結構來代替閘極電極結構 220。

第 2n 圖示意地描繪在進一步之階段中之半導體裝置 200，其中遮罩材料 230 可以例如氧化物層(其可基於氧化和類似製程產生)之形式形成於個別電極材料 220、220S 上。再者，為了保護暴露部位(其中將不形成閘極電極結構)，可於該裝置 200 上方形成蝕刻遮罩 231。也就是說，該蝕刻遮罩 231 可暴露對應於該等犧牲結構 220S 之部位，並且可覆蓋結構 220。其後，可利用例如用以移除暴

露之遮罩材料 230 之氫氟酸(hydrofluoric acid)來實施經適當設計之蝕刻順序，並且在這之後為了選擇性地移除該等結構 220S 之材料(例如：為多晶矽之形式)，可實施選擇性電漿輔助蝕刻製程，其選擇性係針對氮化物和氧化物。再者，在此案例中，可使用類似平面電晶體組構所使用之技術之蝕刻策略。在其他案例中，如先前所說明者，可使用濕式化學蝕刻藥劑。

第 2o 圖示意地描繪在上述製程順序和移除該蝕刻遮罩 231 之後的半導體裝置 200。因此，在暴露隔離結構 208 的同時，該等遮罩元件 207A、207B 仍然可覆蓋該汲極和源極區域 211D、211S。其後，可針對該遮罩材料 230 和該等隔離結構 208 選擇性地移除該等遮罩元件 207A、207B。當該等遮罩元件 207A、207B 係由氮化矽所組成時，可利用熱磷酸(phosphoric acid)來完成。

第 2p 圖示意地描繪在移除該等遮罩元件 207A、207B 之後沿著該等鰭 210 之寬度方向之剖面圖。因此，如圖中所描繪，該閘極電極結構 220 係形成於該等凹陷 208R 中和上方以及該等鰭 210 周圍和上方，同時各個閘極介電質 221A、221B、221C 係設置於該等鰭 210 之表面上。也就是說，在所示之實施例中，可設置有三閘極組構，其中該等鰭 210 之兩個側壁上可形成有該等閘極介電質 221A、221C，同時該等鰭 210 之頂部表面上亦可形成有該閘極介電材料 221B。再者，該遮罩材料 230 仍然可形成於該閘極電極結構 220 上，亦即，其閘極電極材料 222(如多晶矽材

料)上。

第 2q 圖示意地描繪如第 2p 圖中所示該裝置 200 之頂部視圖。因此，該隔離結構 208 側向地包圍著包括該汲極和源極區域 211D、211S 和形成為該鰭 210 之形式之各個通道區的三閘極電晶體 250。如圖中所描繪，先前所實施之遮罩方式(masking regime)可定義該等通道(亦即，鰭 210)之長度，並因此定義該閘極電極結構 220 之長度，藉此亦提供該汲極和源極 211D、211S 和該隔離結構 208 之自我校準圖案化(patterning)和定位(positioning)。

第 2r 圖於左手側示意地描繪沿著第 2q 圖 II 左線之剖面圖，同時於右手側示意地描繪沿著第 2q 圖 II 右線之剖面圖。因此，如同第 2r 圖左手側所描繪者，閘極電極材料 222 結合形成於鰭 210 頂部上之閘極介電材料 221B 和結合該汲極和源極 211D、211S 可具有非常類似於平面電晶體架構之組構。於第 2r 圖之右手側，"缺口"區域(亦即，如第 2q 圖中所示相鄰的鰭 210 之間的區域)之個別剖面圖描繪了下述基本概念，亦即，該等鰭 210 之高度(如第 2r 圖左手側所示)係由該等隔離區之凹陷程度所定義。因此，如第 2r 圖左手側所示之電晶體 250 之組構可採用廣為接受之平面製程技術，藉此除了於該鰭 210 中提供高矽容積之外還提供用以適當地調整該電晶體 250 之總體電性特性之增強效率。為此目的，可實作廣為接受之佈植技術、應變引發機制等。

藉由參考第 2s 至 2v 圖，可依據例示實施例描述個別

製程技術以求得到所期望之P通道電晶體和N通道電晶體效能。

第2s圖於左手側示意地描繪沿著第2q圖所描繪之截面之剖面圖，亦即描繪了該等鰭 210 之長度方向上之截面，同時第 2s 圖於右手側描繪了缺口區域內之個別剖面圖。如圖所示，電晶體組構 250N 可代表 N 通道電晶體，並且可包括鄰近鰭 210 而在該汲極和源極區域 211D、211S(如第 2r 圖所示)中之精密摻雜物分布，以定義汲極和源極區 211。舉例而言，為了形成與通道區 213(可由該鰭 210 代表)之適當 PN 接面，可設置類似平面電晶體組構中之延伸區 211E。再者，為了適當地定義該汲極和源極區 211 中之摻雜物濃度，可於具有適當寬度之閘極電極材料 222 之側壁上形成間隔件結構 223。

於第 2s 圖之右手側，描繪了該缺口區域中之對應組構。在此案例中，如先前所說明，該閘極電極材料 222 延伸進入形成於該隔離區 208A 中之凹陷，同時，在一些例示實施例中，由於該佈植製程 209 期間(如第 2k 圖中所示)之逆摻雜，故可增加該汲極和源極區 211 相對於閘極電極材料 222 之偏移(offset)，其中該半導體層 203 之暴露側壁部位可容置與該井摻雜種類對應之摻雜種類，藉此提供相對於該汲極和源極區 211 之"獨立(withdrawn)"PN 接面，使得該汲極和源極區 211 和該閘極電極材料 222 之間的寄生電容因偏移增加而降低。

如第 2s 圖所描繪之電晶體組構 250N 可藉由實施適當

之佈值製程來完成，同時為了依據廣為接受之配方適當地增加該鰭 210 和該汲極和源極區 211 之間之區域之井摻雜物濃度，可利用例如環形佈植製程(halo implantation process)來遮罩 P 通道電晶體。其後，可利用例如該結構 223 經適當設計之偏移間隔件來形成該延伸區 211E，且其後為了建立所期望之濃度分佈，於接下來的深汲極和源極區域佈值期間，可形成具有適當寬度之間隔件結構 223 以便作為佈值遮罩。應體會到，間隔件 223 可包括複數個個別間隔件元件，該等間隔件元件可在對應之佈植製程之後形成。

第 2t 圖根據一些例示實施例示意地描繪與 P 通道電晶體對應之電晶體組構 250P。如圖中所描繪，電晶體 250P 可包括可埋置入鄰近該鰭 210 之材料 203 之應變引發材料 214(例如：矽/鍺合金和類似形式)，以便沿著該鰭 210 中之電流方向建立壓縮應變元件(compressive strain element)，藉此增強其中之電洞移動率。可藉由基於(例如)該間隔件結構 223 或其他任何適當之遮罩材料在該半導體層 203 中蝕刻洞孔來形成應變引發材料 214，接著實施用於生長所期望之半導體合金 214(亦可以高度摻雜材料之形式設置)之選擇性磊晶生長製程，藉此可避免用於形成該深汲極和源極區之佈植製程。如圖中所描繪，如果適當的考量，該應變引發材料 214 可設置有某種程度之過量高度。再者，可形成個別延伸區 211E，以便連接至該通道區(亦即該鰭 210)。

於第 2t 圖之右手側，描繪了與該缺口區對應之組構。如圖中所描繪，亦在此案例中，由於該逆摻雜區 203C，所以該閘極電極材料 222 和該汲極和源極區 211 之間的偏移亦可增加，其中該逆摻雜區 203C 可形成於該佈植製程 209(包含如第 2k 圖所示之傾斜佈植 209A)期間。

應體會到，個別應變引發機制亦可以例如適當半導體合金(如矽/碳)之形式或者於該汲極和源極區 211 形成期間應用個別應力記憶技術(stress memorization technique)而設置於 N 通道電晶體 250N 中。也就是說，為了於應變狀態(strained state)中產生該汲極和源極區之重新生長部位(re-grown portion)，可在大致上非結晶狀態(amorphized state)下基於堅硬材料層(如氮化矽層)而重新生長該汲極和源極區 211 之至少一部份。在其他例示實施例中，在形成該汲極和源極區 211 之後，為了提供相對於後續矽化製程(silicidation process)之優勢(可能結合如拉張應力接觸材料(tensile stressed contact material)等之應力引發材料)，可凹陷這些區。

在混合用於形成該等電晶體 250N、250P 之汲極和源極區 211 之摻雜物種類之後，可實施最終退火製程以活化該等摻雜物並且將佈值所造成之損害重新結晶(re-crystallize)，也可藉此調整所期望之最終摻雜物分佈。

第 2u 圖示意地描繪在進一步之製造階段中之電晶體組構 250N。如圖所示，可設置接觸結構 240 且其可包括層間介電材料(interlayer dielectric material)241(如二氧化矽

等)，其中可埋置一個或多個接觸件 242。該等接觸元件 242 可由任何適當之金屬(如鎢(tungsten)、銅、鋁等)組成，可能結合適當之導電性阻障材料(conductive barrier material)，視總體製程和裝置需求而定。在一些例示實施例中，該等接觸元件 242 可包括具有高度內部拉張應力等級(high internal tensile stress level)之含金屬材料，其可(例如)基於廣為接受且用於形成鎢材料之沉積配方來完成，藉此在該通道或鰭 210 中提供所期望之拉張應力等級。

第 2u 圖之右手側示意地描繪該缺口區域中該接觸層級(contact level)240 之組構。如圖中所描繪，在此區域中，也可設置一個或多個接觸元件 242 或連續延伸接觸元件，以降低至該汲極和源極區 211 之總體接觸電阻。

典型上，該接觸層級 240 可基於廣為接受之"平面"製程技術而形成，例如，藉由在熱處理(heat treatment)期間沉積耐火金屬和啟始化學反應並且接著沉積適當之介電材料(如二氧化矽)，其中該所沉積之介電材料可藉由 CMP 等進行平面化。其後，為了得到個別接觸開口，可藉由微影和非等向性蝕刻技術對該介電材料進行圖案化，並且可接著利用期望之接觸金屬(如鎢等)填充該等個別接觸開口。

第 2v 圖示意地描繪該 P 通道電晶體 250P 之接觸結構 240，其可具有類似上述之組構。

接下來，可藉由例如設置介電材料(例如：以低 k 介電材料形式)並且於其中形成通孔(可連接至第一金屬化層之金屬線)來形成金屬化系統(metallization system)。

在一些例示實施例中，可藉由包含含金屬電極材料以及高 k 介電材料之精密結構來代替該閘極電極結構 220。為了此目的，在形成該介電材料 241 內之接觸元件 242 之前，可基於例如 TMAH 選擇性地移除該閘極電極材料 222，其中 TMAH 可有效率地相對於二氧化矽和氮化矽而選擇性地移除矽。在其他案例中，可使用其他選擇性蝕刻配方(如基於 HBr 之電漿輔助製程)，同時在其他例示實施例中，可使用任何選擇性蝕刻製程，視該閘極電極結構 220 和四周介電材料之材料組成(material composition)而定。其後，可自該鰭 210 之暴露側壁部位移除該閘極介電質(如該介電材料 221B)。如果該閘極介電質大致上由二氧化矽所組成，則可利用 HF 來完成移除。

第 2w 圖示意地描繪在上述製程順序之後和進一步之製造階段中沿著該鰭之寬度方向之剖面圖。如圖中所描繪，該裝置 200 可包括代替閘極電極結構 220R，該代替閘極電極結構 220R 可包括含金屬材料 222R(如氮化鈦等)以及高 k 介電材料 221R，且該高 k 介電材料 221R 可覆蓋該等鰭 210 之側壁部位和頂部表面。因此，可設置三閘極組構，該三閘極組構包含在該鰭 210 之側壁上所形成之個別閘極電極結構 220A、220C 以及在該鰭 210 之頂部上所形成之閘極電極結構 220B，亦藉此設置複數個電晶體單元 250A…250D。因此，該等電晶體單元 250A…250D 之每一者或其組合均代表基於經適當選擇之金屬材料 222R 和用於形成對應之汲極和源極區之製造順序而對於每一種導電

性類型提供特定臨限電壓(threshold voltage)之三閘極電晶體。如果需要更高的臨限電壓，為了產生普通大的臨限電壓偏移(shift)，可將不同功函數(work function)整合於多個閘極金屬，同時，在其他案例中，為了產生輕微的臨限電壓偏移，可實施經適當設計之環形佈植。

因此，由於降低串聯電阻和使用廣為接受且有效率之製造技術以及廣為接受之平面電晶體組構機制，可得到具增強之電晶體效能之有效率的三維電晶體組構。此外，該汲極和源極區、通道區或鰭 210、及個別隔離結構之自我校準組構可基於先前所述之遮罩方式而完成。再者，相較於傳統策略，可免除用於提供複數個電晶體之連續汲極和源極區之複雜磊晶生長製程，亦藉此增強總體製程效率。

藉由參考第 3a 至 3c 圖，可詳述用於形成雙閘極或 FinFET 電晶體組構之對應製程順序。一般而言，可使用如先前所述用於三閘極電晶體組構 250 的類似製程順序，然而其中，可藉由不移除用於在該半導體材料中圖案化該等鰭之硬遮罩而於該等鰭之頂部設置普通厚之罩蓋層。因此，對應之閘極電極材料可藉由厚絕緣體(insulator)而與該鰭之頂部隔離，且電流僅發生於該鰭之側邊表面(side surface)上。一般而言，對於相較於三閘極組構之相同有效的電晶體寬度而言，該 FinFET 必須增加鰭之高度，同時，由於設置於該頂部表面上方之閘極電極大致上對該鰭內之空乏化沒有效果，因此可能必須縮減該鰭之寬度。

第 3a 圖示意地描繪半導體裝置 300 之剖面圖，該半

導體裝置300可具有與如第2j圖所示之半導體裝置200非常類似之組構。因此，除了第一個數字是"3"而不是"2"以外，類似元件均標示以相同的元件符號。因此，該裝置300可包括半導體層 303，該半導體層 303 包含多個隔離區308A(藉由個別深鰭 310L 分隔開)，且該等隔離區 308A 上設置有多個鰭 310，而罩蓋元件 306(如氮化矽元件)結合蝕刻停止材料 304A(例如：以二氧化矽形式)罩蓋該等鰭 310。如先前所說明，相較於該等鰭 210，該等鰭 310 可增加大約 30 至 40nm 之高度，同時可縮減其寬度且寬度範圍在大約 10 至 15nm。

該半導體裝置300可基於如先前所述參考根據對應於第 2b 至 2j 圖所述之裝置 200 之相同製造技術而形成。因此，將省略個別說明。然而，應體會到，與參考第 2b 至 2j 圖所述之製程方式相反，該等罩蓋元件 306 可代表先前形成作為圖案化該等鰭 310 之硬遮罩之對應間隔件元件，如同參考該等間隔件元件 206(如第 2g 圖所示)所亦說明者。也應體會到，該等罩蓋元件 306 可形成為具有縮減之寬度，以便符合該等鰭 310 之需求。同樣地，為了得到該鰭 310 所期望之高度增加，可適當地調適用於在該隔離區 308A 中形成凹陷 308R 之製程(也如同當參照該半導體裝置 200 時，參考第 2i 圖所說明者)。

第 3b 圖示意地描繪具有基本井佈植種類 309W 之裝置 300 之剖面圖，該井佈植種類 309W 可如同當參照該半導體裝置 200 時參考第 2k 至 2l 圖所說明者進行佈植。其

後，可繼續進一步處理，如同先前參考該裝置 200 所述者。也就是說，可藉由設置適當之介電材料並沉積閘極電極材料來形成個別閘極電極結構或假性閘極電極結構(dummy gate electrode structure)。其後，為了完成基本電晶體組構，可暴露該汲極和源極區域並且應用對應之"平面"製造程序。再者，如果有需要，如先前所述，可以高 k 介電材料結合含金屬電極材料來代替該閘極電極結構。

第 3c 圖示意地描繪在進階之製造階段中之半導體裝置 300，其中替代閘極電極結構 320R 可結合高 k 介電材料 321 而設置於該等鰭 310 周圍。因此，可為每一個電晶體單元 350A…350D 建立雙閘極組構，亦即，第一閘極電極結構 320A 可設置於該鰭 310 之其中一個側壁上，而第二閘極電極結構 320C 可設置於相對之側壁上。另一方面，仍然可以該罩蓋元件 306 結合該蝕刻停止層 304A(如第 3b 圖所示)覆蓋該鰭 310 之頂部表面。

因此，本發明之內容提供了增強之三維電晶體組構(亦即，雙閘極和三閘極電晶體組構)，其中該等電晶體之鰭可基於塊狀半導體材料而設置，藉此增加半導體容積，同時連續之汲極和源極區域可連接至該鰭之通道區，而無須可作為高電阻汲極和源極部位之中間鰭部位(intermediate fin portion)(如同典型在案例中之傳統 FinFET 和三閘極電晶體架構所需要者)。再者，該通道區域(亦即，該等鰭和該閘極電極結構)、該汲極和源極區以及該隔離結構可基於可容許自我校準製程順序

(self-aligned process sequence)之遮罩方式來設置，同時可免除用於設置連續汲極和源極區域之複雜選擇性磊晶生長製程。再者，在形成該等鰭之後，可應用來自二維(two-dimensional)或平面電晶體製造製程之廣為接受且有效率之製程技術(可能包含有效率的應變引發機制)，使得除了增加半導體容積以及免除該等鰭中之高電阻汲極和源極部位之外，還可有利地應用進一步的效能增強機制。

以上所揭示之特定實施例僅為說明，當熟習本領域者在看過本文所教示之優點後，咸了解本發明可以不同但是相等之方式做各種修改和實現。舉例而言，以上所提出之製程步驟可以不同之順序實施。再者，除了下文中申請專利範圍所描述者以外，本文中所示並非意圖限制建構或設計之細節。因此，顯然可對於上文中所揭示之特定實施例進行修飾或修改，且所有此類變動均視為落於本發明之範疇和精神內。因此，本發明欲保護之內容係如下文中申請專利範圍所提出者。

【圖式簡單說明】

本發明所揭示之內容可藉由參考以下說明並配合附加圖式而了解，其中相同的元件符號識別類似的元件，且其中：

第 1a 至 1b 圖分別示意地描繪包括以 SOI 基板為基礎之傳統 FinFET 電晶體單元之半導體裝置之透視圖和頂部視圖；

第 2a 圖根據例示實施例示意地描繪包含形成於塊狀

基板中之"三維"電晶體組構之透視圖，其中該汲極和源極區和該鰭可藉由提供相對於該閘極電極結構之自我校準製程技術而於共同製程中形成；

第 2b 至 2i 圖根據例示實施例示意地描繪，於用以在塊狀半導體層中形成多個鰭之各種製造階段期間，包含複數個 FinFET 電晶體單元之半導體裝置之透視圖；

第 2j 圖根據例示實施例示意地描繪在實施井佈植製程前該鰭之剖面圖；

第 2k 至 2l 圖分別示意地描繪在井佈植製程之後之透視圖和剖面圖；

第 2m 至 2o 圖根據例示實施例示意地描繪，於形成自我校準之閘極電極結構之各種製造階段期間，該半導體裝置之透視圖；

第 2p 圖示意地描繪沿著該鰭之方向之剖面圖；

第 2q 圖示意地描繪該半導體裝置之頂部視圖；

第 2r 至 2v 圖根據例示實施例示意地描繪，於各種製造階段期間，沿著該鰭之長度方向之透視剖面圖；

第 2w 圖根據例示實施例示意地描繪具有金屬替代閘極和高 k 介電材料沿著該鰭之寬度方向之剖面圖；以及

第 3a 至 3c 圖根據所描繪之其他實施例分別示意地描繪包含複數個雙通道電晶體單元之半導體裝置之剖面圖和透視圖。

雖然本文中所提出之發明內容能夠容許各種修改和替代形式，但是其特定實施例已藉由範例之方式顯示於附

加圖式中，並且詳述於本文中。然而，應了解到，本說明書中之特定實施例並非意圖限制本發明為所揭示之特殊形式，相反地，係意圖涵蓋所有落於如本發明附加申請專利範圍所定義之精神與範疇中之修改、等效及替代態樣。

【主要元件符號說明】

100	半導體裝置	101	基板
102	埋置絕緣層	103	半導體層
104	間隔件元件	110	鰭
110A	側壁	110B	側壁
110H	高度	110L	長度
110W	寬度	111	汲極和源極區
112	罩蓋層	120A	閘極電極結構
120B	閘極電極結構	150	FinFET
200	半導體裝置	201	基板
203	半導體層	203C	逆摻雜區
203R	凹陷	204	層堆疊
204A	蝕刻停止層	204B	遮罩層
204M	遮罩特徵	205	光阻劑特徵
206	側壁間隔件元件	207	遮罩層
207A	遮罩元件	207B	遮罩元件
207C	遮罩元件	207D	遮罩特徵
207M	開口	207N	開口
208	隔離結構	208A	隔離結構
208R	凹陷	209	佈植順序、佈植製程

209A 傾斜佈植步驟
210 鰭
210H 高度
210W 寬度
211D 汲極區
211S 源極區
214 應變引發材料
220S 犧牲閘極電極結構
221B 閘極介電質
222 閘極電極材料
230 遮罩材料
240 接觸結構
250 雙閘極或三閘極電晶體
250P P通道電晶體
304A 蝕刻停止材料
308A 隔離區
310 鰭
320C 閘極電極結構
321 高k介電材料
350D 電晶體單元
209W 井佈植種類
210A 深鰭
210L 上側部位
211 汲極和源極區
211F 側壁
213 通道區
220 閘極電極結構
221A 閘極介電質
221C 閘極介電質
223 間隔件結構
231 蝕刻遮罩
241 層間介電材料
250N N通道電晶體
300 半導體裝置
306 罩蓋元件
308R 凹陷
320A 閘極電極結構
320R 閘極電極結構
350A 電晶體單元

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發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫）

※ 申請案號：98121967

※ 申請日：98.6.30 ※IPC 分類：H01L 21/336 (2006.01)
H01L 21/76 (2006.01)

一、發明名稱：（中文/英文）

形成在塊狀基板上之雙閘極與三閘極電晶體及形成該電晶體之方法

DOUBLE GATE AND TRI-GATE TRANSISTOR FORMED ON A BULK SUBSTRATE AND METHOD FOR FORMING THE TRANSISTOR

二、中文發明摘要：

如鰭形電晶體(FinFET)和三閘極電晶體之三維電晶體結構可基於增強之遮罩方式而形成，藉此在塊狀半導體材料中以自我校準的方式形成汲極和源極區域、該等鰭和隔離結構。在定義基本的鰭結構之後，可使用高效率之平面電晶體組構製造技術，藉此進一步增強該三維電晶體組構之總體效能。

三、英文發明摘要：

Three-dimensional transistor structures such as FinFETS and tri-gate transistors may be formed on the basis of an enhanced masking regime, thereby enabling the formation of drain and source areas, the fins and isolation structures in a self-aligned manner within a bulk semiconductor material. After defining the basic fin structures, highly efficient manufacturing techniques of planar transistor configurations may be used, thereby even further enhancing overall performance of the three-dimensional transistor configurations.

七、申請專利範圍：

1. 一種方法，包括：

於半導體裝置之半導體層上方形成層堆疊，該層堆疊包括形成於該半導體層上方之蝕刻停止層以及形成於該蝕刻停止層上方之第一遮罩層；

圖案化該第一遮罩層，以便得到遮罩特徵；

於該遮罩特徵之側壁上形成間隔件元件；

相對於該側壁間隔件元件選擇性地移除該遮罩特徵；

設置具有暴露該側壁間隔件元件之一部份之第一開口之第二遮罩層，以便定義通道區域和汲極與源極區域；

利用該側壁間隔件元件和該第二遮罩層作為蝕刻遮罩從而於該半導體層中形成溝槽，以便於該半導體層中形成鰭，該鰭對應於該通道區域；

至少於該鰭之側壁上形成閘極電極結構；以及

於該汲極和源極區域中形成汲極和源極區，該汲極和源極區連接至該鰭。

2. 如申請專利範圍第 1 項之方法，其中，設置該第二遮罩層係包括設置第二開口，以定義隔離結構之位置和側向尺寸。

3. 如申請專利範圍第 2 項之方法，其中，形成該等溝槽係包括基於該第一和第二開口形成該等溝槽。

4. 如申請專利範圍第 3 項之方法，復包括以介電材料填充

該等溝槽和該第一和第二開口。

5. 如申請專利範圍第4項之方法，復包括將該等開口中之介電材料凹陷至低於對應於該半導體層之表面之高度，以便調整該鰭之有效高度。

6. 如申請專利範圍第5項之方法，復包括在凹陷該介電材料之後基於該第二遮罩層來實施井佈植製程。

7. 如申請專利範圍第6項之方法，復包括利用傾斜角度實施逆摻雜佈植製程，以在該半導體層之經暴露之側壁區域引進相對於該汲極和源極區為逆摻雜之摻雜物種。

8. 如申請專利範圍第1項之方法，其中，形成該閘極電極結構係包括於該第二遮罩層之該第一開口內之該鰭的經暴露之側壁區域上形成介電材料，並且在形成該汲極和源極區之前於該第一開口中沉積定位件材料和閘極電極材料之至少一者。

9. 如申請專利範圍第8項之方法，復包括在移除該第二遮罩層以及形成該汲極和源極區，同時利用定位件材料和閘極電極材料之至少一者作為佈植遮罩。

10. 如申請專利範圍第9項之方法，其中，形成該汲極和源極區係包括實施第一佈植製程、於定位件材料和閘極電極材料之至少一者之側壁上形成第二側壁間隔件元件以及利用該第二側壁間隔件元件作為佈植遮罩來實施第二佈植製程。

11. 如申請專利範圍第8項之方法，復包括以含金屬材料取代該定位件材料和閘極電極材料之至少一者。

12.如申請專利範圍第 11 項之方法，復包括自該經暴露之側壁部位移除該介電材料並且沉積高 k 介電材料。

13.如申請專利範圍第 12 項之方法，復包括暴露該鰭之頂部表面，以及於該經暴露之頂部表面上沉積該高 k 介電材料。

14.如申請專利範圍第 12 項之方法，復包括於該鰭之頂部表面上形成罩蓋層，以及於該罩蓋層上沉積該高 k 介電材料。

15.如申請專利範圍第 1 項之方法，復包括在形成該汲極和源極區之前於該汲極和源極區域中之該半導體層中形成洞孔，以及以應變引發半導體材料填充該等洞孔。

16.一種形成電晶體之方法，該方法包括：

於半導體層上方形成遮罩特徵，該遮罩特徵定義欲形成於該半導體層中之鰭之側向尺寸；

形成具有第一開口和第二開口之遮罩層，該第一開口定義該鰭之長度，該第二開口定義隔離結構之側向尺寸和位置；

利用該遮罩層作為蝕刻遮罩而以共同的蝕刻製程於該半導體層中形成該鰭和隔離溝槽；

於該鰭之第一側壁之一部份上形成第一閘極電極結構，並且於該鰭之第二側壁之一部份上形成第二閘極電極結構；以及

於鄰接該鰭之末端部位之該半導體層中形成汲極和源極區。

17.如申請專利範圍第 16 項之方法，其中，形成該遮罩特徵係包括於該半導體層上形成蝕刻停止層、於該蝕刻停止層上形成犧牲遮罩層、圖案化該犧牲遮罩層以形成線特徵、於該線特徵之側壁上形成間隔件元件以及選擇性地移除該線特徵。

18.如申請專利範圍第 16 項之方法，其中，形成該第一和第二閘極電極係包括在形成該鰭之後以定位件材料填充該第一和第二開口，以及在形成該汲極和源極區之後以高 k 介電材料和含金屬電極材料取代該定位件材料。

19.如申請專利範圍第 16 項之方法，其中，第三閘極電極係形成於該鰭之頂部表面上。

20.如申請專利範圍第 17 項之方法，其中，該蝕刻停止層係由二氧化矽所組成，而該犧牲遮罩材料係由矽所組成。

21.一種半導體裝置，包括：

半導體層；

第一隔離區和第二隔離區，係形成於該半導體層中，並且藉由以該半導體層之材料形成之深鰭將該第一和第二隔離區分隔開；

形成於該第一隔離區中之第一凹陷和形成於該第二隔離區中之第二凹陷，以便暴露該深鰭之一部份，其中該深鰭之一部分代表多閘極電晶體之鰭，且該鰭之高度小於該半導體層之厚度；

第一閘極電極結構，其係形成於該鰭之第一側壁

上；

第二閘極電極結構，其係形成於該鰭之第二側壁上；以及

汲極和源極區，其係連接至該鰭。

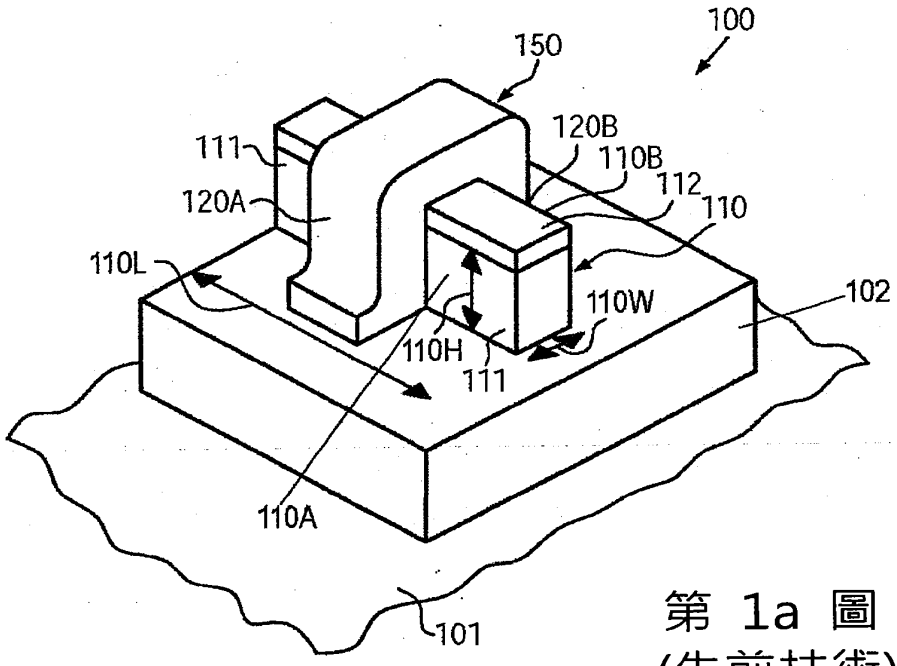
22.如申請專利範圍第 21 項之半導體裝置，復包括形成於該鰭之頂部表面上之第三閘極電極結構。

23.如申請專利範圍第 22 項之半導體裝置，復包括形成於該半導體層上方之間隔件結構，該間隔件結構定義汲極和源極延伸區自位於該鰭中之通道區之側向延伸。

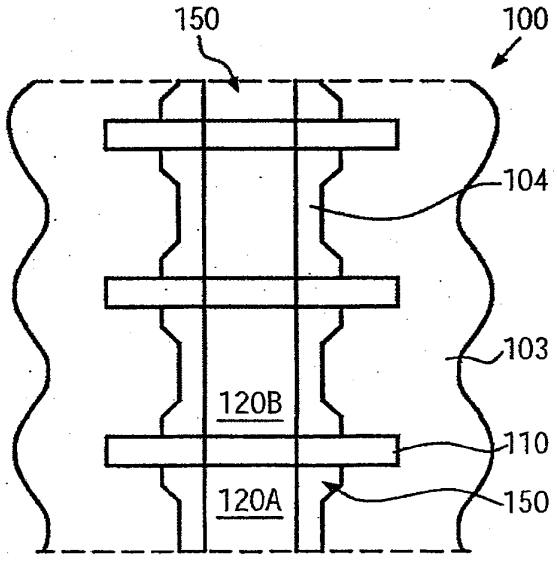
24.如申請專利範圍第 21 項之半導體裝置，其中，該第一和第二閘極電極結構包括高 k 閘極介電材料。

25.如申請專利範圍第 23 項之半導體裝置，復包括形成於鄰接該間隔件結構之該半導體層中之應變引發半導體合金。

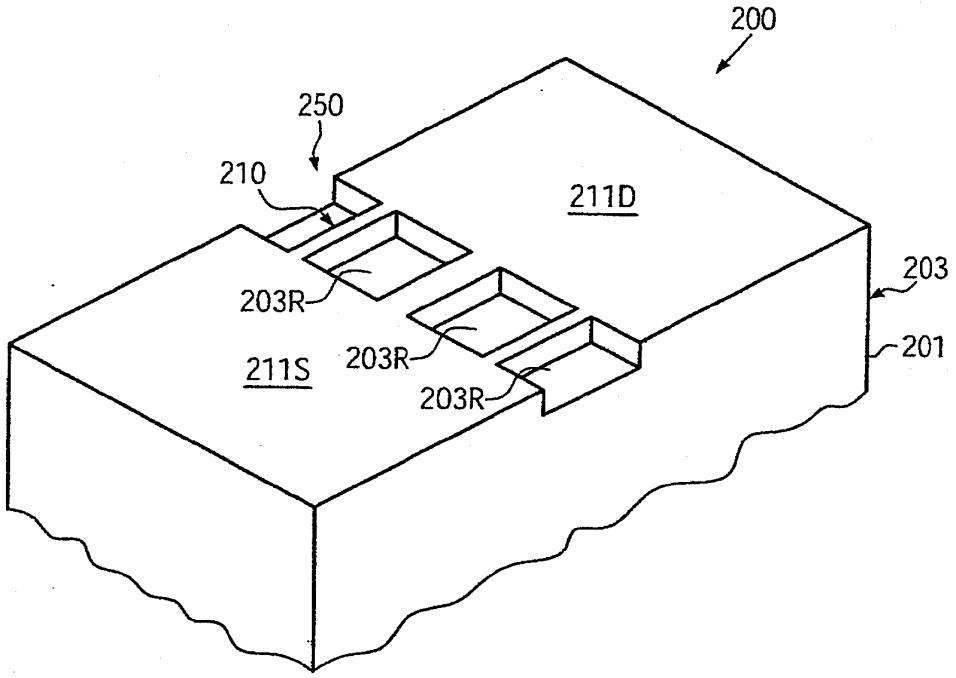
八、圖式:



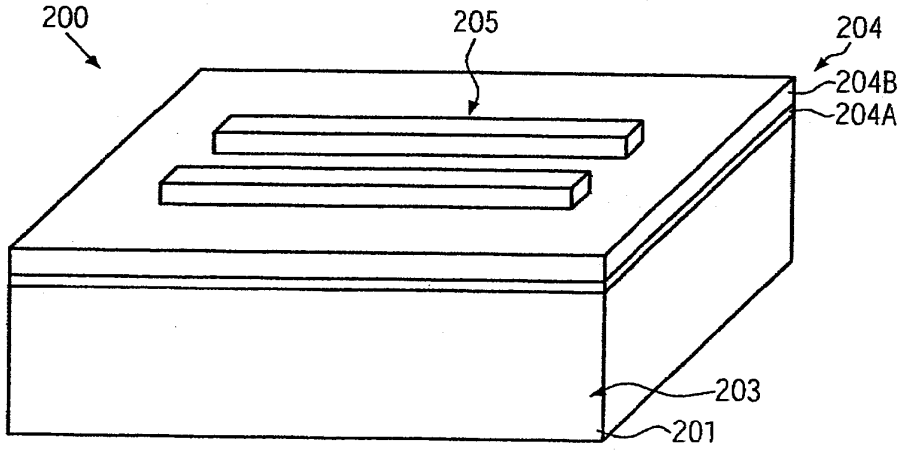
第 1a 圖
(先前技術)



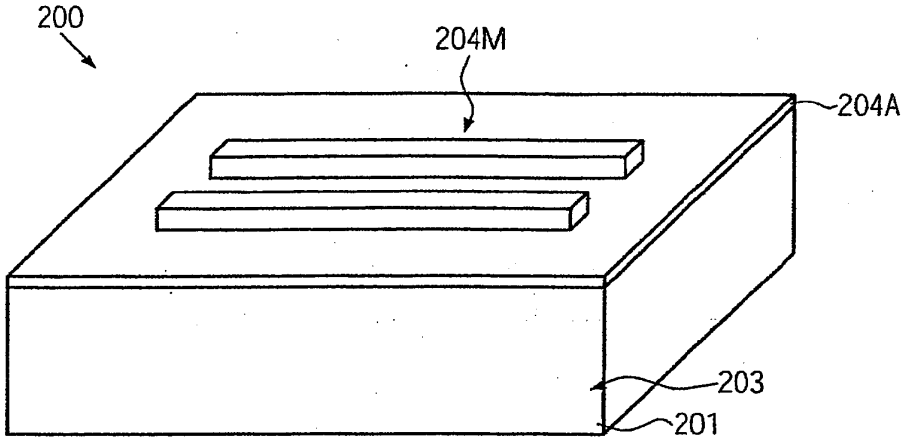
第 1b 圖
(先前技術)


200
250
210
211D
203
203R
201
211S
203R
203R

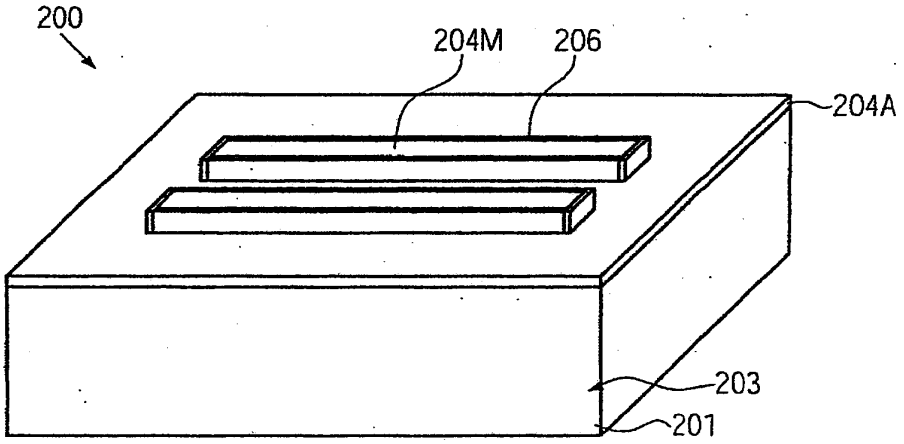
第 2a 圖


200
205
204
204B
204A
203
201

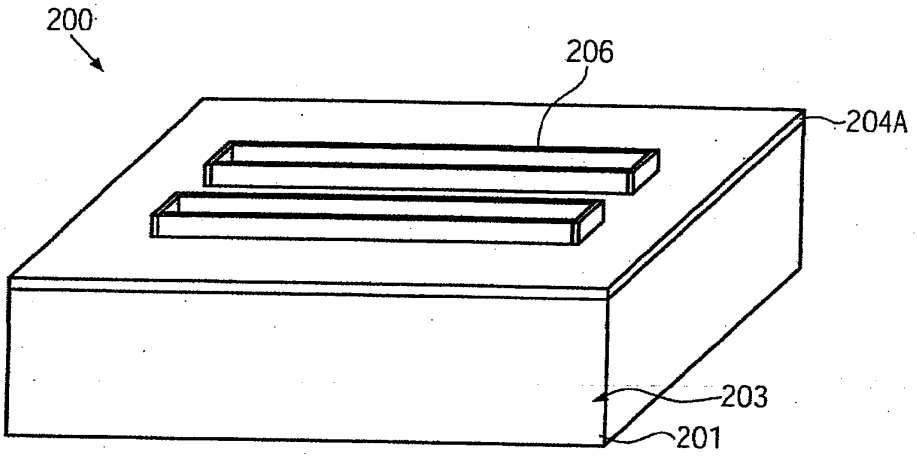
第 2b 圖



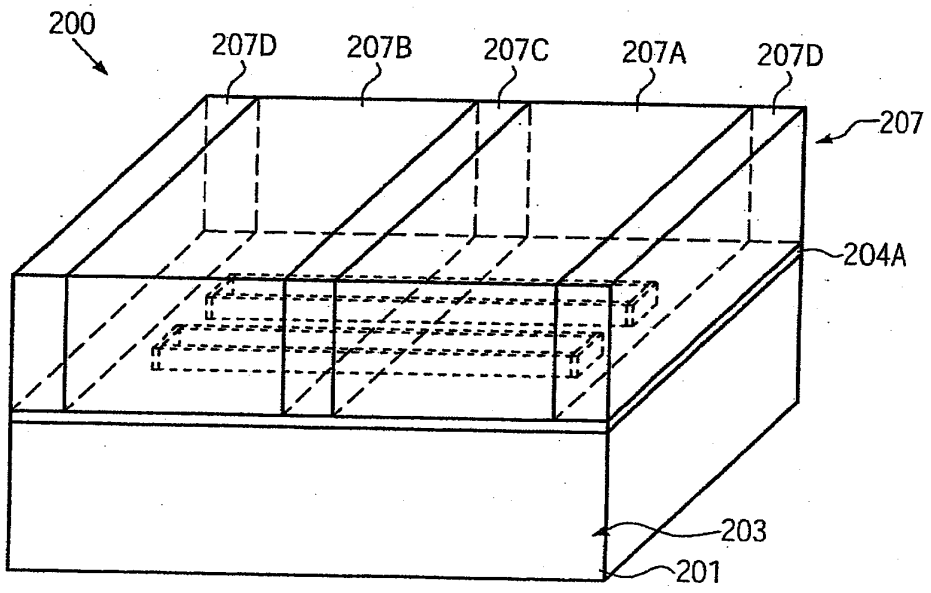
第 2c 圖



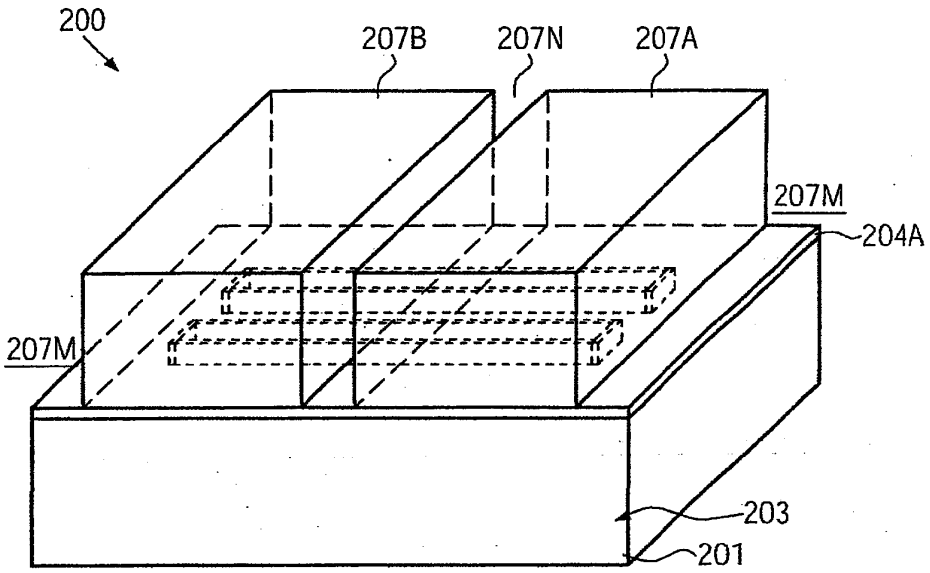
第 2d 圖


200
206
204A
203
201

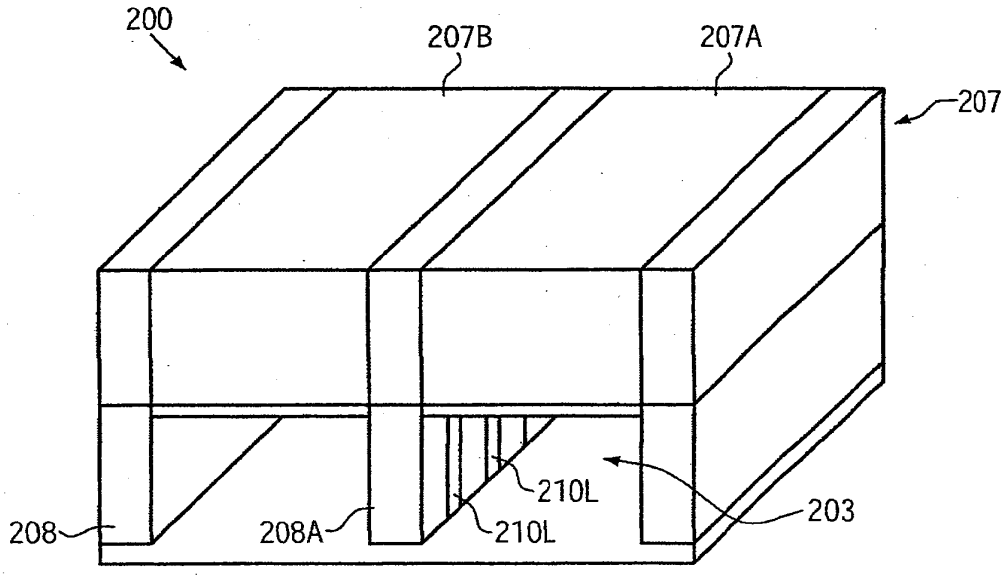
第 2e 圖


200
207D
207B
207C
207A
207D
207
204A
203
201

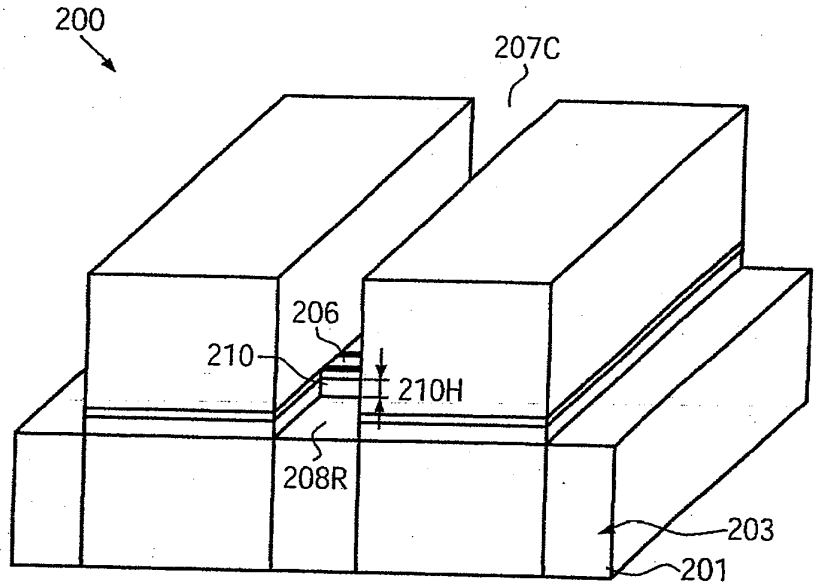
第 2f 圖


200
207B
207N
207A
207M
204A
207M
203
201

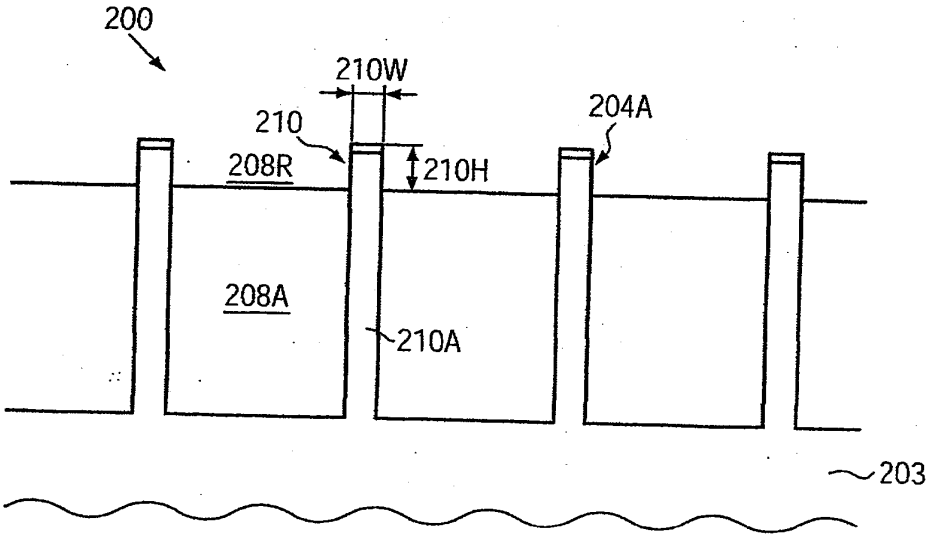
第 2g 圖


200
207B
207A
207
210L
203
208
208A
210L

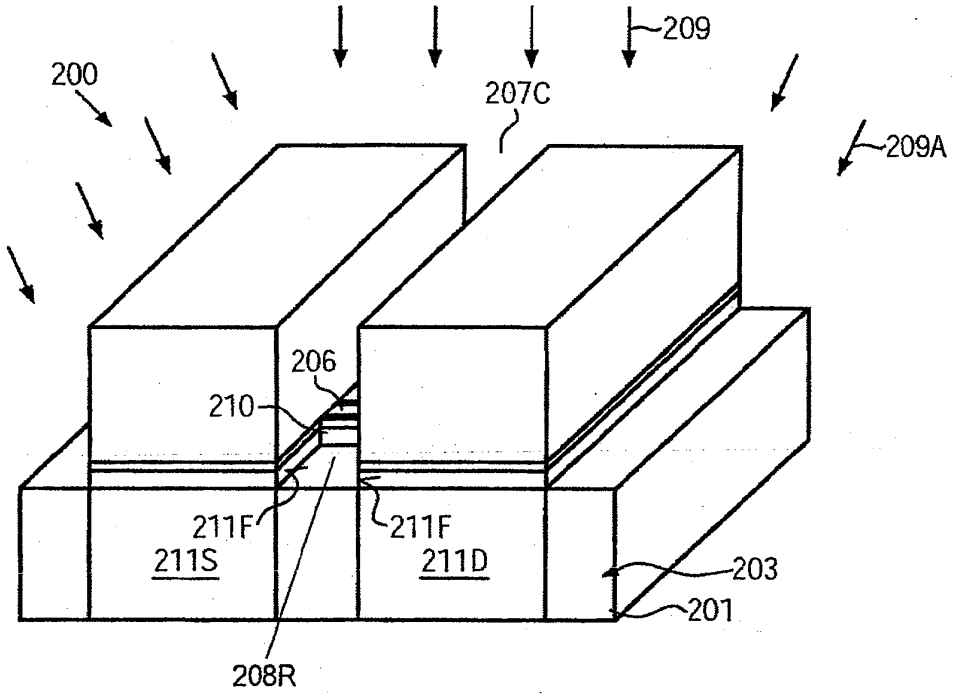
第 2h 圖


200
207C
206
210
210H
208R
203
201

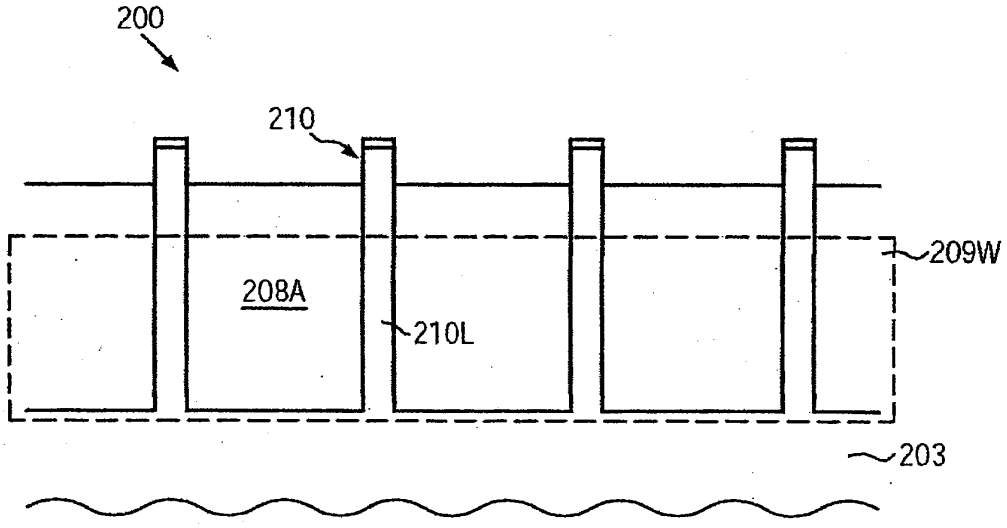
第 2i 圖


200
210W
210
204A
208R
210H
208A
210A
203

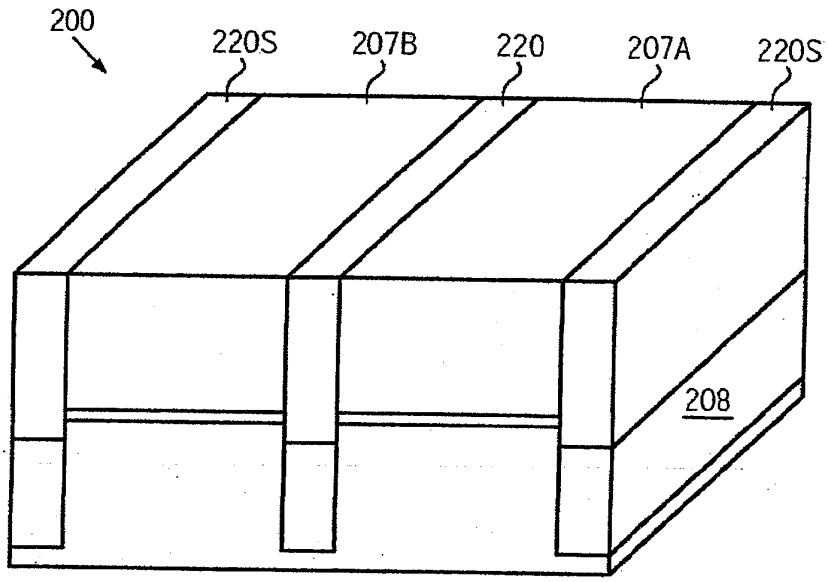
第 2j 圖


209
200
207C
209A
206
210
211F
211F
211S
211D
203
201
208R

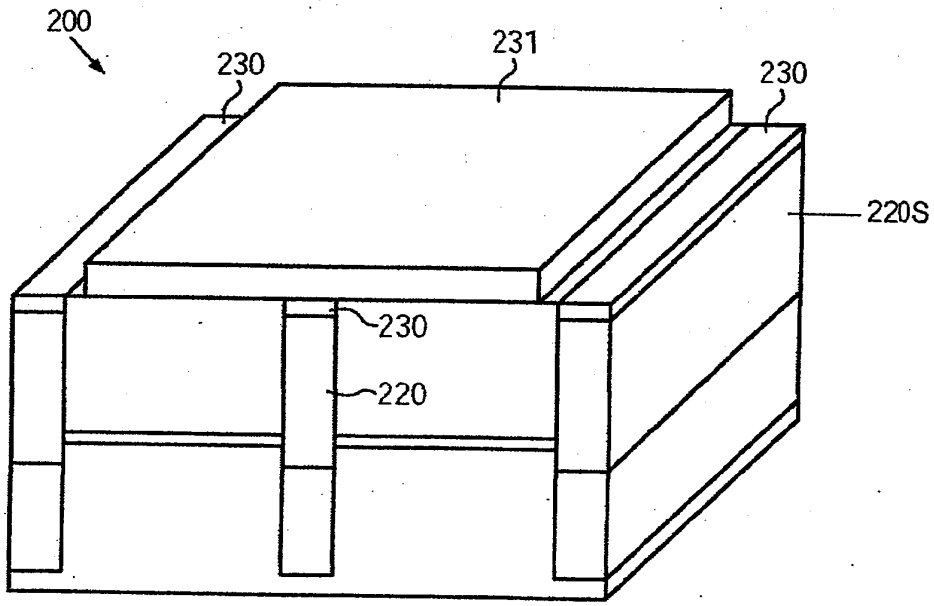
第 2k 圖


200
210
209W
208A
210L
203

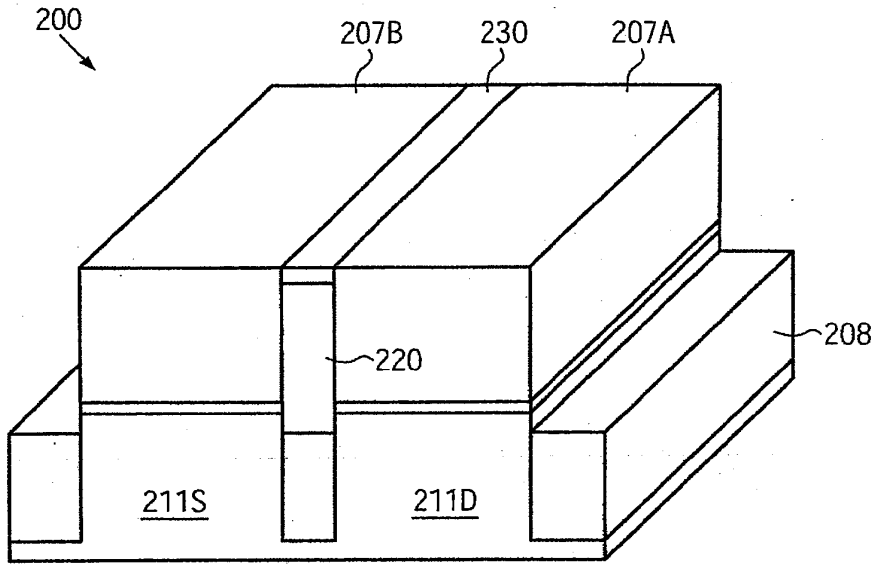
第 2l 圖



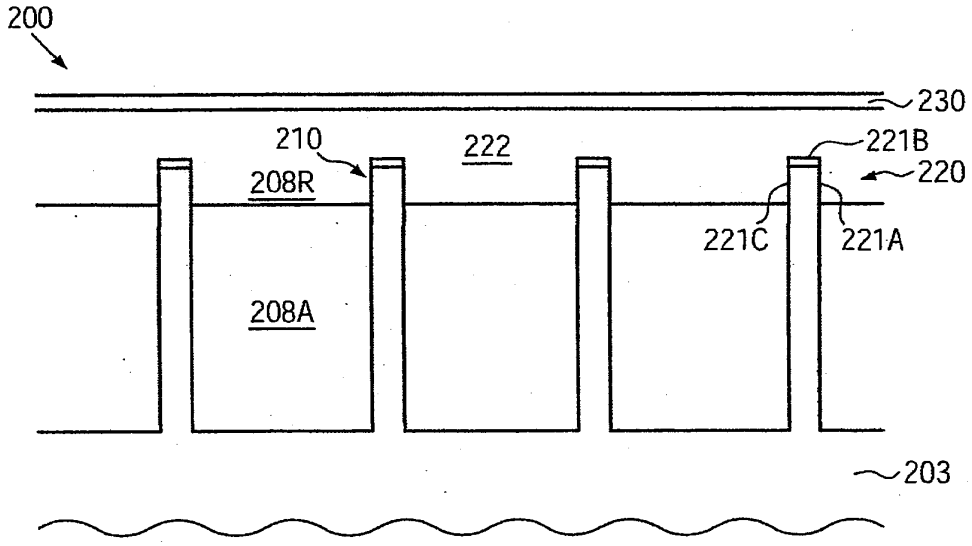
第 2m 圖



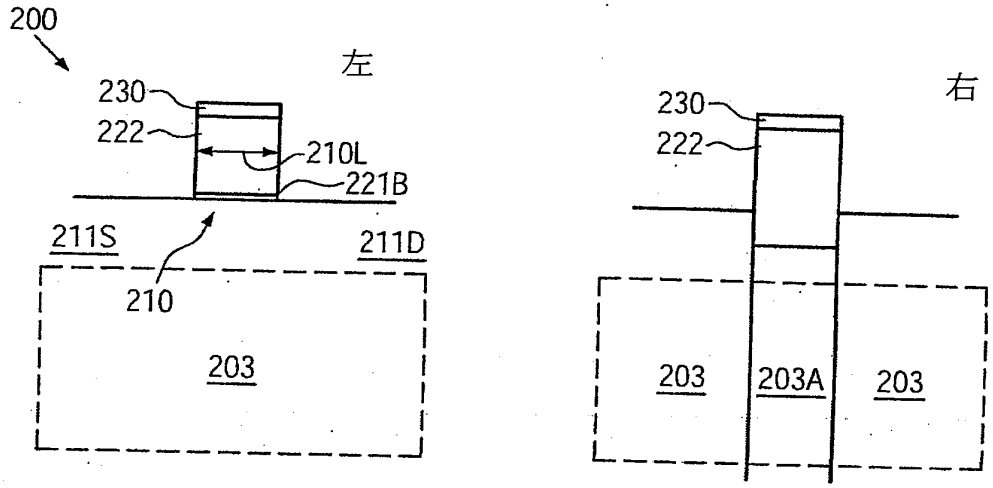
第 2n 圖


200
207B
230
207A
208
220
211S
211D

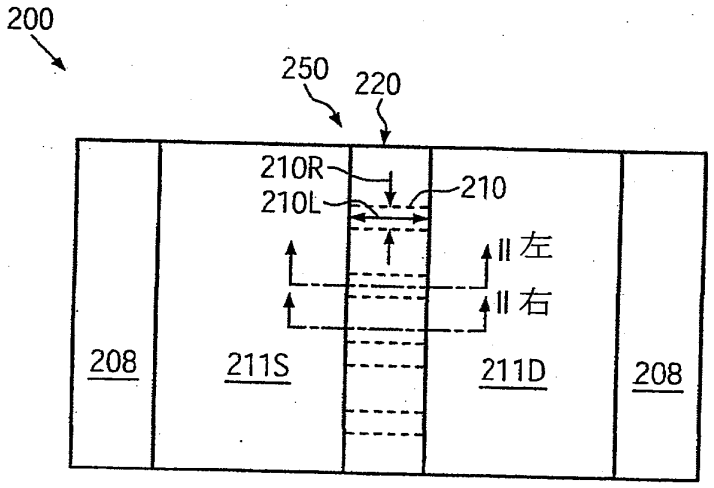
第 2o 圖


200
230
210
222
221B
208R
220
221C
221A
208A
203

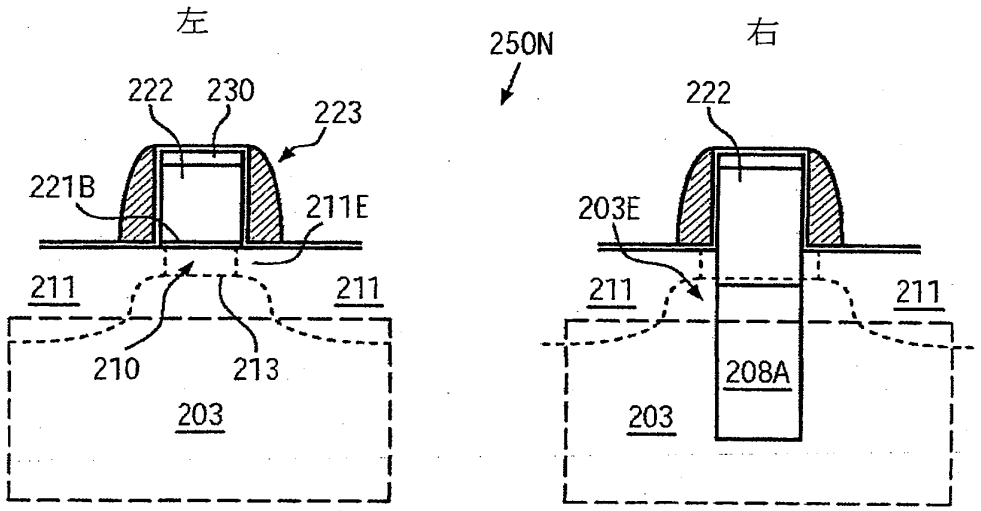
第 2p 圖


200
左
230
222
210L
221B
211S
211D
210
203
右
230
222
203
203A
203

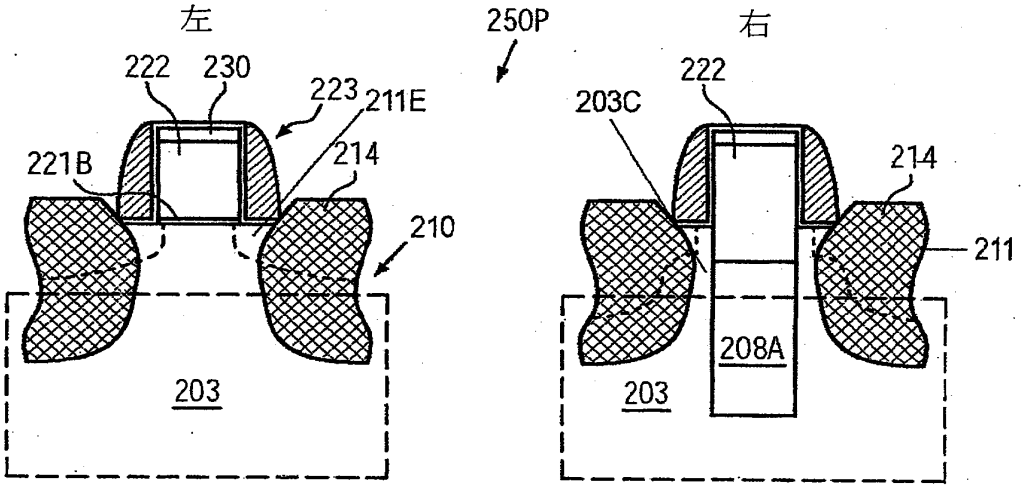
第 2r 圖


200
250
220
210R
210L
210
II 左
II 右
208
211S
211D
208

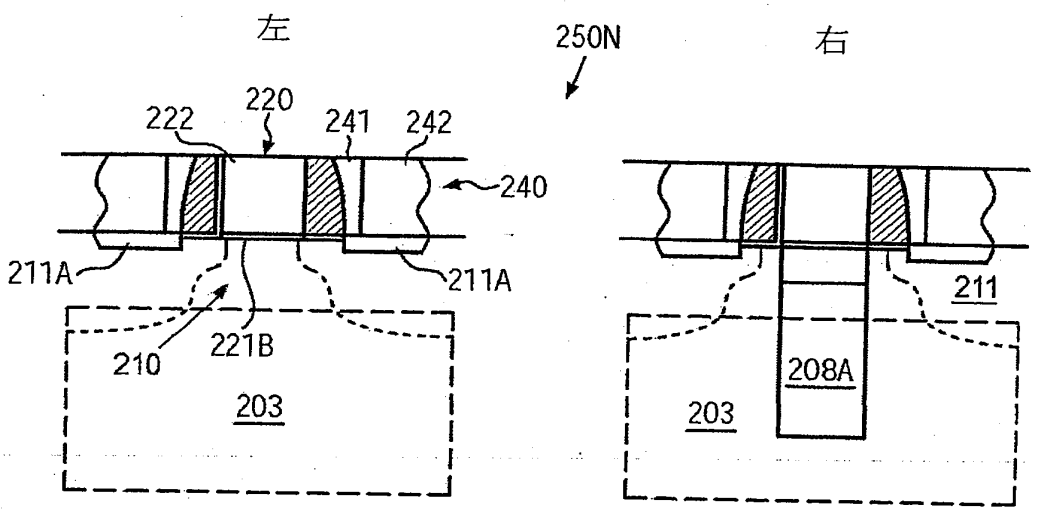
第 2q 圖


左
250N
右
222
230
223
221B
211E
211
211
210
213
203
222
203E
211
211
208A
203

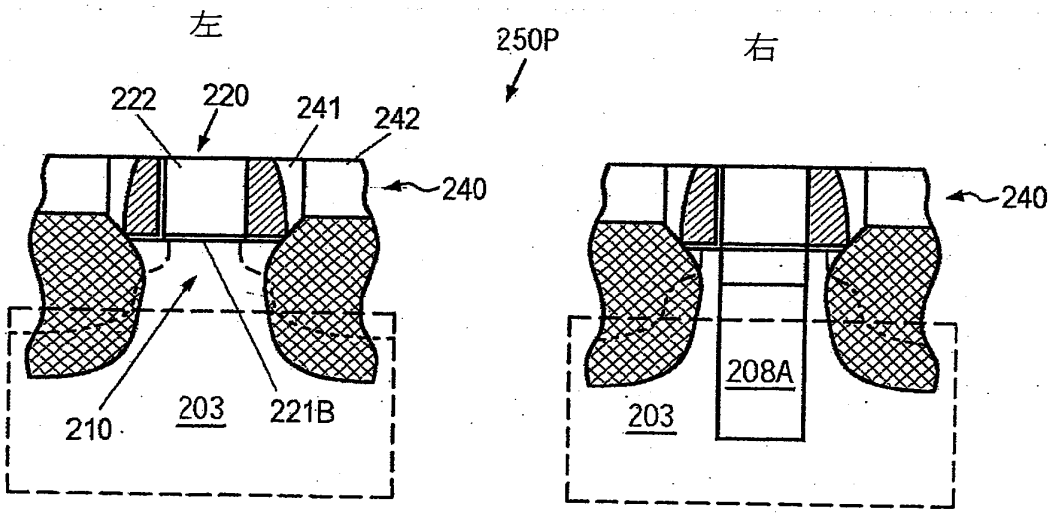
第 2s 圖


左
250P
右
222
230
223
211E
221B
214
210
203
222
203C
214
211
208A
203

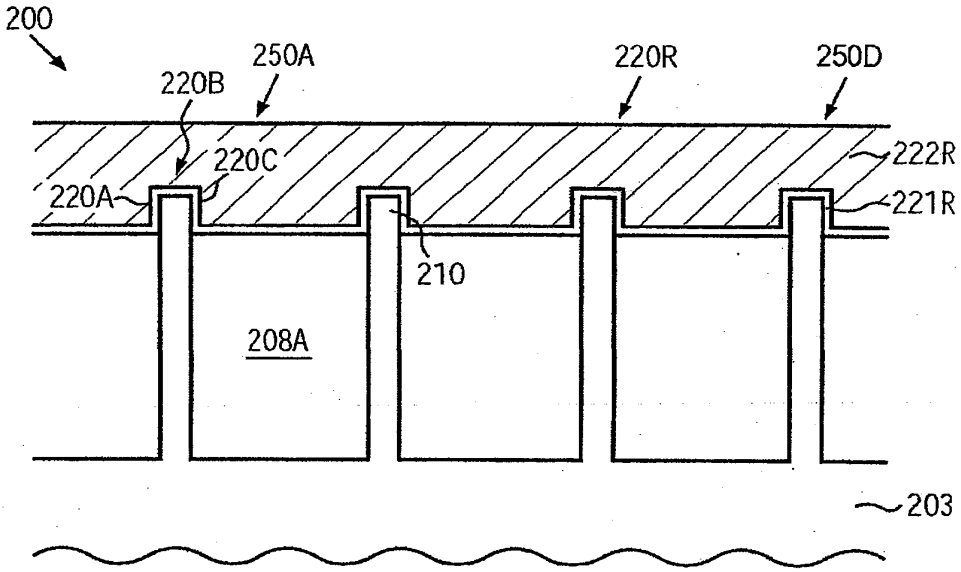
第 2t 圖


左
250N
右
222
220
241
242
240
211A
211A
210
221B
203
211
208A
203

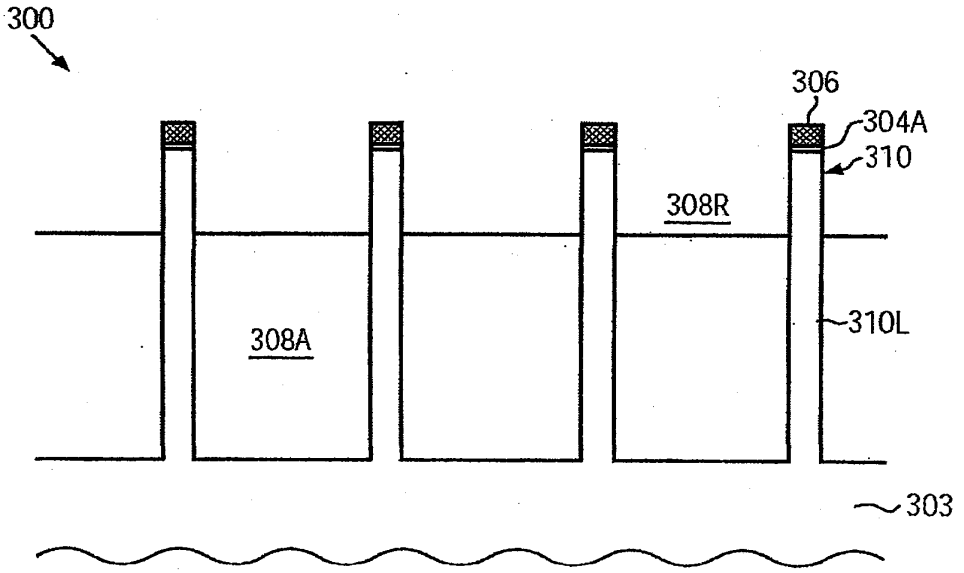
第 2u 圖


左
250P
右
222
220
241
242
240
240
210
203
221B
208A
203

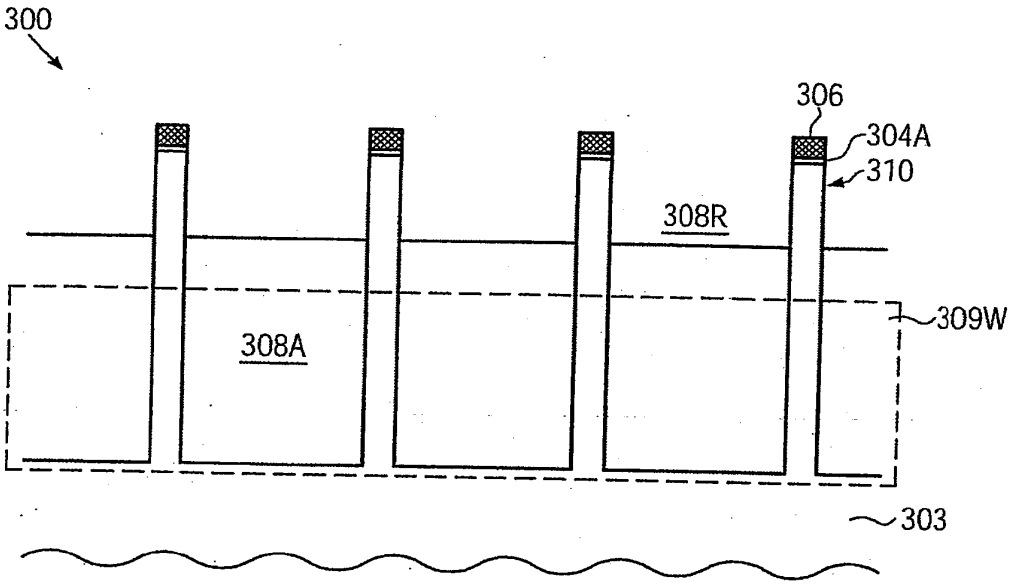
第 2v 圖


200
250A
220R
250D
220B
220C
222R
220A
221R
210
208A
203

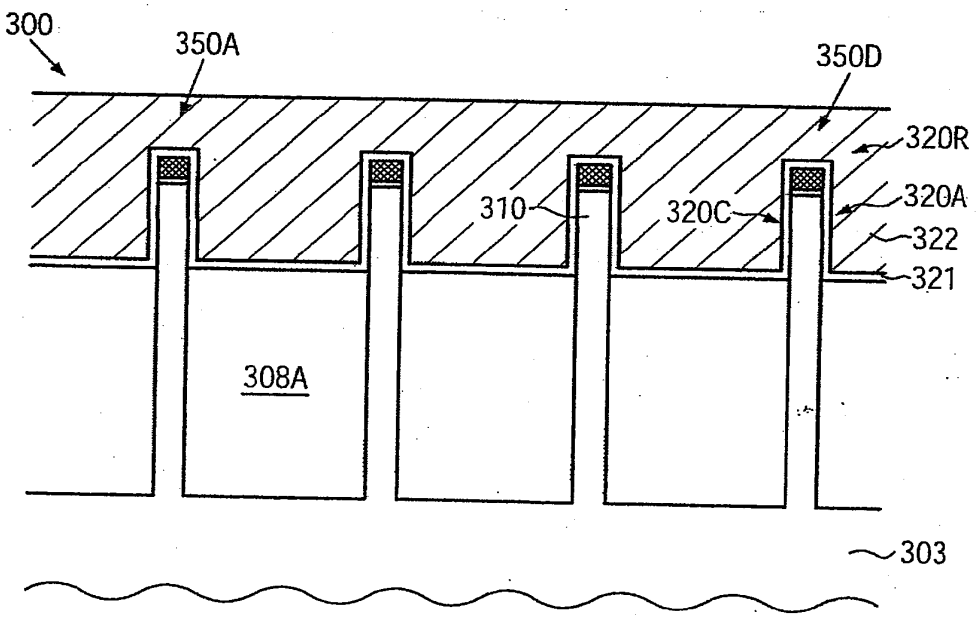
第 2w 圖


300
306
304A
310
308R
310L
308A
303

第 3a 圖


300
306
304A
310
308R
309W
308A
303

第 3b 圖


300
350A
350D
320R
320A
310
320C
322
321
308A
303

第 3c 圖

四、指定代表圖：

(一)本案指定代表圖為：第（ 2a ）圖。

(二)本代表圖之元件符號簡單說明：

200	半導體裝置
201	基板
203	半導體層
203R	凹陷
210	鰭
211D	汲極區
211S	源極區
250	雙閘極或三閘極電晶體

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無。

PATENT COOPERATION TREATY

ADVANCE E-MAIL

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING TRANSMITTAL OF COPY OF INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (CHAPTER I OF THE PATENT COOPERATION TREATY)
(PCT Rule 44bis.1(c))

To:

JKB-BV

BRASK, Justin K.
Blakely, Sokoloff, Taylor & Zafman LLP
1279 Oakmead Parkway
Sunnyvale, California 94085-4040
ETATS-UNIS D'AMERIQUE

Entered into Fl
By: LB

Date of mailing *(day/month/year)*	
30 June 2016 (30.06.2016)	
Applicant's or agent's file reference	IMPORTANT NOTICE
42P60397PCT	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2013/076673	19 December 2013 (19.12.2013)	

Applicant
INTEL CORPORATION

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)

RECEIVED
JUL 15 2016
BEAVERTON

RECEIVED
SUNNYVALE
JUL 06 2016
BLAKELY SOKOLOFF
TAYLOR & ZAFMAN

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Simin Baharlou

e-mail: pt09.pct@wipo.int

Form PCT/IB/326 (January 2004)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference 42P60397PCT	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2013/076673	International filing date *(day/month/year)* 19 December 2013 (19.12.2013)	Priority date *(day/month/year)*
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant INTEL CORPORATION		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 21 June 2016 (21.06.2016)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Simin Baharlou e-mail: pt09.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
BRASK, JUSTIN K.

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279 OAKMEAD PARKWAY SUNNYVALE CA 94085-4040 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**26 September 2014 (26.09.2014)**
Applicant's or agent's file reference 42P60397PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2013/076673	**19 December 2013 (19.12.2013)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 21/336(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	26 September 2014 (26.09.2014)	KIM, Young Jin Telephone No. +042 481 5771

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/076673

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

   ☐ on paper

   ☐ in electronic form

   b. (time)

   ☐ in the international application as filed.

   ☐ together with the international application in electronic form.

   ☐ subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/076673

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-25	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-25	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-25	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2007-0080380 A1 (PETER CHANG) 12 April 2007
D2: US 2011-0021027 A1 (FRANK SCOTT JOHNSON) 27 January 2011
D3: US 2013-0020615 A1 (SU CHEN FAN et al.) 24 January 2013
D4: KR 10-2005-0082099 A (SAMSUNG ELECTRONICS CO., LTD.) 22 August 2005
D5: US 2007-0054464 A1 (GUOWEI ZHANG) 08 March 2007

1 Novelty and Inventive Step

1.1. Claims 1-8

The subject matter of claim 1 differs from these prior art documents in a semiconductor structure comprising a pair of gate edge isolation structures centered with the semiconductor fin, wherein a first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 1 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Claims 2-8 are directly or indirectly dependent on claim 1 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.2. Claims 9-14

The subject matter of claim 9 differs from these prior art documents in a semiconductor structure comprising a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 9 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Continued on Supplemental Box

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

In claim 3, lines 3-4, 'the first semiconductor fin' lacks proper antecedent basis.

In claim 4, lines 2-3, 'the first gate structure' is not predefined.

Claim 5 is unclear since the expression 'the pair of and the third gateedge isolation structures' is vague.

In claim 19, lines 3-4, 'the sidewalls' and 'the first and second semiconductor fins' are not predefined.

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: Box No. V

Claims 10-14 are directly or indirectly dependent on claim 9 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.3. Claims 15-18
The subject matter of claim 15 differs from these prior art documents in a semiconductor structure comprising a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 15 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Claims 16-18 are dependent on claim 15 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.4. Claims 19-25
The subject matter of claim 19 differs from these prior art documents in a method comprising: forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins, wherein the dummy spacers of the first semiconductor fin are non-continuous with the dummy spacers of the second semiconductor fin; forming an isolation structure between the dummy spacers of the first and second semiconductor fins; removing the dummy spacers; and forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 19 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Claims 20-25 are dependent on claim 19 and therefore meet the requirements of PCT Article 33(2) and 33(3).

2. Industrial Applicability
Claims 1-25 are industrially applicable under PCT Article 33(4).

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Milton	~~C.~~ Clair	WEBB	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Aloha	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	20180 SW Inglis Drive
Address 2	

City	Aloha	State/Province	OR
Postal Code	97007	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Mark		BOHR	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Aloha	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	19475 SW Suncrest Lane
Address 2	

City	Aloha	State/Province	OR
Postal Code	97007	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tahir		GHANI	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	14191 NW Stonebridge Drive		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country i	US

Remove

Inventor 4

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Szuya	S.	LIAO	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Hillsboro	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	7214 NE Shaleen Street		
Address 2			
City	Hillsboro	State/Province	OR
Postal Code	97124	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	45209		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same		
Attorney Docket Number	P60397US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	45209		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	a 371 of international	PCT/US13/76673	2013-12-19

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Applicant:

Address 1	2200 Mission College Boulevard		
Address 2			
City	Santa Clara	**State/Province**	CA
Country	US	Postal Code	95054
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Justin K. Brask/			Date (YYYY-MM-DD)	
First Name	Justin K.	Last Name	Brask	Registration Number	61080

Additional Signature may be generated within this form by selecting the Add button.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	15/024,750
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (S U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	27063303
Application Number:	15024750
International Application Number:	
Confirmation Number:	9490
Title of Invention:	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same
First Named Inventor/Applicant Name:	Milton C. WEBB
Customer Number:	45209
Filer:	Justin K. Brask/Sheri Villarreal
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US
Receipt Date:	28-SEP-2016
Filing Date:	24-MAR-2016
Time Stamp:	18:07:05
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P60397US_IDS_9-28-16.pdf	105397 9375a833f922b3d2b24082c242b8afd797e5fe58	yes	2

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Foreign Reference	TW201017772A_w_abstract.pdf	2801941 bde5bdcdbdee14173b7f3ec7fda694fd480870a9	no	59
Warnings:					
Information:					
3	Other Reference-Patent/App/Search documents	42P60397PCT_IPRP_6-30-16.pdf	324846 811831af3786fd547217fabc25cd37917b91b74d	no	7
Warnings:					
Information:					
4	Non Patent Literature	P60397TW_OA_w_Search_Report_6-3-16.pdf	38261 bfb636abc116fa2f3ef7cbe9680d992ab44c7ff7	no	3
Warnings:					
Information:					
5	Application Data Sheet	P60397US_Updated_ADS_Filed_9-28-16.pdf	523143 ce44b4ae7a34a75b6b5dafff9f545996b8bcaa9d	no	9
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
		Total Files Size (in bytes):	3793588		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/024,750
Filing Date	March 24, 2016
First Inventor	Milton C. WEBB, et al.
Art Unit	2822
Examiner Name	Feeney, Brett A.
Attorney Docket No.	P60397US Conf. No. 9490

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	09-28-2016
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal */Sheri Villarreal/* *Date* *09-28-16*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/024,750	03/24/2016	Milton C. WEBB	P60397US

CONFIRMATION NO. 9490

45209
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

PUBLICATION NOTICE

OC000000085025377

Title: Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same

Publication No.US-2016-0233298-A1
Publication Date:08/11/2016

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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U.S. APPLICATION NUMBER NO.	FIRST NAMED INVENTOR	ATTY. DOCKET NO.
15/024,750	Milton C. WEBB	P60397US

45209
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

INTERNATIONAL APPLICATION NO.	
PCT/US2013/076673	
I.A. FILING DATE	PRIORITY DATE
12/19/2013	

CONFIRMATION NO. 9490
371 ACCEPTANCE LETTER

OC00000082677243

Date Mailed: 05/05/2016

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office, in its capacity as a Designated / Elected Office (37 CFR 1.495), has ACCEPTED the above identified international application for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above. A Filing Receipt will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE "FILING DATE or 371(c) DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1) and (c)(2) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN BELOW.** The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363)

03/24/2016
DATE OF RECEIPT OF 35 U.S.C.
371(c)(1) and (c)(2) REQUIREMENTS

The following items have been received:

- Copy of the International Application filed on 03/24/2016
- Copy of the International Search Report filed on 03/24/2016
- Preliminary Amendments filed on 03/24/2016
- Information Disclosure Statements filed on 03/24/2016
- Inventor's Oath or Declaration filed on 03/24/2016
- Request for Immediate Examination filed on 03/24/2016
- U.S. Basic National Fees filed on 03/24/2016
- Authorize Access to Search Results filed on 03/24/2016
- Authorization to Permit Access filed on 03/24/2016
- Application Data Sheet (37 CFR 1.76) filed on 03/24/2016

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.495(c).

- The name of the inventor set forth in the inventor's oath or declaration does not correspond to the name of the inventor as established under 37 CFR 1.41(e) or corrected under 37 CFR 1.48 for the inventor listed below.

FORM PCT/DO/EO/903 (371 Acceptance Notice)

Any request to correct or update the name of an inventor must be made in accordance with the provisions of 37 CFR 1.48(f) and include an ADS in accordance with 37 CFR 1.76 (including markings showing the changes) that identifies each inventor by his or her legal name and the required processing fee: **Milton C. WEBB**.

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

MARY-ANN R FOSTER

Telephone: (703) 756-1122

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/024,750	03/24/2016		2440	P60397US	25	4

CONFIRMATION NO. 9490

45209
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
c/o CPA Global
900 2nd Avenue South, Suite 600
Minneapolis, MN 55402

FILING RECEIPT



Date Mailed: 05/05/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Milton C. WEBB, Aloha, OR;
Mark BOHR, Aloha, OR;
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Szuya S. LIAO, Hillsboro, OR;

Applicant(s)

INTEL CORPORATION, Santa Clara, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US2013/076673 12/19/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/04/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/024,750**

Projected Publication Date: 08/11/2016

Non-Publication Request: No

Early Publication Request: No
Title

Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/024,750

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	480
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	25 minus 20 =	* 5			OR	x 80 =	400
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1				x 420 =	420
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2300

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

Substitute for Form PTO-1360
(For use with Form PTO/SB/06)

Application Number	Filing Date
15024750	

Applicant(s) Milton WEBB

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT	
	Indep	Depend	Indep	Depend	Indep	Depend
1	1					
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Total Indep	4		0		0	
Total Depend	21	↵	0	↵	0	↵
Total Claims	25		0		0	

	*		*		*	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	WEBB, Milton C., et al.	Confirmation No.:	Not Yet Assigned
Serial No.:	Not Yet Assigned U.S. National Phase Filing of PCT/US13/076673 under U.S.C. § 371	Art Unit:	Not Yet Assigned
Filed:	Herewith		
For:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME		
Docket No.:	P60397US		

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Applicant respectfully requests that the following Preliminary Amendment be entered prior to examination of the above-identified patent application. The Examiner is requested to enter this amendment before calculating the fee.

Amendments to the Specification begin on page 2 of this paper.
Conclusion begins on page 3 of this paper.

I hereby certify that this correspondence is being deposited via EFS Web on the date below:
March 24, 2016
Date of Deposit

/Robert S. Caldwell/
Robert S. Caldwell

AMENDMENTS TO THE SPECIFICATION

At page 1, line 2, add the following:

CLAIM OF PRIORITY

[**0001**] This application is a U.S. National Phase application under 35 U.S.C. § 371 of International Application No. PCT/US13/076673, filed December 19, 2013, entitled "SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME" the entire contents of which are incorporated herein by reference.

Applicants respectfully submit that no new matter has been entered, and the amendments correct and clarify the previously submitted claim of priority.

CONCLUSION

The Commissioner is authorized to charge or credit any deficiencies or overpayments in connection with this submission to Deposit Account No. 504238, and is requested to notify us of same.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

March 24, 2016
Date

/Justin K. Brask/
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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
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25 June 2015 (25.06.2015)

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WO 2015/094305 A1

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H01L 21/336 (2006.01)

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19 December 2013 (19.12.2013)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard MS: RNB-4-150, Santa Clara, California 95054 (US).

(72) Inventors; and

(71) Applicants : **WEBB, Milton Clair** [US/US]; 20180 SW Inglis Drive, Aloha, Oregon 97007 (US). **BOHR, Mark** [US/US]; 19475 SW Suncrest Lane, Aloha, Oregon 97007 (US). **GHANI, Tahir** [US/US]; 14191 NW Stonebridge Drive, Portland, Oregon 97229 (US). **LIAO, Szuya S.** [—/US]; 7214 NE Shaleen St., Hillsboro, Oregon 97124 (US).

(74) Agents: **BRASK, Justin K.** et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 1279 Oakmead Parkway, Sunnyvale, California 94085-4040 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

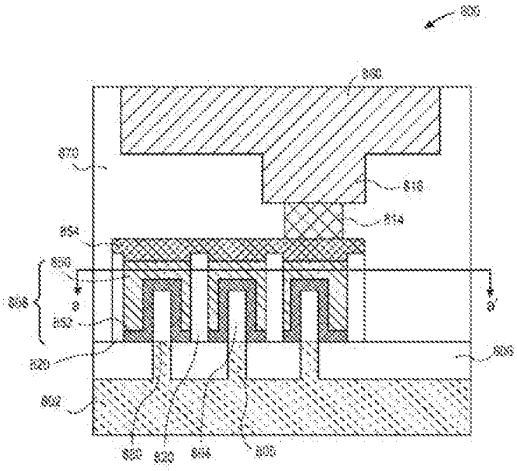


FIG. 8A

(57) Abstract: Self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures are described. In an example, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length in a first direction. A gate structure is disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction. A pair of gate edge isolation structures is centered with the semiconductor fin. A first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

WO 2015/094305 A1

Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same

TECHNICAL FIELD

[0001] Embodiments of the invention are in the field of semiconductor devices and processing and, in particular, self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures.

BACKGROUND

[0002] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

[0003] In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes, tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and because they enable a less complicated tri-gate fabrication process.

[0004] Scaling multi-gate transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of fundamental building blocks fabricated in a given region is increased, the constraints on the lithographic processes used to pattern these building blocks have become overwhelming. In particular, there may be a trade-off between the smallest dimension of a feature patterned in a semiconductor stack (the critical dimension) and the spacing between such features.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 illustrates a plan view of a layout including fin-based semiconductor devices accommodating end-to-end spacing.

[0006] Figures 2A-2D illustrate cross-sectional views of process operations of significance in a conventional finFET or tri-gate process fabrication scheme.

[0007] Figures 3A-3D illustrate cross-sectional views of process operations of significance in a self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with an embodiment of the present invention.

[0008] Figures 4A-4G illustrate cross-sectional views and corresponding top views of process operations in another self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with another embodiment of the present invention.

[0009] Figure 5A illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a pitch division patterned local interconnect (LI), in accordance with one embodiment of the present invention.

[0010] Figure 5B illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a self-aligned local interconnect (SAGELI), in accordance with another embodiment of the present invention.

[0011] Figures 6A-6H illustrate angled, three-dimensional cross-sectional views of various operations in the fabrication of self-aligned gate endcaps, in accordance with an embodiment of the present invention.

[0012] Figures 7A-7D illustrate angled, three-dimensional cross-sectional views of various structural options for providing a foundation for local interconnect fabrication, in accordance with an embodiment of the present invention.

[0013] Figure 8A illustrates a cross-sectional view of a non-planar semiconductor device having self-aligned gate edge isolation, in accordance with an embodiment of the present invention.

[0014] Figure 8B illustrates a plan view taken along the a-a' axis of the semiconductor device of Figure 8A, in accordance with an embodiment of the present invention.

[0015] Figure 9 illustrates a computing device in accordance with one implementation of the invention.

DESCRIPTION OF THE EMBODIMENTS

[0016] Self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0017] One or more embodiments of the present invention are directed to semiconductor structures or devices having one or more gate edge structures (e.g., as gate isolation regions) of gate electrodes of the semiconductor structures or devices. One or more embodiments are directed to the fabrication of local interconnects for such gate electrode structures. Additionally, methods of fabricating gate edge isolation structures in a self-aligned manner and/or methods of fabricating local interconnects are also described. In one or more embodiments, self-aligned gate edge structures and/or local interconnects are fabricated for logic transistors based on complementary metal oxide semiconductor (CMOS) devices.

[0018] To provide context, scaling of gate endcap and trench contact (TCN) endcap regions are important contributors towards improving transistor layout area and density. Gate and TCN endcap regions refer to gate and TCN overlap of the

diffusion region/fins of semiconductor devices. As an example, Figure 1 illustrates a plan view of a layout 100 including fin-based semiconductor devices accommodating end-to-end spacing. Referring to Figure 1, first 102 and second 104 semiconductor devices are based on semiconductor fins 106 and 108, respectively. Each device 102 and 104 has a gate electrode 110 or 112, respectively. Additionally, each device 102 and 104 has trench contacts (TCNs) 114 and 116, respectively, at source and drain regions of the fins 106 and 108, respectively. The gate electrodes 110 and 112 and the TCNs 114 and 116 each have an end cap region, which is located off of the corresponding fins 106 and 108, respectively.

[0019] Referring again to Figure 1, typically, gate and TCN endcap dimensions must include an allowance for mask registration error to ensure robust transistor operation for worst case mask mis-registration, leaving an end-to-end spacing 118. Thus, another important design rule critical to improving transistor layout density is the spacing between two adjacent endcaps facing each other. However, the parameters of *"2*Endcap + End-to-End Spacing"* are becoming increasingly difficult to scale using lithographic patterning to meet the scaling requirements for new technologies. In particular, the additional endcap length required to allow for mask registration error also increases gate capacitance values due to longer overlap length between TCN and gate electrodes, thereby increasing product dynamic energy consumption and degrading performance. Previous solutions have focused on improving registration budget and patterning or resolution improvements to enable shrinkage of both endcap dimension and endcap-to-endcap spacing.

[0020] In accordance with an embodiment of the present invention, approaches are described which provide for self-aligned gate endcap and TCN overlap of a semiconductor fin without any need to allow for mask registration. In one such embodiment, a disposable spacer is fabricated on the semiconductor fin edges which determines the gate endcap and the contact overlap dimensions. The spacer defined endcap process enables the gate and TCN endcap regions to be self-aligned to the semiconductor fin and, therefore, does not require extra endcap length to account for mask mis-registration. Furthermore, approaches described herein do not require lithographic patterning at previously required stages since the gate and TCN endcap/overlap dimensions remain fixed, leading to improvement (i.e., reduction) in device to device variability in electrical parameters.

[0021] In order to provide a side-by-side comparison, Figures 2A-2D illustrate cross-sectional views of process operations of significance in a conventional finFET or tri-gate process fabrication scheme, while Figures 3A-3D illustrate cross-sectional views of process operations of significance in a self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with an embodiment of the present invention.

[0022] Referring to Figures 2A and 3A, a bulk semiconductor substrate 200 or 300, such as a bulk single crystalline silicon substrate is provided having fins 202 or 302, respectively, etched therein. In an embodiment, the fins are formed directly in the bulk substrate 200 or 300 and, as such, are formed continuous with the bulk substrate 200 or 300. It is to be appreciated that within the substrate 200 or 300, shallow trench isolation structures may be formed between fins. Referring to Figure 3A, a hardmask layer 304, such as a silicon nitride hardmask layer, and a pad oxide

layer 306, such as a silicon dioxide layer, remain atop fins 302 following patterning to form the fins 302. By contrast, referring to Figure 2A, such a hardmask layer and pad oxide layer have been removed.

[0023] Referring to Figure 2B, a dummy or permanent gate dielectric layer 210 is formed on the exposed surfaces of the semiconductor fins 202, and a dummy gate layer 212 is formed over the resulting structure. By contrast, referring to Figure 3B, a dummy or permanent gate dielectric layer 310 is formed on the exposed surfaces of the semiconductor fins 302, and dummy spacers 312 are formed adjacent to the resulting structure.

[0024] Referring to Figure 2C, gate endcap cut patterning is performed and isolation regions 214 are formed at the resulting patterned dummy gate ends 216. In the conventional process scheme, a larger gate endcap must be fabricated to allow for gate mask mis-registration, as depicted by the arrowed regions 218. By contrast, referring to Figure 3C, self-aligned isolation regions 314 are formed by providing an isolation layer over the structure of Figure 3B, e.g., by deposition and planarization. In one such embodiment, the self-aligned gate endcap process does not require extra space for mask registration, as compared in Figures 2C and 3C.

[0025] Referring to Figure 2D, the dummy gate electrode 212 of Figure 2C is replaced with permanent gate electrodes. In the case of use of a dummy gate dielectric layer, such a dummy gate dielectric layer may also be replaced by a permanent gate dielectric layer in this process. In the specific example shown, a dual metal gate replacement process is performed to provide an N-type gate electrode 220 over a first semiconductor fin 202A and to provide a P-type gate electrode 222 over a second semiconductor fin 202B. The N-type gate electrode 220

and the P-type gate electrode 222 are formed between the gate edge isolations structures 214, but form a P/N junction 224 where they meet. The exact location of the P/N junction 224 may vary, depending on mis-registration, as depicted by the arrowed region 226.

[0026] By contrast, referring to Figure 3D, the hardmask layer 304 and pad oxide layer 306 are removed, and the dummy spacers 314 of Figure 3C are replaced with permanent gate electrodes. In the case of use of a dummy gate dielectric layer, such a dummy gate dielectric layer may also be replaced by a permanent gate dielectric layer in this process. In the specific example shown, a dual metal gate replacement process is performed to provide an N-type gate electrode 320 over a first semiconductor fin 302A and to provide a P-type gate electrode 322 over a second semiconductor fin 302B. The N-type gate electrode 320 and the P-type gate electrode 322 are formed between, and are also separated by, the gate edge isolations structures 314.

[0027] Referring again to Figure 2D, a local interconnect 240 may be fabricated to contact N-type gate electrode 220 and P-type gate electrode 322 to provide a conductive path around the P/N junction 224. Likewise, referring to Figure 3D, a local interconnect 340 may be fabricated to contact N-type gate electrode 320 and P-type gate electrode 322 to provide a conductive path over the intervening isolation structure 314 there between. Referring to both Figures 2D and 3D, a hardmask 242 or 342 may be formed on the local interconnect 240 or 340, respectively.

[0028] In another aspect, a hardmask and pad oxide layer may not be retained atop patterned find throughout a dummy spacer and self-aligned gate edge

isolations structure fabrication process. As such, the height of the semiconductor fins relative to the height of the dummy spacers may need to be differentiated in another way. As an example, Figures 4A-4G illustrate cross-sectional views and corresponding top views of process operations in another self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with another embodiment of the present invention.

[0029] Referring to Figure 4A, a bulk semiconductor substrate 400, such as a bulk single crystalline silicon substrate, is provided having fins 402 etched therein. In an embodiment, the fins 402 are formed directly in the bulk substrate 400 and, as such, are formed continuous with the bulk substrate 400. It is to be appreciated that within the substrate 400, shallow trench isolation structures may be formed between fins. In one embodiment, artifacts from patterning the fins 402, such as a hardmask layer and a pad oxide layer, have been removed, as is depicted in Figure 4A.

[0030] Referring to Figure 4B, dummy spacers 404 are formed along the sidewalls of the fins 402. In an embodiment, the dummy spacers 404 are formed by a deposition and etch process that ultimately exposes the top surface of the fins 402. It is to be appreciated that the fins 402 may be passivated, e.g., by deposition or growth of a dummy gate dielectric layer, prior to the formation of the dummy spacers 404. In one embodiment, the fins 402 are silicon fins passivated with a silicon dioxide layer, and the dummy spacers are fabricated from silicon nitride or like material. In another embodiment, however the fins 402 are not passivated at this stage.

[0031] Referring to Figure 4C, isolations structures 406 are formed in the open regions of the structure of Figure 4B. In an embodiment, the isolation regions

406 are formed by deposition and subsequent planarization (e.g., by chemical mechanical polishing) of a dielectric film over the structure of Figure 4B. In a particular embodiment, the isolation structures are composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0032] Referring to Figure 4D, the fins 402 are recessed relative to the height of the isolation structures 406 and relative to the height of the dummy spacers 404. In an embodiment, the recessing is performed by using a selective etch process. In one such embodiment, a passivation layer first formed on fins 402 is removed prior to or during the recessing of the fins 402.

[0033] Referring to Figure 4E, the dummy spacers 404 are removed from the structure of Figure 4D. In an embodiment, the removal is performed by using a selective etch process. In one such embodiment, the isolation structures 406 are composed of silicon oxide, the fins 402 are composed of silicon, and the selectively removed dummy spacers are composed of silicon nitride.

[0034] Referring to Figure 4F, a gate electrode stack 408 is formed in the locations from which dummy spacers 404 were removed and along the top surfaces of the recessed fins 402. In an embodiment, the gate electrode stack 408 includes a conformal gate dielectric layer 410, such as a high-k gate dielectric layer, and a metal gate electrode 412. The cross-sectional view of Figure 4F is taken along the a-a' axis of the top view of Figure 4F. It is to be understood, however, that the top view is taken somewhat deeper into the structure in order to show the whole fins 402. In actuality, the metal gate material 412 would cover the fins 402 in the top view.

[0035] Referring to Figure 4G, trench contacts 414 are formed adjacent to the gate electrode stacks 408 and along the top surfaces of the recessed fins 402. In an embodiment, the trench contacts 414 are for contacting source and drain regions within the fins 402, and are separated from the gate electrode stacks 408 by dielectric spacers 416. The cross-sectional view of Figure 4G is taken along the b-b' axis of the top view of Figure 4G. It is to be understood, however, that the top view is taken somewhat deeper into the structure in order to show the whole fins 402. In actuality, the trench contacts 414 would cover the fins 402 in the top view.

[0036] In another aspect, referring again to Figure 3D, in an embodiment, one or more of the above approaches requires an additional local interconnect layer (LI) above gate and trench contact (TCN) to connect adjacent gates and TCN electrodes. In one such embodiment, such a local interconnect must overlap gate and TCN, without creating contact to gate (CTG) shorting. As such, fabrication of the local interconnect can require patterning of lines at 1/2 of gate pitch with good CTG short margin, while maintaining robust LI to TCN contact. Hence, the alignment between LI and gate or TCN is another difficult patterning problem. As such, in accordance with an embodiment of the present invention, in order to address the above concern, a fabrication scheme for local interconnect lines which are self-aligned to gate and TCN without any need to allow for mask registration is provided. The approach involves fabrication of a spacer along a taller stack that includes a dummy gate and hardmask and which extends above the self-aligned gate endcap. In one such embodiment, the spacers serve as continuous self-aligned walls separating gate and contact. Two additional dielectric materials with contrasting

etch properties may be used as hardmasks to allow for selectively opening an area for gate-LI (LIG) and TCN-LI (LIT).

[0037] As an example, Figure 5A illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a pitch division patterned local interconnect (LI), in accordance with one embodiment of the present invention. By contrast, Figure 5B illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a self-aligned local interconnect (SAGELI), in accordance with another embodiment of the present invention.

[0038] Referring to Figure 5A, a semiconductor device 500A includes a semiconductor fin 502. A plurality of short self-aligned isolation structures 504 separate alternating gate 506 and trench contact 508 regions. Upper isolation structures 510 separate alternating trench contact local interconnects 512 and gate local interconnects 514. The trench contact local interconnects 512 and gate local interconnects 514 are formed by pitch division patterning to accommodate for mis-registration, as is shown in Figure 5A. It is to be appreciated that dielectric caps may be formed on the trench contact local interconnects 512 and gate local interconnects 514, as is also depicted in Figure 5A.

[0039] Referring to Figure 5B, a semiconductor device 500B includes a semiconductor fin 552. A plurality of tall self-aligned isolation structures 554 separate alternating gate 556 and trench contact 558 regions. The same isolation structures 554 also separate alternating trench contact local interconnects 562 and gate local interconnects 564. The trench contact local interconnects 512 and gate local interconnects 514 are formed without using an additional lithography operation

as was need for the case of Figure 5A. It is to be appreciated that dielectric caps may be formed on the trench contact local interconnects 562 and gate local interconnects 564, as is depicted in Figure 5B. It is also to be appreciated that the trench contact local interconnects 512 and gate local interconnects 514 are, in an embodiment, fabricated at different times, the process for forming each taking advantage of the use of plugs/hardmask layers as placeholders prior to replacement with the actual permanent materials of the trench contact local interconnects 512 and gate local interconnects 514. Furthermore, although all locations in Figure 5B are shown as having a gate local interconnect or trench contact local interconnect, not all locations need be selected for local interconnection. In locations not selected a dielectric plug or hardmask may remain (i.e., it is not selected for removal at certain locations).

[0040] As exemplary approaches, Figures 6A-6H illustrate angled, three-dimensional cross-sectional views of various operations in the fabrication of self-aligned gate endcaps, in accordance with an embodiment of the present invention. Figures 7A-7D illustrate angled, three-dimensional cross-sectional views of various structural options for providing a foundation for local interconnect fabrication, in accordance with an embodiment of the present invention.

[0041] Referring to Figure 6A, a plurality of semiconductor fins 602 is formed by patterning a substrate 600, such as a single crystalline silicon substrate, and the patterning may involve pitch halving or pitch quartering patterning. Furthermore, a passivation layer 604, a dummy gate layer 606 (such as a polycrystalline silicon layer), and a hardmask layer 608 are patterned during the fin 602 patterning.

[0042] Referring to Figure 6B, a shallow trench isolation (STI) layer 610 is formed over the structure of Figure 6A. In an embodiment, the STI layer 610 includes a silicon dioxide layer and is formed by chemical vapor deposition (CVD) and subsequent chemical mechanical planarization (CMP). In one embodiment, the STI structure includes a liner dielectric layer 612, as shown in Figure 6B.

[0043] Referring to Figure 6C, the STI layer 610 of Figure 6B is recessed to form an STI structure 614 (which may include a liner dielectric layer) and a dummy gate dielectric layer 616 is formed on the resulting structure. In one such embodiment, the dummy gate dielectric layer 616 is formed by deposition and is further deposited on the STI structure 614, as depicted. Furthermore, hardmask layer 608 may be removed, as is also depicted.

[0044] Referring to Figure 6D, spacers 618 are formed along the sidewalls of the protruding portions of the structure of Figure 6C. In an embodiment, the spacers 618 are formed by a deposition and subsequent anisotropic etch process. In one such embodiment, the spacers are composed of deposited polycrystalline silicon. Depending on the spacing between certain of the fins 602, some spacers 618 are discrete from all other spacers, while some spacers are continuous with another spacer. As an example, the portion 620A has discrete spacers 618A, while the portion 620B includes a pair of continuous spacers 618B. Thus, referring collectively to Figures 6A-6D, a finFET "hat" and dummy gate poly are patterned with a standard pitch division fin patterning process and a spacer is created on both sides of the patterned fin-poly pillars.

[0045] Referring to Figure 6E, the gaps between the spacers 618 of Figure 6D are filled with a dielectric material layer 622 to create transistor isolations. In an embodiment, the dielectric material is composed of a silicon nitride material.

[0046] Referring to Figure 6F, the dielectric material layer 622 is planarized (e.g., by CMP) to expose the dummy gate layer 606 and the corresponding spacers 618. In an embodiment, both the dummy gate layer 606 and the corresponding spacers 618 are composed of polycrystalline silicon. The process forms self-aligned end cap isolation walls 624.

[0047] Referring to Figure 6G, a second dummy layer and hardmask stack or a tall hardmask only are/is deposited and patterned using pitch division gate patterning (both cases shown as item 626 in Figure 6G) on the structure of Figure 6H. In an embodiment, in the case that a dummy layer and hardmask stack is used, the dummy layer is composed of polycrystalline silicon.

[0048] Referring to Figure 6H, an anisotropic etch selective to hardmask layer 626, isolation walls 624 and finFET "hat" 616 (e.g., remaining from the dummy gate dielectric layer) is performed to provide a straight profile between patterned lines and resulting endcap isolation cages 628. Although not shown, following gate spacer formation, N-type or P-type source drain formation, and gate electrode replacement (e.g., with high-k/metal gate), a conductive material can be formed in the endcap isolation cages 628 to provide trench contacts. And, in cases where the isolation walls are of sufficient height, self-aligned local interconnect lines may be fabricated, examples of which are described below in association with Figures 7C and 7D.

[0049] To provide an initial comparison, Figure 7A illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700A without self-aligned gate edge isolation. Referring to Figure 7A, a plurality of fins 702A has a dummy gate layer 704A and corresponding hardmask 706A patterned thereon. In the subsequent fabrication of local interconnects, a pitch divisional patterning scheme would have to be employed.

[0050] Figure 7B illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700B having self-aligned gate edge isolation. Referring to Figure 7B, a plurality of fins 702B has a dummy gate layer 704B and corresponding hardmask 706B patterned thereon. Self-aligned gate edge isolation structures 708B are formed between various groupings of the fins 702B. However, the hardmask 706B is relatively short compared with the self-aligned gate edge isolation structures 708B. As such, in the subsequent fabrication of local interconnects, a pitch divisional patterning scheme would have to be employed.

[0051] Figure 7C illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700C having self-aligned gate edge isolation. Referring to Figure 7C, a plurality of fins 702C has a dummy gate layer 704C, corresponding second dummy layer 705C, and corresponding hardmask 706C patterned thereon. Self-aligned gate edge isolation structures 708C are formed between various groupings of the fins 702C. The height of the hardmask 706C together with the second dummy layer 705C is relatively tall compared with the self-aligned gate edge isolation structures 708C. As such, in the subsequent fabrication of local interconnects, a self-aligned local interconnect scheme may be employed.

[0052] Figure 7D illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700D having self-aligned gate edge isolation. Referring to Figure 7D, a plurality of fins 702D has a dummy gate layer 704D and a corresponding tall hardmask 706D patterned thereon. Self-aligned gate edge isolation structures 708D are formed between various groupings of the fins 702D. The height of the tall hardmask 706D is relatively tall compared with the self-aligned gate edge isolation structures 708D. As such, in the subsequent fabrication of local interconnects, a self-aligned local interconnect scheme may be employed.

[0053] More generally, one or more embodiments described herein provide an avenue for area scaling, reducing capacitance, and/or eliminating various critical front end masks, such as gate cut masks. In one such embodiment the width of a minimum transistor can be reduced by up to 30% by implementing one or more of the approaches describe herein. The smaller transistor size reduces the capacitance between the gate and TCN and other parasitic capacitances. No extra mask steps are needed to create the endcaps, contacts and local interconnect lines so the many masks needed for such features in the standard process are eliminated.

[0054] More specifically, key features of one or more embodiments described above may include one or more of: (1) the gate endcap is the distance from the fin edge to the isolation edge. This distance is defined by the spacer width and is the same size for all transistors. No lithographic patterning is needed to define the endcap so there is no need to allow for mask registration in the endcap. (2) The TCN overlap of the fin is determined by the spacer width and is also not affected by mask registration. (3) The local interconnect lines are self-aligned to the gate and TCN by utilizing the gate patterning lines above the transistor isolation

walls to form three distinct hardmasks that can be selectively opened one at a time. Embodiments may be applicable to the 7nm node generation, e.g., to improve transistor layout density and gate capacitance (dynamic energy and performance improvement) and reduce total mask count.

[0001] It is to be appreciated that the structures resulting from the above exemplary processing schemes may be used in a same or similar form for subsequent processing operations to complete device fabrication, such as PMOS and NMOS device fabrication. As an example of a completed device, Figures 8A and 8B illustrate a cross-sectional view and a plan view (taken along the a-a' axis of the cross-sectional view), respectively, of a non-planar semiconductor device having self-aligned gate edge isolation, in accordance with an embodiment of the present invention, and as building on the structure described in association with Figure 3D.

[0002] Referring to Figure 8A, a semiconductor structure or device 800 includes a non-planar active regions (e.g., a fin structures including protruding fin portion 804 and sub-fin region 805) formed from substrate 802, and within isolation region 806. Gate structures 808 are disposed over the protruding portions 804 of the non-planar active regions as well as over a portion of the isolation region 806. As shown, gate structures 808 include a gate electrode 850 and a gate dielectric layer 852. In one embodiment, although not shown, gate structures 808 may also include a dielectric cap layer. Gate structures 808 are separated by self-aligned gate edge isolation structures 820. A local interconnect 854 coupled adjacent gate structures 808. A gate contact 814, and overlying gate contact via 816 are also seen from this perspective, along with an overlying metal interconnect 860, all of which are disposed in inter-layer dielectric stacks or layers 870. Also seen from the

perspective of Figure 8A, the gate contact 814 is, in one embodiment, disposed over the non-planar active regions. As is also depicted in Figure 8A, an interface 880 exists between a doping profile of protruding fin portions 804 and sub-fin regions 805, although other embodiments do not include such an interface in doping profile between these regions.

[0003] Referring to Figure 8B, the gate structures 808 are shown as disposed over the protruding fin portions 804, as isolated by self-aligned gate edge isolation structures 820. Source and drain regions 804A and 804B of the protruding fin portions 804 are shown in this perspective, although it is to be understood that these regions would be overlapped with trench contact structures. In one embodiment, the source and drain regions 804A and 804B are doped portions of original material of the protruding fin portions 804. In another embodiment, the material of the protruding fin portions 804 is removed and replaced with another semiconductor material, e.g., by epitaxial deposition. In either case, the source and drain regions 804A and 804B may extend below the height of dielectric layer 806, i.e., into the sub-fin region 805.

[0004] In an embodiment, the semiconductor structure or device 800 is a non-planar device such as, but not limited to, a finFET or a tri-gate device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate structures 808 surround at least a top surface and a pair of sidewalls of the three-dimensional body.

[0005] Substrate 802 may be composed of a semiconductor material that can withstand a manufactoring process and in which charge can migrate. In an

embodiment, substrate 802 is a bulk substrate composed of a crystalline silicon, silicon/germanium or germanium layer doped with a charge carrier, such as but not limited to phosphorus, arsenic, boron or a combination thereof, to form active region 804. In one embodiment, the concentration of silicon atoms in bulk substrate 802 is greater than 97%. In another embodiment, bulk substrate 802 is composed of an epitaxial layer grown atop a distinct crystalline substrate, e.g. a silicon epitaxial layer grown atop a boron-doped bulk silicon mono-crystalline substrate. Bulk substrate 802 may alternatively be composed of a group III-V material. In an embodiment, bulk substrate 802 is composed of a III-V material such as, but not limited to, gallium nitride, gallium phosphide, gallium arsenide, indium phosphide, indium antimonide, indium gallium arsenide, aluminum gallium arsenide, indium gallium phosphide, or a combination thereof. In one embodiment, bulk substrate 802 is composed of a III-V material and the charge-carrier dopant impurity atoms are ones such as, but not limited to, carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium.

[0006] Isolation region 806 may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, portions of a permanent gate structure from an underlying bulk substrate or isolate active regions formed within an underlying bulk substrate, such as isolating fin active regions. For example, in one embodiment, the isolation region 806 is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0007] Self-aligned gate edge isolation structures 820 may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of,

portions of permanent gate structures from one another. For example, in one embodiment, the isolation region 806 is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0008] Gate structures 808 may be composed of a gate electrode stack which includes a gate dielectric layer 852 and a gate electrode layer 850. In an embodiment, the gate electrode of the gate electrode stack is composed of a metal gate and the gate dielectric layer is composed of a high-K material. For example, in one embodiment, the gate dielectric layer is composed of a material such as, but not limited to, hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or a combination thereof. Furthermore, a portion of gate dielectric layer may include a layer of native oxide formed from the top few layers of the substrate 802. In an embodiment, the gate dielectric layer is composed of a top high-k portion and a lower portion composed of an oxide of a semiconductor material. In one embodiment, the gate dielectric layer is composed of a top portion of hafnium oxide and a bottom portion of silicon dioxide or silicon oxy-nitride.

[0009] In one embodiment, the gate electrode is composed of a metal layer such as, but not limited to, metal nitrides, metal carbides, metal silicides, metal aluminides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides. In a specific

embodiment, the gate electrode is composed of a non-workfunction-setting fill material formed above a metal workfunction-setting layer.

[0010] Spacers associated with the gate electrode stacks may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, a permanent gate structure from adjacent conductive contacts, such as self-aligned contacts. For example, in one embodiment, the spacers are composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0011] Local interconnect 854, gate contact 814, and overlying gate contact via 816 may be composed of a conductive material. In an embodiment, one or more of the contacts or vias are composed of a metal species. The metal species may be a pure metal, such as tungsten, nickel, or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., such as a silicide material). It is to be appreciated that a hardmask layer may be disposed on the local interconnect 854 in locations where gate contact 814 is not located thereon. Furthermore, the local interconnect 854 may be fabricated by lithographic patterning or, in other embodiments, may be fabricated as a self-aligned interconnect structure, as aligned with taller versions of the Self-aligned gate edge isolation structures 820.

[0012] In an embodiment (although not shown), providing structure 800 involves formation of a contact pattern which is essentially perfectly aligned to an existing gate pattern while eliminating the use of a lithographic step with exceedingly tight registration budget. In one such embodiment, this approach enables the use of intrinsically highly selective wet etching (e.g., versus conventionally implemented dry or plasma etching) to generate contact openings. In

an embodiment, a contact pattern is formed by utilizing an existing gate pattern in combination with a contact plug lithography operation. In one such embodiment, the approach enables elimination of the need for an otherwise critical lithography operation to generate a contact pattern, as used in conventional approaches. In an embodiment, a trench contact grid is not separately patterned, but is rather formed between poly (gate) lines. For example, in one such embodiment, a trench contact grid is formed subsequent to gate grating patterning but prior to gate grating cuts.

[0013] Furthermore, the gate structures 808 may be fabricated by a replacement gate process. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing. In an embodiment, dummy gates are removed by a dry etch or wet etch process. In one embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process including use of SF_6. In another embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a wet etch process including use of aqueous NH_4OH or tetramethylammonium hydroxide. In one embodiment, dummy gates are composed of silicon nitride and are removed with a wet etch including aqueous phosphoric acid.

[0014] In an embodiment, one or more approaches described herein contemplate essentially a dummy and replacement gate process in combination with a dummy and replacement contact process to arrive at structure 800. In one such embodiment, the replacement contact process is performed after the replacement

gate process to allow high temperature anneal of at least a portion of the permanent gate stack. For example, in a specific such embodiment, an anneal of at least a portion of the permanent gate structures, e.g., after a gate dielectric layer is formed, is performed at a temperature greater than approximately 600 degrees Celsius. The anneal is performed prior to formation of the permanent contacts.

[0015] Referring again to Figure 8A, in an embodiment, a semiconductor device has contact structures that contact portions of a gate electrode formed over an active region. In general, prior to (e.g., in addition to) forming a gate contact structure (such as a via) over an active portion of a gate and in a same layer as a trench contact via, one or more embodiments of the present invention include first using a gate aligned trench contact process. Such a process may be implemented to form trench contact structures for semiconductor structure fabrication, e.g., for integrated circuit fabrication. In an embodiment, a trench contact pattern is formed as aligned to an existing gate pattern. By contrast, conventional approaches typically involve an additional lithography process with tight registration of a lithographic contact pattern to an existing gate pattern in combination with selective contact etches. For example, a conventional process may include patterning of a poly (gate) grid with separate patterning of contact features.

[0016] Figure 9 illustrates a computing device 900 in accordance with one implementation of the invention. The computing device 900 houses a board 902. The board 902 may include a number of components, including but not limited to a processor 904 and at least one communication chip 906. The processor 904 is physically and electrically coupled to the board 902. In some implementations the at least one communication chip 906 is also physically and electrically coupled to the

board 902. In further implementations, the communication chip 906 is part of the processor 904.

[0017] Depending on its applications, computing device 900 may include other components that may or may not be physically and electrically coupled to the board 902. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0018] The communication chip 906 enables wireless communications for the transfer of data to and from the computing device 900. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 906 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device

900 may include a plurality of communication chips 906. For instance, a first communication chip 906 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 906 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0019] The processor 904 of the computing device 900 includes an integrated circuit die packaged within the processor 904. In some implementations of the invention, the integrated circuit die of the processor includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0020] The communication chip 906 also includes an integrated circuit die packaged within the communication chip 906. In accordance with another implementation of the invention, the integrated circuit die of the communication chip includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention.

[0021] In further implementations, another component housed within the computing device 900 may contain an integrated circuit die that includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention.

[0022] In various implementations, the computing device 900 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal

digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 900 may be any other electronic device that processes data.

[0023] Thus, embodiments of the present invention include self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures.

[0024] In an embodiment, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length in a first direction. A gate structure is disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction. A pair of gate edge isolation structures is centered with the semiconductor fin. A first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

[0025] In one embodiment, the semiconductor structure further includes source and drain regions disposed in the semiconductor fin, on either side of the gate structure. A first trench contact is disposed over the source region and a second trench contact disposed over the drain region. Each of the first and second trench contacts has a first end opposite a second end in the second direction. The first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the first trench contact and to the first end of the second trench contact. The

second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.

[0026] In one embodiment, the semiconductor structure further includes a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin. A second gate structure is disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction. The second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure. A third gate edge isolation structure is disposed directly adjacent to the second end of the second gate structure. The third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.

[0027] In one embodiment, the semiconductor structure further includes a local interconnect disposed above and electrically coupling the first and second gate structures.

[0028] In one embodiment, the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

[0029] In one embodiment, the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.

[0030] In one embodiment, the gate structure includes a high-k gate dielectric layer and a metal gate electrode.

[0031] In one embodiment, the pair of gate edge isolation structures is composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0032] In an embodiment, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length. Alternating source/drain and channel regions are disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin. The semiconductor structure also includes a plurality of gate edge isolation structures. An adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. A gate local interconnect is disposed above one of the gate structures and between a pair of the plurality of gate edge isolation structures.

[0033] In one embodiment, the semiconductor structure further includes a dielectric cap disposed on the gate local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

[0034] In one embodiment, the semiconductor structure further includes a trench contact local interconnect disposed above one of the trench contacts and between a second pair of the plurality of gate edge isolation structures.

[0035] In one embodiment, the semiconductor structure further includes a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the second pair of the plurality of gate edge isolation structures.

[0036] In one embodiment, each gate structure includes a high-k gate dielectric layer and a metal gate electrode.

[0037] In one embodiment, each of the plurality of gate edge isolation structures is composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0038] In an embodiment, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length. Alternating source/drain and channel regions are disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin. The semiconductor structure also includes a plurality of gate edge isolation structures. An adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. A trench contact local interconnect is disposed above one of the trench contacts and between a pair of the plurality of gate edge isolation structures.

[0039] In one embodiment, the semiconductor structure further includes a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

[0040] In one embodiment, each gate structure includes a high-k gate dielectric layer and a metal gate electrode.

[0041] In one embodiment, each of the plurality of gate edge isolation structures is composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0042] In an embodiment, a method of fabricating a semiconductor structure involves forming first and second parallel semiconductor fins above a substrate.

The method also involves forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins. The dummy spacers of the first semiconductor fin are non-continuous with the dummy spacers of the second semiconductor fin. The method also involves forming an isolation structure between the dummy spacers of the first and second semiconductor fins. The method also involves removing the dummy spacers. The method also involves forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure.

[0043] In one embodiment, the method also involves forming a first pair of trench contacts over the first semiconductor fin and a second pair of trench contacts over the second semiconductor fin. The first and pairs of trench contacts are directly adjacent to, and separated from one another by, the isolation structure.

[0044] In one embodiment, the method also involves, subsequent to forming an isolation structure and prior to removing the dummy spacers, recessing the first and second semiconductor fins.

[0045] In one embodiment, forming the dummy spacers involves forming and etching a polycrystalline silicon layer.

[0046] In one embodiment, forming the isolation structure involves depositing and planarizing a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0047] In one embodiment, forming one or both of the first and second replacement gate structures involves forming a high-k gate dielectric layer and a metal gate electrode.

[0048] In one embodiment, the method also involves forming a local interconnect above and electrically coupling the first and second replacement gate structures.

CLAIMS

What is claimed is:

1. A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length in a first direction;

a gate structure disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction; and

a pair of gate edge isolation structures centered with the semiconductor fin, wherein a first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

2. The semiconductor structure of claim 1, further comprising:

source and drain regions disposed in the semiconductor fin, on either side of the gate structure; and

a first trench contact disposed over the source region and a second trench contact disposed over the drain region, each of the first and second trench contacts having a first end opposite a second end in the second direction, wherein the first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the first trench contact and to the first end of the second trench contact, and the second of the pair of gate edge isolation structures is

disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.

3. The semiconductor structure of claim 1, further comprising:

a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin;

a second gate structure disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction, wherein the second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure; and

a third gate edge isolation structure disposed directly adjacent to the second end of the second gate structure, wherein the third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.

4. The semiconductor structure of claim 3, further comprising:

a local interconnect disposed above and electrically coupling the first and second gate structures.

5. The semiconductor structure of claim 4, wherein the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

6. The semiconductor structure of claim 3, wherein the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.

7. The semiconductor structure of claim 1, wherein the gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

8. The semiconductor structure of claim 1, wherein the pair of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

9. A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length;

alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and

a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and

a gate local interconnect disposed above one of the gate structures and between a pair of the plurality of gate edge isolation structures.

10. The semiconductor structure of claim 9, further comprising:

a dielectric cap disposed on the gate local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

11. The semiconductor structure of claim 9, further comprising:

a trench contact local interconnect disposed above one of the trench contacts and between a second pair of the plurality of gate edge isolation structures.

12. The semiconductor structure of claim 11, further comprising:

a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the second pair of the plurality of gate edge isolation structures.

13. The semiconductor structure of claim 9, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

14. The semiconductor structure of claim 9, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

15. A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length;

alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench

contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and

a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and

a trench contact local interconnect disposed above one of the trench contacts and between a pair of the plurality of gate edge isolation structures.

16. The semiconductor structure of claim 15, further comprising:

a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

17. The semiconductor structure of claim 15, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

18. The semiconductor structure of claim 15, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

19. A method of fabricating a semiconductor structure, the method comprising:

forming first and second parallel semiconductor fins above a substrate;

forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins, wherein the dummy spacers of the first semiconductor

fin are non-continuous with the dummy spacers of the second semiconductor fin;

forming an isolation structure between the dummy spacers of the first and second semiconductor fins;

removing the dummy spacers; and

forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure.

20. The method of claim 19, further comprising:

forming a first pair of trench contacts over the first semiconductor fin and a second pair of trench contacts over the second semiconductor fin, wherein the first and pairs of trench contacts are directly adjacent to, and separated from one another by, the isolation structure.

21. The method of claim 19, further comprising:

subsequent to forming an isolation structure and prior to removing the dummy spacers, recessing the first and second semiconductor fins.

22. The method of claim 19, wherein forming the dummy spacers comprises forming and etching a polycrystalline silicon layer.

23. The method of claim 19, wherein forming the isolation structure comprises depositing and planarizing a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

24. The method of claim 19, wherein forming one or both of the first and second replacement gate structures comprises forming a high-k gate dielectric layer and a metal gate electrode.

25. The method of claim 19, further comprising:

forming a local interconnect above and electrically coupling the first and second replacement gate structures.

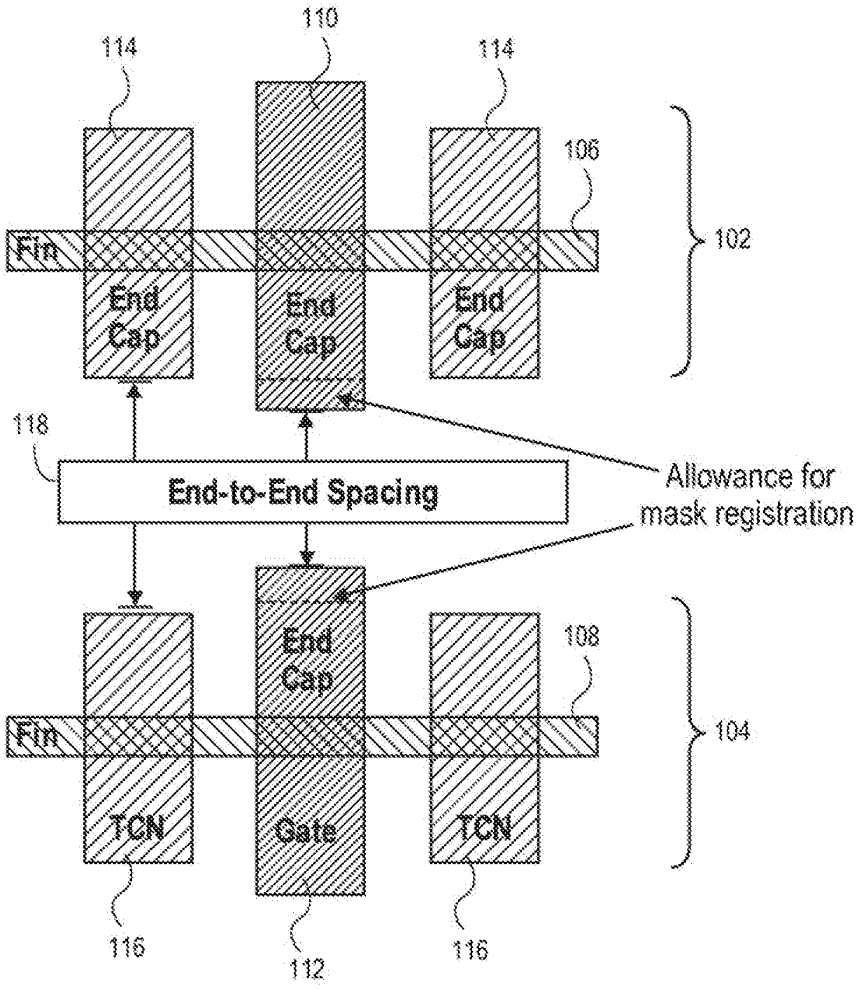

110
114
114
106
102
Fin
End Cap
End Cap
End Cap
118
End-to-End Spacing
Allowance for mask registration
End Cap
108
104
Fin
TCN
Gate
TCN
116
112
116

FIG. 1

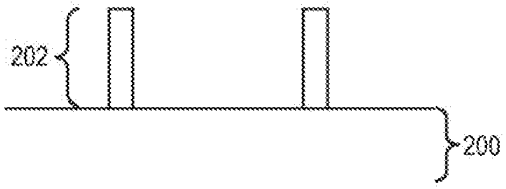


FIG. 2A

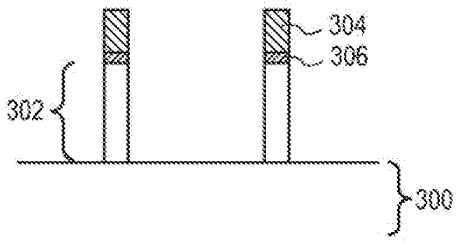


FIG. 3A

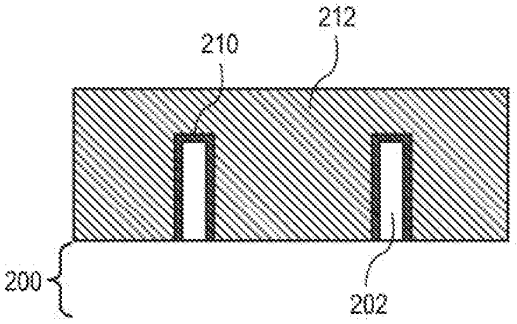


FIG. 2B

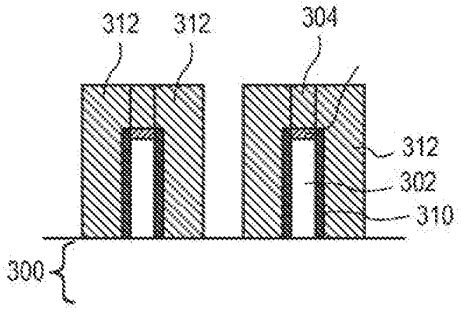


FIG. 3B

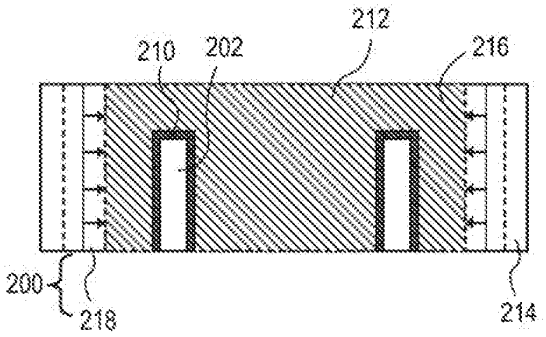


FIG. 2C

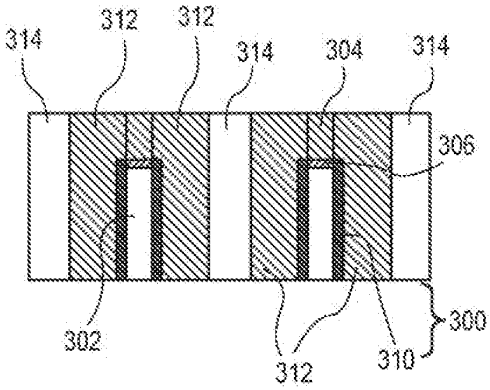


FIG. 3C

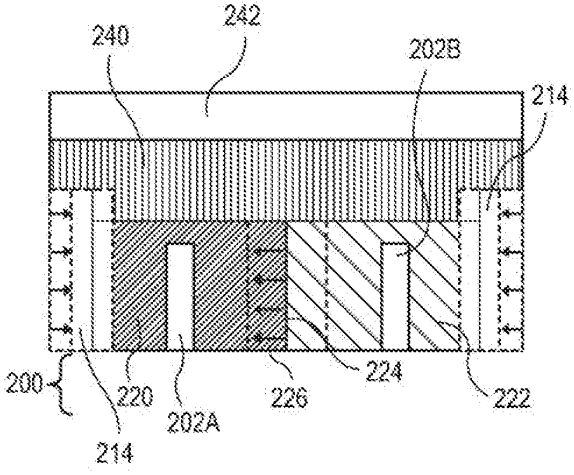


FIG. 2D

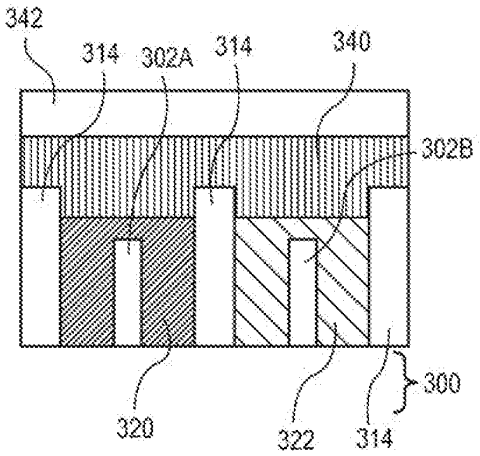


FIG. 3D

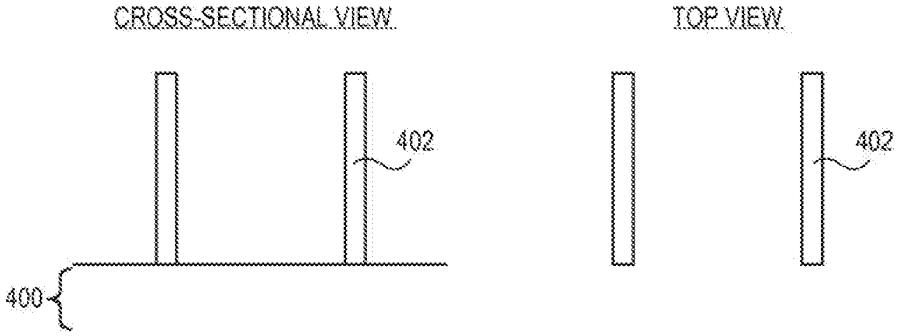


FIG. 4A

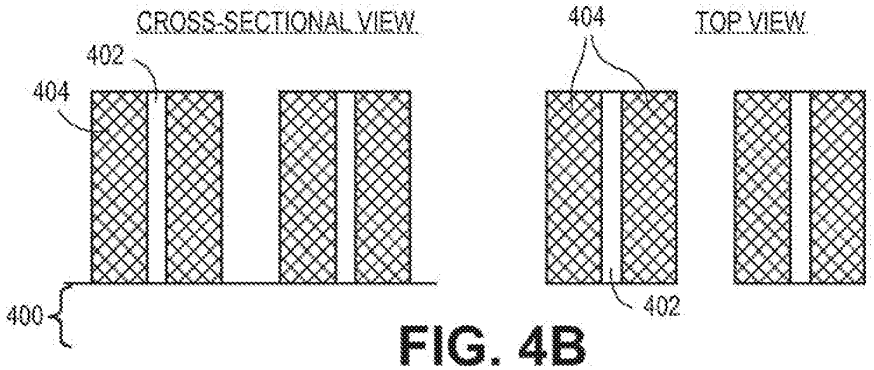


FIG. 4B

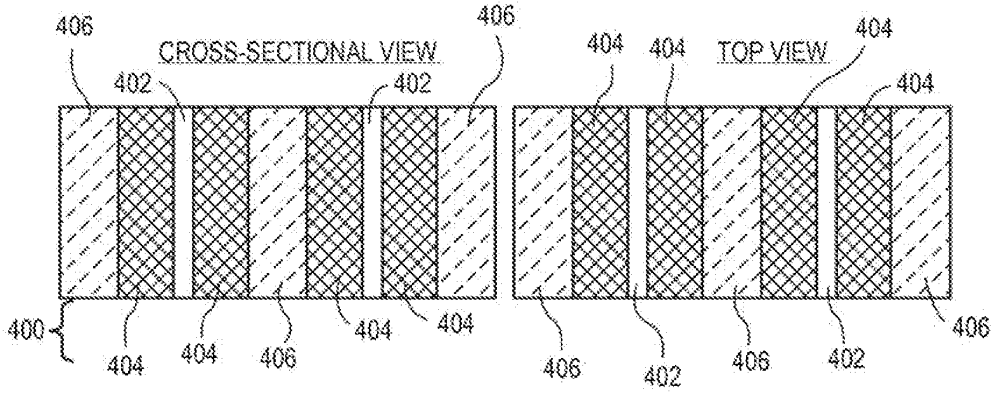


FIG. 4C

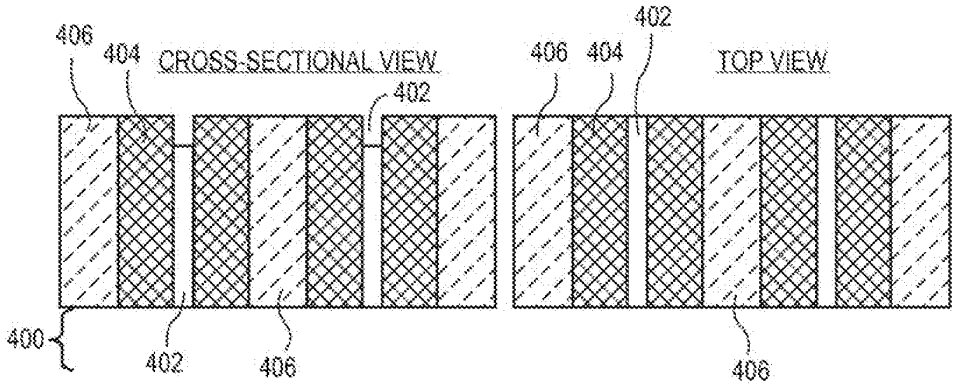


FIG. 4D

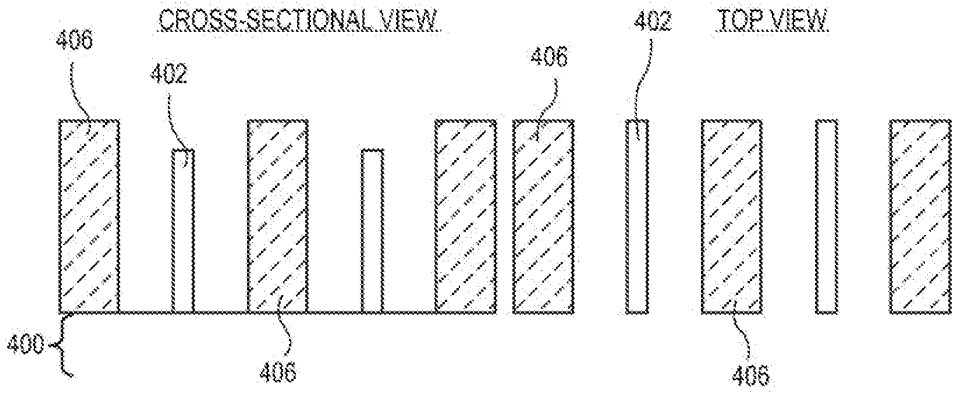


FIG. 4E

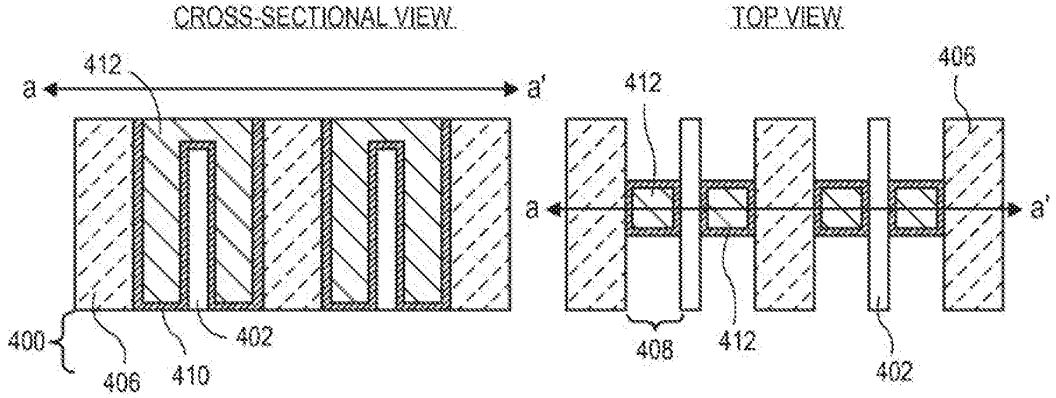


FIG. 4F

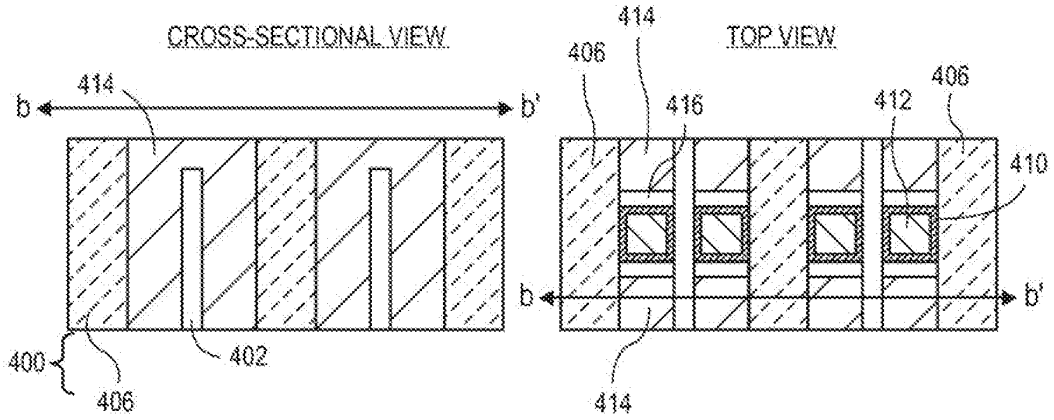


FIG. 4G

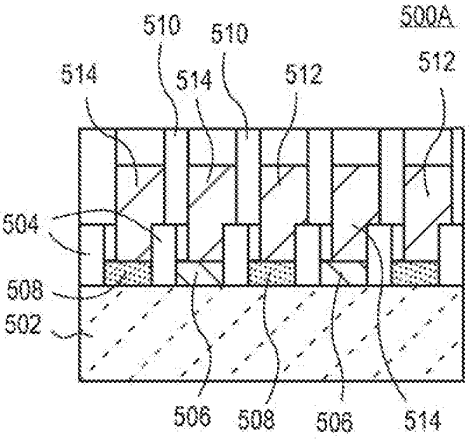


FIG. 5A

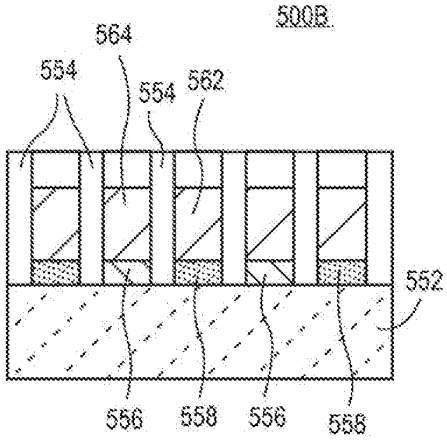


FIG. 5B

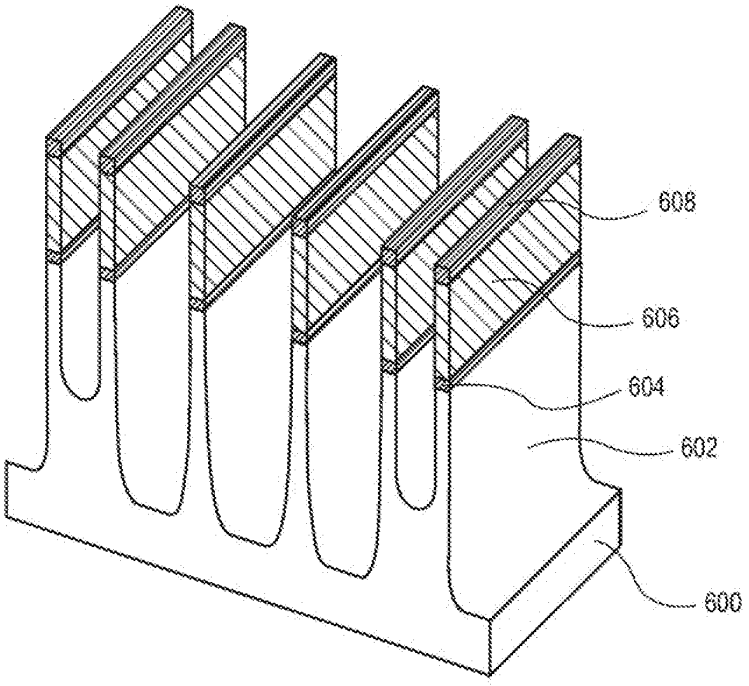


FIG. 6A

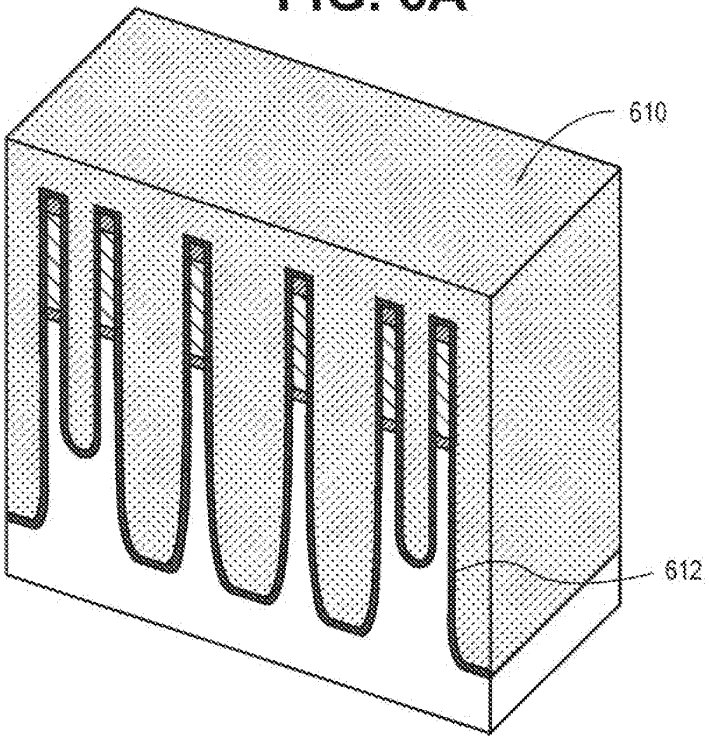


FIG. 6B

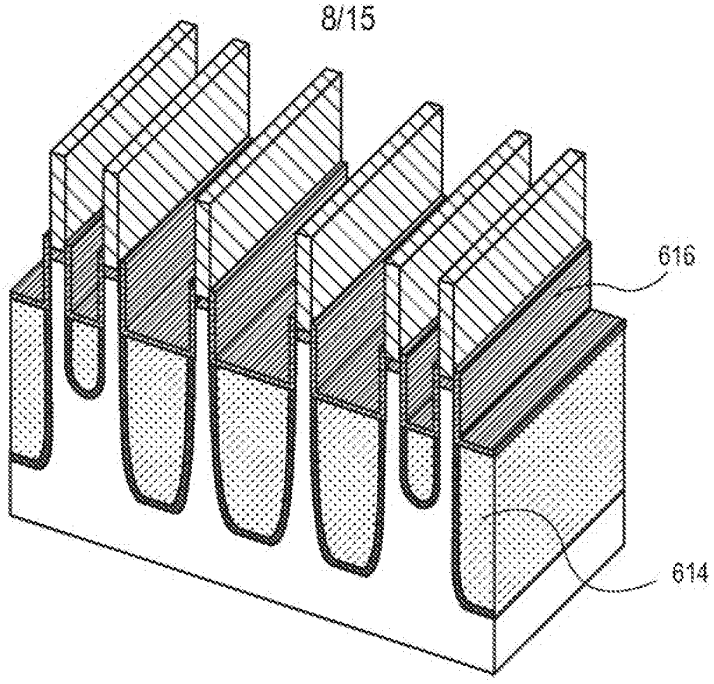


FIG. 6C

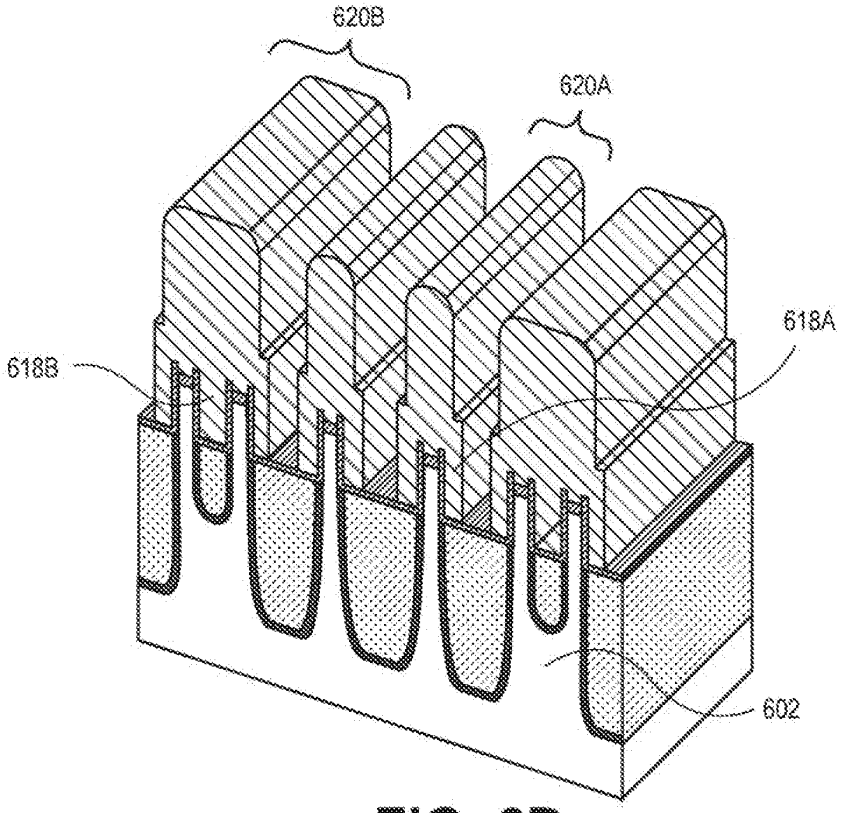


FIG. 6D

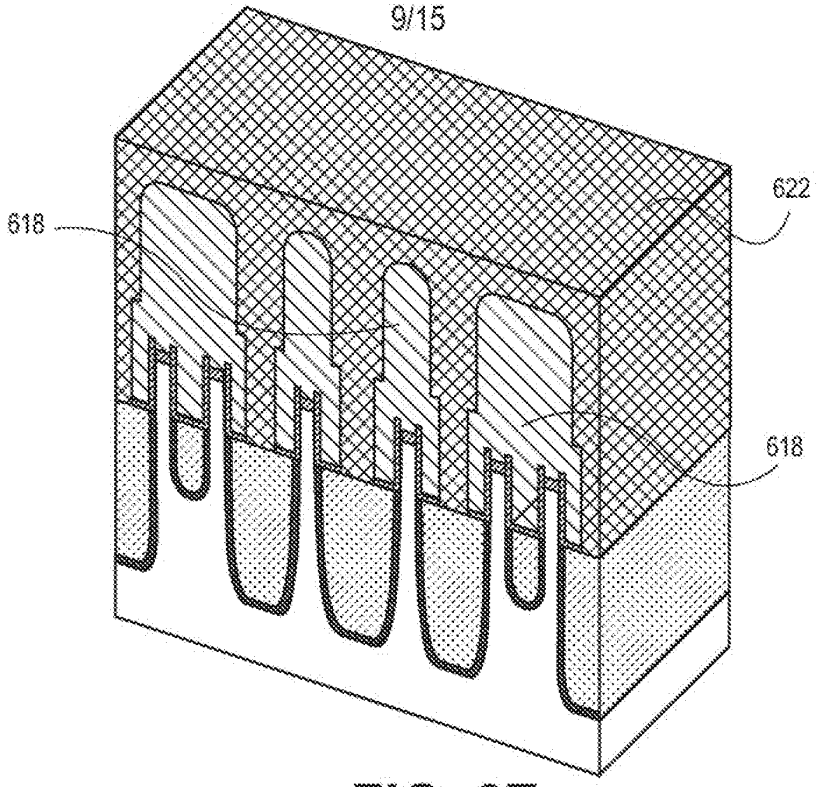


FIG. 6E

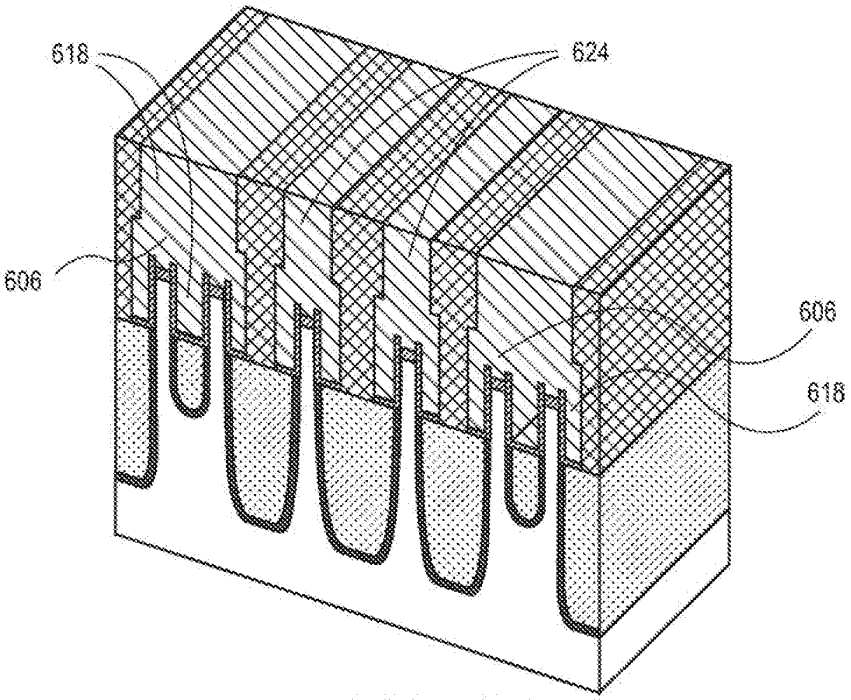


FIG. 6F

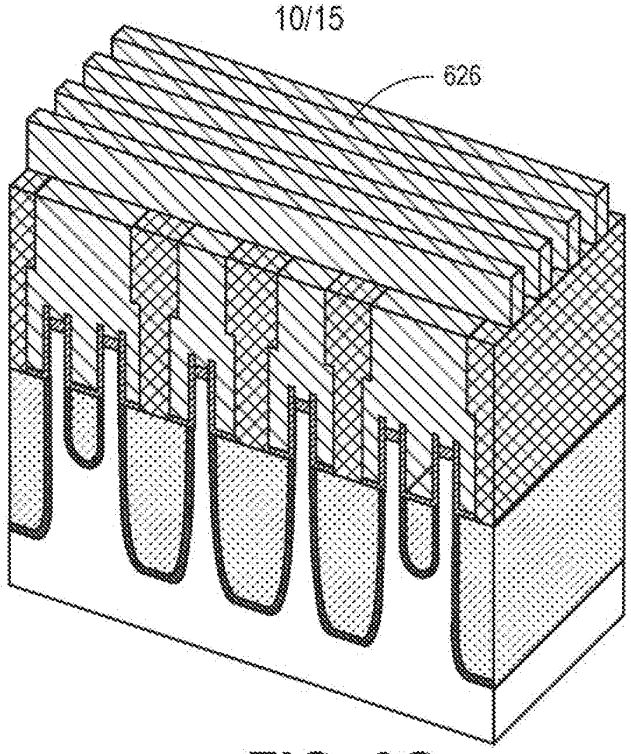


FIG. 6G

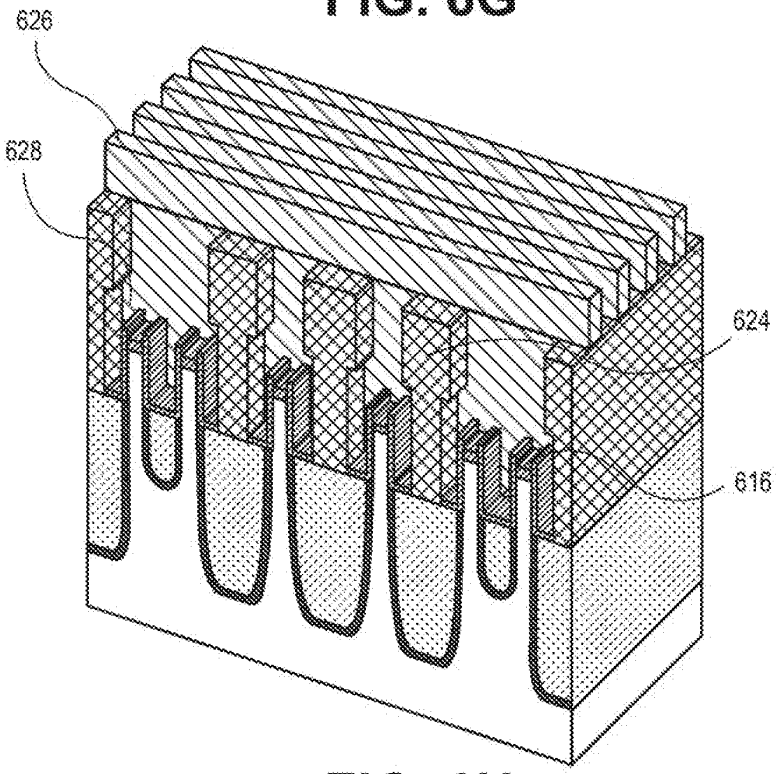


FIG. 6H

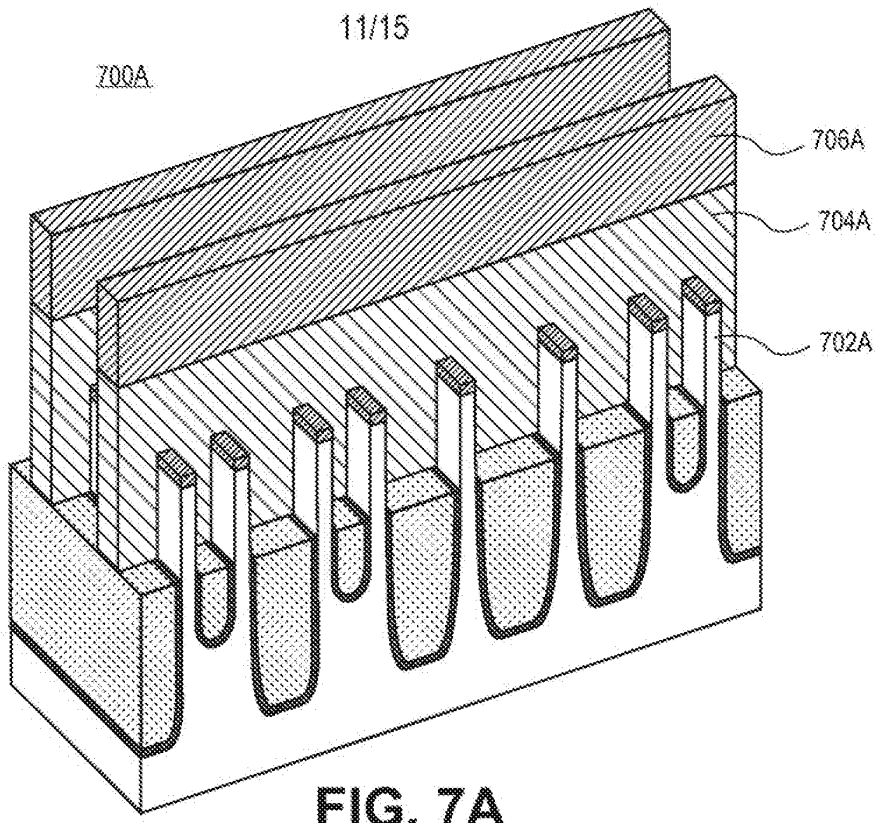


FIG. 7A

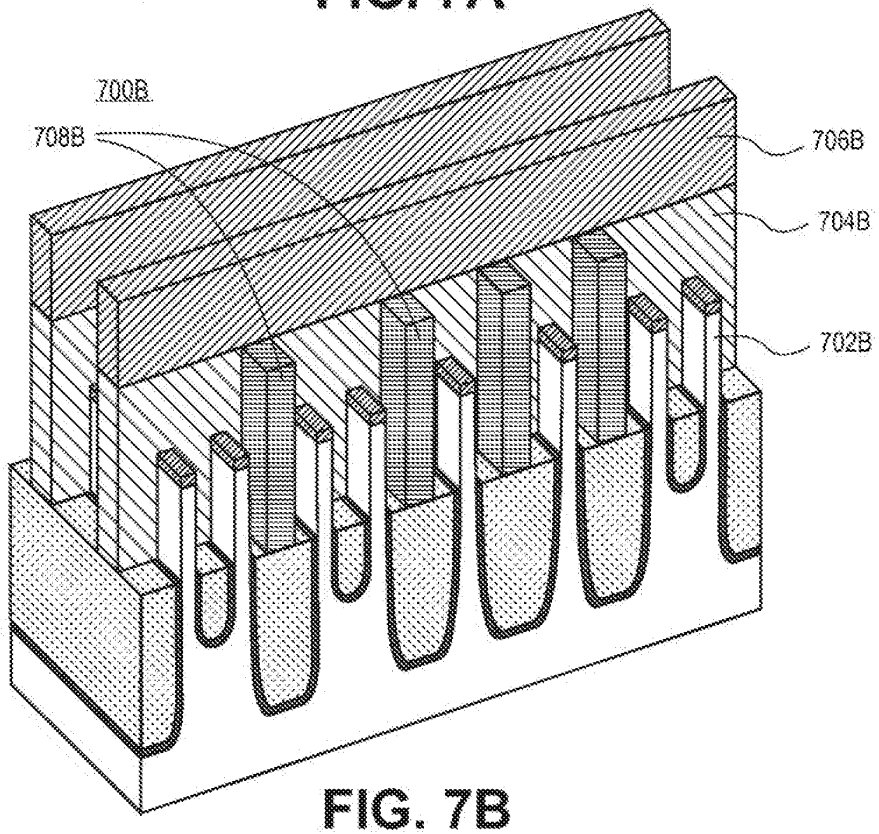


FIG. 7B

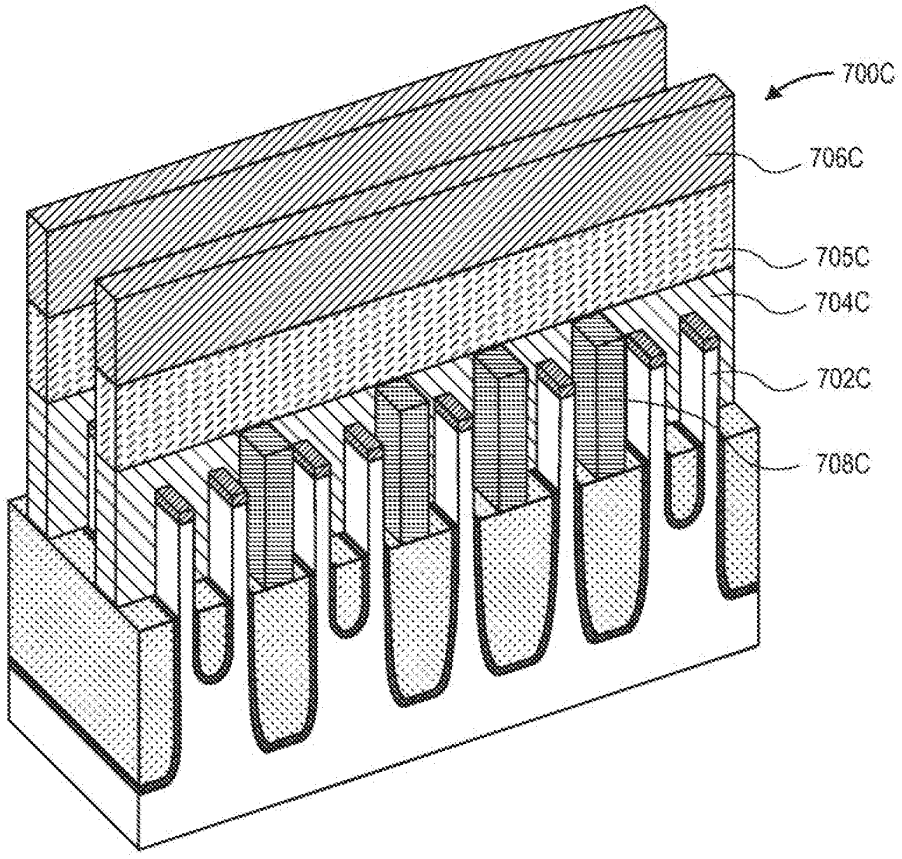


FIG. 7C

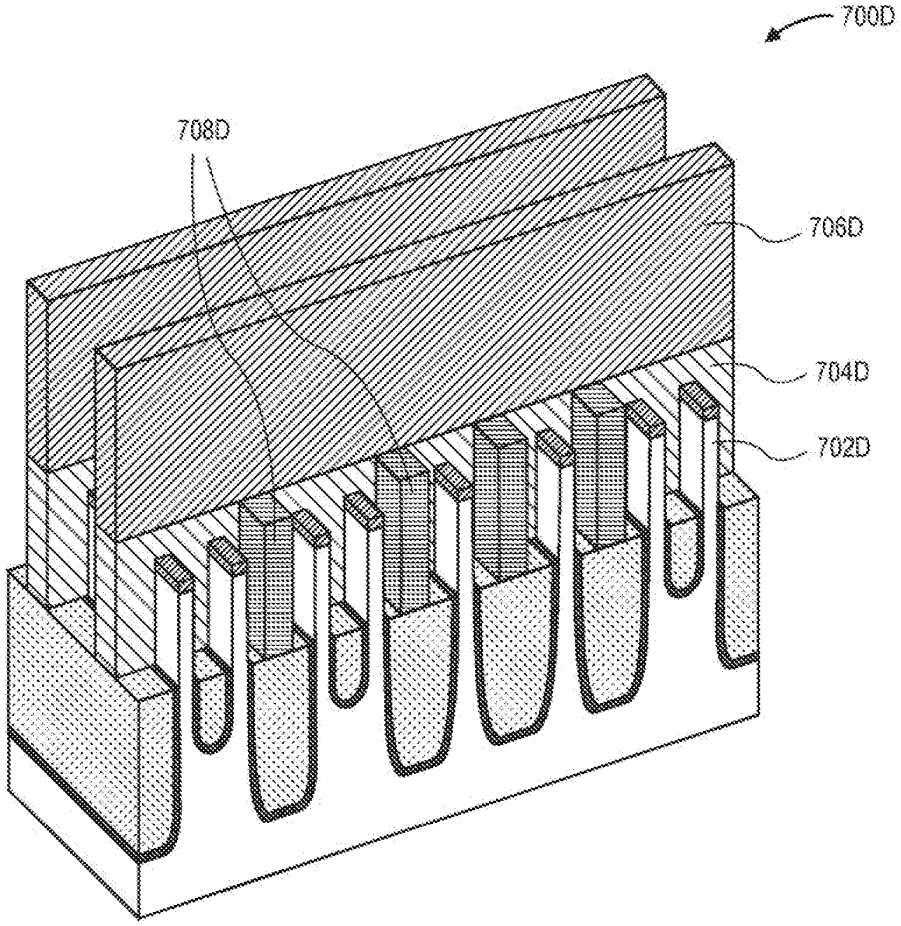


FIG. 7D

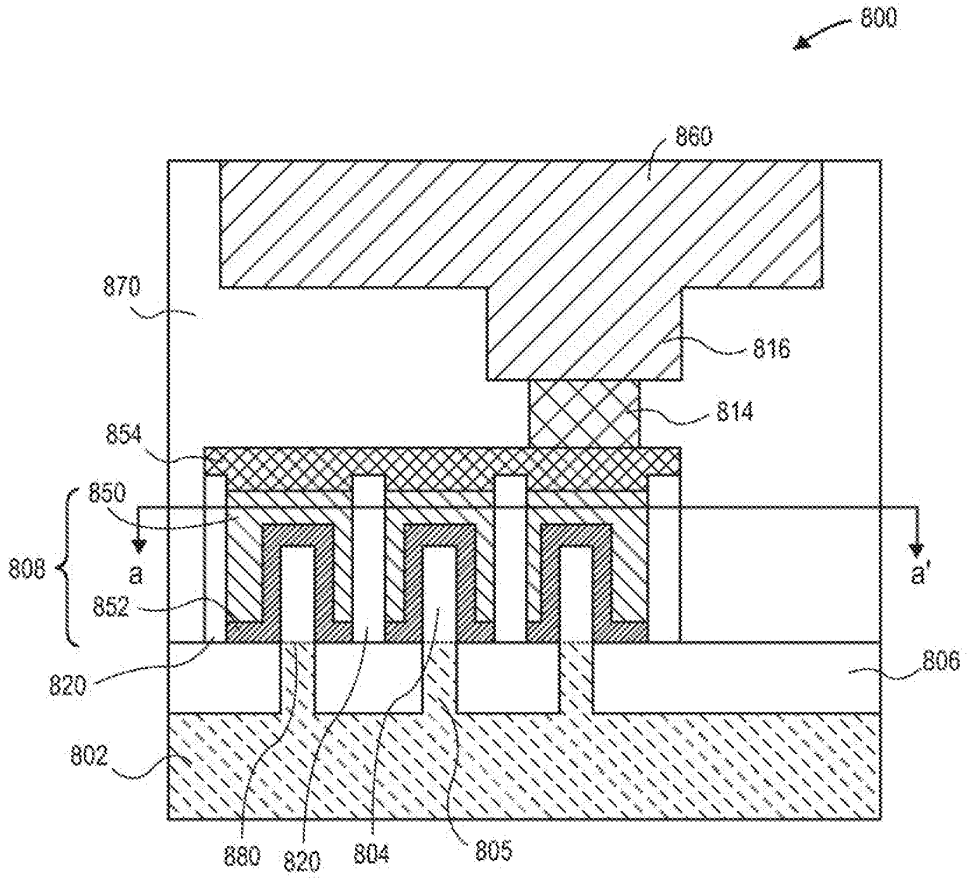

800
860
870
816
814
854
850
808
a
a'
852
820
806
802
880
820
804
805

FIG. 8A

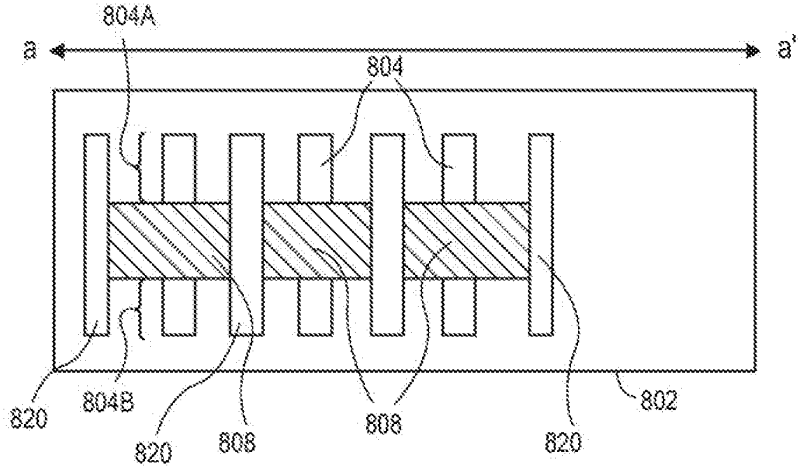

804A
a
a'
804
820
804B
820
808
808
820
802

FIG. 8B

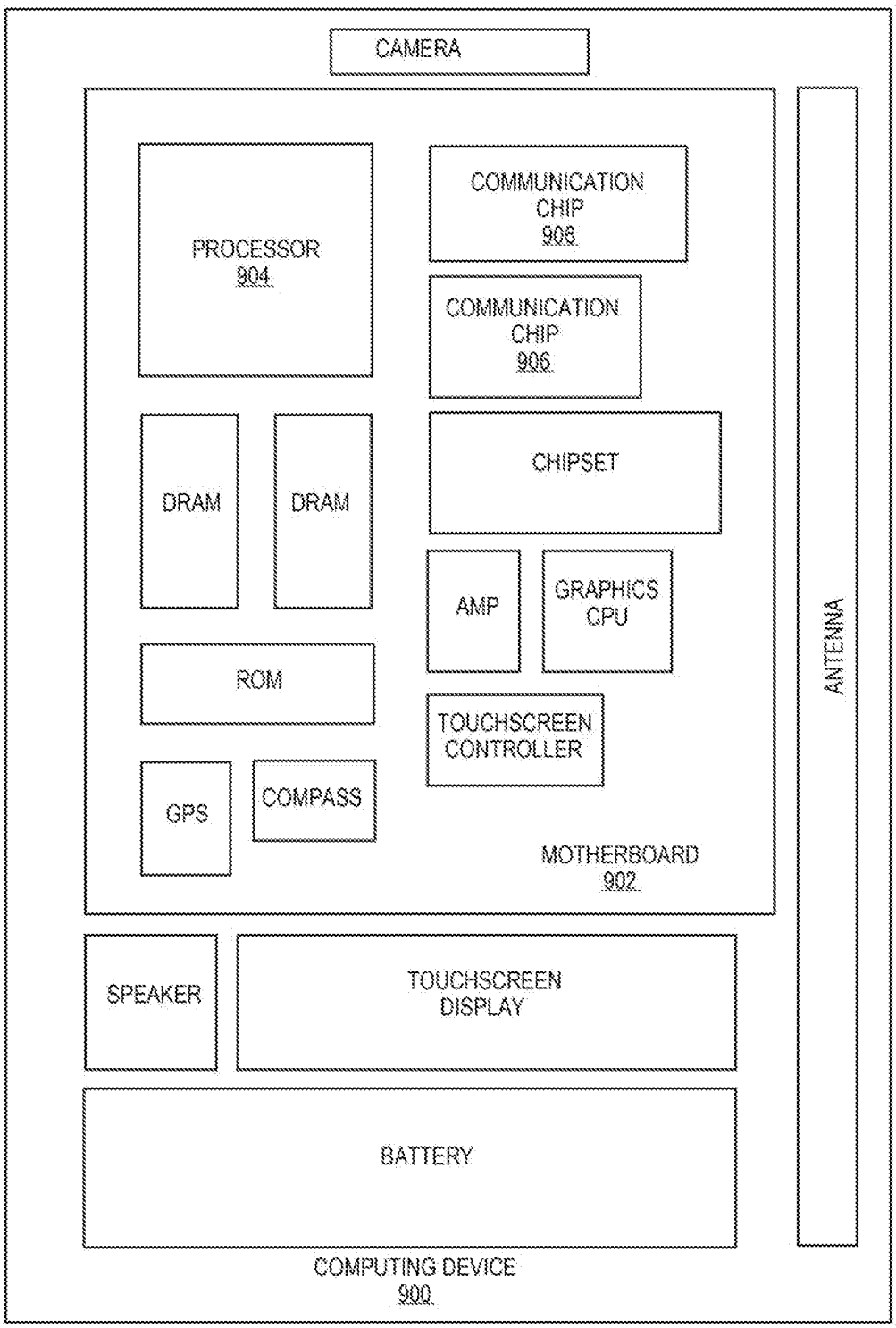

CAMERA
PROCESSOR
904
COMMUNICATION
CHIP
906
COMMUNICATION
CHIP
906
DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD
902
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE
900

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/076673

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/336; H01L 29/06; H01L 21/3065; H01L 29/80; H01L 21/28; H01L 29/78; H01L 21/8238; H01L 21/76

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: fin, isolation structure, dummy, orthogonal, direction, self-align and tri-gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
A	US 2007-0080380 A1 (PETER CHANG) 12 April 2007 See abstract, paragraphs [0043]-[0047], claims 1, 15 and figures 8-11.	1-25
A	US 2011-0021027 A1 (FRANK SCOTT JOHNSON) 27 January 2011 See abstract, paragraphs [0016]-[0020] claim 1 and figure 8.	1-25
A	US 2013-0020615 A1 (SU CHEN FAN et al.) 24 January 2013 See abstract, paragraphs [0028]-[0029], claim 1 and figures 8-9.	1-25
A	KR 10-2005-0082099 A (SAMSUNG ELECTRONICS CO., LTD.) 22 August 2005 See abstract, page 5, claim 1 and figures 18-23.	1-25
A	US 2007-0054464 A1 (GUOMEI ZHANG) 08 March 2007 See abstract, paragraphs [0011], [0022], claim 1 and figure 7.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 September 2014 (26.09.2014)	**26 September 2014 (26.09.2014)**

Name and mailing address of the ISA/KR	Authorized officer
International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	KIM, Young Jin Telephone No. +042 481 5771

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/076673

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0080380 A1	12/04/2007	CN 101283446 A	08/10/2008
		CN 101283446 B	05/12/2012
		DE 112006002726 T5	28/08/2008
		GB 0806265 D	14/05/2008
		GB 2444466 A	04/06/2008
		GB 2444466 B	16/03/2011
		KR 10-1038118 B1	31/05/2011
		KR 10-2008-0047452 A	28/05/2008
		TW 313041 A	01/08/2009
		TW 313041 B	01/08/2009
		US 7223650 B2	29/05/2007
		WO 2007-046920 A1	26/04/2007
US 2011-0021027 A1	27/01/2011	US 8192641 B2	05/06/2012
US 2013-0020615 A1	24/01/2013	US 2013-023115 A1	24/01/2013
		US 8637908 B2	28/01/2014
		US 8741752 B2	03/06/2014
KR 10-2005-0082089 A	22/08/2005	CN 100472806 C	25/03/2009
		CN 1938861 A	28/03/2007
		JP 2007-522683 A	09/08/2007
		JP 4642786 B2	02/03/2011
		US 2007-0272925 A1	29/11/2007
		US 2011-0053989 A1	10/02/2011
		US 7838915 B2	23/11/2010
		WO 2005-078804 A1	25/08/2005
US 2007-0054464 A1	08/03/2007	SG 131008 A1	26/04/2007

Form PCT/ISA/210 (patent family annex) (July 2009)

ISR/WO

JKB/BV

PCT/US2013/076673

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
BRASK, JUSTIN K.

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279
OAKMEAD PARKWAY SUNNYVALE CA 94085-4040 USA

RECEIVED
OCT 08 2014
BEAVERTON

RECEIVED
SUNNYVALE
OCT 07 2014
BLAKELY SOKOLOFF TAYLOR ZAFMAN

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 42P60397PCT	Date of mailing *(day/month/year)* 26 September 2014 (26.09.2014) **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. **PCT/US2013/076673**	International filing date *(day/month/year)* **19 December 2013 (19.12.2013)**

Applicant
INTEL CORPORATION et al

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

How? Directly to the International Bureau of WIPO preferably through ePCT or on paper to: 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9-011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Within **19 months** from the priority date, the applicant may request that a supplementary international search be carried out by an International Searching Authority that offers this service (Rule 45*bis*.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/KR International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer COMMISSIONER Telephone No. 82-42-481-8751

Form PCT/ISA/220 (July 2014)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for six months(expire date : **2015.03.26**) from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **N34927A8**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through iPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com

Email: ipkc@ipkcenter.com

Notes to Form PCT/ISA/220 (July 2014)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 42P60397PCT	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. **PCT/US2013/076673**	International filing date *(day/month/year)* **19 December 2013 (19.12.2013)**	(Earliest) Priority Date *(day/month/year)*

Applicant

INTEL CORPORATION et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of :

☒ the international application in the language in which it was filed

☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (See Box No. II)

3. ☐ **Unity of invention is lacking** (See Box No. III)

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the drawings,

a. the figure of the **drawings** to be published with the abstract is Figure No. **8A**

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/076673

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/336; H01L 29/00; H01L 21/3065; H01L 29/80; H01L 21/28; H01L 29/78; H01L 21/8238; H01L 21/76

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: fin, isolation structure, dummy, orthogonal, direction, self-align and tri-gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0090380 A1 (PETER CHANG) 12 April 2007 See abstract, paragraphs [0043]-[0047], claims 1, 10 and figures 9-11.	1-25
A	US 2011-0021027 A1 (FRANK SCOTT JOHNSON) 27 January 2011 See abstract, paragraphs [0016]-[0020] claim 1 and figure 8.	1-25
A	US 2012-0020015 A1 (SU CHEN FAN et al.) 24 January 2013 See abstract, paragraphs [0028]-[0029], claim 1 and figures 8-9.	1-25
A	KR 10-2005-0082099 A (SAMSUNG ELECTRONICS CO., LTD.) 22 August 2005 See abstract, page 5, claim 1 and figures 18-28.	1-25
A	US 2007-0054464 A1 (GUOHUI ZHANG) 08 March 2007 See abstract, paragraphs [0011], [0022], claim 1 and figure 7.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 September 2014 (26.09.2014)	**26 September 2014 (26.09.2014)**
Name and mailing address of the ISA/KR International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	Authorized officer KIM, Young Jin Telephone No. +042 481 5771

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/076673

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0080380 A1	12/04/2007	CN 101283446 A	08/10/2008
		CN 101283446 B	05/12/2012
		DE 112006002726 T5	28/08/2008
		GB 0806285 D	14/05/2008
		GB 2444406 A	04/06/2008
		GB 2444406 B	16/03/2011
		KR 10-1038118 B1	31/05/2011
		KR 10-2008-0047453 A	28/05/2008
		TW 313041 A	01/08/2009
		TW 313041 B	01/08/2009
		US 7223650 B2	29/05/2007
		WO 2007-046920 A1	26/04/2007
US 2011-0021027 A1	27/01/2011	US 8192641 B2	05/06/2012
US 2013-0020615 A1	24/01/2013	US 2013-023115 A1	24/01/2013
		US 8637908 B2	28/01/2014
		US 8741752 B2	03/06/2014
KR 10-2005-0082099 A	22/08/2005	CN 100472806 C	25/03/2009
		CN 1938861 A	28/03/2007
		JP 2007-522683 A	09/08/2007
		JP 4642786 B2	02/03/2011
		US 2007-0272925 A1	29/11/2007
		US 2011-0033989 A1	10/02/2011
		US 7828915 B2	23/11/2010
		WO 2005-078804 A1	25/08/2005
US 2007-0054404 A1	08/03/2007	SG 131008 A1	26/04/2007

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
BRASK, JUSTIN K.

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279
OAKMEAD PARKWAY SUNNYVALE CA 94085-4040
USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**26 September 2014 (26.09.2014)**
Applicant's or agent's file reference 42P60397PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2013/076673	**19 December 2013 (19.12.2013)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 21/336(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	26 September 2014 (26.09.2014)	KIM, Young Jin Telephone No. +082 481 5771

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/076673

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)
   ☐ on paper
   ☐ in electronic form

   b. (time)
   ☐ in the international application as filed.
   ☐ together with the international application in electronic form.
   ☐ subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/076673

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-25	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-25	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-25	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2007-0080380 A1 (PETER CHANG) 12 April 2007
D2: US 2011-0021027 A1 (FRANK SCOTT JOHNSON) 27 January 2011
D3: US 2013-0020615 A1 (SU CHEN FAN et al.) 24 January 2013
D4: KR 10-2005-0082090 A (SAMSUNG ELECTRONICS CO., LTD.) 22 August 2005
D5: US 2007-0054464 A1 (GUOWEI ZHANG) 08 March 2007

1 Novelty and Inventive Step
1.1. Claims 1-8
The subject matter of claim 1 differs from these prior art documents in a semiconductor structure comprising a pair of gate edge isolation structures centered with the semiconductor fin, wherein a first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 1 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Claims 2-8 are directly or indirectly dependent on claim 1 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.2. Claims 9-14
The subject matter of claim 9 differs from these prior art documents in a semiconductor structure comprising a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 9 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Continued on Supplemental Box

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/076673

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

In claim 3, lines 3-4, 'the first semiconductor fin' lacks proper antecedent basis.

In claim 4, lines 2-3, 'the first gate structure' is not predefined.

Claim 5 is unclear since the expression 'the pair of and the third gateedge isolation structures' is vague.

In claim 19, lines 3-4, 'the sidewalls' and 'the first and second semiconductor fins' are not predefined.

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of : Box No. V

Claims 10-14 are directly or indirectly dependent on claim 9 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.3. Claims 15-18
The subject matter of claim 15 differs from these prior art documents in a semiconductor structure comprising a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 15 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Claims 16-18 are dependent on claim 15 and therefore meet the requirements of PCT Article 33(2) and 33(3).

1.4. Claims 19-25
The subject matter of claim 19 differs from these prior art documents in a method comprising: forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins, wherein the dummy spacers of the first semiconductor fin are non-continuous with the dummy spacers of the second semiconductor fin; forming an isolation structure between the dummy spacers of the first and second semiconductor fins; removing the dummy spacers; and forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure. And it is not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 19 meets the requirements of PCT Article 33(2) and 33(3) with respect to novelty and inventive step.

Claims 20-25 are dependent on claim 19 and therefore meet the requirements of PCT Article 33(2) and 33(3).

2. Industrial Applicability
Claims 1-25 are industrially applicable under PCT Article 33(4).

Box No. VIII (iv) DECLARATION: INVENTORSHIP (only for the purposes of the designation of the United States of America)
The declaration must conform to the following standardized wording provided for in Section 214; see Notes to Boxes Nos. VIII, VIII (i) to (v) (in general) and the specific Notes to Box No.VIII (iv). If this Box is not used, this sheet should not be included in the request.

Declaration of Inventorship (Rules 4.17(iv) and 51*bis*.1(a)(iv))
for the purposes of the designation of the United States of America:

I hereby declare that I believe I am the original or an original joint inventor of a claimed invention in the application.

This declaration is directed to the international application of which it forms a part (if filing declaration with application).

This declaration is directed to international application No. PCT/US13/076673 (if furnishing declaration pursuant to Rule 26*ter*).

I hereby declare that the above-identified international application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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Espacenet

Bibliographic data: KR20050082099 (A) — 2005-08-22

SEMICONDUCTOR DEVICE HAVING MULTI-GATE STRUCTURE AND METHOD OF MANUFACTURING THE SAME

Inventor(s): CHOI JUNG A [KR]; YANG JEONG HWAN [KR]; JIN YOU SEUNG [KR] ± (CHOI, JUNG A, ; YANG, JEONG HWAN, ; JIN, YOU SEUNG)

Applicant(s): SAMSUNG ELECTRONICS CO LTD [KR] ± (SAMSUNG ELECTRONICS CO., LTD)

Classification: - international: ***H01L21/336; H01L27/12; H01L29/78; H01L29/786;*** (IPC1-7): H01L29/78
- cooperative: **H01L27/1203**; **H01L29/41725**; **H01L29/4232**; **H01L29/66795**; **H01L29/7831**; **H01L29/7848**; **H01L29/785**; **H01L29/78696** more

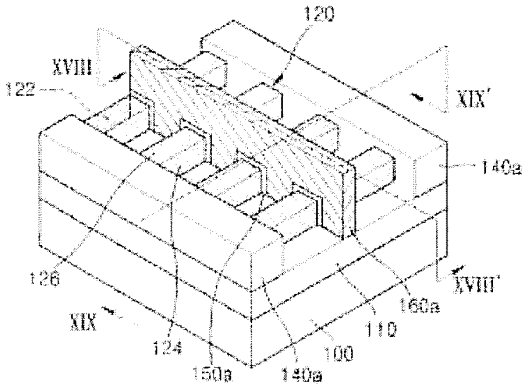
Application number: KR20040010472 20040217

Priority number (s): KR20040010472 20040217

Also published as: KR100574971 (B1) WO2005078804 (A1) US2011033989 (A1) US2007272925 (A1) US7838915 (B2) more

Abstract not available for KR20050082099 (A)
Abstract of corresponding document: WO2005078804 (A1)

Provided are a semiconductor device having a mesa-type active region including a plurality of slabs and a method of manufacturing the semiconductor device. The semiconductor device includes a first active region and a second active region. The first active region is formed in a line-and-space pattern on a substrate and includes the slabs, each slab having a first surface, a second surface facing a direction opposite to the first side, and a top surface. The first active region and the second active



region are composed of identical or different materials. The second active region contacts at least one end of each of the slabs on the substrate to connect the slabs to one another. The method includes forming a first active region in a line-and-space pattern on the substrate and forming the second active region.

Espacenet

Description: KR20050082099 (A) — 2005-08-22

SEMICONDUCTOR DEVICE HAVING MULTI-GATE STRUCTURE AND METHOD OF MANUFACTURING THE SAME

Description of KR20050082099 (A)

A high quality text as facsimile in your desired language may be available amongst the following family members:

CN1938861 (A) DE112005000394 (T5) US2007272925 (A1) WO2005078804 (A1) DE112005000394 (B4) US2011033989 (A1)

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멀티-게이트 구조의 반도체 소자 및 그 제조 방법{Semiconductor device having multi-gate structure and method of manufacturing the same}

도 1a는 종래 기술에 따른 멀티-게이트 트랜지스터의 개략적인 구조를 도시한 것이다.

도 1b는 종래 기술에 따른 반도체 소자 제조 방법에서 활성 영역을 패터닝하기 위한 리소그래피 공정시 사용되는 OPC (Optical Proximity Correction)가 적용된 레티클 (reticle) 패턴을 나타낸다.

도 1c는 종래 기술에 따라 OPC가 적용된 멀티-게이트 레티클을 이용하여 구현된 활성 영역의 평면 프로파일을 나타낸다.

도 2 내지 도 17은 본 발명의 제1 실시예에 따른 반도체 소자의 제조 방법을 설명하기 위하여 공정 순서에 따라 도시한 부분 사시도들이다.

도 18은 도 17의 XVIII - XVIII'선 단면도이다.

도 19는 도 17의 XIX - XIX'선 단면도이다.

도 20 내지 도 22는 본 발명의 제2 실시예에 따른 반도체 소자의 제조 방법을 설명하기 위하여 공정 순서에 따라 도시한 부분 사시도들이다.

도 23은 도 22의 XXIII - XXIII'선 단면도이다.

도 24는 도 22의 XXIV - XXIV'선 단면도이다.

<도면의 주요 부분에 대한 부호의 설명>

100: 실리콘 기판, 110: 매몰 산화막, 120: 슬랩, 122: 제1 측면, 124: 제2 측면, 126: 상면, 128: 단부, 130: 마스크층, 130a: 마스크 패턴, 130b: 마스크 패턴, 132: 포토레지스트막, 132a: 포토레지스트 패턴, 140: 반도체층, 140a: 제2 활성 영역, 142: 오버랩 영역, 150: 절연막, 150a: 게이트 절연막, 160: 도전층, 160a: 게이트 라인, 172: 마스크층, 172a: 마스크 패턴, 174: 포토레지스트막, 174a: 포토레지스트 패턴, 182: 제1 채널 영역, 184: 제2 채널 영역, 186: 제3 채널 영역, 240: 제2 활성 영역, 242: 오버랩 영역.

본 발명은 반도체 소자 및 그 제조 방법에 관한 것으로, 특히 채널이 슬랩(slab) 형상의 메사(mesa)형 활성 영역에 형성되는 멀티-게이트 구조의 MOS (metal-oxide-semiconductor)형 트랜지스터를 구비하는 반도체 소자 및 그 제조 방법에 관한 것이다.
반도체 소자의 고속화, 고기능화 및 저소비 전력화를 구현하기 위하여 집적 회로를 구성하는 개개의 트랜지스터의 우수한 구동 능력을 유지하면서 그 사이즈를 축소시켜 집적 회로에서의 소자 밀도를 증가시키기 위한 노력이 계속되고 있다. 소자 밀도를 증가시키기 위하여는 반도체 소자의 피쳐 사이즈 (feature size)를 줄일 수 있는 기술이 필요하다.CMOS (complementary MOS)에서의 소자 밀도를 높이기 위한 FET (field effect transistor)의 스케일링 (scailing) 기술 중 하나로서 SOI (silicon-on-insulator) 웨이퍼를 사용하여 핀 (fin) 형상의 실리콘 바디(body)를 형성하고, 그 표면 위에 게이트를 형성하는 멀티-게이트 트랜지스터가 제안되었다. (예를 들면, Fu-Liang Yang et al., "35nm CMOS FinFETs", Symposium on VLSI Technology Digest of Technical Papers, pp. 104-105, 2002; 및 B. S. Doyle et al., "High Performance Fully-Depleted Tri-Gate CMOS Transistors", IEEE Electron Device Letters, Vol. 24, No. 4, April, 2003, pp. 263-365)실리콘 핀 바디를 이용한 멀티-게이트 트랜지스터는 3차원의 채널을 이용함으로써 CMOS의 스케일링시 매우 유리하게 적용될 수 있으며, 완전 공핍형 SOI 구조를 채용함으로써 게이트 길이를 증가시키지 않고도 우수한 서브쓰레숄드 특성 및 전류 제어 능력을 제공할 뿐 만 아니라 드레인 전압에 의해 채널 영역의 전위가 영향을 받는 SCE (short channel effect)를 효과적으로 억제할 수 있는 이점을 제공하는 것으로 널리 알려져 있다.
특히, 트리-게이트 (tri-gate) CMOS는 3개의 표면에 형성되는 채널을 이용하므로 FinFET에 비하여 채널을 형성하기 위한 활성 영역의 폭 및 높이에 있어서 설계상의 허용 범위가 큰 장점이 있다.도 1a에 도시한 바와 같이, SOI 웨이퍼의 매몰 산화막 (buried oxide film)(10) 위에 멀티-게이트 트랜지스터를 제조하는 데 있어서 소스/드레인 역할을 하기 위한 실리콘 활성 영역(12)이 통상적으로 메사형 슬랩 형상으로 구현된다. 여기서, 상기 실리콘 활성 영역(12)에는 그 상면 및 양 측면을 덮는 게이트 라인(14)과 대면하는 부분 근방에 채널이 형성된다.멀티-게이트 트랜지스터의 전기적 특성은 활성 영역의 높이, 폭 등과 같은 활성 영역의 사이즈와, 활성 영역의 곡률 (curvature), 평면상에서 볼 때의 라운딩 프로파일 등과 같은 활성 영역의 형상에 따라 크게 영향을 받는다. 즉, 게이트 라인에 의해 덮이는 활성 영역 슬랩의 사이즈 및 형상의 균일도에 따라 멀티-게이트 트랜지스터의 퍼포먼스 (performance)에 편차가 발생하거나, 전기적 특성이 열화될 수 있다.
종래 기술에서는 도 1a에 도시한 바와 같은 형상의 활성 영역을 패터닝할 때, 리소그래피 공정시의 근접효과 (proximity effect)에 따른 문제를 해결하기 위하여 도 1b에 도시한 바와 같이 OPC (Optical Proximity Correction)를 적용한 레티클 (reticle) 패턴을 이용한다. 도 1b에서, "22"는 활성 영역 슬랩 패턴을 나타내고, "24"는 더미 패턴을 나타낸다. 즉, 종래 기술에서는 레티클상에 OPC를 적용한 독립적인 활성 영역 슬랩을 패터닝하고, 리소그래피 특성을 이용하여 각 활성 영역 슬랩을 연결시킨다.도 1b에 도시한 바와 같은 레티클 패턴을 이용하여 리소그래피 공정을 행하는 경우, 도 1c의 평면도에 나타낸 바와 같이 "라운딩(rounding)" 현상이 발생된 활성 영역 패턴(30)이 구현될 가능성이 매우 크다.도 1a에 나타낸 바와 같은 활성 영역(12)에서 각 슬랩의 피치가 작아질수록 도 1b를 참조하여 설명한 바와 같이 종래 기술에 따라 OPC를 적용하여 활성 영역을 형성하는 경우에는 리소그래피 공정에서의 해상 한계로 인하여 도 1c에 도시한 바와 같이 활성 영역

을 구성하는 슬랩에서 프로파일 라운딩 현상이 발생하거나, ADI (after-development inspection)시 CD 편차 (critical dimension variation)를 야기한다. 특히, 여러 개의 슬랩이 평행하게 배열되어 있는 트랜지스터를 구현할 때에는 각 슬랩에서 균일한 프로파일 및 CD를 가지도록 패터닝하는 것이 더욱 어렵다. 그 결과, 종래 기술에 따라 도 1a에 도시한 형상의 활성 영역(12)을 형성할 때에는 리소그래피 공정 후에 얻어지는 패턴 프로파일 불량, 식각 공정 후에 각 슬랩의 사이즈 균일도 분량, 식각 공정 후에 활성 영역상에서의 원하지 않는 실리콘 잔류물 발생, 식각 공정시 각 슬랩 사이의 갭이 오픈되지 않는 "낫 오픈(not open)" 현상 발생 등과 같은 다양한 문제가 발생된다. 또한, 도 1c에 도시한 바와 같이 패턴 라운딩 현상이 발생된 활성 영역 위에 게이트 라인이 y축 방향에 따라 미스얼라인되어 형성되는 경우에는 멀티-게이트 트랜지스터의 퍼포먼스에 큰 편차가 발생하는 것을 피할 수 없다.본 발명은 상기한 바와 같은 종래 기술에서의 문제점을 해결하고자 하는 것으로, 안정적이고 균일한 프로파일 및 제어된 CD를 가지는 활성 영역을 구비함으로써 멀티-게이트 트랜지스터에서 균일한 퍼포먼스를 얻을 수 있고 전기적 특성을 향상시킬 수 있는 반도체 소자를 제공하는 것이다.본 발명의 다른 목적은 멀티-게이트 트랜지스터를 구현하는 데 있어서 활성 영역의 재현성 있는 프로파일 및 CD 제어 가능성을 안정적으로 확보할 수 있는 반도체 소자의 제조 방법을 제공하는 것이다.

상기 목적을 달성하기 위하여, 본 발명에 따른 반도체 소자는 상호 연결되어 있는 제1 활성 영역 및 제2 활성 영역을 포함한다. 제1 활성 영역은 기판 위에 라인 앤드 스페이스 패턴 (line and space pattern) 형상으로 형성되고, 상호 반대 방향인 제1 측면 및 제2 측면과 상면을 각각 가지는 복수의 슬랩(slab)으로 구성된다. 제2 활성 영역은 상기 제1 활성 영역과는 같거나 다른 물질로 이루어지고 상기 복수의 슬랩을 상호 연결시키도록 상기 기판상에서 상기 슬랩의 적어도 일단부에 접하여 연장되어 있다. 상기 슬랩의 적어도 제1 측면 및 제2 측면과 상면 위에 게이트 라인이 형성되어 있다. 상기 슬랩과 상기 게이트 라인과의 사이에는 게이트 절연막이 개재되어 있다.상기 슬랩의 상면은 상기 기판으로부터 제1 거리 만큼 이격되어 있으며, 상기 제2 활성 영역은 상기 기판으로부터 상기 제1 거리와 같거나 더 큰 제2 거리 만큼 이격되어 있다.상기 제2 활성 영역은 상기 슬랩의 양 단부에 접해 있는 상태에서 상기 슬랩의 연장 방향과 직교하는 방향으로 연장되어 있다. 바람직하게는, 상기 제2 활성 영역은 상기 슬랩 중 상기 제1 측면, 제2 측면 및 상면의 일부와 접하여 연장되어 있는 오버랩 영역을 가진다.바람직하게는, 상기 게이트 라인은 상기 슬랩의 연장 방향과는 직교하는 방향으로 연장되어 있고, 상기 제2 활성 영역의 연장 방향과는 평행한 방향으로 연장되어 있다.상기 제1 활성 영역 중 상기 슬랩의 제1 측면 및 제2 측면에 근접하여 상기 게이트 라인과 대면하는 부분에는 각각 제1 채널 영역 및 제2 채널 영역이 위치한다. 트리-게이트 트랜지스터를 구성하기 위하여, 상기 제1 활성 영역 중 상기 슬랩의 상면에 근접하여 상기 게이트 라인과 대면하는 부분에 제3 채널 영역이 더 위치될 수 있다.상기 다른 목적을 달성하기 위하여, 본 발명에 따른 반도체 소자의 제조 방법에서는 라인 앤드 스페이스 패턴 형상을 가지고 제1 물질로 이루어지는 제1 활성 영역을 기판 위에 형성한다. 상기 제1 활성 영역의 적어도 일부에 접하여 연장되고 상기 제1 물질과 같거나 다른 제2 물질로 이루어지는 제2 활성 영역을 상기 기판 위에 형성한다. 상기 제1 활성 영역 위에 게이트 절연막을 형성한다. 상기 게이트 절연막 위에 게이트를 형성한다.상기 제2 활성 영역을 형성하기 위하여, 먼저 상기 슬랩의 양 단부를 노출시키도록 상기 슬랩의 일부를 덮는 마스크 패턴을 상기 기판 위에 형성한다. 그 후, 상기 제2 물질을 증착하여 상기 슬랩의 노출된 양 단부 및 상기 마스크 패턴을 덮는 제2 물질층을 형성한다. 이어서, 상기 제2 물질층을 평탄화한다.본 발명에 의하면, 멀티-게이트 트랜지스터의 활성 영역을 각각 제1 활성 영역 및 제2 활성 영역으로 나누어 형성함으로써 디자인 룰 300nm 이하의 피치를 가지는 활성 영역을 형성할 때 리소그래피 공정시의 해상 한계에 따른 문제점들을 회피할 수 있으며, 활성 영역에서 CD 편차에 따른 문제를 개선할 수 있다. 따라서, 본 발명에 의하면 활성 영역의 재현성 있는 프로파일 및 CD 제어 가능성을 안정적으로 확보할 수 있으며, 멀티-게이트 트랜지스터에서 균일한 퍼포먼스 및 향상된 전기적 특성을 제공할 수 있는 반도체 소자를 구현할 수 있다.다음에, 본 발명의 바람직한 실시예들에 대하여 첨부 도면을 참조하여 상세히 설명한다.다음에 예시하는 실시예들은 여러가지 다른 형태로 변형될 수 있으며, 본 발명의 범위가 다음

에 상술하는 실시예에 한정되는 것은 아니다. 본 발명의 실시예는 당 업계에서 평균적인 지식을 가진 자에게 본 발명을 보다 완전하게 설명하기 위하여 제공되어지는 것이다. 첨부 도면에서 막 또는 영역들의 크기 또는 두께는 명세서의 명확성을 위하여 과장되어진 것이다.도 2 내지 도 17은 본 발명의 제1 실시예에 따른 반도체 소자의 제조 방법을 설명하기 위하여 공정 순서에 따라 도시한 부분 사시도들이다.도 2를 참조하면, 실리콘 기판(100), 매몰 산화막(110), 및 단결정 실리콘층으로 이루어지는 SOI층이 차례로 적층된 SOI 기판을 준비한다. 상기 SOI 기판으로서 예를 들면 SIMOX (Separation by Implantation of Oxygen) 공정에 의하여 형성된 SOI 기판을 사용할 수 있다. 예를 들면, 상기 매몰 산화막(110)은 약 1000 ~ 1500Å의 두께를 가진다.포토레지스트 패턴 또는 하드 마스크 패턴을 식각 마스크로 이용하는 식각 공정에 의하여 상기 SOI층을 패터닝하여 상기 매몰 산화막(110) 위에 라인 앤드 스페이스 패턴 (line and space pattern) 형상의 메사형 활성 영역으로서 복수의 슬랩(120)을 형성한다. 상기 복수의 슬랩(120)은 제1 활성 영역을 구성한다. 상기 슬랩(120)은 각각 상기 실리콘 기판(100)의 주면 연장 방향과 수직을 이루도록 연장되는 제1 측면(122) 및 제2 측면(124)과, 상기 실리콘 기판(100)의 주면 연장 방향과 평행하게 연장되는 상면(126)을 가지도록 형성된다. 각 슬랩(120)의 상면의 폭(W)은 약 50nm 이하의 범위에서 선택될 수 있고, 각 슬랩(120)의 높이(H)는 약 70 nm 이하의 범위에서 선택될 수 있다. 그러나, 본 발명은 이에 한정되는 것은 아니다. 도 3을 참조하면, 상기 매몰 산화막(110) 위에 상기 슬랩(120)을 완전히 덮는 마스크층(130)을 형성하고, 상기 마스크층(130) 위에 포토레지스트막(132)을 형성한다.상기 마스크층(130)은 예를 들면 SiON막, Si3N4막, 또는 SiO2막으로 구성되는 단일막, 또는 이들의 조합으로 구성되는 다중막으로 이루어진다. 바람직하게는, 상기 마스크층(130)은 SiON막 및 Si3N4막으로 구성되는 이중막으로 이루어진다. 더욱 바람직하게는, 상기 마스크층(130)은 상기 슬랩(120)과 접하도록 상기 슬랩(120)의 바로 위에 형성되는 SiON막과, 그 위에 형성되어 상기 마스크층(130)의 상면을 구성하는 Si3N4막으로 이루어진다. 상기 마스크층(130)을 이와 같이 형성하면, 하부의 SiON막에 의하여 상기 슬랩(120)을 구성하는 실리콘(Si)이 외부 요인에 의하여 손상받는 것을 방지할 수 있고, 상부의 Si3N4막에 의하여 후속의 CMP (chemical mechanical polishing) 공정시 우수한 연마 특성을 얻을 수 있다.도 4를 참조하면, 상기 포토레지스트막(132)을 패터닝하여 상기마스크층(130)을 일부 노출시키는 포토레지스트 패턴(132a)을 형성한다.도 5를 참조하면, 상기 포토레지스트 패턴(132a)을 식각 마스크로 하여 상기 마스크층(130)을 식각하여, 각 슬랩(120)의 양 단부(128)를 노출시키도록 상기 슬랩(120)의 일부 만을 덮는 마스크 패턴(130a)을 형성한다. 상기 마스크 패턴(130a)이 형성된 후, 상기 마스크 패턴(130a) 주위에서는 각 슬랩(120)의 양 단부(128)에 인접한 제1 측면(122), 제2 측면(124) 및 상면(126)이 일부 노출된다.도 6을 참조하면, 상기 포토레지스트 패턴(132a)을 제거하여 상기 마스크 패턴(130a)의 상면을 노출시킨다.도 7을 참조하면, 상기 마스크 패턴(130a) 및 그 주위에 노출되어 있는 각 슬랩(120)을 완전히 덮는 반도체층(140)을 형성한다. 상기 반도체층(140)은 예를 들면 LPCVD (low pressure chemical vapor deposition) 방법을 이용하여 형성될 수 있다. 상기 반도체층(140)은 상기 제1 활성 영역인 복수의 슬랩(120)을 구성하는 단결정 실리콘과 같거나 다른 물질로서, Si을 포함하는 물질로 이루어진다. 바람직하게는, 상기 반도체층(140)은 폴리실리콘, 비정질 실리콘, 또는 실리콘을 함유하는 반도체 화합물 예를 들면 Si1-xGex(0<x<1)로 이루어질 수 있다. 더욱 바람직하게는, 상기 반도체층(140)은 폴리실리콘으로 이루어진다. 상기 반도체층(140)은 원하는 바에 따라 수 백 ~ 수 천 Å의 두께로 형성될 수 있다.도 8을 참조하면, 상기 마스크 패턴(130a)이 노출될 때 까지 상기 반도체층(140)을 CMP 또는 에치백 (etch back) 방법에 의하여 평탄화하여 각슬랩(120)의 양 단부(128)를 덮는 제2 활성 영역(140a)을 형성한다. 상기 제2 활성 영역(140a)에 의하여 도 5에서 노출되었던 상기 슬랩(120)의 양 단부(128)에서 상기 제1 측면(122), 제2 측면(124) 및 상면(126) 중 일부가 덮이게 된다. 상기 제2 활성 영역(140a)을 통하여 제1 활성 영역인 각 슬랩(120)들이 상호 연결될 수 있다.도 9를 참조하면, 애싱(ashing) 및 습식 식각 공정에 의하여 상기 마스크 패턴(130a)을 제거한다. 그 결과, 상기 매몰 산화막(110) 위에서 제1 활성 영역인 복수의 슬랩(120)과 이들을 상호 연결시키는 제2 활성 영역(140a)이 완전히 노출된다. 상기 제2 활성 영역(140a)은 각 슬랩(120)의 양 단부(128)에 접하면서 상기 슬랩(120)의 연장 방향과 직교하는 방향으로

연장되어 있다. 또한, 상기 제2 활성 영역(140a)은 각 슬랩(120) 중 상기 제1 측면(122), 제2 측면(124) 및 상면(126)의 일부와 접하여 연장되어 있는 오버랩 영역(142)을 가진다. 여기서, 각 슬랩(120)의 양 단부(128) 중 가장 끝 표면은 상기 제2 활성 영역(140a)에 의해 덮일 수도 있고 덮이지 않을 수도 있다. 도 9에 있어서, 각 슬랩(120) 중 도 9의 전방(前方)에 있는 단부(128)의 끝 표면은 상기 제2 활성 영역(140a)에 의해 덮인 것으로 도시되어 있고, 도 9의 후방(後方)에 있는 단부(128)의 끝 표면은 상기 제2 활성 영역(140a)에 의해 덮이지 않은 것으로 도시되어 있다.그리고, 상기 제2 활성 영역(140a)의 상면은 상기 제1 활성 영역인 상기 슬랩(120)의 상면(126) 보다 높은 레벨을 가지며, 따라서 상기 실리콘 기판(100) 또는 상기 매몰 산화막(110)으로부터 상기 제2 활성 영역(140a)의 상면까지의 거리는상기 실리콘 기판(100) 또는 매몰 산화막(110)으로부터 상기 슬랩(120)의 상면(126)까지의 거리보다 더 크다.도 10을 참조하면, 상기 제1 활성 영역인 슬랩(120) 위에 절연막(150)을 형성한다. 상기 절연막(150)은 게이트 절연막을 형성하기 위하여 형성되는 것이다. 상기 절연막(150)은 상기 슬랩(120)의 표면으로부터 열산화 방법에 의하여 원하는 막질을 성장시켜 얻어질 수 있다. 또는 상기 절연막(150)을 형성하기 위하여 CVD 또는 ALD (atomic layer deposition) 방법을 이용할 수도 있다. 예를 들면, 상기 절연막(150)은 SiO2, SiON, Si3N4, GexOyNz또는 GexSiyOz로 이루어질 수도 있고, HfO2, ZrO2, Al2O3, TiO2, Ta2O5와 같은 금속 산화물로 구성되는 고유전 물질로 이루어질 수도 있다. 또한, 상기 절연막(150)은 상기 예시된 막질들 중에서 선택되는 2종 이상의 물질을 복수 층으로 적층하여 구성될 수도 있다. 이 때, 상기 제2 활성 영역(140a) 위에도 절연막이 형성될 수 있으나, 후속 공정에서 제거될 것이므로 문제되지 않는다.도 11을 참조하면, 상기 제2 활성 영역(140a) 및 상기 절연막(150) 위에 게이트 라인 형성을 위한 도전층(160)을 형성하고, 그 위에 마스크층(172) 및 포토레지스트막(174)을 형성한다. 상기 도전층(160)은 예를 들면 도전성 폴리실리콘막, 금속막, 금속 질화물막 또는 금속 실리사이드막으로 이루어질 수 있다. 상기 도전층(160)은 상기 절연막(150)을 사이에 두고 상기 슬랩(120)의 제1 측면(122), 제2 측면(124) 및 상면(126)을 모두 덮도록 형성된다. 상기 마스크층(172)은 예를 들면Si3N4막으로 이루어질 수 있으며, 경우에 따라 생략 가능하다.도 12를 참조하면, 상기 포토레지스트막(174)을 패터닝하여 게이트 라인이 형성될 영역을 덮는 포토레지스트 패턴(174a)을 형성한다.도 13을 참조하면, 상기 포토레지스트 패턴(174a)을 식각 마스크로 하여 상기 마스크층(172)의 노출된 부분을 식각하여 마스크 패턴(172a)을 형성한다. 그 결과, 상기 마스크 패턴(172a) 주위에서는 상기 도전층(160)이 일부 노출된다.도 14를 참조하면, 상기 포토레지스트 패턴(174a)을 제거하여 상기 마스크 패턴(172a)의 상면을 노출시킨다.도 15를 참조하면, 상기 마스크 패턴(172a)을 식각 마스크로 하여 상기 도전층(160)을 이방성 식각하여 게이트 라인(160a)을 형성한다. 여기서, 상기 마스크층(172)의 형성을 생략한 경우에는 상기 포토레지스트 패턴(174a)을 식각 마스크로 이용할 수 있다. 상기 게이트 라인(160a)은 각 슬랩(120)의 연장 방향과는 직교하는 방향으로 연장되어 있고, 상기 제2 활성 영역(140a)과는 평행한 방향으로 연장되어 있다. 상기 게이트 라인(160a)이 형성된 후, 상기 게이트 라인(160a)의 주위에는 상기 슬랩(120)을 덮고 있는 절연막(150)이 노출된다.도 16을 참조하면, 상기 마스크 패턴(172a)을 제거하여 상기 게이트 라인(160a)의 상면을 노출시킨다.도 17을 참조하면, 상기 슬랩(120)의 표면을 덮고 있는 절연막(150)을 제거한다. 이 때, 상기 제2 활성 영역(140a) 위에도 절연막이 형성되어 있다면 이 단계에서 상기 절연막(150)과 함께 제거된다. 그 결과, 상기 게이트 라인(160a)의 주위에서 각 슬랩(120)이 노출되고, 상기 슬랩(120)의 대략 중앙부에서는 그 제1 측면(122), 제2 측면(124) 및 상면(126)과 상기 게이트 라인(160a)과의 사이에 게이트 절연막(150a)이 남아 있게 된다.그 후, 통상의 방법에 의하여 상기 게이트 라인(160a)의 측벽에 절연 스페이서(도시 생략)를 형성하고, 소스/드레인 형성을 위한 이온 주입 공정 및 어닐링 공정을 행한다.도 18은 도 17의 XVIII - XVIII'선 단면도이고, 도 19는 도 17의 XIX - XIX'선 단면도이다.도 18에 도시된 바와 같이, 제1 활성 영역인 각 슬랩(120)의 제1 측면(122), 제2 측면(124) 및 상면(126)은 각각 상기 게이트 라인(160a)과 대면하고 있으며, 이들 사이에 상기 게이트 절연막(160)이 개재되어 있다. 또한, 상기 슬랩(120) 내부에는 상기 제1 측면(122), 제2 측면(124) 및 상면(126)에 근접하여 상기 게이트 라인(160a)과 대면하는 부분에 각각 제1 채널 영역(182), 제2 채널 영역(184) 및 제3 채널 영역(186)이 위치된다. 즉, 상기 슬랩(120)중 3개의 면에 각

각 채널이 형성되는 트리-게이트 구조가 구현된다. 그러나, 본 발명은 이에 한정되는 것은 아니며, 본 발명의 사상의 범위 내에서 단순한 공정 설계 변형을 통하여 FinFET 구조를 구현하는 것도 당 업자이면 용이하게 실시할 수 있다. FinFET 구조를 구현하는 경우에는 상기 슬랩(120) 내에서 제1 측면(122) 및 제2 측면(124) 근방에 각각 위치하는 상기 제1 채널 영역(182) 및 제2 채널 영역(184)에서만 채널이 형성된다.또한, 도 19에 도시된 바와 같이, 상기 매몰 산화막(110) 위에서 제1 활성 영역인 복수의 슬랩(120)을 상호 연결시키는 제2 활성 영역(140a)은 각 슬랩(120)의 양 단부(128)에 접해 있으며, 각 슬랩(120) 중 상기 제1 측면(122), 제2 측면(124) 및 상면(126)의 일부와 접하여 연장되어 있는 오버랩 영역(142)을 가진다. 도 19에 있어서, 상기 슬랩(120)의 양 단부(128) 중 한 단부의 끝 표면은 상기 제2 활성 영역(140a)에 의해 덮여 있고, 다른 단부의 끝 표면은 상기 제2 활성 영역(140a)에 의해 덮여 있지 않은 것으로 도시되어 있다.도 20 내지 도 22는 본 발명의 제2 실시예에 따른 반도체 소자의 제조 방법을 설명하기 위하여 공정 순서에 따라 도시한 부분 사시도들이다.제2 실시예는 제1 실시예와 대체로 동일하나, 제1 실시예와 다른 점은 제2 활성 영역(240)의 상면(242)이 슬랩(120)의 상면(126)과 동일한 레벨로 형성된다는 것이다. 도 20 내지 도 22에 있어서, 제1 실시예에서와 동일한 참조 부호는 동일 부재를 나타낸다.도 20을 참조하여 보다 상세히 설명하면, 도 2 내지 도 7을 참조하여 설명한 바와 같은 방법으로 매몰 산화막(110) 위에 슬랩(120), 마스크 패턴(130a) 및 반도체층(140)을 차례로 형성한 후, 상기 슬랩(120)의 상면(126)이 노출될 때까지 상기 반도체층(140) 및 마스크 패턴(130a)을 CMP 또는 에치백 방법에 의하여 평탄화하여 각 슬랩(120)의 양 단부(128) 및 그 주위를 덮는 제2 활성 영역(240)을 형성한다. 그 결과, 상기 슬랩(120)의 제1 측면(122) 및 제2 측면(124) 중 양 단부(128)가 상기 제2 활성 영역(240)에 의해 덮이게 되고, 상기 슬랩(120)의 상면(126)은 완전히노출된다. 상기 제2 활성 영역(240)을 통하여 제1 활성 영역인 각 슬랩(120)이 상호 연결된다. 그리고, 상기 매몰 산화막(110) 위에는 각 슬랩(120) 사이의 갭 영역에 상기 슬랩(120)과 대략 동일한 높이의 상면을 가지는 마스크 패턴(130b)이 남아 있게 된다.도 21을 참조하면, 애싱 및 습식 식각 공정에 의하여 상기 마스크 패턴(130b)을 제거한다. 그 결과, 상기 매몰 산화막(110) 위에서 제1 활성 영역인 복수의 슬랩(120)과 이들을 상호 연결시키는 제2 활성 영역(240)이 완전히 노출된다. 상기 제2 활성 영역(240)은 각 슬랩(120)의 양 단부(128)에 접하면서 상기 슬랩(120)의 연장 방향과 직교하는 방향으로 연장되어 있다. 또한, 상기 제2 활성 영역(240)은 각 슬랩(120) 중 상기 제1 측면(122) 및 제2 측면(124)의 일부와 접하여 연장되어 있는 오버랩 영역(242)을 가진다. 여기서, 각 슬랩(120)의 양 단부(128)에서 가장 끝 표면은 상기 제2 활성 영역(240)에 의해 덮일 수도 있고, 덮이지 않을 수도 있다. 도 21에 있어서, 각 슬랩(120) 중 도 21의 전방측에 있는 단부(128)의 끝 표면은 상기 제2 활성 영역(240)에 의하여 덮인 것으로 도시되어 있고, 도 21의 후방측에 있는 단부(128)의 끝 표면은 상기 제2 활성 영역(240)에 의하여 덮이지 않은 것으로 도시되어 있다.그리고, 상기 제2 활성 영역(240)의 상면은 상기 제1 활성 영역인 상기 슬랩(120)의 상면(126)과 대략 동일한 레벨을 가지며, 따라서 상기 실리콘 기판(100) 또는 상기 매몰 산화막(110)으로부터 상기 제2 활성 영역(240)까지의 거리는 상기 실리콘 기판(100) 또는 매몰 산화막(110)으로부터 상기 슬랩(120)의 상면(126)까지의 거리와 대략 같다.도 22를 참조하면, 도 10 내지 도 17을 참조하여 설명한 바와 같은 방법에 의하여 상기 슬랩(120)의 대략 중앙부에서 그 제1 측면(122), 제2 측면(124) 및 상면(126)을 덮는 게이트 절연막(150a)과, 상기 게이트 절연막(150a)을 사이에 두고 상기 슬랩(120)의 제1 측면(122), 제2 측면(124) 및 상면(126)과 대면하고 있는 게이트 라인(160a)을 형성한다.도 23은 도 22의 XXIII - XXIII'선 단면도이고, 도 24는 도 22의 XXIV - XXIV'선 단면도이다.도 23의 구성은 도 18에서와 대체로 동일하므로 상세한 설명은 생략한다.도 24에 도시된 바와 같이, 상기 매몰 산화막(110) 위에서 제1 활성 영역인 복수의 슬랩(120)을 상호 연결시키는 제2 활성 영역(240)은 각 슬랩(120)의 양 단부(128)에 접해 있으며, 각 슬랩(120) 중 상기 제1 측면(122) 및 제2 측면(124)의 일부와 접하여 연장되어 있다. 그리고, 상기 제2 활성 영역(240)의 상면은 제1 활성 영역인 상기 슬랩(120)의 상면(126)과 대략 동일한 레벨을 가진다. 도 24에 있어서, 상기 슬랩(120)의 양 단부(128) 중 한 단부의 끝 표면은 상기 제2 활성 영역(240)에 의해 덮여 있고, 다른 단부의 끝 표면은 상기 제2 활성 영역(240)에 의해 덮여 있지 않은 것으로 도시되어 있다.

본 발명에서는 멀티-게이트 트랜지스터 형성을 위한 활성 영역을 형성하는 데 있어서, OPC를 이용하는 리소그래피 공정 또는 식각 공정에서의 제어 한계에 따른 문제점을 해결하기 위하여, 먼저 라인 앤드 스페이스 패턴의 제1 활성 영역을 슬랩 형태로 형성한 후, 이어서 각 슬랩을 연결시키기 위한 제2 활성 영역을 형성한다. 본 발명에 따라 활성 영역을 각각 제1 활성 영역 및 제2 활성 영역으로 나누어 형성함으로써 디자인 룰 300nm 이하의 피치를 가지는 멀리-게이트 트랜지스터용 활성 영역을 형성할 때 리소그래피 공정시의 해상 한계에 따른 라운딩 현상 또는 "낫오픈" 현상에 의한 문제점들을 회피할 수 있으며, 활성 영역에서 CD 편차에 따른 문제를 개선할 수 있다. 또한, 게이트 라인 형성시 미스얼라인이 발생하더라도 트랜지스터의 특성 편차가 발생될 가능성이 현저히 줄어들게 된다. 따라서, 본 발명에 의하면 활성 영역의 재현성 있는 프로파일 및 CD 제어 가능성을 안정적으로 확보할 수 있으며, 멀티-게이트 트랜지스터에서 균일한 퍼포먼스 및 향상된 전기적 특성을 제공할 수 있는 반도체 소자를 구현할 수 있다.이상, 본 발명을 바람직한 실시예를 들어 상세하게 설명하였으나, 본 발명은 상기 실시예에 한정되지 않고, 본 발명의 기술적 사상 및 범위 내에서 당 분야에서 통상의 지식을 가진 자에 의하여 여러가지 변형 및 변경이 가능하다.

Espacenet

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SEMICONDUCTOR DEVICE HAVING MULTI-GATE STRUCTURE AND METHOD OF MANUFACTURING THE SAME

Claims of KR20050082099 (A)

A high quality text as facsimile in your desired language may be available amongst the following family members:

CN100472806 (C) DE112005000394 (T5) JP2007522683 (A) US2007272925 (A1) WO2005078804 (A1) DE112005000394 (B4) US2011033989 (A1)

- Original claims
- Claims tree

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1. 기판상에서 상호 반대 방향인 제1 측면 및 제2 측면과 상면을 각각 가지는 복수의 슬랩(slab)으로 구성되는 제1 활성 영역과,
상기 복수의 슬랩을 상호 연결시키도록 상기 기판상에서 상기 슬랩의 적어도 일단부에 접하여 연장되어 있는 제2 활성 영역과,
상기 슬랩의 적어도 제1 측면 및 제2 측면과 상면 위에 형성되어 있는 게이트 라인과,
상기 슬랩과 상기 게이트 라인과의 사이에 개재되어 있는 게이트 절연막을 포함하는 것을 특징으로 하는 반도체 소자.

2. 제1항에 있어서,
상기 제1 활성 영역은 라인 앤드 스페이스 패턴 (line and space pattern) 형상으로 형성된 것을 특징으로 하는 반도체 소자.

3. 제1항에 있어서,
상기 제2 활성 영역은 상기 제1 활성 영역과는 다른 물질로 이루어지는 것을 특징으로 하는 반도체 소자.

4. 제1항에 있어서,
상기 슬랩의 상면은 상기 기판으로부터 제1 거리 만큼 이격되어 있고,
상기 제2 활성 영역은 상기 기판으로부터 상기 제1 거리와 같거나 더 큰 제2 거리 만큼 이격되어 있는 상면을 가지는 것을 특징으로 하는 반도체 소자.

5. 제4항에 있어서,
상기 제2 거리는 상기 제1 거리 보다 더 큰 것을 특징으로 하는 반도체 소자.

6. 제4항에 있어서,
상기 제2 거리는 제1 거리와 같은 것을 특징으로 하는 반도체 소자.

7. 제1항에 있어서,
상기 제2 활성 영역은 상기 슬랩의 양 단부에 접해 있는 상태에서 상기 슬랩의 연장 방향과 직교하는 방향으로 연장되어 있는 것을 특징으로 하는 반도체 소자.

8. 제1항에 있어서,
상기 제2 활성 영역은 상기 슬랩 중 상기 제1 측면, 제2 측면 및 상면의 일부와 접하여 연장되어 있는 오버랩 영역을 가지는 것을 특징으로 하는 반도체 소자.

9. 제1항에 있어서,
상기 제1 활성 영역은 단결정 실리콘으로 이루어지고,
상기 제2 활성 영역은 폴리실리콘, 비정질 실리콘, 또는 실리콘을 함유하는 반도체 화합물로 이루어지는 것을 특징으로 하는 반도체 소자.

10. 제1항에 있어서,
상기 제1 활성 영역 및 제2 활성 영역은 소스/드레인 영역을 구성하는 것을 특징으로 하는 반도체 소자.

11. 제1항에 있어서,
상기 제1 활성 영역은 채널 영역을 포함하는 것을 특징으로 하는 반도체 소자.

12. 제1항에 있어서,
상기 게이트 라인은 상기 슬랩의 연장 방향과 직교하는 방향으로 연장되어 있는 것을 특징으로 하는 반도체 소자.

13. 제1항에 있어서,
상기 게이트 라인은 상기 제2 활성 영역의 연장 방향과 평행한 방향으로 연장되어 있는 것을 특징으로 하는 반도체 소자.

14. 제1항에 있어서,
상기 게이트 라인은 도전성 폴리실리콘, 금속, 금속 질화물 또는 금속 실리사이드로 이루어지는 것을 특징으로 하는 반도체 소자.

15. 제1항에 있어서,
상기 게이트 절연막은 SiO2, SiON, Si3N4, GexOyNz, GexSiyOz, HfO2, ZrO2, Al2O3, TiO2또는 Ta2O5을 포함하는 것을 특징으로 하는 반도체 소자.

16. 제1항에 있어서,
상기 기판은 매몰 산화막과 실리콘층을 포함하는 SOI 기판이고,
상기 제1 활성 영역 및 제2 활성 영역은 상기 매몰 산화막 위에 형성되어 있는 것을 특징으로 하는 반도체 소자.

17. 제1항에 있어서,
상기 제1 활성 영역 중 상기 슬랩의 제1 측면 및 제2 측면에 근접하여 상기 게이트 라인과 대면하는 부분에 각각 위치하는 제1 채널 영역 및 제2 채널 영역을 더 포함하는 것을 특징으로 하는 반도체 소자.

18. 제17항에 있어서,
상기 제1 활성 영역 중 상기 슬랩의 상면에 근접하여 상기 게이트 라인과 대면하는 부분

에 위치하는 제3 채널 영역을 더 포함하는 것을 특징으로 하는 반도체 소자.

19. 제1 물질로 이루어지는 제1 활성 영역을 기판 위에 형성하는 단계와,
상기 제1 활성 영역의 적어도 일부에 접하여 연장되고 제2 물질로 이루어지는 제2 활성 영역을 상기 기판 위에 형성하는 단계와,
상기 제1 활성 영역 위에 게이트 절연막을 형성하는 단계와,
상기 게이트 절연막 위에 게이트를 형성하는 단계를 포함하는 것을 특징으로 하는 반도체 소자의 제조 방법.

20. 제19항에 있어서,
상기 제1 활성 영역은 라인 앤드 스페이스 패턴 형상을 가지는 것을 특징으로 하는 반도체 소자의 제조 방법.

21. 제19항에 있어서,
상기 제2 물질은 상기 제1 물질과는 다른 물질인 것을 특징으로 하는 반도체 소자의 제조 방법.

22. 제19항에 있어서,
상기 제1 활성 영역을 형성하는 단계에서는 상호 반대 방향인 제1 측면 및 제2 측면과 상면을 각각 가지며 상기 기판상에 제1 방향으로 연장되는 복수의 슬랩(slab)을 형성하는 것을 특징으로 하는 반도체 소자의 제조 방법.

23. 제22항에 있어서,
상기 슬랩의 상면은 상기 기판으로부터 제1 거리 만큼 이격되고,
상기 제2 활성 영역은 상기 기판으로부터 상기 제1 거리와 같거나 더 큰 제2 거리 만큼 이격되어 있는 상면을 가지도록 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

24. 제22항에 있어서,
상기 제2 활성 영역은 상기 슬랩의 양 단부에 접하면서 상기 제1 방향과 직교하는 제2 방향으로 연장되도록 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

25. 제22항에 있어서,
상기 제2 활성 영역은 상기 슬랩 중 상기 제1 측면, 제2 측면 및 상면의 일부와 접하여 연장되어 있는 오버랩 영역을 가지도록 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

26. 제22항에 있어서,
상기 제2 활성 영역을 형성하는 단계는
상기 슬랩의 양 단부를 노출시키도록 상기 슬랩의 일부를 덮는 마스크 패턴을 상기 기판 위에 형성하는 단계와,
상기 제2 물질을 증착하여 상기 슬랩의 노출된 양 단부 및 상기 마스크 패턴을 덮는 제2 물질층을 형성하는 단계와,
상기 제2 물질층을 평탄화하여 상기 제2 활성 영역을 형성하는 단계를 포함하는 것을 특징으로 하는 반도체 소자의 제조 방법.

27. 제26항에 있어서,
상기 마스크 패턴은 SiON막, Si3N4막 또는 SiO2막으로 구성되는 단일막, 또는 이들의 조합으로 구성되는 다중막으로 이루어지는 것을 특징으로 하는 반도체 소자의 제조 방법.

28. 제27항에 있어서,
상기 마스크 패턴은 SiON막 및 Si3N4막으로 구성되는 이중막으로 이루어지는 것을 특

징으로 하는 반도체 소자의 제조 방법.

29. 제26항에 있어서,
상기 마스크 패턴이 형성된 후 상기 마스크 패턴 주위에서 상기 복수의 슬랩 각각의 상면이 일부 노출될 수 있도록 상기 마스크 패턴은 상기 슬랩의 상면 중 일부 만을 덮는 것을 특징으로 하는 반도체 소자의 제조 방법.

30. 제26항에 있어서,
상기 제2 물질층을 평탄화하는 데 있어서 상기 마스크 패턴을 식각 정지층으로 이용하는 것을 특징으로 하는 반도체 소자의 제조 방법.

31. 제30항에 있어서,
상기 마스크 패턴은 상기 슬랩에 접해있는 SiON막과, 상기 마스크 패턴의 상면을 구성하는 Si3N4막을 포함하는 것을 특징으로 하는 반도체 소자의 제조 방법.

32. 제26항에 있어서,
상기 제2 물질층을 평탄화하기 위하여 CMP (chamical mechanical polishing) 또는 에치백(etchback) 방법을 이용하는 것을 특징으로 하는 반도체 소자의 제조 방법.

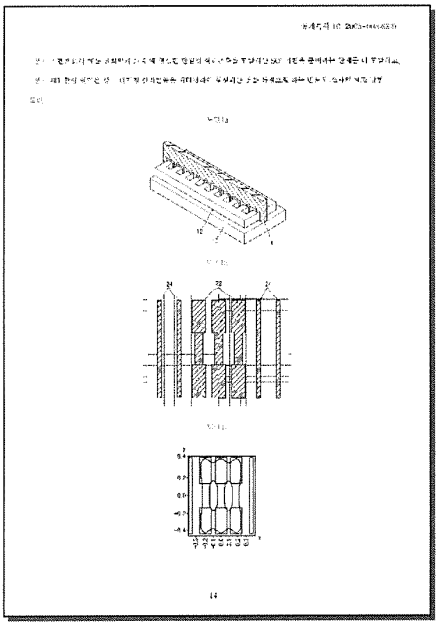
33. 제19항에 있어서,
상기 제1 물질은 단결정 실리콘이고,
상기 제2 물질은 폴리실리콘, 비정질 실리콘, 또는 실리콘을 함유하는 반도체 화합물로 이루어지는 것을 특징으로 하는 반도체 소자의 제조 방법.

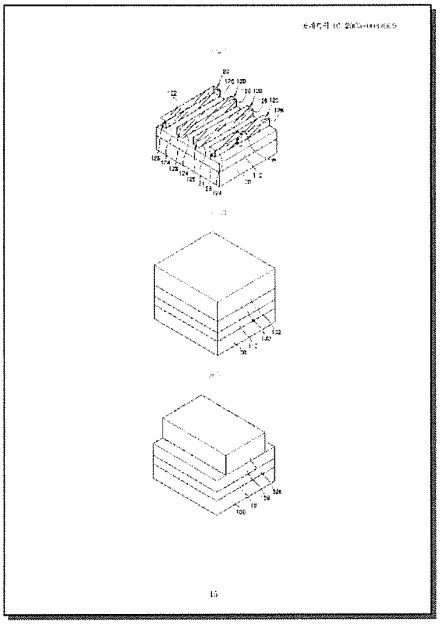
34. 제19항에 있어서,
상기 게이트 절연막은 SiO2, SiON, Si3N4, GexOyNz, GexSiyOz, HfO2, ZrO2, Al2O3, TiO2또는 Ta2O5을 포함하는 것을 특징으로 하는 반도체 소자의 제조 방법.

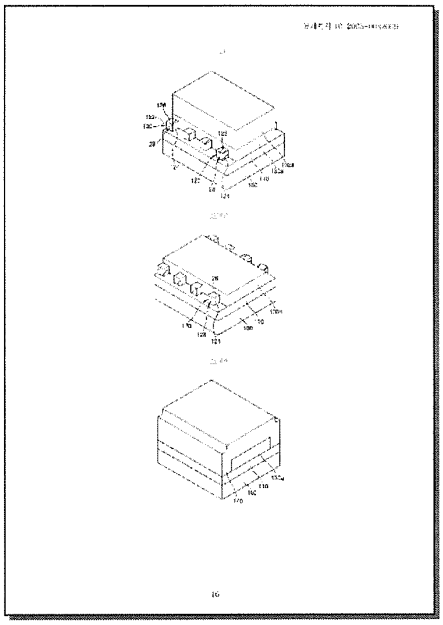
35. 제22항에 있어서,
상기 게이트를 형성하기 위하여 상기 슬랩 중 상기 제1 측면, 제2 측면 및 상면을 덮도록 상기 제1 방향과 직교하는 제2 방향으로 연장되는 게이트 라인을 형성하는 것을 특징으로 하는 반도체 소자의 제조 방법.

36. 제35항에 있어서,
상기 게이트 라인은 도전성 폴리실리콘, 금속, 금속 질화물 또는 금속 실리사이드로 이루어지는 것을 특징으로 하는 반도체 소자의 제조 방법.

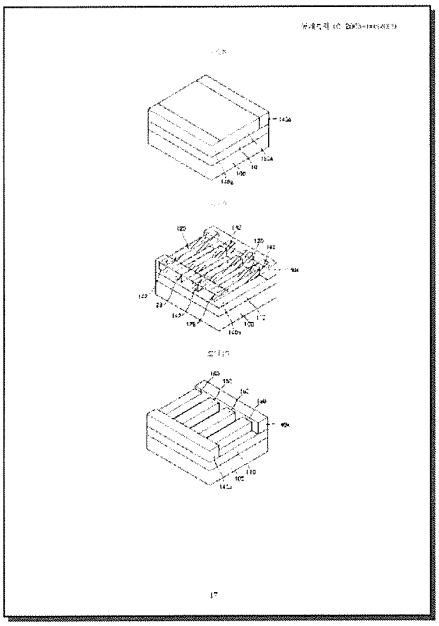
37. 제19항에 있어서,
상기 기판으로서 매몰 산화막과 그 위에 형성된 단결정 실리콘층을 포함하는 SOI 기판을 준비하는 단계를 더 포함하고,
상기 제1 활성 영역은 상기 단결정 실리콘층을 패터닝하여 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

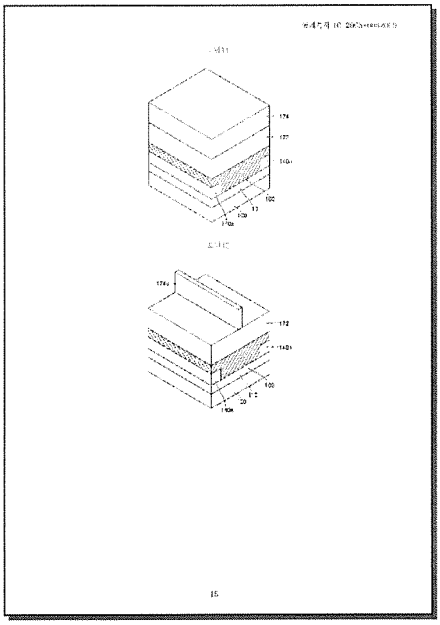


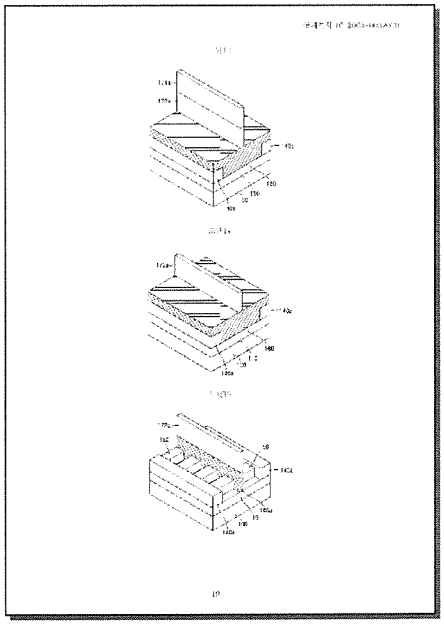


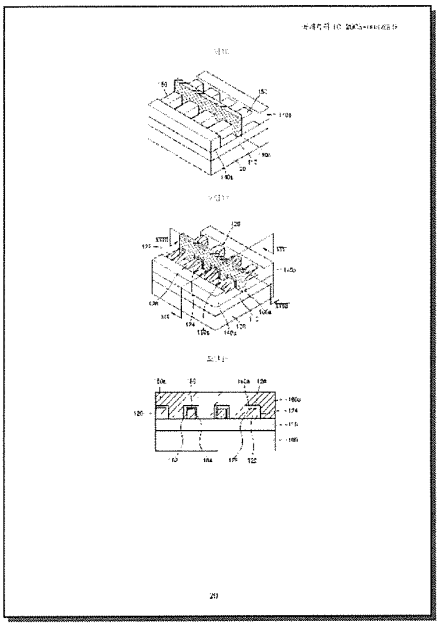


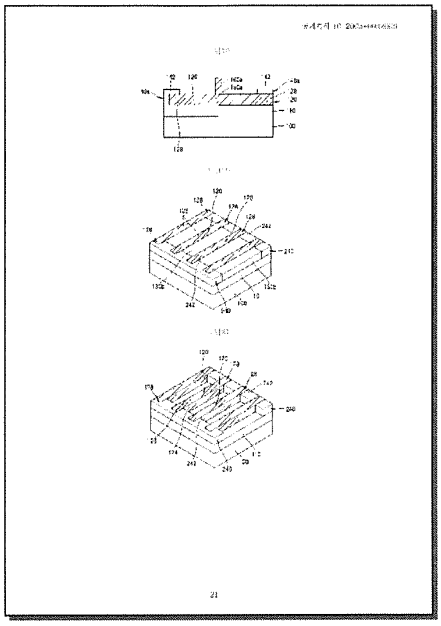
Drawing pages of KR20050082099 A

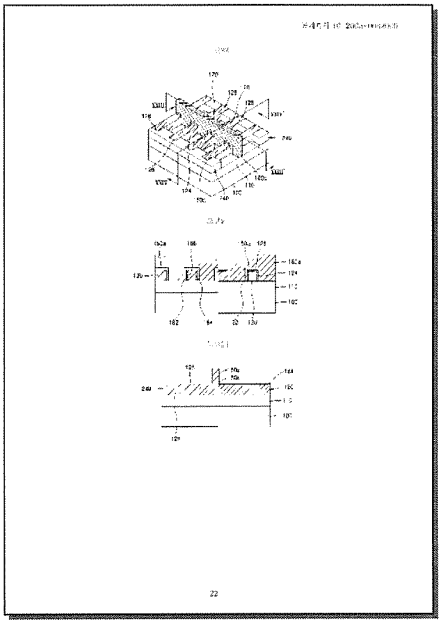












Drawing pages of KR20050082099 A

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application No.	Herewith
	Filing Date	
	First Inventor	Milton C. WEBB, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket No.	42P60397US Conf. No.

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted concurrently with the . It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature		Date (MM-DD-YYYY)	03-24-2016
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Robert S. Caldwell /Robert S. Caldwell/ *Date* *03-24-16*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	Unknown
	Filing Date	December 19, 2013
	First Named Inventor	Webb, M.
	Group Art Unit	0
	Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No: P60397US	

US PATENT DOCUMENTS					
Examiner Initial*	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-2007/0054464	03/08/2007	ZHANG, Guowei	
		US-2008/0080380	04/03/2008	LEE, Kwang il, et al.	
		US-20110021027	01/27/2011	JOHNSON, Frank S.	
		US-2013/0020615	01/24/2013	FAN, Su Chen, et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**
		KR-20050082099		CHOI, Jung A., et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		International Search Report and Written Opinion from PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) Mailed September 26, 2014, 10 pages.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same
First Named Inventor/Applicant Name:	Milton C. WEBB
Filer:	Justin K. Brask/Robert Caldwell
Attorney Docket Number:	P60397US

Filed as Large Entity

Filing Fees for U.S. National Stage under 35 USC 371

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
National Stage Fee	1631	1	280	280
Natl Stage Search Fee - Report provided	1642	1	480	480
National Stage Exam - all other cases	1633	1	720	720
Pages:				
Claims:				
Claims in excess of 20	1615	5	80	400
Independent claims in excess of 3	1614	1	420	420
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2300**

Electronic Acknowledgement Receipt	
EFS ID:	25299807
Application Number:	15024750
International Application Number:	PCT/US2013/076673
Confirmation Number:	9490
Title of Invention:	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same
First Named Inventor/Applicant Name:	Milton C. WEBB
Customer Number:	45209
Filer:	Justin K. Brask
Filer Authorized By:	
Attorney Docket Number:	P60397US
Receipt Date:	24-MAR-2016
Filing Date:	
Time Stamp:	17:07:12
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2300
RAM confirmation Number	4203
Deposit Account	504238
Authorized User	BRASK, JUSTIN
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 CFR 1.492 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

Charge any Additional Fees required under 37 CFR 1.492(a) (basic national fee only)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	P60397US_National_Phase_Transmittal_Letter_Filed_3_24_16.pdf	223292 d2f47a009bb2653f0eb53ae117fa9a9fd8ab7bf4	no	4
Warnings:					
Information:					
2	Application Data Sheet	P60397US_ADS_Filed_3_24_16.pdf	1793077 3feae284afd7536d50188144c6915bb716057936	no	9
Warnings:					
Information:					
3		P60397US_Prelim_Amend_Filed_3_24_16.pdf	155570 dc4a21da8d2c404da964b981a70b1c72eb6b230a	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Preliminary Amendment		1	1	
	Specification		2	2	
	Applicant Arguments/Remarks Made in an Amendment		3	3	
Warnings:					
Information:					
4	Documents submitted with 371 Applications	WO2015094305.pdf	7657531 601eedf5ecfa3707a8085834bf5c80c8fcc40393	no	58
Warnings:					
Information:					
5	Documents submitted with 371 Applications	P60397PCT_ISRWO_092614.pdf	1414229 0db2e7eb2c8252d771bdd1e8037a3bc93b6ecaf9	no	10
Warnings:					
Information:					
6	Oath or Declaration filed	42P60397PCT_DEC_EXECUTED.pdf	1608859 7e8e0746f71dc90b34052b870160b25adbf5c4f4	no	4

Warnings:					
Information:					
7	Foreign Reference	KR20050082099.pdf	1090970 1d25d16fb1e3835ea755b50093f557cf79e03cc1	no	15
Warnings:					
Information:					
8		P60397US_IDS_Filed_3_24_16.pdf	110659 266683e94e01b3de9144fad0505f92a7420926d4	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	38635 8af41b62ee5aa897b4b16267ea1b3cf850ce6d39	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	14092822		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO-1390 (06-13)
Approved for use through 6/30/2013. OMB 0651-0021
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371		Attorney Docket No. P60397US U.S. Application No. (if known, see 37 CFR 1.5) NEW
International Application No. PCT/US2013/076673	International Filing Date 12/19/2013	Priority Date Claimed 12/19/2013

Title of Invention
Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same

First Named Inventor
WEBB, Milton C.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. ☑ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). NOTE: The express request under 35 U.S.C. 371(f) will not be effective unless the requirements under 35 U.S.C. 371(c)(1), (2), and (4) for payment of the basic national fee, copy of the International Application and English translation thereof (if required), and the oath or declaration of the inventor(s) have been received.
2. ☑ A copy of the International Application (35 U.S.C. 371(c)(2)) is attached hereto (not required if the International Application was previously communicated by the International Bureau or was filed in the United States Receiving Office (RO/US)).
3. An English language translation of the International Application (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
4. An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4))
   a. ☑ is attached.
   b. ☑ was previously filed in the international phase under PCT Rule 4.17(iv).

Items 5 to 8 below concern amendments made in the international phase.

PCT Article 19 and 34 amendments

5. ☐ Amendments to the claims under PCT Article 19 are attached (not required if communicated by the International Bureau) (35 U.S.C. 371(c)(3)).
6. ☐ English translation of the PCT Article 19 amendment is attached (35 U.S.C. 371(c)(3)).
7. ☐ English translation of annexes (Article 19 and/or 34 amendments only) of the International Preliminary Examination Report is attached (35 U.S.C. 371(c)(5)).

Cancellation of amendments made in the international phase

8a. ☐ Do not enter the amendment made in the international phase under PCT Article 19.

8b. ☐ Do not enter the amendment made in the international phase under PCT Article 34.

NOTE: A proper amendment made in English under Article 19 or 34 will be entered in the U.S. national phase application absent a clear instruction from applicant not to enter the amendment(s).

The following items 9 to 17 concern a document(s) or information included.

9. ☑ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
10. ☑ A preliminary amendment.
11. ☑ An Application Data Sheet under 37 CFR 1.76.
12. ☐ A substitute specification. NOTE: A substitute specification cannot include claims. See 37 CFR 1.125(b).
13. ☐ A power of attorney and/or change of address letter.
14. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.3 and 37 CFR 1.821-1.825.
15. ☐ Assignment papers *(cover sheet and document(s))*. Name of Assignee: _____
16. ☐ 37 CFR 3.73(c) Statement *(when there is an Assignee)*.

This collection of information is required by 37 CFR 1.414 and 1.491-1.492. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO-1390 (06-13)
Approved for use through 6/30/2013. OMB 0651-0021
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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U.S. APPLN. No. (if known – see 37 CFR 1.5)	INTERNATIONAL APPLICATION No.	ATTORNEY DOCKET No.
NEW	PCT/US2013/076673	P60397US

17. ☑ Other items or information:

WO2015094305; ISRWO

The following fees have been submitted.	CALCULATIONS	PTO USE ONLY
18. ☑ Basic national fee (37 CFR 1.492(a)) **$280**	$ 280	
19. ☑ Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** All other situations **$720**	$ 720	
20. ☑ Search fee (37 CFR 1.492(b)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority .....**$120** International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB .....**$480** All other situations **$600**	$ 480	
TOTAL OF 18, 19, and 20 =	$ 1480	
☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) in an electronic medium or computer program listing in an electronic medium) (37 CFR 1.492(j)). Fee for each additional 50 sheets of paper or fraction thereof **$400**		

Total Sheets	Extra Sheets	Number of each addition 50 or fraction thereof (round **up** to a whole number)	RATE	
- 100 =	/ 50 =		x **$400**	$
Surcharge of **$140.00** for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).				$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	25 - 20 =	5	x **$80**	$ 400	
Independent claims	4 - 3 =	1	x **$420**	$ 420	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			**+ $780**	$	
Processing fee of **$140.00** for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)). +				$	
TOTAL OF ABOVE CALCULATIONS =				$ 820	
☐ **Applicant asserts small entity status.** See 37 CFR 1.27. Fees above are reduced by ½.					
☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Fees above are reduced by ¾. Applicant must attach form PTO/SB/15A or B or equivalent.					
TOTAL NATIONAL FEE =				$ 2300	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property. +				$	
TOTAL FEES ENCLOSED =				$ 2300	
				Amount to be refunded:	$
				Amount to be charged:	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☑ Please charge my Deposit Account No. 504238 in the amount of $2300.00 to cover the above fees.

c. ☑ The Director is hereby authorized to charge additional fees which may be required, or credit any overpayment, to Deposit Account No. 504238 as follows:

i. ☐ any required fee.

ii. ☑ any required fee except for excess claims fees required under 37 CFR 1.492(d) and (e) and multiple dependent claim fee required under 37 CFR 1.492(f).

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. The PTO-2038 should only be mailed or faxed to the USPTO. However, when paying the basic national fee, the PTO-2038 may NOT be faxed to the USPTO.

ADVISORY: If filing by EFS-Web, do **NOT** attach the PTO-2038 form as a PDF along with your EFS-Web submission. Please be advised that this is **not** recommended and by doing so your **credit card information may be displayed via PAIR**. To protect your information, it is recommended to pay fees online by using the electronic payment method.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File)Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013, and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE 1: By providing this statement under 37 CFR 1.55 or 1.78, **this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA**.

NOTE 2: A U.S. national stage application may not claim priority to the international application of which it is the national phase. The filing date of a U.S. national stage application is the international filing date. See 35 U.S.C. 363.

Correspondence Address

☑ The address associated with Customer Number: 45209 **OR** ☐ Correspondence address below

Name	Justin K. Brask, BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP				
Address	1279 Oakmead Parkway				
City	Sunnyvale	State	CA	Zip Code	94085
Country	U.S.A.	Telephone	(408)720-8300		
Email	intel_foreign_docs@bstz.com				

Signature	/Justin K. Brask/	Date	3/24/16
Name (Print/Type)	Justin K. Brask	Registration No. (Attorney/Agent)	61,080

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Milton	C.	WEBB	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Aloha	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	20180 SW Inglis Drive		
Address 2			
City	Aloha	State/Province	OR
Postal Code	97007	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Mark		BOHR	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Aloha	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	19475 SW Suncrest Lane		
Address 2			
City	Aloha	State/Province	OR
Postal Code	97007	Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tahir		GHANI	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	14191 NW Stonebridge Drive		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country	US

Inventor 4 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Szuya	S.	LIAO	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Hillsboro	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	7214 NE Shaleen Street		
Address 2			
City	Hillsboro	State/Province	OR
Postal Code	97124	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	45209		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same		
Attorney Docket Number	P60397US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	Suggested Figure for Publication (if any)	

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	45209		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	a 371 of international	PCT/US13/76673	2013-12-19

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☐

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Applicant:

Address 1	2200 Mission College Boulevard		
Address 2			
City	Santa Clara	**State/Province**	CA
Country	US	Postal Code	95054
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Justin K. Brask/			Date (YYYY-MM-DD)	2016-03-24
First Name	Justin K.	Last Name	Brask	Registration Number	61080

Additional Signature may be generated within this form by selecting the Add button. Add

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US
	Application Number	
Title of Invention	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Box No. VIII (iv) DECLARATION: INVENTORSHIP (only for the purposes of the designation of the United States of America)
The declaration must conform to the following standardized wording provided for in Section 214; see Notes to Boxes Nos. VIII, VIII (i) to (v) (in general) and the specific Notes to Box No.VIII (iv). If this Box is not used, this sheet should not be included in the request.

Declaration of Inventorship (Rules 4.17(iv) and 51*bis*.1(a)(iv)) for the purposes of the designation of the United States of America:

I hereby declare that I believe I am the original or an original joint inventor of a claimed invention in the application.

This declaration is directed to the international application of which it forms a part (if filing declaration with application).

This declaration is directed to international application No. PCT/US13/076673 (if furnishing declaration pursuant to Rule 26*ter*).

I hereby declare that the above-identified international application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Name: Milton Clair WEBB

Residence: Aloha, OR US
(City and either US state, if applicable, or country)
Mailing Address: 20180 SW Inglis Drive

Aloha, OR 97007 US

Inventor's Signature Milton Clair Webb Date 3/24/14
(The signature must be that of the inventor, not that of the agent)

Name: Mark BOHR

Residence: Aloha, OR US
(City and either US state, if applicable, or country)
Mailing Address: 19475 SW Suncrest Lane

Aloha, OR 97007 US

Inventor's Signature Date
(The signature must be that of the inventor, not that of the agent)

Name: Tahir GHANI

Residence: Portland, OR US
(City and either US state, if applicable, or country)
Mailing Address: 14191 NW Stonebridge Drive

Portland, OR 97229 US

Inventor's Signature Date
(The signature must be that of the inventor, not that of the agent)

Name: Szuya S. LIAO

Residence: Hillsboro, OR US
(City and either US state, if applicable, or country)

Mailing Address: 7214 NE Shaleen St

Hillsboro, OR 97124 US

Inventor's Signature _____ Date _____
(The signature must be that of the inventor, not that of the agent)

Name: _____

Residence: _____
(City and either US state, if applicable, or country)

Mailing Address: _____

Inventor's Signature _____ Date _____
(The signature must be that of the inventor, not that of the agent)

Name: _____

Residence: _____
(City and either US state, if applicable, or country)

Mailing Address: _____

Inventor's Signature _____ Date _____
(The signature must be that of the inventor, not that of the agent)

Name: _____

Residence: _____
(City and either US state, if applicable, or country)

Mailing Address: _____

Inventor's Signature _____ Date _____
(The signature must be that of the inventor, not that of the agent)

Name: _____

Residence: _____
(City and either US state, if applicable, or country)

Mailing Address: _____

Inventor's Signature _____ Date _____
(The signature must be that of the inventor, not that of the agent)

Box No. VIII (iv) DECLARATION: INVENTORSHIP (only for the purposes of the designation of the United States of America)
The declaration must conform to the following standardized wording provided for in Section 214; see Notes to Boxes Nos. VIII, VIII (i) to (v) (in general) and the specific Notes to Box No. VIII (iv). If this Box is not used, this sheet should not be included in the request.

Declaration of Inventorship (Rules 4.17(iv) and 51*bis*.1(a)(iv)) for the purposes of the designation of the United States of America:

I hereby declare that I believe I am the original or an original joint inventor of a claimed invention in the application.

This declaration is directed to the international application of which it forms a part (if filing declaration with application).

This declaration is directed to international application No. PCT/US13/076673 (if furnishing declaration pursuant to Rule 26*ter*).

I hereby declare that the above-identified international application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Name: Milton Clair WEBB

Residence: Aloha, OR US
(City and either US state, if applicable, or country)
Mailing Address: 20180 SW Inglis Drive

Aloha, OR 97007 US

Inventor's Signature ..... Date .....
(The signature must be that of the inventor, not that of the agent)

Name: Mark BOHR

Residence: Aloha, OR US
(City and either US state, if applicable, or country)
Mailing Address: 19475 SW Suncrest Lane

Aloha, OR 97007 US

Inventor's Signature Mark Bohr Date 3/24/14
(The signature must be that of the inventor, not that of the agent)

Name: Tahir GHANI

Residence: Portland, OR US
(City and either US state, if applicable, or country)
Mailing Address: 14191 NW Stonebridge Drive

Portland, OR 97229 US

Inventor's Signature Tahir Date 3-18-14
(The signature must be that of the inventor, not that of the agent)

Name: Szuya S. LIAO

Residence: Hillsboro, OR US
(City and either US state, if applicable, or country)
Mailing Address: 7214 NE Shaleen St.

Hillsboro, OR 97124 US

Inventor's Signature [signature] Date 3-18-2014
(The signature must be that of the inventor, not that of the agent)

Name:

Residence:
(City and either US state, if applicable, or country)
Mailing Address:

Inventor's Signature Date
(The signature must be that of the inventor, not that of the agent)

Name:

Residence:
(City and either US state, if applicable, or country)
Mailing Address:

Inventor's Signature Date
(The signature must be that of the inventor, not that of the agent)

Name:

Residence:
(City and either US state, if applicable, or country)
Mailing Address:

Inventor's Signature Date
(The signature must be that of the inventor, not that of the agent)

Name:

Residence:
(City and either US state, if applicable, or country)
Mailing Address:

Inventor's Signature Date
(The signature must be that of the inventor, not that of the agent)

PCT REQUEST

Original (for **SUBMISSION**)

0	**For receiving Office use only**	
0-1	International Application No.	PCT/US13/76673
0-2	International Filing Date	19 DEC 2013 19-12-2013
0-3	Name of receiving Office and "PCT International Application"	PCT International Application RO/US

0-4	**Form PCT/RO/101 PCT Request**	
0-4-1	Prepared Using	PCT-SAFE [EASY/EFS-Web mode] Version 3.51.060.236 MT/FOP 20131001/0.20.5.21
0-5	**Petition** The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	United States Patent and Trademark Office (USPTO) (RO/US)
0-7	**Applicant's or agent's file reference**	42P60397PCT
I	**Title of Invention**	Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same
II	**Applicant**	
II-1	This person is	Applicant only
II-2	Applicant for	All designated States
II-4	Name	INTEL CORPORATION
II-5	Address	2200 Mission College Boulevard MS: RNB-4-150 Santa Clara, California 95054 United States of America
II-6	State of nationality	US
II-7	State of residence	US
III-1	**Applicant and/or inventor**	
III-1-1	This person is	Applicant and inventor
III-1-2	Applicant for	All designated States
III-1-4	Name (LAST, First)	WEBB, MILTON CLAIR
III-1-5	Address	20180 SW Inglis Drive Aloha, Oregon 97007 United States of America
III-1-6	State of nationality	US
III-1-7	State of residence	US

PCT REQUEST

Original (for **SUBMISSION**)

III-2	**Applicant and/or inventor**	
III-2-1	This person is	**Applicant and inventor**
III-2-2	Applicant for	**All designated States**
III-2-4	Name (LAST, First)	**BOHR, MARK**
III-2-5	Address	**19475 SW Suncrest Lane Aloha, Oregon 97007 United States of America**
III-2-6	State of nationality	**US**
III-2-7	State of residence	**US**
III-3	**Applicant and/or inventor**	
III-3-1	This person is	**Applicant and inventor**
III-3-2	Applicant for	**All designated States**
III-3-4	Name (LAST, First)	**GHANI, TAHIR**
III-3-5	Address	**14191 NW Stonebridge Drive Portland, Oregon 97229 United States of America**
III-3-6	State of nationality	**US**
III-3-7	State of residence	**US**
III-4	**Applicant and/or inventor**	
III-4-1	This person is	**Applicant and inventor**
III-4-2	Applicant for	**All designated States**
III-4-4	Name (LAST, First)	**LIAO, SZUYA S.**
III-4-5	Address	**7214 NE Shaleen St. Hillsboro, Oregon 97124 United States of America**
III-4-6	State of nationality	TAIWAN
III-4-7	State of residence	**US**

PCT REQUEST

Original (for **SUBMISSION**)

IV-1	**Agent or common representative; or address for correspondence**	
	The person identified below is hereby/ has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	Agent
IV-1-1	Name (LAST, First)	BRASK, Justin K.
IV-1-2	Address	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279 Oakmead Parkway Sunnyvale, California 94085-4040 United States of America
IV-1-3	Telephone No.	(408) 720-8300
IV-1-4	Facsimile No.	(408) 720-8383
IV-1-5	e-mail	Intel_Foreign_Docs@bstz.com
IV-1-5(a)	E-mail authorization The receiving Office, the International Searching Authority, the International Bureau and the International Preliminary Examining Authority are authorized to use this e-mail address, if the Office or Authority so wishes, to send notifications issued in respect of this international application:	as advance copies followed by paper notifications
IV-1-6	Agent's registration No.	61,080
IV-2	**Additional agent(s)**	Agent
IV-2-1	Name (LAST, First)	MALLIE, Michael J.
IV-2-2	Address	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279 Oakmead Parkway Sunnyvale, California 94085-4040 United States of America
IV-2-3	Telephone No.	(408) 720-8300
IV-2-4	Facsimile No.	(408) 720-8383
IV-2-5	e-mail	Intel_Foreign_Docs@BSTZ.com
IV-2-5(a)	E-mail authorization The receiving Office, the International Searching Authority, the International Bureau and the International Preliminary Examining Authority are authorized to use this e-mail address, if the Office or Authority so wishes, to send notifications issued in respect of this international application:	as advance copies followed by paper notifications
IV-2-6	Agent's registration No.	36,591

PCT REQUEST

Original (for **SUBMISSION**)

IV-3	**Additional agent(s)**	**Agent**
IV-3-1	Name (LAST, First)	**VINCENT, Lester J.**
IV-3-2	Address	**BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279 Oakmead Parkway Sunnyvale, California 94085-4040 United States of America**
IV-3-3	Telephone No.	**(408) 720-8300**
IV-3-4	Facsimile No.	**(408) 720-8383**
IV-3-5	e-mail	**Intel_Foreign_Docs@BSTZ.com**
IV-3-5(a)	E-mail authorization The receiving Office, the International Searching Authority, the International Bureau and the International Preliminary Examining Authority are authorized to use this e-mail address, if the Office or Authority so wishes, to send notifications issued in respect of this international application:	**as advance copies followed by paper notifications**
IV-3-6	Agent's registration No.	**31,460**
IV-4	**Additional agent(s)**	**Agent**
IV-4-1	Name (LAST, First)	**NICHOLSON, David F.**
IV-4-2	Address	**BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 1279 Oakmead Parkway Sunnyvale, California 94085-4040 United States of America**
IV-4-3	Telephone No.	**(408) 720-8300**
IV-4-4	Facsimile No.	**(408) 720-8383**
IV-4-5	e-mail	**Intel_Foreign_Docs@BSTZ.com**
IV-4-5(a)	E-mail authorization The receiving Office, the International Searching Authority, the International Bureau and the International Preliminary Examining Authority are authorized to use this e-mail address, if the Office or Authority so wishes, to send notifications issued in respect of this international application:	**as advance copies followed by paper notifications**
IV-4-6	Agent's registration No.	**62,888**
V	**DESIGNATIONS**	
V-1	**The filing of this request constitutes under Rule 4.9(a), the designation of all Contracting States bound by the PCT on the international filing date, for the grant of every kind of protection available and, where applicable, for the grant of both regional and national patents.**	
VI-1	**Priority Claim**	**NONE**
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VIII-2	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent	–	
VIII-3	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	–	
VIII-4	Declaration of inventorship (only for the purposes of the designation of the United States of America)	–	
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IX-3	Claims	7	–
IX-4	Abstract	1	✓
IX-5	Drawings	15	–
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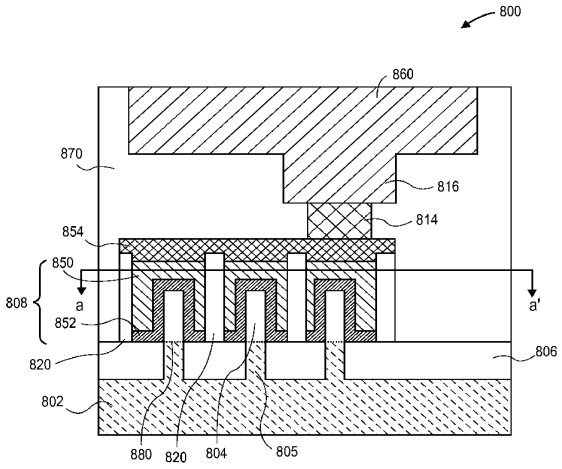


FIG. 8A

(57) **Abstract**: Self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures are described. In an example, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length in a first direction. A gate structure is disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction. A pair of gate edge isolation structures is centered with the semiconductor fin. A first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

WO 2015/094305 A1

Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same

TECHNICAL FIELD

[0001] Embodiments of the invention are in the field of semiconductor devices and processing and, in particular, self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures.

BACKGROUND

[0002] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

[0003] In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes, tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and because they enable a less complicated tri-gate fabrication process.

[0004] Scaling multi-gate transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of fundamental building blocks fabricated in a given region is increased, the constraints on the lithographic processes used to pattern these building blocks have become overwhelming. In particular, there may be a trade-off between the smallest dimension of a feature patterned in a semiconductor stack (the critical dimension) and the spacing between such features.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 illustrates a plan view of a layout including fin-based semiconductor devices accommodating end-to-end spacing.

[0006] Figures 2A-2D illustrate cross-sectional views of process operations of significance in a conventional finFET or tri-gate process fabrication scheme.

[0007] Figures 3A-3D illustrate cross-sectional views of process operations of significance in a self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with an embodiment of the present invention.

[0008] Figures 4A-4G illustrate cross-sectional views and corresponding top views of process operations in another self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with another embodiment of the present invention.

[0009] Figure 5A illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a pitch division patterned local interconnect (LI), in accordance with one embodiment of the present invention.

[0010] Figure 5B illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a self-aligned local interconnect (SAGELI), in accordance with another embodiment of the present invention.

[0011] Figures 6A-6H illustrate angled, three-dimensional cross-sectional views of various operations in the fabrication of self-aligned gate endcaps, in accordance with an embodiment of the present invention.

[0012] Figures 7A-7D illustrate angled, three-dimensional cross-sectional views of various structural options for providing a foundation for local interconnect fabrication, in accordance with an embodiment of the present invention.

[0013] Figure 8A illustrates a cross-sectional view of a non-planar semiconductor device having self-aligned gate edge isolation, in accordance with an embodiment of the present invention.

[0014] Figure 8B illustrates a plan view taken along the a-a' axis of the semiconductor device of Figure 8A, in accordance with an embodiment of the present invention.

[0015] Figure 9 illustrates a computing device in accordance with one implementation of the invention.

DESCRIPTION OF THE EMBODIMENTS

[0016] Self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0017] One or more embodiments of the present invention are directed to semiconductor structures or devices having one or more gate edge structures (e.g., as gate isolation regions) of gate electrodes of the semiconductor structures or devices. One or more embodiments are directed to the fabrication of local interconnects for such gate electrode structures. Additionally, methods of fabricating gate edge isolation structures in a self-aligned manner and/or methods of fabricating local interconnects are also described. In one or more embodiments, self-aligned gate edge structures and/or local interconnects are fabricated for logic transistors based on complementary metal oxide semiconductor (CMOS) devices.

[0018] To provide context, scaling of gate endcap and trench contact (TCN) endcap regions are important contributors towards improving transistor layout area and density. Gate and TCN endcap regions refer to gate and TCN overlap of the

diffusion region/fins of semiconductor devices. As an example, Figure 1 illustrates a plan view of a layout 100 including fin-based semiconductor devices accommodating end-to-end spacing. Referring to Figure 1, first 102 and second 104 semiconductor devices are based on semiconductor fins 106 and 108, respectively. Each device 102 and 104 has a gate electrode 110 or 112, respectively. Additionally, each device 102 and 104 has trench contacts (TCNs) 114 and 116, respectively, at source and drain regions of the fins 106 and 108, respectively. The gate electrodes 110 and 112 and the TCNs 114 and 116 each have an end cap region, which is located off of the corresponding fins 106 and 108, respectively.

[0019] Referring again to Figure 1, typically, gate and TCN endcap dimensions must include an allowance for mask registration error to ensure robust transistor operation for worst case mask mis-registration, leaving an end-to-end spacing 118. Thus, another important design rule critical to improving transistor layout density is the spacing between two adjacent endcaps facing each other. However, the parameters of "*2*Endcap + End-to-End Spacing*" are becoming increasingly difficult to scale using lithographic patterning to meet the scaling requirements for new technologies. In particular, the additional endcap length required to allow for mask registration error also increases gate capacitance values due to longer overlap length between TCN and gate electrodes, thereby increasing product dynamic energy consumption and degrading performance. Previous solutions have focused on improving registration budget and patterning or resolution improvements to enable shrinkage of both endcap dimension and endcap-to-endcap spacing.

[0020] In accordance with an embodiment of the present invention, approaches are described which provide for self-aligned gate endcap and TCN overlap of a semiconductor fin without any need to allow for mask registration. In one such embodiment, a disposable spacer is fabricated on the semiconductor fin edges which determines the gate endcap and the contact overlap dimensions. The spacer defined endcap process enables the gate and TCN endcap regions to be self-aligned to the semiconductor fin and, therefore, does not require extra endcap length to account for mask mis-registration. Furthermore, approaches described herein do not require lithographic patterning at previously required stages since the gate and TCN endcap/overlap dimensions remain fixed, leading to improvement (i.e., reduction) in device to device variability in electrical parameters.

[0021] In order to provide a side-by-side comparison, Figures 2A-2D illustrate cross-sectional views of process operations of significance in a conventional finFET or tri-gate process fabrication scheme, while Figures 3A-3D illustrate cross-sectional views of process operations of significance in a self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with an embodiment of the present invention.

[0022] Referring to Figures 2A and 3A, a bulk semiconductor substrate 200 or 300, such as a bulk single crystalline silicon substrate is provided having fins 202 or 302, respectively, etched therein. In an embodiment, the fins are formed directly in the bulk substrate 200 or 300 and, as such, are formed continuous with the bulk substrate 200 or 300. It is to be appreciated that within the substrate 200 or 300, shallow trench isolation structures may be formed between fins. Referring to Figure 3A, a hardmask layer 304, such as a silicon nitride hardmask layer, and a pad oxide

layer 306, such as a silicon dioxide layer, remain atop fins 302 following patterning to form the fins 302. By contrast, referring to Figure 2A, such a hardmask layer and pad oxide layer have been removed.

[0023] Referring to Figure 2B, a dummy or permanent gate dielectric layer 210 is formed on the exposed surfaces of the semiconductor fins 202, and a dummy gate layer 212 is formed over the resulting structure. By contrast, referring to Figure 3B, a dummy or permanent gate dielectric layer 310 is formed on the exposed surfaces of the semiconductor fins 302, and dummy spacers 312 are formed adjacent to the resulting structure.

[0024] Referring to Figure 2C, gate endcap cut patterning is performed and isolation regions 214 are formed at the resulting patterned dummy gate ends 216. In the conventional process scheme, a larger gate endcap must be fabricated to allow for gate mask mis-registration, as depicted by the arrowed regions 218. By contrast, referring to Figure 3C, self-aligned isolation regions 314 are formed by providing an isolation layer over the structure of Figure 3B, e.g., by deposition and planarization. In one such embodiment, the self-aligned gate endcap process does not require extra space for mask registration, as compared in Figures 2C and 3C.

[0025] Referring to Figure 2D, the dummy gate electrode 212 of Figure 2C is replaced with permanent gate electrodes. In the case of use of a dummy gate dielectric layer, such a dummy gate dielectric layer may also be replaced by a permanent gate dielectric layer in this process. In the specific example shown, a dual metal gate replacement process is performed to provide an N-type gate electrode 220 over a first semiconductor fin 202A and to provide a P-type gate electrode 222 over a second semiconductor fin 202B. The N-type gate electrode 220

and the P-type gate electrode 222 are formed between the gate edge isolations structures 214, but form a P/N junction 224 where they meet. The exact location of the P/N junction 224 may vary, depending on mis-registration, as depicted by the arrowed region 226.

[0026] By contrast, referring to Figure 3D, the hardmask layer 304 and pad oxide layer 306 are removed, and the dummy spacers 314 of Figure 3C are replaced with permanent gate electrodes. In the case of use of a dummy gate dielectric layer, such a dummy gate dielectric layer may also be replaced by a permanent gate dielectric layer in this process. In the specific example shown, a dual metal gate replacement process is performed to provide an N-type gate electrode 320 over a first semiconductor fin 302A and to provide a P-type gate electrode 322 over a second semiconductor fin 302B. The N-type gate electrode 320 and the P-type gate electrode 322 are formed between, and are also separated by, the gate edge isolations structures 314.

[0027] Referring again to Figure 2D, a local interconnect 240 may be fabricated to contact N-type gate electrode 220 and P-type gate electrode 322 to provide a conductive path around the P/N junction 224. Likewise, referring to Figure 3D, a local interconnect 340 may be fabricated to contact N-type gate electrode 320 and P-type gate electrode 322 to provide a conductive path over the intervening isolation structure 314 there between. Referring to both Figures 2D and 3D, a hardmask 242 or 342 may be formed on the local interconnect 240 or 340, respectively.

[0028] In another aspect, a hardmask and pad oxide layer may not be retained atop patterned find throughout a dummy spacer and self-aligned gate edge

isolations structure fabrication process. As such, the height of the semiconductor fins relative to the height of the dummy spacers may need to be differentiated in another way. As an example, Figures 4A-4G illustrate cross-sectional views and corresponding top views of process operations in another self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with another embodiment of the present invention.

[0029] Referring to Figure 4A, a bulk semiconductor substrate 400, such as a bulk single crystalline silicon substrate, is provided having fins 402 etched therein. In an embodiment, the fins 402 are formed directly in the bulk substrate 400 and, as such, are formed continuous with the bulk substrate 400. It is to be appreciated that within the substrate 400, shallow trench isolation structures may be formed between fins. In one embodiment, artifacts from patterning the fins 402, such as a hardmask layer and a pad oxide layer, have been removed, as is depicted in Figure 4A.

[0030] Referring to Figure 4B, dummy spacers 404 are formed along the sidewalls of the fins 402. In an embodiment, the dummy spacers 404 are formed by a deposition and etch process that ultimately exposes the top surface of the fins 402. It is to be appreciated that the fins 402 may be passivated, e.g., by deposition or growth of a dummy gate dielectric layer, prior to the formation of the dummy spacers 404. In one embodiment, the fins 402 are silicon fins passivated with a silicon dioxide layer, and the dummy spacers are fabricated from silicon nitride or like material. In another embodiment, however the fins 402 are not passivated at this stage.

[0031] Referring to Figure 4C, isolations structures 406 are formed in the open regions of the structure of Figure 4B. In an embodiment, the isolation regions

406 are formed by deposition and subsequent planarization (e.g., by chemical mechanical polishing) of a dielectric film over the structure of Figure 4B. In a particular embodiment, the isolation structures are composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0032] Referring to Figure 4D, the fins 402 are recessed relative to the height of the isolation structures 406 and relative to the height of the dummy spacers 404. In an embodiment, the recessing is performed by using a selective etch process. In one such embodiment, a passivation layer first formed on fins 402 is removed prior to or during the recessing of the fins 402.

[0033] Referring to Figure 4E, the dummy spacers 404 are removed from the structure of Figure 4D. In an embodiment, the removal is performed by using a selective etch process. In one such embodiment, the isolation structures 406 are composed of silicon oxide, the fins 402 are composed of silicon, and the selectively removed dummy spacers are composed of silicon nitride.

[0034] Referring to Figure 4F, a gate electrode stack 408 is formed in the locations from which dummy spacers 404 were removed and along the top surfaces of the recessed fins 402. In an embodiment, the gate electrode stack 408 includes a conformal gate dielectric layer 410, such as a high-k gate dielectric layer, and a metal gate electrode 412. The cross-sectional view of Figure 4F is taken along the a-a' axis of the top view of Figure 4F. It is to be understood, however, that the top view is taken somewhat deeper into the structure in order to show the whole fins 402. In actuality, the metal gate material 412 would cover the fins 402 in the top view.

[0035] Referring to Figure 4G, trench contacts 414 are formed adjacent to the gate electrode stacks 408 and along the top surfaces of the recessed fins 402. In an embodiment, the trench contacts 414 are for contacting source and drain regions within the fins 402, and are separated from the gate electrode stacks 408 by dielectric spacers 416. The cross-sectional view of Figure 4G is taken along the b-b' axis of the top view of Figure 4G. It is to be understood, however, that the top view is taken somewhat deeper into the structure in order to show the whole fins 402. In actuality, the trench contacts 414 would cover the fins 402 in the top view.

[0036] In another aspect, referring again to Figure 3D, in an embodiment, one or more of the above approaches requires an additional local interconnect layer (LI) above gate and trench contact (TCN) to connect adjacent gates and TCN electrodes. In one such embodiment, such a local interconnect must overlap gate and TCN, without creating contact to gate (CTG) shorting. As such, fabrication of the local interconnect can require patterning of lines at 1/2 of gate pitch with good CTG short margin, while maintaining robust LI to TCN contact. Hence, the alignment between LI and gate or TCN is another difficult patterning problem. As such, in accordance with an embodiment of the present invention, in order to address the above concern, a fabrication scheme for local interconnect lines which are self-aligned to gate and TCN without any need to allow for mask registration is provided. The approach involves fabrication of a spacer along a taller stack that includes a dummy gate and hardmask and which extends above the self-aligned gate endcap. In one such embodiment, the spacers serve as continuous self-aligned walls separating gate and contact. Two additional dielectric materials with contrasting

etch properties may be used as hardmasks to allow for selectively opening an area for gate-LI (LIG) and TCN-LI (LIT).

[0037] As an example, Figure 5A illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a pitch division patterned local interconnect (LI), in accordance with one embodiment of the present invention. By contrast, Figure 5B illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a self-aligned local interconnect (SAGELI), in accordance with another embodiment of the present invention.

[0038] Referring to Figure 5A, a semiconductor device 500A includes a semiconductor fin 502. A plurality of short self-aligned isolation structures 504 separate alternating gate 506 and trench contact 508 regions. Upper isolation structures 510 separate alternating trench contact local interconnects 512 and gate local interconnects 514. The trench contact local interconnects 512 and gate local interconnects 514 are formed by pitch division patterning to accommodate for mis-registration, as is shown in Figure 5A. It is to be appreciated that dielectric caps may be formed on the trench contact local interconnects 512 and gate local interconnects 514, as is also depicted in Figure 5A.

[0039] Referring to Figure 5B, a semiconductor device 500B includes a semiconductor fin 552. A plurality of tall self-aligned isolation structures 554 separate alternating gate 556 and trench contact 558 regions. The same isolation structures 554 also separate alternating trench contact local interconnects 562 and gate local interconnects 564. The trench contact local interconnects 512 and gate local interconnects 514 are formed without using an additional lithography operation

as was need for the case of Figure 5A. It is to be appreciated that dielectric caps may be formed on the trench contact local interconnects 562 and gate local interconnects 564, as is depicted in Figure 5B. It is also to be appreciated that the trench contact local interconnects 512 and gate local interconnects 514 are, in an embodiment, fabricated at different times, the process for forming each taking advantage of the use of plugs/hardmask layers as placeholders prior to replacement with the actual permanent materials of the trench contact local interconnects 512 and gate local interconnects 514. Furthermore, although all locations in Figure 5B are shown as having a gate local interconnect or trench contact local interconnect, not all locations need be selected for local interconnection. In locations not selected a dielectric plug or hardmask may remain (i.e., it is not selected for removal at certain locations).

[0040] As exemplary approaches, Figures 6A-6H illustrate angled, three-dimensional cross-sectional views of various operations in the fabrication of self-aligned gate endcaps, in accordance with an embodiment of the present invention. Figures 7A-7D illustrate angled, three-dimensional cross-sectional views of various structural options for providing a foundation for local interconnect fabrication, in accordance with an embodiment of the present invention.

[0041] Referring to Figure 6A, a plurality of semiconductor fins 602 is formed by patterning a substrate 600, such as a single crystalline silicon substrate, and the patterning may involve pitch halving or pitch quartering patterning. Furthermore, a passivation layer 604, a dummy gate layer 606 (such as a polycrystalline silicon layer), and a hardmask layer 608 are patterned during the fin 602 patterning.

[0042] Referring to Figure 6B, a shallow trench isolation (STI) layer 610 is formed over the structure of Figure 6A. In an embodiment, the STI layer 610 includes a silicon dioxide layer and is formed by chemical vapor deposition (CVD) and subsequent chemical mechanical planarization (CMP). In one embodiment, the STI structure includes a liner dielectric layer 612, as shown in Figure 6B.

[0043] Referring to Figure 6C, the STI layer 610 of Figure 6B is recessed to form an STI structure 614 (which may include a liner dielectric layer) and a dummy gate dielectric layer 616 is formed on the resulting structure. In one such embodiment, the dummy gate dielectric layer 616 is formed by deposition and is further deposited on the STI structure 614, as depicted. Furthermore, hardmask layer 608 may be removed, as is also depicted.

[0044] Referring to Figure 6D, spacers 618 are formed along the sidewalls of the protruding portions of the structure of Figure 6C. In an embodiment, the spacers 618 are formed by a deposition and subsequent anisotropic etch process. In one such embodiment, the spacers are composed of deposited polycrystalline silicon. Depending on the spacing between certain of the fins 602, some spacers 618 are discrete from all other spacers, while some spacers are continuous with another spacer. As an example, the portion 620A has discrete spacers 618A, while the portion 620B includes a pair of continuous spacers 618B. Thus, referring collectively to Figures 6A-6D, a finFET "hat" and dummy gate poly are patterned with a standard pitch division fin patterning process and a spacer is created on both sides of the patterned fin-poly pillars.

[0045] Referring to Figure 6E, the gaps between the spacers 618 of Figure 6D are filled with a dielectric material layer 622 to create transistor isolations. In an embodiment, the dielectric material is composed of a silicon nitride material.

[0046] Referring to Figure 6F, the dielectric material layer 622 is planarized (e.g., by CMP) to expose the dummy gate layer 606 and the corresponding spacers 618. In an embodiment, both the dummy gate layer 606 and the corresponding spacers 618 are composed of polycrystalline silicon. The process forms self-aligned end cap isolation walls 624.

[0047] Referring to Figure 6G, a second dummy layer and hardmask stack or a tall hardmask only are/is deposited and patterned using pitch division gate patterning (both cases shown as item 626 in Figure 6G) on the structure of Figure 6H. In an embodiment, in the case that a dummy layer and hardmask stack is used, the dummy layer is composed of polycrystalline silicon.

[0048] Referring to Figure 6H, an anisotropic etch selective to hardmask layer 626, isolation walls 624 and finFET "hat" 616 (e.g., remaining from the dummy gate dielectric layer) is performed to provide a straight profile between patterned lines and resulting endcap isolation cages 628. Although not shown, following gate spacer formation, N-type or P-type source drain formation, and gate electrode replacement (e.g., with high-k/metal gate), a conductive material can be formed in the endcap isolation cages 628 to provide trench contacts. And, in cases where the isolation walls are of sufficient height, self-aligned local interconnect lines may be fabricated, examples of which are described below in association with Figures 7C and 7D.

[0049] To provide an initial comparison, Figure 7A illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700A without self-aligned gate edge isolation. Referring to Figure 7A, a plurality of fins 702A has a dummy gate layer 704A and corresponding hardmask 706A patterned thereon. In the subsequent fabrication of local interconnects, a pitch divisional patterning scheme would have to be employed.

[0050] Figure 7B illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700B having self-aligned gate edge isolation. Referring to Figure 7B, a plurality of fins 702B has a dummy gate layer 704B and corresponding hardmask 706B patterned thereon. Self-aligned gate edge isolation structures 708B are formed between various groupings of the fins 702B. However, the hardmask 706B is relatively short compared with the self-aligned gate edge isolation structures 708B. As such, in the subsequent fabrication of local interconnects, a pitch divisional patterning scheme would have to be employed.

[0051] Figure 7C illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700C having self-aligned gate edge isolation. Referring to Figure 7C, a plurality of fins 702C has a dummy gate layer 704C, corresponding second dummy layer 705C, and corresponding hardmask 706C patterned thereon. Self-aligned gate edge isolation structures 708C are formed between various groupings of the fins 702C. The height of the hardmask 706C together with the second dummy layer 705C is relatively tall compared with the self-aligned gate edge isolation structures 708C. As such, in the subsequent fabrication of local interconnects, a self-aligned local interconnect scheme may be employed.

[0052] Figure 7D illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700D having self-aligned gate edge isolation. Referring to Figure 7D, a plurality of fins 702D has a dummy gate layer 704D and a corresponding tall hardmask 706D patterned thereon. Self-aligned gate edge isolation structures 708D are formed between various groupings of the fins 702D. The height of the tall hardmask 706D is relatively tall compared with the self-aligned gate edge isolation structures 708D. As such, in the subsequent fabrication of local interconnects, a self-aligned local interconnect scheme may be employed.

[0053] More generally, one or more embodiments described herein provide an avenue for area scaling, reducing capacitance, and/or eliminating various critical front end masks, such as gate cut masks. In one such embodiment the width of a minimum transistor can be reduced by up to 30% by implementing one or more of the approaches describe herein. The smaller transistor size reduces the capacitance between the gate and TCN and other parasitic capacitances. No extra mask steps are needed to create the endcaps, contacts and local interconnect lines so the many masks needed for such features in the standard process are eliminated.

[0054] More specifically, key features of one or more embodiments described above may include one or more of: (1) the gate endcap is the distance from the fin edge to the isolation edge. This distance is defined by the spacer width and is the same size for all transistors. No lithographic patterning is needed to define the endcap so there is no need to allow for mask registration in the endcap. (2) The TCN overlap of the fin is determined by the spacer width and is also not affected by mask registration. (3) The local interconnect lines are self-aligned to the gate and TCN by utilizing the gate patterning lines above the transistor isolation

walls to form three distinct hardmasks that can be selectively opened one at a time. Embodiments may be applicable to the 7nm node generation, e.g., to improve transistor layout density and gate capacitance (dynamic energy and performance improvement) and reduce total mask count.

[0001] It is to be appreciated that the structures resulting from the above exemplary processing schemes may be used in a same or similar form for subsequent processing operations to complete device fabrication, such as PMOS and NMOS device fabrication. As an example of a completed device, Figures 8A and 8B illustrate a cross-sectional view and a plan view (taken along the a-a' axis of the cross-sectional view), respectively, of a non-planar semiconductor device having self-aligned gate edge isolation, in accordance with an embodiment of the present invention, and as building on the structure described in association with Figure 3D.

[0002] Referring to Figure 8A, a semiconductor structure or device 800 includes a non-planar active regions (e.g., a fin structures including protruding fin portion 804 and sub-fin region 805) formed from substrate 802, and within isolation region 806. Gate structures 808 are disposed over the protruding portions 804 of the non-planar active regions as well as over a portion of the isolation region 806. As shown, gate structures 808 include a gate electrode 850 and a gate dielectric layer 852. In one embodiment, although not shown, gate structures 808 may also include a dielectric cap layer. Gate structures 808 are separated by self-aligned gate edge isolation structures 820. A local interconnect 854 coupled adjacent gate structures 808. A gate contact 814, and overlying gate contact via 816 are also seen from this perspective, along with an overlying metal interconnect 860, all of which are disposed in inter-layer dielectric stacks or layers 870. Also seen from the

perspective of Figure 8A, the gate contact 814 is, in one embodiment, disposed over the non-planar active regions. As is also depicted in Figure 8A, an interface 880 exists between a doping profile of protruding fin portions 804 and sub-fin regions 805, although other embodiments do not include such an interface in doping profile between these regions.

[0003] Referring to Figure 8B, the gate structures 808 are shown as disposed over the protruding fin portions 804, as isolated by self-aligned gate edge isolation structures 820. Source and drain regions 804A and 804B of the protruding fin portions 804 are shown in this perspective, although it is to be understood that these regions would be overlapped with trench contact structures. In one embodiment, the source and drain regions 804A and 804B are doped portions of original material of the protruding fin portions 804. In another embodiment, the material of the protruding fin portions 804 is removed and replaced with another semiconductor material, e.g., by epitaxial deposition. In either case, the source and drain regions 804A and 804B may extend below the height of dielectric layer 806, i.e., into the sub-fin region 805.

[0004] In an embodiment, the semiconductor structure or device 800 is a non-planar device such as, but not limited to, a finFET or a tri-gate device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate structures 808 surround at least a top surface and a pair of sidewalls of the three-dimensional body.

[0005] Substrate 802 may be composed of a semiconductor material that can withstand a manufacturing process and in which charge can migrate. In an

embodiment, substrate 802 is a bulk substrate composed of a crystalline silicon, silicon/germanium or germanium layer doped with a charge carrier, such as but not limited to phosphorus, arsenic, boron or a combination thereof, to form active region 804. In one embodiment, the concentration of silicon atoms in bulk substrate 802 is greater than 97%. In another embodiment, bulk substrate 802 is composed of an epitaxial layer grown atop a distinct crystalline substrate, e.g. a silicon epitaxial layer grown atop a boron-doped bulk silicon mono-crystalline substrate. Bulk substrate 802 may alternatively be composed of a group III-V material. In an embodiment, bulk substrate 802 is composed of a III-V material such as, but not limited to, gallium nitride, gallium phosphide, gallium arsenide, indium phosphide, indium antimonide, indium gallium arsenide, aluminum gallium arsenide, indium gallium phosphide, or a combination thereof. In one embodiment, bulk substrate 802 is composed of a III-V material and the charge-carrier dopant impurity atoms are ones such as, but not limited to, carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium.

[0006] Isolation region 806 may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, portions of a permanent gate structure from an underlying bulk substrate or isolate active regions formed within an underlying bulk substrate, such as isolating fin active regions. For example, in one embodiment, the isolation region 806 is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0007] Self-aligned gate edge isolation structures 820 may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of,

portions of permanent gate structures from one another. For example, in one embodiment, the isolation region 806 is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0008] Gate structures 808 may be composed of a gate electrode stack which includes a gate dielectric layer 852 and a gate electrode layer 850. In an embodiment, the gate electrode of the gate electrode stack is composed of a metal gate and the gate dielectric layer is composed of a high-K material. For example, in one embodiment, the gate dielectric layer is composed of a material such as, but not limited to, hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or a combination thereof. Furthermore, a portion of gate dielectric layer may include a layer of native oxide formed from the top few layers of the substrate 802. In an embodiment, the gate dielectric layer is composed of a top high-k portion and a lower portion composed of an oxide of a semiconductor material. In one embodiment, the gate dielectric layer is composed of a top portion of hafnium oxide and a bottom portion of silicon dioxide or silicon oxy-nitride.

[0009] In one embodiment, the gate electrode is composed of a metal layer such as, but not limited to, metal nitrides, metal carbides, metal silicides, metal aluminides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides. In a specific

embodiment, the gate electrode is composed of a non-workfunction-setting fill material formed above a metal workfunction-setting layer.

[0010] Spacers associated with the gate electrode stacks may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, a permanent gate structure from adjacent conductive contacts, such as self-aligned contacts. For example, in one embodiment, the spacers are composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0011] Local interconnect 854, gate contact 814, and overlying gate contact via 816 may be composed of a conductive material. In an embodiment, one or more of the contacts or vias are composed of a metal species. The metal species may be a pure metal, such as tungsten, nickel, or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., such as a silicide material). It is to be appreciated that a hardmask layer may be disposed on the local interconnect 854 in locations where gate contact 814 is not located thereon. Furthermore, the local interconnect 854 may be fabricated by lithographic patterning or, in other embodiments, may be fabricated as a self-aligned interconnect structure, as aligned with taller versions of the Self-aligned gate edge isolation structures 820.

[0012] In an embodiment (although not shown), providing structure 800 involves formation of a contact pattern which is essentially perfectly aligned to an existing gate pattern while eliminating the use of a lithographic step with exceedingly tight registration budget. In one such embodiment, this approach enables the use of intrinsically highly selective wet etching (e.g., versus conventionally implemented dry or plasma etching) to generate contact openings. In

an embodiment, a contact pattern is formed by utilizing an existing gate pattern in combination with a contact plug lithography operation. In one such embodiment, the approach enables elimination of the need for an otherwise critical lithography operation to generate a contact pattern, as used in conventional approaches. In an embodiment, a trench contact grid is not separately patterned, but is rather formed between poly (gate) lines. For example, in one such embodiment, a trench contact grid is formed subsequent to gate grating patterning but prior to gate grating cuts.

[0013] Furthermore, the gate structures 808 may be fabricated by a replacement gate process. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing. In an embodiment, dummy gates are removed by a dry etch or wet etch process. In one embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process including use of SF_6. In another embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a wet etch process including use of aqueous NH_4OH or tetramethylammonium hydroxide. In one embodiment, dummy gates are composed of silicon nitride and are removed with a wet etch including aqueous phosphoric acid.

[0014] In an embodiment, one or more approaches described herein contemplate essentially a dummy and replacement gate process in combination with a dummy and replacement contact process to arrive at structure 800. In one such embodiment, the replacement contact process is performed after the replacement

gate process to allow high temperature anneal of at least a portion of the permanent gate stack. For example, in a specific such embodiment, an anneal of at least a portion of the permanent gate structures, e.g., after a gate dielectric layer is formed, is performed at a temperature greater than approximately 600 degrees Celsius. The anneal is performed prior to formation of the permanent contacts.

[0015] Referring again to Figure 8A, in an embodiment, a semiconductor device has contact structures that contact portions of a gate electrode formed over an active region. In general, prior to (e.g., in addition to) forming a gate contact structure (such as a via) over an active portion of a gate and in a same layer as a trench contact via, one or more embodiments of the present invention include first using a gate aligned trench contact process. Such a process may be implemented to form trench contact structures for semiconductor structure fabrication, e.g., for integrated circuit fabrication. In an embodiment, a trench contact pattern is formed as aligned to an existing gate pattern. By contrast, conventional approaches typically involve an additional lithography process with tight registration of a lithographic contact pattern to an existing gate pattern in combination with selective contact etches. For example, a conventional process may include patterning of a poly (gate) grid with separate patterning of contact features.

[0016] Figure 9 illustrates a computing device 900 in accordance with one implementation of the invention. The computing device 900 houses a board 902. The board 902 may include a number of components, including but not limited to a processor 904 and at least one communication chip 906. The processor 904 is physically and electrically coupled to the board 902. In some implementations the at least one communication chip 906 is also physically and electrically coupled to the

board 902. In further implementations, the communication chip 906 is part of the processor 904.

[0017] Depending on its applications, computing device 900 may include other components that may or may not be physically and electrically coupled to the board 902. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0018] The communication chip 906 enables wireless communications for the transfer of data to and from the computing device 900. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 906 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device

900 may include a plurality of communication chips 906. For instance, a first communication chip 906 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 906 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0019] The processor 904 of the computing device 900 includes an integrated circuit die packaged within the processor 904. In some implementations of the invention, the integrated circuit die of the processor includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0020] The communication chip 906 also includes an integrated circuit die packaged within the communication chip 906. In accordance with another implementation of the invention, the integrated circuit die of the communication chip includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention.

[0021] In further implementations, another component housed within the computing device 900 may contain an integrated circuit die that includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention.

[0022] In various implementations, the computing device 900 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal

digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 900 may be any other electronic device that processes data.

[0023] Thus, embodiments of the present invention include self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures.

[0024] In an embodiment, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length in a first direction. A gate structure is disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction. A pair of gate edge isolation structures is centered with the semiconductor fin. A first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

[0025] In one embodiment, the semiconductor structure further includes source and drain regions disposed in the semiconductor fin, on either side of the gate structure. A first trench contact is disposed over the source region and a second trench contact disposed over the drain region. Each of the first and second trench contacts has a first end opposite a second end in the second direction. The first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the first trench contact and to the first end of the second trench contact. The

second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.

[0026] In one embodiment, the semiconductor structure further includes a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin. A second gate structure is disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction. The second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure. A third gate edge isolation structure is disposed directly adjacent to the second end of the second gate structure. The third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.

[0027] In one embodiment, the semiconductor structure further includes a local interconnect disposed above and electrically coupling the first and second gate structures.

[0028] In one embodiment, the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

[0029] In one embodiment, the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.

[0030] In one embodiment, the gate structure includes a high-k gate dielectric layer and a metal gate electrode.

[0031] In one embodiment, the pair of gate edge isolation structures is composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0032] In an embodiment, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length. Alternating source/drain and channel regions are disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin. The semiconductor structure also includes a plurality of gate edge isolation structures. An adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. A gate local interconnect is disposed above one of the gate structures and between a pair of the plurality of gate edge isolation structures.

[0033] In one embodiment, the semiconductor structure further includes a dielectric cap disposed on the gate local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

[0034] In one embodiment, the semiconductor structure further includes a trench contact local interconnect disposed above one of the trench contacts and between a second pair of the plurality of gate edge isolation structures.

[0035] In one embodiment, the semiconductor structure further includes a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the second pair of the plurality of gate edge isolation structures.

[0036] In one embodiment, each gate structure includes a high-k gate dielectric layer and a metal gate electrode.

[0037] In one embodiment, each of the plurality of gate edge isolation structures is composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0038] In an embodiment, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length. Alternating source/drain and channel regions are disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin. The semiconductor structure also includes a plurality of gate edge isolation structures. An adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. A trench contact local interconnect is disposed above one of the trench contacts and between a pair of the plurality of gate edge isolation structures.

[0039] In one embodiment, the semiconductor structure further includes a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

[0040] In one embodiment, each gate structure includes a high-k gate dielectric layer and a metal gate electrode.

[0041] In one embodiment, each of the plurality of gate edge isolation structures is composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0042] In an embodiment, a method of fabricating a semiconductor structure involves forming first and second parallel semiconductor fins above a substrate.

The method also involves forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins. The dummy spacers of the first semiconductor fin are non-continuous with the dummy spacers of the second semiconductor fin. The method also involves forming an isolation structure between the dummy spacers of the first and second semiconductor fins. The method also involves removing the dummy spacers. The method also involves forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure.

[0043] In one embodiment, the method also involves forming a first pair of trench contacts over the first semiconductor fin and a second pair of trench contacts over the second semiconductor fin. The first and pairs of trench contacts are directly adjacent to, and separated from one another by, the isolation structure.

[0044] In one embodiment, the method also involves, subsequent to forming an isolation structure and prior to removing the dummy spacers, recessing the first and second semiconductor fins.

[0045] In one embodiment, forming the dummy spacers involves forming and etching a polycrystalline silicon layer.

[0046] In one embodiment, forming the isolation structure involves depositing and planarizing a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0047] In one embodiment, forming one or both of the first and second replacement gate structures involves forming a high-k gate dielectric layer and a metal gate electrode.

[0048] In one embodiment, the method also involves forming a local interconnect above and electrically coupling the first and second replacement gate structures.

CLAIMS

What is claimed is:

1. A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length in a first direction;

a gate structure disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction; and

a pair of gate edge isolation structures centered with the semiconductor fin, wherein a first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

2. The semiconductor structure of claim 1, further comprising:

source and drain regions disposed in the semiconductor fin, on either side of the gate structure; and

a first trench contact disposed over the source region and a second trench contact disposed over the drain region, each of the first and second trench contacts having a first end opposite a second end in the second direction, wherein the first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the first trench contact and to the first end of the second trench contact, and the second of the pair of gate edge isolation structures is

disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.

3. The semiconductor structure of claim 1, further comprising:

a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin;

a second gate structure disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction, wherein the second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure; and

a third gate edge isolation structure disposed directly adjacent to the second end of the second gate structure, wherein the third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.

4. The semiconductor structure of claim 3, further comprising:

a local interconnect disposed above and electrically coupling the first and second gate structures.

5. The semiconductor structure of claim 4, wherein the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

6. The semiconductor structure of claim 3, wherein the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.

7. The semiconductor structure of claim 1, wherein the gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

8. The semiconductor structure of claim 1, wherein the pair of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

9. A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length;

alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and

a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and

a gate local interconnect disposed above one of the gate structures and between a pair of the plurality of gate edge isolation structures.

10. The semiconductor structure of claim 9, further comprising:

a dielectric cap disposed on the gate local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

11. The semiconductor structure of claim 9, further comprising:

a trench contact local interconnect disposed above one of the trench contacts and between a second pair of the plurality of gate edge isolation structures.

12. The semiconductor structure of claim 11, further comprising:

a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the second pair of the plurality of gate edge isolation structures.

13. The semiconductor structure of claim 9, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

14. The semiconductor structure of claim 9, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

15. A semiconductor structure, comprising:

a semiconductor fin disposed above a substrate and having a length;

alternating source/drain and channel regions disposed in the length of the semiconductor fin, each source/drain region having an associated trench

contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin; and

a plurality of gate edge isolation structures, wherein an adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures; and

a trench contact local interconnect disposed above one of the trench contacts and between a pair of the plurality of gate edge isolation structures.

16. The semiconductor structure of claim 15, further comprising:

a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

17. The semiconductor structure of claim 15, wherein each gate structure comprises a high-k gate dielectric layer and a metal gate electrode.

18. The semiconductor structure of claim 15, wherein each of the plurality of gate edge isolation structures comprises a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

19. A method of fabricating a semiconductor structure, the method comprising:

forming first and second parallel semiconductor fins above a substrate;

forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins, wherein the dummy spacers of the first semiconductor

fin are non-continuous with the dummy spacers of the second semiconductor fin;

forming an isolation structure between the dummy spacers of the first and second semiconductor fins;

removing the dummy spacers; and

forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure.

20. The method of claim 19, further comprising:

forming a first pair of trench contacts over the first semiconductor fin and a second pair of trench contacts over the second semiconductor fin, wherein the first and pairs of trench contacts are directly adjacent to, and separated from one another by, the isolation structure.

21. The method of claim 19, further comprising:

subsequent to forming an isolation structure and prior to removing the dummy spacers, recessing the first and second semiconductor fins.

22. The method of claim 19, wherein forming the dummy spacers comprises forming and etching a polycrystalline silicon layer.

23. The method of claim 19, wherein forming the isolation structure comprises depositing and planarizing a material selected from the group consisting of silicon oxide, silicon nitride, silicon carbide, and a combination thereof.

24. The method of claim 19, wherein forming one or both of the first and second replacement gate structures comprises forming a high-k gate dielectric layer and a metal gate electrode.

25. The method of claim 19, further comprising:

forming a local interconnect above and electrically coupling the first and second replacement gate structures.

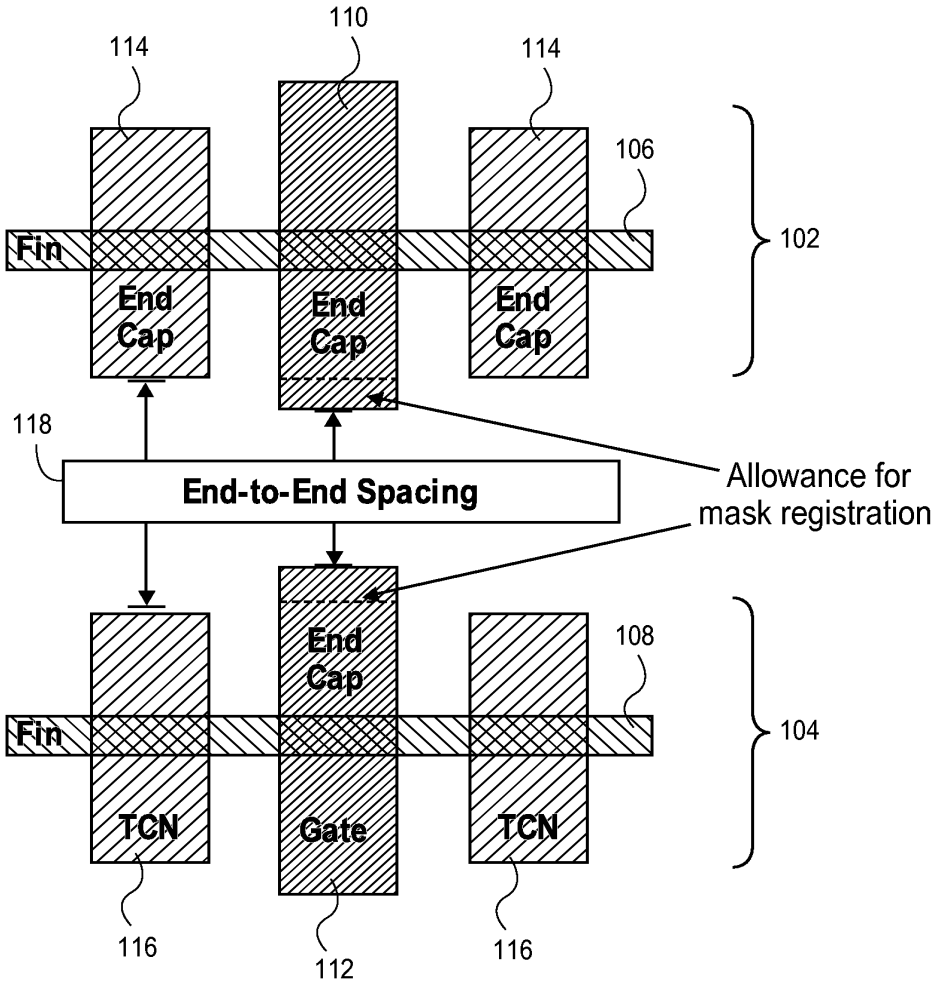

110
114
114
106
102
Fin
End Cap
End Cap
End Cap
118
End-to-End Spacing
Allowance for mask registration
End Cap
108
104
Fin
TCN
Gate
TCN
116
112
116

FIG. 1

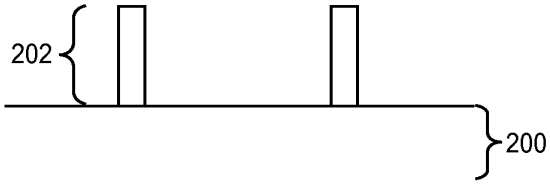


FIG. 2A

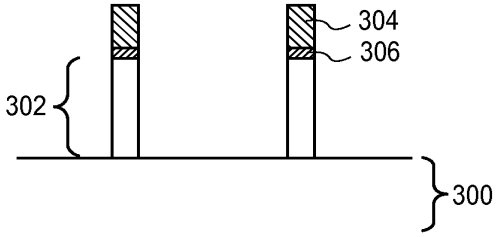


FIG. 3A

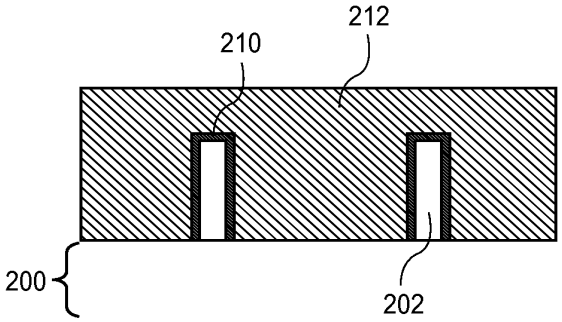


FIG. 2B

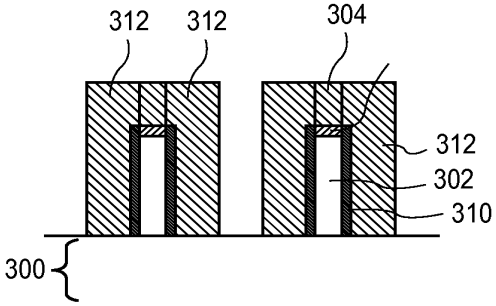


FIG. 3B

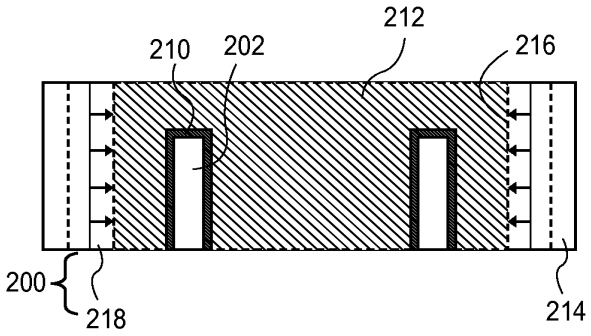


FIG. 2C

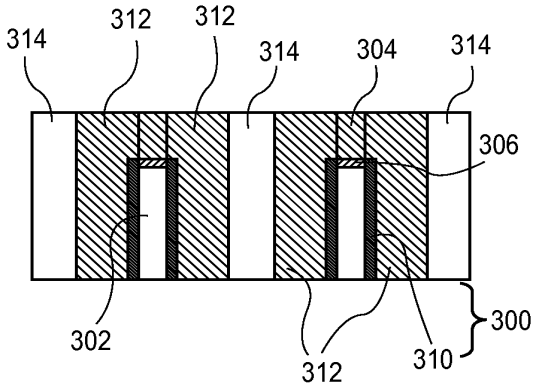


FIG. 3C

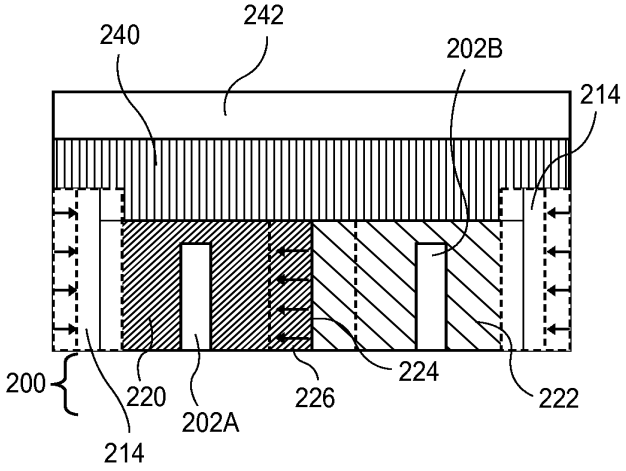


FIG. 2D

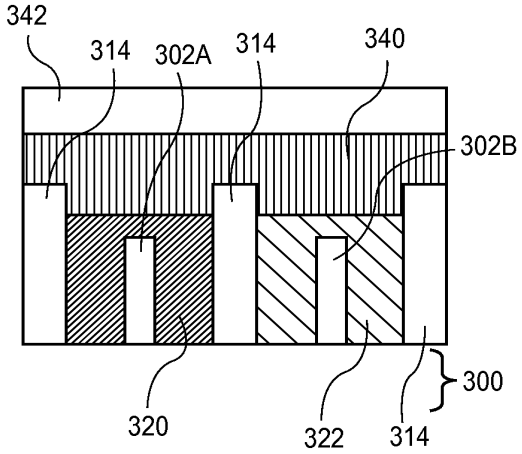


FIG. 3D

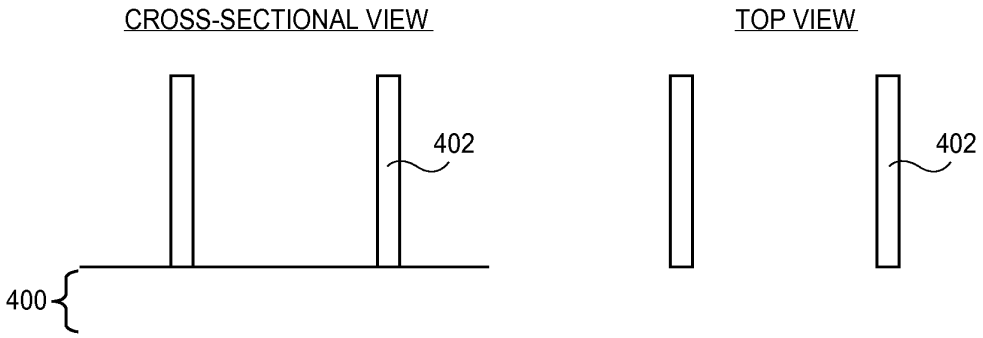


FIG. 4A

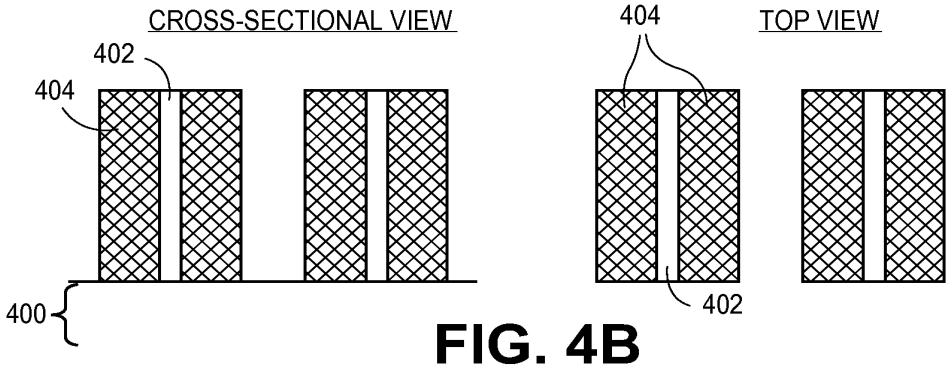


FIG. 4B

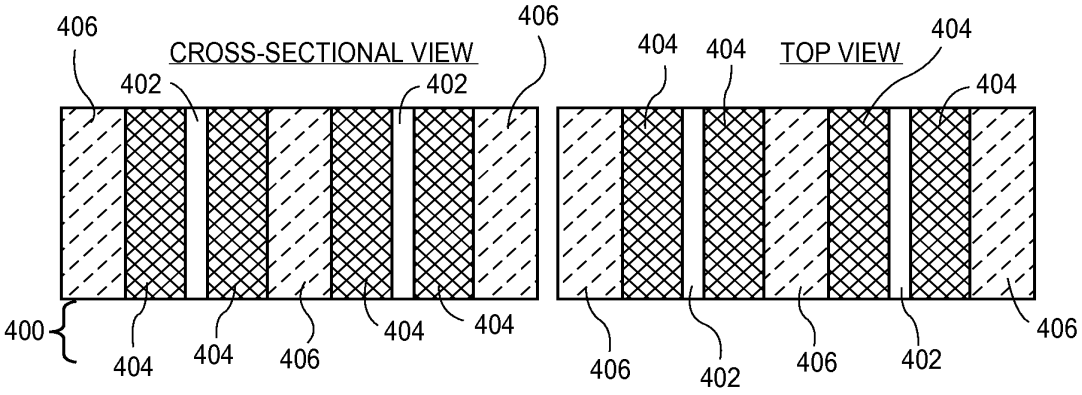


FIG. 4C

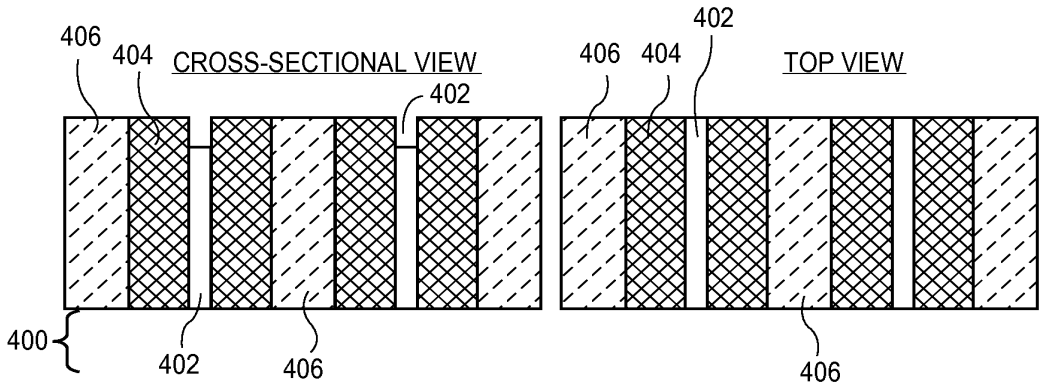


FIG. 4D

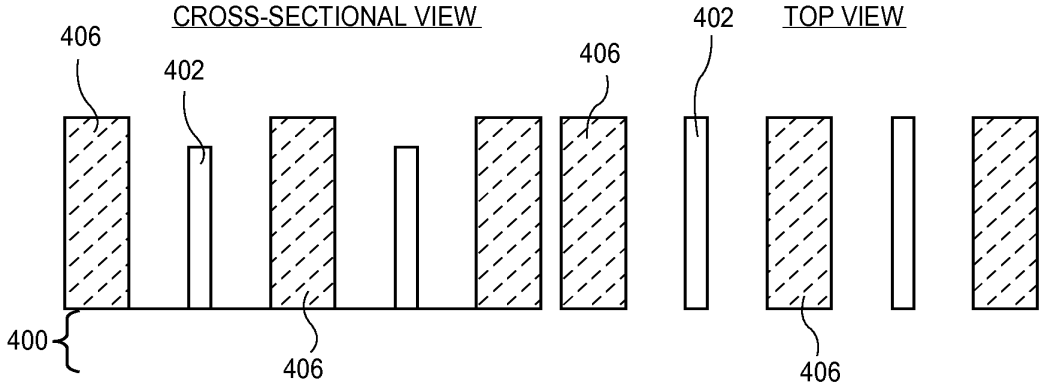


FIG. 4E

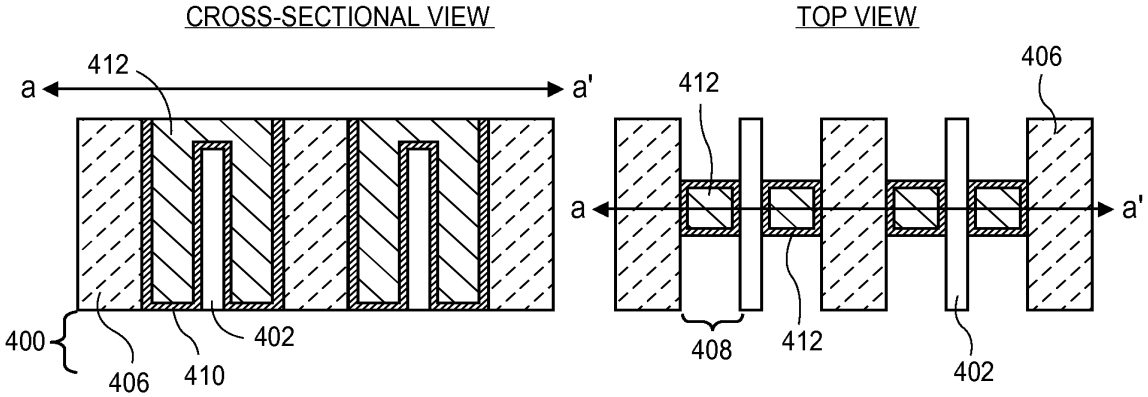


FIG. 4F

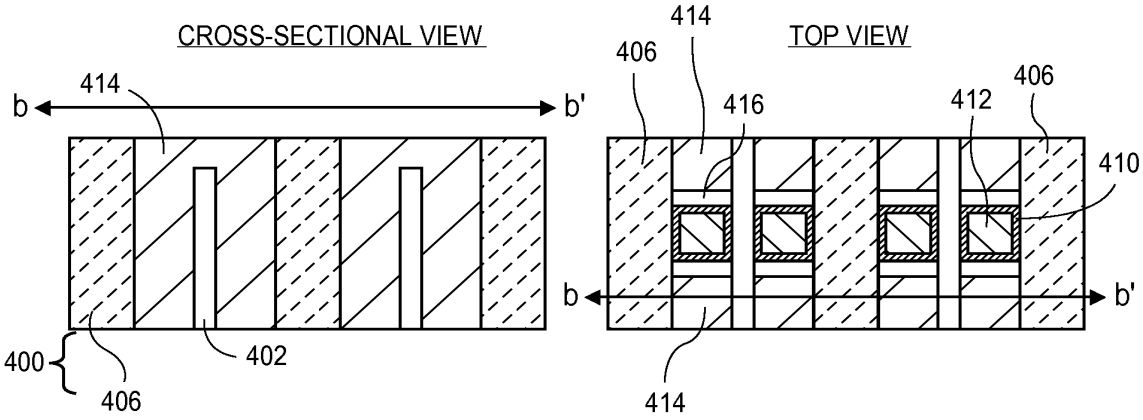


FIG. 4G

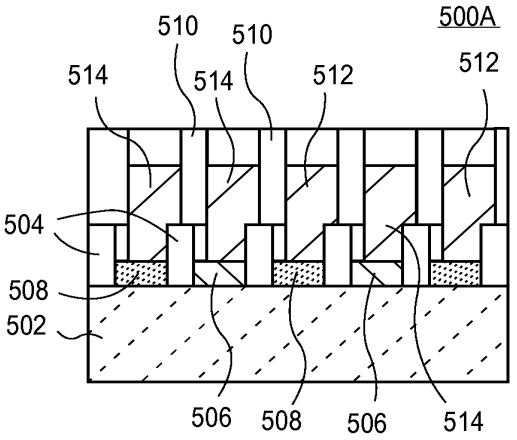


FIG. 5A

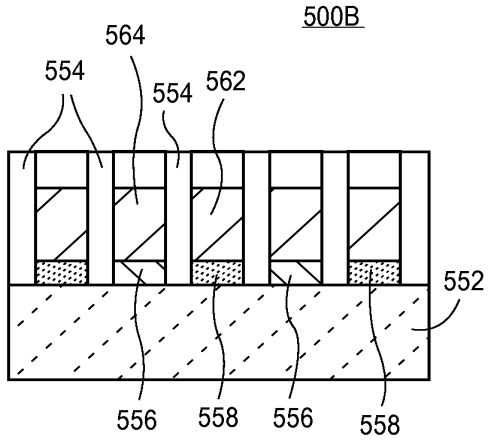


FIG. 5B

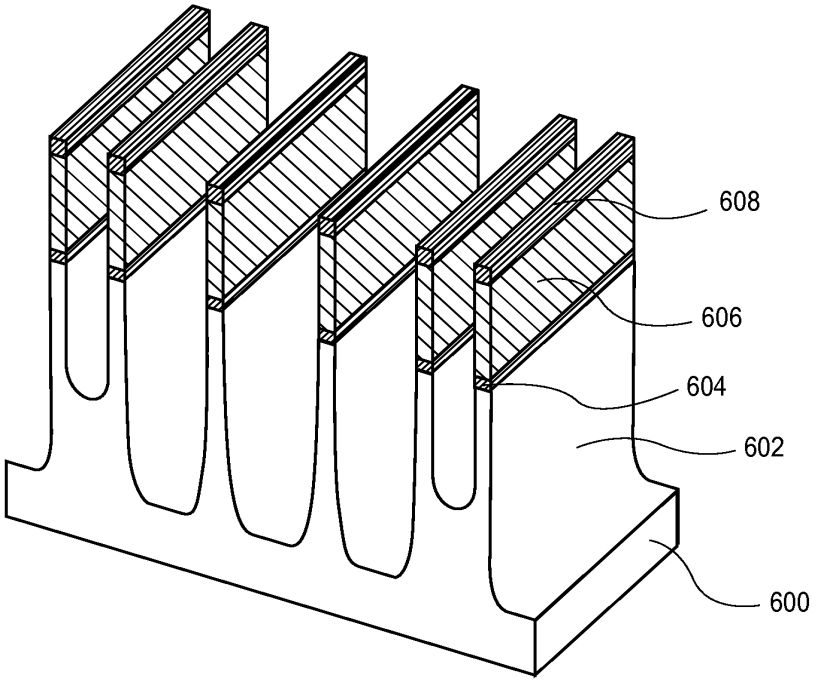


FIG. 6A

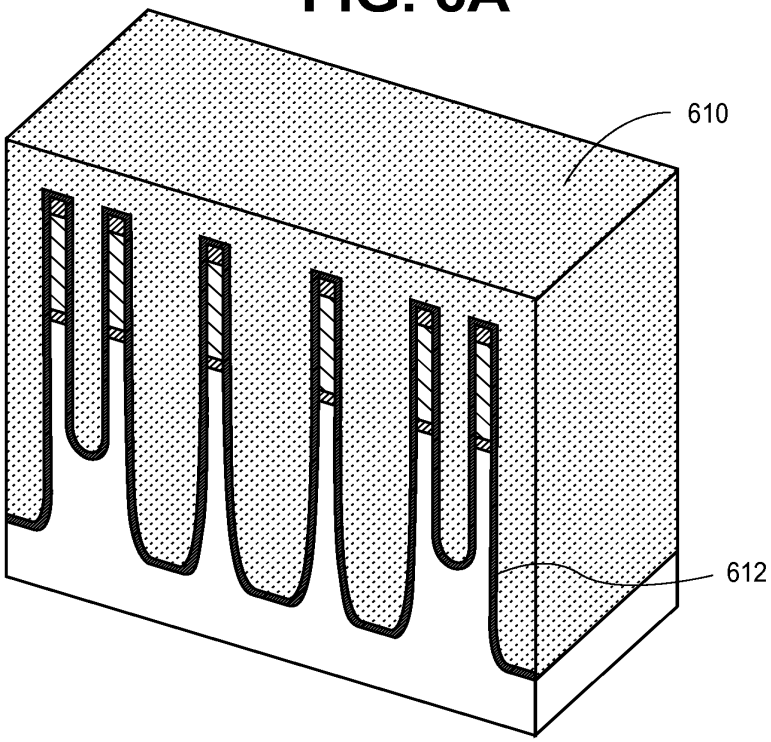


FIG. 6B

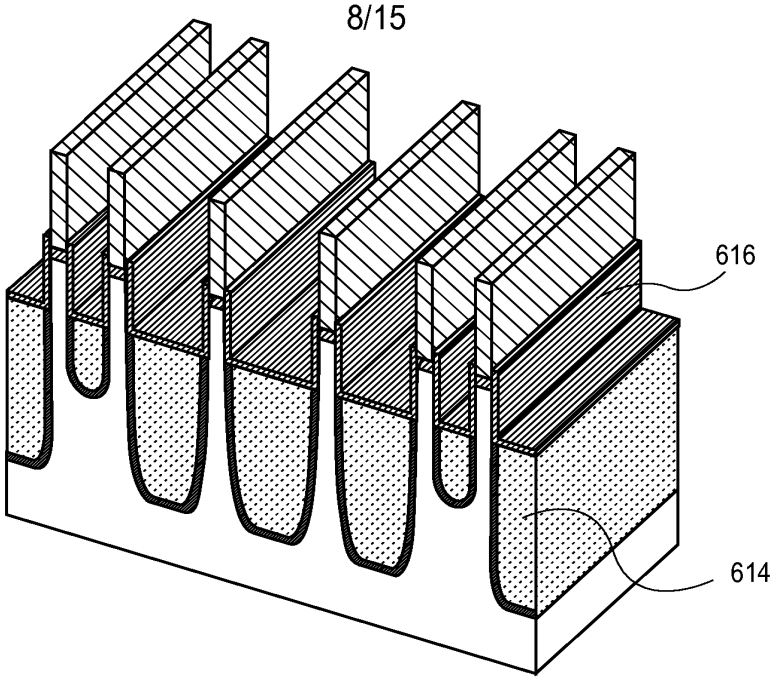


FIG. 6C

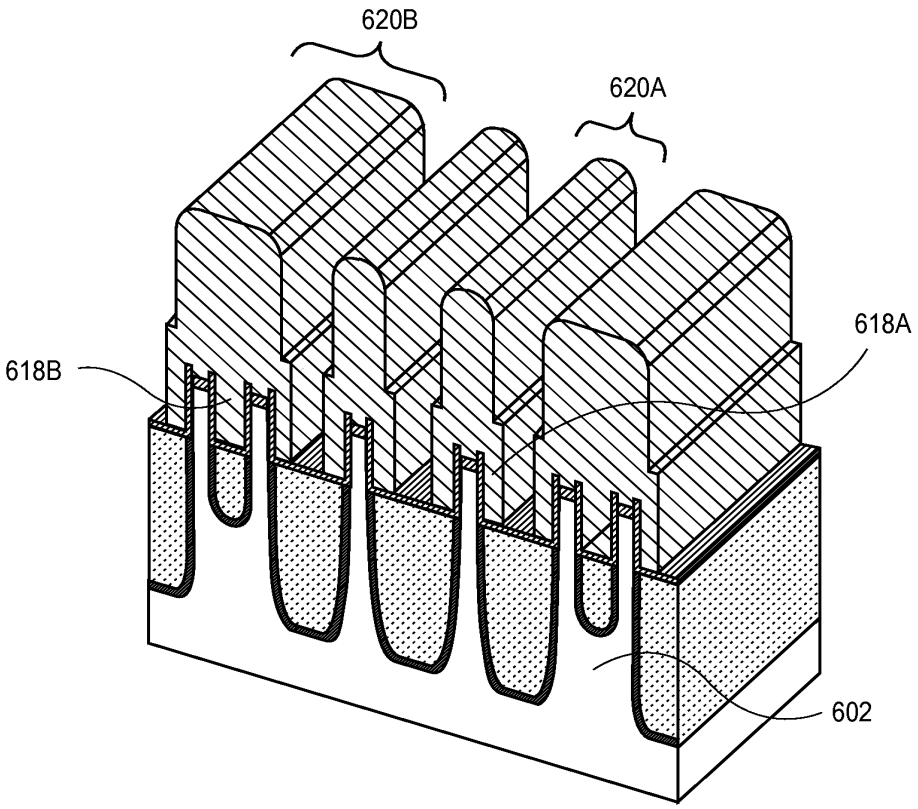


FIG. 6D

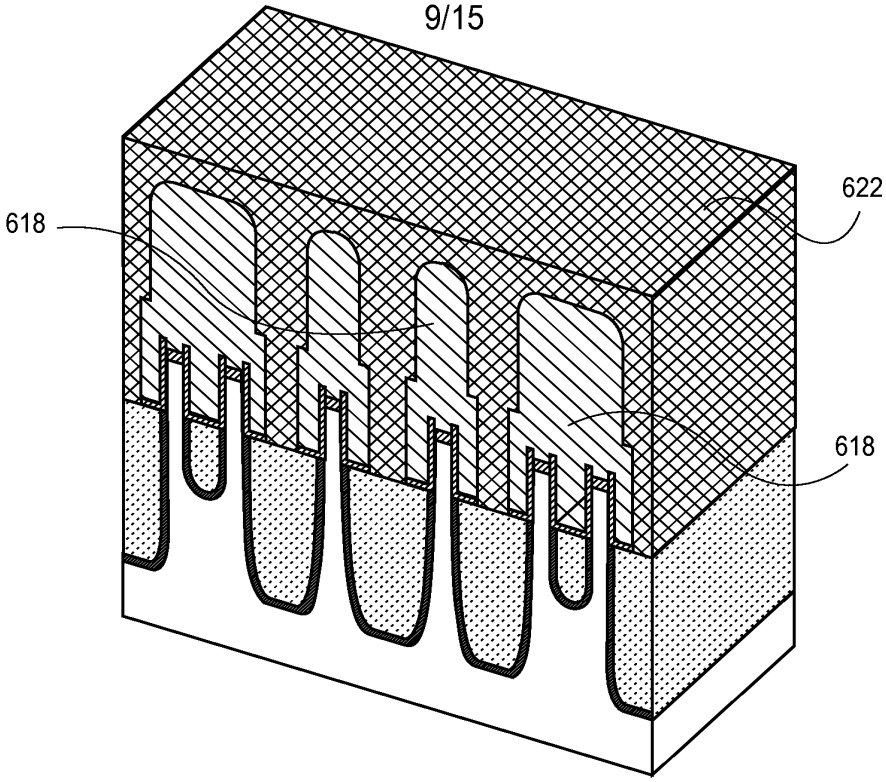


FIG. 6E

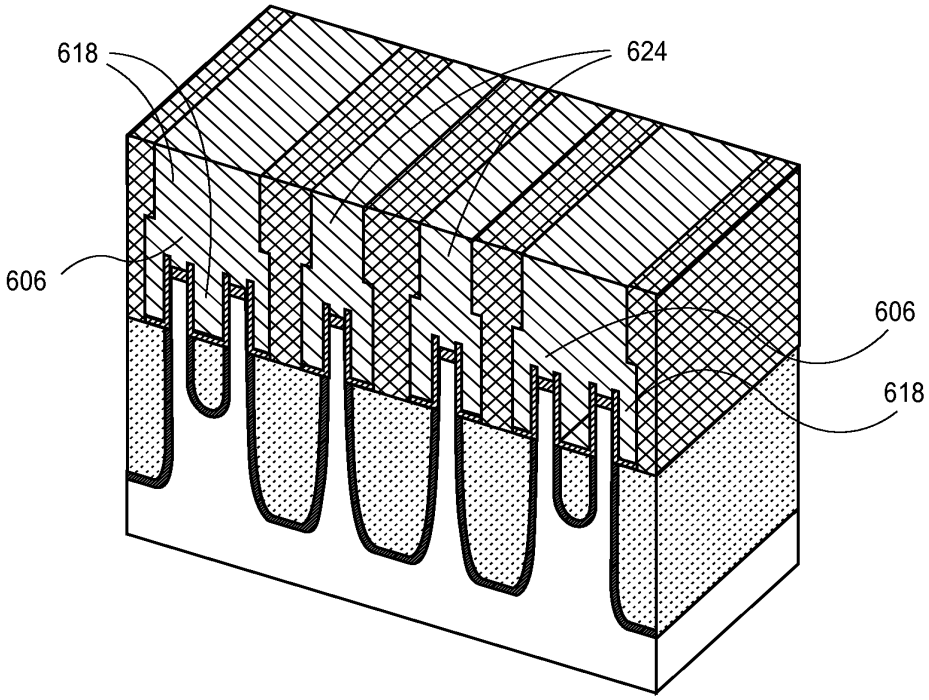


FIG. 6F

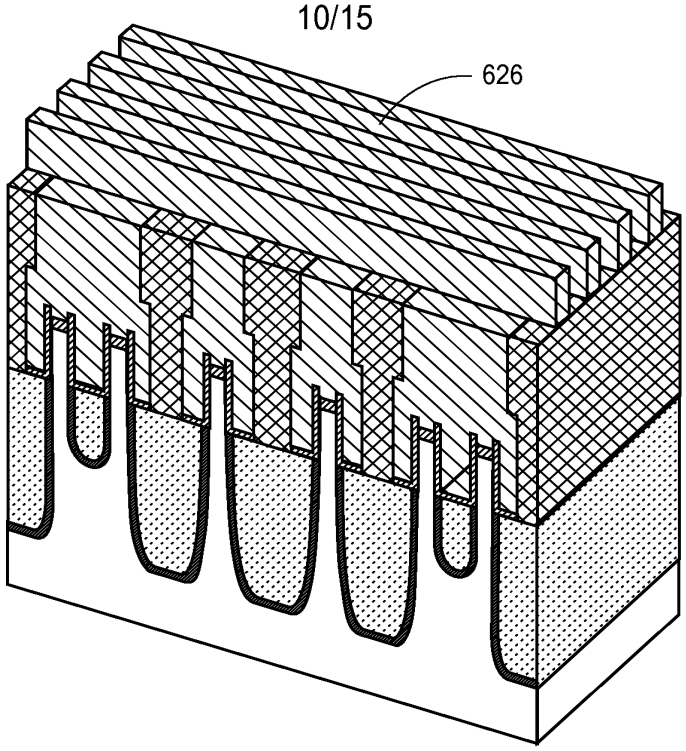


FIG. 6G

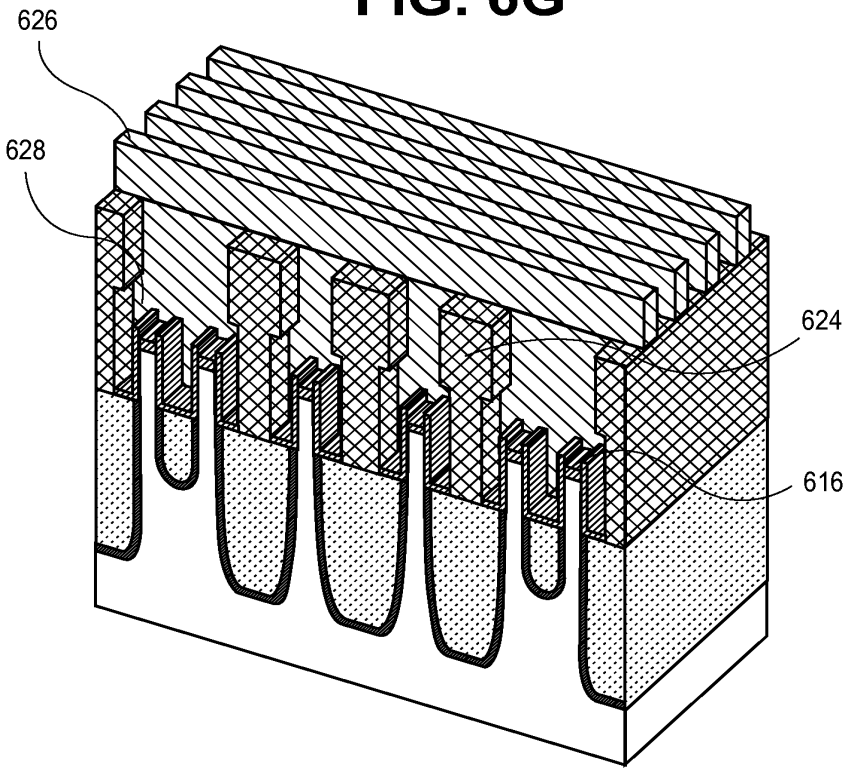


FIG. 6H

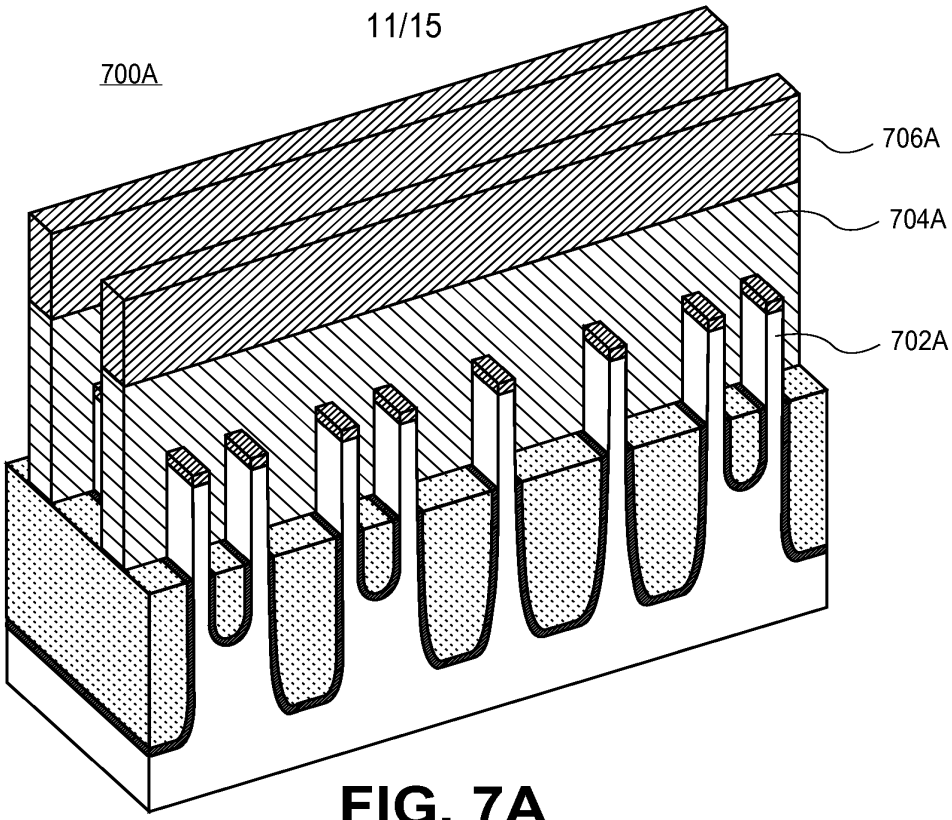


FIG. 7A

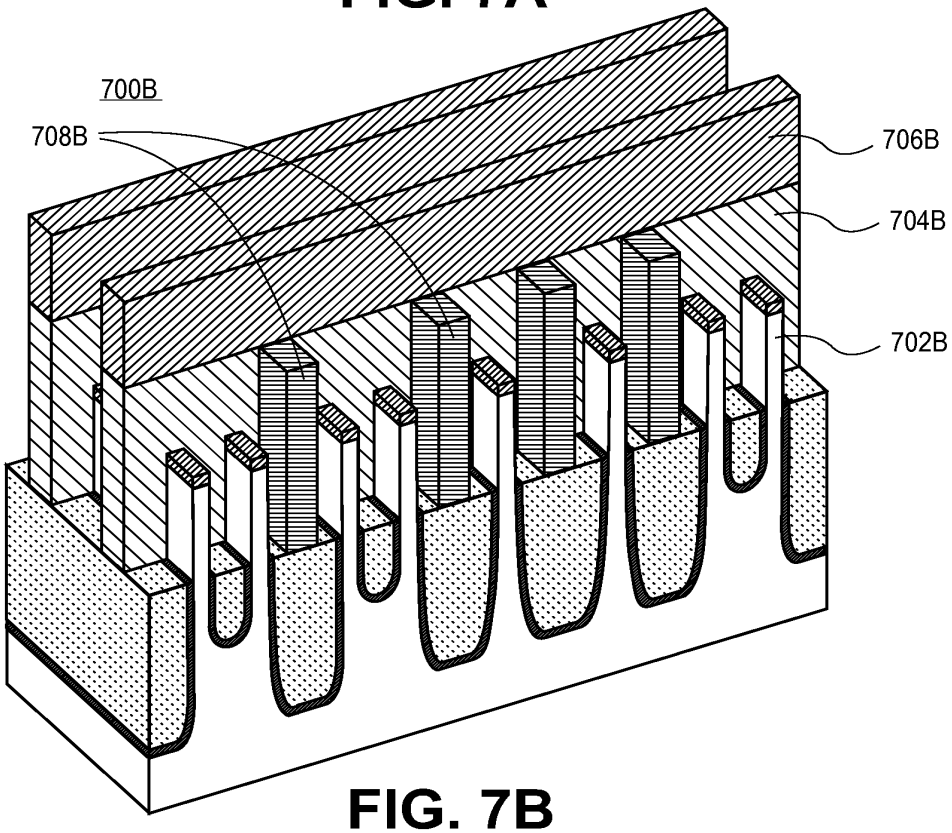


FIG. 7B

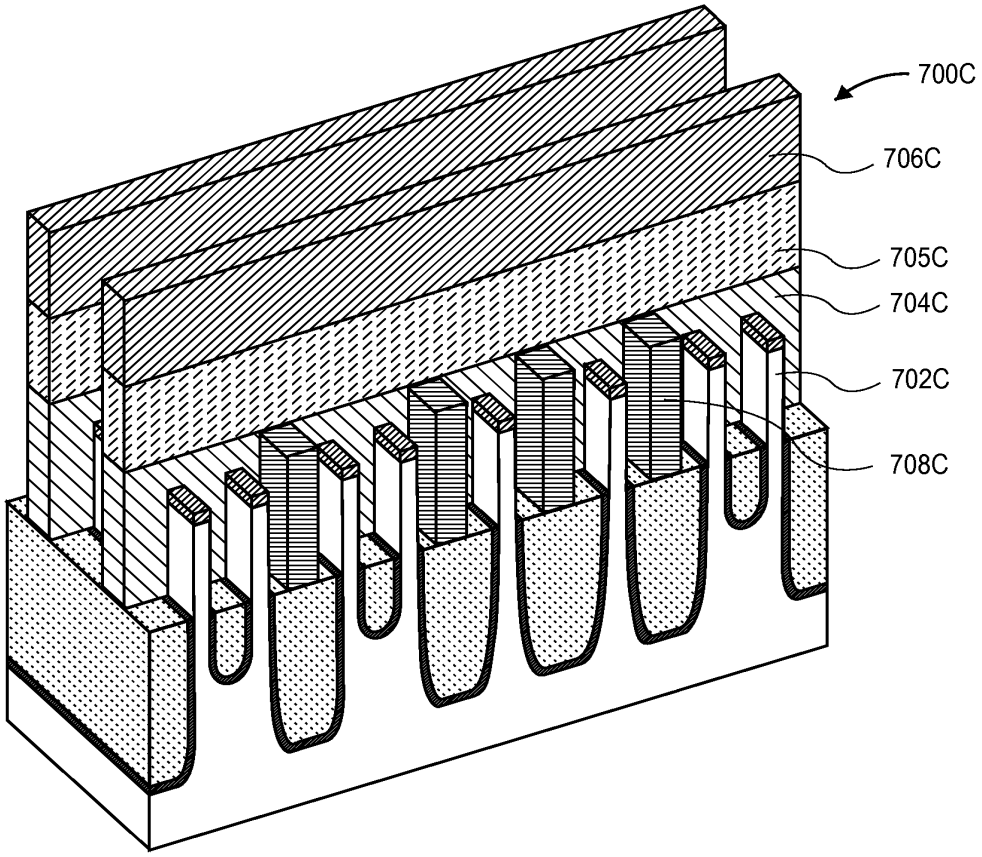


FIG. 7C

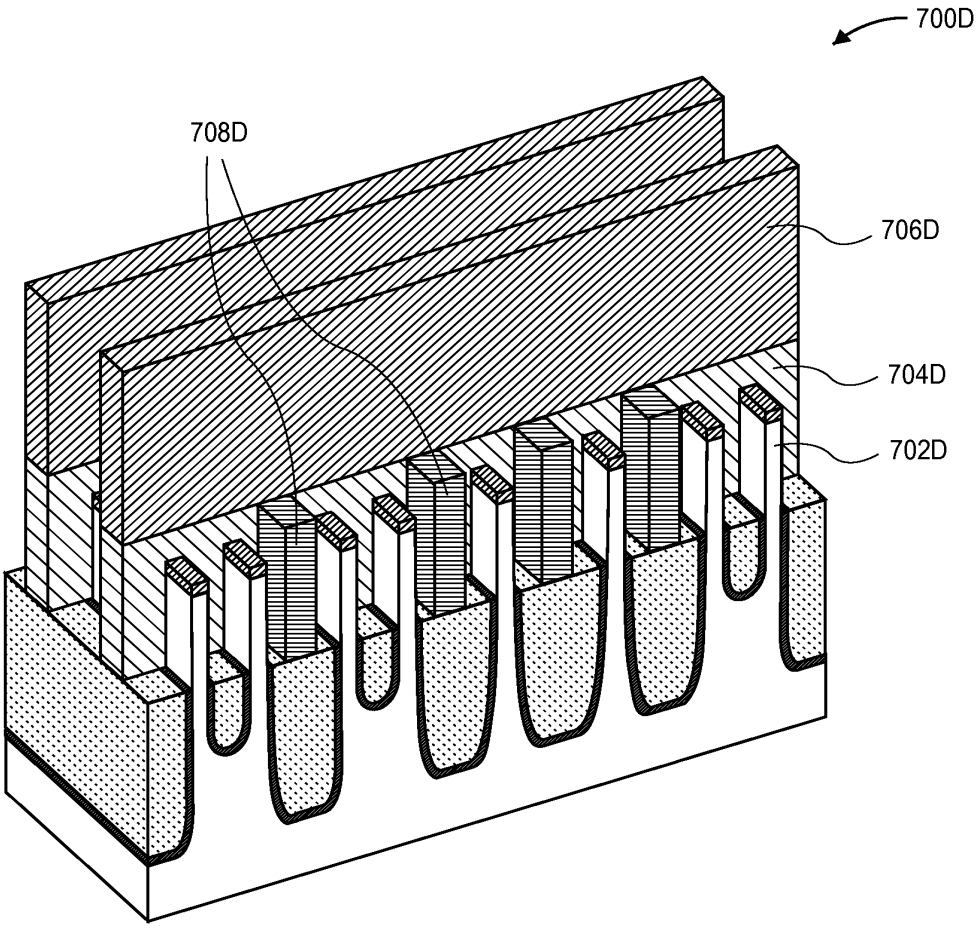


FIG. 7D

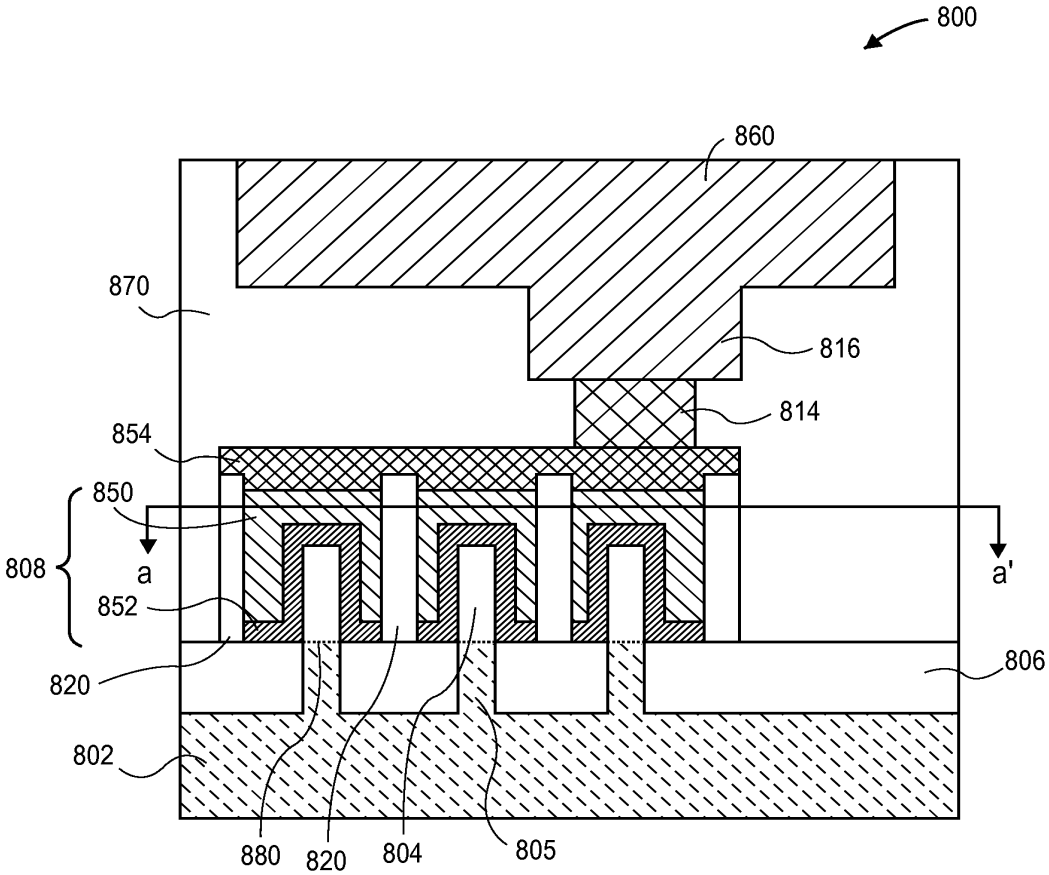

800
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870
816
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a
a'
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805

FIG. 8A

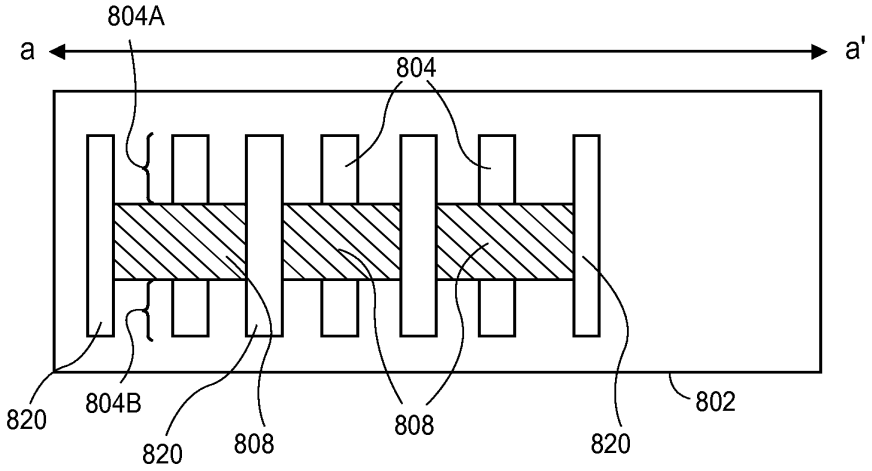

804A
a
a'
804
820
804B
820
808
808
820
802

FIG. 8B

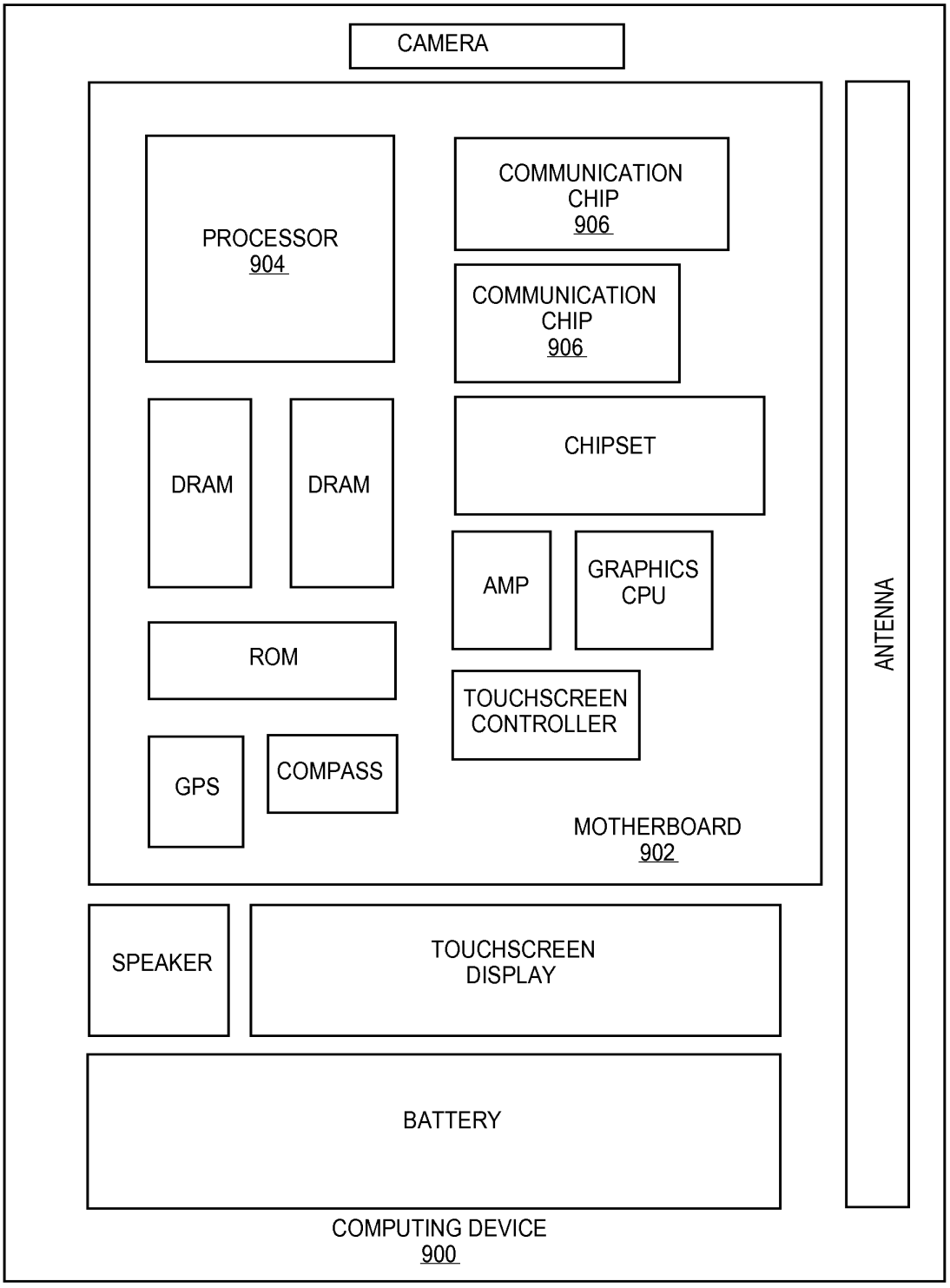

CAMERA
PROCESSOR
904
COMMUNICATION
CHIP
906
COMMUNICATION
CHIP
906
DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD
902
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE
900

FIG. 9