IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Milton Clair Webb, et al.	
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DECLARATION OF DAVID KUAN-YU LIU

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I, David Kuan-Yu Liu, declare the following:

I. QUALIFICATIONS AND BACKGROUND INFORMATION

1. My education and experience are described more fully in the attached curriculum vitae. For ease of reference, I have highlighted certain information below.

A. Educational Background

2. I received a Bachelor of Science degree in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

B. Professional Experience

3. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

4. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD's CMOS-based 0.5um and 0.35um Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for

accommodating x-decoder transistors and high voltage transistors for negative gate erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

5. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

6. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

7. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm). The flash memory products I developed at Xilinx are used as the configuration memory for the FPGA, with the configuration interface between them being the JTAG interface.

8. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

9. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

10. I have 20 years of experience as an engineer and engineering manager/director of Complementary Metal Oxide Semiconductor (CMOS) technology development. During my career, I have worked at some of the leading technology companies in the world, such as Texas Instruments, Advanced Micro Devices, Altera Corporation (now a subsidiary of Intel Corp.), and Xilinx. At these companies, my work focused on various aspects of CMOS and semiconductor technology.

11. I hold over 99 U.S. patents, a large number of which are directed to logic CMOS processes technology and high voltage CMOS process technology. The vast majority of my patents are in the area of CMOS process technology and memory architecture. As such, I am intimately familiar with the implementation of integrated process flows that essentially are repetitive sequences of modules, each composed of a layer patterning step followed by selective deposition and etching of various semiconductor materials, with the area of selectivity dictated by the

layer patterning. I am also familiar with the different layout techniques, including the use of various interconnect layers, to achieve compact array density. I also have worked on FinFET technologies, and hold U.S. Patent No. 10,629,607, directed to FinFET technology for non-volatile memory.

12. I have been retained on behalf of Samsung Electronics Co., Ltd., to offer technical opinions relating to U.S. Patent No. 9,831,306 ("the '306 Patent") and prior art references related to its subject matter. I have reviewed the '306 Patent and the following references.

- U.S. Patent Pub. No. 2015/0054078 to Xie ("Xie") (SAMSUNG-1004)
- U.S. Patent No. 9,397,217 to Tseng ("Tseng") (SAMSUNG-1005)
- U.S. Patent Pub. No. 2007/0080380 to Chang ("Chang") (SAMSUNG-1009)
- U.S. Patent No. 9,324,790 to Akarvardar ("Akarvardar") (SAMSUNG-1010)

13. I have also reviewed various supporting references, including the following, and other documentation as further noted in my opinions below.

- SAMSUNG-1006 U.S. Patent Pub. No. 2012/0086055 to Anderson ("Anderson")
- SAMSUNG-1007 U.S. Patent No. 9,041,125 to Lin ("Lin")

- SAMSUNG-1008 U.S. Patent Pub. No. 2013/0026572 to Kawa ("Kawa")
- SAMSUNG-1011 U.S. Patent No. 8,994,116 to Gan ("Gan")
- SAMSUNG-1012 U.S. Patent No. 11,037,923 to Bohr ("Bohr")
- SAMSUNG-1013 U.S. Patent No. 7,898,037 to Chuang ("Chuang")
- SAMSUNG-1014 U.S. Patent No. 9,166,053 to Kuo ("Kuo")
- SAMSUNG-1015 U.S. Patent Pub. No. 2013/0164924 to Shieh ("Shieh")
- SAMSUNG-1017 U.S. Patent No. 9,196,613 to Basker ("Basker")
- SAMSUNG-1025 U.S. Patent No. 9,281,378 to Ching ("Ching")
- SAMSUNG-1026 U.S. Patent No. 6,894,357 to Guo ("Guo")
- SAMSUNG-1027 U.S. Patent No. 7,586,159 to Lee ("Lee")
- SAMSUNG-1028 U.S. Patent Pub. No. 2006/0220090 to Metz ("Metz")
- SAMSUNG-1029 U.S. Patent Pub. No. 2015/0200275 to Zhu ("Zhu")
- SAMSUNG-1030 U.S. Patent No. 8,637,931 to Basker ("Basker-931")
- SAMSUNG-1031 U.S. Patent No. 8,697,515 to Yin ("Yin")
- SAMSUNG-1034 U.S. Patent No. 7,632,745 to Chen ("Chen")

- SAMSUNG-1035 U.S. Patent No. 9,246,003 to Cheng ("Cheng")
- SAMSUNG-1036 U.S. Patent No. 7,592,675 to Liaw ("Liaw")
- SAMSUNG-1037 U.S. Patent No. 9,214,529 to Chang ("Chang-529")
- SAMSUNG-1038 U.S. Patent Pub. No. 2011/0031552 to Iwamatsu ("Iwamatsu")
- SAMSUNG-1039 U.S. Patent No. 9,461,143 to Pethe ("Pethe")
- SAMSUNG-1040 U.S. Patent No. 8,901,665 to Kelly ("Kelly")
- SAMSUNG-1041 U.S. Patent No. 6,720,619 to Chen ("Chen-619")

14. Counsel has informed me that I should consider these materials through the lens of one of ordinary skill in the art related to the '306 Patent at the time of the earliest possible priority date of the '306 Patent, and I have done so during my review of these materials. The '306 Patent claims the benefit of priority to a PCT application filed December 19, 2013 ("the Critical Date"). Counsel has informed me that the Critical Date represents the earliest possible priority date to which the challenged claims of '306 Patent are entitled, and I have therefore used that Critical Date in my analysis below.

15. I have no financial interest in the parties or in the outcome of this proceeding. I am being compensated for my work as an expert on an hourly basis.

My compensation is not dependent on the outcome of these proceedings or the content of my opinions.

16. In writing this declaration, I have considered the following: my own knowledge and experience, including my work experience in the fields of mechanical engineering, computer science, biomedical engineering, and electrical engineering; and my experience in working with others involved in those fields. In addition, I have analyzed various publications and materials, in addition to other materials I cite in my declaration.

17. My opinions, as explained below, are based on my education, experience, and expertise in the fields relating to the ’306 Patent. Unless otherwise stated, my testimony below refers to the knowledge of one of ordinary skill in the art as of the Critical Date, or before. Any figures that appear within this document have been prepared with the assistance of Counsel and reflect my understanding of the ’306 Patent and the prior art discussed below.

II. OVERVIEW OF CONCLUSIONS FORMED

18. This declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions, based upon my knowledge and experience and my review of the prior art publications listed above, I believe that:

- Claims 26-29 and 31 are obvious over Chang and Tseng;
- Claims 26-29 and 31 are obvious over Akarvardar and Xie; and

- Claims 26-29 and 31 are obvious over Akarvardar, Xie, and Tseng

III. LEVEL OF ORDINARY SKILL IN THE ART

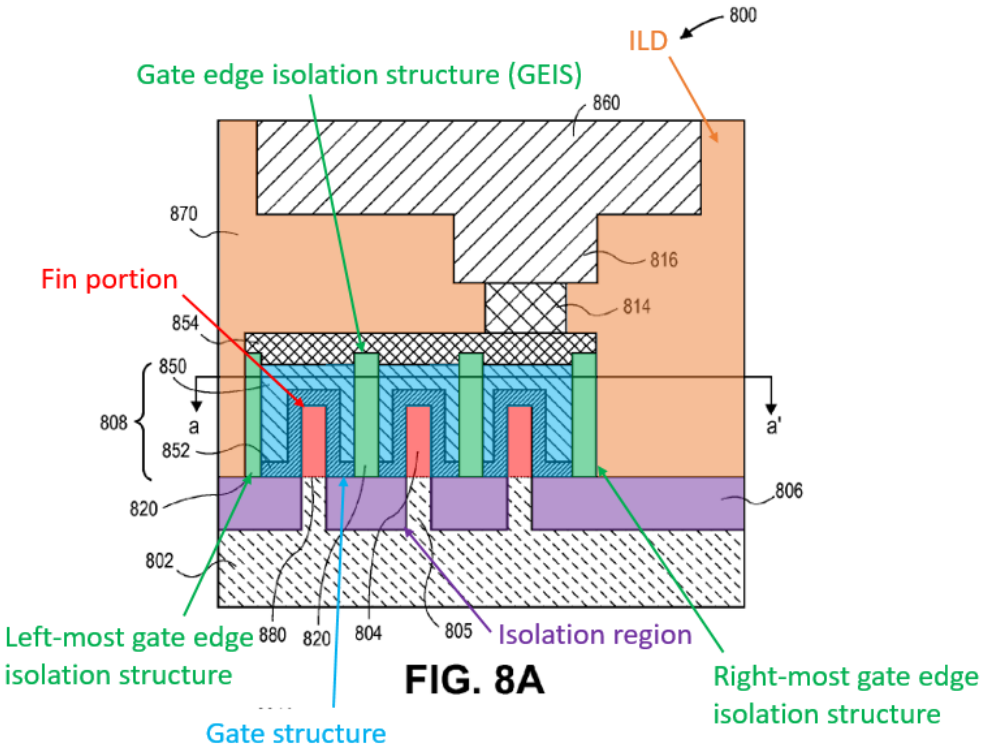
19. In my opinion, one of ordinary skill in the art relating to, and at the time of, the invention of the '306 Patent would have been a person with a Master's degree in electrical engineering, physics, or a related field, and two years of work experience in integrated circuit design or manufacturing.

20. Based on my experiences, I have a good understanding of the capabilities of one of ordinary skill. Indeed, I have participated in organizations and worked closely with many such persons over the course of my career. Based on my knowledge, skill, and experience, I have an understanding of the capabilities of one of ordinary skill. For example, from my industry experience, I am familiar with what an engineer would have known and found predictable in the art. Furthermore, I possess those capabilities myself.

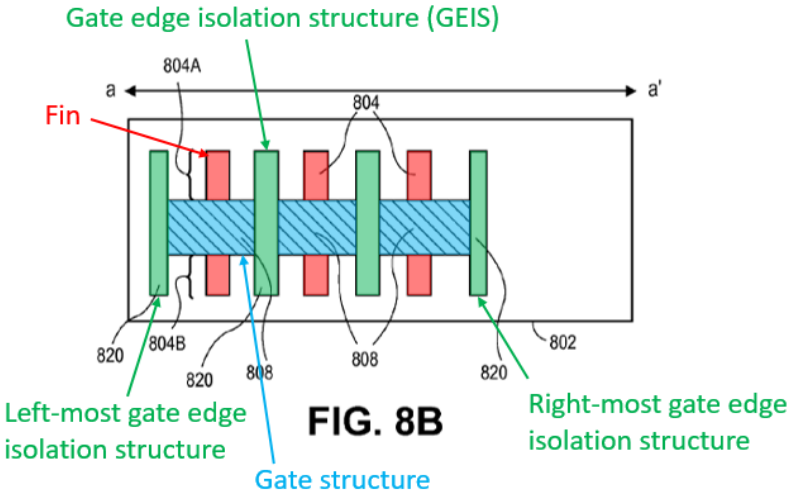
IV. THE '306 PATENT

A. Overview of the '306 Patent

21. The '306 Patent is said to describe "[s]elf-aligned gate edge and local interconnect structures." SAMSUNG-1001 ('306 Patent), Abstract. An example of such a structure—specifically, a "non-planar semiconductor device having self-aligned gate isolation"—is shown in "a cross-sectional view and a plan view" in FIGS. 8A-8B, *infra*. *Id.*, 9:27-30.



Excerpt from ’306 Patent, FIG. 8A (annotated)



Excerpt from ’306 Patent, FIG. 8B (annotated)

22. This semiconductor device includes “non-planar active regions (e.g., a fin structures [sic] including protruding fin portion 804 and sub-fin region 805)

formed from substrate 802, and within isolation region 806." SAMSUNG-1001 ('306 Patent), 9:34-37; *see* claim 26. I have highlighted the protruding fin portions 804 in red and the isolation region 806 in purple. "Gate structures 808," highlighted in blue, are "disposed over the protruding portions 804 of the non-planar active regions as well as over a portion of the isolation region 806." SAMSUNG-1001 ('306 Patent), 9:37-39; *see* claim 26. "Gate structures 808 are separated by self-aligned gate edge isolation structures 820," green. *Id.*, 9:43-44; *see* claim 26.

23. Interconnects 854, 860 and contacts 814 are "disposed in inter-layer dielectric stacks or layers 870," orange. SAMSUNG-1001 ('306 Patent), 9:45-49. As shown in cross-section, the inter-layer dielectric (ILD) 870 covers the gate structures and gate edge isolation structures, and fills the space next to the exposed outer sidewalls of the right-most and left-most gate edge isolation structures (labeled in the figures above).[1]

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[1] I note that FIG. 8B does not specifically label the dielectric material 870. However, since FIG. 8B illustrates a top view through the a-a′ cut in FIG. 8A, it is my opinion that a POSITA at best would understand or find obvious that the dielectric material 870 is present at least next to the left-most and right-most gate edge isolation structures that are shown in FIG. 8B.

B. Spatial Relationships of Elements of the Challenged Claims

24. The Challenged Claims recite spatial relationships between various features of an integrated circuit structure. I have provided an overview of some of these features, and their relationships, in the following paragraphs, with reference to FIGS. 8A and 8B, reproduced throughout this section.

25. The Challenged Claims recite that the fins (red) have "a longest dimension ***along a first direction***," which I have marked in the figures below. SAMSUNG-1001 ('306 Patent), claim 26. That is, the claims indicate the orientation of the fins, and thus, the claims define an orientation that is along the first direction. Based on these figures and read in light of the specification, it is my opinion that a POSITA would understand or find obvious that the longest dimension of the fins extends from top to bottom in the top view (FIG. 8B), and correspondingly into the page in the cross-sectional view (FIG. 8A). *See id.*, Abstract, 13:47-49, 14:4-8. This direction is the first direction.

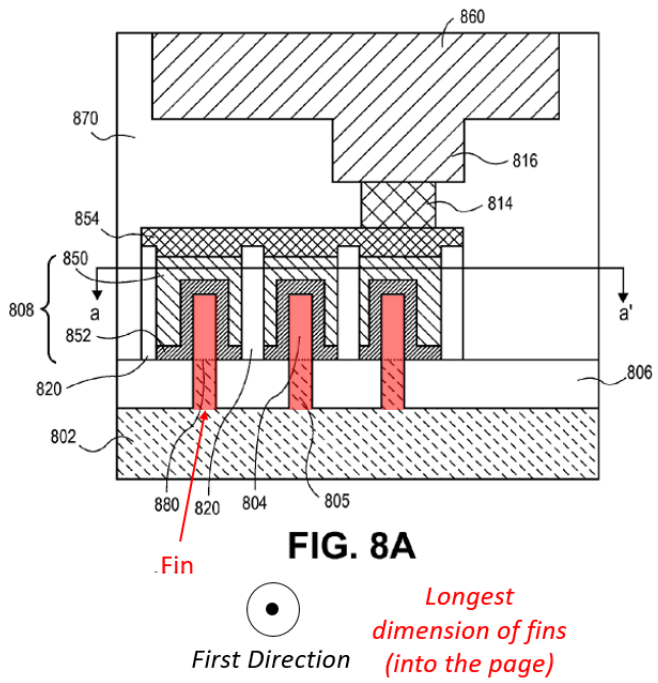


FIG. 8A

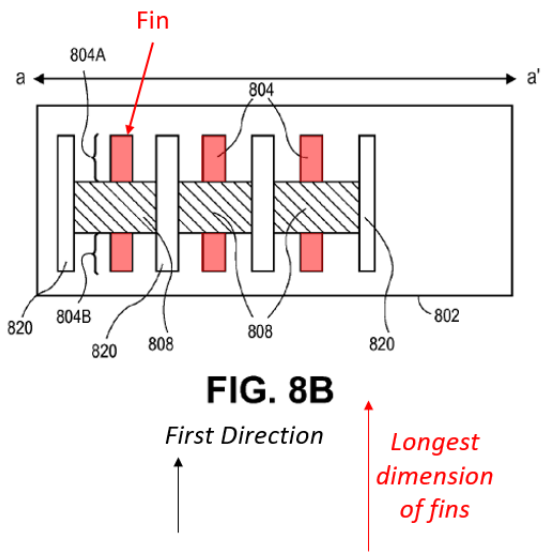
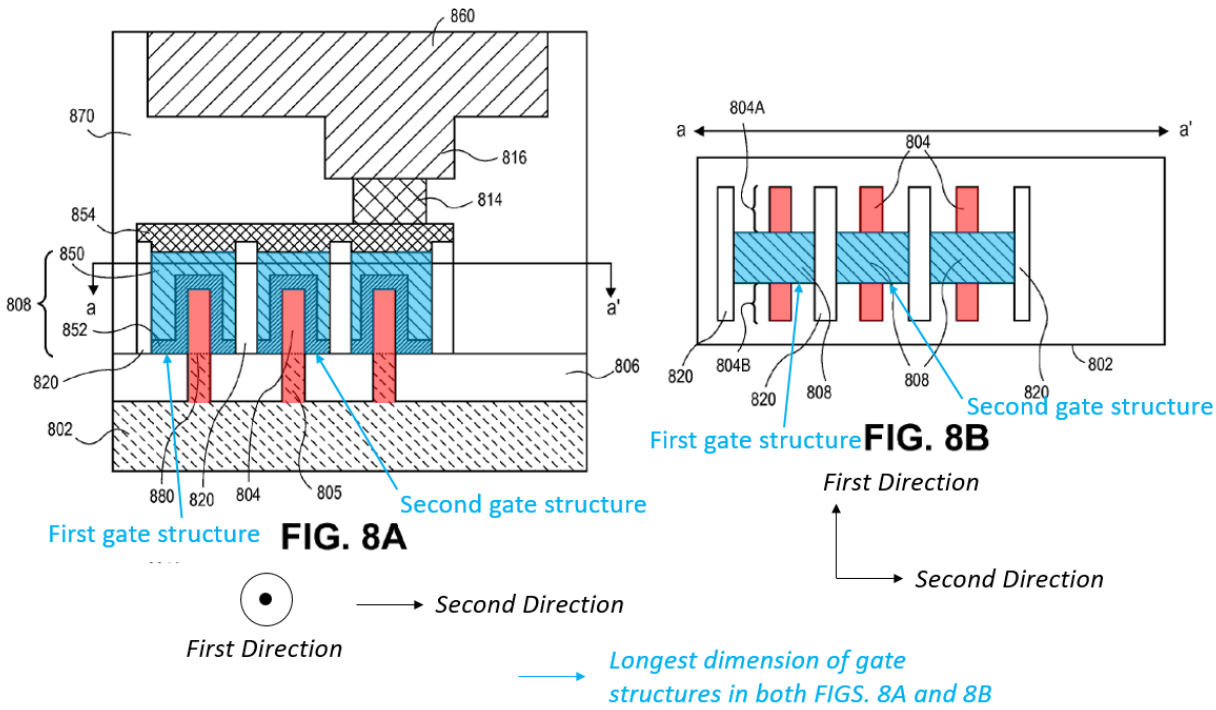
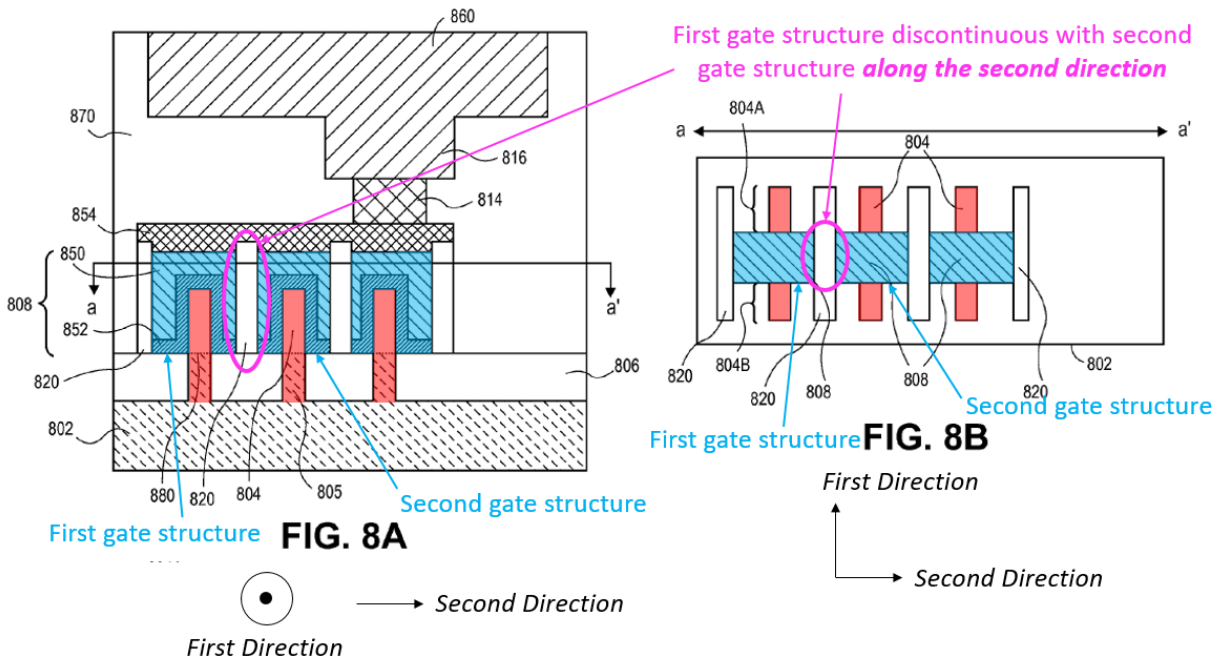


FIG. 8B

26. The Challenged Claims also recite that the gate structures have "a longest dimension ***along a second direction*** … orthogonal to the first direction." SAMSUNG-1001 ('306 Patent), claim 26. The direction orthogonal to the length of the fins (*i.e.*, orthogonal to the first direction) is the left-to-right direction in both the cross-sectional view (FIG. 8A) and top view (FIG. 8B), marked in the figures below. It is my opinion that a POSITA would have understood or found obvious that this direction is the second direction. For instance, I note that these figures illustrate gate structure dimension that appear to be longest along this direction. *See id.*, Abstract, 13:49-52, 14:8-10.



27. The Challenged Claims recite that a "second gate structure [is] discontinuous with [a] first gate structure ***along the second direction***." SAMSUNG-1001 ('306 Patent), claim 26. This discontinuity, and its orientation along the second direction, are shown in the figures below. For instance, when viewing the structure starting from the first gate structure and ***moving along the second direction*** (*i.e.*, moving from left to right in both the top view and the cross-sectional view), as a discontinuity exists (occupied by the gate edge isolation structure, discussed below) between the two gate structures before reaching the second gate structure.



28. Similarly, the Challenged Claims recite that "an edge" of the second gate structure "fac[es] an edge of the first gate structure ***along the second direction***." It is my opinion that a POSITA would have understood or considered this to be obvious when viewing the structure starting from the edge of the first gate structure (which I have outlined in pink in the figures below) and ***moving along the second direction*** to encounter the edge of the second gate structure (also outlined in pink).

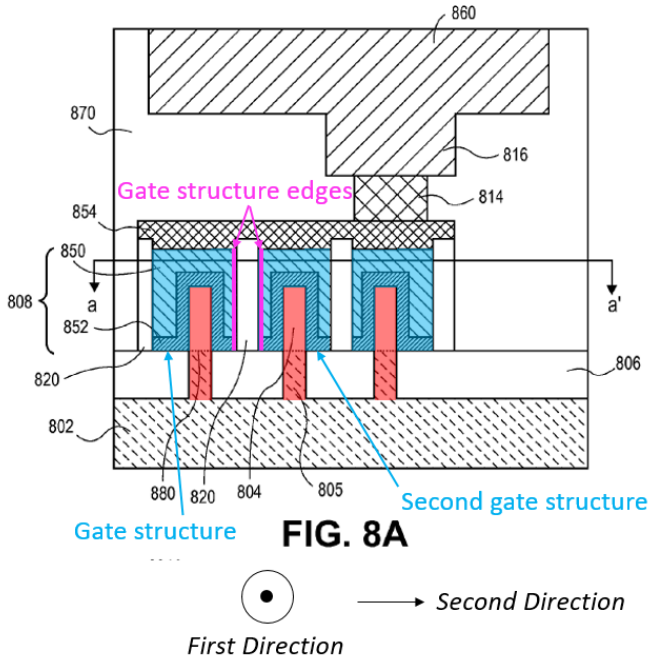


FIG. 8A

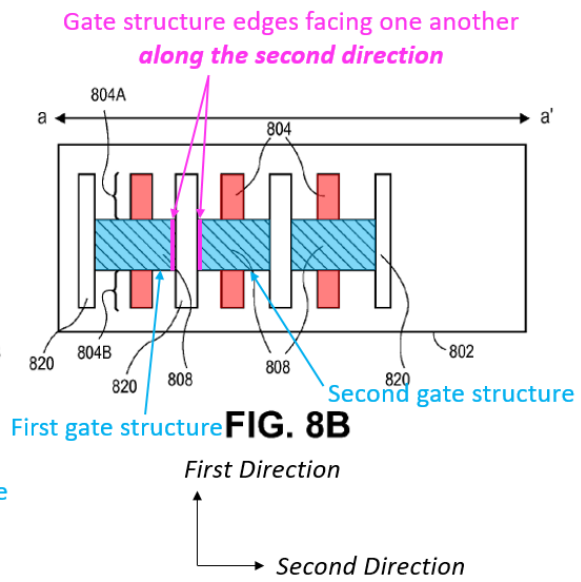
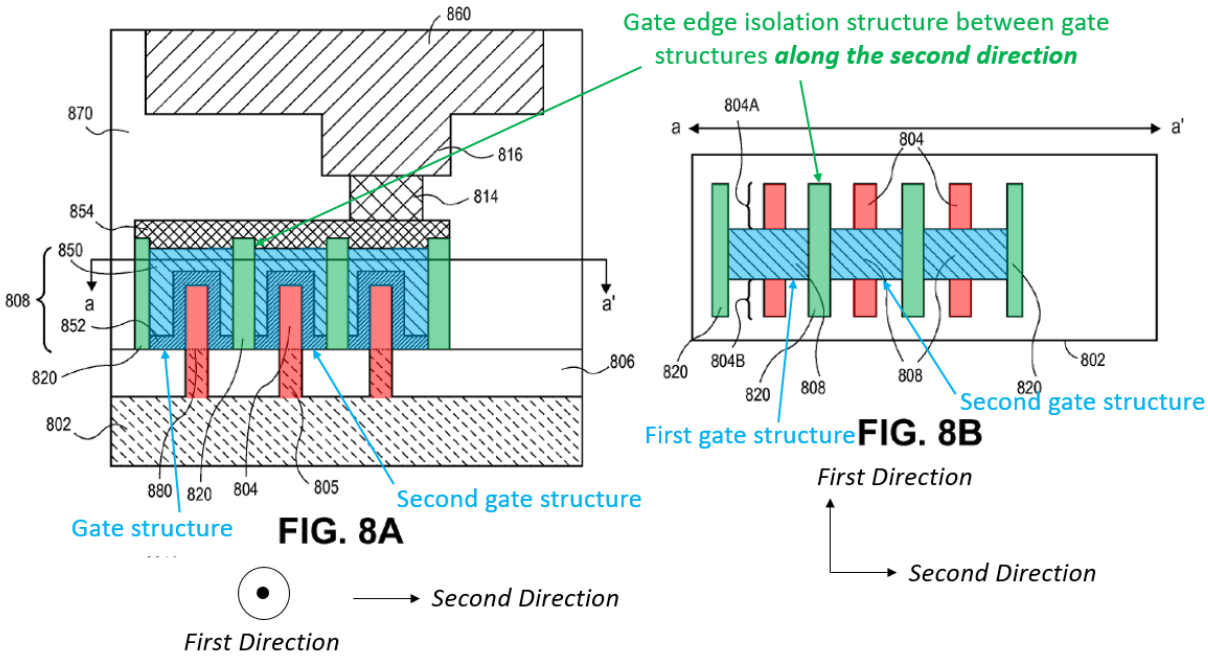


FIG. 8B

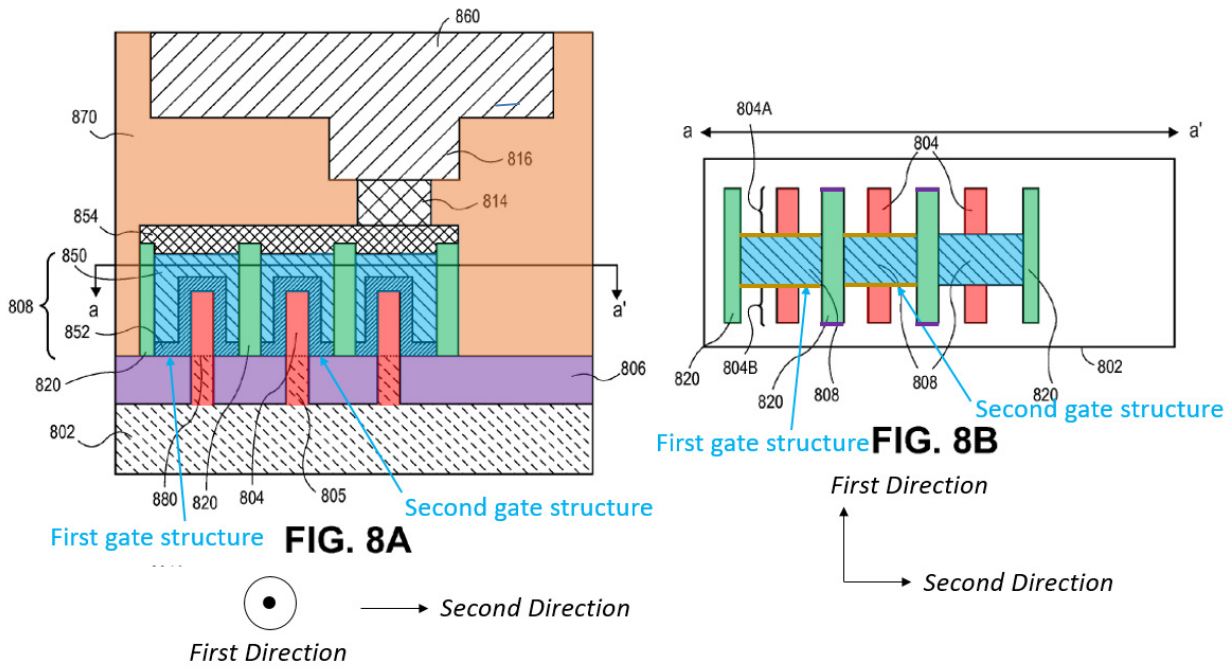
29. The gate edge isolation structure of the Challenged Claims is "between and in contact with the edge of the first gate structure and the edge of the second gate structure ***along the second direction***." SAMSUNG-1001 ('306 Patent), claim 26. As illustrated in the figures below, the gate edge isolation structure (which I have highlighted in green) is between and in contact with the edges (outlined in pink) of the gate structures ***along the second direction***: starting from the edge of the first gate structure and ***moving along the second direction***, one reaches first the gate edge isolation structure and then the edge of the second gate structure. Notably, the '306 Patent provides no illustration or description of a gate edge isolation structure between and in contact with edges of gate structures in an arrangement such that starting from the edge of the first gate structure and moving in the orthogonal direction (*e.g.*, from top to bottom in the top view

figure), one would reach first the gate edge isolation structure and then the edge of the second gate structure.



30. The Challenged Claims also recite that the "dielectric material [is] laterally adjacent to the first and second gate structures ***along the first direction***" and "laterally adjacent to the gate edge isolation structure … ***along the first direction***." SAMSUNG-1001 ('306 Patent), claim 26. I interpret these limitations consistent with the use of the phrase "along the second direction" (discussed in the previous paragraphs). For instance, as shown in the figures below, a dielectric material would be laterally adjacent to the gate structures (blue) ***along the first direction*** if it wereat the sidewalls of the gate structures (outlined in pink in FIG. 8B, reproduced again *infra*). Similarly, a dielectric material would be laterally adjacent to the gate edge isolation structure (green) ***along the first direction*** if it

were at the short ends of the gate edge isolation structure (outlined in purple in FIG. 8B).



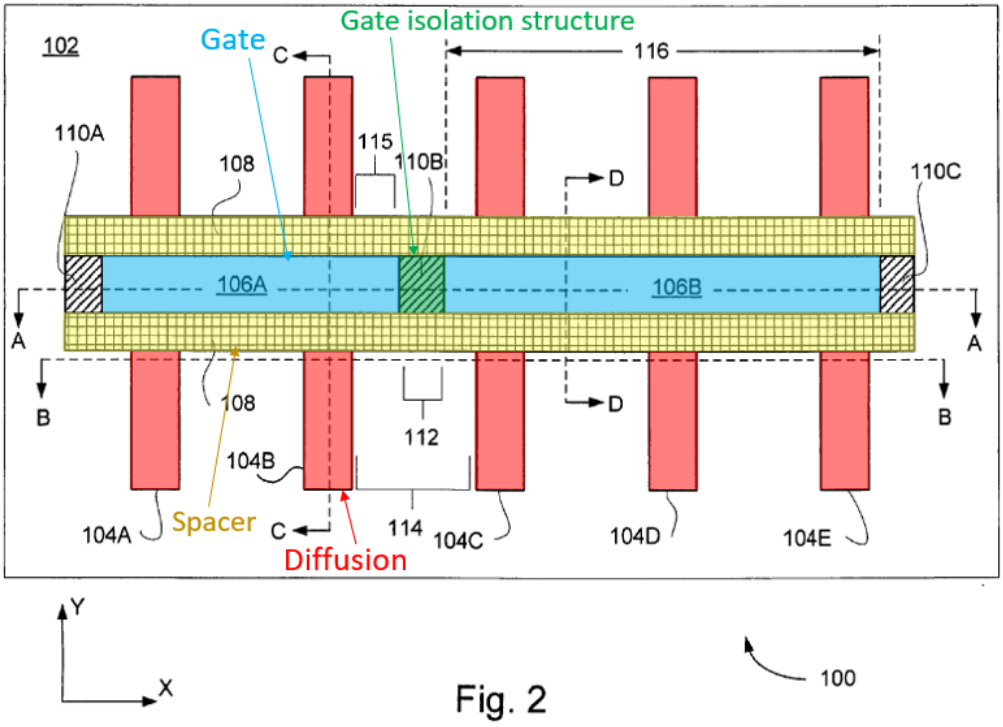
V. PRIOR ART ANALYSIS

A. [GROUND 1] – CLAIMS 26-29 AND 31 ARE OBVIOUS OVER CHANG AND TSENG

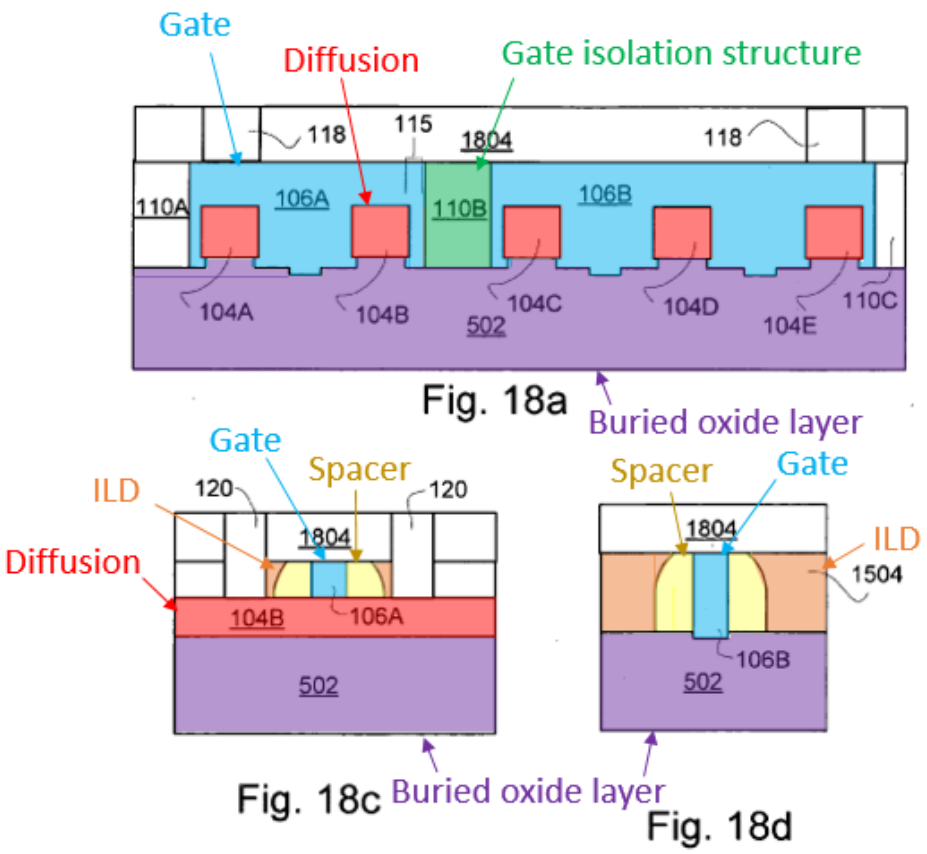
1. Chang describes tri-gate transistors with self-aligned isolation regions and gates

31. Chang describes "forming self-aligned gates on transistors," *e.g.*, for "a tri-gate transistor." SAMSUNG-1009 (Chang), [0035], [0046]. Chang's FIG. 2, reproduced below, is "a top view that illustrates a portion of a circuit 100 that includes transistors with end caps of gates 106," highlighted in blue, "self-aligned to diffusions 104," which I have highlighted in red. SAMSUNG-1009 (Chang), [0036]. This circuit is also shown in its cross-section side view in Chang's FIGS.

18a and 18c-18d, also reproduced below. *See id.*, [0056] (FIG. 18a is a cross-sectional side view, taken through line A-A of FIG. 2," and FIGS. 18c and 18d "are cross-sectional side views that illustrate the circuit 100 at the same stage of fabrication through lines … C-C, and D-D of FIG. 2, respectively." *Id.*, [0056].



Excerpt from Chang, FIG. 2 top-view (annotated)



Excerpt from Chang, FIGS. 18a, 18c-18d cross-sectional views (annotated)

32. Chang's diffusions 104 (red) are formed on a substrate, such as on "a bulk silicon wafer" or on "a silicon-on-insulator (SOI) substrate" that "includes a buried oxide layer 502," shown in purple. SAMSUNG-1009 (Chang), [0040]. For instance, the diffusions are formed from a semiconductor layer of an SOI substrate. *See* SAMSUNG-1009 (Chang), [0041], FIGS. 5-6, 10. The formation of Chang's diffusions is shown in FIGS. 5-6, below, and involves using a "patterned photoresist 510" "to remove portions of the hardmask layer 508, the pad oxide layer 506, and the semiconductor layer 504," resulting in the formation of

"diffusions 104, each isolated from each other … where the substrate 102 is an SOI substrate." SAMSUNG-1009 (Chang), [0041]. After further processing (illustrated in FIGS. 7-9 and described in Chang's [0042]-[0045]," the pad oxide layer 506 is removed "to expose the diffusions 104." *Id.*, [0046]; *see* FIG. 10.

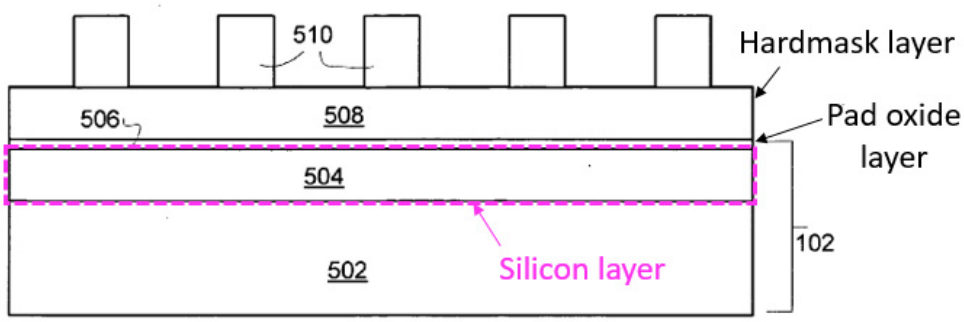


Fig. 5

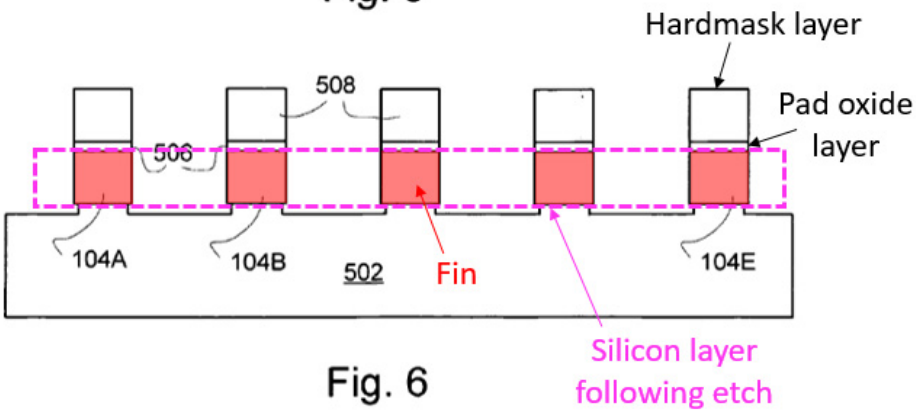


Fig. 6

Excerpts from Chang, FIGS. 5-6 (annotated)

33. "[G]ate isolation structures 110," one of which I have highlighted in green, are formed "self-aligned to the diffusions 104." SAMSUNG-1009 (Chang), [0036]; *see* [0043]-[0044]. "[G]ates 106," highlighted in blue, are formed "self-aligned to the isolation structures 110." *Id.*, [0036].

34. Because of the self-alignment process, "the distance 112 between gates may not depend on the lithography alignment accuracy but rather be pre-defined by the distance between diffusions 104A and 104B" and by the thickness of a spacer layer used during the fabrication process. SAMSUNG-1009 (Chang), [0044]; *see* FIG. 2, above. The spacer layer 702 is illustrated in FIG. 7, below, which shows an interim structure "after formation of a spacer layer 702 on the diffusions 104, pad oxide layer 506, and hardmask 508," and before the deposition of an insulating material that will form the gate isolation structures. *Id.*, [0042]; *see* [0043]. This allows "the distance 114 between diffusions 104 and gates 106 [to] be smaller than if the placement of gates 106 were dependent on the alignment and minimum resolution of a lithography system, and had to take alignment errors and critical dimensions into account." *Id.*, [0036]; *see* [0056], FIG. 2.

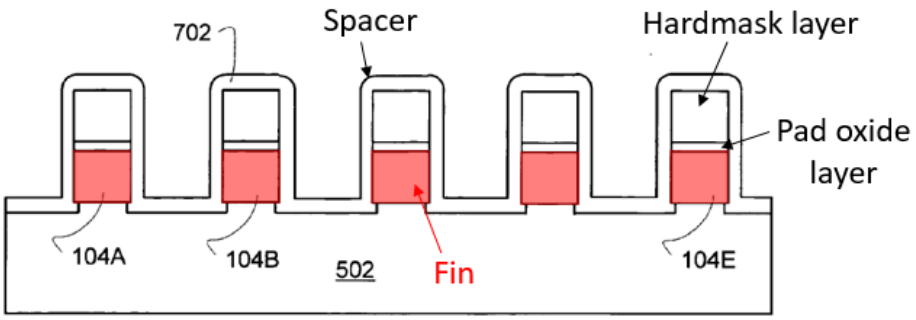


Fig. 7

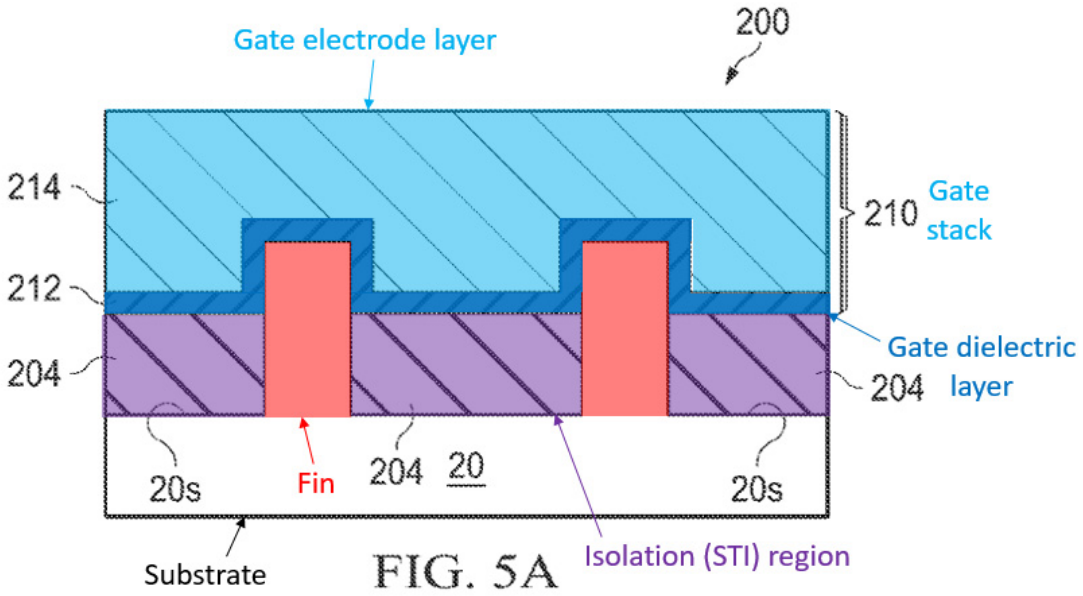
Excerpt from Chang, FIG. 7 (annotated)

35. Chang indicates that the gate structures can be "made by a replacement gate process" in which "a final metal gate and gate dielectric replace" a place-holder gate material. *Id.*, [0047], [0050]. Chang also indicates that alternatively, the gate structures can be made in a gate-first process in which a "first gate material 1102" and a "gate dielectric (not shown) are "the material of the gate in the final transistor." *Id.*, [0047]; *see* FIGS. 11-16.

36. Chang's circuit also includes "spacers 108," which I have highlighted in yellow, "on either side of the gates 106" and on either side of the isolation structures 110, as illustrated in the top view figure. SAMSUNG-1009 (Chang), [0037]. A "layer 1504 of interlayer dielectric 1502," highlighted in orange, is disposed next to the spacers 108. *Id.*, [0051].

2. Tseng describes FinFET devices having fins isolated by STI regions

37. Tseng describes a FinFET semiconductor device that includes "a fin structure 202 (comprising a first fin 202a of the substrate and a second fin 202b of the substrate 20," which I have highlighted in red in FIG. 5A, below. SAMSUNG-1005 (Tseng), 3:4-9; *see* FIG. 2. The fins 202 are formed by etching the substrate 20 to "form trenches 206a," where "[e]ach portion of the substrate 20 between trenches 206a forms one semiconductor fin." *Id.*, 3:24-25, 3:60-65; *see* FIG. 3A.



Excerpt from Tseng, FIG. 5A (annotated)

38. Tseng's trenches are "filled with a dielectric material to form the isolation regions 204 to define and electrically isolate the various fins of the fin structure." *Id.*, 4:25-27; *see* 3:9-10 ("an insulation region 204 between the first fin 202a and second fin 202b"), FIGS. 2, 5A. The isolation regions 204, which I have highlighted in purple, can be "shallow trench isolation (STI) regions." *Id.*, 4:28-32. A gate stack 210, highlighted in blue, including a "gate electrode layer 214 and [] gate dielectric layer 212" is "sequentially deposited over the substrate" and "travers[es] over the first fin 202a and second fin 202b." *Id.*, 3:4-12, 5:5-13; *see* FIG. 2, 5A. The gate dielectric layer 212, outlined in dark blue, can be a "high dielectric constant (high-k) dielectric," and the gate electrode layer 214,

highlighted in light blue, can be an "N-work function metal" or a "P-work function metal." *Id.*, 5:14-42.

3. The combination of Chang and Tseng

39. I illustrate an example of a structure of the Chang-Tseng combination in the composite figure below, noting that this figure (as well as other composite figures I include in this declaration), is just one example combination that a POSITA would have found to be obvious. I provide such composite figures for illustrative purposes only. It is my opinion that other example configurations could be conceived that also would have been obvious and that would render the challenged claims obvious for similar reasons as those discussed herein.

40. As shown in the Chang-Tseng composite figure below, the Chang-Tseng combination structure is a FinFET structure that includes elongated diffusions (shown in red in Chang's FIG. 6, immediately below) on a substrate, such as an SOI substrate, *e.g.*, as taught by Chang. *See* SAMSUNG-1009 (Chang), [0040]-[0041]. For instance, as described by Chang, the diffusions are formed by "removing portions of [a] hardmask layer 508, [a] pad oxide layer 506, and [a] semiconductor layer," thus forming "diffusions 104, each isolated from each other" "by the buried oxide layer 502" of the SOI substrate. SAMSUNG-1009 (Chang), [0041].

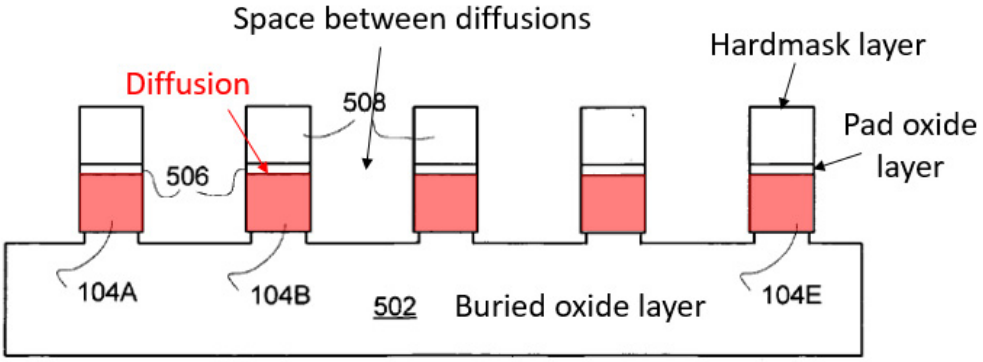
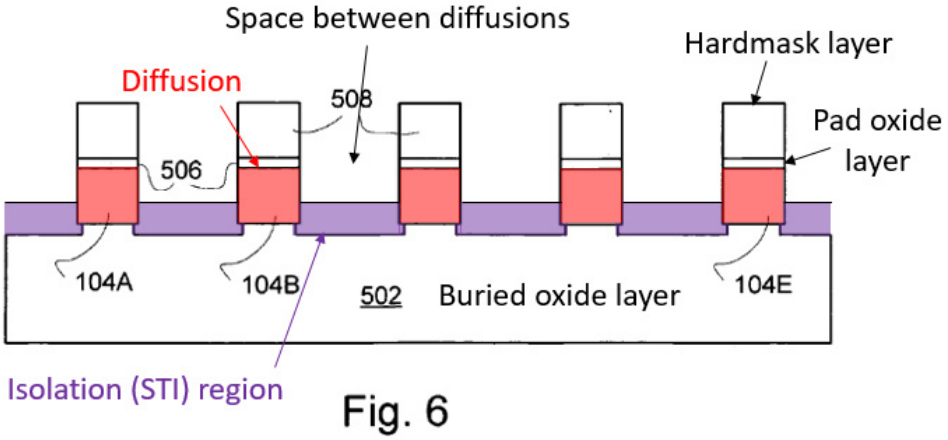


Fig. 6

Excerpt from Chang, FIG. 6 (annotated)

41. Based on the teachings of Tseng, the spaces between diffusions (*e.g.*, the spaces shown between the diffusions in Chang's FIG. 6) are "filled with a dielectric material to form isolation regions" such as "shallow trench isolation (STI) regions,. SAMSUNG-1005 (Tseng), 4:25-32; *see* FIGS. 2 and 5A. I have highlighted these STI regions in purple. The STI regions "define and electrically isolate the various fins of the fin structure." SAMSUNG-1005 (Tseng), 4:25-32.



Chang-Tseng composite figure

42. After formation of the STI regions, "gate isolation structures," shown in green in the further composite figures below, are "self-aligned" to the diffusions, *e.g.*, using a self-alignment process such as that described by Chang. SAMSUNG-1009 (Chang), [0036]; *see* [0042]-[0044], FIGS. 7-8. For instance, to form the isolation structures, a "layer of an insulating material 802" is deposited in the spaces between diffusions, and thus onto the dielectric material previously deposited between the diffusions to form the STI regions. SAMSUNG-1009 (Chang), [0042]-[0043], FIGS. 7-8; *see* SAMSUNG-1005 (Tseng), 4:25-32, FIGS. 2 and 5A. This insulating material is "used as the insulating isolation structures 110." SAMSUNG-1009 (Chang) [0044].

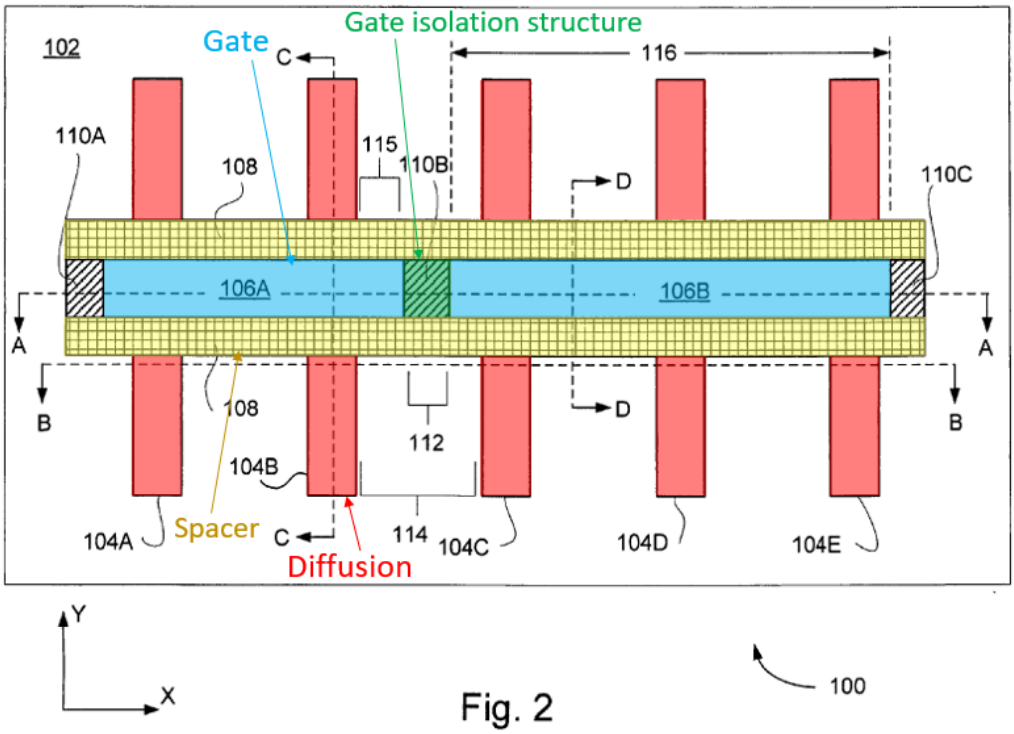
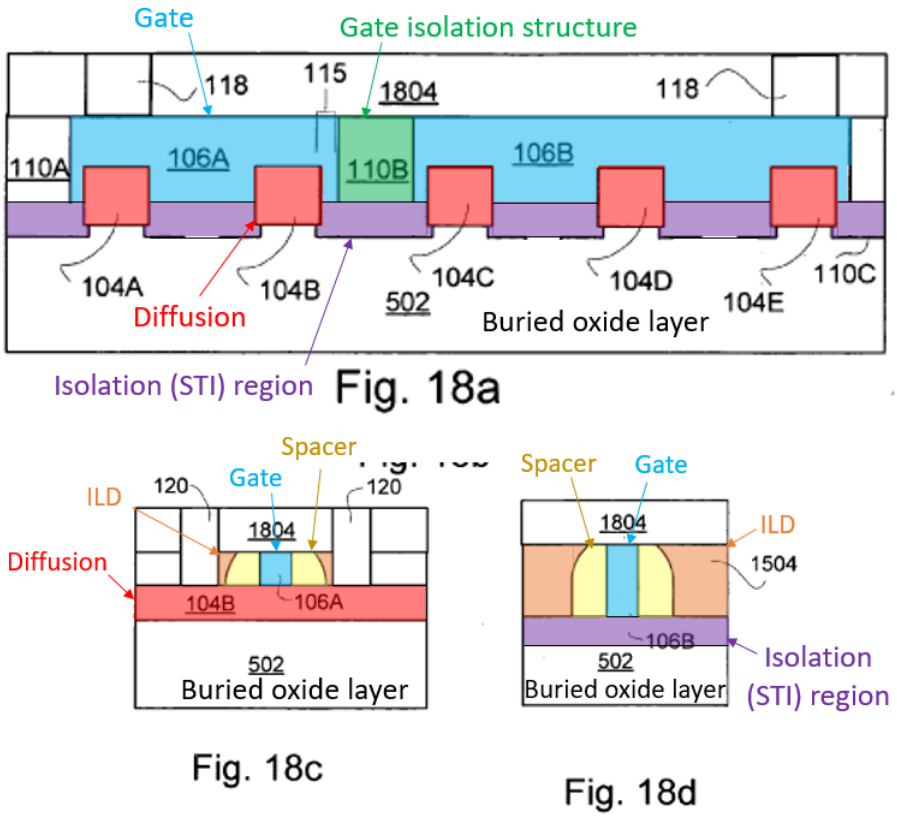


Fig. 2

Chang-Tseng top-view composite figure



Chang-Tseng cross-sectional composite figures

43. "[G]ates 106," highlighted in blue, are formed "self-aligned to the isolation structures 110," consistent with Chang's gate structures. SAMSUNG-1009 (Chang), [0036]; *see* [0047], [0050], FIG. 11, FIGS. 18a-18d. These gates include a gate dielectric layer and a metal gate electrode, *e.g.*, as described by Chang. *Id.*, [0047]. I note that this gate structure—with a gate dielectric layer and a metal gate electrode—is also consistent with the structure of the gate stack described by Tseng. *See* SAMSUNG-1005 (Tseng), 3:4-12, 5:5-13, FIGS. 2 and 5A.

44. Spacers 108, highlighted in yellow, are disposed "on either side of the gates 106," and a "layer 1504 of interlayer dielectric," highlighted in orange, is disposed next to the spacers. SAMSUNG-1009 (Chang), [0037], [0051].

4. **Reasons to combine Chang and Tseng**

45. It is my opinion that a POSITA would have been motivated to incorporate shallow trench isolation (STI) around the base of the diffusions of the Chang-Tseng integrated circuit structure for at least the following reasons.

46. One reason why a POSITA would have been motivated to incorporate STI regions around the fins is to isolate the fins from one another, thereby improving the electrical performance of the device, *e.g.*, by reducing leakage current between neighboring fins. *See* SAMSUNG-1005 (Tseng), 4:25-27 ("the trenches 22 are filled with a dielectric material to form the isolation regions 204 to define and electrically isolate the various fins of the fin structure 202. In one example, the isolation regions 204 include shallow trench isolation (STI) regions"); SAMSUNG-1010 (Akarvardar), 1:43-45 ("In bulk FinFET technology, isolation regions may be used to electrically insulate adjacent devices or to electrically separate the fins of a given device from one another"); SAMSUNG-1031 (Yin), 5:16-18 ("The isolation regions 440 utilize isolation technology, such as STI, to define and electrically isolate various regions of the FinFET device 400.").

47. A second reason why a POSITA would have been motivated to integrate STI regions specifically over Chang's buried oxide layer is because STI used in conjunction with silicon-on-insulator (SOI) substrates was a conventional approach providing benefits of both SOI and STI. *See* SAMSUNG-1034 (Chen-745), 2:24-36 ("The SOI substrate may allow a transistor to operate at a higher switching speed or with a lower power consumption when compared to a bulk semiconductor substrate. … [S]hallow trench isolation (STI) that extends from a surface of the SOI substrate … may provide an electrical isolation around a periphery of the transistor primarily in a horizontal (or lateral) direction"); SAMSUNG-1035 (Cheng), 1:22-32 ("FinFET structures may be formed on a semiconductor-on-insulator (SOI) substrate, because of the low source/drain diffusion, low substrate capacitance, and ease of electrical isolation by shallow trench isolation structures"); SAMSUNG-1041 (Chen-619), 3:46-56 (describing a device having SOI and STI isolation that "maintains [] manufacturing simplicity, and benefits from FD-SOI's and FinFET's immunity to floating-body effects"), 6:6-46; SAMSUNG-1036 (Liaw), 3:55-59; SAMSUNG-1037 (Chang-529), 3:16-18; SAMSUNG-1038 (Iwamatsu), [0074].

48. Finally, it is my opinion that a POSITA would have been motivated to incorporate shallow trench isolation (STI) around the base of the diffusions in the Chang-Tseng combination simply because this implementation is just the

application of known techniques (*e.g.*, STI in an integrated circuit device) to a known structure (*e.g.*, a finFET integrated circuit structure) that results in a predictable outcome (*e.g.*, a finFET-based integrated circuit having STI around the fins).

49. It is my opinion that a POSITA would have expected success in incorporating STI regions around the fins because of Tseng's process for forming the STI regions is compatible with the initial steps of Chang's fabrication process. For instance, both Chang and Tseng describe initial steps of forming fins. *See* SAMSUNG-1009 (Chang), [0039], [0041], FIG. 4, FIG. 6; SAMSUNG-1005 (Tseng), 2:11-14, 3:44-4:5, FIG. 2, FIGS. 3A-3C. I believe that a POSITA would have expected success in integrating an STI step after these similar fin formation steps, and prior to other steps of Chang's process. I also believe that a POSITA also would have expected success given that the use of STI in integrated circuits, such as non-planar integrated circuits (*e.g.*, FinFET-based devices), was well-known as of the Critical Date. *See* SAMSUNG-1005 (Tseng), 4:25-27; SAMSUNG-1031 (Yin), 5:16-18; SAMSUNG-1032, 1:50-53.

5. Claim-by-Claim Analysis

(1) Claim 26

[26pre] An integrated circuit structure, comprising:

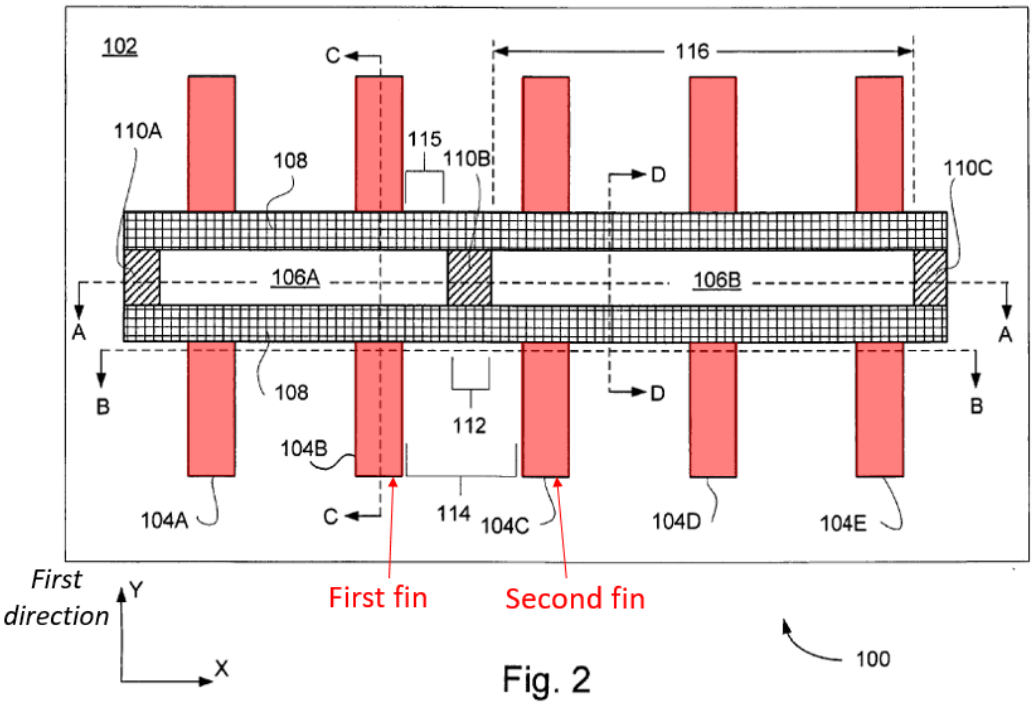
50. To the extent the preamble is deemed to be limiting, it is my opinion that the Chang-Tseng combination renders it obvious. *See* SAMSUNG-1009

(Chang), Abstract ("a circuit with a transistor having a self-aligned gate"), [0035] ("The exemplary embodiments of the present invention pertain to forming self-aligned gates on transistors"), [0036] ("FIG. 2 … illustrates a portion of a circuit 100 that includes transistors with end caps of gates 106 self-aligned to diffusions 104").

[26a] a first fin comprising silicon, the first fin having a longest dimension along a first direction;

[26b] a second fin comprising silicon, the second fin having a longest dimension along the first direction;

51. The Chang-Tseng combination renders obvious [26a] and [26b]. For instance, the Chang-Tseng combination structure includes **first and second fins**, *e.g.*, based on Chang's ***diffusions 104***. *See* SAMSUNG-1009 (Chang), [0036] ("a circuit 100 that includes transistors with end caps of gates 106 self-aligned to ***diffusions 104***"), [0039] ("Diffusions 104 may be formed on a substrate 102"), [0041] ("diffusions 104, each isolated from each other … where the substrate 102 is an SOI substrate"); claims 1 ("forming a first diffusion on a substrate; forming a second diffusion on the substrate a distance from the first diffusion"), 5 ("wherein the first transistor gate and the first diffusion are part of a tri-gate transistor"), 10, 14, 15, 18; FIGS. 2-18. I have highlighted these fins (*e.g.*, Chang's diffusions) in red in the composite figures below.



Chang-Tseng top-view composite figure

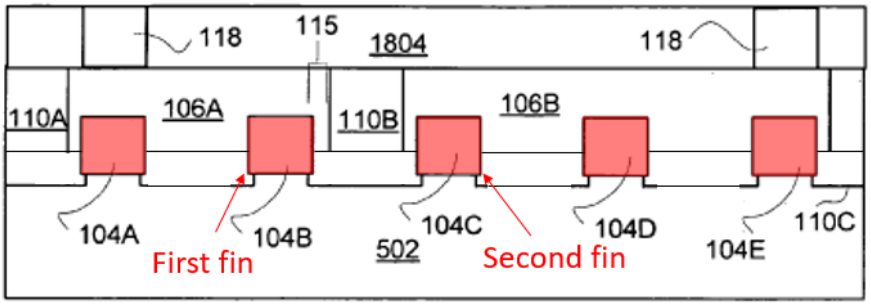


Fig. 18a

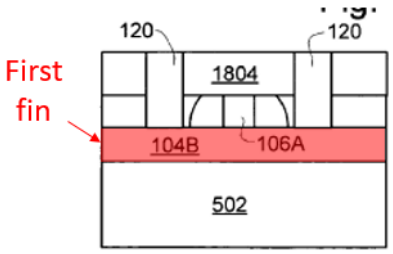


Fig. 18c

First direction

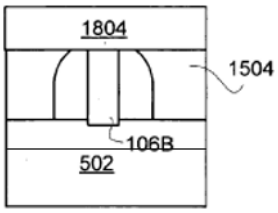


Fig. 18d

First direction

Chang-Tseng cross-sectional composite figures

52. It is my opinion that a POSITA would have understood that Chang's diffusions are **fins** at least in that they are elongated semiconductor structures disposed on the surface of a semiconductor substrate (*see* SAMSUNG-1009 (Chang), [0041], FIG. 2, FIG. 6) and arranged such that a gate can surround a

respective fin on three sides (*see id.* , FIGS. 18a-18d).[2] *See* SAMSUNG-1005 (Tseng), 1:17-24 ("A typical FinFET is fabricated with a thin vertical 'fin' (or fin structure) extending from a substrate formed by, for example, etching away a portion of a silicon layer of the substrate. … A gate is provided over three sides (e.g., wrapping) the fin."); SAMSUNG-1017 (Basker), 1:28-34 ("FinFETs may have a fin structure formed from a semiconductor substrate material. … A gate structure may be located over the fin enfolding the channel region"); SAMSUNG-1012 (Bohr), 1:24-27 (Non-planar transistors which utilize a fin of a semiconductor material protruding from a substrate surface employ a gate electrode that wraps around two, three, or even all sides of the fin (i.e., dual-gate, tri-gate, nanowire transistors"); SAMSUNG-1011 (Gan), 1:21-28 ("A typical FinFET is fabricated with a thin 'fin' extending from a substrate, for example, etched into a silicon layer of the substrate. … A gate is provided over (e.g., wrapping) the fin").

53. Furthermore, to the extent Patent Owner interprets fins as requiring the elongated semiconductor structure to have flat (*e.g.*, not undercut) sides, I note

[2] Indeed, I note that the '306 Patent uses "diffusion region" interchangeably with "fin": "Gate and TCN endcap regions refer to gate and TCN overlap of the ***diffusion region/fins*** of semiconductor devices." SAMSUNG-1001, 2:66-3:1.

that Chang discloses that its diffusions have such a geometry: the illustrated "the etching and/or cleaning process … removed a portion of the buried oxide layer 502 and … undercut the diffusions 104 to some extent, although in some other embodiments such undercutting may be absent." SAMSUNG-1009 (Chang), [0041].

54. In the Chang-Tseng combination structure, each fin has **a longest dimension along a first direction**, which I have marked in the figures. *See* SAMSUNG-1009 (Chang), [0036] ("***the diffusions 104 have a major axis in the Y direction*** and a minor axis in the X direction"). This longest dimension is **along the first direction** in that the longest dimension of the fins is traversed ***as one moves along the fins in the first direction***, *e.g.*, from top to bottom in the top-view composite figure, and into the page in the A-A cross-sectional composite figure.

55. Also in the Chang-Tseng combination structure, **the fins**, *e.g.*, Chang's diffusions 104, **comprise silicon**. This is made apparent by Chang's fabrication process. Chang's diffusions 104 are formed by using a patterned photoresist 510 to guide etching of a stack of materials including a "hardmask layer 508, [a] pad oxide layer 506, and ***[a] semiconductor layer 504***." SAMSUNG-1009 (Chang), [0041], FIG. 5, below (in which I have outlined the semiconductor layer in pink). The "semiconductor layer 504 … may comprise ***single crystal silicon***." *Id.*, [0041]. The portions of the semiconductor layer that

remain following the etch (and following subsequent processing steps to remove the hardmask layer 508 and pad oxide layer 506) constitute the diffusions 104. *Id.*, [0041], [0045]-[0046], FIGS. 6 (also below) and 9-10. That is, the fins (*e.g.*, Chang's diffusions) are formed of the remaining, unetched portions of the silicon semiconductor layer 504. Thus, the fins (*e.g.*, Chang's diffusions) **include silicon**.

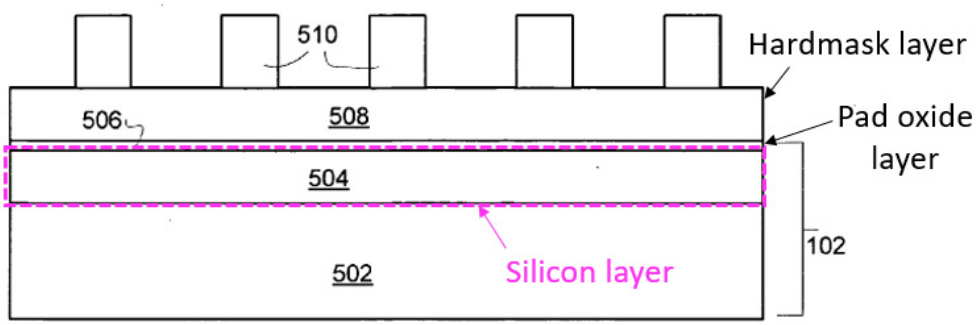


Fig. 5

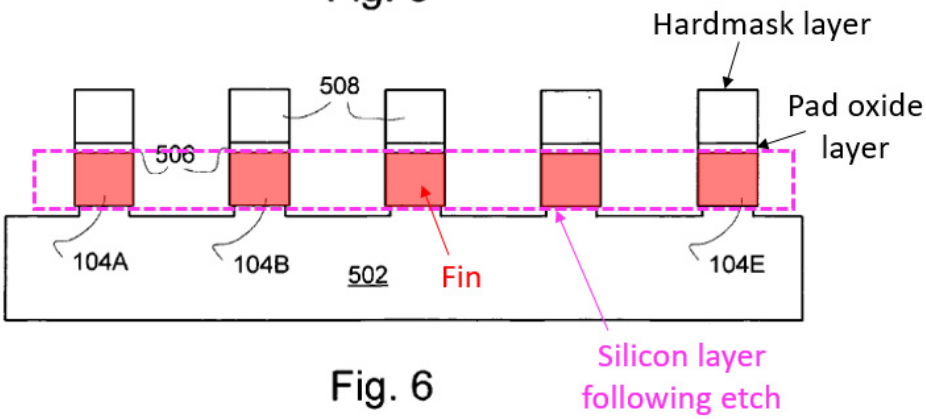


Fig. 6

Excerpts from Chang, FIGS. 5-6 (annotated)

[26c] an isolation material between the first fin and the second fin;

56. The Chang-Tseng combination renders obvious [26c] For instance, in the Chang-Tseng combination structure, based on the teachings of Tseng, a

"***dielectric material***" is disposed in the spaces between diffusions "to form isolation regions" such as "***shallow trench isolation (STI) regions***." SAMSUNG-1005 (Tseng), 4:25-32, FIG. 4A. The dielectric material of the STI regions, which I have highlighted in purple in the composite figure below, is **an isolation material**. *See also* SAMSUNG-1005 (Tseng), 4:33-57, 3:9-10 ("an insulation region 204 between the first fin 202a and second fin 202b"), 4:20-24 ("an insulation region 204 above the substrate major surface 20s between the first fin 202a and second fin 202b comprising an insulation top surface 204s lower than the fin top surfaces 202t"), claim 1 ("an insulation region over the substrate, wherein a first portion of the fin is embedded in the insulation region and a second portion of the fin extends above a top surface of the insulation region"), claim 10, claim 12, 2:15-19, FIGS. 1-2, 4-10.

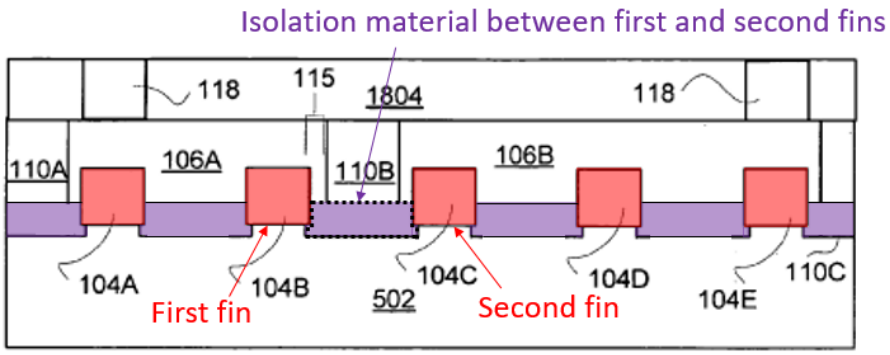


Fig. 18a

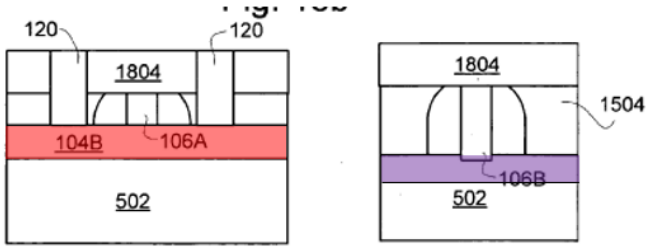


Fig. 18c

Fig. 18d

Chang-Tseng cross-sectional composite figures

57. In the Chang-Tseng combination structure, the dielectric material of the STI regions is **an isolation material** because it provides electrical isolation between fins. This is confirmed by Tseng: "the trenches 22 are filled with a dielectric material to form the isolation regions 204 to define and ***electrically isolate the various fins of the fin structure 202***. In one example, the isolation regions 204 include shallow trench isolation (STI) regions." SAMSUNG-1005 (Tseng), 4:25-29; *see* SAMSUNG-1010 (Akarvardar), 1:43-45 ("In bulk FinFET technology, isolation regions may be used to electrically insulate adjacent devices or to electrically separate the fins of a given device from one another");

SAMSUNG-1031 (Yin), 5:16-18 ("The isolation regions 440 utilize isolation technology, such as STI, to define and electrically isolate various regions of the FinFET device 400."); SAMSUNG-1034 (Chen), 2:24-36 ("[S]hallow trench isolation (STI) that extends from a surface of the SOI substrate … may provide an electrical isolation around a periphery of the transistor primarily in a horizontal (or lateral) direction")"); SAMSUNG-1035 (Cheng), 1:22-32 (("FinFET structures may be formed on a semiconductor-on-insulator (SOI) substrate, because of the … ease of electrical isolation by shallow trench isolation structures").

58. In the Chang-Tseng combination structure, the isolation material (*e.g.*, the dielectric material of Tseng's STI regions) is **between the first and second fins** at least in that it is in the space separating the first and second fins (*e.g.*, the space separating Chang's diffusions), as shown in the composite figures above. *See* SAMSUNG-1005 (Tseng), 3:9-10 ("an insulation region 204 ***between the first fin 202a and second fin 202b***"), 4:20-24 ("an insulation region 204 above the substrate major surface 20s between ***the first fin 202a and second fin 202b*** comprising an insulation top surface 204s lower than the fin top surfaces 202t"), claim 10 ("forming an insulation region above the major surface of the substrate ***between the first fin and the second fin***"), 2:15-19, claim 1, claim 12, FIGS. 2, 4-10.

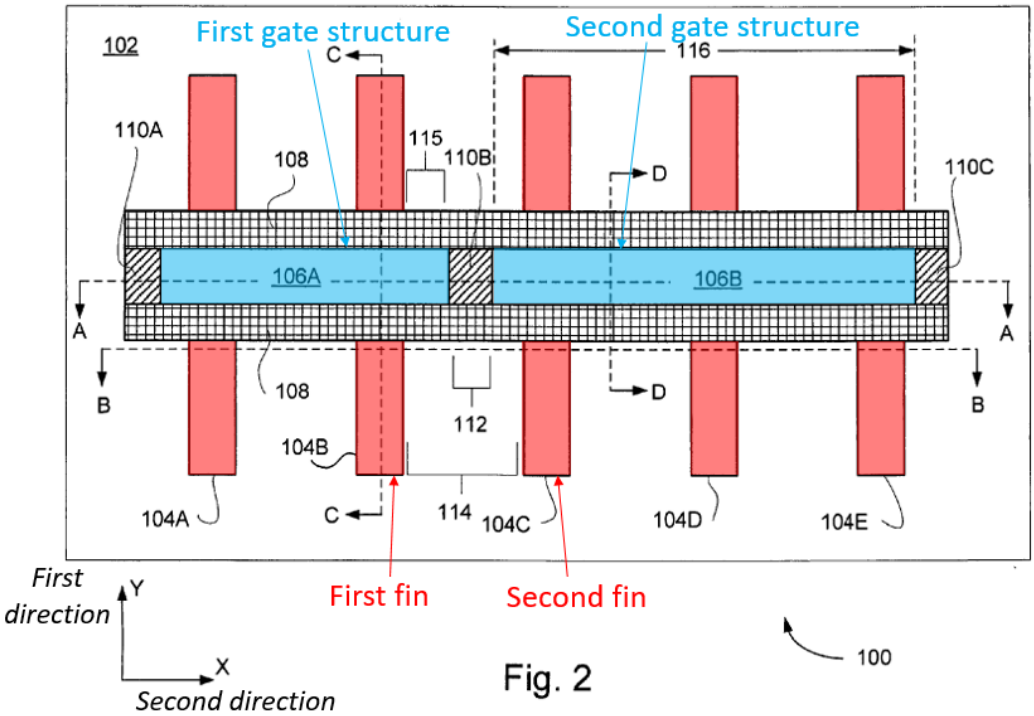
[26d] a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to

the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;

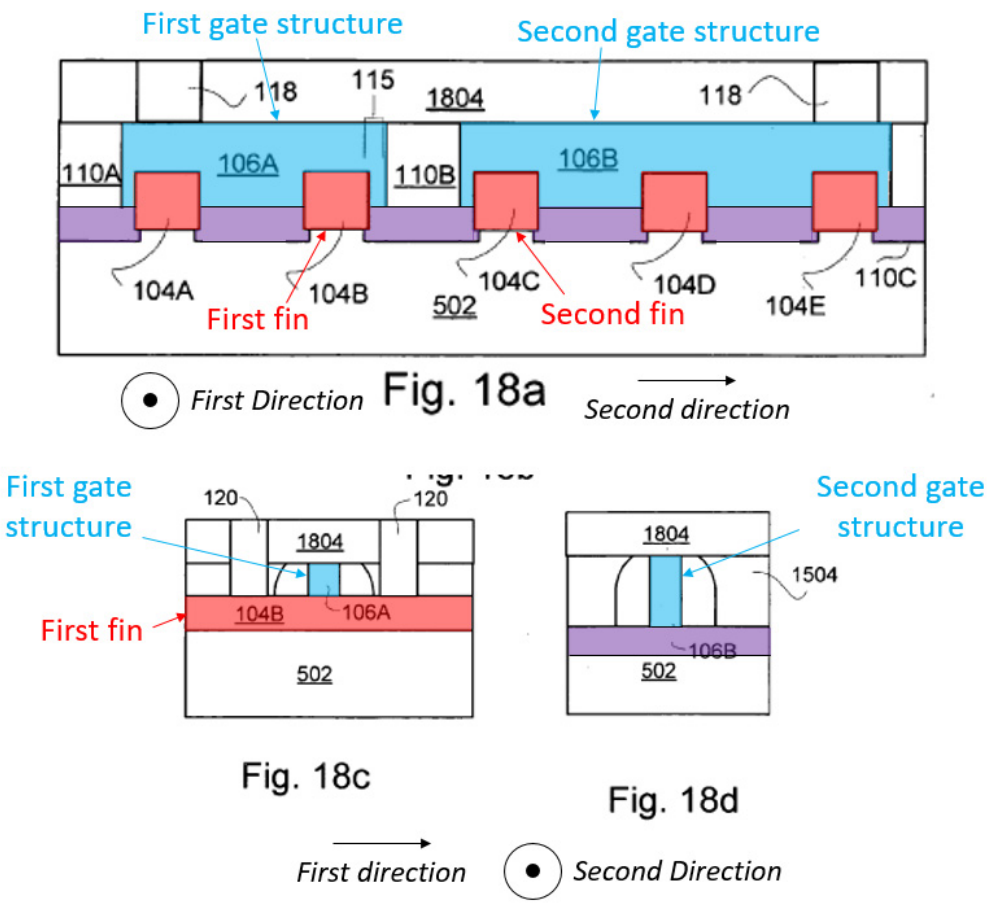
[26e] a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;

59. The Chang-Tseng combination renders obvious [26d] and [26e]. For instance, the combination structure includes **first and second gate structures**, *e.g.*, based on Chang's gates 106, which I have highlighted in blue in the composite figures below. *See* SAMSUNG-1009 (Chang), [0036] ("a circuit 100 that includes transistors with end caps of ***gates 106*** self-aligned to diffusions 100"), [0037] ("The embodiment of the circuit 100 shown in FIG. 2 includes ***two gates, 106A and 106B***"), [0039] ("FIG. 4 is a flow chart 400 that provides a general overview of how ***a gate 106*** that is self-aligned to diffusions 104, such as gate 106A self-aligned to diffusion structures 104 … may be fabricated"), [0047] ("In one embodiment, the first gate material 1102 may be a placement holder for replacement gate processes where the first gate material 1102 is removed and a final metal gate and gate dielectric replace the place-hold first gate material 1102."), [0050] ("In one embodiment the transistor is made by a replacement gate process"), [0056] ("FIG. 18a is a cross-sectional side view … that illustrates the circuit 100 after formation of the gates 106"), claim 1 ("forming … a first

transistor gate on the first diffusion and a second transistor gate on the second diffusion"), claim 10, claim 15, claim 18, FIGS. 2-4, FIGS. 18a-d.



Chang-Tseng top-view composite figure



Chang-Tseng cross-sectional composite figures

60. As illustrated in these composite figures, the first and second gate structures have **a longest dimension along a second direction**: the longest dimension of the gate structures is traversed ***as one moves along the gate structures in the second direction*** (from left to right in the top-view and Fig. 18a cross-sectional view composite figures, and into the page in the Figs. 18c and 18d cross-sectional views). *See* SAMSUNG-1009 (Chang), [0036] ("the gates 106 have a length in the Y direction and a width in the X direction"), FIGS. 2-3, FIGS. 18a-d.

61. The composite figures also illustrate that **the second direction is orthogonal to the first direction**, *e.g.*, the gates 106 extend in a direction orthogonal to the extension of the fins. *See* SAMSUNG-1009 (Chang), [0036] ("the diffusions 104" (*e.g.*, the fins in the combination) "have a major axis in the Y direction and a minor axis in the X direction; the gates 106 have a length in the Y direction and a width in the X direction"), FIGS. 2-3, FIGS. 18a-d. To the extent that Chang's disclosure of this orthogonality is not explicit, it is my opinion a POSITA nevertheless would have understood this to be the case, or otherwise found this to be obvious. This orthogonality is consistent with Chang's description and figures (*see* SAMSUNG-1009 (Chang), FIGS. 2-3, FIGS. 18a-d). Moreover, gate structures orthogonal to fins in finFET devices was well-known in the art as of the Critical Date. *See*, *e.g.*, SAMSUNG-1008 (Kawa), [0053] ("gate traces … which are elements of the patterned gate conductor layer, and are disposed over and orthogonal to the set of fins"); SAMSUNG-1029 (Zhu), [0042] ("The patterned second gate conductor 106 intersects the semiconductor fin and extends, e.g., along a direction perpendicular to a length direction of the semiconductor fin 102."); SAMSUNG-1030 (Basker), Abstract ("The fin structures each comprise a semiconductor layer and extend in a first direction, and the gate stack extends in a second direction that is perpendicular.").

62. In the Chang-Tseng combination structure, the **first gate structure is over the first fin** and **the second gate structure is over the second fin**, as shown in the composite figures above. *See* SAMSUNG-1009 (Chang), FIG. 2, FIGS. 18a-18d. This configuration is also made apparent by the description of Chang's fabrication process. For instance, Chang describes a "replacement gate process" in which a "first gate material 1102 around the diffusions" is removed, exposing the diffusions and defining "a volume within which the gates 106 may be formed." SAMSUNG-1009 (Chang), [0055], FIG. 17a. The gates 106 are then formed in that volume. *See id.*, [0056], FIG. 18a. When the gate material is deposited into that volume, it is deposited over the exposed diffusions (*e.g.*, **over the fins**).

63. Moreover, in the Chang-Tseng combination structure, **the second gate structure is discontinuous with the first gate structure**. This is illustrated in the Chang-Tseng composite figures, which I have reproduced again below. As illustrated, the first and second gate structures (*e.g.*, Chang's gates 106A, 106B, blue) are **discontinuous** at least because they are separated by the isolation structure 110b (which I have highlighted in green, and which I discuss in [26f], below). *See* SAMSUNG-1009 (Chang), [0036] ("The isolation structures 110 may have a width 112 that determines ***the distance between adjacent gates 106***"), [0044] ("the width 112 of the insulating isolation structure 110B … may define the distance between two adjacent gates 106, such as ***the distance 112 between***

adjacent gates 106A and 106B"), [0055] ("The distance between two adjacent gates 106 may be defined by the width 112 of the insulating isolation structures 110"), claim 1 ("forming … a first transistor gate on the first diffusion and a second transistor gate on the second diffusion, the insulating isolation structure defining a separation distance between the first and second transistor gates"), claim 15 ("an insulating isolation structure between the first and second gates that ***separates*** and insulates ***the first and second gates from each other***"), FIGS. 2-3, FIG. 4 ("Form Gates ***Separated By*** Insulating Isolation Structure"), FIGS. 18a-18d.

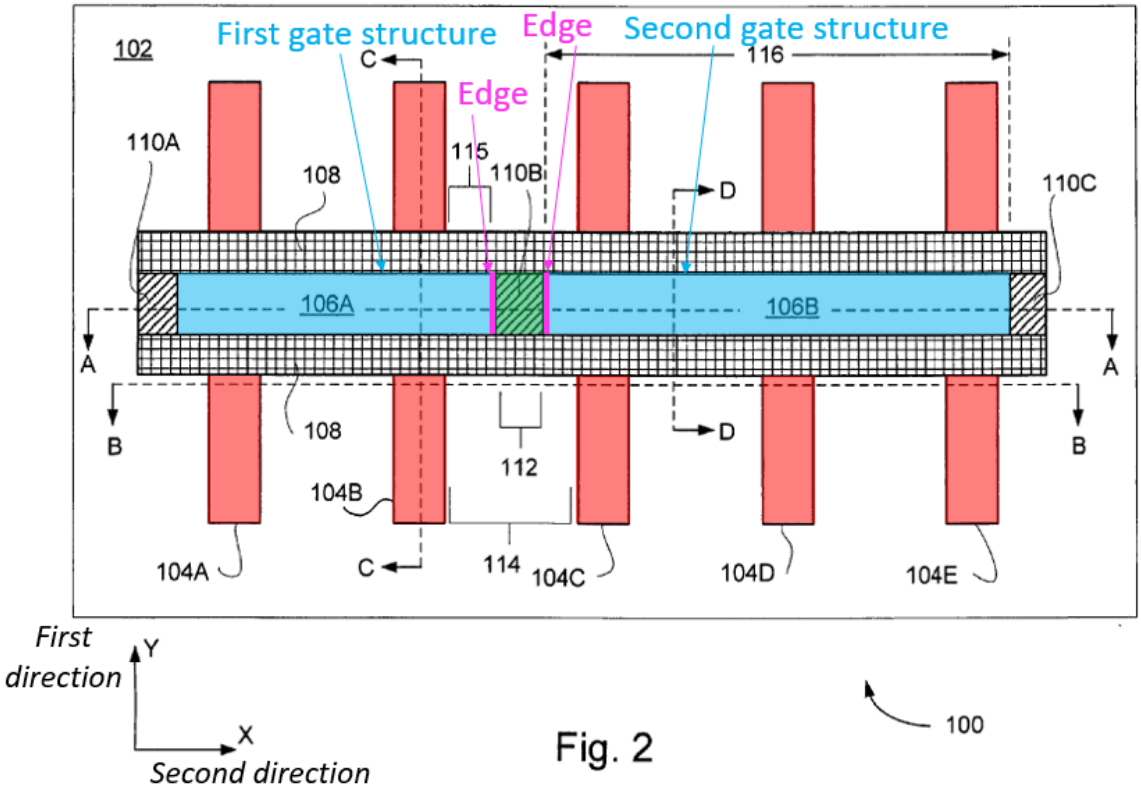
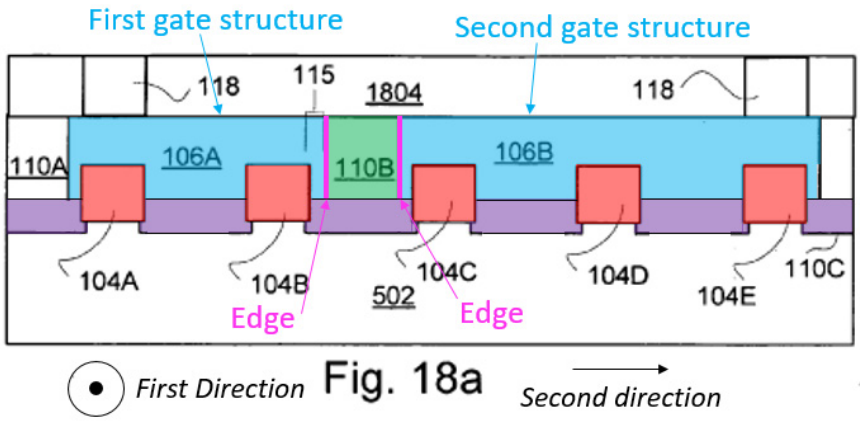


Fig. 2

Chang-Tseng top-view composite figure



Chang-Tseng cross-sectional composite figure

64. As shown in the composite figures above, the discontinuity between the first and second gate structures is **along the second direction**: the discontinuity is reached ***as one moves in the second direction*** from one gate structure to the other (*e.g.*, from left to right in the top-view and FIG. 18a cross-sectional view composite figures above). *See* SAMSUNG-1009 (Chang), FIGS. 2-3, FIGS. 18a-18d.

65. The composite figures also illustrate that **the second gate structure has an edge** (outlined in pink) **that faces an edge of the first gate structure** (also outlined in pink). For instance, the edge (pink) of the second gate structure (blue) that contacts the isolation structure 110B (green) faces the edge (pink) of the first gate structure (blue) that also contacts that isolation structure 110B (green). *See* SAMSUNG-1009 (Chang), [0037] ("the width 116 of gate 106B is defined by the placement of isolation structures 110B and 110C on either side of that gate 106B"), FIGS. 2-3, FIGS. 18a-18d. The edges face one another **along the second**

direction: from the edge of the second gate structure, the edge of the first gate structure is reached ***as one moves in the second direction*** (*e.g.*, from right to left in the top-view and FIG. 18a cross-sectional view composite figures above).

66. In the Chang-Tseng combination structure, the first and second gate structures each includes **a gate dielectric layer and a gate electrode**. For instance, Chang describes that when the gates are made by a replacement gate process, "***a final metal gate*** and ***gate dielectric*** replace the place-holder first gate material 1102." SAMSUNG-1009 (Chang), [0047]; *see* [0064], [0066]. Chang's final metal gate is a gate electrode, and Chang's gate dielectric is a gate dielectric layer.

[26f] a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and

67. The Chang-Tseng combination renders obvious [26f]. For instance, the combination structure includes **a gate edge isolation structure**, *e.g.*, based on Chang's isolation structure 110B, and which I have highlighted in green in the composite figures below. *See* SAMSUNG-1009 (Chang), [0037] ("the width 116 of gate 106B is defined by the placement of isolation structures 110B and 110C on either side of that gate 106B"), [0039] ("Insulating isolations structures 110 may be formed 406 between the diffusions), [0043]-[0044], , FIGS. 2-4, FIGS. 14a-18d; claim 15 ("an insulating isolation structure between the first and second gates that

separates and insulates the first and second gates from each other"), claims 1, 10-12, 18.

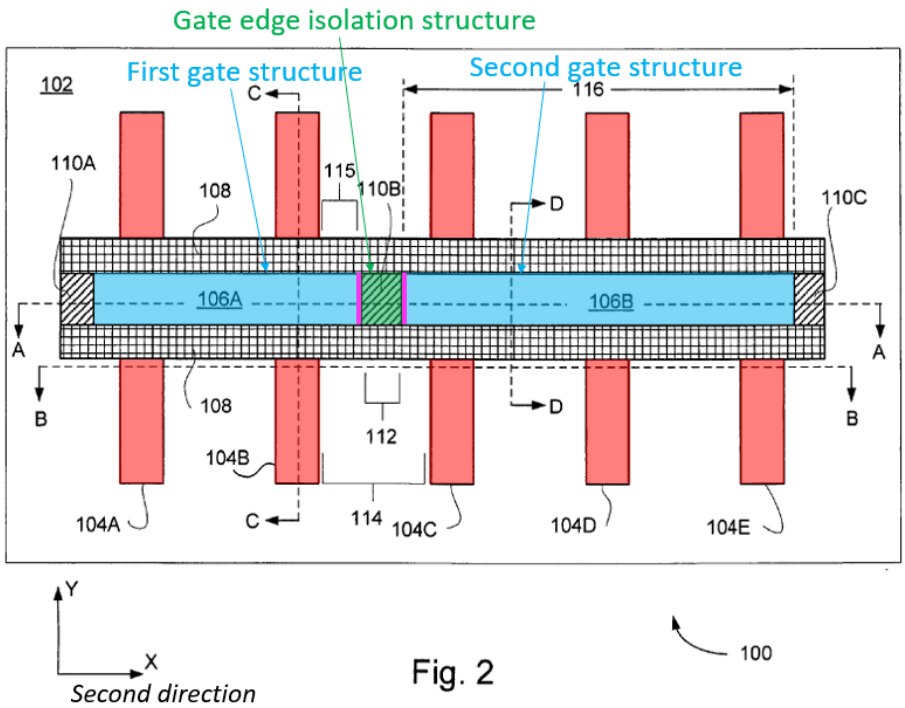


Fig. 2

Chang-Tseng top-view composite figure

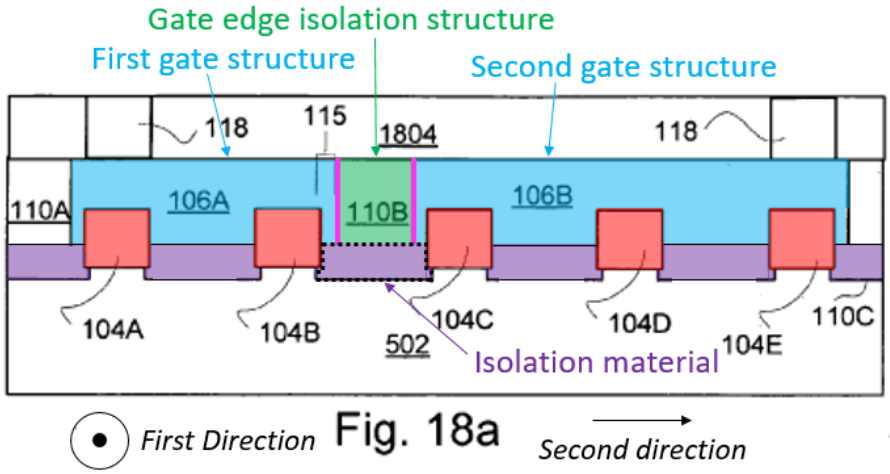


Fig. 18a

Chang-Tseng cross-sectional composite figure

68. Chang's isolation structure 110B, in the Chang-Tseng combination, is **a gate edge isolation structure**: it is a self-aligned structure that is disposed between the edges of the gate structures (discussed in [26d]-[26e] and discussed further below) and isolates those gate structures from one another (*e.g.*, physically and electrically).

69. Notably, Chang's isolation structure 110B is a ***self-aligned*** structure. *See* SAMSUNG-1009 (Chang), [0046] ("The self-alignment may be accomplished by forming gate isolation structures 110 ***self-aligned*** to the diffusion 104"), Abstract ("Insulating isolation structures may be formed, self-aligned to diffusions"), [0039] ("As the insulating isolation structures are self-aligned to the diffusions 104, the gates 106 are thus self-aligned to the diffusions 104, which may aid in keeping the size of the circuit small"), [0044] ("The insulating isolation structures 110 are thus self-aligned to the diffusions 104"), claim 1 ("forming an insulating isolation structure on the substrate between the first and second diffusions, the insulating isolation structure being self-aligned to the first and second diffusions"), claim 10, claim 18.

70. Moreover, Chang's isolation structure 110B ***physically isolates*** the first and second gate structures in that the isolation structure is "between the first and second gates" and "***separates … the first and second gates from each other***," thus preventing them from contacting one another. SAMSUNG-1009 (Chang),

claim 15; *see* FIG. 4 ("Gates Separated By Insulating Isolation Structure"), [0035], [0036] ("The isolation structures 110 may have a width 112 that determines the distance between adjacent gates 106"), [0044] ("This width 112 [of the insulating isolation structure 110B] may define the distance between two adjacent gates, such as the distance 112 between adjacent gates 106A and 106B"), [0055] ("The distance between two adjacent gates 106 may be defined by the width 112 of the insulating isolation structures 110"), claim 1 ("the insulating isolation structure defining a separation distance between the first and second transistor gates"), FIGS. 2-3, FIGS. 18a-18d.

71. Moreover, Chang's isolation structure also ***electrically isolates*** the first and second gate structures. *See* SAMSUNG-1009 (Chang), [0035] ("The gates may be self-aligned to ***isolation structures insulating gates from each other***"), claim 15 ("an insulating isolation structure between the first and second gates that … ***insulates the first and second gates from each other***"), [0039] ("***Insulating isolation structures 110***"), Abstract, [0007] ("a circuit that includes transistors with gates self-aligned to isolation structures that insulate the gates from each other"), FIG. 4.

72. In the Chang-Tseng combination, **the gate edge isolation structure** (*e.g.*, Chang's isolation structure 110b) **is between and in contact with the edge of the first gate structure and the edge of the second gate structure**. The

composite figures above illustrate this positioning. I have outlined the edges of the first and second gate structures in pink.

73. Specifically, in the Chang-Tseng combination, Chang describes that the gate edge isolation structure is **between** the first and second gate structures: "an insulating isolation structure ***between the first and second gates*** that separates … the first and second gates from each other." SAMSUNG-1009 (Chang), claim 15; *see* FIG. 4 ("Gates Separated By Insulating Isolation Structure"), [0035], [0036], [0044] ("This width 112 [of the insulating isolation structure 110B] may define the distance between two adjacent gates, such as the distance 112 between adjacent gates 106A and 106B"), [0055] ("The distance between two adjacent gates 106 may be defined by the width 112 of the insulating isolation structures 110"), claim 1, FIGS. 2-3, FIGS. 18a-18d.

74. Additionally, in the Chang-Tseng combination, the gate edge isolation structure is **in contact with** the edges of the gate structures, which is made apparent by Chang's description of the fabrication process. In Chang's replacement gate process, the "first gate material 1102" is removed, as shown in FIG. 17a, exposing the edges of the isolation structure 110B. SAMSUNG-1009 (Chang), [0055]. The gates are then formed in the space previously occupied by the first material 1102, thus contacting the exposed edges of the isolation structure 110b. *See* SAMSUNG-1009 (Chang), [0056], [0047] ("the first gate material 1102

is removed and a final metal gate and gate dielectric replace the place-holder first gate material 1102").

75. The gate edge isolation structure is between and in contact with the edges of the gate structures **along the second direction**: ***as one moves in the second direction*** (*e.g.*, from left to right in the top-view and FIG. 18a cross-sectional view composite figures above) starting from the edge of the first gate structure, one reaches first the gate edge isolation structure and then the edge of the second gate structure.

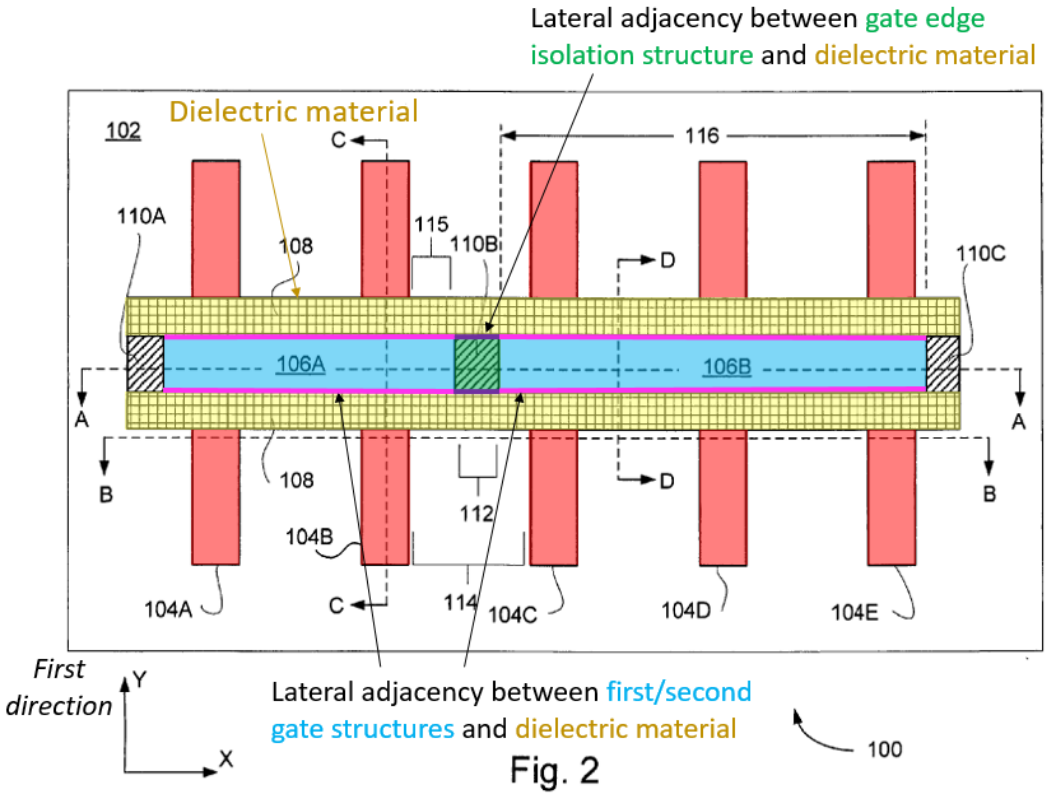
76. Furthermore, in the Chang-Tseng combination, the gate edge isolation structure is **over the isolation material**, as shown in the composite figures above. As I discussed in my overview of the Chang-Tseng combination, the isolation material (*e.g.*, the dielectric material of Tseng's STI regions) is deposited into the spaces between the fins (*e.g.*, between Chang's diffusions). *See* SAMSUNG-1005 (Tseng), 4:25-32, FIGS. 2 and 5A. A "layer of an insulating material 802," which will "be used as the insulating isolation structure[]" (*e.g.*, as the gate edge isolation structure), then is deposited into the spaces between fins, and thus is deposited onto (over) the previously-deposited isolation material. SAMSUNG-1009 (Chang), [0042]-[0044], FIGS. 7-8; *see* SAMSUNG-1005 (Tseng), 4:25-32. Thus, the gate edge isolation structure is over the isolation material.

[26g] a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to

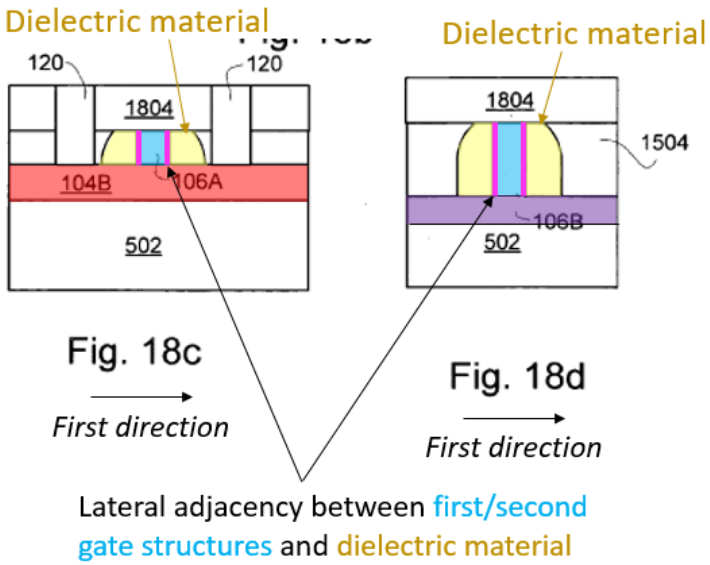
the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.

In the combination, Chang's spacers are a dielectric material

77. In a first alternative, which is applicable, *e.g.*, to the extent Patent Owner equates gate spacers to the claimed dielectric material, the Chang-Tseng combination structure includes **a dielectric material**, *e.g.*, based on Chang's "***spacers 108***," which I have highlighted in yellow in the composite figures below, disposed "on either side of the gates 106." SAMSUNG-1009 (Chang), [0037]; *see* [0049] ("The spacers 108 can be formed around the gates as shown in FIG. 14c" and "may be on either side of the first gate material 1102"), [0054] ("the spacers 108 may at least partially define a volume within which the gate interconnects may be formed"), [0055] ("The length of the gates 106 may be defined by the distance 1702 between the two spacers 108"), FIGS. 2-3, FIGS. 14a-18d. The spacers are **dielectric material** at least because they are formed of a dielectric (*e.g.*, insulating) material. *See* SAMSUNG-1009 (Chang), [0045] ("spacers 108 (which may comprise carbon-doped silicon nitride)").



Chang-Tseng top-view composite figure



Chang-Tseng cross-sectional composite figures

78. The sidewalls of the gate structures are outlined in pink in the composite figures above. These sidewalls extend into the page of the top-view figure. As can be seen from the cross-sectional composite figures, **the dielectric material** (highlighted in yellow) **is laterally adjacent to the gate structures** at least at these pink-outlined sidewalls. For instance, the dielectric material (*e.g.*, the spacers) is near (*e.g.*, next to) the sidewalls of the gate structures.

79. The dielectric material is laterally adjacent to the gate structures **along the first direction** at these pink-outlined sidewalls: viewing the structure starting from either of the gate structures and ***moving along the first direction*** (*e.g.*, from top to bottom in the top-view composite figure and from left to right in the cross-sectional composite figures above), one reaches the dielectric material (*e.g.*, the spacers).

80. The sidewalls of the gate edge isolation structure 110B are outlined in purple in the top-view composite figure above. These sidewalls extend into the page of the top-view figure, *e.g.*, substantially even with the sidewalls of the gate structures. The spacers 108 are disposed on either side of the gate edge isolation structure 110B at these purple-outlined sidewalls, *e.g.*, consistent with their positioning relative to the gate structures. *See* SAMSUNG-1009 (Chang), FIGS. 2-3. The spacers 108 are thus near (*e.g.*, next to) the sidewalls of the gate edge

isolation structure, *e.g.*, **the dielectric material** (yellow) **is laterally adjacent to the gate edge isolation structure** at least at these purple-outlined sidewalls.

81. The dielectric material is laterally adjacent to the gate edge isolation structure **along the first direction** at these purple-outlined sidewalls: viewing the structure starting from the gate edge isolation structure and ***moving along the first direction*** (*e.g.*, from top to bottom in the top-view composite figure above), one reaches the dielectric material.

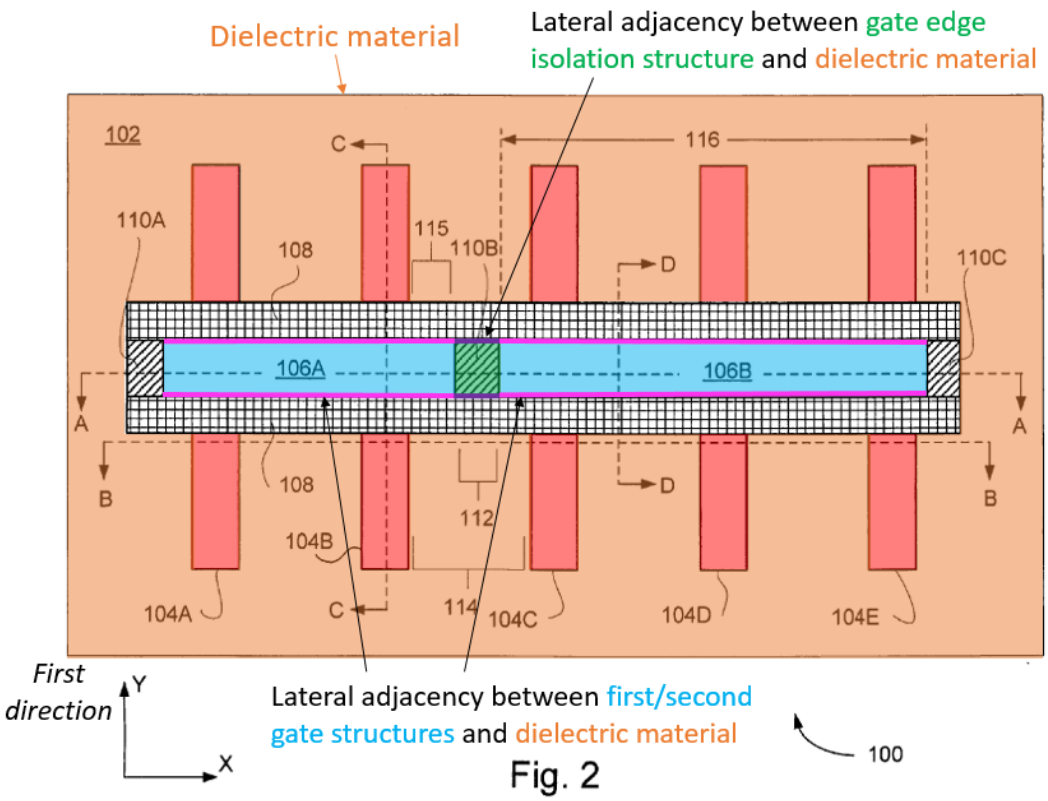
82. In the Chang-Tseng combination structure, **the dielectric material is discrete from the gate edge isolation structure**, *e.g.*, the spacers 108 are discrete from the isolation structure 110B. For instance, the dielectric material is discrete from the gate edge isolation structure at least in that ***they are formed in two distinct processing steps***. Specifically, the gate edge isolation structure is formed prior to deposition of the spacers, as made apparent by Chang's description and illustration of the fabrication process. *See* SAMSUNG-1009 (Chang), [0043] ("A layer of an insulating material 802 may then be deposited," where "[p]ortions of the insulating material 802 may be used as the insulating isolation structures"), [0049] ("As seen in FIG. 14b, the spacers 108 have been formed around the diffusions"), FIG. 8, FIGS. 14a-14c.

83. Alternatively or additionally, **the dielectric material is discrete from the gate edge isolation structure** at least in that ***they are composed of two***

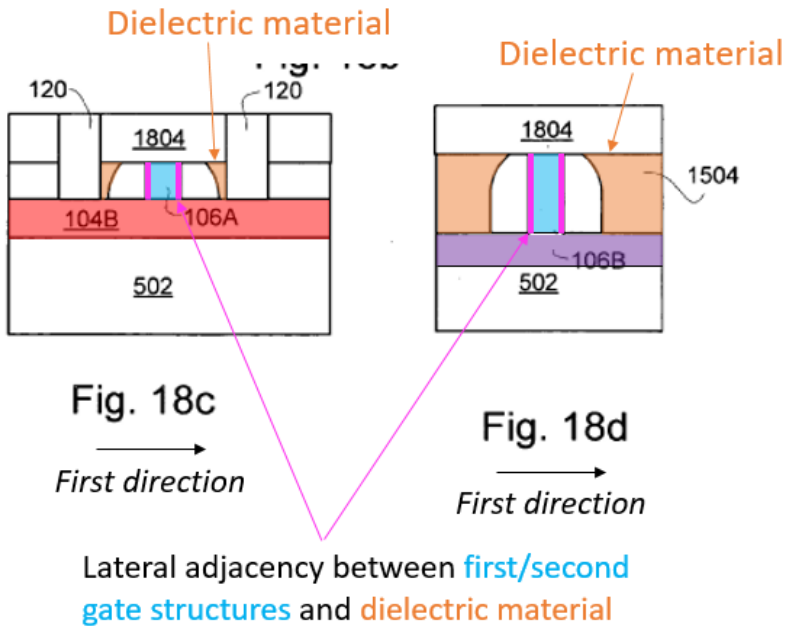
different materials. For instance, the dielectric material (*e.g.*, Chang's spacers) are carbon-doped silicon nitride while the gate edge isolation structure (*e.g.*, Chang's isolation structure 110B) is silicon nitride. *See* SAMSUNG-1009 (Chang), [0054], [0043]-[0044] ("the insulating material 802 may comprise silicon nitride," where "[p]ortions of the insulating material 802 may be used as the insulating isolation structures 110").

In the combination, Chang's interlayer dielectric is a dielectric material

84. In a second alternative, the Chang-Tseng combination structure includes **a dielectric material**, *e.g.*, based on Chang's "***layer 1504 of interlayer dielectric (ILD)***," highlighted in orange in the composite figures below. SAMSUNG-1009 (Chang), [0051]; *see* FIGS. 15a-18d. As shown in the top-view figure, the ILD is disposed around the structure that includes the gate structures, gate edge isolation structure, and spacers, and is "substantially planar with the top of the remaining insulating material 802" (*e.g.*, with the gate edge isolation structure; *see* SAMSUNG-1009 (Chang), [0044]) "and first gate material 1102." *Id.*, [0051]. That is, for instance, the ILD extends into the page of the top view figure around the structure that includes the gate structures, gate edge isolation structure, and spacers.



Chang-Tseng top-view composite figure



Chang-Tseng cross-sectional composite figures

85. I have outlined the sidewalls of the gate structures in pink in the composite figures above. These sidewalls extend into the page of the top-view figure. As can be seen from the cross-sectional composite figures, **the dielectric material** (orange) **is laterally adjacent to the gate structures** at least at these pink-outlined sidewalls. For instance, the dielectric material (*e.g.*, Chang's ILD) contacts the spacers 108 (*see* SAMSUNG-1009 (Chang), [0037]) that are disposed on those sidewalls. The dielectric material is thus **laterally adjacent** to the gate structures, *e.g.*, in that the dielectric material is near (*e.g.*, next to) the sidewalls of the gate structures (*e.g.*, separated only by the spacers).

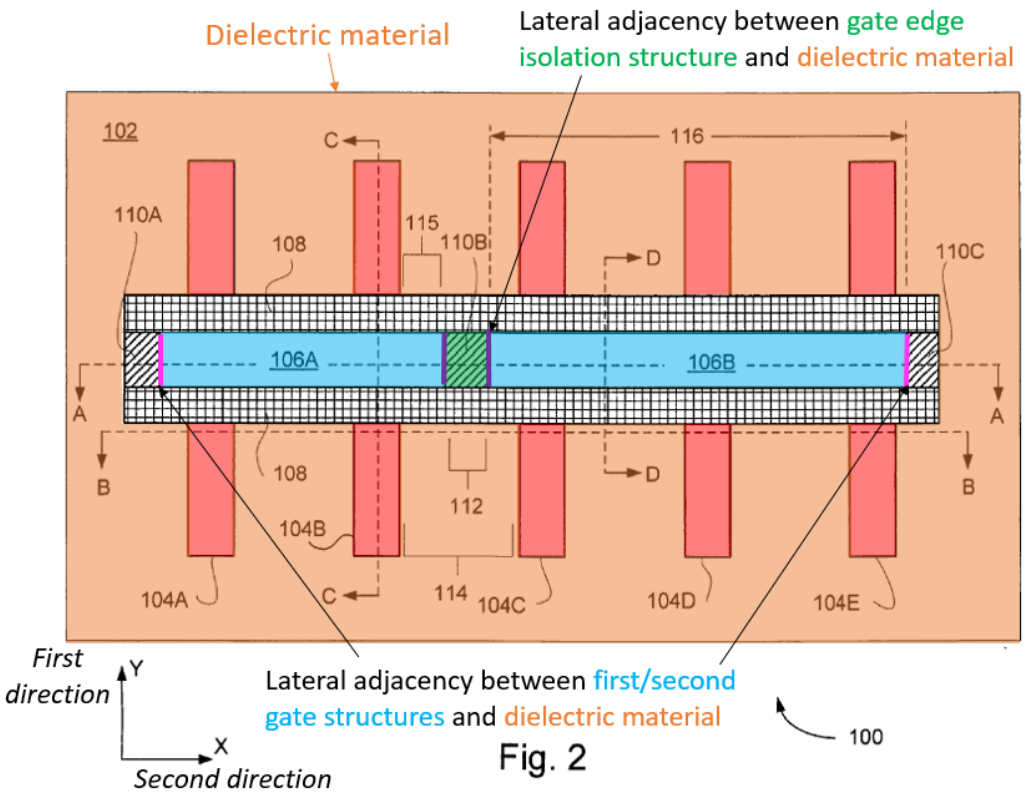
86. The dielectric material is laterally adjacent to the gate structures **along the first direction** at these pink-outlined sidewalls: viewing the structure starting from either of the gate structures and ***moving along the first direction*** (*e.g.*, from left to right in the cross-sectional composite figures and from top to bottom in the top-view composite figure), one reaches the dielectric material, passing through the spacers.

87. I have outlined the sidewalls of the gate edge isolation structure in purple in the top-view composite figure above. These sidewalls extend into the page of the top-view figure, *e.g.*, substantially even with the sidewalls of the gate structures. As with the sidewalls of the gate structures, **the dielectric material** (orange) **is laterally adjacent to the gate edge isolation structure** at least at these

purple-outlined sidewalls. For instance, the dielectric material (*e.g.*, Chang's ILD) contacts the spacers 108 (*see* SAMSUNG-1009 (Chang), [0037]) that are disposed on those sidewalls. The dielectric material is thus **laterally adjacent** to the gate edge isolation structure, *e.g.*, in that the dielectric material is near (*e.g.*, next to) the sidewalls of the gate edge isolation structure (*e.g.*, separated only by the spacers).

88. The dielectric material is laterally adjacent to the gate edge isolation structure **along the first direction**: viewing the structure starting from the gate edge isolation structure and ***moving along the first direction*** (*e.g.*, from top to bottom in the top-view composite figure above), one reaches the dielectric material, passing through the spacer.

89. Moreover, alternatively or additionally, the dielectric material of the combination (*e.g.*, Chang's ILD) also is laterally adjacent to the gate structures at the pink-outlined edges of the gate structures in the alternative top-view composite figure that I have reproduced below. For instance, viewing the structure starting from, *e.g.*, the second gate structure and moving along the second direction (left to right in the top-view composite figure), one reaches the dielectric material, passing through the end-most isolation structure 110C. To the extent this spatial relationship is considered to be laterally adjacent **along the first direction**, the dielectric material of the combination is laterally adjacent to the first and second gate structures along the first direction.



Chang-Tseng top-view composite figure (alternative)

90. Similarly, the dielectric material of the combination also is laterally adjacent to the gate edge isolation structure at the purple-outlined edges of the gate edge isolation structure. For instance, as illustrated above, viewing the structure starting from the gate edge isolation structure and moving along the second direction, one reaches the dielectric material, *e.g.*, passing through the second gate structure and the end-most isolation structure 110C. To the extent this spatial relationship is considered to be laterally adjacent along **the first direction**, the dielectric material of the combination is laterally adjacent to the gate edge isolation structure along the first direction.

91. In the Chang-Tseng combination, **the dielectric material is discrete from the gate edge isolation structure**, *e.g.*, Chang's ILD is discrete from the isolation structure 110B. For instance, the two structures are discrete at least in that ***they are formed in two distinct processing steps***: the gate edge isolation structure is formed prior to deposition of the ILD. *See* SAMSUNG-1009 (Chang), [0043]-[0044] (referring to FIG. 8 and describing deposition of an insulating material 802 that is "used as the insulating isolation structures"), [0051] (referring to FIGS. 15a-15d and describing subsequent deposition of the ILD layer).

(2) Claim 27

[27] The integrated circuit structure of claim 26, wherein the gate edge isolation structure comprises silicon and nitrogen.

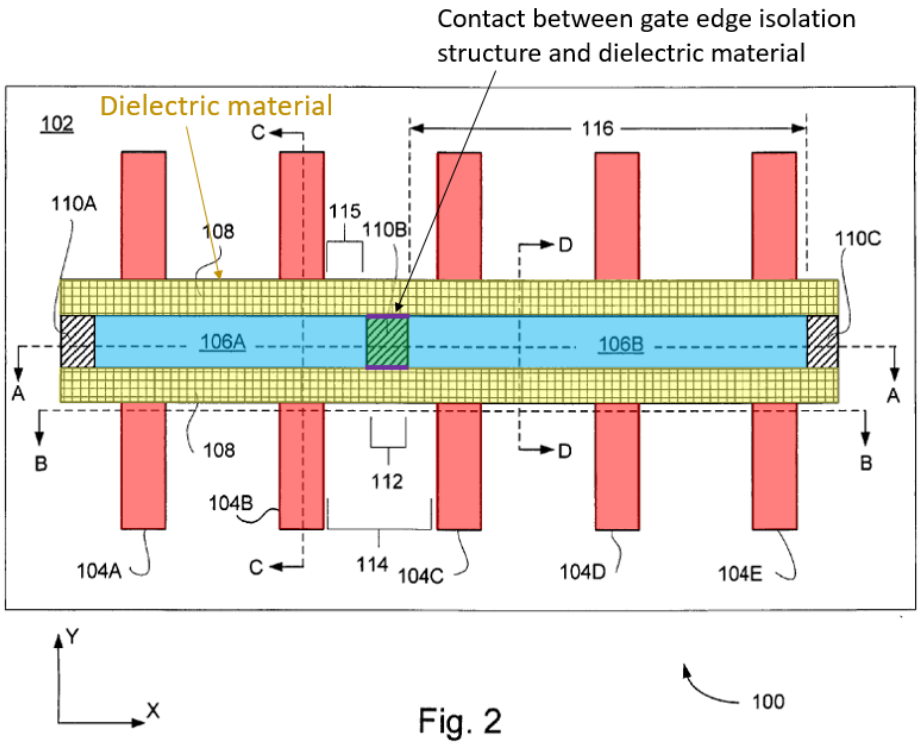
92. The Chang-Tseng combination renders obvious [27]. For instance, in the combination, Chang describes that the gate edge isolation structure (*e.g.*, Chang's isolation structure 110B) **comprises silicon and nitrogen**. Chang describes deposition of an "insulating material 802" that "may comprise silicon nitride," where "[p]ortions of the insulating material 802 may be used as the insulating isolation structures 110." SAMSUNG-1009 (Chang), [0043]-[0044].

(3) Claim 28

[28] The integrated circuit structure of claim 26, wherein the dielectric material is in contact with the gate edge isolation structure.

93. The Chang-Tseng combination renders obvious [28]. For instance, in the Chang-Tseng combination, Chang's spacers 108 (the dielectric material; *see*

[26g]) are **in contact with the gate edge isolation structure** (*e.g.*, Chang's isolation structure 110B) at least on the purple-highlighted sidewalls of the gate edge isolation structure, as shown in the composite figure below.



Chang-Tseng top-view composite figure

94. The description of Chang's fabrication process demonstrates that there is contact between the gate edge isolation structure and the dielectric material (*e.g.*, Chang's spacers). Chang describes that "[a] layer of an insulating material 802 may then be deposited to substantially fill the volume between spacers 806," *i.e.*, the spacers contact the insulating material. SAMSUNG-1009 (Chang), [0043]; *see* FIG. 8. This insulating material is "used as the insulating isolation structures," *e.g.*, as the gate edge isolation structure of the combination. *Id.*, [0044]. Thus, in

the combination, the dielectric material (*e.g.*, Chang's spacers) are in contact with the gate edge isolation structure (*e.g.*, Chang's isolation structure, which is made of the insulating material 802.

95. Alternatively or additionally, I note that a portion of the spacer 806 is aligned with the gate edge isolation structure. I have outlined this portion in dashed lines in the composite figure below. To the extent that this portion of the spacer can be considered as part of the gate edge isolation structure, the dielectric material (*e.g.*, Chang's ILD, orange) is in contact with the gate edge isolation structure at least at the outer edges of these portions of the spacers, which I have outlined in pink.

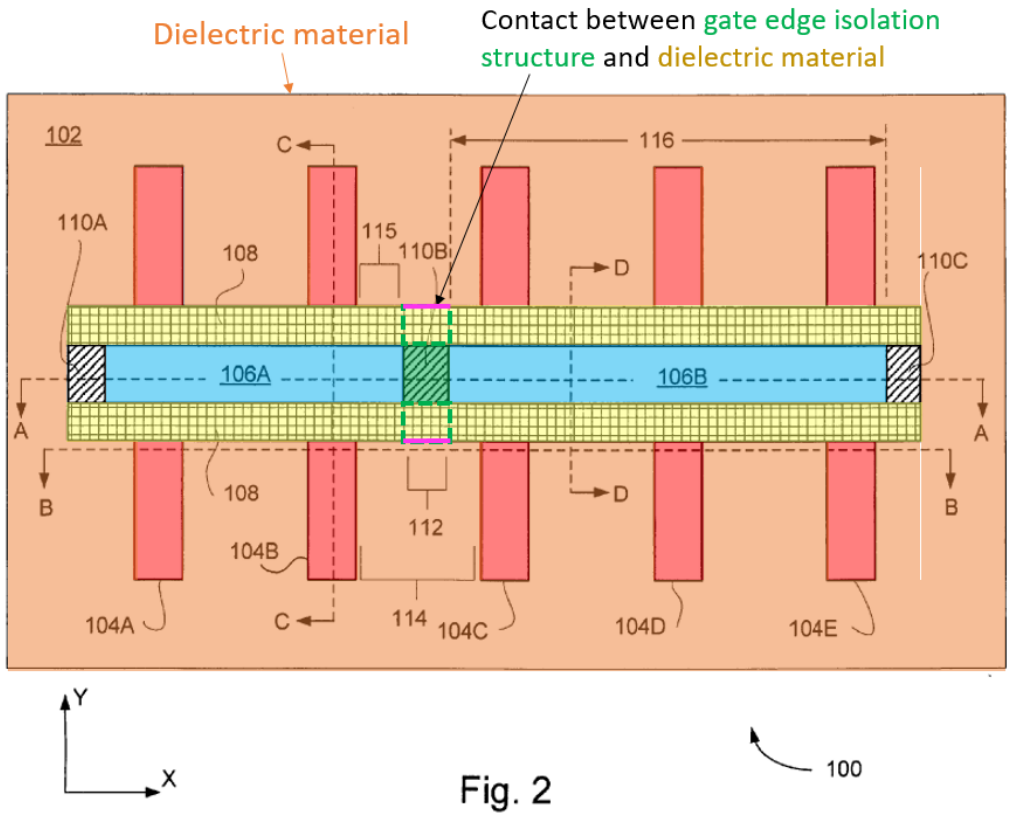


Fig. 2

Chang-Tseng composite figure

(4) Claim 29

[29] The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

96. The Chang-Tseng combination renders obvious [29]. For instance, in the Chang-Tseng combination, at least when the gate structures are fabricated by a replacement gate process (*see* SAMSUNG-1009 (Chang), [0047], [0050], [0055]-[0056], FIGS. 17-18), **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures**. In a replacement gate process, the sacrificial "first gate material 1102" is removed, as shown in FIG. 17a, defining a

"volume within which the gates 106 may be formed" and exposing the edges of the isolation structure 110B. SAMSUNG-1009 (Chang), [0055]. The gates are then formed in that defined volume—*i.e.*, the space previously occupied by the first material 1102—and thus the gates contact the exposed edges of the isolation structure 110B. *See* SAMSUNG-1009 (Chang), [0055]-[0056], [0047] ("the first gate material 1102 is removed and a final metal gate and gate dielectric replace the place-holder first gate material 1102").

97. I note that the general process flow for forming a replacement gate structure was well-known in the art as of the Critical Date. For instance, a POSITA would have understood that formation of a replacement gate can involve first depositing the gate dielectric layer into the space left by removal of the sacrificial gate material, followed by deposition of the gate electrode onto the gate dielectric layer. *See* SAMSUNG-1025 (Ching), 4:39-5:56 ("First, gate dielectric layer 50 is formed in recess 44 … and on the top surfaces and sidewalls of semiconductor fins 48. … Next, conductive material 52 is formed over gate dielectric layer 50, and fills the remaining recess 44."), FIG. 8A; SAMSUNG-1005 (Tseng), 8:62-9:4 ("the gate-last process comprises … fill[ing] the trench with a gate dielectric layer and a conductive gate electrode layer"); SAMSUNG-1015 (Shieh), [0045]-[0047] ("The gate dielectric 9 may be formed on the fins" and "[t]he gate electrode layer 8 may be formed over the gate dielectric 9");

SAMSUNG-1012 (Bohr), 11:1-14 ("the gate dielectric 545 and gate electrodes 520A and 520B … may be deposited into the openings 560A and 560C" which "expos[e] second semiconductor fin regions 585A and 585B"); SAMSUNG-1014 (Kuo), 7:8-42 ("a gate dielectric 230 and a gate structure 232 are formed over the second insulation layer 228").

98. As illustrated in the composite figure below, when the gate dielectric layer (dark blue) is deposited into the space left by removal of the sacrificial gate material, the gate dielectric layer is coated onto exposed surfaces, which include the exposed edges of the isolation structure 110B (highlighted in green). *See* SAMSUNG-1025 (Ching), 4:39-5:56; SAMSUNG-1040 (Kelly), 6:33-38, FIGS. 7A-7B (showing the gate dielectric layer 704 coating onto exposed sidewalls of an opening formed by removing a dummy gate structure); SAMSUNG-1036 (Liaw), [0023] ("a high-k dielectric layer 118 is formed over the upper portions 106 of the fin structures 104 as well as the rest of the opening 116 left by removal of the dummy gates 110, 111"), FIG. 1F. Thus, **the gate edge isolation structure** (*e.g.*, Chang's isolation structure 110B) **is in contact with the gate dielectric layer** of each gate structure, *e.g.*, at least because the gate dielectric layer of each of the first and second gate structures coats the respective edges of the gate separation structure.

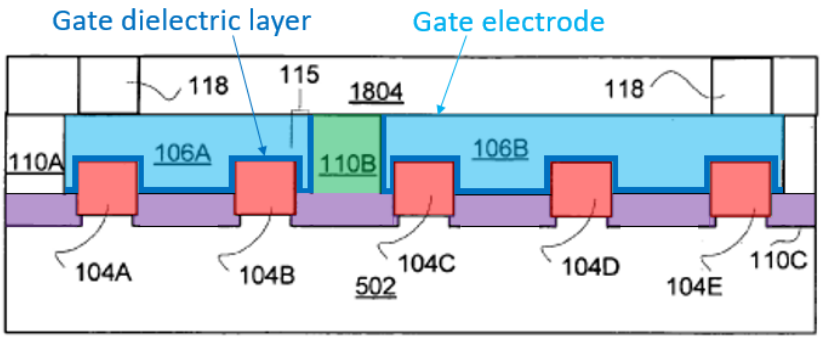


Fig. 18a

Chang-Tseng cross-sectional composite figure

(5) Claim 31

[31] The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

99. The Chang-Tseng combination renders obvious [30]. For instance, in the Chang-Tseng combination structure, the gate dielectric layers of the first and second gate structures **include a high-k dielectric material** based on the teachings of Tseng.

100. Tseng's FinFET includes "a gate stack 210" including a "gate electrode layer 214 and [a] gate dielectric layer 212." SAMSUNG-1005 (Tseng), 5:5-10; *see* FIG. 9A. The gate dielectric layer can be a "high dielectric constant (high-k) dielectric," and the gate electrode can include a "N-work function metal" or a "P-work function metal." SAMSUNG-1005 (Tseng), 5:12-46. Tseng's gate stack can be "fabricated using a gate-first process" or "using a gate-last process performed by first forming a dummy gate stack." *Id.*, 8:59-62.

101. In the Chang-Tseng combination, the gate dielectric layer of the gate structures (*see* SAMSUNG-1009 (Chang), [0047]) is implemented as a "***high dielectric constant (high-k) dielectric***" and the gate electrode is implemented as a metal gate electrode, such as an N- or P-work function metal, as taught by Tseng. SAMSUNG-1005 (Tseng), 5:12-46, 8:67-9:4, FIG. 5A.

102. It is my opinion that a POSITA would have been motivated to implement the gate dielectric layer of the combination's gate structures as a high-k gate dielectric layer for at least the following reasons.

103. A first reason why POSITA would have been motivated to use a high-k gate dielectric layer (*e.g.*, along with a metal gate electrode) is to obtain the performance advantages afforded by use of these materials. For instance, high-k gate dielectrics decrease threshold voltage, reduce fringe capacitance, and suppress leakage current. *See* SAMSUNG-1011 (Gan), 1:32-35 ("There has been a desire to replace the gate oxide and polysilicon gate electrode with a high-k gate dielectric and metal gate electrode t***o improve device performance as feature sizes continue to decrease***."); SAMSUNG-1026 (Guo), Abstract ("A high-k dielectric is used for the gate dielectric, providing increased inversion carrier density without having to resort to aggressive scaling of the thickness of the gate dielectric while at the same time preventing excessive gate leakage current from occurring.."); SAMSUNG-1027 (Lee), 1:38-46 ("methods have been sought to reduce leakage current while

achieving a high gate capacitance. One method investigated by the industry is the use of materials having a high dielectric constant (high-k or high-∈) for the gate dielectric layer."); SAMSUNG-1028 (Metz), Abstract ("The high-k gate dielectric layer has off-state leakage characteristics that are superior to those of a silicon dioxide based gate dielectric, and on-state mobility characteristics that are superior to those of a high-k gate dielectric that comprises an isotropic material.). Moreover, the use of a high-k gate dielectric layer provides the gate with finer control over the channel potential, enabling more effective on/off control to be achieved, thus facilitating higher speed performance. *See* SAMSUNG-1028 (Metz), Abstract.

104. A second reason why a POSITA would have been motivated to use a high-k gate dielectric layer is because gate structures having high-k gate dielectric layers and metal gate electrodes were standard elements of FinFET transistors, such as the FinFET structure of the Chang-Tseng combination. The implementation of the gate dielectric layer and gate electrode layer as a high-k gate dielectric layer and a metal gate electrode, respectively, is thus merely a comprehensive implementation of a structure already described by the Chang-Tseng combination.

105. Additionally, it is my opinion that a POSITA would have been motivated to use a high-k dielectric layer in the combination because this is just the

application of known techniques (*e.g.*, high-k gate dielectric layers and metal gate electrodes) to a known structure (*e.g.*, the gate insulation layer and bulk conductive metal layer of the gate structure of the Chang-Tseng FinFET device), which results in a predictable outcome (*e.g.*, a gate structure having a high-k gate dielectric layer and a metal gate electrode).

106. Moreover, it is my opinion that a POSITA would have expected success in implementing a high-k gate dielectric layer in the combination given that high-k gate dielectric layers and metal gate electrodes are well-known elements of both replacement gate structures and gate-first gate structures for FinFET devices. *See* SAMSUNG-1005 (Tseng), 5:5-46 (describing that the gate dielectric layer is a "high dielectric constant (high-k) dielectric" and the gate electrode includes an "N-work function metal" or a "P-work function metal"), 8:67-9:4, FIG. 5A; SAMSUNG-1025 (Ching), 4:39-5:3 ("[t]he resulting remaining portions of the conductive material and gate dielectric layer 50 thus form the replacement gate, which includes gate electrode 52 and gate dielectric 50," where "gate dielectric layer 50 comprises a high-k dielectric material" and "[c]onductive material 52 may comprise a metal-containing material such as TiN, TaN, TaC, Co, Ru, Al, combinations thereof"), FIG. 9A; SAMSUNG-1006 (Anderson), [0029] ("The gate stack 20 can be, for example, a gate dielectric and a gate electrode material," where "the gate dielectric can be, for example, a high-k dielectric

material" and "the gate electrode material being either a metal or a metal and polysilicon stack"); SAMSUNG-1011 (Gan), 3:59-4:10 ("The gate structure 110 includes a gate dielectric layer and a gate electrode. … The gate dielectric layer may further include … dielectric with a high dielectric constant (high-k) … The gate electrode may include … a metal including metal compounds such as, TiN, TaN, NiSi, CoSi, Mo, Cu, W, Al, Co"); SAMSUNG-1012 (Bohr), 4:46-54 ("The gate electrode … is a portion of a gate electrode stack which further includes a gate dielectric layer … Generally, the gate electrode 120 and gate dielectric layer 165 may be of any material compositions known in the art to be applicable to non-planar transistors with many known ultra high-k materials (e.g., having a dielectric constant above that of Si_3N_4) … being viable options"); SAMSUNG-1014 (Kuo), 7:8-22 ("a gate dielectric 230 and a gate structure 232 are formed over the second insulation layer 228. The gate dielectric 230 includes a dielectric material, such as … high-k dielectric material"); SAMSUNG-1015 (Shieh), [0046] ("The gate dielectric 9 may alternatively be formed from a high permittivity (high-k) material")-[0047].

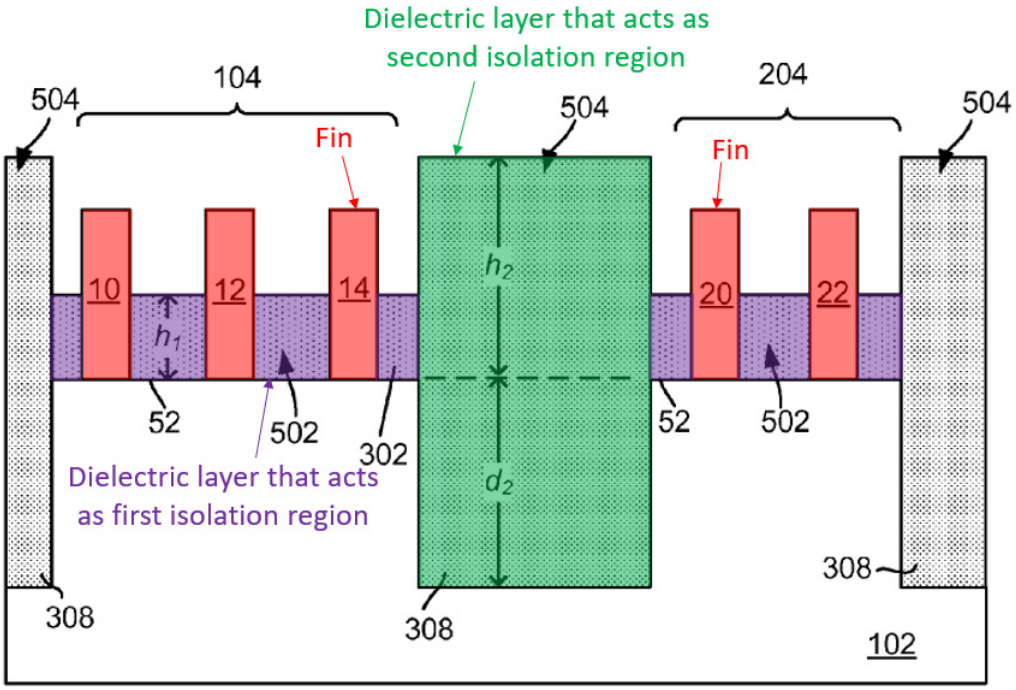
107. It is also my opinion that a POSITA also would have expected success because high-k gate dielectric layers and metal gate electrodes are consistent with Chang's description of the composition of its gate structures when fabricated using a subtractive process. *See* SAMSUNG-1009 (Chang), [0064] ("The gate dielectric

may comprise … a layer of high-k dielectric material … The first gate material 2202 may comprise Au, TiN, or another suitable material").

B. [GROUND 2] – CLAIMS 26-29 AND 31 ARE OBVIOUS OVER AKARVARDAR AND XIE

1. Akarvardar describes self-aligned isolation regions in FinFET devices

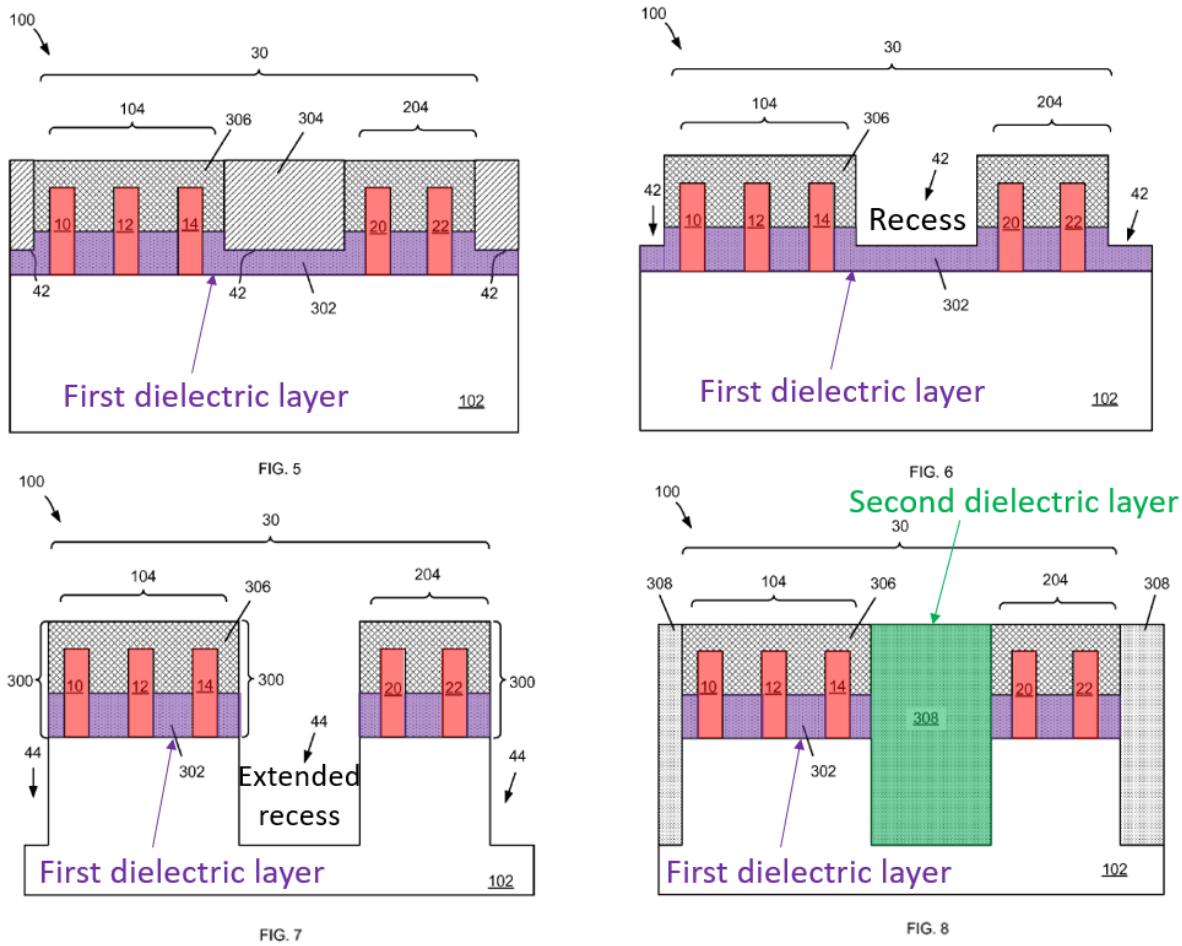
108. Akarvardar describes "bulk FinFET devices" including "multiple self-aligned isolation regions." SAMSUNG-1010 (Akarvardar), 3:46-58; *see* 1:6-9. Akarvardar's device includes a "first group of fins 104 [that] may include fins 10, 12, and 14" and a "second group of fins 204 [that] may include fins 20 and 22" (which I have highlighted in red in FIG. 9, below). *Id.*, 4:28-30, FIGS. 1-9. A "first dielectric layer 302" is disposed in the spaces between fins and acts as "first isolation region[s] 502," highlighted in purple, that "electrically separate[s] each individual fin of the first and second group of fins." *Id.*, 5:65-6:3, 7:36-38, 7:63-65, FIGS. 2-9. A "second dielectric layer 308" acts as a "second isolation region 504," highlighted in green, that extends into the bulk semiconductor substrate and "electrically separate[s] the first group of fins 104 from the second group of fins 204." *Id.*, 7:8-38, 7:64-65, FIGS. 8-9; *see* 6:47-66. As shown in FIG. 9, "[a] height and a depth of the second isolation region may be greater than a height and a depth of the first isolation region." *Id.*, 8:16-19.



Excerpt from Akarvardar, FIG. 9 (annotated)

109. Akarvardar's fabrication process involves multiple etch steps to form the second isolation region 504. For instance, as shown in FIGS. 5-6, reproduced below, in a first etch step, a "dummy material 304" is "removed from the recess 42" that is "between [the] two groups of fins and above the first dielectric layer 302," thus exposing "a portion of the first dielectric layer 302 positioned between … the first group of fins 104 and the second group of fins 204." SAMSUNG-1010 (Akarvardar), 5:23-24, 6:33-41. This portion of the first dielectric layer 302 then is removed in a second etch step, "expos[ing] the bulk semiconductor substrate." *Id.*, 6:39-46. In a third etch step, "[t]he etch process [] continue[s] to etch the bulk semiconductor substrate 102 to form an extended recess 44." *Id.*, 6:47-51, FIG. 7,

below. The result of these multiple etch steps is a self-aligned recess that "may subsequently be used to form a second isolation region" by depositing "a second dielectric layer 308 … within the extended recess 44." *Id.*, 6:52-67, FIG. 8, below.



Excerpts from Akarvardar, FIGS. 5-8 (annotated)

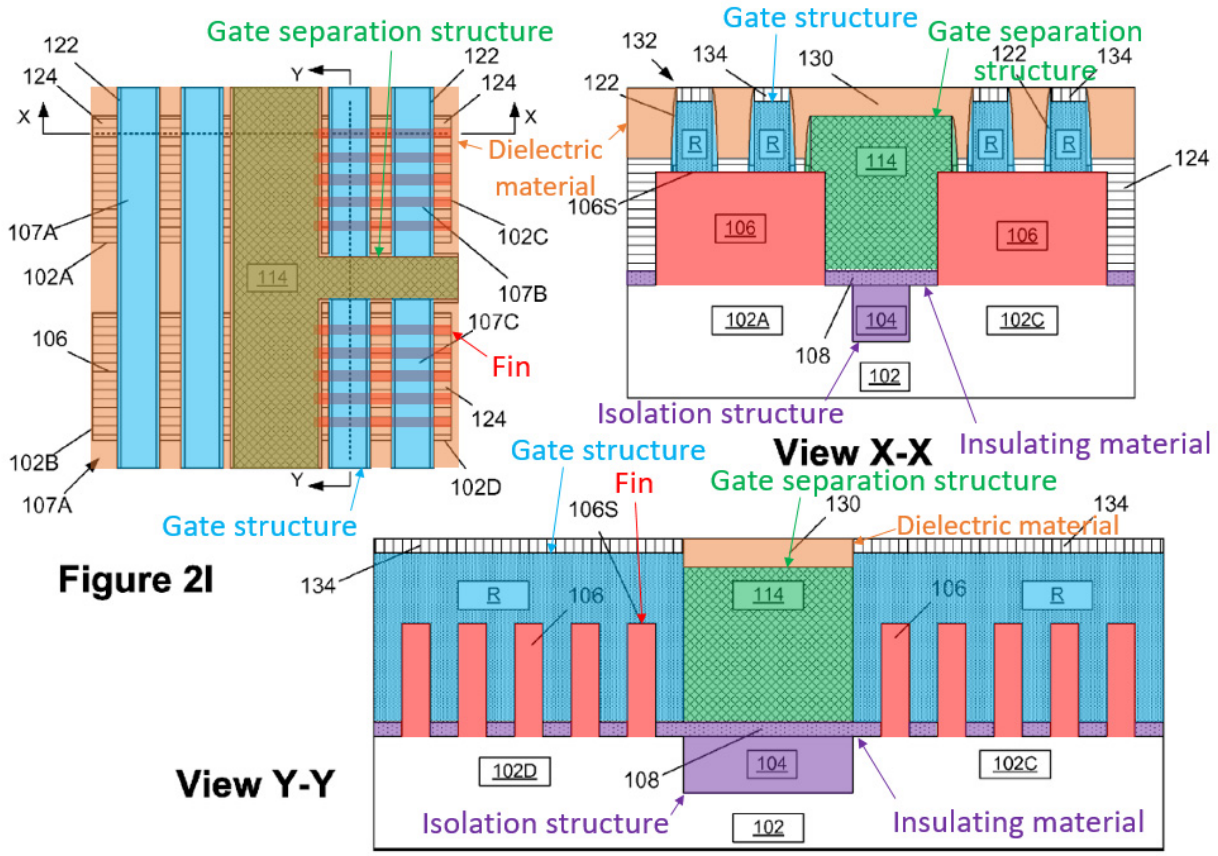
110. The second dielectric layer 308 deposited in the recess 44 forms the second isolation region 504, which is "self-aligned to the first group of fins 104 and the second group of fins 204." SAMSUNG-1010 (Akarvardar), 7:57-59; *see* 7:8-10, FIG. 9. Thus, "the use of additional masks to define the isolation regions

may not be required hence reducing bulk FinFET manufacturing costs." *Id.*, 8:25-28. Moreover, the illustrated configuration, which includes "self-aligned isolation regions having different heights and different depths," provides "enhanced device isolation and additional protection" to "each subsequently formed FinFET device." *Id.*, 8:9-22. For instance, "the first group of fins 104 may be part of a subsequently formed p-FET device and the second group of fins 204 may be part of a subsequently formed n-FET device, or vice versa" that are electrically isolated from one another by the second isolation region 504. *Id.*, 7:65-8:2.

2. Xie describes FinFET devices having gate separation structures

111. Xie, in the field of FinFET devices, describes "methods … for forming gate structures for FinFET devices and resulting devices." SAMSUNG-1004 (Xie), [0027]. One such FinFET structure is illustrated Xie's FIG. 2I, reproduced below. This structure includes a substrate 102 having "active regions 102A-D" defined by "isolation structures 104," which I have highlighted in purple. SAMSUNG-1004 (Xie), [0028]. "[A] plurality of fins 106," some of which are highlighted in red, are formed in the substrate. *Id.*. The fins extend from left to right in the top view and X-X cross-sectional views of FIG. 2I, and into the page in the Y-Y cross-sectional view: "the view 'X-X is taken along a line that passes through the fins 106, while the view 'Y-Y' is a cross-section view that is taken transverse to ***the long axis of the fins 106***." *Id.*, [0027]. An insulating material

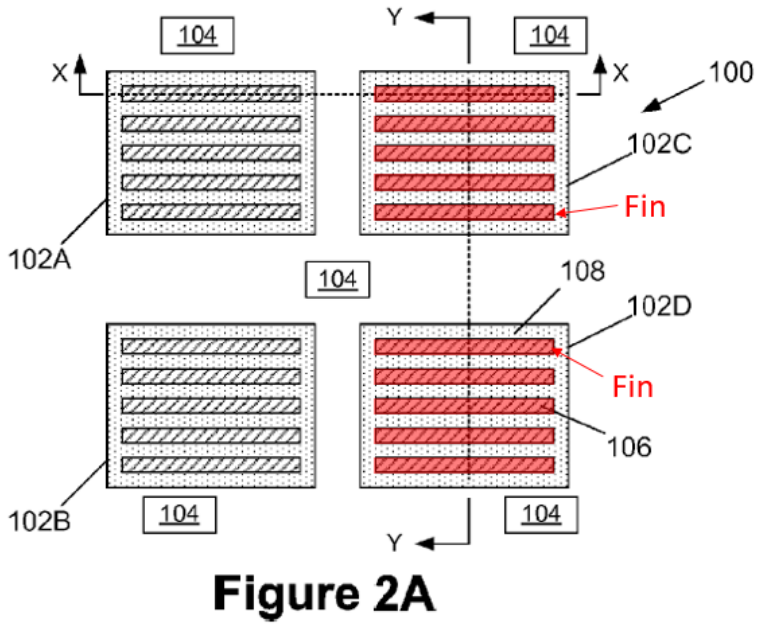
108, also highlighted in purple, "remains in the bottom of the trenches" between the fins "so as to locally isolate the fins 106 from one another." *Id.*, [0028].



Excerpt from Xie, FIG. 2I (annotated)[3]

[3] In the top view figure, the dielectric material 130 would cover the gate separation structure, as shown in the X-X and Y-Y views. I do not show the dielectric material as covering the gate separation structure in this (and other) reproductions of Xie's FIG. 2I in this document solely for clarity.

112. I note that in the top view of Xie's FIG. 2I, the fins 106 are covered with "an epi semiconductor 124" and as such, are obscured in the figure by the epi semiconductor layer 124. SAMSUNG-1004 (Xie), [0035]. A top view of the exposed fins 106 can be seen in FIG. 2A, the top view of which is reproduced below. FIG. 2A shows Xie's structure prior to deposition of the epi semiconductor 124 and confirms the presence of the fins.



Excerpt from Xie, FIG. 2A (annotated)

113. Returning to my discussion of Xie's FIG. 2I, gate structures, highlighted in blue, are disposed over the fins.[4] *See* SAMSUNG-1004 (Xie),

[4] I note that the top view of FIG. 2I includes reference numerals 107A-107C, which Xie identifies as sacrificial gate structures. *See* SAMSUNG-1004 (Xie),

[0016]-[0018], [0038]. Each gate structures is "a stack of material layers" that "may be formed using either gate-first or gate-last techniques." *Id.*, [0017], [0030]; *see* claims 4-5 ("wherein said plurality of gate structures are sacrificial gate structures" and "wherein said plurality of gate structures are final gate structures").

114. A "gate separation structure 114," which I have highlighted in green, is "positioned between the first and second spaced-apart gate structures" and over the insulating material 108. SAMSUNG-1004 (Xie), [0017], [0032]. A "layer of insulating material 130," highlighted in orange, is "blanket-deposited" onto the structure such that the insulating material is disposed on the gate separation structure 114 and to the sides of the gate separation structure and gate structures. SAMSUNG-1004 (Xie), [0036]; *see* FIG. 2I. For instance, in the top-view figure

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[0030]. It is my opinion that a POSITA would have understood that the features referred to by these reference numerals correspond to the replacement gate structures R and the gate cap layers 134, *e.g.*, based on the illustration in the X-X and Y-Y cross-sectional views and based on Xie's description of the fabrication process, in which the sacrificial gate structures 107 were previously removed and replacement gate structures R and gate cap layers 134 formed in the locations previously occupied by the sacrificial gate structures106. *See id.*, [0038].

of FIG. 2I, the insulating material extends into the page to the sides of the gate separation structure and gate structures.

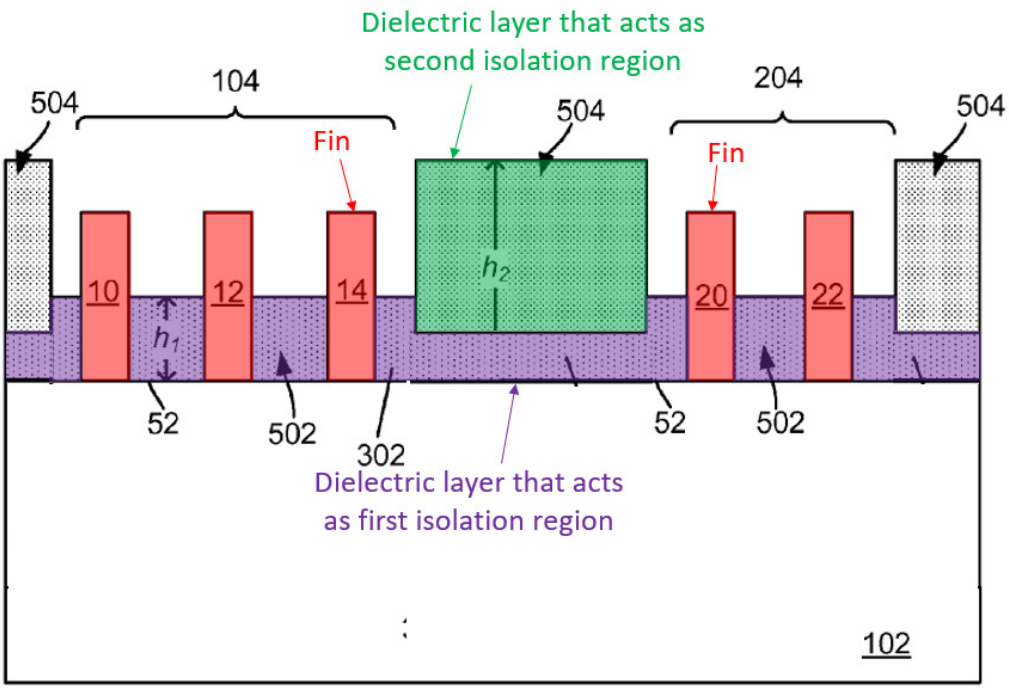
3. **The Akarvardar-Xie combination**

The self-aligned isolation region in the Akarvardar-Xie combination

115. I illustrate an example of a structure of the Akarvardar-Xie combination in the composite figure below. In this combination structure, fins (highlighted in red) are "formed from a bulk semiconductor substrate," as taught by Akarvardar. SAMSUNG-1010 (Akarvardar), 3:61-63, FIGS. 1-9. Also as taught by Akarvardar, a "first isolation region 502" (highlighted in purple) is made from a "first dielectric layer 302" disposed in the space around the base of the fins, to "electrically separate the fins 30 from one another." *Id.*, 7:35-37, 7:63-65, FIGS. 2-9.

116. A self-aligned "second isolation region 504" (highlighted in green) is made from a "second dielectric layer 308" that is disposed "between … the first group of fins 104 and the second group of fins 204" and "electrically separate[s]" the two groups of fins. SAMSUNG-1010 (Akarvardar), 6:39-41, 6:64-65, 7:8-10, 7:64-65. Based on the teachings of Xie, this second isolation region 504 is disposed on the first dielectric layer 302, *e.g.*, such that the second isolation region 504 does not extend into a recess formed in the bulk semiconductor substrate. *See* SAMSUNG-1004 (Xie), [0031]-[0032], [0039]-[0041], FIGS. 2C-2I (showing a

fabrication process in which the gate separation structure is formed on insulating material 108).



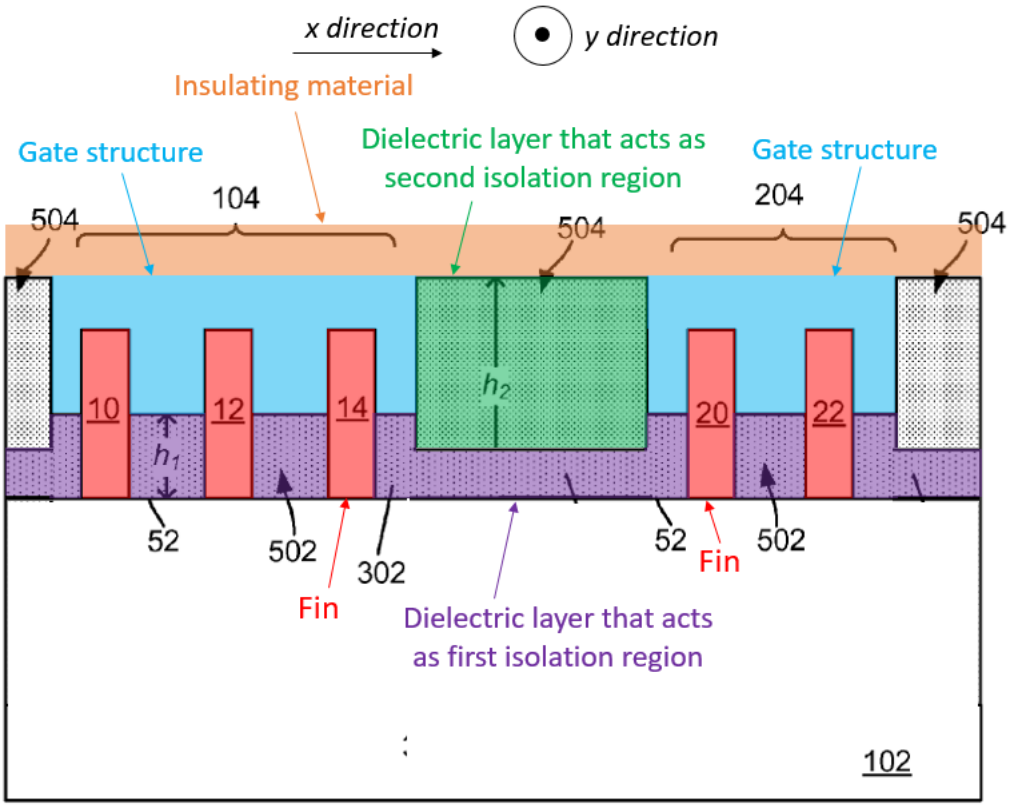
Akarvardar-Xie cross-sectional composite figure

117. In the combination, this configuration is implemented using a simplified version of the fabrication process described by Akarvardar, *e.g.*, based on the structure of Xie's integrated circuit device. For instance, consistent with Akarvardar's fabrication process, a recess 42 is opened by removing dummy material 304 from the recess, exposing a "portion of the first dielectric layer 302 positioned between … the first group of fins 104 and the second group of fins 204" at the bottom of the recess. *See* SAMSUNG-1010 (Akarvardar), 5:23-24, 6:33-41, FIGS. 5-6. Akarvardar's second dielectric layer 308 then is deposited into that

recess, *e.g.*, onto the exposed portion of the first dielectric layer 302. *See* SAMSUNG-1010 (Akarvardar), 6:64-66; *see* SAMSUNG-1004 (Xie), [0032], FIGS. 2C-2D (illustrating formation of the gate separation structure 114 in an opening 112, with insulating material 108 exposed at the bottom of the opening). That is, the dielectric layer 308 is deposited without formation of Akarvardar's extended recess 44: Akarvardar's further etch steps to remove the portion of the first dielectric layer and to etch an extended recess into the substrate (*see* SAMSUNG-1010 (Akarvardar), 6:39-51) are eliminated.

FinFET devices in the Akarvardar-Xie combination

118. The Akarvardar-Xie composite structure I described above is used as the base for "subsequently formed" FinFET devices, as suggested by Akarvardar. SAMSUNG-1010 (Akarvardar), 7:65-8:2. For instance, gate structures (highlighted in blue) are formed over the fins (red) and the first isolation regions 502 (purple), *e.g.*, based on the teachings of Xie. *See* SAMSUNG-1004 (Xie), [0016]-[0018], [0038]. The gate structures are "a stack of material layers," *e.g.*, including a gate dielectric layer and a gate electrode, as taught by Xie and as I discuss in more detail below. *See* SAMSUNG-1004 (Xie), [0017], [0030].



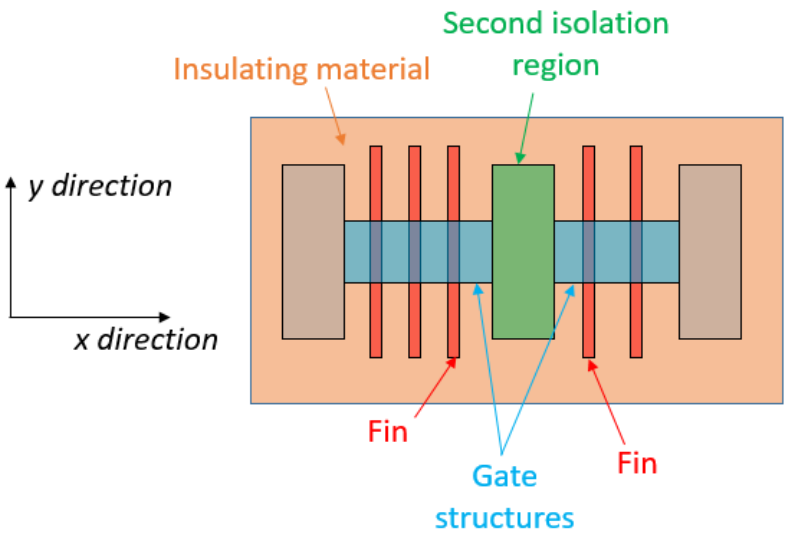
Akarvardar-Xie cross-sectional composite figure

119. Based on the teachings of Xie, the gate structures are "spaced-apart gate structures," with the modified second isolation region 504 (green) that I discussed above disposed between the edges of the two gate structures. *See* SAMSUNG-1004 (Xie), [0017] ("a gate separation structure positioned between the first and second spaced-apart gate structures"). In this configuration, the second isolation region electrically separates the two gates, consistent with its role in Akarvardar's structure. *See* SAMSUNG-1010 (Akarvardar), 8:1-4 ("p-FET and n-FET devices may be electrically separated by the second isolation region"), 7:66-8:4.

120. A "layer of insulating material 130," highlighted in orange, is "blanket-deposited" onto the gate structures and the modified second isolation region, as also taught by Xie. SAMSUNG-1004 (Xie), [0036].

121. I have generated the following composite top-view figure of elements of the Akarvardar-Xie structure.[5] In the combination, the fins extend in one direction (marked as the y-direction in the figures), and the gates extend orthogonal to the length of the fins (in the x-direction in the figures). *See* SAMSUNG-1010 (Akarvardar), FIG. 9; SAMSUNG-1004 (Xie), [0027] ("the view 'X-X' is taken along a line that passes through the fins 106, while the view 'Y-Y' is a cross-section view that is taken transverse to ***the long axis of the fins 106***."), Fig. 2I. The layer of insulating material is disposed over the top of illustrated structure, extending into the page next to the sidewalls of the gate structures and next to at least the end walls of the modified second isolation region 504. *See* SAMSUNG-1004 (Xie), [0036].

[5] This top view composite figure is for illustration only and is not to scale. For instance, the extent of the long axis of the fins, the extent of the second isolation region, or the width of the gate structures in the y-direction are not necessarily as they are depicted in this figure.



Akarvardar-Xie top-view composite figure

4. **Reasons to combine Akarvardar and Xie**

122. It is my opinion that a POSITA would have been motivated to implement the Akarvardar-Xie combination for at least the following reasons.

Arrangement of Akarvardar's second isolation region on the first dielectric layer

123. First, as I discussed above, in the Akarvardar-Xie combination structure, the configuration of Akarvardar's second isolation region 504 is modified based on the teachings of Xie such that the second isolation region is disposed on the first dielectric layer 302, *e.g.*, rather than extended into the substrate. It is my opinion that a POSITA would have been motivated to pursue this implementation for at least the following reasons.

124. One reason why a POSITA would have been motivated to modify the configuration of Akarvardar's second isolation region in this way is to simplify the

processing. The number of process steps involved in forming this modified second isolation region is reduced as compared to the fabrication process described by Akarvardar. For instance, Akarvardar describes three etch steps to form the second isolation region: a first etch to remove dummy material 304 (*see* SAMSUNG-1010 (Akarvardar), 5:23-24, FIGS. 5-6), thus forming a recess 42; a second etch to remove the portion of the first dielectric layer from the recess (*see id.*, 6:39-46, FIGS. 6-7); and a third etch to form an extended recess in the semiconductor substrate (*see id.*, 6:47-51, FIG. 7). By contrast, the second isolation region in the Akarvardar-Xie combination is formed using only the first etch to remove the dummy material; Akarvardar's second and third etches are eliminated. It is my opinion that a POSITA would have recognized the advantages, *e.g.*, processing efficiency and corresponding time and cost savings, that would be achieved by this processing change, and would have been motivated to pursue this implementation to achieve these advantages.

125. Another reason why a POSITA would have been motivated to pursue this modification to Akarvardar's second isolation region is that the POSITA would have recognized that the self-alignment of Akarvardar's second isolation region would be maintained in the combination. *See* SAMSUNG-1010 (Akarvardar), 3:51-56, 7:57-58, 8:9-22; claims 2, 10. Specifically, it is my opinion that a POSITA would have recognized the advantages of self-aligned isolation

structures and would have been motivated to pursue an approach in which these advantages are maintained even with a simpler fabrication process. *See* SAMSUNG-1010 (Akarvardar), 8:23-28 ("since the second isolation region is self-aligned with respect to the groups of fins, the use of additional masks to define the isolation regions may not be required hence reducing bulk FinFET manufacturing costs"); SAMSUNG-1009 (Chang), [0056] ("This self-aligned gate formation process may allow the diffusions 104 to be placed closer together than if alignment errors need to be taken into account for gate placement"). To the extent there is a reduction in the ability of Akarvardar's modified second isolation region to "electrically isolate one group from the neighboring group of fins" (SAMSUNG-1010 (Akarvardar), 8:14-16) because it no longer extends into the underlying substrate, a POSITA would nevertheless recognize that some isolation benefit is still obtained, and would weigh the advantages offered by the simplified fabrication process against the potential reduction in isolation capability.

126. I also believe that a POSITA would have been motivated to modify Akarvardar's structure based on the structure described by Xie because of the similarity between the Akarvardar and Xie structures. I note that Akarvardar's process enables the fabrication of a structure such as that described by Xie—that is, a structure where the isolation structure between the gates is located on a dielectric layer on top of the substrate instead of extending into the substrate.

Given these similarities, I believe a POSITA would have viewed the depth of the etch (and thus the depth of the resulting isolation structure) as a matter of obvious design choice that a POSITA would have readily considered in evaluating Akarvardar's process in view of Xie's structural design. *Id.* For instance, a POSITA would have found it obvious to consider the parameters of Xie's design—height and depth of the isolation structure—when looking to implement and potentially simplify Akarvardar's process.

127. Additionally, a POSITA would have been motivated to modify Akarvardar's second isolation region simply because this implementation is just the application of known techniques (*e.g.*, gate isolation structures that do not extend into the underlying substrate) to a known structure (*e.g.*, a finFET integrated circuit structure) that results in a predictable outcome (*e.g.*, a finFET-based integrated circuit having a gate isolation structure disposed on a layer of dielectric material on the substrate).

128. It is my opinion that a POSITA would have expected success in pursuing this implementation because the configuration of the Akarvardar-Xie isolation region would retain, at least to some extent, the functional benefits provided by Akarvardar's unmodified second isolation region. For instance, Akarvardar describes its second isolation region as "providing … device isolation" between FinFET devices. SAMSUNG-1010 (Akarvardar), 8:16-20. Xie

demonstrates that isolation regions between gates electrically isolate those gates even when the isolation regions do not extend into the substrate. *See* SAMSUNG-1004 (Xie), [0032], [0035]. Akarvardar also describes that its second isolation region provides "additional protection during subsequent processing steps, including CMP of gate structures and epi isolation." SAMSUNG-1010 (Akarvardar), 8:16-22. Because the height of Akarvardar's second isolation region is not modified in the combination, I believe that a POSITA would have expected the second isolation region in the combination to continue to afford these physical protection advantages.

129. Additionally, it is my opinion that a POSITA would have expected success because Akarvardar itself indicates that the etching of the first dielectric layer and substrate to form the extended recess are optional: "a portion of the first dielectric layer 302 positioned between two groups of fins … ***may be removed***," and "[t]he etch process ***may continue to etch the bulk semiconductor substrate*** 102 to form an extended recess." SAMSUNG-1010 (Akarvardar), 6:39-51. Indeed, the structure of the Akarvardar-Xie combination is generally of a similar configuration to the interim Akarvardar structure of Akarvardar's FIG. 4.

130. Furthermore, it is my opinion that a POSITA also would have expected success given that FinFET devices having gate isolation structures that do not extend into the underlying substrate were well-known in the art as of the

Critical Date. *See* SAMSUNG-1004 (Xie), [0032] ("a gate separation structure 114 was formed in the opening"), FIG. 2I; SAMSUNG-1009 (Chang), [0056], FIG. 18a; SAMSUNG-1012 (Bohr), Abstract ("ends of adjacent semiconductor fins are electrically isolated from each other with an isolation region that is self-aligned to gate electrodes of the semiconductor fins").

Incorporation of gate structures

131. Second, it is my opinion that a POSITA would have been motivated to incorporate gate structures into the Akarvardar-Xie integrated circuit structure for at least the following reasons.

132. One reason why POSITA would have been motivated to incorporate gate structures into the combination is to follow Akarvardar's direction to use its structure with "subsequently formed FinFET device[s]." SAMSUNG-1010 (Akarvardar), 8:19. Indeed, I believe that a POSITA would have recognized gate structures as standard features of FinFET devices and would have provided gate structures as part of the FinFET fabrication process. *See* SAMSUNG-1009 (Chang), [0036] 9 ("a circuit 100 that includes transistors with end caps of gates 106 self-aligned to diffusions 104"); SAMSUNG-1005 (Tseng), 3:4-12 ("The semiconductor device 200 comprises a FinFET" that includes "a gate electrode layer 214 traversing over the first fin 202a and second fin 202b"), 5:5-42 ("The gate electrode layer 214 and the gate dielectric layer 212 form a gate stack 210");

SAMSUNG-1004 (Xie), [0016]-[0018] ("forming a stack of material layers to form a plurality of gate structures above a plurality of spaced-apart active regions defined in a semiconductor substrate"), [0038] ("FIG. 2I depicts the product 100 after a schematically depicted replacement gate structure 'R' and a gate cap layer 134 have been formed in the gate cavities"); SAMSUNG-1006 (Anderson), [0038]-[0039] ("gate stack 20 is formed over the isolation structures 28a and 28b and the exposed portions of the wafer 10. The gate stack 20 can be, for example, a gate dielectric and a gate electrode material"); SAMSUNG-1007 (Lin), 4:65-5:9 ("a second etch process to complete etching of gate electrode layer 120 … thereby forming gate electrodes 432").

133. Additionally, it is my opinion POSITA would have been motivated to incorporate gate structures into the combination because this implementation is just the application of known techniques (*e.g.*, gate structures in an integrated circuit device) to a known structure (*e.g.*, a finFET integrated circuit structure) resulting in a predictable outcome (*e.g.*, a finFET-based integrated circuit having gate structures).

134. It is my opinion that a POSITA would have expected success in incorporating gate structures into the combination because gate structures are part of the "subsequently formed FinFET device[s]" to be made from Akarvardar's structures. SAMSUNG-1010 (Akarvardar), 8:19-22; see 7:64-8:4. Indeed,

Akarvardar explicitly contemplates the formation of "gate structures" in its devices. SAMSUNG-1010 (Akarvardar), 8:21. It is also my opinion that a POSITA would have expected success given that the use of gate structure in FinFET-based devices, was standard as of the Critical Date. *See* SAMSUNG-1009 (Chang), [0036]; SAMSUNG-1005 (Tseng), 3:4-12, 5:5-42; SAMSUNG-1004 (Xie), [0016]-[0018], [0038]; SAMSUNG-1006 (Anderson), [0038]-[0039]; SAMSUNG-1007 (Lin), 4:65-5:9.

Incorporation of an interlayer dielectric

135. Third, it is my opinion that a POSITA would have been motivated to incorporate an interlayer dielectric (ILD) into the Akarvardar-Xie integrated circuit structure for at least the following reasons.

136. One reason why a POSITA would have been motivated to incorporate an ILD into the combination is to provide electrical isolation between the transistor-level structures (*e.g.*, the "subsequently formed FinFET device[s] contemplated by Akarvardar) and overlying interconnect structures. SAMSUNG-1010 (Akarvardar), 7:65-8:2, 8:19-22; *see* SAMSUNG-1008 (Kawa), [0068] ("An insulating fill 515 provides an interlayer insulator between the patterned gate conductor layer including the gate traces 505 and 506, and overlying patterned conductor layers, including the first patterned conductor layer M1"); SAMSUNG-1017 (Basker), 6:42-44 ("The ILD layer 20 may fill the gaps between gate

structures and other existing devices within the semiconductor structure 300"); SAMSUNG-1039 (Pethe), 9:5-8 ("The inter-layer dielectric (ILD) 330 may be composed of a material suitable to electrically isolate metal features ultimately formed therein while maintaining a robust structure between front end and back end processing"). For instance, the presence of an ILD would enable the FinFET devices envisioned by Akarvardar to be connected to upper-level wiring. *See* SAMSUNG-1010 (Akarvardar), 7:65-8:2, 8:19-22; SAMSUNG-1008 (Kawa), [0068].

137. A second reason why POSITA would have been motivated to incorporate an ILD into the combination is because the use of ILDs above transistor-level structures was a standard element of integrated circuits. *See* SAMSUNG-1004 (Xie), [0036] ("FIG. 2G depicts the product 100 after a layer of insulating material 130, e.g., silicon dioxide, has been blanket-deposited above the epi semiconductor material"), FIG. 2I; SAMSUNG-1009 (Chang), [0051] ("An ILD layer 1504 may be deposited and planarized so the top of the ILD layer 1504 may be substantially planar with the top of the remaining insulating material 802 and first gate material 1102"), FIGS. 15A-18D; SAMSUNG-1007 (Lin), 5:15-17 ("an inter-layer dielectric (ILD) 560 formed over the gate electrodes 432"), FIGS. 5A-5C; SAMSUNG-1008 (Kawa), [0068] ("An insulating fill 515 provides an interlayer insulator between the patterned gate conductor layer including the gate

traces 505 and 506, and overlying patterned conductor layers"), FIG. 5; SAMSUNG-1017 (Basker), 6:42-44 ("The ILD layer 20 may cover the gate structure 14 … [and] may fill the gaps between gate structures and other existing devices within the semiconductor structure 300"), FIG. 5; SAMSUNG-1039 (Pethe), 9:1-8 ("an inter-layer dielectric (ILD) 330 and hardmask 332 stack is formed and patterned to provide, e.g., a metal (0) trench 334"), FIG. 3F.

138. Additionally, a POSITA would have been motivated to incorporate an ILD into the combination because this implementation is just the application of known techniques (*e.g.*, ILD in an integrated circuit device) to a known structure (*e.g.*, a finFET integrated circuit structure) resulting in a predictable outcome (*e.g.*, a finFET-based integrated circuit having an ILD disposed on the gate structures).

139. It is my opinion that a POSITA would have expected success in pursuing the incorporation of an ILD into the combination because the use of an ILD is compatible with the further device structure and processing described by Akarvardar. *See* SAMSUNG-1010 (Akarvardar), 8:19-22 ("providing to each subsequently formed FinFET device enhanced device isolation and additional protection during subsequent processing steps, including CMP of gate structures and epi isolation"). A POSITA also would have expected success given that the use of ILDs in integrated circuits, such as FinFET-based devices, was well-known as of the Critical Date. *See* SAMSUNG-1004 (Xie), [0036], FIG. 2I; SAMSUNG-

1009 (Chang), [0051], FIGS. 15A-18D; SAMSUNG-1007 (Lin), 5:15-17, FIGS. 5A-5C; SAMSUNG-1008 (Kawa), [0068], FIG. 5; SAMSUNG-1017 (Basker), 6:42-44, FIG. 5; SAMSUNG-1039 (Pethe), 9:5-8, FIG. 3F.

5. The Akarvardar-Xie gate structures each includes a gate dielectric layer and a gate electrode

140. As I discussed previously, based on the teachings of Xie, the gate structures in the Akarvardar-Xie combination include "a stack of material layers" including "a high-k (k value greater than 10) gate insulation layer," "one or more metal layers … (e.g., layers of titanium nitride or TiAlC)," and "a bulk conductive metal layer … such as tungsten or aluminum." SAMSUNG-1004 (Xie), [0038], claim 1; *see* claim 5, [0015]-[0016], [0040]. It is my opinion that to the extent Xie does not explicitly disclose gate structures each having a gate dielectric layer and a gate electrode, a POSITA would have found this configuration obvious, as I discuss in the following paragraphs.

141. First, I note that it was well-known in the art as of the Critical Date for a gate structure in a FinFET device to include a gate dielectric layer (*e.g.*, a high-k gate dielectric layer) and a gate electrode (*e.g.*, a metal gate electrode). *See*, *e.g.*, SAMSUNG-1005 (Tseng), 5:5-46 (describing that the gate dielectric layer is a "high dielectric constant (high-k) dielectric" and the gate electrode includes an "N-work function metal" or a "P-work function metal"), 8:67-9:4 ("the gate-last process comprises … fill[ing] the trench with ***a gate dielectric layer and a***

conductive gate electrode layer"), FIGS. 2 and 5A; SAMSUNG-1025 (Ching), 4:39-5:3 ("[t]he resulting remaining portions of the conductive material and gate dielectric layer 50 thus form the ***replacement gate, which includes gate electrode 52 and gate dielectric 50***," where "gate dielectric layer 50 comprises a high-k dielectric material" and "[c]onductive material 52 may comprise a metal-containing material such as TiN, TaN, TaC, Co, Ru, Al, combinations thereof"), Fig. 9A; SAMSUNG-1006 (Anderson), [0029] ("The gate stack 20 can be, for example, ***a gate dielectric and a gate electrode material***," where "the gate dielectric can be, for example, a high-k dielectric material" and "the gate electrode material being either a metal or a metal and polysilicon stack"); SAMSUNG-1011, 3:59-4:10 ("The gate structure 110 includes a gate dielectric layer and a gate electrode. … The gate dielectric layer may further include … dielectric with a high dielectric constant (high-k) … The gate electrode may include … a metal including metal compounds such as, TiN, TaN, NiSi, CoSi, Mo, Cu, W, Al, Co"); SAMSUNG-1012 (Bohr), 4:46-48 ("The gate electrode 120 … is a portion of a gate electrode stack which further includes a gate dielectric layer 165"); SAMSUNG-1013 (Chuang), 3:45-46 ("Gate electrode strip 32 and gate dielectric 145 form the gate stack of FinFET 100"); SAMSUNG-1014 (Kuo), 7:8-22 ("a gate dielectric 230 and a gate structure 232 are formed over the second insulation layer 228"); SAMSUNG-1015 (Shieh), [0041] ("a substrate 1 with fins 4, shallow trench

isolations (STIs) 6, a gate dielectric 9, and a gate electrode layer 8 formed thereon"), [0046]-[0047]. Indeed, the '306 Patent itself acknowledges that this was conventional: *see* SAMSUNG-1001, 3:49-4:49 (acknowledging that in "a conventional finFET or tri-gate process fabrication scheme," "the dummy gate electrode … is replaced with permanent gate electrodes" and "a dummy gate dielectric layer may also be replaced by a permanent gate dielectric layer").

142. In view of the state of the art and given Xie's description of the composition of its gate structures (*see* SAMSUNG-1004 (Xie), [0038] ("Such a replacement gate structure typically comprises a high-k … gate insulation layer … and a bulk conductive material layer"), [0015]-[0016] ("forming a stack of material layers to form a plurality of gate structures"), [0040], claims 1 and 5), it is my opinion that a POSITA would have understood or found obvious that the Akarvardar-Xie gate structures each comprises "a stack of material layers" including a gate dielectric layer (*e.g.*, Xie's a high-k gate insulation layer) and a gate electrode (*e.g.*, Xie's bulk conductive metal layer). SAMSUNG-1004 (Xie), [0038].

143. It is my opinion that a POSITA would have been motivated to implement the "high-k … gate insulation layer" and "bulk conductive metal layer" of Xie's gate structure as a high-k gate dielectric layer and metal gate electrode, respectively, for at least the following reasons.

144. One reason why a POSITA would have been motivated to implement a high-k gate dielectric and a metal gate electrode is because gate structures having high-k gate dielectric layers and metal gate electrodes were standard elements of FinFET transistors, as I discussed above. *See*, *e.g.*, SAMSUNG-1005, 5:5-46; SAMSUNG-1025, 4:39-5:3; SAMSUNG-1011 (Gan), 3:59-4:10. The implementation of Xie's gate insulation layer and bulk conductive material layer as a gate dielectric layer and gate electrode, respectively, is thus merely a comprehensive implementation of a structure already described by Xie.

145. Another reason why a POSITA would have been motivated to pursue the use of a high-k gate dielectric layer and a metal gate electrode is to obtain the performance advantages afforded by use of these materials. For instance, high-k gate dielectrics decrease threshold voltage, reduce fringe capacitance, and suppress leakage current. *See* SAMSUNG-1011, 1:32-35 ("There has been a desire to replace the gate oxide and polysilicon gate electrode with a high-k gate dielectric and metal gate electrode ***to improve device performance as feature sizes continue to decrease***."); SAMSUNG-1026 (Guo), Abstract ("A high-k dielectric is used for the gate dielectric, providing increased inversion carrier density without having to resort to aggressive scaling of the thickness of the gate dielectric while at the same time preventing excessive gate leakage current from occurring.."); SAMSUNG-1027 (Lee), 1:38-46 ("methods have been sought to reduce leakage current while

achieving a high gate capacitance. One method investigated by the industry is the use of materials having a high dielectric constant (high-k or high-∈) for the gate dielectric layer."); SAMSUNG-1028 (Metz), Abstract ("The high-k gate dielectric layer has off-state leakage characteristics that are superior to those of a silicon dioxide based gate dielectric, and on-state mobility characteristics that are superior to those of a high-k gate dielectric that comprises an isotropic material.). Moreover, the use of a high-k gate dielectric layer provides the gate with finer control over the channel potential, enabling more effective on/off control to be achieved, thus facilitating higher speed performance. *See* SAMSUNG-1028 (Metz), Abstract.

146. Additionally, a POSITA would have been motivated to use high-k gate dielectric layers and metal gate electrodes because this implementation is just the application of known techniques (*e.g.*, high-k gate dielectric layers and metal gate electrodes) to a known structure (*e.g.*, the gate insulation layer and bulk conductive metal layer of the gate structure of Xie's FinFET device) that results in a predictable outcome (*e.g.*, a gate structure having a high-k gate dielectric layer and a metal gate electrode).

147. It is my opinion that a POSITA would have expected success in high-k gate dielectric layers and metal gate electrodes because these materials are consistent with Xie's description of the composition of its gate structures. *See*

SAMSUNG-1004 (Xie), [0038] ("a high-k (k value greater than 10) gate insulation layer," "one or more metal layers," and "a bulk conductive metal layer"). It is also my opinion that a POSITA also would have expected success given that high-k gate dielectric layers and metal gate electrodes are well-known elements of both replacement gate structures and gate-first gate structures for FinFET devices. *See* SAMSUNG-1005 (Tseng), 5:5-46, 8:67-9:4, FIG. 5A; SAMSUNG-1025 (Ching), 4:39-5:3, FIG. 9A; SAMSUNG-1006 (Anderson), [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1012 (Bohr), 4:46-48 SAMSUNG-1013 (Chuang), 3:45-46; SAMSUNG-1014 (Kuo), 7:8-22; SAMSUNG-1015 (Shieh), [0041], [0046]-[0047].

6. Analysis

(1) Claim 26

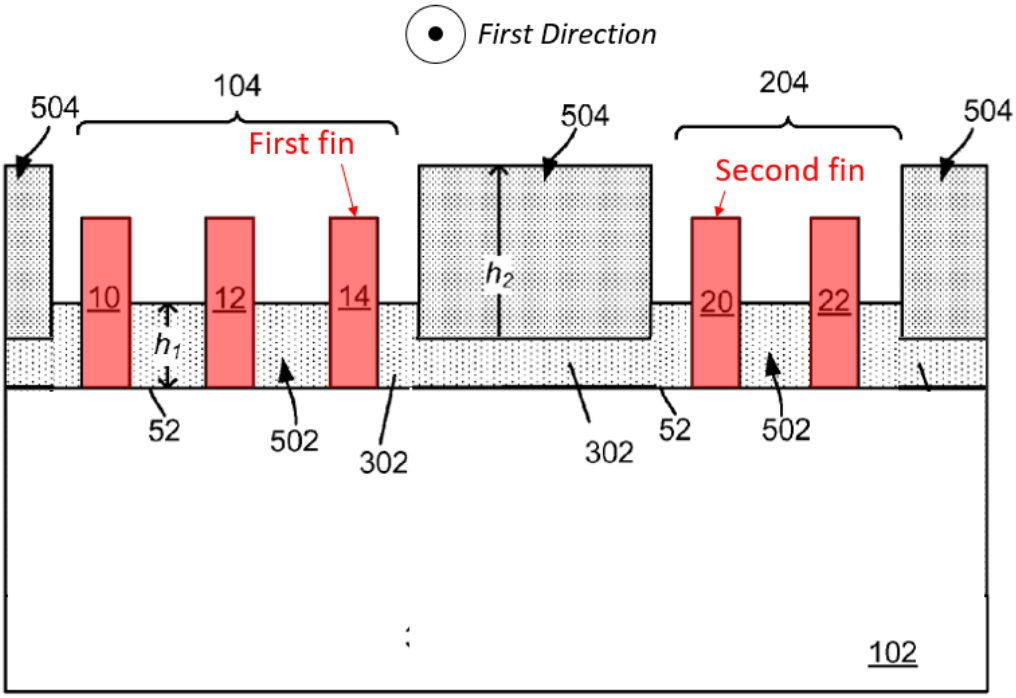
[26pre] An integrated circuit structure, comprising:

148. To the extent the preamble is deemed to be limiting, it is my opinion that the Akarvardar-Xie combination renders it obvious. For instance, Akarvardar indicates that its structure is for use with "FinFET device[s]." SAMSUNG-1010 (Akarvardar), 8:19; *see* 1:6-9 ("The present disclosure generally relates to semiconductor structures, and more particularly to bulk fin field effect transistor (FinFET) devices").

[26a] a first fin comprising silicon, the first fin having a longest dimension along a first direction;

[26b] a second fin comprising silicon, the second fin having a longest dimension along the first direction;

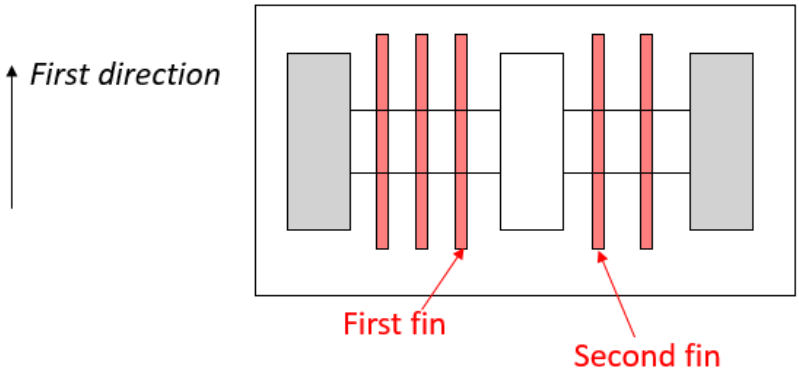
149. The Akarvardar-Xie combination renders obvious [26a] and [26b]. For instance, the Akarvardar-Xie combination structure includes **first and second fins**, *e.g.*, based on Akarvardar's fins 14, 20, which I have highlighted in red in the composite figures below. *See* SAMSUNG-1010 (Akarvardar), 3:61-63 ("the semiconductor structure 100 may include a plurality of fins 30"), 4:23-31 ("The fins 30 may include a first group of fins 104 and a second group of fins 204. … the first group of fins 104 may include 10, 12, 14 and the second group of fins 204 may include fins 20 and 22"), 2:15-18 ("forming a first group of fins and a second group of fins in a bulk semiconductor substrate"), 2:39-44 ("the first and second groups of fins are formed in a bulk semiconductor substrate"), 4:32-46, FIGS. 1-9.



Akarvardar-Xie cross-sectional composite figure

150. In the Akarvardar-Xie combination structure, each fin has **a longest dimension along a first direction**, which I have marked in the cross-sectional composite figure above and in the top-view composite figure below. I should note that this direction was previously designated as the Y-direction. As shown, the first direction extends into the page in the cross-sectional view and top to bottom in the top view. To the extent that Akarvardar does not explicitly state this orientation of the fins, it is my opinion that a POSITA would have understood this to be the case given that it was well-known in the art as of the Critical Date for fins in FinFET devices to be elongated in one direction. *See*, *e.g.*, SAMSUNG-1004, [0027], FIG. 2A; SAMSUNG-1006 (Anderson), [0036], FIG. 11; SAMSUNG-

1007 (Lin), 2:14-25, FIGS. 1A-1C; SAMSUNG-1005 (Tseng), 3:4-15, FIG. 2. An example top view of the Akarvardar-Xie combination structure is shown in the composite figure below, illustrating that each fin has a longest dimension. This longest dimension is **along the first direction** in that the longest dimension of the fins is traversed ***as one moves along the fins in the first direction***.



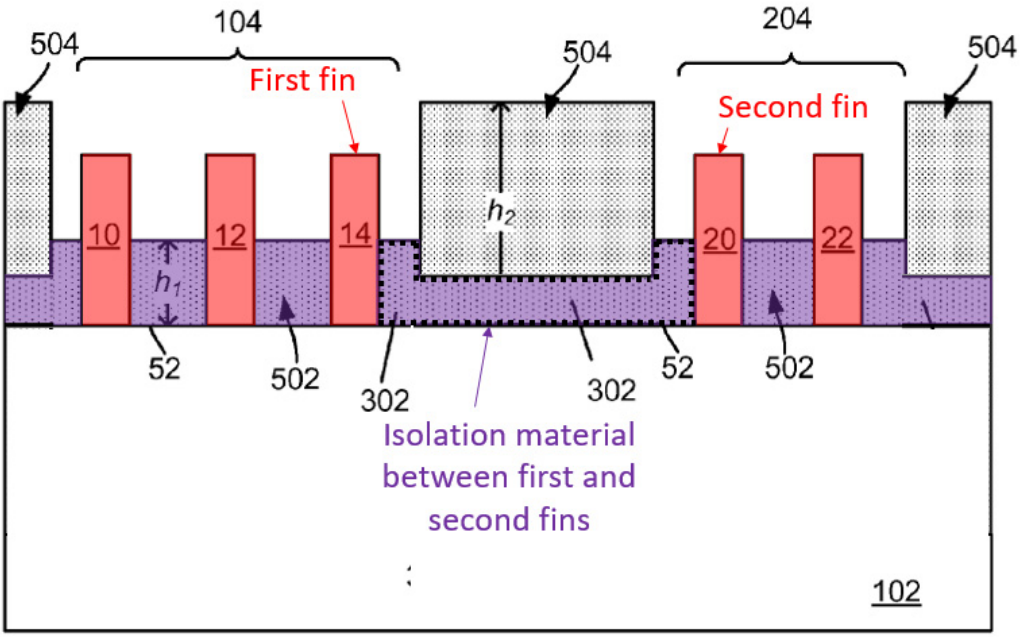
Akarvardar-Xie top-view composite figure

151. Also in the Akarvardar-Xie combination structure, **the fins comprise silicon**. For instance, Akarvardar describes that the "plurality of fins" are "formed from a bulk semiconductor substrate 102," which "may include ***a bulk silicon substrate***." SAMSUNG-1010 (Akarvardar), 3:62-65; *see* 3:64-4:8, FIG. 1.

[26c] an isolation material between the first fin and the second fin;

152. The Akarvardar-Xie combination renders obvious [26c]. For instance, the Akarvardar-Xie combination structure includes **an isolation material**, *e.g.*, based on Akarvardar's "***first dielectric layer 302***," which I have highlighted in purple in the composite figure below. SAMSUNG-1010 (Akarvardar), 7:36-38;

see 4:59-67 ("a first dielectric layer 302 may be deposited on the semiconductor structure"), 2:18-27 ("A first dielectric layer is conformally deposited on the bulk semiconductor substrate above the first and second group of fins; the first dielectric layer substantially fills a space between each individual fin of the first and second group of fins"), 2:2-5 ("forming a first isolation region between fins of a first group of fins and fins of a second group of fins"), 5:65-6:3 ("a thickness of a remaining portion of the first dielectric layer 302 may represent a height (h1) of a shallower isolation region"), 7:63-65, FIGS. 2-9.



Akarvardar-Xie cross-sectional composite figure

153. In the combination, the dielectric material 302 is **an isolation material** because it provides electrical isolation between fins, as described by Akarvardar: "the semiconductor structure 100 may include a first isolation region

502 made from the first dielectric layer 302," where "[t]he first isolation region 502 may ***electrically separate the fins 30 from one another***." SAMSUNG-1010 (Akarvardar), 7:35-37, 63-64; *see* 8:9-14 ("The first isolation region may be located between each individual fin of a determined group of fins to electrically isolate each fin from one another"), 2:2-4 ("forming a first isolation region between fins of a first group of fins and between fins of a second group of fins").

154. The isolation material (*e.g.*, Akarvardar's dielectric material 302 forming the first isolation regions) is **between the first and second fins** in the combination at least in that it is in the space separating the first and second fins, as shown in the composite figure above. Indeed, Akarvardar describes depositing the first dielectric layer 302 between the first and second fins. *See* SAMSUNG-1010 (Akarvardar), 5:18-20 ("the first dielectric layer 302 may be conformally deposited between two groups of fins, such as the first and second group of fins 104, 204"), 5:4-14 ("depositing the first dielectric layer 302 … may … create a conformal contour in the gap 38," which is "the distance between any two adjacent groups of fins," *id.*, 4:31-32), 8:10-14, FIGS. 2-6. Akarvardar describes later removing the portion of the first dielectric layer between the first and second fins. *See* 6:39-41 ("a portion of the first dielectric layer 302 positioned between two groups of fins, such as the first group of fins 104 and the second group of fins 204 … may be removed"), 2:24-27, FIG. 7. However, in the combination, this portion of the first

dielectric layer is not removed, based on the teachings of Xie, as I have previously discussed. Thus, this portion of the first dielectric layer that is "positioned between … the first group of fins 104 and the second group of fins" (SAMSUNG-1010 (Akarvardar), 6:39-41), outlined in dashed lines, remains in the combination structure, and is **between the first fin and the second fin** in the Akarvardar-Xie combination.

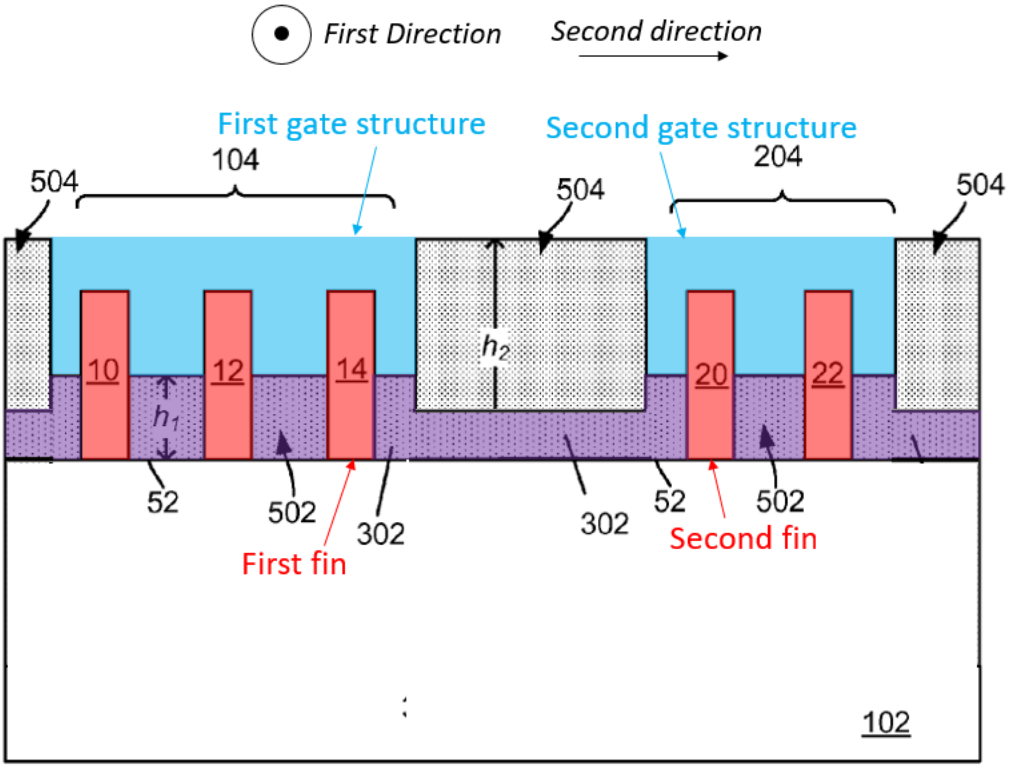
[26d] a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;

[26e] a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;

The Akarvardar-Xie combination includes first and second gate structures

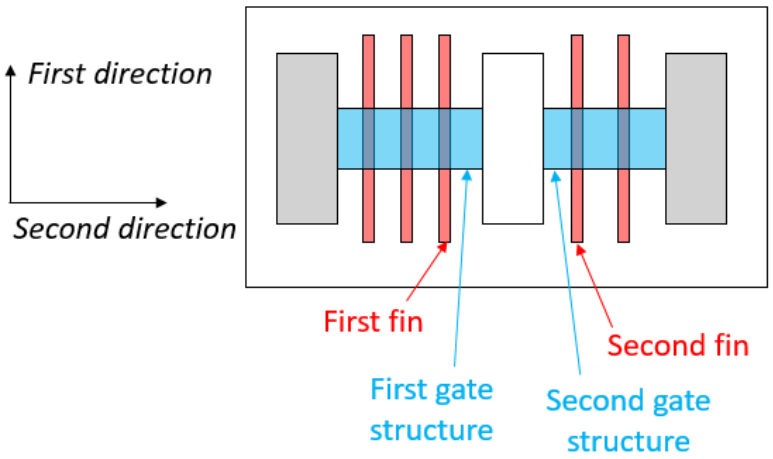
155. The Akarvardar-Xie combination renders obvious [26d] and [26e]. For instance, the Akarvardar-Xie combination structure includes **first and second gate structures**, *e.g.*, based on Xie's "***final gate structures***," which I have highlighted in blue in the composite figure below. SAMSUNG-1004 (Xie), [0030]. For instance, based on the teachings of Xie, and as I discuss further below, the first and second gate structures are disposed on opposing sides of a gate edge isolation structure that is based on a modified version of Akarvardar's second isolation region 504 (*see* [26g]). *See* SAMSUNG-1004 (Xie), [0017] ("***first and***

second spaced-apart gate structures"), [0040] ("the stack of materials 140S that will comprise ***the gate structure 140*** (be it a final gate structure or a sacrificial gate structure) are blanket-deposited," and "[t]he formation of the trenches 112 defines what will become the end surfaces 110X of the ***gate structures 140***"), claims 1 and 5 ("forming a stack of material layers to form said plurality of gate structures," "wherein said plurality of gate structures are final gate structures"), [0002] ("methods of forming ***gate structures*** for FinFET devices"), [0013]-[0016], [0027], [0041], FIG. 2I, FIGS. 2K-2O, claims 9, 11, and 16.



Akarvardar-Xie cross-sectional composite figure

156. The first and second gate structures in the combination structure have **a longest dimension along a second direction** in that the longest dimension of the gate structures is traversed ***as one moves along the gate structures in the second direction*** (from left to right in the cross-sectional and top-view composite figures). This configuration is consistent with the configuration of Xie's gate structures. *See* SAMSUNG-1004 (Xie), FIG. 2I.



Akarvardar-Xie top-view composite figure

157. In the combination structure, **the second direction is orthogonal to the first direction**, *e.g.*, the gates extend in a direction orthogonal to the direction in which the fins extend, as shown in the composite figures above. *See* SAMSUNG-1004 (Xie), FIG. 2I, SAMSUNG-1010 (Akarvardar), FIG. 9. To the extent that Xie does not explicitly state this orthogonality, it is my opinion that a POSITA nevertheless would have understood this to be the case, or otherwise found this to be obvious, consistent with the schematic depiction of Xie's structure

in FIG. 2I and given that gate structures orthogonal to fins in FinFET devices was well-known in the art as of the Critical Date. *See*, *e.g.*, SAMSUNG-1008 (Kawa), [0053]; SAMSUNG-1029 (Zhu), [0042] ("The patterned second gate conductor 106 intersects the semiconductor fin and extends, e.g., along a direction perpendicular to a length direction of the semiconductor fin 102."); SAMSUNG-1030 (Basker), Abstract ("The fin structures each comprise a semiconductor layer and extend in a first direction, and the gate stack extends in a second direction that is perpendicular.").

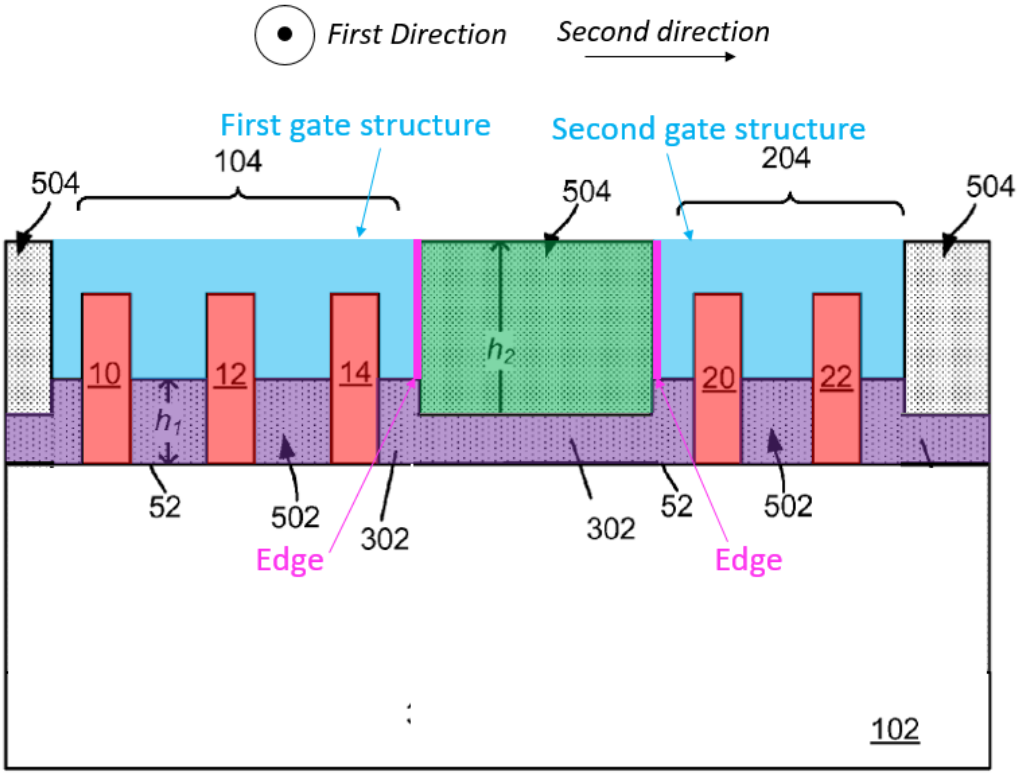
The Akarvardar-Xie gate structures are positioned in the recited configuration

158. In the Akarvardar-Xie combination structure, the **first gate structure is over the first fin** and **the second gate structure is over the second fin**, as shown in the composite figure above. For instance, based on the teachings of Xie, gate structures are formed onto a structure based on Akarvardar's FIG. 9. *See* SAMSUNG-1010 (Akarvardar), 7:65-8:2 ("the first group of fins 104 may be part of a subsequently formed p-FET device and the second group of fins 204 may be part of a subsequently formed n-FET device", 8:19-22. In this Akarvardar-based structure, the fins are exposed because a previously-deposited protective layer has been removed: "the protective material 306 may be removed selective to the first and second group of fins 104, 204," and "may be conducted in a way such that the integrity of the first and second group of fins 104, 204 may not be compromised."

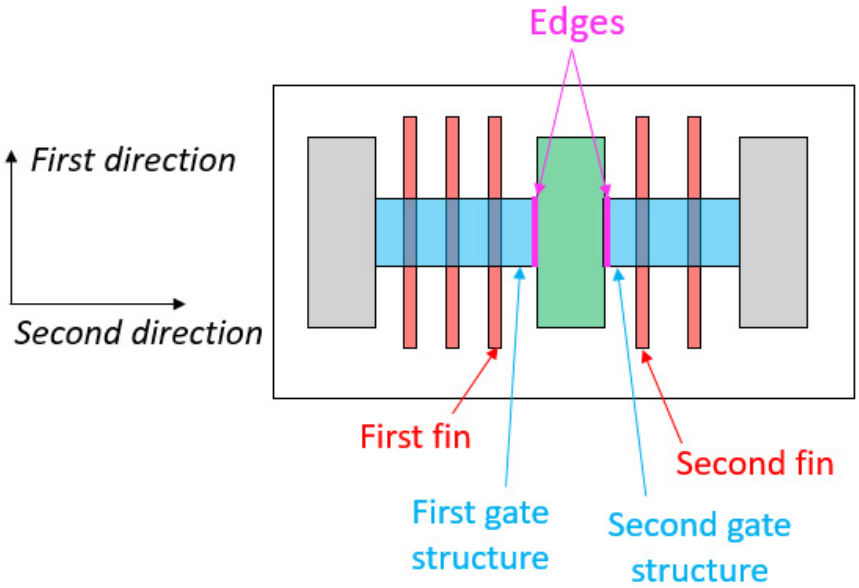
SAMSUNG-1010 (Akarvardar), 7:20-27, FIGS. 8-9. The gate structures are deposited onto these exposed fins and thus are **over** the respective fins, *e.g.*, consistent with the teachings of Xie. *See* SAMSUNG-1004 (Xie), [0017] ("first and second spaced-apart active regions formed in a semiconductor substrate, wherein ***each of the active regions includes at least one fin***, [and] first and second spaced-apart ***gate structures positioned above said first and second active regions***."), [0016] ("forming a stack of material layers to form ***a plurality of gate structures above a plurality of spaced-apart active regions*** defined in a semiconductor substrate, wherein ***each of the active regions have at least one fin*** formed thereabove"), [0040] ("the stack of materials 140S that will comprise the gate structure 140 (be it a final gate structure or a sacrificial gate structure) are blanket-deposited across all of the active regions"), [0015], [0018], [0041], FIG. 2I, FIGS. 2K-2O; claims 9, 11, 16.

159. Moreover, in the Akarvardar-Xie combination structure, **the second gate structure is discontinuous with the first gate structure**, as illustrated in the composite figures, reproduced again below. As shown, and consistent with the teachings of Xie, the first and second gate structures (blue) are **discontinuous** at least because they are separated by a gate edge isolation structure based on a modified version Akarvardar's second isolation region 504 (which I have highlighted in green and which I discuss in [26f], below). *See* SAMSUNG-1004

(Xie), [0017] ("first and second ***spaced-apart gate structures*** …, and a gate separation structure positioned between the first and second spaced-apart gate structures"), [0031]-[0032] ("a transverse 'cut' 115 of the gate stack material layer(s) is first performed to define the ends 110X of what will become the sacrificial gate structures 107" (in a replacement gate process; or final gate structures in a gate-first process), and "a gate separation structure 114 [is] formed in the opening"), [0040] ("The formation of the trenches 112 defines what will become the end surfaces 110X of the gate structures 140. … [a] gate separation structure [is] formed in the spaced apart trenches"), [0015]-[0016], [0018], [0041], FIG. 2I, FIGS. 2K-2O, claims 1, 9, 11, 16.



Akarvardar-Xie cross-sectional composite figure



Akarvardar-Xie top-view composite figure

160. As shown in the composite figures above, the discontinuity between the first and second gate structures is **along the second direction**: the discontinuity is reached ***as one moves in the second direction*** from one gate structure to the other (*e.g.*, left to right in the cross-sectional and top-view composite figures). *See* SAMSUNG-1010 (Akarvardar), FIG. 9; SAMSUNG-1004 (Xie), FIG. 2I.

161. The composite figures also illustrate that **the second gate structure has an edge** (outlined in pink) **that faces an edge of the first gate structure** (also outlined in pink). For instance, the edge (pink) of the second gate structure (blue) that contacts the gate edge isolation structure (green) faces the edge (pink) of the first gate structure (blue) that also contacts the gate edge isolation structure (green). This arrangement, too, is consistent with the teachings of Xie. For instance, Xie explains that "each of the gate structures has an end surface" (*e.g.*, **an edge**), where "first and second opposing surfaces of the gate separation structure" "abut the end surfaces of first and second spaced-apart gate structures, respectively." SAMSUNG-1004 (Xie), [0016]. In the combination, these gate structure end surfaces abutting the gate separation structure (*e.g.*, the structure based on Akarvardar's second isolation region) disposed therebetween are edges that face one another. *See* [0032] (in FIG. 2D, "***the ends 110X*** of what will become the sacrificial gate structures 107 abut the horizontal portions 114H of the gate separation structure 114"), [0041] ("the formation of the continuous trench 112

defines what will become ***the end surfaces 110X of the gate structure***"), [0035], [0040], FIG. 2I, FIGS. 2C-2E, FIGS. 2K-2O, claims 1, 11, and 16.

162. The edges (*e.g.*, end surfaces) of the gate structures face one another **along the second direction**: from the edge of the second gate structure, the edge of the first gate structure is reached ***as one moves in the second direction*** (*e.g.*, left to right in the cross-sectional and top-view composite figures).

The Akarvardar-Xie gate structures each includes a gate dielectric layer and a gate electrode

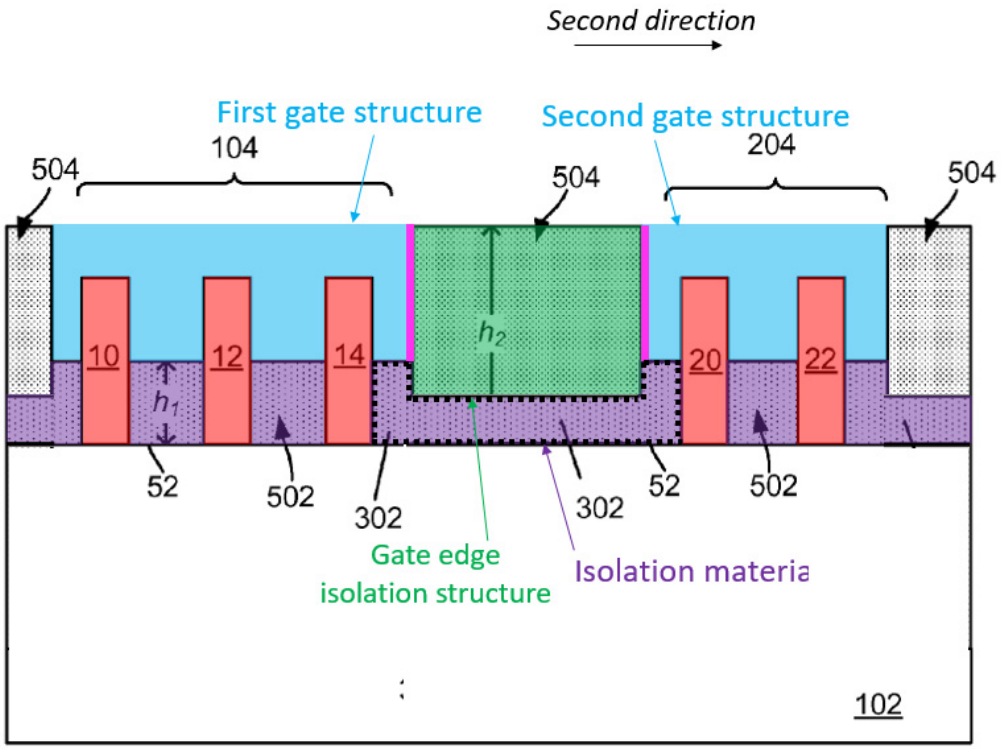
163. In the Akarvardar-Xie combination, Xie describes that its gate structures include "a high-k (k value greater than 10) gate insulation layer," "one or more metal layers … (e.g., layers of titanium nitride or TiAlC)," and "a bulk conductive metal layer … such as tungsten or aluminum." *Id.*, [0038]; *see* [0030]. As I discussed previously, a POSITA would have understood or found obvious to implement the "gate insulation layer" and "bulk conductive metal layer" (*id.*, [0038]) of Xie's gate structures as a gate dielectric layer and a gate electrode, respectively, such that the gate structures each includes **a gate dielectric layer** and **a gate electrode**. *See* SAMSUNG-1005 (Tseng), 5:5-46 ("The gate electrode layer 214 and the gate dielectric layer 212 form a gate stack 210"), 8:67-9:4 ("the gate-last process comprises … fill[ing] the trench with a gate dielectric layer and a conductive gate electrode layer"), FIG. 5A; SAMSUNG-1025 (Ching), 4:39-5:3 ("[t]he resulting remaining portions of the conductive material and gate dielectric

layer 50 thus form the replacement gate, which includes gate electrode 52 and gate dielectric 50"), FIG. 9A; SAMSUNG-1006 (Anderson), [0029] ("The gate stack 20 can be, for example, a gate dielectric and a gate electrode material"); SAMSUNG-1011, 3:59-4:10 ("The gate structure 110 includes a gate dielectric layer and a gate electrode"); SAMSUNG-1012 (Bohr), 4:46-54 ("The gate electrode … is a portion of a gate electrode stack which further includes a gate dielectric layer"); SAMSUNG-1013 (Chuang), 3:45-46 ("Gate electrode strip 32 and gate dielectric 145 form the gate stack of FinFET 100"); SAMSUNG-1014 (Kuo), 7:8-22 ("a gate dielectric 230 and a gate structure 232 are formed over the second insulation layer 228"); SAMSUNG-1015 (Shieh), [0041] ("a substrate 1 with fins 4, shallow trench isolations (STIs) 6, a gate dielectric 9, and a gate electrode layer 8 formed thereon"), [0046]-[0047].

[26f] a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and

164. The Akarvardar-Xie combination renders obvious [26f]. For instance, the Akarvardar-Xie combination structure includes **a gate edge isolation structure**, highlighted in green in the composite figure below, *e.g.*, based on Akarvardar's ***second isolation region 504*** modified based on the teachings of Xie. *See* SAMSUNG-1010 (Akarvardar), 6:39-41, 6:64-65, 7:8-10, 7:64-65, FIG. 9. For instance, as I have discussed previously, in the Akarvardar-Xie combination,

Akarvardar's second isolation region 504 is modified such that it is disposed directly on the first dielectric layer 302 (*e.g.*, the isolation material, highlighted purple). *See* SAMSUNG-1004 (Xie), [0031]-[0032], [0039]-[0041], FIGS. 2C-2I.



Akarvardar-Xie cross-sectional composite figure

165. In the Akarvardar-Xie combination, Akarvardar's modified second isolation region 504 is **a gate edge isolation structure**: it is a self-aligned structure that is disposed between the edges of the gate structures (discussed below) and isolates those gate structures from one another (*e.g.*, physically and electrically).

166. Notably, Akarvardar's modified second isolation region is a ***self-aligned*** structure: "the second isolation region 508 may be formed self-aligned to

the first group of fins 104 and the second group of fins 204." SAMSUNG-1010 (Akarvardar), 7:57-59; *see* 1:6-9 (bulk fin field effect transistor (FinFET) devices including self-aligned isolation regions"), 8:25-28 ("since the second isolation region is self-aligned with respect to the groups of fins, the use of additional masks to define the isolation regions may not be required"), 1:64-66, 3:51-58, 8:9-11, claim 2.

167. Moreover, Akarvardar's modified second isolation region ***physically isolates*** the first and second gate structures in that it separates the two gate structures such that the gate structures are not in physical contact. *See* SAMSUNG-1010 (Akarvardar), 8:14-16 ("The second isolation region may be located ***between*** two adjacent groups of fins"), 6:59-61 ("The extended recess 44 may subsequently be used to form a second isolation region between the first group of fins 104 and the second group of fins 204"), 6:18-20, claims 1 and 5, FIGS. 8-9.

168. Akarvardar's modified second isolation region also ***electrically isolates*** the first and second gate structures. Akarvardar describes that "the second isolation region 504 may ***electrically separate*** the first group of fins 104 from the second group of fins 204." SAMSUNG-1010 (Akarvardar), 7:64-67. More specifically, Akarvardar describes that when the groups of fins are part of subsequently formed FET devices, such "***devices may be electrically separated*** by the second isolation region 504." *Id.*, 7:67-8:4. In the combination, when gate

structures are disposed over the fins to form FinFET devices (*see* [26d]-[26e]), these devices (*e.g.*, devices including the first and second gate structures) are thus electrically separated by Akarvardar's modified second isolation region.

169. In the combination, **the gate edge isolation structure** (*e.g.*, Akarvardar's modified second isolation region) is b**etween and in contact with the edge of the first gate structure and the edge of the second gate structure**. The composite figures above illustrate this positioning, with the edges of the first and second gate structures outlined in pink.

170. Specifically, in the combination, the gate edge isolation structure is **between** the first and second gate structures, as illustrated in the composite figures. For instance, based on the teachings of Xie, Akarvardar's modified second isolation region is "***positioned between the first and second spaced-apart gate structures***." SAMSUNG-1004 (Xie), [0017]; *see* [0031]-[0032], [0040], [0015]-[0016], [0018], [0041], FIG. 2I, FIGS. 2K-2O, claims 1, 9, 11, 16; SAMSUNG-1010 (Akarvardar), FIG. 9. This positioning of the gate edge isolation structure between the first and second gate structures enables Akarvardar's modified second isolation region to fulfill its functionality: "p-FET and n-FET devices" formed over the first and second groups of fins "may be electrically separated by the second isolation region 504." SAMSUNG-1010 (Akarvardar), 7:66-8:4.

171. Additionally, in the combination, the gate edge isolation structure is **in contact with** the edges of the gate structures, as made apparent by the fabrication process for the combination structure. For instance, Akarvardar describes that to form the second isolation region, "a second dielectric layer 308" is deposited into a recess "between the first group of fins 104 and the second group of fins 204." SAMSUNG-1010 (Akarvardar), 6:58-65; *see* FIGS. 6-8. A "protective material 306 [is] removed selective to … the first and second dielectric layers 302, 308," thus exposing the sidewalls of the second dielectric layer 308. *Id.*, 7:20-28; *see* FIG. 9. In the combination, this process exposes the sidewalls of Akarvardar's second isolation region, *e.g.*, the gate edge isolation structure. When the gate structures are then deposited on opposite sides of that gate edge isolation structure, the edges of the gate structures (outlined in pink in the composite figures above) are **in contact with** those exposed edges of the gate edge isolation structure.

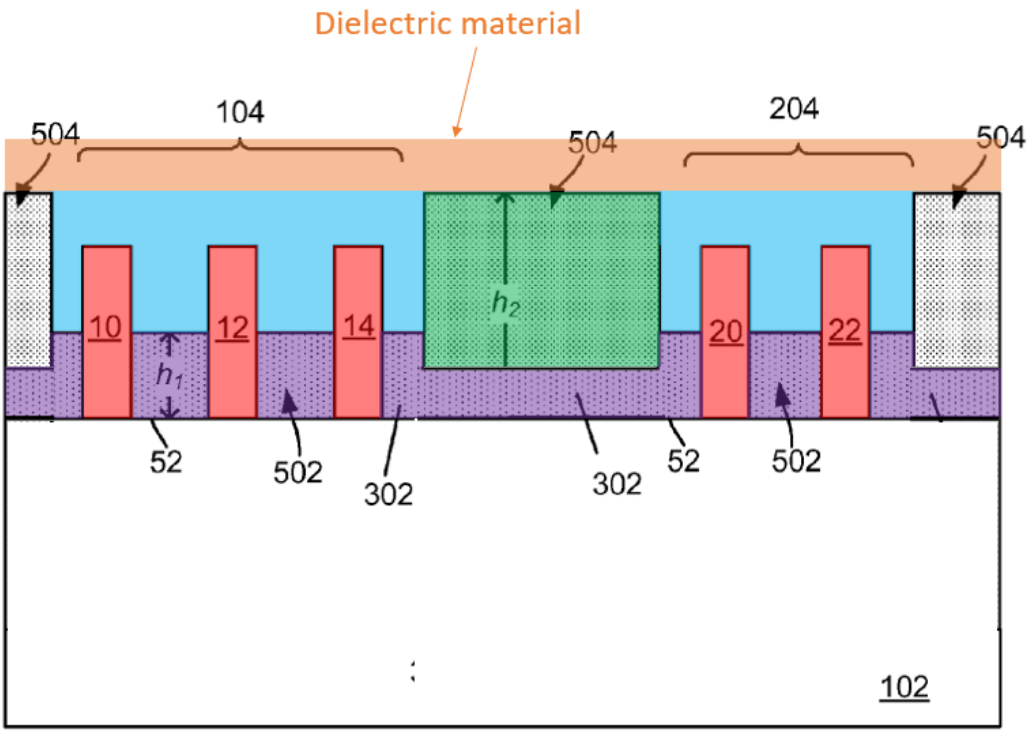
172. The gate edge isolation structure is between and in contact with the edges of the gate structures **along the second direction**: ***as one moves in the second direction*** (*e.g.*, from left to right in the cross-sectional view *supra*) starting from the edge of the first gate structure, one reaches first the gate edge isolation structure and then the edge of the second gate structure.

173. Furthermore, in the combination, the gate edge isolation structure is **over the isolation material**, as shown in the composite figures above. As I have

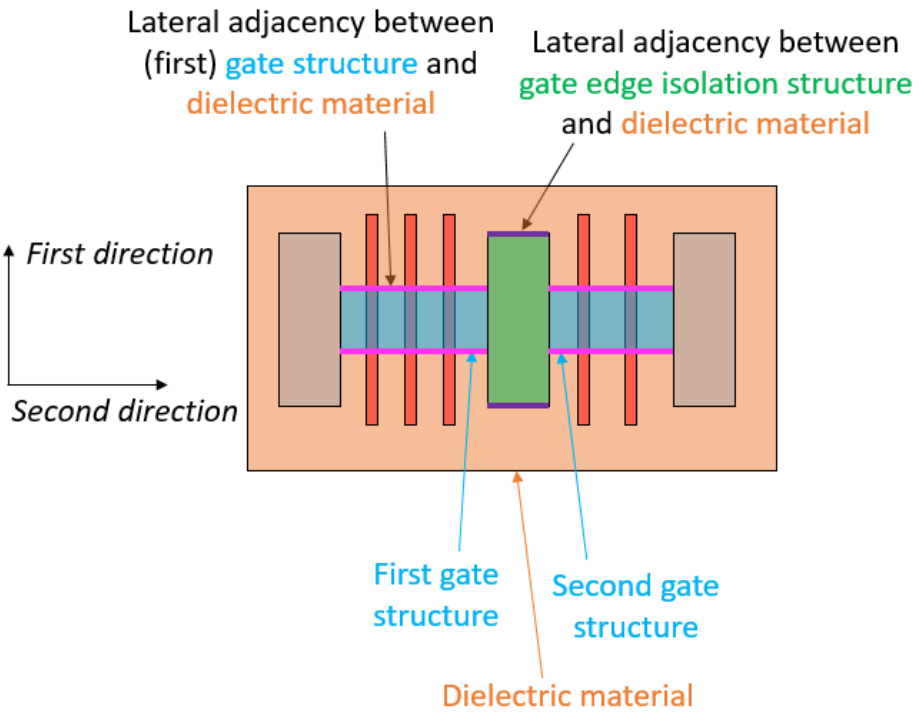
discussed previously , in the Akarvardar-Xie combination structure, Akarvardar's modified second isolation region 504 is disposed directly on the first dielectric layer 302 (*e.g.*, the isolation material, purple), consistent with Xie's teachings of a gate edge isolation structure over isolation material. *See* SAMSUNG-1004 (Xie), [0031]-[0032], [0039]-[0041] (describing forming a gate separation structure 114 in an opening 112 (*see* FIG. 2C), where insulating material 108 is disposed at the bottom of the opening), FIGS. 2C-2I.

[26g] a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.

174. The Akarvardar-Xie combination renders obvious [26g]. For instance, the Akarvardar-Xie combination structure includes **a dielectric material**, *e.g.*, based on Xie's insulating material 130, highlighted in orange in the composite figures below. *See* SAMSUNG-1004 (Xie), [0036] ("a layer of ***insulating material 130***, *e.g.*, silicon dioxide, … blanket-deposited above the epi semiconductor material and … planarize[d]"), FIG. 2I. An insulating material such as silicon dioxide is a dielectric material. In the combination, the dielectric material (*e.g.*, Xie's insulating material) is deposited onto the gate structures and the modified second isolation region. When seen in top view, the dielectric material extends into the page next to the sidewalls of the gates and next to at least the end walls of the modified second isolation region 504.



Akarvardar-Xie cross-sectional composite figure



Akarvardar-Xie top-view composite figure

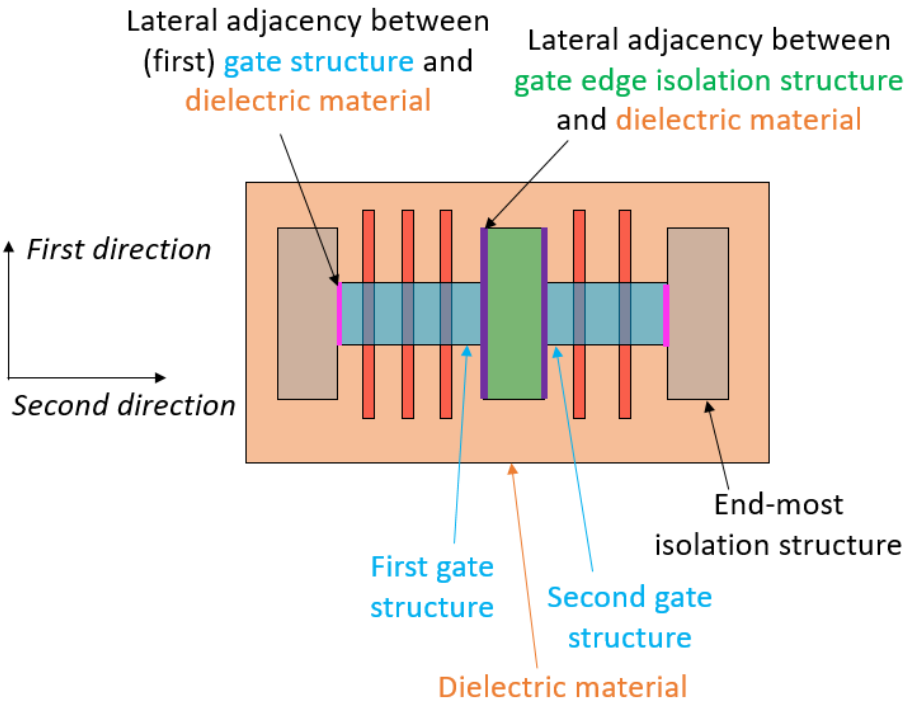
175. The sidewalls of the gate structures are outlined in pink in the top-view composite figure above. These sidewalls extend into the page of the top-view figure, and the dielectric material is disposed next to these sidewalls. That is the **dielectric material** (orange) **is laterally adjacent to the gate structures** at least at these pink-outlined sidewalls.

176. The dielectric material is laterally adjacent to the gate structures **along the first direction** at these pink-outlined sidewalls: viewing the structure starting from either of the gate structures and ***moving along the first direction*** (*e.g.*, from top to bottom in the top-view composite figure), one reaches the dielectric material.

177. The ends of the gate edge isolation structure are outlined in purple in the composite figure above. These ends extend into the page of the top-view figure, and the dielectric material is disposed next to these ends, *i.e.*, the **dielectric material** (orange) **is laterally adjacent to the gate edge isolation structure** at least at these purple-outlined ends.

178. The dielectric material is laterally adjacent to the gate edge isolation structure **along the first direction** at these purple-outlined ends: viewing the structure starting from the gate edge isolation structure and ***moving along the first direction*** (*e.g.*, from top to bottom in the top-view composite figure), one reaches the dielectric material.

179. Moreover, alternatively or additionally, the dielectric material of the combination (*e.g.*, Xie's insulating material) also is laterally adjacent to the gate structure and gate edge isolation at the pink-outlined edges of the gate structures in the alternative top-view composite figure that I have reproduced below. For instance, viewing the structure starting from *e.g.*, the second gate structure and moving along the second direction (left-to-right in the top-view figure), one reaches the dielectric material, passing through the end-most isolation structure. To the extent this spatial relationship is considered to be laterally adjacent **along the first direction**, the dielectric material of the combination is laterally adjacent to the first and second gate structures along the first direction.



Akarvardar-Xie top-view composite figure (alternative)

180. Similarly, the dielectric material of the combination also is laterally adjacent to the gate edge isolation structure at the purple-outlined edges of the gate edge isolation structure. For instance, as illustrated *supra*, viewing the structure starting from the gate edge isolation structure and moving along the second direction, one reaches the dielectric material, *e.g.*, passing through the second gate structure and the end-most isolation structure. To the extent this spatial relationship is considered to be laterally adjacent **along the first direction**, the dielectric material of the combination is laterally adjacent to the gate edge isolation structure along the first direction.

181. In the Akarvardar-Xie combination, **the dielectric material is discrete from the gate edge isolation structure**, *e.g.*, Xie's insulating material 130 is discrete from Akarvardar's modified second isolation region 504. For instance, the two structures are discrete at least in that ***they are formed in two distinct processing steps***: the modified second isolation region is formed in a self-alignment process (*see* SAMSUNG-1010 (Akarvardar), 5:52-65, 7:8-11, 7:57-59) while the insulating material is deposited over the second isolation region (*see* SAMSUNG-1004 (Xie), [0031]-[0032], [0039]-[0041], FIGS. 2C-2I).

182. Alternatively or additionally, **the dielectric material is discrete from the gate edge isolation structure** at least in that ***they are formed of different materials***. The gate edge isolation structure (*e.g.*, Akarvardar's modified second isolation region) "may include oxides, nitrides, and oxynitrides of silicon," while the dielectric material (*e.g.*, Xie's insulating material) is "silicon dioxide." SAMSUNG-1010 (Akarvardar), 6:64-7:9; SAMSUNG-1004 (Xie), [0036].

(2) Claim 27

[27] The integrated circuit structure of claim 26, wherein the gate edge isolation structure comprises silicon and nitrogen.

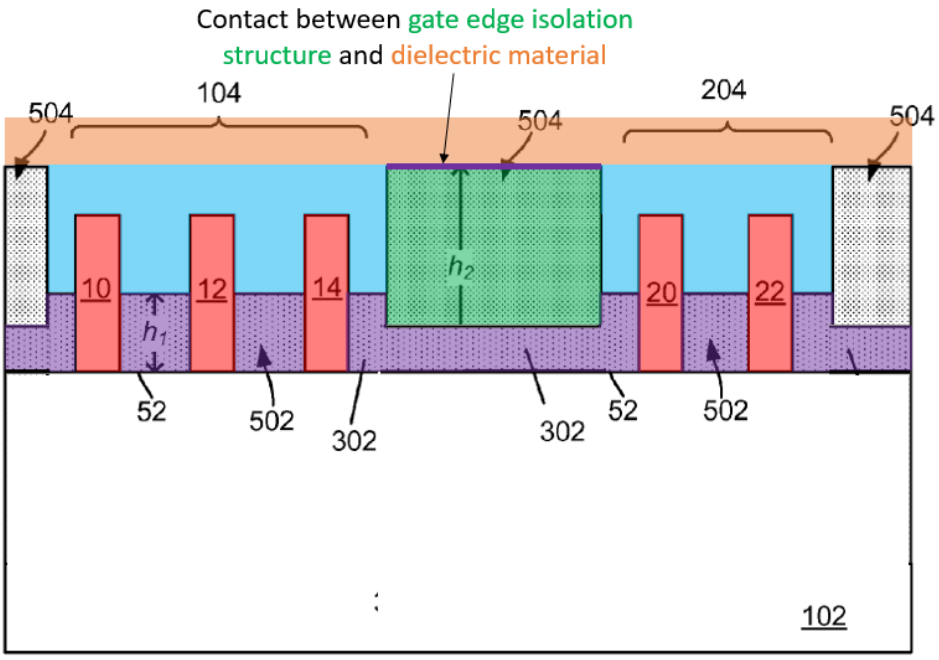
183. The Akarvardar-Xie combination renders obvious [27]. For instance, in the combination, Akarvardar describes that the gate edge isolation structure (*e.g.*, based on Akarvardar's second isolation region 504) includes **silicon and nitrogen**: "a second dielectric layer 208 … may include oxides, ***nitrides, and***

oxynitrides of silicon," where "[t]he second dielectric layer 308 may form a second isolation region 504." SAMSUNG-1010 (Akarvardar), 6:64-7:9.

(3) Claim 28

[28] The integrated circuit structure of claim 26, wherein the dielectric material is in contact with the gate edge isolation structure.

184. The Akarvardar-Xie combination renders [28] obvious. For instance, in the combination, the dielectric material (*e.g.*, Xie's insulating material) is "blanket-deposited" onto the gate structures and gate edge isolation structure (*e.g.*, based on Akarvardar's second isolation region 504). SAMSUNG-1004 (Xie), [0036]. Thus, **the dielectric material is in contact with the gate edge isolation structure** at least on the top surface of the gate edge isolation structure, outlined in purple in the composite figure *infra*.



Akarvardar-Xie cross-sectional composite figure

(4) Claim 29

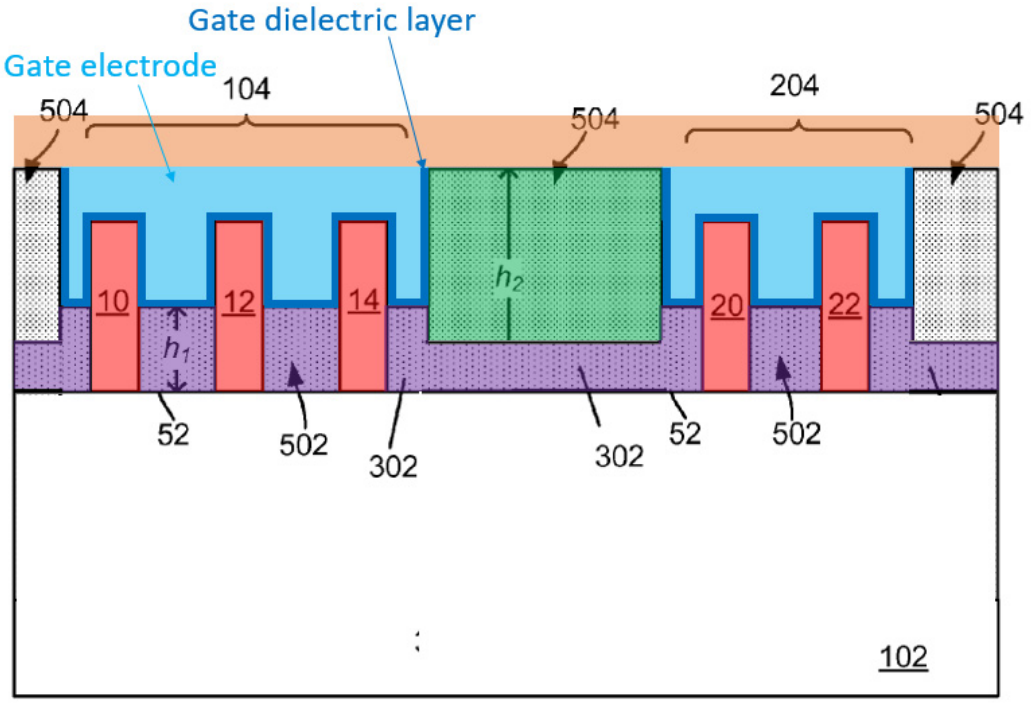
[29] The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

185. The Akarvardar-Xie combination renders obvious [29]. In the combination, the gate structures are deposited after formation of the gate edge isolation structure, and thus the gate material is in contact with the exposed sidewalls of the gate edge isolation structure. *See* SAMSUNG-1010 (Akarvardar), 7:65-8:2; SAMSUNG-1004 (Xie), [0038].

186. I note that the general process flow for forming a gate structure was well-known in the art as of the Critical Date. For instance, as I discussed previously for Ground 1, a POSITA would have understood that formation of a

replacement gate involves first depositing the gate dielectric layer in the space over the fins and bounded by the gate edge isolation structure, followed by deposition of the gate electrode onto the gate dielectric layer. *See* SAMSUNG-1025 (Ching), 4:39-5:56, FIG. 8A; SAMSUNG-1005 (Tseng), 8:62-9:4; SAMSUNG-1015 (Shieh), [0045]-[0047]; SAMSUNG-1012 (Bohr), 11:4-14; SAMSUNG-1014 (Kuo), 7:8-42; .

187. As illustrated in the composite figure below, when the gate dielectric layer (dark blue) is deposited into a space left by removal of a sacrificial gate material, the gate dielectric layer is coated onto exposed surfaces, including onto the exposed edges of the gate edge isolation structure (highlighted in green). *See* SAMSUNG-1025 (Ching), 4:39-5:56; SAMSUNG-1040 (Kelly), 6:33-38, FIGS. 7A-7B; SAMSUNG-1036 (Liaw), [0023], FIG. 1F. Thus, **the gate edge isolation structure is in contact with the gate dielectric layer** of each gate structure, *e.g.*, at least because the gate dielectric layer of each of the first and second gate structures coats the respective edges of the gate separation structure.



Akarvardar-Xie cross-sectional composite figure

(5) Claim 31

[31] The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

188. The Akarvardar-Xie combination renders obvious [31]. For instance, it is my opinion that a POSITA would have understood or found obvious that Xie's gate structures each includes a gate dielectric layer (*e.g.*, **a high-k gate dielectric layer**) and a gate electrode (*e.g.*, a metal gate electrode). *See* SAMSUNG-1004 (Xie), [0038]; SAMSUNG-1005 (Tseng), 5:5-46; SAMSUNG-1025 (Ching), 4:39-5:3; SAMSUNG-1006 (Anderson), [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1014 (Kuo), 7:8-22; SAMSUNG-1015 (Shieh), [0047]. Specifically,

a POSITA would have understood or found obvious for Xie's "high-k … gate insulation layer" to be a gate dielectric layer that includes **a high-k dielectric material**. SAMSUNG-1004 (Xie), [0038].

C. [GROUND 3] – CLAIMS 26-29 AND 31 ARE OBVIOUS OVER AKARVARDAR, XIE, AND TSENG

189. Ground 3 is substantively identical to, and incorporates the analysis of, Ground 2 in all but the following respects. Ground 2 demonstrated that the Element [26d] and [26e] features that each gate structure includes a respective gate dielectric layer and gate electrode are obvious in view of Akarvardar and Xie. In Ground 2, I rely on the even more explicit disclosure of Tseng to reach these features, as well as to reach dependent claims 29 and 31. I note that my reliance on Tseng in Ground 3 does not affect the mapping of the Akarvardar-Xie combination to other claim elements, and so for brevity, I have addressed only the pertinent portions of Elements [26d]-[26e] and claims 29-31 are addressed in Ground 3. The unaddressed claim 26 elements, and dependent claims 27-28, are obvious over the Akarvardar-Xie-Tseng combination at least as I discussed above for Ground 2.

1. Tseng describes FinFET gate structures having a gate dielectric layer and a gate electrode

190. Tseng, in the field of FinFET devices, describes a FinFET having a "gate stack 210" including a "gate electrode layer 214 and [a] gate dielectric layer 212." SAMSUNG-1005 (Tseng), 5:5-10; *see* FIG. 9A. The gate dielectric layer

can be a "high dielectric constant (high-k) dielectric," and the gate electrode can include a "N-work function metal" or a "P-work function metal." SAMSUNG-1005 (Tseng), 5:12-46. Tseng's gate stack can be "fabricated using a gate-first process" or "using a gate-last process performed by first forming a dummy gate stack." *Id.*, 8:59-62.

2. The Akarvardar-Xie-Tseng combination

191. In the Akarvardar-Xie-Tseng combination, the gate structures (*e.g.*, Xie's replacement gate structures; *see* SAMSUNG-1004 (Xie), [0030], [0038]) include gate dielectric layers and gate electrodes based on the teachings of Tseng. *See* SAMSUNG-1005 (Tseng), 5:5-46. For instance, in the combination, Xie's "high-k … gate insulation layer" is implemented as a high-k gate dielectric layer, and Xie's "bulk conductive metal layer" is implemented as a metal gate electrode layer, based on the teachings of Tseng. SAMSUNG-1004 (Xie), [0038]; *see* Tseng, 5:5-46, 8:67-9:4, FIG. 5A.

192. A POSITA would have been motivated to pursue this implementation, and would have expected success in doing so, for at least similar reasons as those I discussed for Ground 2 . Moreover, a POSITA would have expected success specifically in the Akarvardar-Xie-Tseng combination given that Akarvardar, Xie, and Tseng all relate to FinFET fabrication processes. *See* SAMSUNG-1010

(Akarvardar), 7:11-14, 8:1-8, 8:23-28; SAMSUNG-1004 (Xie), [0030]; SAMSUNG-1005 (Tseng), 8:59-62.

3. Analysis

(1) Claim 26

[26d] a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;

[26e] a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;

193. The Akarvardar-Xie-Tseng combination renders obvious first and second gate structures having the recited features, *e.g.*, in view of Xie's final gate structures. *See* [26d]-[26e] of Ground 2.

194. In the Akarvardar-Xie-Tseng combination, the first and second gate structures (*e.g.*, replacement gate structures or gate-first gate structures) include respective **gate dielectric layers** and respective **gate electrodes**, *e.g.*, based on Tseng's description of gate structures with gate dielectric layers and gate electrodes. *See* SAMSUNG-1005 (Tseng), 5:5-46, 3:4-12, FIGS. 2, 5A.

(2) Claim 29

[29] The integrated circuit structure of claim 26, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

195. When the Akarvardar-Xie-Tseng gate structures are fabricated by a replacement gate process (*see* SAMSUNG-1004 (Xie), [0030]), **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures**. *See* [29] of Ground 1.

(3) Claim 31

[31] The integrated circuit structure of claim 29, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

196. The gate dielectric layers of the Akarvardar-Xie-Tseng gate structures include **a high-k dielectric material**. For instance, in the combination, Xie's "high-k … gate insulation layer" is implemented as a **gate dielectric layer** that includes **a high-k dielectric material** based on the teachings of Tseng. SAMSUNG-1004 (Xie), [0038]; *see* SAMSUNG-1005 (Tseng), 5:5-46.

VI. LEGAL PRINCIPLES

A. Anticipation

197. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates.

198. I have been informed by counsel that a claim is invalid under 35 U.S.C. § 102(a)(1) if the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(a)(2) if the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

B. Obviousness

199. I have been informed that a patent claim is invalid as "obvious" under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a POSITA, taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called "secondary considerations" of non-obviousness, which include: (i) "long felt need" for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) "copying" of the claimed invention by others.

200. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a

single prior art reference or multiple prior art references, there must be a reason to modify the single prior art reference, or combine two or more references, in order to achieve the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves, the knowledge or "common sense" of one skilled in the art, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

VII. ADDITIONAL REMARKS

201. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

202. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code.

Dated: 1/19/2023 By: _____

APPENDIX A

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PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 12 years of experience serving as expert consultant.
    - Named inventor on 99 US patents.
- Consultant and expert witness for past 15 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

KEY EXPERT WORK EXPERIENCE:

Case:	**Netlist, Inc. vs. *Samsung Electronics Co. Ltd. et al.,***
Jurisdiction:	Civil Action No. 2:21-cv-00463 Eastern District of Texas
Work Product:	Expert relating to memory modules.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Tony Nguyen)
Date:	8/22 – Current

Case:	**Vervain, LLC vs. *Micron Technology &* related IPR Petition**
Jurisdiction:	Action No. 6:21-cv-00487-ADA Western District of Texas
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents, all 4 petitions instituted, and deposed on both initial declaration and reply declaration.
Counsel:	Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared Bobrow)
Date:	8/21 – Current

Case:	**Monterey Research vs. *Qualcomm* PTAB Matter**
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Jones Day (Contact: David Cochran)
Date:	12/21 – Current

Case:	***Semiconductor Energy Laboratory Co.,* OLED Patent Matters**
Jurisdiction:	Action No. 8:21-cv-00554-JAK-ADS Central District of California
Work Product:	Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Bryan Basso)
Date:	9/21 – 4/22

Case:	***Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Erise IP (Contact: Paul Hart)
Date:	8/21 – 9/21

Case:	***Texas Instruments IPR Petition***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Fish & Richardson (Contact: Josh Griswold)
Date:	9/20 – 4/21

Case:	***Micron Technology* vs. UMC/JinHua**
Jurisdiction:	Case No. 4:17-CV-06932-MMC United States District Court for the Northern District of California
Work Product:	Testifying expert, trade secret documents review, and declaration submission.
Nature of Case:	Trade secret contention of Micron confidential documents.
Counsel:	Retained by Jones Day (Contact: Randy Kay)
Date:	3/17 – Current

Case:	***SK Hynix* vs. BitMicro**
Jurisdiction:	Investigation No. 337-TA-1097 United States International Trade Commission
Work Product:	Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, deposition taken, issued witness statement.
Nature of Case:	ITC infringement case concerning module stacking of SDRAM.
Counsel:	Retained by Fish Richardson (Contact: Joseph Colaianni)
Date:	11/18 – 4/19

Case:	***Rohm Company IPR Petition***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Fish & Richardson (Contact: Matt Colvin)
Date:	4/18 – 8/18

Case:	***Apple Inc.,* vs. Qualcomm Incorporated**
Jurisdiction:	Case No. 3:17-CV-02402 United States District Court for the Southern District of California
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, 2 depositions taken.
Counsel:	Fish & Richardson (Contact: Tony Nguyen)
Date:	1/18 – 5/19

Case:	***Macronix* vs. Toshiba**
Jurisdiction:	Investigation No. 337-TA-1046 United States International Trade Commission
Work Product:	Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, deposition taken for 2 patents, issued witness statement and rebuttal witness statement, testified in ITC court on both infringement and invalidity.
Nature of Case:	ITC infringement case concerning advanced NAND Flash memory.
Counsel:	Retained by Fish Richardson (Contact: David Barken)
Date:	4/17 – 10/18

Case:	***Novatek Microelecronics Corp. IPR Petition***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)
Date:	2/17 – 4/17

Case:	***Taiwan Semiconductor Manufacturing Company IPR Petition***
Work Product:	Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel:	Retained by Fish & Richardson (Contact: John Goetz)
Date:	7/15 – 4/17

Case:	**Triune Systems, LLC vs. *Wayne Chen, et al.,***
Jurisdiction:	Case No. 296-03209-2013, District Court of Collin County, TX
Work Product:	Testifying expert, database viewing, expert report, video-taped testimony
Nature of Case:	Defending against trade secret contention.
Counsel:	Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date:	5/15 – 9/15

Case:	***Macronix* vs. Spansion**
Jurisdiction:	Investigation No. 337-TA-922 United States International Trade Commission
Work Product:	Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case:	ITC infringement case concerning Flash memory cell
Counsel:	Retained by Fish Richardson (Contact: David Barken)
Date:	9/14 – 1/15

Case:	***Macronix* vs. Spansion**
Jurisdiction:	Investigation No. 337-TA-909 United States International Trade Commission
Work Product:	Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case:	ITC infringement case concerning Flash memory cell
Counsel:	Retained by Winston & Strawn (Contact Michael Murray)
Date:	5/14 – 1/15

Case:	***Keranos, LLC* v. Analog Devices et. al.**
Jurisdiction:	Civil Case No. 2:10-CV-00207 United States District Court for the Eastern District of Texas
Work Product:	Claim Chart Generation and Claim Construction
Nature of Case:	Patent infringement case concerning split gate Flash memory cell
Counsel:	Retained by Agility IP (Contact Michelle Breit)
Date:	2/09 – 2/14

Case:	**Silicon Storage Technology, Inc. v. *Xicor, LLC***
Jurisdiction:	Civil Case No. CV 10-01515 United States District Court for the Northern District of California
Work Product:	Expert report and declarations
Nature of Case:	Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel:	Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date:	6/11 – 10/11

Case:	***Fast Memory Erase, LLC* v. Spansion et.al.**
Jurisdiction:	Civil Case No. 3:10CV-481 United States District Court for the Northern District of Texas
Work Product:	Declarations
Nature of Case:	Defending Motion for Attorney Fees.
Counsel:	Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date:	2/10 – 6/10

Case:	***Fast Memory Erase, LLC* v. Spansion et.al.**
Jurisdiction:	Civil Case No. 3-08cv0977M United States District Court for the Northern District of Texas
Work Product:	Testifying expert: issuing expert report, declarations, and deposition taken.
Nature of Case:	Patent infringement case concerning minimizing source current during erase of Flash memory cell.
Counsel:	Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date:	2/09 – 5/10

EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 6 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35μm and 0.18μm CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**

Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**

Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00 **Programmable Silicon Solutions, Sunnyvale, California**
Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98 **AMIC Technology, Santa Clara, California**
Director of Flash Technology. Responsible for developing 0.35μm ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97 **Altera Corp., San Jose, California**
Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35μm generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96 **Information Storage Devices, San Jose, California**
Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95 **Advanced Micro Devices, Sunnyvale, California**
Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5μm and 0.35μm flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92 **Texas Instruments, Dallas, Texas**

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983
AEA Faculty Development Fellowship, 1983-1985
AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K-L. Chen and H. Tigelaar), issued April 21, 1992.

2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.

3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.

4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.

5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.

6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.

7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.

8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.

9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994

10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.

11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.

12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.

13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.

14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.

15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.

16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.

17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.

18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.

19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.

20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.

21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.

22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.

23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.

24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.

25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997

26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.

27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.

28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.

29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998

30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.

31. U.S. Patent 5,814,854, "Highly scalable FLASH EEPROM cell," Issued September 29, 1998.

32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.

33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.

34. U.S. Patent 5,930,174, "Circuit and Method for Erasing Flash Memory Array," Issued July 27, 1999.

35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.

36. U.S. Patent 5,995,418, "Circuit and Method for Erasing Flash Memory Array," Issued November 30, 1999.

37. U.S. Patent 6,026,017, "Compact nonvolatile memory," Issued February 15, 2000.

38. U.S. Patent 6,027,974, "Nonvolatile memory," Issued February 22, 2000.

39. U.S. Patent 6,088,263, "Non-volatile memory using substrate electrons," Issued July 11, 2000.

40. U.S. Patent 6,091,636, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued July 18, 2000.

41. U.S. Patent 6,127,225, "Memory cell having implanted region formed between select and sense transistors," Issued October 3, 2000.

42. U.S. Patent 6,159,800, "Method of forming memory cell," Issued December 12, 2000.

43. U.S. Patent 6,188,604, "Flash memory cell & array with improved pre-program and erase characteristics," Issued February 13, 2001.

44. U.S. Patent 6,185,133, "Flash EPROM using junction hot hole injection for erase," Issued February 6, 2001.

45. U.S. Patent 6,252,799, "Device with embedded Flash and EERPOM memories," Issued June 26, 2001.

46. U.S. Patent 6,326,265, "Device with Embedded Flash and EPROM Memories," Issued December 4, 2001.

47. U.S. Patent 6,417,550, "High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage," Issued July 9, 2002.

48. U.S. Patent 6,479,862, "Charge trapping device and method for implementing a transistor having a negative differential resistance mode," Issued November 12, 2002.

49. U.S. Patent 6,512,274, "CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same," Issued January 28, 2003.

50. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device," Issued July 22, 2003.

51. U.S. Patent 6,624,026, "Nonvolatile Memory," Issued September 23, 2003.

52. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process," Issued January 20, 2004.

53. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same," Issued February 3, 2004.

54. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR) characteristic," Issued February 17, 2004.

55. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold," Issued March 2, 2004.

56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.

57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.

58. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same," Issued November 29, 2005.

59. U.S. Patent 6,972,234, "High Voltage MOS Devices with High Gated-Diode Breakdown Voltage and Punch-through Voltage," Issued December 6, 2005.

60. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same," Issued December 6, 2005.

61. U.S. Patent 7,067,873, "Charge Trapping Device," Issued June 27, 2006.

62. U.S. Patent 7,091,077, "Method of directionally trimming polysilicon width," Issued August 15, 2006.

63. U.S. Patent 7,109,078, "CMOS compatible process for making a charge trapping device," Issued September 19, 2006.

64. U.S. Patent 7,301,194, "Shrinkable and highly coupled double poly EEPROM with Inverter," Issued November 27, 2007.

65. U.S. Patent 7,436,710, "EEPROM memory device with cell having NMOS in a P pocket as a control gate, PMOS program/erase transistor, and PMOS access transistor in a common well," Issued October 14, 2008.

66. U.S. Patent 7,535,758, "One or Multiple-Times Programming Device," Issued May 19, 2009.

67. U.S. Patent 7,782,668, "Integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 24, 2010.

68. U.S. Patent 7,787,295, "Integrated circuit embedded with Non-volatile Multiple-Time Programmable memory having variable coupling," Issued August 31, 2010.

69. U.S. Patent 7,787,304, "Method of making integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 31, 2010

70. U.S. Patent 7,787,309, "Method of operating integrated circuit embedded with Non-volatile One-Time Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.

71. U.S. Patent 7,791,955, "Method of erasing a block of memory cells," Issued September 7, 2010.

72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010

73. U.S. Patent 7,835,186, "Method of programming a selected memory cell," Issued November 16, 2010.

74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010

75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011

76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011

77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011

78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012

79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012

80. U.S. Patent 8,300,470, "Two Terminal Programmable Hot Channel Electron Non-Volatile Memory," Issued October 30, 2012

81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012

82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.

83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.

84. U.S. Patent 8,582,342, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued November 12, 2013.

85. U.S. Patent 8,599,612, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Related Application data," Issued December 3, 2013.

86. U.S. Patent 8,705,263, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued April 22, 2014.

87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.

88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.

89. U.S. Patent 9,224,739, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued December 29, 2015.

90. U.S. Patent 9,305,931, "Zero Cost NVM Cell Using High Voltage Devices in Analog Process," Issued April 5, 2016.

91. U.S. Patent 9,324,438, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued April 26, 2016.

92. U.S. Patent 9,558,813, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued January 31, 2017.

93. U.S. Patent 9,570,161, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.

94. U.S. Patent 9,570,175, "Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.

95. U.S. Patent 10,061,738, "Ephemeral Peripheral Device," Issued August 28, 2018.

96. U.S. Patent 10,115,467, "One time Accessible (OTA) Non-Volatile Memory," Issued October 30, 2018.

97. U.S. Patent 10,198,889, "Automatic Valid Vote Count Storage Using Secure Embedded Non-Volatile Memory," Issued February 5, 2019

98. U.S. Patent 10,559,700, "Zero Cost ANVM Cell Using High Voltage Devices in Analog Process," Issued February 11, 2020.

99. U.S. Patent 10,629,607, "Semiconductor CMOS Non-Volatile Memory Device," Issued April 21, 2020

(additional patent applications pending)

PUBLICATIONS

1. S.D. Leeke, D. K. Y. Liu and J. P. McVittie, "Plasma mode trench etching with direct hydrocarbon injection," *Materials Research Society Symposium Proceedings*, Vol. 68, pp. 21-27, 1986.
2. D. K. Y. Liu and J. D. Plummer, "A novel trench-injector power device with low ON-resistance and high switching speed," *IEEE Electron Device Letters*, Vol. 9, No. 7, pp. 321-323, 1988.
3. D. M. Boisvert, D. K. Y. Liu and J. D. Plummer, "Circuit approaches to increasing IGBT switching speed," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1276-1279, 1988.
4. D. K. Y. Liu and J. D. Plummer, "Device physics and optimization of conductivity-modulated power MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, pp. 2457-2458, 1988.
5. D. K. Y. Liu, K.-L. Chen, H. Tigelaar, J. Paterson and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 12, No. 4, pp. 151-153, 1991.
6. M. Wong, D. K. Y. Liu, M. M. Moslehi and D. W. Reed, "Preoxidation treatment using HCl/HF vapor," *IEEE Electron Device Letters*, Vol. 12, No. 8, pp. 425-426, 1991.
7. D. K. Y. Liu, C. Kaya, M. Wong, J. Paterson and P. Shah, "Optimization of a source-side injection FAMOS cell for flash EPROM applications," *International Electron Devices Meeting Technical Digest*, pp. 315-318, 1991.
8. K.-L. Chen, D. K. Y. Liu, G. Misium, W. M. Gosney, S.-J. Wang, J. Camp and H. Tigelaar, "A sublithographic antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 13, No. 1, pp. 53-55, 1992.
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