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Paper 8
Date: December 16, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORPORATION,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00994
Patent 8,301,833 B1

Before: LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Sandisk Corporation, Inc. ("Petitioner") filed a Petition, on June 20, 2014, requesting an *inter partes* review of claims 1–30 of US Patent No. 8,301,833 B1 (Ex. 1001, "the '833 patent"). Paper 1 ("Pet."). Netlist, Inc.

("Patent Owner") filed a Preliminary Response on October 2, 2014. Paper 7 ("Prelim. Resp.").

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Pursuant to 35 U.S.C. § 314, the Board does not find a reasonable likelihood that Petitioner would prevail with respect to at least one claim of the '833 patent and, thus, does not authorize an *inter partes* review to be instituted as to those claims.

A. Related Proceedings

Petitioner indicates that the '833 patent is involved in the following co-pending actions: *Netlist, Inc. v. Smart Modular Technologies, Inc*., U.S. District Court for the Northern District of California, Civil Action No. 3:13-CV-05889-YGR; *Diablo Technologies, Inc. v. Netlist, Inc.*, U.S. District Court for the Northern District of California, Civil Action No. 4:13-CV-03901-YGR; and *Smart Modular Technologies, Inc. v. Netlist, Inc.*, U.S. District Court for the Northern District of California, Civil Action No. 4:13-CV-03916-YGR.). Pet. 59.

B. The '833 Patent

The invention in the '833 patent relates to a specific configuration of hybrid memory systems that addresses non-volatile memory backup, while running the volatile memory subsystem at lower power, and therefore, at lower clock speeds. Ex. 1001, col. 16, ll. 29–34. Specifically, the alleged invention of the '833 patent includes circuitry for providing a regular high-

speed clock frequency (first clock frequency) during communications between the host and the volatile memory subsystem, and a slower clock frequency during communications between the volatile memory subsystem (using third clock frequency) and the non-volatile memory subsystem (using second clock frequency). *Id.* at col. 21, ll. 5–21. Further, the second and third clock frequencies may be substantially equal. *Id.* at col. 21, ll. 23–24.

C. Illustrative Claim

Of the challenged claims, 1 and 5 are independent claims. Claim 1 is illustrative of the claimed subject matter of the ’833 patent, and is reproduced below:

> 1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:
>
> operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;
>
> operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem; and
>
> operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

1. *Prior Art Relied Upon*

Petitioner relies upon the following prior art references:

Fukuzo ("Fukuzo," Ex. 1013)	US 2006/0294295 A1	June 24, 2005
Panabaker ("Panabaker," Ex. 1014)	US 7,716,411 B2	June 7, 2006
Li ("Li," Ex. 1015)	US 6,336,174 B1	August 9, 1999
Spiers ("Spiers," Ex. 1016)	US 2006/0080515 A1	October 12, 2004
Hansen ("Hansen," Ex. 1017)	US 2005/0132250 A1	December 16, 2003
Sun ("Sun," Ex. 1018)	US 7,102,391 B1	July 29, 2004
Komatsuzaki ("Komatsuzaki," Ex. 1019)	US 6,944,042 B2	December 31, 2002

2. *The Asserted Grounds*

Petitioner asserts that the challenged claims are unpatentable based on the following grounds:

Reference[s]	**Basis**	**Claims challenged**
Fukuzo	§ 102	1, 2, 6, 8, 11, 12, 15, 18, 22, 24, 27, and 28
Panabaker	§ 102	1–6, 8, 11–13, 15, 17–22, 24, and 27–29
Fukuzo and Li	§ 103	3 and 19
Fukuzo, Li, and Spiers	§ 103	3 and 19
Fukuzo and Hansen	§ 103	7 and 23
Fukuzo, Li, and Hansen	§ 103	7, 9, 10, 23, 25, and 26
Fukuzo and Sun	§ 103	14 and 30
Fukuzo, Li,	§ 103	14 and 30

Reference[s]	Basis	Claims challenged
and Sun		
Fukuzo and Komatsuzaki	§ 103	16
Fukuzo, Li, and Komatsuzaki	§ 103	16
Panabaker and Li	§ 103	1–6, 8, 11, 12, 15, 17–22, 24, 27, and 28
Panabaker and Spiers	§ 103	3 and 19
Panabaker, Li, and Spiers	§ 103	3 and 19
Panabaker and Hansen	§ 103	7, 9, 23, and 25
Panabaker, Li, and Hansen	§ 103	7, 9, 10, 23, 25, and 26
Panabaker and Fukuzo	§ 103	13 and 29
Panabaker, Li, and Fukuzo	§ 103	13 and 29
Panabaker and Sun	§ 103	14 and 30
Panabaker, Li, and Sun	§ 103	14 and 30
Panabaker and Komatsuzaki	§ 103	16
Panabaker, Li, and Komatsuzaki	§ 103	16

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner does not present any claim constructions, rather, Petitioner states that "each claim should be construed in accordance with its plain and ordinary meaning under the required broadest reasonable interpretation." Pet. 9–10. Patent Owner provides a construction for one term only—"clock frequency." Patent Owner argues "the claimed 'clock frequency' should be construed literally as <u>clock</u> frequency." Prelim Resp. 18. Because the claims refer specifically to "clock" frequency, on this record, and for purposes of this Decision, we determine that the broadest reasonable interpretation of "clock frequency" requires identification of a clock running at a particular frequency.

B. Claims 1, 2, 6, 8, 11, 12, 15, 18, 22, 24, 27, and 28—Anticipated by Fukuzo (Ex. 1013)

Petitioner argues that claims 1, 2, 6, 8, 11, 12, 15, 18, 22, 24, 27, and 28 are anticipated by Fukuzo under 35 U.S.C. § 102(a) and (e). Pet. 9–17. Fukuzo discloses an SDRAM memory chip device that comprises a non-

volatile memory controller operating a nonvolatile memory and a FIFO memory. Ex. 1013, Abstract, ¶ 27. Fukuzo's SDRAM memory chip device is used to store data to its internal SDRAM memory array (volatile memory) and to external FLASH (nonvolatile memory) using at least two additional pins as compared with conventional SDRAM standard. *Id.* Two further pins reflecting the flash memory status provide appropriate issuance of load or store signals by the host. *Id.* Fukuzo teaches using foreground and background operations such that read/write operations to volatile memory can occur simultaneously with read/write operations to non-volatile memory. *Id*

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Claim 15 recites "the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency." Figure 3 of Fukuzo is

reproduced below.

FIG 3

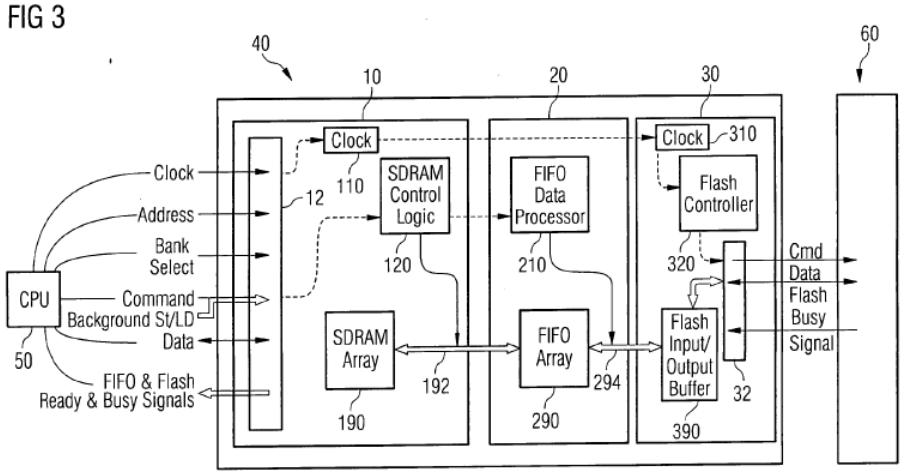

Figure 3, above, depicts a schematic block diagram of a memory chip device according to the invention of the Fukuzo device.

Petitioner asserts that Fukuzo's disclosure of SDRAM memory chip device 40 ("SDRAM Chip 40") is the claimed volatile memory subsystem and Fukuzo's disclosure of clock generator 110, which operates at 110 MHz and is valid for blocks 10 and 20 of the SDRAM chip 40, is the claimed first clock frequency. Pet. 14 (citing Ex. 1013 ¶¶ 84, 87–8). Further, Petitioner asserts that Fukuzo's disclosure of flash clock 310 which drives flash controller 320 and flash input/output buffer 390, which is described as operating at 20 MHz and is valid for block 30 of SDRAM chip 40, meets the limitation to a third clock frequency. Pet. 14 (citing Ex. 1013 ¶¶ 84, 87–88). We are not persuaded by Petitioner's argument or cited disclosure.

Petitioner reads the entire SDRAM chip 40 on the volatile memory subsystem. However, SDRAM chip 40 has at least two clocks running at different frequencies. Petitioner does not sufficiently explain how the chip reads on operating at a first frequency in one mode and a second frequency

in a second mode when the chip appears to be running both frequencies all the time or at least at the first frequency all the time. *See* Prelim. Resp. 21. It appears what Petitioner is actually doing is using blocks 10 and 20 to be the volatile memory subsystem at one time and block 30 to be the volatile memory subsystem at other times.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984). Nonetheless, Petitioner reads inconsistently the claim limitation on two distinct structures, SDRAM core section 10 and flash controller section 30 of the SDRAM chip 40, described in the reference as being driven by two different clocks.

Petitioner presents no persuasive or credible explanation or disclosure to support this way of reading Fukuzo on the claim language. Alternately, if the Petitioner reads the volatile memory subsystem to be chip 40 as a whole, then it does not appear the chip "operates" at the frequency of flash clock 310, but rather at the frequency of the system clock 110. *See* Prelim. Resp. 21. Nonetheless, Petitioner does not explain its reading of two different clocks which drive different sets of components as corresponding to the clock for the single volatile memory subsystem of the claim.

The claim language must be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Sneed*, 710 F.2d 1544, 1548, (Fed. Cir. 1983). While it would be unreasonable to ignore any interpretive guidance afforded by the specification, *see In re Morris*, 127 F.3d 1048, 1054–55, (Fed. Cir. 1997), it is improper to read limitations from the specification into the claims. *Id.* For example, the specification of the

’833 patent discloses only one bank of volatile memory devices 32. Ex. 1001, Fig. 1. The Specification of the ’833 patent discloses only one clock input into the volatile memory subsystem and does not suggest that there are subsections of the volatile memory subsystem that are operating at different clock frequencies. *Id.* at col. 15, l. 41–col. 17, l. 38.

Additionally, the specification suggests “[r]unning the volatile memory subsystem 30 at the reduced frequency during a backup and/or restore operation may advantageously reduce overall power consumption of the memory system 10.” *Id.* at col. 16, ll. 34–37. Petitioner’s reading of two separate sections of memory on the volatile memory subsystem is not consistent with the goal of reducing overall power consumption because the memory that Petitioner points to as running at a reduced frequency (flash/input output buffer 390) is not the same memory that is accessed by the host system (SDRAM array 190). Thus, on the record before us, Petitioner has not shown sufficiently that Fukuzo discloses the limitations to “operating the volatile memory subsystem at a third clock frequency . . . the third clock frequency being less than the first clock frequency” and “the volatile memory subsystem further being operable at a third clock frequency . . . the third clock frequency being less than the clock first frequency,” as recited in independent claims 1 and 15.

Thus, upon review of Petitioner’s analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 1 and 15, or claims 2, 6, 8, 11, 12, 18, 22, 24, 27, and 28 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Fukuzo.

C. Claims 1–6, 8, 11–13, 15, 17–22, 24, and 27–29 — Anticipated by Panabaker (Ex. 1014)

Petitioner argues that claims 1–6, 8, 11–13, 15, 17–22, 24, and 27–29 are anticipated by Panabaker under 35 U.S.C. § 102(e). Pet. 9–17. Panabaker discloses a hybrid memory device comprising a memory controller, a volatile memory (e.g. SDRAM) and nonvolatile memory (e.g. flash memory). *See e.g.*, Ex. 1014, Abstract, Fig. 3A, col. 7, ll. 8–11. Panabaker's memory controller operates such that the memory device has only a single memory interface with respect to voltage and access protocols defined for one type of memory. *Id.* Panabaker teaches that the memory controller allows access to both SDRAM (volatile memory) and non-volatile memory, with the non-volatile memory overlaid in one or more designated blocks of the volatile memory address space (or vice-versa). *Id.* In Panabaker, a host is coupled to the controller of the hybrid memory device, where the controller either allows a direct access to the volatile memory or uses a buffer for speed matching between the host and the nonvolatile memory. *Id.*

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Claim 15 recites "the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency."

Petitioner asserts that Panabaker's disclosure of SDRAM buffer set 210 as the volatile memory subsystem "is at least as fast as a given SDRAM

chip and its protocol requires . . . " meets the limitation to a first clock frequency. Pet. 19 (citing Ex. 1014, col. 4, ll. 33–47). Further, Petitioner asserts that Panabaker's disclosure of speed matching buffer set as volatile memory subsystem meets the limitation to a first clock frequency. Pet. 20 (citing Ex. 1013 ¶¶ 84, 87–88). We are not persuaded by this cited disclosure.

Petitioner apparently reads the controller 308A and the buffer 310 and the SDRAM 304 on the volatile memory subsystem in the first mode. However, in the second mode, Petitioner is unclear whether it reads the volatile memory subsystem on the controller 308A or the speed matching buffer 310. Reading the controller as the volatile memory subsystem is inconsistent with specification which discloses a controller 62 that is separate from the volatile and non-volatile memory subsystems. Ex. 1001, Fig. 1. The controller 62 provides the clock signal to the volatile and nonvolatile memory subsystems. Ex. 1001, Fig. 6. As Patent Owner points out, Petitioner does not sufficiently explain what it considers the volatile memory subsystem and does not point to any clock which provides a first or third frequency to that subsystem. *See* Prelim. Resp. 28–29.

Petitioner does not specify that Panabaker teaches that the speed matching buffer operates at a third clock frequency. For example, Panabaker teaches that a firmware protocol is used for speed matching. *See e.g.*, Ex. 1014, 6:32–36 ("As can be readily appreciated, because SDRAM is presently one or more orders of magnitude faster than flash, the protocol includes a way for the controller 308A to signal to the firmware 330 when a flash read or write request is busy and when the request is ready."). Petitioner does not explain how this scheme amounts to operating the speed

matching buffer at a third clock frequency. We find that one of ordinary skill at the time of the invention reasonably would not consider Panabaker as disclosing a volatile memory subsystem that operates at the first and third clock frequencies. Thus, on the record before us, Petitioner has not shown sufficiently that Panabaker discloses these limitations.

Therefore, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 1 and 15, and claims 2–6, 8, 11–13, 17–22, 24, and 27–29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Panabaker.

D. Obviousness Grounds

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Based on the arguments and evidence presented by Petitioner, we are unpersuaded that it has established a reasonable likelihood that it would prevail in showing the unpatentability of any of the challenged claim under

35 U.S.C. § 103 as obvious over a combination relying on either Fukuzo or Panabaker.

As discussed above in the context of the anticipation analysis with regard to Fukuzo and Panabaker, Petitioner has not shown sufficiently that Fukuzo or Panabaker discloses a volatile memory subsystem that operates at a third frequency, as is required by each of independent claims 1 and 15. Additionally, Petitioner does not provide any further explanation why Fukuzo or Panabaker disclose a volatile memory subsystem that operates at a third frequency under an obviousness analysis. Each of Petitioner's obviousness grounds assumes that either Fukuzo or Panabaker discloses that limitation. Pet. 7–9. Petitioner bears the burden of proof of showing that limitation for each independent claim. Nonetheless, as shown above, none of the challenges relied on to meet claims 1 and 15 has shown sufficiently the required "third frequency."

Thus, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to: the ground that claims 3 and 19 are unpatentable over Fukuzo and Li; the ground that claims 3 and 19 are unpatentable over Fukuzo, Li, and Spiers; the ground that claims 7 and 23 are unpatentable over Fukuzo and Hansen; the ground that claims 7, 9, 10, 23, 25, and 26 are unpatentable over Fukuzo, Li, and Hansen; the ground that claims 14 and 30 are unpatentable over Fukuzo and Sun; the ground that claims 14 and 30 are unpatentable over Fukuzo, Li, and Sun; the ground that claim 16 is unpatentable over Fukuzo and Komatsuzaki; the ground that claim 16 is unpatentable over Fukuzo, Li, and Komatsuzaki; the ground that claims 1–6, 8, 11, 12, 15, 17–22, 24, 27, and 28 are unpatentable over

Panabaker and Li; the ground that claims 3 and 19 are unpatentable over Panabaker and Spiers; the ground that claims 3 and 19 are unpatentable over Panabaker, Li, and Spiers; the ground that claims 7, 9, 23, and 25 are unpatentable over Panabaker and Hansen; the ground that claims 7, 9, 10, 23, 25, and 26 are unpatentable over Panabaker, Li, and Hansen; the ground that claims 13 and 29 are unpatentable over Panabaker and Fukuzo; the ground that claims 13 and 29 are unpatentable over Panabaker, Li, and Fukuzo; the ground that claims 14 and 30 are unpatentable over Panabaker and Sun; the ground that claims 14 and 30 are unpatentable over Panabaker, Li, and Sun; the ground that claim 16 is unpatentable over Panabaker and Komatsuzaki; the ground that claim 16 is unpatentable over Panabaker, Li, and Komatsuzaki.

III. CONCLUSION

The information presented does not show that there is a reasonable likelihood that Petitioner would prevail at trial with respect to at least one claim of the ’833 patent, based on any ground presented in the petition. On this record, we deny the petition for *inter partes* review of claims 1–30.

IV. ORDER

Accordingly, it is

ORDERED that that the petition is *denied* as to all challenged claims, and no trial is instituted.

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